ANALOG DEVICES

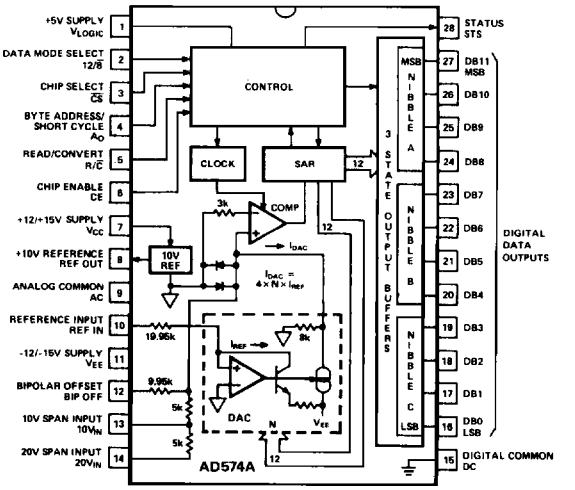
Complete 12-Bit A/D Converter

AD574A*

FEATURES

- Complete 12-Bit A/D Converter with Reference and Clock
- 8- and 16-Bit Microprocessor Bus Interface
- Guaranteed Linearity Over Temperature
  - 0 to +70°C – AD574AJ, K, L
  - −55°C to +125°C – AD574AS, T, U
- No Missing Codes Over Temperature
- 35μs Maximum Conversion Time
- Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10ppm/°C max AD574AL 12.5ppm/°C max AD574AU
- Ceramic DIP, Plastic DIP or PLCC Package
- Available in Higher Speed, Pinout-Compatible Versions (15μs AD674B, 8μs AD774B; 10μs (with SHA) AD1674)
- Available in Versions Compliant with MIL-STD-883 and JAN QPL.

BLOCK DIAGRAM AND PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8- or 16-bit microprocessor bus. A high-precision voltage reference and clock are included on-chip, and the circuit guarantees full-rated performance without external circuitry or clock signals.

The AD574A design is implemented using Analog Devices' Bipolar/I^2L process, and integrates all analog and digital functions on one chip. Offset, linearity and scaling errors are minimized by active laser-trimming of thin-film resistors at the wafer stage. The voltage reference uses an implanted buried Zener for low noise and low drift. On the digital side, I^2L logic is used for the successive-approximation register, control circuitry and 3-state output buffers.

The AD574A is available in six different grades. The AD574AJ, K, and L grades are specified for operation over the 0 to +70°C temperature range. The AD574AS, T, and U are specified for the −55°C to +125°C range. All grades are available in a 28-pin hermetically-sealed ceramic DIP. Also, the J, K, and L grades are available in a 28-pin plastic DIP and PLCC, and the J and K grades are available in ceramic LCC.

The S, T, and U grades in ceramic DIP or LCC are available with optional processing to MIL-STD-883C Class B; the T and U grades are available as JAN QPL. The Analog Devices' Military Products Databook should be consulted for details on /883B testing of the AD574A.

PRODUCT HIGHLIGHTS

1. The AD574A interfaces to most 8- or 16-bit microprocessors. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 and 0 to +20 volts unipolar, −5 to +5 and −10 to +10 volts bipolar. Typical bipolar offset and full-scale calibration errors of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried Zener reference is trimmed to 10.00 volts with 0.2% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 1.5mA beyond the requirements of the reference and bipolar offset resistors.
4. AD674B (15μs) and AD774B (8μs) provide higher speed, pin compatibility; AD1674 (10μs) includes on-chip Sample-Hold Amplifier (SHA).

*Protected by U.S. Patent Nos. 3,803,590; 4,213,806; 4,511,413; RE 28,633.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise noted)

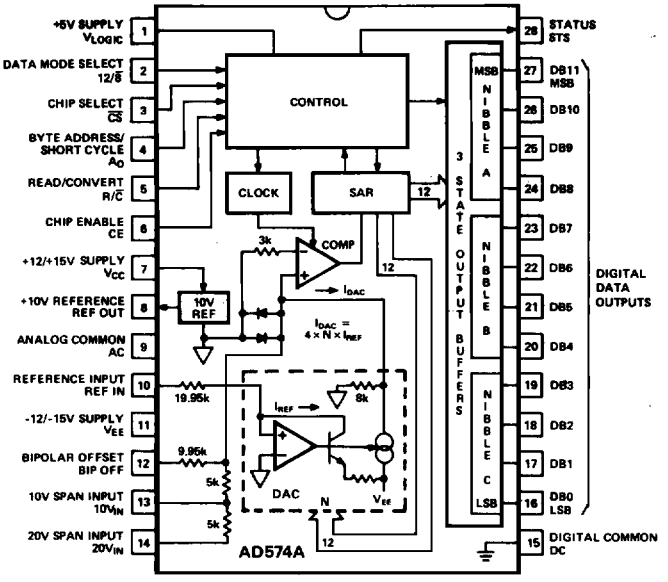
Model	AD574AJ Min	AD574AJ Typ	AD574AJ Max	AD574AK Min	AD574AK Typ	AD574AK Max	AD574AL Min	AD574AL Typ	AD574AL Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR @ +25°C			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1/2			±1/2	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)										
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to zero)			±2			±1			±1	LSB
BIPOLAR OFFSET (Adjustable to zero)			±4			±4			±2	LSB
FULL-SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero)			0.25			0.25			0.125	% of F.S.
TEMPERATURE RANGE	0		+70	0		+70	0		+70	°C
TEMPERATURE COEFFICIENTS (Using internal reference)										
T_{min} to T_{max}										
Unipolar Offset			±2 (10)			±1 (5)			±1 (5)	LSB (ppm/°C)
Bipolar Offset			±2 (10)			±1 (5)			±1 (5)	LSB (ppm/°C)
Full-Scale Calibration			±9 (50)			±5 (27)			±2 (10)	LSB (ppm/°C)
POWER SUPPLY REJECTION										
Max change in Full Scale Calibration										
V_{CC} = 15V ± 1.5V or 12V ± 0.6V			±2			±1			±1	LSB
V_{LOGIC} = 5V ± 0.5V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15V ± 1.5V or −12V ± 0.6V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS[1] (T_{min}–T_{max})										
Inputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0)										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−20		+20	20		+20	−20		+20	μA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage ($I_{SOURCE} \leq 500\mu A$)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage ($I_{SINK} \leq 1.6mA$)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.98	10.0	10.02	9.98	10.0	10.02	9.99	10.0	10.01	Volts
Output current (available for external loads)[3] (External load should not change during conversion)			1.5			1.5			1.5	mA
PACKAGE OPTIONS[4]										
Ceramic (D-28)		AD574ASD			AD574AKD			AD574ALD		
Plastic (N-28)		AD574AJN			AD574AKN			AD574ALN		
PLCC (P-28A)		AD574AJP			AD574AKP			AD574ALP		
LCC (E-28A)		AD574AJE			AD574AKE					

NOTES
[1]Detailed Timing Specifications appear in the Timing Section.
[2]12/$\overline{8}$ Input is not TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.
[3]The reference should be buffered for operation on ± 12V supplies.
[4]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.
Specifications subject to change without notice.

Model	AD574AS Min	AD574AS Typ	AD574AS Max	AD574AT Min	AD574AT Typ	AD574AT Max	AD574AU Min	AD574AU Typ	AD574AU Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR @ +25°C			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1			±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)										
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to zero)			±2			±1			±1	LSB
BIPOLAR OFFSET (Adjustable to zero)			±4			±4			±2	LSB
FULL-SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero)			0.25			0.25			0.125	% of F.S.
TEMPERATURE RANGE	−55		+125	−55		+125	−55		+125	°C
TEMPERATURE COEFFICIENTS (Using internal reference)										
T_{min} to T_{max}										
Unipolar Offset			±2(5)			±1(2.5)			±1(2.5)	LSB (ppm/°C)
Bipolar Offset			±4(10)			±2(5)			±1(2.5)	LSB (ppm/°C)
Full-Scale Calibration			±20(50)			±10(25)			±5(12.5)	LSB (ppm/°C)
POWER SUPPLY REJECTION										
Max change in Full Scale Calibration										
V_{CC} = 15V ±1.5V or 12V ±0.6V			±2			±1			±1	LSB
V_{LOGIC} = 5V ±0.5V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15V ±1.5V or −12V ±0.6V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS[1] (T_{min}–T_{max})										
Inputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0)										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage ($I_{SOURCE} \leq 500\mu A$)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage ($I_{SINK} \leq 1.6mA$)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.98	10.0	10.02	9.98	10.0	10.02	9.99	10.0	10.01	Volts
Output current (available for external loads)[3] (External load should not change during conversion)			1.5			1.5			1.5	mA
PACKAGE OPTIONS[4]										
Ceramic (D-28)		AD574ASD			AD574ATD			AD574AUD		

NOTES
[1]Detailed Timing Specifications appear in the Timing Section.
[2]12/$\overline{8}$ Input is not TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.
[3]The reference should be buffered for operation on ±12V supplies.
[4]D = Ceramic DIP. For outline information see Package Information section.

Specifications subject to change without notice.



AD574A Block Diagram and Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common . . . . . 0 to +16.5V
V_{EE} to Digital Common . . . . . 0 to −16.5V
V_{LOGIC} to Digital Common . . . . . 0 to +7V
Analog Common to Digital Common . . . . . ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common . . −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to
Analog Common . . . . . V_{EE} to V_{CC}
$20V_{IN}$ to Analog Common . . . . . ±24V
REF OUT . . . . . Indefinite short to common
Momentary short to V_{CC}

Chip Temperature . . . . . 175°C
Power Dissipation 825mW
Lead Temperature, Soldering . . . . . +300°C, 10 sec.
Storage Temperature (Ceramic) . . . . . −65°C to +150°C
(Plastic) . . . . . −25°C to +100°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error Max (T_{min} to T_{max})	Resolution No Missing Codes (T_{min} to T_{max})	Max Full Scale T.C. (ppm/°C)
AD574AJ(X)	0 to +70°C	±1LSB	11 Bits	50.0
AD574AK(X)	0 to +70°C	±1/2LSB	12 Bits	27.0
AD574AL(X)	0 to +70°C	±1/2LSB	12 Bits	10.0
AD574AS(X)[2]	−55°C to +125°C	±1LSB	11 Bits	50.0
AD574AT(X)[2]	−55°C to +125°C	±1LSB	12 Bits	25.0
AD574AU(X)[2]	−55°C to +125°C	±1LSB	12 Bits	12.5

NOTES
[1]X = Package designator. Available packages are:
D (D-28) for all grades.
E (E-28A) for J and K grades and /883B processed S, T and U grades.
N (N-28) for J, K, and L grades.
P (P-28A) for PLCC in J, K grades.
Example: AD574AKN is K grade in plastic DIP.
[2]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices Military Products Databook.