FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-29125-1E

Spread Spectrum Clock Generator

MB88152A

MB88152A-100/101/102/110/111/112

■ DESCRIPTION

MB88152A is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator. It corresponds to both of the center spread which modulates input frequency as Middle Centered and down spread which modulates so as not to exceed input frequency.

■ FEATURES

- Input frequency : 16.6 MHz to 134 MHz
- Output frequency : 16.6 MHz to 134 MHz
- Modulation rate : ± 0.5%, ± 1.5% (Center spread), – 1.0%, – 3.0% (Down spread)
- Equipped with oscillation circuit: Range of oscillation 16.6 MHz to 48 MHz
- Modulation clock output Duty : 40% to 60%
- Modulation clock Cycle-Cycle Jitter : Less than 100 ps
- Low current consumption by CMOS process : 5 mA (24 MHz : Typ-sample, no load)
- Power supply voltage : 3.3 V ± 0.3 V
- Operating temperature : – 40 °C to +85 °C
- Package : SOP 8-pin

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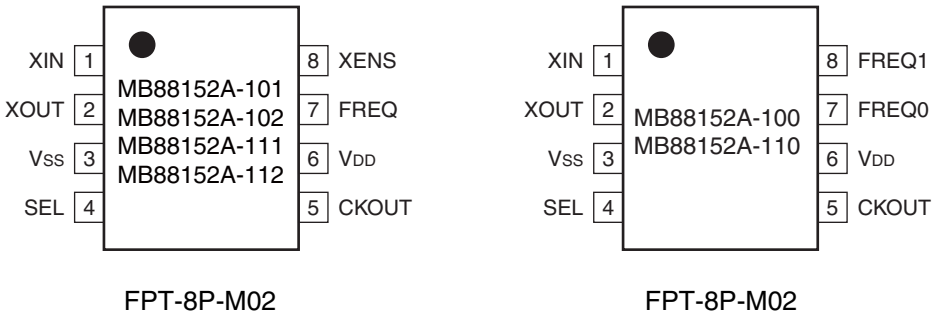
■ PRODUCT LINE-UP

MB88152A has three kinds of input frequency, and two kinds of modulation type (center/down spread), total six line-ups.

Product	Input/Output Frequency	Modulation type	Modulation enable pin
MB88152A-100	16.6 MHz to 134 MHz	Down spread	No
MB88152A-101	16.6 MHz to 67 MHz		Yes
MB88152A-102	40 MHz to 134 MHz		
MB88152A-110	16.6 MHz to 134 MHz	Center spread	No
MB88152A-111	16.6 MHz to 67 MHz		Yes
MB88152A-112	40 MHz to 134 MHz		

■ PIN ASSIGNMENT

TOP VIEW

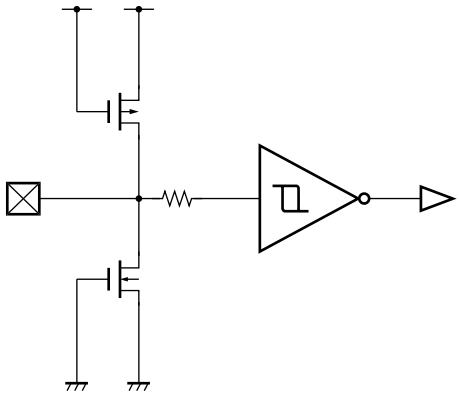
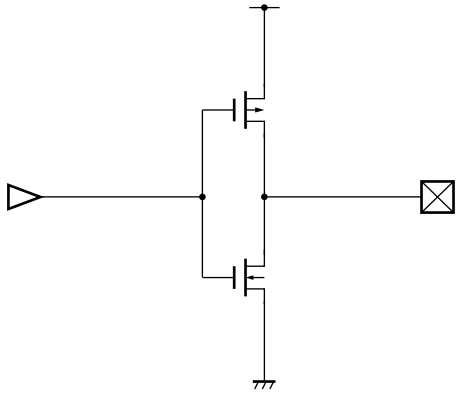


FPT-8P-M02 FPT-8P-M02

■ PIN DESCRIPTION

Pin name	I/O	Pin no.	Description
XIN	I	1	Crystal resonator connection pin/clock input pin
XOUT	O	2	Crystal resonator connection pin
V_{SS}	—	3	GND pin
SEL	I	4	Modulation rate setting pin
CKOUT	O	5	Modulated clock output pin
V_{DD}	—	6	Power supply voltage pin
FREQ/FREQ0	I	7	Frequency setting pin
XENS/FREQ1	I	8	Modulation enable setting pin/frequency setting pin

■ I/O CIRCUIT TYPE

Pin	Circuit type	Remarks
SEL FREQ FREQ0 FREQ1 XENS		CMOS hysteresis input
CKOUT		• CMOS output • I_{OL} = 4 mA

Note : For XIN and XOUT pins, refer to “■OSCILLATION CIRCUIT”.

■ HANDLING DEVICES

Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than V_{DD} or a voltage lower than V_{SS} is applied to an input or output pin or (b) a voltage higher than the rating is applied between V_{DD} and V_{SS}. The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

Unused output pin should be opened.

The attention when the external clock is used

Input the clock to XIN pin, and XOUT pin should be opened when you use the external clock.

Please pay attention so that an overshoot and an undershoot do not occur to an input clock of XIN pin.

Power supply pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

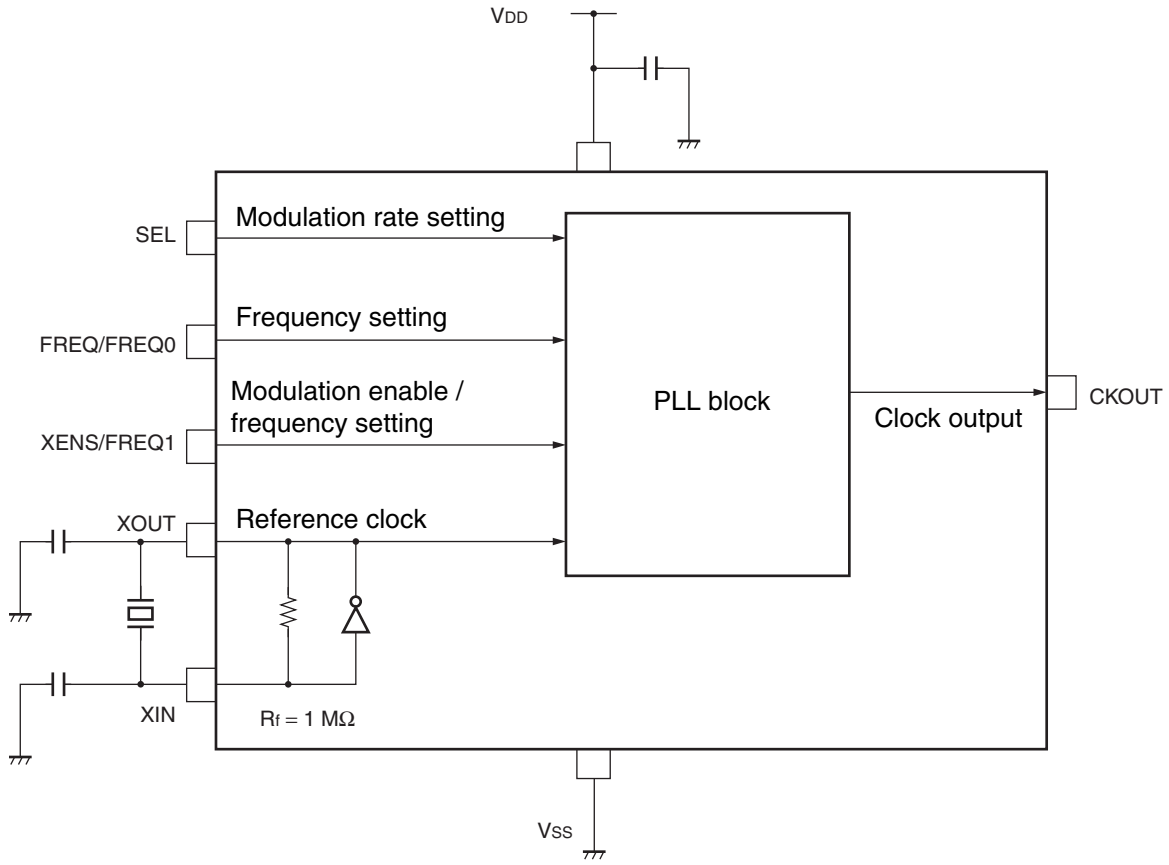
We recommend connecting electrolytic capacitor (about 10 μF) and the ceramic capacitor (about 0.01 μF) in parallel between V_{SS} and V_{DD} near the device, as a bypass capacitor.

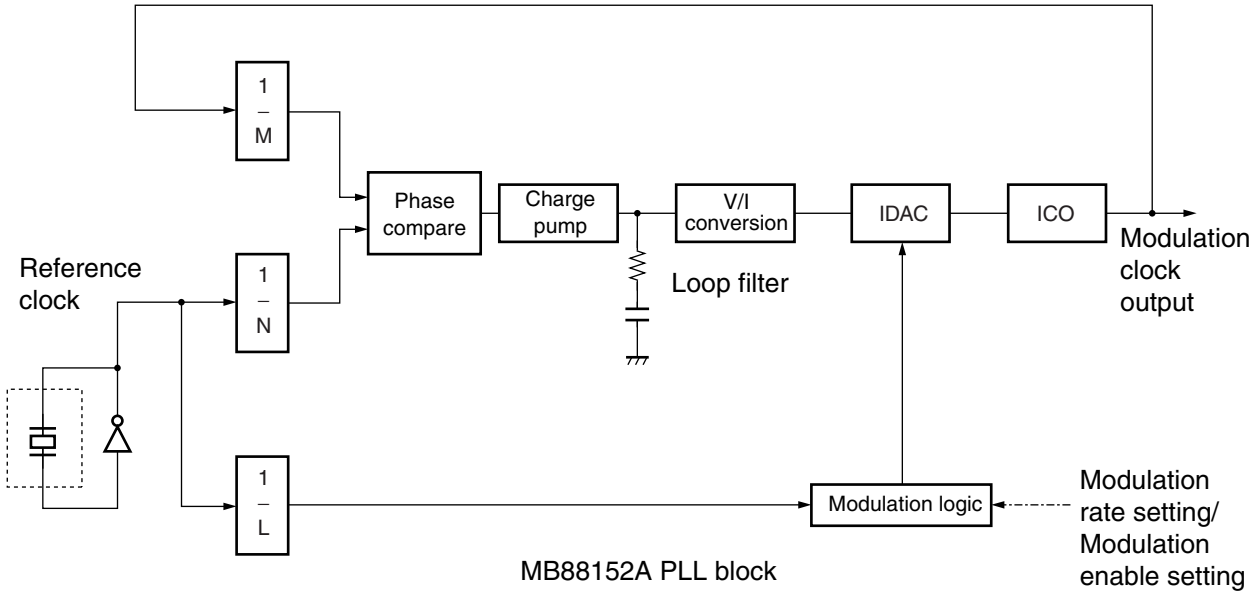
Oscillation Circuit

Noise near the XIN and XOUT pins may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN or XOUT pin and resonator (or ceramic oscillator) do not intersect other wiring.

Design the printed circuit board that surrounds the XIN and XOUT pins with ground.

■ BLOCK DIAGRAM





MB88152A PLL block

A glitchless IDAC (current output D/A converter) provides precise modulation, thereby dramatically reducing EMI.

■ PIN SETTING

When changing the pin setting, the stabilization wait time for the modulation clock is required. The stabilization wait time for the modulation clock takes the maximum value of Lock-Up time in "■ ELECTRICAL CHARACTERISTICS • AC characteristics Lock-Up time".

Modulation enable setting

XENS	Modulation	
L	Modulation	MB88152A-101, 102, 111, 112
H	No modulation	

Note : MB88152A-100 and 110 do not have XENS pin.

SEL modulation rate setting

SEL	Modulation rate		Remarks
L	± 0.5%	MB88152A-110, 111, 112	Center spread
	− 1.0%	MB88152A-100, 101, 102	Down spread
H	± 1.5%	MB88152A-110, 111, 112	Center spread
	− 3.0%	MB88152A-100, 101, 102	Down spread

Note : The modulation rate can be changed at the level of the terminal.

Frequency setting

FREQ	Frequency	
L	16.6 MHz to 40 MHz	MB88152A-101, 111
	40 MHz to 80 MHz	MB88152A-102, 112
H	33 MHz to 67 MHz	MB88152A-101, 111
	66 MHz to 134 MHz	MB88152A-102, 112

Note : MB88152A-100 and 110 do not have FREQ pin.

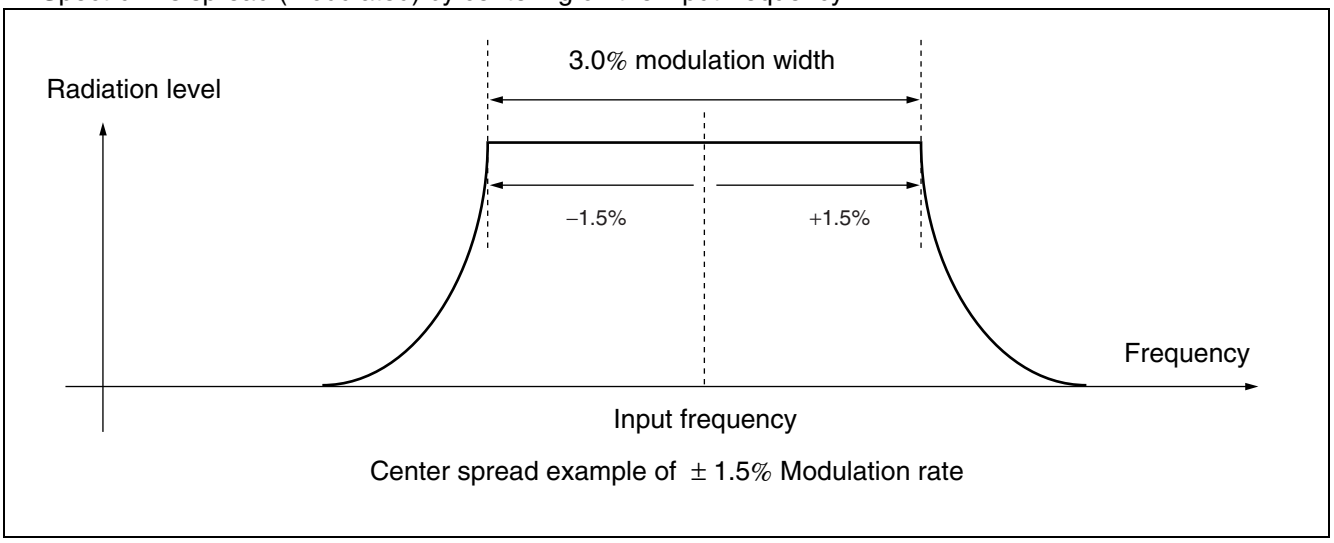
Frequency setting

FREQ1	FREQ0	Frequency	
L	L	16.6 MHz to 40 MHz	MB88152A-100, 110
L	H	33 MHz to 67 MHz	
H	L	40 MHz to 80 MHz	
H	H	66 MHz to 134 MHz	

Note : MB88152A-101, 111, 102 and 112 have neither FREQ0 pin nor FREQ1 pin.

• Center spread

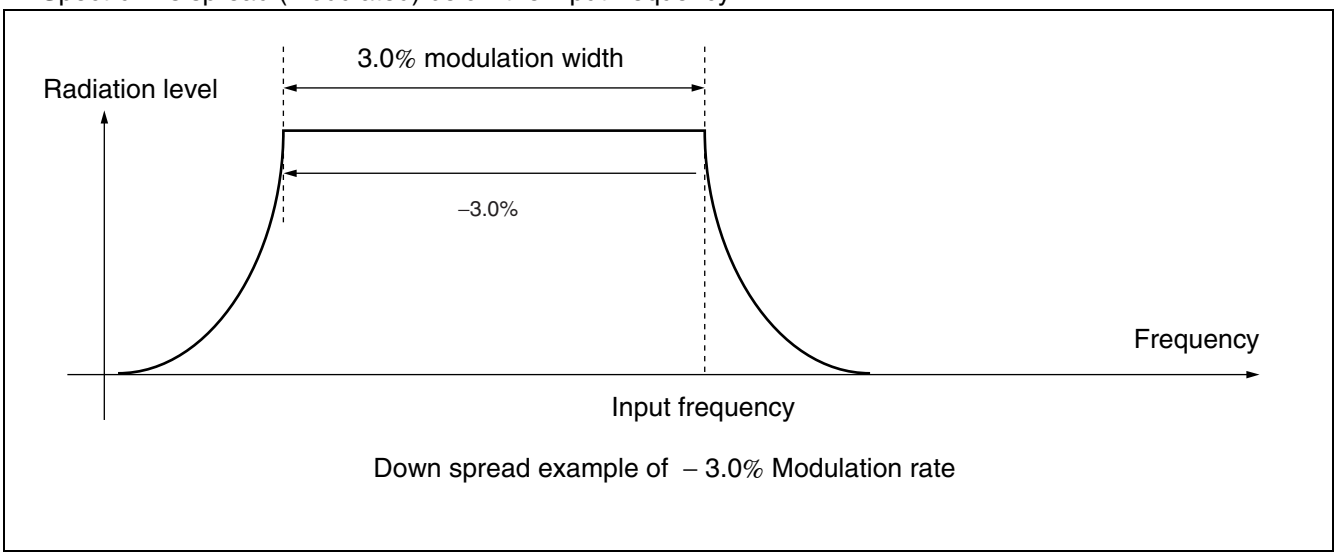
Spectrum is spread (modulated) by centering on the input frequency.



Center spread example of ± 1.5% Modulation rate

• Down spread

Spectrum is spread (modulated) below the input frequency.



Down spread example of – 3.0% Modulation rate

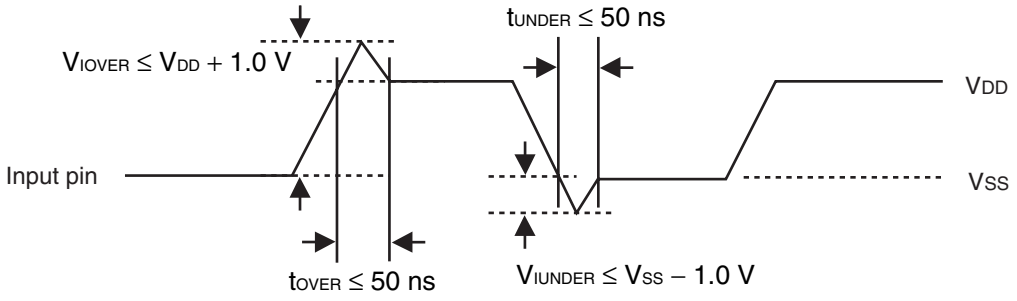
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 4.0	V
Input voltage*	V_I	V_{SS} − 0.5	V_{DD} + 0.5	V
Output voltage*	V_O	V_{SS} − 0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	− 55	+ 125	°C
Operation junction temperature	T_J	− 40	+ 125	°C
Output current	I_O	− 14	+ 14	mA
Overshoot	V_{IOVER}	—	V_{DD} + 1.0 (t_{OVER} ≤ 50 ns)	V
Undershoot	V_{IUNDER}	V_{SS} − 1.0 (t_{UNDER} ≤ 50 ns)	—	V

* : The parameter is based on V_{SS} = 0.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot



■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0.0 V)

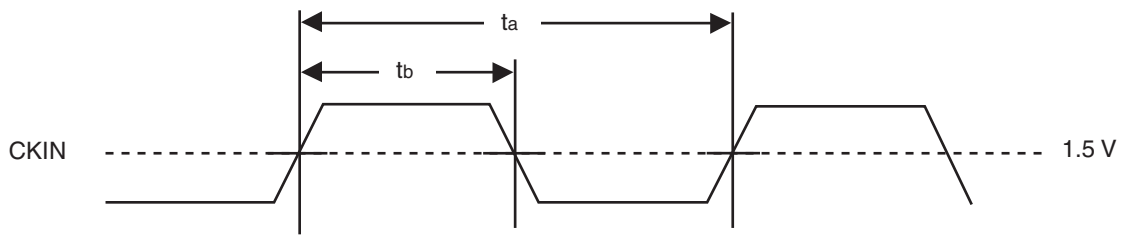
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{DD}	V_{DD}	—	3.0	3.3	3.6	V
"H" level input voltage	V_{IH}	SEL, FREQ/FREQ0, XENS/FREQ1	—	$V_{DD} \times 0.8$	—	$V_{DD} + 0.3$	V
		XIN	Input through rate 3 V / ns 16.6 MHz to 100 MHz	$V_{DD} \times 0.8$	—	$V_{DD} + 0.3$	V
			Input through rate 3 V / ns 100 MHz to 134 MHz	$V_{DD} \times 0.9$	—	$V_{DD} + 0.3$	V
"L" level input voltage	V_{IL}	SEL, FREQ/FREQ0, XENS/FREQ1	—	V_{SS}	—	$V_{DD} \times 0.2$	V
		XIN	Input through rate 3 V / ns 16.6 MHz to 100 MHz	V_{SS}	—	$V_{DD} + 0.2$	V
			Input through rate 3 V / ns 100 MHz to 134 MHz	V_{SS}	—	$V_{DD} + 0.1$	V
Input clock duty cycle	t_{DCI}	XIN	16.6 MHz to 100 MHz	40	50	60	%
			100 MHz to 134 MHz	45	50	55	
Operating temperature	Ta	—	—	−40	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_b/t_a$)



■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

(Ta = –40 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

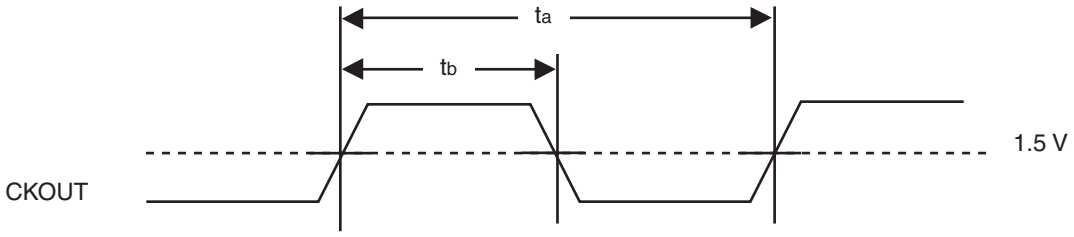
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	V_{DD}	24 MHz output No load capacitance	—	5.0	7.0	mA
Output voltage	V_{OH}	CKOUT	"H" level output I_{OH} = – 4 mA	V_{DD} – 0.5	—	V_{DD}	V
	V_{OL}		"L" level output I_{OL} = 4 mA	V_{SS}	—	0.4	V
Output impedance	Z_O	CKOUT	16.6 MHz to 134 MHz	—	45	—	Ω
Input capacitance	C_{IN}	XIN, SEL, FREQ/FREQ0, XENS/FREQ1	Ta = + 25 °C V_{DD} = V_I = 0.0 V f = 1 MHz	—	—	16	pF
Load capacitance	C_L	CKOUT	16.6 MHz to 67 MHz	—	—	15	pF
			67 MHz to 100 MHz	—	—	10	
			100 MHz to 134 MHz	—	—	7	

• AC Characteristics

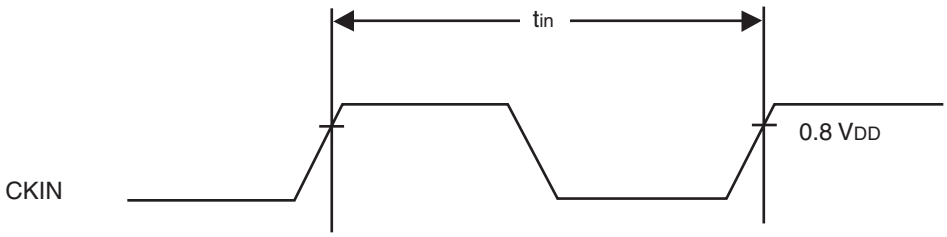
(Ta = –40 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Oscillation frequency	f_x	XIN, XOUT	Fundamental oscillation	16.6	—	40	MHz
			3rd over tone	40	—	48	
Input frequency	f_{in}	XIN	MB88152A-100, 110	16.6	—	134	MHz
			MB88152A-101, 111	16.6	—	67	
			MB88152A-102, 112	40	—	134	
Output frequency	f_{OUT}	CKOUT	MB88152A-100, 110	16.6	—	134	MHz
			MB88152A-101, 111	16.6	—	67	
			MB88152A-102, 112	40	—	134	
Output slew rate	SR	CKOUT	0.4 V to 2.4 V Load capacitance 15 pF	0.4	—	4.0	V/ns
Output clock duty cycle	t_{DCC}	CKOUT	1.5 V	40	—	60	%
Modulation cycle	f_{MOD}	CKOUT	—	—	12.5	—	kHz
Lock-Up time	t_{LK}	CKOUT	—	—	2	5	ms
Cycle-cycle jitter	t_{JC}	CKOUT	No load capacitance, Ta = + 25 °C, V_{DD} = 3.3 V, Standard deviation σ	—	—	100	ps

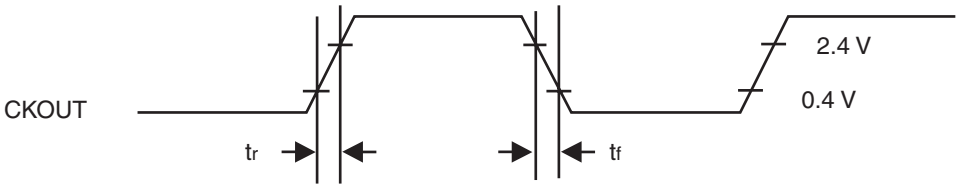
■ OUTPUT CLOCK DUTY CYCLE ($t_{DCC} = t_b/t_a$)



■ INPUT FREQUENCY ($f_{in} = 1/t_{in}$)

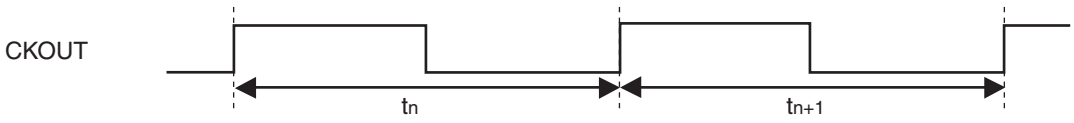


■ OUTPUT SLEW RATE (SR)



Note : SR = (2.4–0.4) /t_r, SR = (2.4–0.4) /t_f

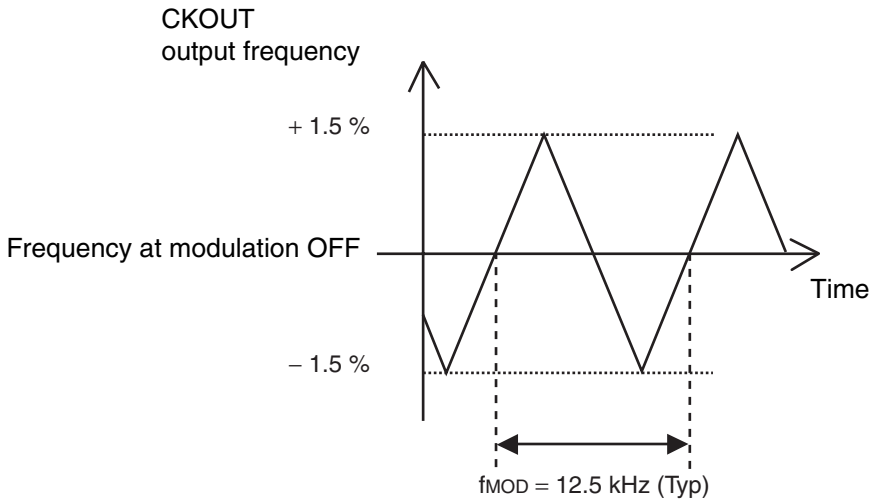
■ CYCLE-CYCLE JITTER ($t_{JC} = | t_n - t_{n+1} |$)



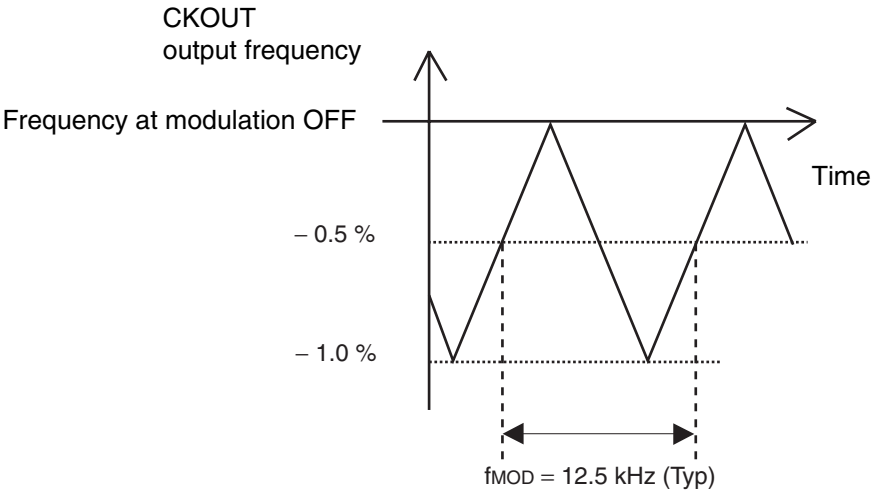
Note : Cycle-cycle jitter is defined the difference between a certain cycle and immediately after (or, immediately before) .

■ MODULATION WAVEFORM

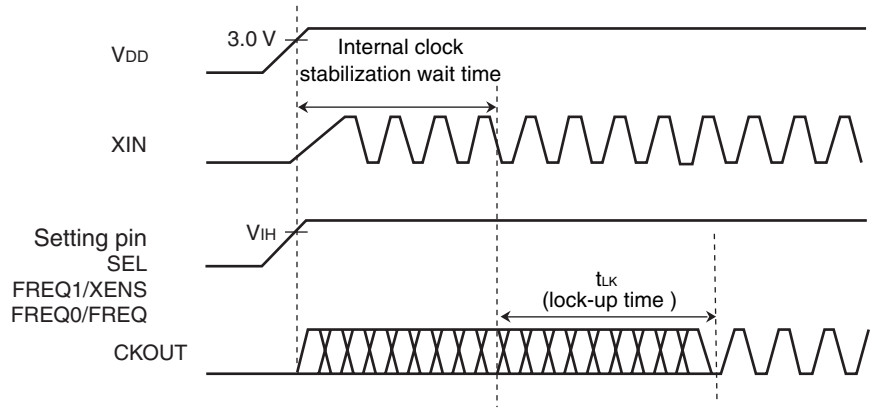
• ±1.5% modulation rate, Example of center spread



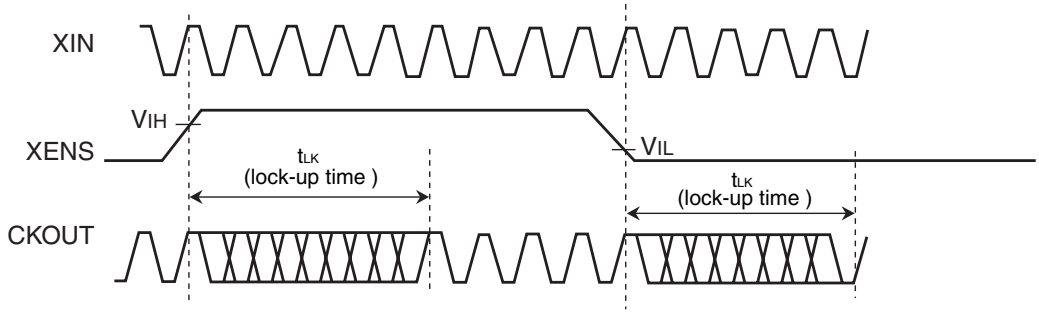
• –1.0% modulation rate, Example of down spread



■ LOCK-UP TIME



If the setting pin is fixed at the “H” or “L” level, the maximum time after the power is turned on until the set clock signal is output from CKOUT pin is (the stabilization wait time of input clock to XIN pin) + (the lock-up time “t_{LK}”). For the input clock stabilization time, check the characteristics of the resonator or oscillator used.



For modulation enable control using the XENS pin during normal operation, the set clock signal is output from CKOUT pin at most the lock-up time (t_{LK}) after the level at the XENS pin is determined.

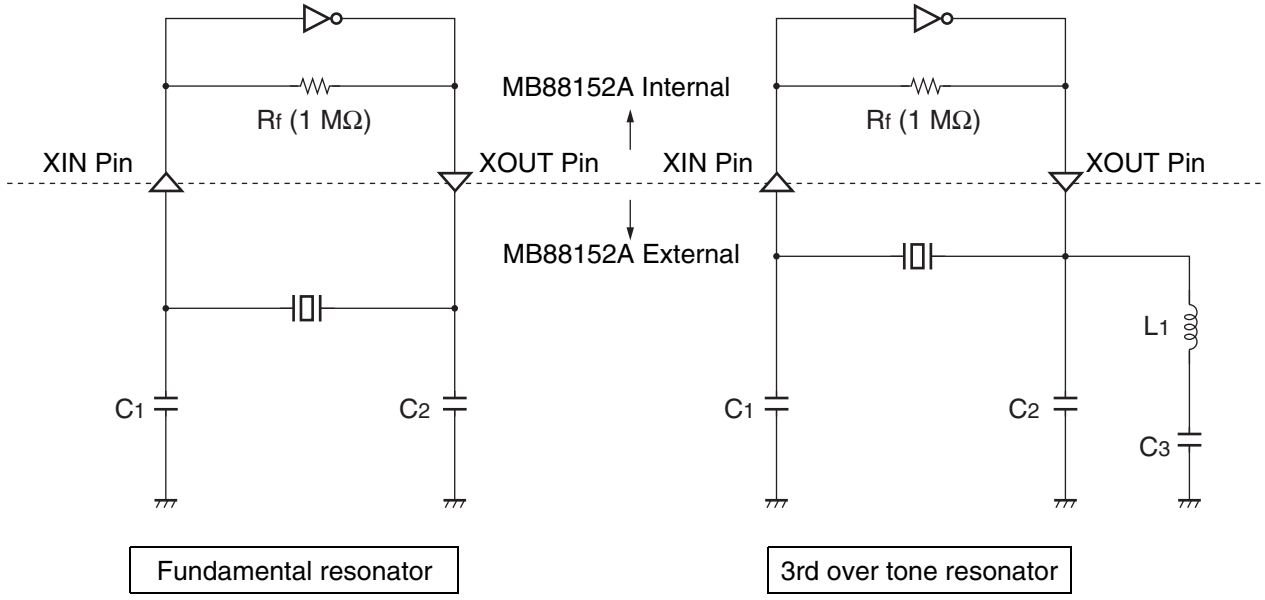
Note : When the pin setting is changed, the CKOUT pin output clock stabilization time is required. Until the output clock signal becomes stable, the output frequency, output clock duty cycle, modulation period, and cycle-cycle jitter cannot be guaranteed. It is therefore advisable to perform processing such as cancelling a reset of the device at the succeeding stage after the lock-up time.

■ OSCILLATION CIRCUIT

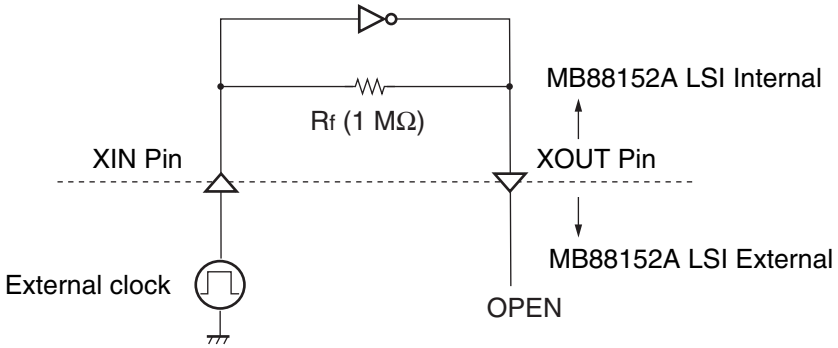
The left side of figures below shows the connection example about general resonator. The oscillation circuit has the built-in feedback resistance (1 MΩ). The value of capacity (C_1 and C_2) is required adjusting to the most suitable value of an individual resonator.

The right side of figures below shows the example of connecting for the 3rd over-tone resonator. The value of capacity (C_1, C_2 and C_3) and inductance (L_1) is needed adjusting to the most suitable value of an individual resonator. The most suitable value is different by individual resonator. Please refer to the resonator manufacturer which you use for the most suitable value. When an external clock is used (the resonator is not used), input the clock to XIN pin and do not connect anything with XOUT pin.

• When using the resonator

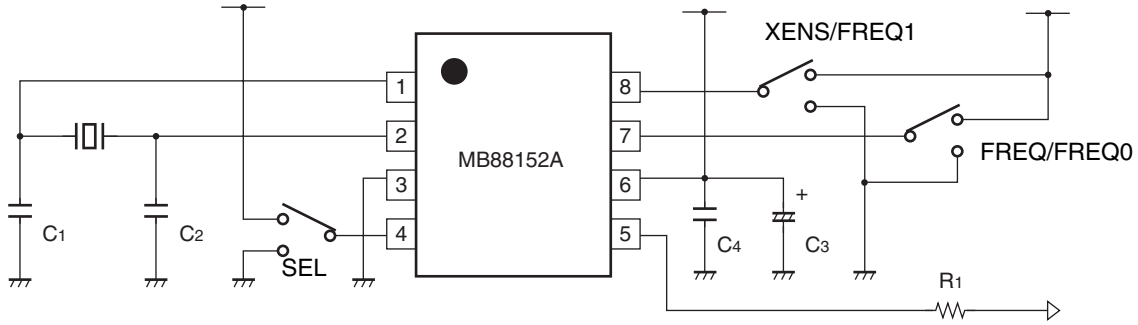


• When using an external clock



Note : Note that a jitter characteristic of an input clock may cause an affect a cycle-cycle jitter characteristic.

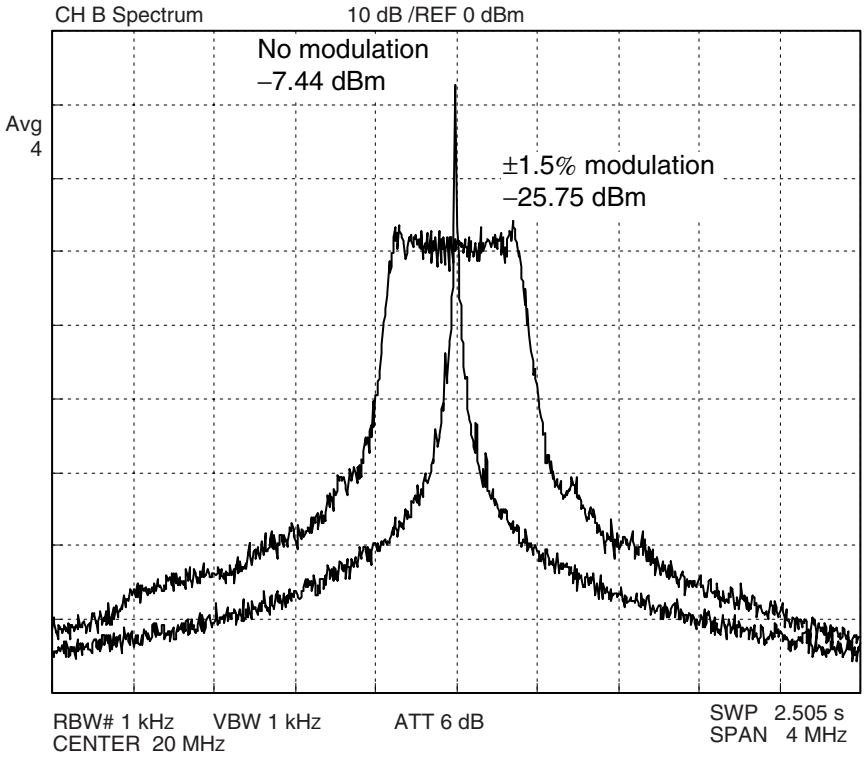
■ INTERCONNECTION CIRCUIT EXAMPLE



C_1, C_2 : Oscillation stabilization capacitance (refer to "■ OSCILLATION CIRCUIT".)
C_3 : Capacitor of 10 μF or higher
C_4 : Capacitor about 0.01 μF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device.)
R_1 : Impedance matching resistor for board pattern

■ EXAMPLE CHARACTERISTICS

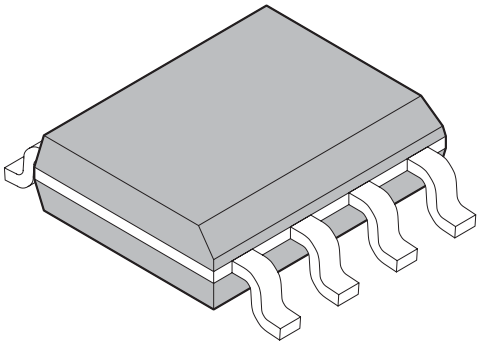
The condition of the examples of the characteristics is shown as follows : Input frequency = 20 MHz (Output frequency = 20 MHz : Use for MB88152A-111)
Power-supply voltage = 3.3 V, None load capacity, Modulation rate = ±1.5% (center spread) .
Spectrum analyzer HP4396B is connected with CKOUT. The result of the measurement with, RBW = 1 kHz (ATT use for −6 dB) .



■ ORDERING INFORMATION

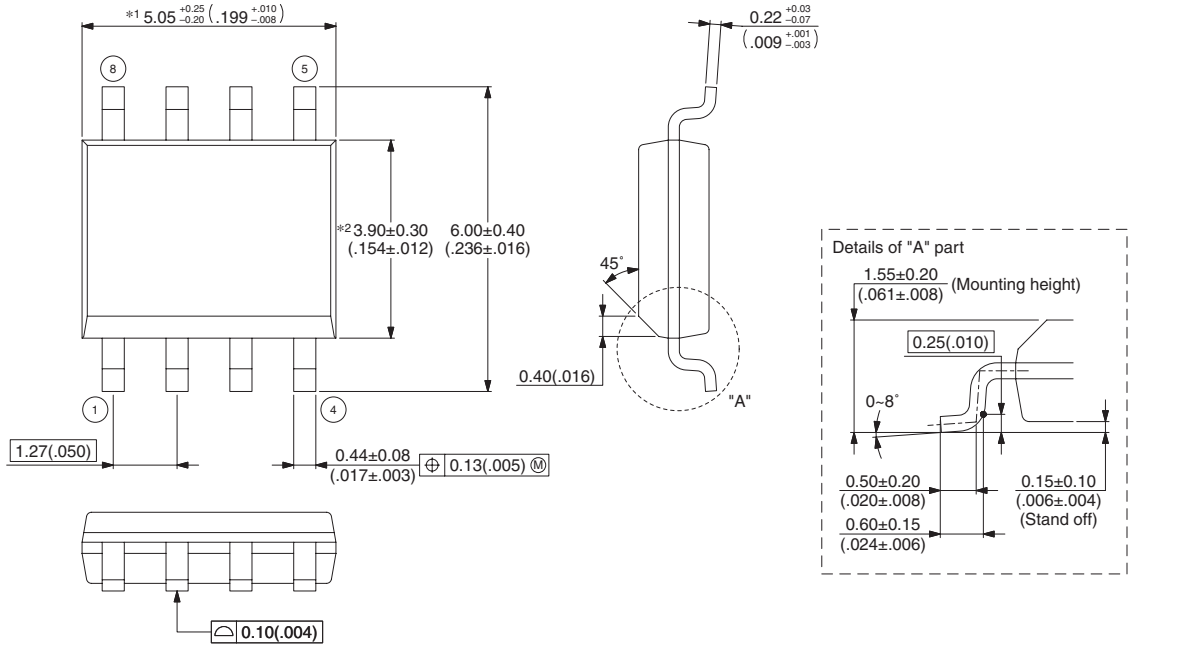
Part number	Input/Output Frequency	Modulation type	Modulation enable pin	Package	Remarks
MB88152APNF-G-100-JNE1	16.6 MHz to 134 MHz	Down spread	No	8-pin plastic SOP (FPT-8P-M02)	
MB88152APNF-G-101-JNE1	16.6 MHz to 67 MHz	Down spread	Yes		
MB88152APNF-G-102-JNE1	40 MHz to 134 MHz	Down spread	Yes		
MB88152APNF-G-110-JNE1	16.6 MHz to 134 MHz	Center spread	No		
MB88152APNF-G-111-JNE1	16.6 MHz to 67 MHz	Center spread	Yes		
MB88152APNF-G-112-JNE1	40 MHz to 134 MHz	Center spread	Yes		
MB88152APNF-G-100-JN-EFE1	16.6 MHz to 134 MHz	Down spread	No	8-pin plastic SOP (FPT-8P-M02)	Emboss taping (EF type)
MB88152APNF-G-101-JN-EFE1	16.6 MHz to 67 MHz	Down spread	Yes		
MB88152APNF-G-102-JN-EFE1	40 MHz to 134 MHz	Down spread	Yes		
MB88152APNF-G-110-JN-EFE1	16.6 MHz to 134 MHz	Center spread	No		
MB88152APNF-G-111-JN-EFE1	16.6 MHz to 67 MHz	Center spread	Yes		
MB88152APNF-G-112-JN-EFE1	40 MHz to 134 MHz	Center spread	Yes		
MB88152APNF-G-100-JN-ERE1	16.6 MHz to 134 MHz	Down spread	No	8-pin plastic SOP (FPT-8P-M02)	Emboss taping (ER type)
MB88152APNF-G-101-JN-ERE1	16.6 MHz to 67 MHz	Down spread	Yes		
MB88152APNF-G-102-JN-ERE1	40 MHz to 134 MHz	Down spread	Yes		
MB88152APNF-G-110-JN-ERE1	16.6 MHz to 134 MHz	Center spread	No		
MB88152APNF-G-111-JN-ERE1	16.6 MHz to 67 MHz	Center spread	Yes		
MB88152APNF-G-112-JN-ERE1	40 MHz to 134 MHz	Center spread	Yes		

■ PACKAGE DIMENSION

8-pin plastic SOP		
 (FPT-8P-M02)	Lead pitch	1.27 mm
	Package width × package length	3.9 × 5.05 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX
	Weight	0.06 g

8-pin plastic SOP
(FPT-8P-M02)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

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