KL5KUSB 201
USB2.0 Compliant Transceiver Chip
Datasheet (Digest)

Rev 1. 1E (2002.4.8)

Kawasaki Microelectronics Inc.

Kawasaki LSI Inc.

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Revision History

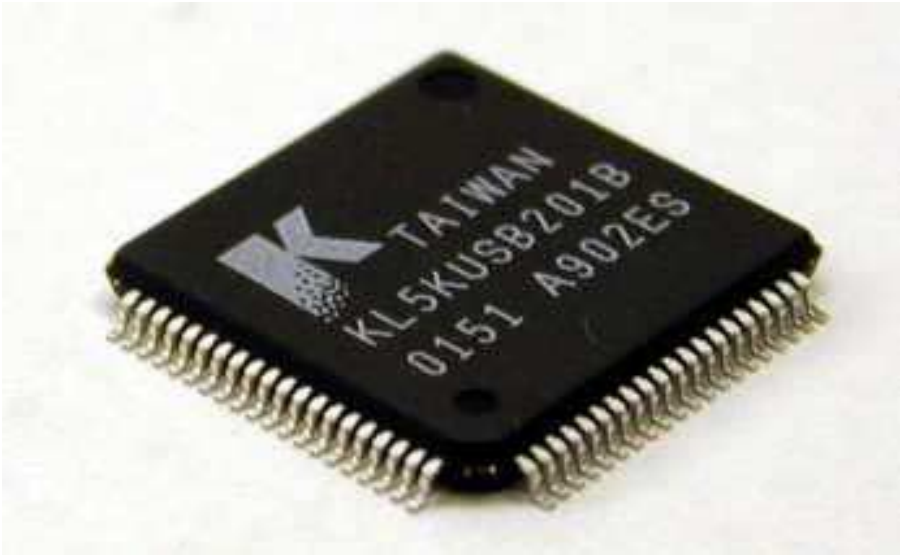
revision	date	Update
0.10J	2001.9.28	release first version
0.21J	2001.10.18	minor error correction
0.30E	2002.3.15	translation from Japanese to English with some minor change
1.0E	2002.3.25	Document Review is closed.
1.1E	2002.4.8	Table 5-3 pin78, 79 error corrected.

Table of Contents

1. Overview

Kawasaki Microelectronics Inc. and Kawasaki LSI Inc. introduce KL5KUSB201 LSI, which is designed based on USB Specification revision 2.0 and operates as both USB2.0 High Speed and Full Speed transceiver chip. It has two modes – UTMI Specification compatible mode and Kawasaki Original mode. In Kawasaki Original mode, the LSI has several convenient function such as automatic CRC generation and verification, transmit packet abortion and automatic test packet generation for High Speed Signal Quality test. The LSI is recognized as USB2.0 PHY chip and customers are able to build up USB2.0 compliant device system with their logic and PHY control / endpoint buffer function (SIE), which is available by Kawasaki or other IP vendor.

Figure 1. KL5KUSB201 Image



1.1 Chip Functionality

KL5KUSB201 Fucntionality is summarized below.

1. HS Chirp Signal Generation and Detection
2. Support for both High Speed (480Mbit/sec) and Full Speed (12Mbit/sec)
3. For received packet, phase lock, buffering, SYNC detection, NRZI decode, bit un-stuffing, CRC error detection (optional), serial to parallel conversion are performed. 16bit data is drived on SIE bus
4. For packet transmission, parallel 16bit data is received, serialized, CRC

generation (optional), bit stuffed and NRZI encoded. Packet is transmitted onto USB bus with SYNC and EOP attached

5. USB Bus status is delivered for outside SIE to monitor it
6. Function is controlled by Input Signals
7. Function defined by UTMI Specification is supported
8. Stand-alone Test packet generation for High Speed Signal Quality

1.2 KL5KUSB201 Product Feature

KL5KUSB201 Product Feature is shown below.

Table 1-2 KL5KUSB201 Product Feature

No	Item	Feature
1	Process	0.18um CMOS
2	Package	LQFP 80 pin plastic package
3	Input Clock Frequency	48MHz
4	Internal Clock Frequency	480MHz、48MHz and other
5	Output Clock Frequency (CKOUT)	30MHz
6	USB port	1 port (USB pin is separated for HS and FS)
7	Parallel Data width (SIE_DAT)	16bit
8	Power voltage	3.3±0.3V、1.8±0.15V
9	Operation Current in FS	typical 50mA
10	Operation Current in HS	typical 90mA
11	Operation Current at suspend	1uA
12	Ambient Temperature	0～70°C

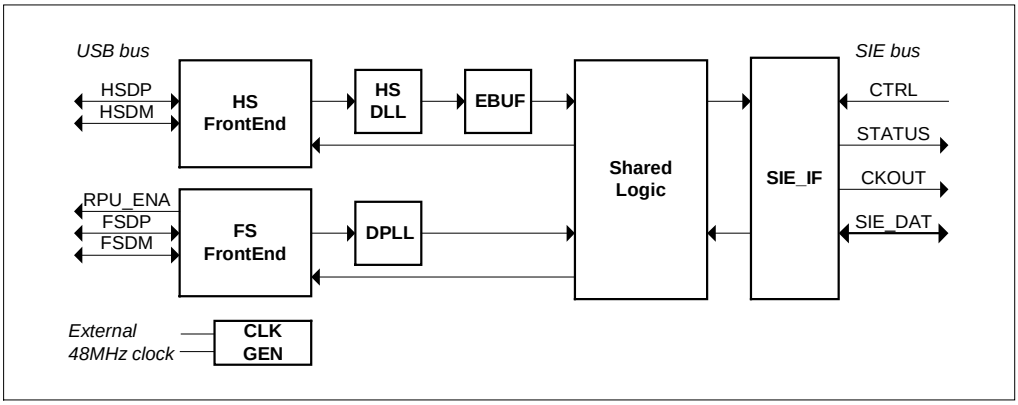
Please contact to our sales and marketing person to request samples, datasheet, USB201 IP and / or HS_SIE included ASCP planning.

2. Chip Architecture

Internal Architecture of KL5KUSB201 is shown in figure 2. The LSI consists of 6 major blocks as follows. **FrontEnd block** transmits and receives USB signals. **HS DLL block** is used to re-clock High Speed signals with internal 480MHz clock. **EBUF block** is for buffering High Speed signals. **Shared Logic block** includes such function as NRZI decode, bit un-stuffing, CRC check, serial to parallel conversion for both High Speed and Full Speed USB signals. **SIE_IF block** interfaces with SIE bus signals. For Full Speed operation, **DPLL block** is used to re-clock the Full Speed signals with

internal 12MHz clock instead of **FrontEnd, HSDLL** and **EBUF blocks**. For received signals, the LSI locks them in **HS DLL** and is buffering them in **EBUF**. Then signals are transferred to **Shared Logic** to convert data format, check the **CRC**, convert from serial to parallel. The data is finally delivered to the SIE bus through **SIE_IF**. For transmit operation, incoming parallel data is received in **SIE_IF** and sent to **Shared Logic** to perform parallel to serial conversion, CRC generation, bit stuffing and NRZI encoding. Finally the data is transmitted onto the USB bus through **FrontEnd block**.
High Speed or Full Speed operation is selected by SIE control signals. USB bus status can be monitored by USB bus status signals.

Figure 2 KL5KUSB201 Internal Architecture

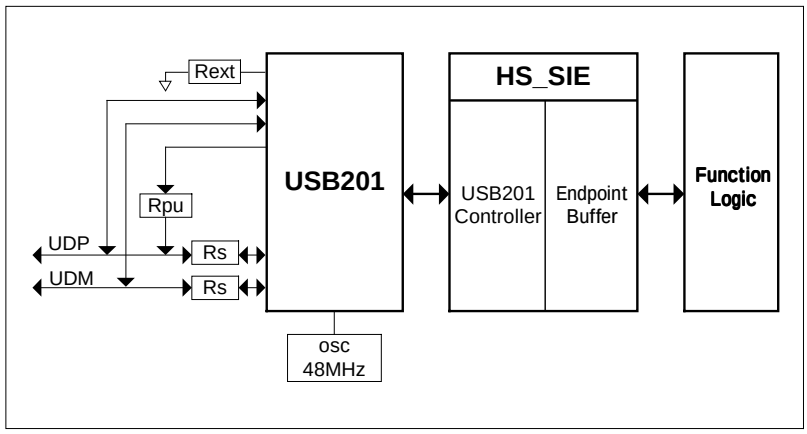


3. Application Example

Example of system configuration using KL5KUSB201 is shown in figure 3. To realize the USB device application, other than the LSI, SIE PHY control and function logic are needed.

Also suitable resistors such as Rpu, Rs and Rext and 48MHz clock oscillator or crystal and related parts are required.

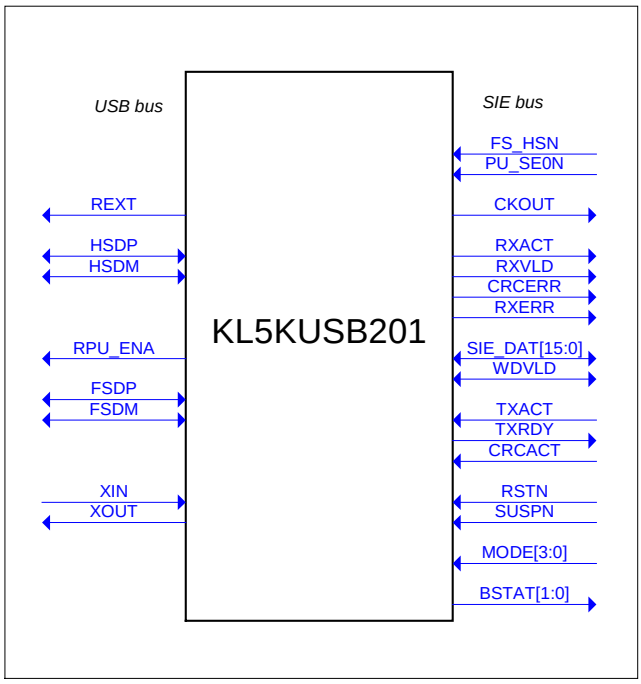
Figure 3 Application Example



4. Pinout Diagram

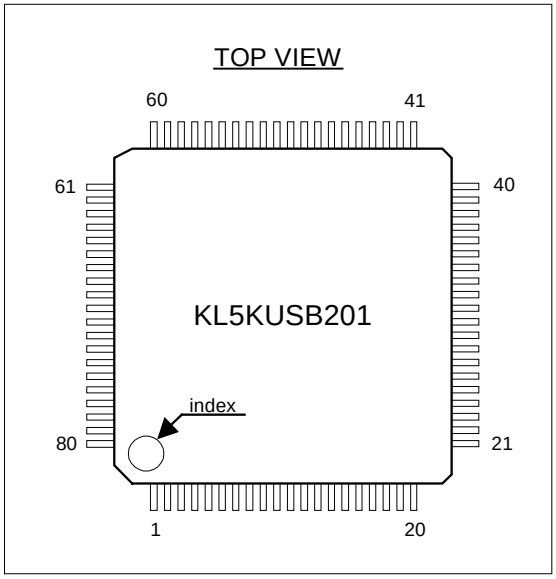
Symbol block of KL5KUSB201 is shown in Figure 4. The LSI has two interfaces – USB bus and SIE bus. USB related bus signals are shown in the left side of the symbol block, while SIE bus signal is in the right side. SIE control signals select LSI operation mode. These signals are FS_HSN, PU_SE0N, MODE, CRCACT, SUSPN and RSTN. USB bus status signals are BSTAT. CRCERR and RXERR are receiving error indicators. SIE_DAT is bi-directional bus. Signal direction and valid timing are controlled by RXACT, RXVLD, TXACT, TXRDY and WDVLD.

Figure 4 KL5KUSB201 Symbol Block



5. Package Information

5.1 Top View



5.2 Package Size

LQFP-80 package size is shown in Table 5.2.

Table 5-2. LQFP-80 size information

No	Item	Size	Unit
1	body size	12.0	mm
2	thickness	max 1.70	mm
3	pin pitch	0.5	mm

5.3 Pin Assignment

Package pin number and signal name Table is listed below. Please note that power pins named VDD18 (Pin No 39, 45, 56 and 62) are required to be supplied 1.8V, while other power pins named AVDD and VDD should be supplied 3.3V.

Table 5-3. Pin Assignment

Pin No	I/O	signal name	Pin No	I/O	signal name	Pin No	I/O	signal name	Pin No	I/O	signal name
1	--	AVDD	21	I	RSTN	41	I/O	SIE_DAT[7]	61	--	GND
2	--	GND	22	I	SUSPN	42	I/O	SIE_DAT[8]	62	--	VDD18
3	--	AVDD	23	O	BSTAT[0]	43	I/O	SIE_DAT[9]	63	IN	PU_SE0N
4	--	GND	24	O	BSTAT[1]	44	--	GND	64	IN	FS_HSN
5	O	REXT	25	I/O	SIE_DAT[0]	45	--	VDD18	65	--	GND
6	3S	RPU_ENA	26	--	VDD	46	--	GND	66	IN	CRCACT
7	--	AVDD	27	--	GND	47	--	VDD	67	IN	TXACT
8	--	GND	28	I/O	SIE_DAT[1]	48	I/O	SIE_DAT[10]	68	--	GND
9	I/O	FSDP	29	I/O	SIE_DAT[2]	49	I/O	SIE_DAT[11]	69	--	VDD
10	I/O	HSDP	30	--	GND	50	--	GND	70	I/O	WDVLD
11	I/O	HSDM	31	I/O	SIE_DAT[3]	51	I/O	SIE_DAT[12]	71	O	TXRDY
12	I/O	FSDM	32	--	VDD	52	--	GND	72	O	RXERR
13	--	GND	33	--	GND	53	I/O	SIE_DAT[13]	73	O	CRCERR
14	--	AVDD	34	I/O	SIE_DAT[4]	54	I/O	SIE_DAT[14]	74	--	GND
15	--	VDD	35	--	GND	55	--	GND	75	O	RXVLD
16	I	MODE[0]	36	--	VDD	56	--	VDD18	76	O	RXACT
17	I	MODE[1]	37	I/O	SIE_DAT[5]	57	--	GND	77	--	VDD
18	--	GND	38	I/O	SIE_DAT[6]	58	--	VDD	78	I	XIN
19	I	MODE[2]	39	--	VDD18	59	O	CKOUT	79	O	XOUT
20	I	MODE[3]	40	--	GND	60	I/O	SIE_DAT[15]	80	--	GND

6. Signal Description

Table 6 describes signal function description and related name in UTMI.

Table 6 Signal Description

No	Signal Name	I/O	Description	UTMI name
1	REXT	O	Reference bias current pin. Connect to GND via external resistor Rext.	--
2	HSDP	I/O	High Speed DP pin. Connect to USB Bus D+.	DP
3	HSDM	I/O	High Speed DM pin. Connect to USB Bus D-.	DM
4	RPU_ENA	O	Pull up resister source pin. Connect to external resistor Rpu, which is tied to USB bus D+. RPU_ENA becomes 3-state in High Speed operation.	--
5	FSDP	I/O	Full Speed DP pin. Connect to USB Bus D+ via termination resistor Rs.	(DP)
6	FSDM	I/O	Full Speed DM pin. Connect to USB Bus D- via termination resistor Rs.	(DM)
7	XIN	I	48MHz clock input pin. Connect to crystal oscillator or crystal oscillation circuit.	--
8	XOUT	O	48MHz clock output pin for crystal oscillation circuit.	--
9	FS_HSN	I	USB bus speed control pin.	XcvrSelect
10	PU_SE0N	I	Termination control pin. With FS_HSN and MODE, LSI operation mode is selected.	TermSelect
11	CKOUT	O	SIE bus clock pin. Frequency is 30MHz.	CLK
12	RXACT	O	USB packet received signal.	RXActive
13	RXVLD	O	SIE bus out data valid signal. Active H.	RXValid (RXValidH)
14	CRCERR	O	CRC error detection signal. Active when CRC logic is enabled.	--
15	RXERR	O	Receive error detection signal. RX error indicator except for CRC error.	RXError
16	TXACT	I	USB bus data transmit control signal. SIE bus switches from output to input when active.	TXValid (TXValidH)
17	TXRDY	O	SIE input data ready signal. Valid when TXACT is active.	TXReady
18	CRCACT	I	CRC detection logic enable signal. Also used for data transmit abortion.	--
19	SIE_DAT[15:0]	I/O	16bit parallel 3-state SIE data bus. Synchronized with CKOUT. Data direction is input when TXACT assertion. Default direction is output.	Data15-8, Data7-0
20	WDVLD	I/O	SIE data width indication signal. If last SIE data is a byte data, WDVLD is asserted.	ValidH
21	RSTN	I	Hardreset signal. Active L. Assertion required when power on and USB reset recognition.	RST (assert H)

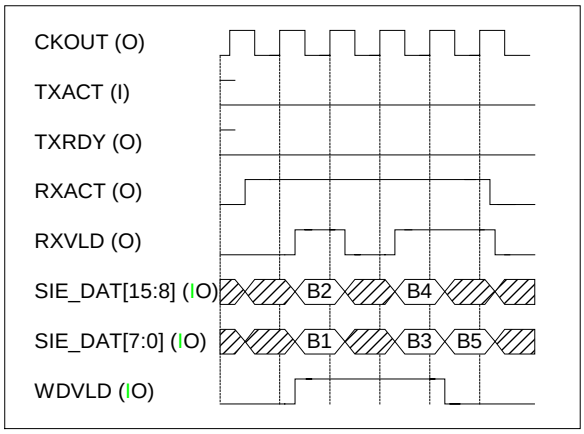
22	SUSPN	I	Asynchronous suspend signal. Active L. When asserted, the LSI internal circuit is set to be in stand-by mode. Only BSTAT[1:0] is active for monitoring USB bus status.	SuspendM
23	BSTAT[1:0]	O	USB bus monitor signals. In normal operation, the signal is synchronized with CKOUT, while asynchronous during suspend. When UTMI mode is selected, BSTAT is compatible with LineState.	LineState [1:0]
24	MODE[3:0]	I	Operation mode selection. One of UTMI mode, device test mode, normal operation mode and stand-alone USB2.0 signal quality test mode is selected.	OpMode [1:0]

7. SIE Bus Timing

7.1 SIE Bus Output Timing

Timing diagram of USB data output to SIE bus is shown in Figure 7-1. SIE bus direction is output in default. The LSI asserts RXACT to notice output of data to the external SIE logic. Valid data is indicated by RXVLD assertion. Odd byte of received USB data is driven to the lower byte of SIE bus. If SIE output data is in odd byte length, the LSI negates WDVLD at the final data valid phase to indicate that the last one is byte data.

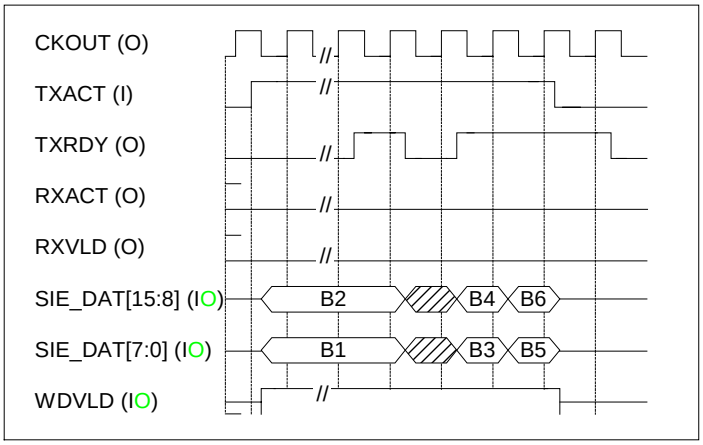
Figure 7-1 SIE Bus Output Timing



7.2 SIE Bus Input Timing

Figure 7-2 shows the receive timing diagram of the LSI from SIE bus. External SIE circuit asserts TXACT to notice the LSI to get data on SIE bus. When TXRDY is asserted, valid data is latched by the LSI. If data from SIE is odd byte length, SIE negates WDVLD at the final data stage like the case in SIE bus output timing. Please note that in Figure 7-2, a case of even byte length data is depicted.

Figure 7-2 SIE Bus Input Timing

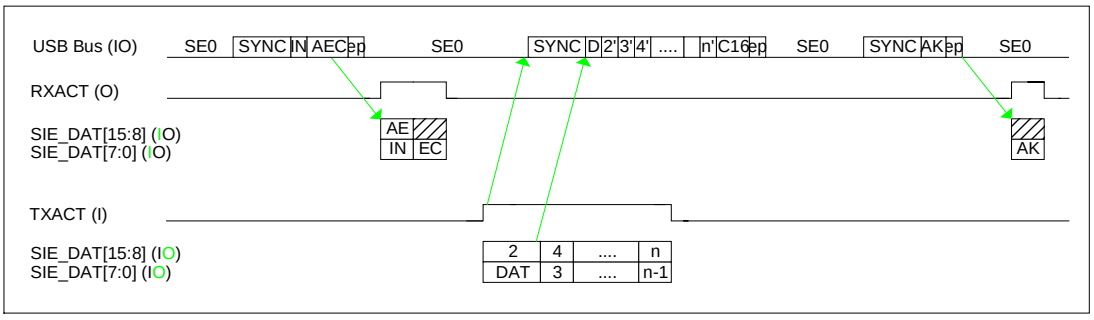


8. USB Bus Timing

8.1 Bulk IN Transaction

Figure 8-1 shows the data timing of a Bulk IN transaction from USB host. When the LSI receives IN packet from the host PC, it asserts RXACT and drives 3 bytes received data on SIE bus. External SIE logic receives the data, checks the information of address, endpoint and CRC if necessary. If it finds the data valid, the SIE returns the DATA packet to be transmitted. Finally the LSI receives ACK packet and finishes a Bulk IN transaction.

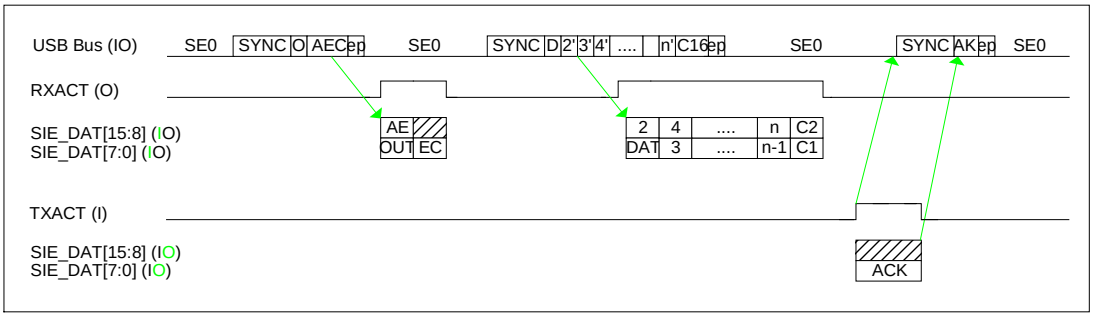
Figure 8-1 Bulk IN transaction



8.2 Bulk OUT Transaction

Figure 8-2 shows the data timing of a Bulk OUT transaction from the host PC. When the LSI receives OUT packet from the USB host, the LSI asserts RXACT and drives 3 bytes data received from the host. If the external SIE logic recognizes the OUT packet is valid, it waits for the next DATA packet from USB host. If the SIE logic receives the DATA packet correctly, it returns ACK.

Figure 8-2 Bulk OUT transaction



9. USB2.0 LSI Family

This section introduces Kawasaki's USB2.0 LSI family.

9.1 T&MT Evaluation Daughter Card (UUT)

The daughter card which is designed based on Transceiver and Macrocell Tester (T&MT) Interface Specification is available for evaluating the KL5KUSB201 chip. All necesary parts including the LSI, USB connector, resistors and crystal oscillator are attached. With using your T&MT compatible controller, the function of the LSI is able to be evaluated such as USB2.0 Test mode function, data transfer in High Speed or Full Speed mode and verification of functionality with the external UTMI compatible SIE.

Figure 9-1 KL5KUSB201 T&MT Daughter Board

9.2 PCI Evaluation Add-in Card

The USB2.0 to PCI Adapter card is developed for the purpose of evaluating the LSI as a USB device system using PC. The PCI card includes the LSI, USB connector, all necessary parts and U2PCI Chip, which is described later. The PCI card performs the control of the LSI, USB packet buffering, PCI bus transfer operation with high throughput. Evaluation software is available together with the board.

Figure 9-2 KL5KUSB201 PCI Evaluation Add-in Card

9.3 KL5BUDV002 LSI (U2PCI)

The KL5BUDV002 LSI is USB2.0 to PCI adapter chip, which consists of HS_SIE block, PCI Interface block and data buffer RAM. With KL5KUSB201, chipset performs data transfer with high throughput between USB2.0 and PCI bus. The chipset makes it easy to build up a USB2.0 device system. Main feature of KL5BUDV002 LSI is as follows.

1. Directly connected with KL5KUSB201 and realizes USB2.0 data transfer in both High Speed and Full Speed
2. Includes HS_SIE function and support up to 4 endpoints

Endpoint 0	Control Transfer	64Bytes buffer
Endpoint 1	Bulk OUT	512Bytes x2 buffers
Endpoint 2	Bulk IN	512Bytes x2 buffers
Endpoint 5	Interrupt IN	8Bytes buffer （option）

3. Includes 33MHz, 32bit PCI bus interface
   Target single access for memory mapped register access
   Master burst access with 2 DMA master controllers for memory access
4. Independent Data buffers for data transmit and receive
5. USB configuration transfer is controlled by the external PCI controller.

Figure 9-3-1 KL5BUDV002 Symbol

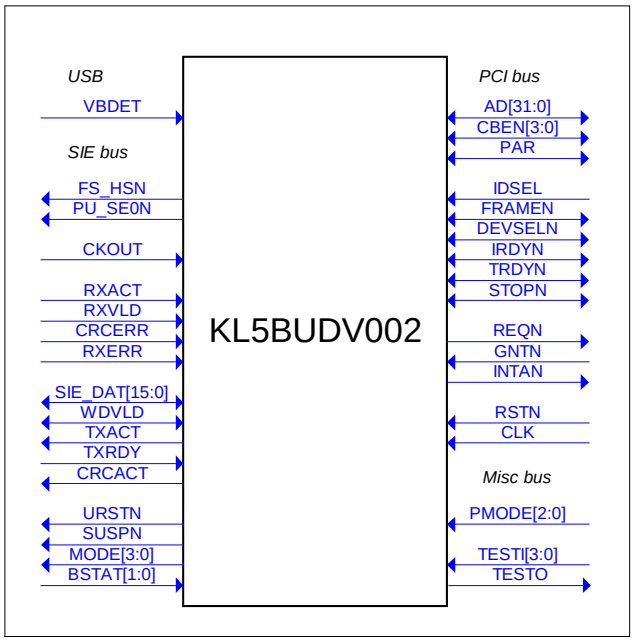


Figure 9-3-2 KL5BUDV002 Application Example

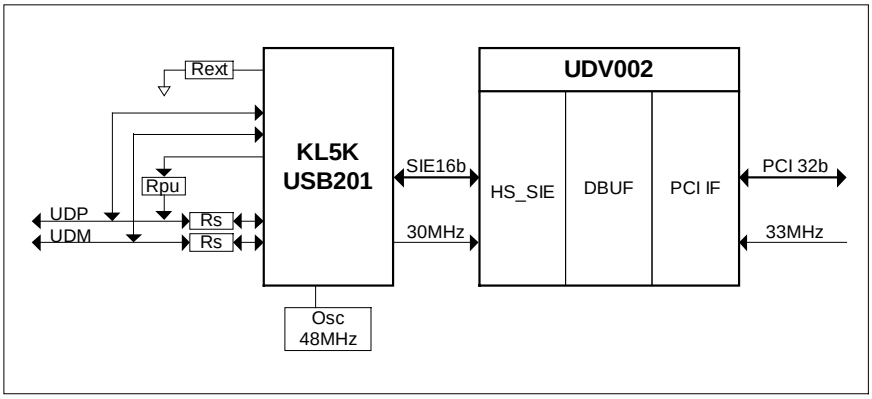


Figure 9-3-3 KL5BUDV002 Package Image

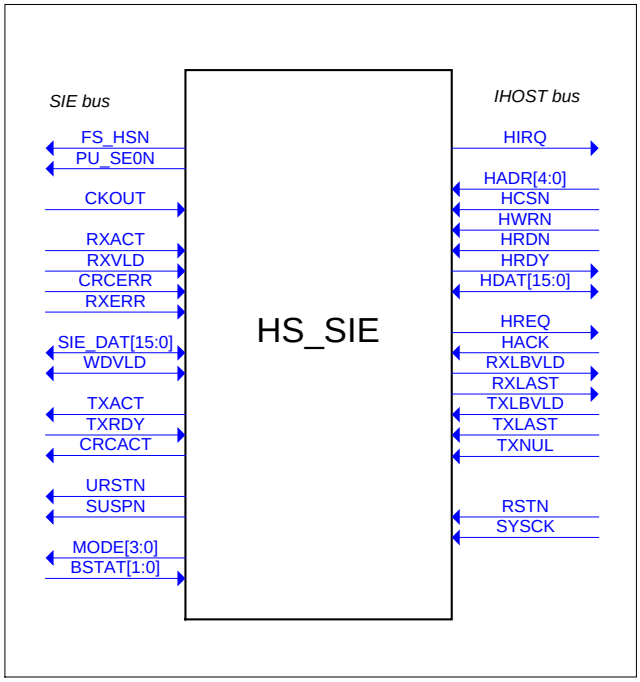
9.4 HS_SIE and USB201 ASIC IP

9.4.1 HS_SIE ASIC IP

HS_SIE IP is useful for Kawasaki ASIC users to design their LSI, which connects to KL5KUSB201 or includes USB201 IP inside. Together with KL5KUSB201 chip, the IP performs USB2.0 lower level protocol. The main features of HS_SIE are shown below.

1. RTL design makes it easy to implement with various processes
2. Compact design such as 20 k logic gates, 4x512 bytes and 1x64 bytes 1-p RAM
3. Performs HS chirp protocol and Speed detection
4. Processes the basic USB transaction such as token decode, miss-hit judgment, error detection and data toggle bit control
5. Controls transaction flow
6. Supports up to 6 endpoints in total – control, 2 bulk in, 2 bulk out and interrupt.
7. Ease-of-use internal bus interface such as 16bit bus register access or DMA

Figure 9-4-1 HS_SIE IP Symbol



9.4.2 USB201 ASIC IP

USB201 macro function is also prepared as ASIC IP in Kawasaki's KS6000 0.18um CMOS technology. Together with synthesizable HS_SIE, a single chip solution of USB device function can be realized.

Figure 9-4-2-1 USB device integration concept

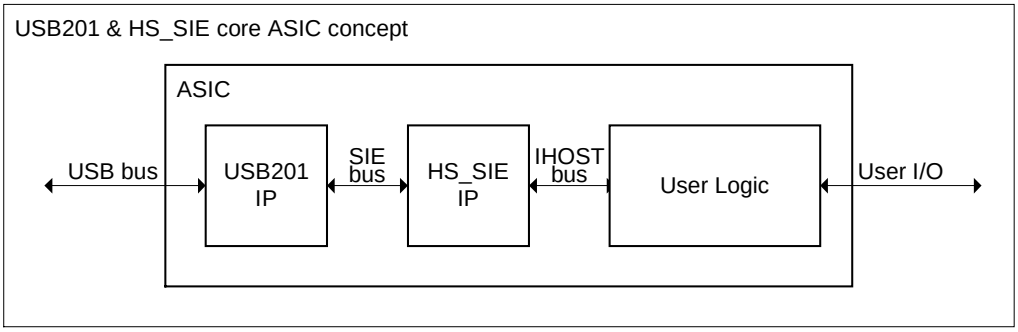
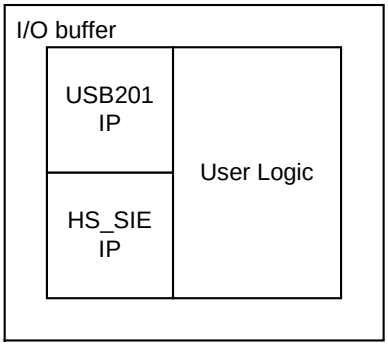


Figure 9-4-2-2 USB201 IP included ASIC chip image



10. References

10.1 USB2.0 Specification

Latest USB Specification, which describes both Full Speed and High Speed operation. The specification is available from USB_IF web site. Following three specifications are piled up to one zip file.

a. USB specification (April 27,2000)

b. errata to the USB2.0 specification (December 7,2000)

c. Mini-B connector Engineering Change Notice to the USB 2.0 specification

(http://www.usb.org/developers/docs.html)

10.2 UTMI Specification

This is the USB2.0 PHY function macro specification proposed by Intel Corp.
The interface between PHY and SIE is defined. It is downloadable from Intel site.

a. The USB 2.0 Transceiver Macrocell Interface, version 1.05(UTMI) specification

(http://developer.intel.com/technology/usb/spec.htm)

10.3 T&MT Interface Specification

This document is the macrocell test interface proposed by Intel Corp. To test PHY efficiently, card dimensions, connector pin layout and interface signals are defined. It is also downloadable from Intel web site.

a. The USB 2.0 Transceiver and Macrocell Tester (T&MT) Interface Specification

(http://developer.intel.com/technology/usb/spec.htm)

10.4 High Speed Board Design Guide

This document depicts the general guideline of High Speed USB device board design. Design tips of handling the high speed signals are available in this document. This document is downloadable from the Intel web site, too.

(http://developer.intel.com/technology/usb/spec.htm)

10.5 Kawasaki's Datasheet

More detailed documents are available by Kawasaki. Please contact our sales person.

a. KL5KUSB201 datasheet

b. KL5BUDV002 datasheet