512Mb DDR2 SDRAM

H5PS5182GFR-xxC
H5PS5182GFR-xxI
H5PS5182GFR-xxL
H5PS5182GFR-xxJ
H5PS5162GFR-xxC
H5PS5162GFR-xxI
H5PS5162GFR-xxL
H5PS5162GFR-xxJ

Revision History

Rev.	History	Draft Date
1.0	Release	Sep. 2010
1.1	Updated IDD Specification	Sep.2010
1.2	Added IDD6 Low Power Products	Nov.2010
1.3	Corrected typo	Dec.2010
1.4	Corrected typo	Feb.2011
1.5	Merged with x8 series(H5PS5182GFR)	Mar.2011
1.6	Corrected typo	Sep.2011
1.7	New revised logo	Feb. 2013

Contents

1. Description

1.1 Device Features & Ordering Information

1.1.1 Key Features

- VDD ,VDDQ =1.8 +/- 0.1V
- All inputs and outputs are compatible with SSTL_18 interface
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous-data transaction aligned to bidirectional data strobe (DQS, $\overline{\text{DQS}}$)
- Differential Data Strobe (DQS, $\overline{\text{DQS}}$)
- Data outputs on DQS, $\overline{\text{DQS}}$ edges when read (edged DQ)
- Data inputs on DQS centers when write(centered DQ)
- On chip DLL align DQ, DQS and $\overline{\text{DQS}}$ transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 2, 3, 4, 5, 6 and 7 supported
- Programmable additive latency 0, 1, 2, 3, 4 and 5 supported
- Programmable burst length 4 / 8 with both nibble sequential and interleave mode
- Internal four bank operations with single pulsed RAS
- tRAS lockout supported
- 8K refresh cycles /64ms
- JEDEC standard 84ball FBGA(x16) : 7.5mm x 12.5mm
- Full strength driver option controlled by EMRS
- On Die Termination supported
- Off Chip Driver Impedance Adjustment supported
- Self-Refresh High Temperature Entry
- Partial Array Self Refresh support

Ordering Information

Part No.	Configura-tion	Power Consumption	Operation Temp	Package
H5PS5182GFR-xx*C	64Mx8	Normal Consumption	Commercial	60 Ball fBGA
H5PS5182GFR-xx*I		Normal Consumption	Industrial	
H5PS5182GFR-xx*L		Low Power Consumption (IDD6 Only)	Commercial	
H5PS5182GFR-xx*J		Low Power Consumption (IDD6 Only)	Industrial	
H5PS5162GFR-xx*C	32Mx16	Normal Consumption	Commercial	84 Ball fBGA
H5PS5162GFR-xx*I		Normal Consumption	Industrial	
H5PS5162GFR-xx*L		Low Power Consumption (IDD6 Only)	Commercial	
H5PS5162GFR-xx*J		Low Power Consumption (IDD6 Only)	Industrial	

Note:

-XX* is the speed bin, refer to the Operating Frequency table for complete part number.
- SK hynix Inc. Halogen-free products are compliant to RoHS.
SK hynix Inc. supports Lead & Halogen free parts for each speed grade with same specification, except Lead free materials.
We'll add "R" character after "F" for Lead & Halogen free products

Operating Frequency

Grade	tCK(ns)	CL	tRCD	tRP	Unit
E3	5	3	3	3	Clk
C4	3.75	4	4	4	Clk
Y5	3	5	5	5	Clk
S6	2.5	6	6	6	Clk
S5	2.5	5	5	5	Clk
G7	1.875	7	7	7	Clk

Note:

-G7 is a special speed product used in electronic engineering for high speed storage of the working data of a consumer digital electronic device.

1.2 Pin Configuration & Address Table

64Mx8 DDR2 PIN CONFIGURATION(Top view: see balls through package)

1	2	3		7	8	9
VDD	NU,$\overline{RDQS}$	VSS	A	VSSQ	$\overline{DQS}$	VDDQ
DQ6	VSSQ	DM,RDQS	B	DQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	C	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	D	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	E	VSSDL	CK	VDD
	CKE	$\overline{WE}$	F	$\overline{RAS}$	$\overline{CK}$	ODT
NC	BA0	BA1	G	$\overline{CAS}$	$\overline{CS}$	
	A10	A1	H	A2	A0	VDD
VSS	A3	A5	J	A6	A4	
	A7	A9	K	A11	A8	VSS
VDD	A12	NC	L	NC	A13	

ROW AND COLUMN ADDRESS TABLE

ITEMS	64Mx8
# of Bank	4
Bank Address	BA0, BA1
Auto Precharge Flag	A10/AP
Row Address	A0 - A13
Column Address	A0-A9
Page size	1 KB

32Mx16 DDR2 PIN CONFIGURATION(Top view: see balls through package)

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	$\overline{\text{UDQS}}$	VDDQ
DQ14	VSSQ	UDM	B	UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ	C	VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11	D	DQ10	VSSQ	DQ13
VDD	NC	VSS	E	VSSQ	$\overline{\text{LDQS}}$	VDDQ
DQ6	VSSQ	LDM	F	LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	G	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	H	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	K	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
NC	BA0	BA1	L	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC	R	NC	NC	

ROW AND COLUMN ADDRESS TABLE

ITEMS	32Mx16
# of Bank	4
Bank Address	BA0, BA1
Auto Precharge Flag	A10/AP
Row Address	A0 - A12
Column Address	A0-A9
Page size	2 KB

1.3 PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, V_{REF} must be maintained to this input. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH.
$\overline{CS}$	Input	Chip Select : All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination Control : ODT(registered HIGH) enables on die termination resistance internal to the DDR2 SDRAM. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$.LDQS/$\overline{LDQS}$, UDM and LDM signal. The ODT pin will be ignored if the Extended Mode Register(EMRS(1)) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (LDM, UDM)	Input	Input Data Mask : DM is an input mask signal for write data. Input Data is masked when DM is sampled High coincident with that input data during a WRITE access. DM is sampled on both edges of DQS, Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 -A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0-BA1. The address inputs also provide the op code during MODE REGISTER SET commands.
DQ	Input/ Output	Data input / output : Bi-directional data bus

-Continue-

PIN	TYPE	DESCRIPTION
UDQS, $\overline{UDQS}$ LDQS, $\overline{LDQS}$	Input/ Output	Data Strobe : Output with read data, input with write data. Edge aligned with read data, centered in write data. For the x16, LDQS correspond to the data on DQ0~DQ7; UDQS corresponds to the data on DQ8~DQ15. The data strobes DQS, LDQS and UDQS may be used in single ended mode or paired with optional complementary signals DQS, LDQS and UDQS to provide differential pair signaling to the system during both reads and wirtes. An EMRS(1) control bit enables or disables all complementary data strobe signals. In this data sheet, "differential DQS signals" refers to any of the following with A10 = 0 of EMRS(1) x16 LDQS/$\overline{LDQS}$ and UDQS/$\overline{UDQS}$ "single-ended DQS signals" refers to any of the following with A10 = 1 of EMRS(1) x16 LDQS and UDQS
NC		No Connect : No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.8V +/- 0.1V
VSSQ	Supply	DQ Ground
VDDL	Supply	DLL Power Supply : 1.8V +/- 0.1V
VSSDL	Supply	DLL Ground
VDD	Supply	Power Supply : 1.8V +/- 0.1V
VSS	Supply	Ground
VREF	Supply	Reference voltage for inputs for SSTL interface.

2. Maximum DC Ratings

2.1 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 1.0 V ~ 2.3 V	V	1
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	℃	1, 2
I_I	Input leakage current; any input 0V VIN VDD; all other balls not under test = 0V)	-2 uA ~ 2 uA	uA	
I_{OZ}	Output leakage current; 0V VOUT VDDQ; DQ and ODT disabled	-5 uA ~ 5 uA	uA	

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions. Please refer to JESD51-2 standard.

2.2 Operating Temperature Condition

Symbol	Parameter		Rating	Units	Notes
T_{OPER}	Operating Temperature	Commercial	0 to 85	°C	1,2
		Industrial	-40 to 95		

Note:

1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
2. At 85~95° T_{OPER} , Double refresh rate(tREFI: 3.9us) is required, and to enter the self refresh mode at this temperature range it must be required an EMRS command to change itself refresh rate.

3. AC & DC Operating Conditons

3.1 DC Operating Conditions

3.1.1 Recommended DC Operating Conditions (SSTL_1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	1,2
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1,2
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3,4
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	5

1. Min. Typ. and Max. values increase by 100mV for C3(DDR2-533 3-3-3) speed option.
2. VDDQ tracks with VDD,VDDL tracks with VDD. AC parameters are measured with VDD,VDDQ and VDD.
3. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ
4. Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
5. VTT of transmitting device must track VREF of receiving device.

3.1.2 ODT DC electrical characteristics

PARAMETER/CONDITION	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75 ohm	Rtt1(eff)	60	75	90	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150 ohm	Rtt2(eff)	120	150	180	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,1; 50 ohm	Rtt3(eff)	40	50	60	ohm	1
Deviation of VM with respect to VDDQ/2	delta VM	-6		+6	%	1

Note:

1. Test condition for Rtt measurements

Measurement Definition for Rtt(eff): Apply V_{IH} (ac) and V_{IL} (ac) to test pin separately, then measure current I(V_{IH} (ac)) and I(V_{IL}(ac)) respectively. V_{IH} (ac), V_{IL} (ac), and VDDQ values defined in SSTL_18

$$\text{Rtt(eff)} = \frac{V_{IH}(ac) - V_{IL}(ac)}{I(V_{IH}(ac)) - I(V_{IL}(ac))}$$

Measurement Definition for VM : Measurement Voltage at test pin(mid point) with no load.

$$\text{delta VM} = \left(\frac{2 \times Vm}{VDDQ} - 1\right) \times 100\%$$

3.2 DC & AC Logic Input Levels

3.2.1 Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH}(dc)	dc input logic high	VREF + 0.125	VDDQ + 0.3	V	
V_{IL}(dc)	dc input logic low	- 0.3	VREF - 0.125	V	

3.2.2 Input AC Logic Level

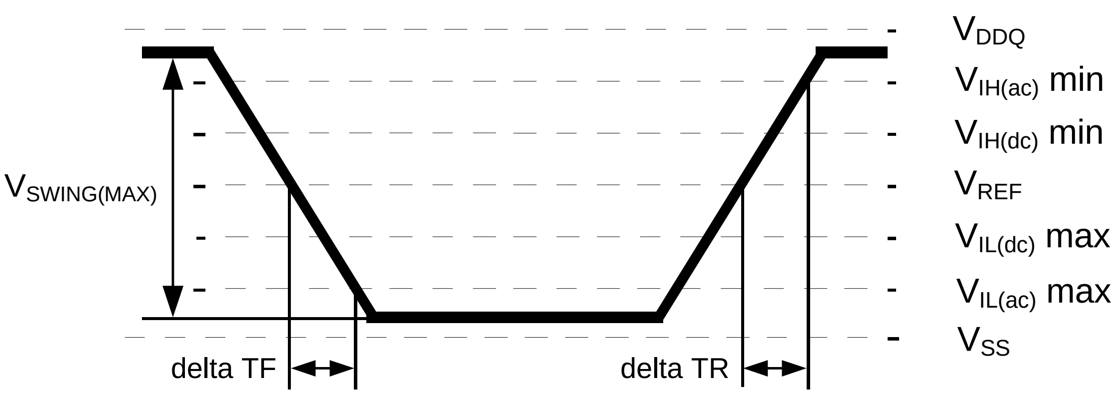
Symbol	Parameter	DDR2 400,533		DDR2 667,800		Units	Notes
		Min.	Max.	Min.	Max.		
V_{IH} (ac)	ac input logic high	VREF + 0.250	-	VREF + 0.200	-	V	
V_{IL} (ac)	ac input logic low	-	VREF - 0.250	-	VREF - 0.200	V	

3.2.3 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Note:

1. Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to $V_{IH(ac)}$ min for rising edges and the range from V_{REF} to $V_{IL(ac)}$ max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.



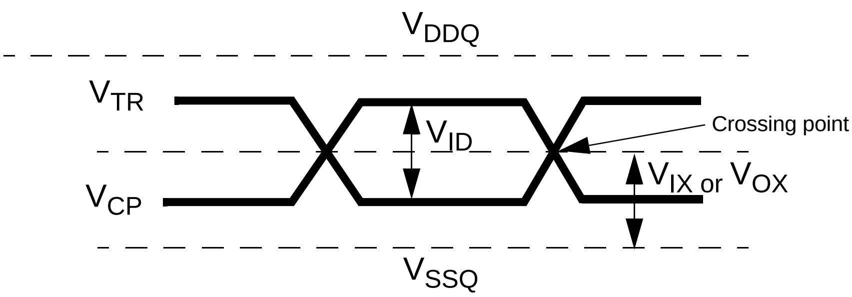
$$\text{Falling Slew} = \frac{V_{REF} - V_{IL(ac)}\ \text{max}}{\text{delta TF}} \qquad \text{Rising Slew} = \frac{V_{IH(ac)}\ \text{min} - V_{REF}}{\text{delta TR}}$$

< Figure : AC Input Test Signal Waveform>

3.2.4 Differential Input AC logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ID} (ac)	ac differential input voltage	0.5	VDDQ + 0.6	V	1
V_{IX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.175	0.5 * VDDQ + 0.175	V	2

1. VIN(DC) specifies the allowable DC execution of each input of differential pair such as CK, $\overline{\text{CK}}$, DQS, $\overline{\text{DQS}}$, LDQS, $\overline{\text{LDQS}}$, UDQS and $\overline{\text{UDQS}}$.
2. VID(DC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input (such as CK, DQS, LDQS or UDQS) level and VCP is the complementary input (such as $\overline{\text{CK}}$, $\overline{\text{DQS}}$, $\overline{\text{LDQS}}$ or $\overline{\text{UDQS}}$) level. The minimum value is equal to VIH(DC) - V IL(DC).



< Differential signal levels >

Note:

1. VID(AC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal (such as CK, DQS, LDQS or UDQS) and VCP is the complementary input signal (such as $\overline{\text{CK}}$, $\overline{\text{DQS}}$, $\overline{\text{LDQS}}$ or $\overline{\text{UDQS}}$). The minimum value is equal to V IH(AC) - V IL(AC).
2. The typical value of VIX(AC) is expected to be about 0.5 * VDDQ of the transmitting device and VIX(AC) is expected to track variations in VDDQ . VIX(AC) indicates the voltage at which differential input signals must cross.

3.2.5 Differential AC output parameters

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.125	0.5 * VDDQ + 0.125	V	1

Note:

1. The typical value of VOX(AC) is expected to be about 0.5 * V DDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ . VOX(AC) indicates the voltage at whitch differential output signals must cross.

3.3 Output Buffer Characteristics

3.3.1 Output AC Test Conditions

Symbol	Parameter	SSTL_18 Class II	Units	Notes
V_{OTR}	Output Timing Measurement Reference Level	0.5 * V_{DDQ}	V	1

1. The VDDQ of the device under test is referenced.

3.3.2 Output DC Current Drive

Symbol	Parameter	SSTl_18	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

1. V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.
2. V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 ohm for values of V_{OUT} between 0 V and 280 mV.
3. The dc value of V_{REF} applied to the receiving device is set to V_{TT}
4. The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Section 3.3) along a 21 ohm load line to define a convenient driver current for measurement.

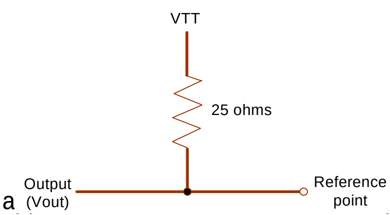
3.3.3 OCD default characteristics

Description	Parameter	Min	Nom	Max	Unit	Notes
Output impedance		See full strength default driver characteristics			ohms	1
Output impedance step size for OCD calibration		0		1.5	ohms	6
Pull-up and pull-down mismatch		0		4	ohms	1,2,3
Output slew rate	Sout	1.5	-	5	V/ns	1,4,5,6,7,8

Note

1. Absolute Specifications (Toper; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V). DRAM I/O specifications for timing,voltage, and slew rate are no longer applicable if OCD is changed from default settings. Please refer to the Device Operation & Timing Diagram of DDR2 for the Full Strength Default Driver Characteristics.
2. Impedance measurement condition for output source dc current: VDDQ=1.7V; VOUT=1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
4. Slew rate measured from vil(ac) to vih(ac).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18 ohms at nominal conditions across all process corners/ variations and represents only the DRAM uncertainty. A 0 ohm value(no calibration) can only be achieved if the OCD impedance is 18 ohms +/- 0.75 ohms under nominal conditions.

Output Slew rate load:



7. DRAM output slew rate specification a eed bins.
8. Timing skew due to DRAM output slew rate mis-match between DQS / $\overline{DQS}$ and associated DQs is included in tDQSQ and tQHS specification.

3.4 IDD Specifications & Test Conditions

IDD Specifications(max)

Symbol		DDR2 1066		DDR2 800		DDR2 667		Units
		x8	x16	x8	x16	x8	x16	
IDD0		50	66	47	56	45	54	mA
IDD1		53	70	50	60	48	58	mA
IDD2P		7	7	7	7	7	7	mA
IDD2Q		18	20	16	18	16	18	mA
IDD2N		22	25	20	21	20	21	mA
IDD3P	F	15	15	15	15	15	15	mA
	S	12	12	12	12	12	12	mA
IDD3N		40	45	38	40	38	38	mA
IDD4W		110	130	110	120	105	110	mA
IDD4R		100	120	100	110	95	100	mA
IDD5		75	90	75	90	70	80	mA
IDD6	Normal	6	6	6	6	6	6	mA
	Low Power	4	4	4	4	4	4	mA
IDD7		110	194	110	184	110	174	mA

Note : Product list

Part No.	Configuration	Power Consumption	Operation Temp	Package
H5PS5182GFR-xx*C	32Mx16	Normal Consumption	Commercial	60 Ball fBGA
H5PS5182GFR-xx*I		Normal Consumption	Industrial	
H5PS5182GFR-xx*L		Low Power Consumption (IDD6 Only)	Commercial	
H5PS5182GFR-xx*J		Low Power Consumption (IDD6 Only)	Industrial	
H5PS5162GFR-xx*C	32Mx16	Normal Consumption	Commercial	84 Ball fBGA
H5PS5162GFR-xx*I		Normal Consumption	Industrial	
H5PS5162GFR-xx*L		Low Power Consumption (IDD6 Only)	Commercial	
H5PS5162GFR-xx*J		Low Power Consumption (IDD6 Only)	Industrial	

IDD Test Conditions

(IDD values are for full operating range of Voltage and Temperature, Notes 1-5)

<table>
<tr><th>Symbol</th><th colspan="2">Conditions</th><th>Units</th></tr>
<tr><td>IDD0</td><td colspan="2">Operating one bank active-precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRAS min(IDD) ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;Address bus inputs are SWITCHING;Data bus inputs are SWITCHING</td><td>mA</td></tr>
<tr><td>IDD1</td><td colspan="2">Operating one bank active-read-precharge current ; IOUT = 0mA;BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD) ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands ; Address bus inputs are SWITCHING ; Data pattern is same as IDD4W</td><td>mA</td></tr>
<tr><td>IDD2P</td><td colspan="2">Precharge power-down current ; All banks idle ; tCK = tCK(IDD) ; CKE is LOW ; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING</td><td>mA</td></tr>
<tr><td>IDD2Q</td><td colspan="2">Precharge quiet standby current ; All banks idle; tCK = tCK(IDD);CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING</td><td>mA</td></tr>
<tr><td>IDD2N</td><td colspan="2">Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING</td><td>mA</td></tr>
<tr><td rowspan="2">IDD3P</td><td rowspan="2">Active power-down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING</td><td>Fast PDN Exit MRS(12) = 0</td><td>mA</td></tr>
<tr><td>Slow PDN Exit MRS(12) = 1</td><td>mA</td></tr>
<tr><td>IDD3N</td><td colspan="2">Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP =tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING</td><td>mA</td></tr>
<tr><td>IDD4W</td><td colspan="2">Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING</td><td>mA</td></tr>
<tr><td>IDD4R</td><td colspan="2">Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING;; Data pattern is same as IDD4W</td><td>mA</td></tr>
<tr><td>IDD5B</td><td colspan="2">Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING</td><td>mA</td></tr>
<tr><td>IDD6</td><td colspan="2">Self refresh current; CK and $\overline{CK}$ at 0V; CKE £ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING</td><td>mA</td></tr>
</table>

IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, $\overline{\text{CS}}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions	mA

Note:

1. VDDQ = 1.8 +/- 0.1V ; VDD = 1.8 +/- 0.1V
   (exclusively VDDQ = 1.9 +/- 0.1V ; VDD = 1.9 +/- 0.1V for C3 speed grade)
2. IDD specifications are tested after the device is properly initialized
3. Input slew rate is specified by AC Parametric Test Condition
4. IDD parameters are specified with ODT disabled.
5. Data bus consists of DQ, DM, DQS, DQS, RDQS, RDQS, LDQS, LDQS, UDQS, and UDQS. IDD values must be met with all combinations of EMRS bits 10 and 11.
6. Definitions for IDD
   LOW is defined as Vin £ VILAC(max)
   HIGH is defined as Vin Š VIHAC(min)
   STABLE is defined as inputs stable at a HIGH or LOW level
   FLOATING is defined as inputs at VREF = VDDQ/2
   SWITCHING is defined as: inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

For purposes of IDD testing, the following parameters are to be utilized

Speed Bin (CL-tRCD-tRP)	DDR2-800		DDR2-667	DDR2-533	DDR2-400	Units
	5-5-5	6-6-6	5-5-5	4-4-4	3-3-3	
CL(IDD)	5	6	5	4	3	tCK
tRCD(IDD)	12.5	15	15	15	15	ns
tRC(IDD)	57.25	60	60	60	55	ns
tRRD(IDD)	10	10	10	10	10	ns
tCK(IDD)	2.5	2.5	3	3.75	5	ns
tRASmin(IDD)	45	45	45	45	40	ns
tRASmax(IDD)	70000	70000	70000	70000	70000	ns
tRP(IDD)	12.5	15	15	15	15	ns
tRFC(IDD)-512Mb	105	105	105	105	105	ns

Detailed IDD7

The detailed timings are shown below for IDD7. Changes will be required if timing parameter changes are made to the specification.

Legend: A = Active; RA = Read with Autoprecharge; D = Deselect

IDD7: Operating Current: All Bank Interleave Read operation

All banks are being interleaved at minimum tRC(IDD) without violating tRRD(IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOUT = 0mA

Timing Patterns for 4 bank devices

-DDR2-400 3/3/3: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D (11 clocks)

-DDR2-533 3/3/3: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D (15 clocks)

-DDR2-533 4/4/4: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D (16 clocks)

-DDR2-667 4/4/4: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D (19 clocks)

-DDR2-667 5/5/5: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D (20 clocks)

-DDR2-800 5/5/5: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D (23 clocks)

-DDR2-800 6/6/6: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D D (24 clocks)

3.5. Input/Output Capacitance

Parameter	Symbol	DDR2- 400 DDR2- 533		DDR2 667		DDR2 800		Units
		Min	Max	Min	Max	Min	Max	
Input capacitance, CK and $\overline{CK}$	CCK	1.0	2.0	1.0	2.0	1.0	2.0	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	x	0.25	x	0.25	x	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	2.0	1.0	2.0	1.0	1.75	pF
Input capacitance delta, all other input-only pins	CDI	x	0.25	x	0.25	x	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	2.5	4.0	2.5	3.5	2.5	3.5	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	x	0.5	x	0.5	x	0.5	pF

4. Electrical Characteristics & AC Timing Specification

-40℃ $\leq T_{CASE} \leq$ 95℃; V_{DDQ} = 1.8 V +/- 0.1V; V_{DD} = 1.8V +/- 0.1V)

Refresh Parameters by Device Density

Parameter	Symbol		256Mb	512Mb	1Gb	2Gb	4Gb	Units
Refresh to Active /Refresh command time	tRFC		75	105	127.5	195	327.5	ns
Average periodic refresh interval	tREFI	-40℃ $\leq T_{CASE} \leq$ 85℃	7.8	7.8	7.8	7.8	7.8	us
		85℃ $< T_{CASE} \leq$ 95℃	3.9	3.9	3.9	3.9	3.9	us

DDR2 SDRAM speed bins and tRCD, tRP and tRC for corresponding bin

Speed	DDR2-800D	DDR2-800E	DDR2-667D	DDR2-533C	DDR2-400B	Units
Bin(CL-tRCD-tRP)	5-5-5	6-6-6	5-5-5	4-4-4	3-3-3	
Parameter	min	min	min	min	min	
CAS Latency	5	6	5	4	5	tCK
tRCD	12.5	15	15	15	15	ns
tRP	12.5	15	15	15	15	ns
tRAS	45	45	45	45	40	ns
tRC	57.5	60	60	60	55	ns

Timing Parameters by Speed Grade

(Refer to notes for information related to this table at the following pages of this table)

Parameter	Symbol	DDR2-400		DDR2-533		Unit	Note
		min	max	min	max		
Clock cycle time, CL=x	tCK	5000	8000	3750	8000	ps	15
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
DQ output access time from CK/$\overline{CK}$	tAC	-600	+600	-500	+500	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-500	+500	-450	+450	ps	
Write command to DQS associated clock edge	WL	RL - 1		RL - 1		tCK	
First DQS latching transition to associated clock edge	tDQSS	-0.25	0.25	-0.25	0.25	tCK	
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK	
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK	
DQS input high pulse width	tDQSH	0.35	-	0.35	-	tCK	
DQS input low pulse width	tDQSL	0.35	-	0.35	-	tCK	
Write preamble	tWPRE	0.35	-	0.35	-	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Address and control input setup time	tIS(base)	350	-	250	-	ps	5,7,9,22
Address and control input hold time	tIH(base)	475	-	375	-	ps	5,7,9,23
Control & Address input pulse width for each input	tIPW	0.6	-	0.6	-	tCK	
DQ and DM input setup time (differential strobe)	tDS (base)	150	-	100	-	ps	6,7,8,20,28
DQ and DM input hold time (differential strobe)	tDH (base)	275	-	225	-	ps	6,7,8,21,28
DQ and DM input setup time (single ended strobe)	tDS1 (base)	25	-	-25	-	ps	6,7,8,25
DQ and DM input hold time (single ended strobe)	tDH1 (base)	25	-	-25	-	ps	6,7,8,26
DQ and DM input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK	
DQ output access time from CK/$\overline{CK}$	tAC	- 600	+ 600	- 500	+ 500	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	- 500	+ 500	- 450	+ 450	ps	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	-	tAC max	-	tAC max	ps	18
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	18
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	ps	18
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	350	-	300	ps	13
CK half period	tHP	min (tCL,tCH)	-	min (tCL,tCH)	-	ps	11,12
DQ hold skew factor	tQHS	-	450	-	400	ps	12
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	tHP - tQHS	-	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	

-Continue-

(Refer to notes for information related to this table at the following pages of this table)

Parameter	Symbol	DDR2-400		DDR2-533		Unit	Note
		min	max	min	max		
Active to active command period for 1KB page size products	tRRD	7.5	-	7.5	-	ns	4
Active to active command period for 2KB page size products	tRRD	10	-	10	-	ns	4
Four Active Window for 1KB page size products	tFAW	37.5	-	37.5	-	ns	
Four Active Window for 2KB page size products	tFAW	50	-	50	-	ns	
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	-	15	-	ns	
Auto precharge write recovery + precharge time	tDAL	WR+tRP	-	WR+tRP	-	tCK	14
Internal write to read command delay	tWTR	10	-	7.5	-	ns	24
Internal read to precharge command delay	tRTP	7.5		7.5		ns	3
CKE minimum pulse width (high and low pulse width)	^{t}CKE	3		3		tCK	27
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200		200		tCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	tCK	
Exit active power down to read command	tXARD	2		2		tCK	1
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		6 - AL		tCK	1, 2
ODT turn-on delay	^{t}AOND	2	2	2	2	tCK	16
ODT turn-on	^{t}AON	tAC(min)	tAC(max) +1	tAC(min)	tAC(max) +1	ns	16
ODT turn-on(Power-Down mode)	^{t}AONPD	tAC(min)+ 2	2tCK+ tAC(max) +1	tAC(min)+ 2	2tCK+ tAC(max) +1	ns	
ODT turn-off delay	^{t}AOFD	2.5	2.5	2.5	2.5	tCK	17,44
ODT turn-off	^{t}AOF	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	ns	17,44
ODT turn-off (Power-Down mode)	^{t}AOFPD	tAC(min)+ 2	2.5tCK+ tAC(max) +1	tAC(min)+ 2	2.5tCK+ tAC(max) +1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
Mode register set command cycle time	tMRD	2	-	2	-	tCK	
MRS command to ODT update delay	tMOD	0	12	0	12	ns	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	15

Parameter	Symbol	DDR2-667		DDR2-800		Unit	Note
		min	max	min	max		
Clock cycle time, CL=x	tCK(avg)	3000	8000	2500	8000	ps	35,36
CK high-level width	tCH(avg)	0.48	0.52	0.48	0.52	tCK (avg)	35,36
CK low-level width	tCL(avg)	0.48	0.52	0.48	0.52	tCK (avg)	35,36
Write command to DQS associated clock edge	WL	RL - 1		RL - 1		nCK	
First DQS latching transition to associated clock edge	tDQSS	- 0.25	+ 0.25	- 0.25	+ 0.25	tCK	30
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK	30
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK	30
DQS input high pulse width	tDQSH	0.35	-	0.35	-	tCK	
DQS input low pulse width	tDQSL	0.35	-	0.35	-	tCK	
Write preamble	tWPRE	0.35	-	0.35	-	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Address and control input setup time	tIS(base)	200	-	175	-	ps	5,7,9,22 ,29
Address and control input hold time	tIH(base)	275	-	250	-	ps	5,7,9,23 .29
Control & Address input pulse width for each input	tIPW	0.6	-	0.6	-	tCK (avg)	
DQ and DM input setup time	tDS (base)	100	-	50	-	ps	6,7,8,20 ,28,31
DQ and DM input hold time	tDH (base)	175	-	125	-	ps	6,7,8,21 ,28.31
DQ and DM input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK	
DQ output access time from CK/$\overline{CK}$	tAC	-450	+450	-400	+400	ps	40
DQS output access time from CK/$\overline{CK}$	tDQSCK	-400	+400	-350	+350	ps	40
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	-	tAC,max	-	tAC,max	ps	18,40
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC,min	tAC,max	tAC,min	tAC,max	ps	18,40
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	ps	18,40
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	240	-	200	ps	13
CK half period	tHP	Min (tCH(abs), tCL(abs))	-	Min (tCH(abs), tCL(abs))	-	ps	37
DQ hold skew factor	tQHS	-	340	-	300	ps	38
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	tHP - tQHS	-	ps	39
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	19,41
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	19,42
Active to active command period for 1KB page size products	tRRD	7.5	-	7.5	-	ns	4,32
Active to active command period for 2KB page size products	tRRD	10	-	10	-	ns	4,32

-Continue-

Parameter	Symbol	DDR2-667		DDR2-800		Unit	Note
		min	max	min	max		
Four Active Window for 1KB page size products	tFAW	37.5	-	35	-	ns	32
Four Active Window for 2KB page size products	tFAW	50	-	45	-	ns	32
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	-	15	-	ns	32
Auto precharge write recovery + precharge time	tDAL	WR+tnRP	-	WR+tnRP	-	tCK	14
Internal write to read command delay	tWTR	7.5	-	7.5	-	ns	24,32
Internal read to precharge command delay	tRTP	7.5		7.5		ns	3,32
CKE minimum pulse width (high and low pulse width)	tCKE	3	-	3	-	tCK	27
Exit self refresh to a non-read command	tXSNR	tRFC + 10	-	tRFC + 10	-	ns	32
Exit self refresh to a read command	tXSRD	200	-	200	-	tCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	tCK	
Exit active power down to read command	tXARD	2		2		tCK	1
Exit active power down to read command (Slow exit, Lower power)	tXARDS	7 - AL		8 - AL		tCK	1, 2
ODT turn-on delay	tAOND	2	2	2	2	tCK	16
ODT turn-on	tAON	tAC,min	tAC,max +0.7	tAC,min	tAC,max +0.7	ns	6,16,40
ODT turn-on(Power-Down mode)	tAONPD	tAC,min+2	2tCK(avg) +tAC,max +1	tAC,min+2	2tCK(avg) +tAC,max +1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK	17,45
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max) +0.6	ns	17.43, 45
ODT turn-off (Power-Down mode)	tAOFPD	tAC,min +2	2.5tCK(avg)+tAC,max +1	tAC(min) +2	2.5tCK(avg)+tAC,max +1	ns	
ODT to power down entry latency	tANPD	3	-	3	-	tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
Mode register set command cycle time	tMRD	2	-	2	-	tCK	
MRS command to ODT update delay	tMOD	0	12	0	12	ns	32
OCD drive mode output delay	tOIT	0	12	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK(av g)+tIH		tIS+tCK(a vg)+tIH		ns	15

General notes, which may apply for all AC parameters

1. Slew Rate Measurement Levels

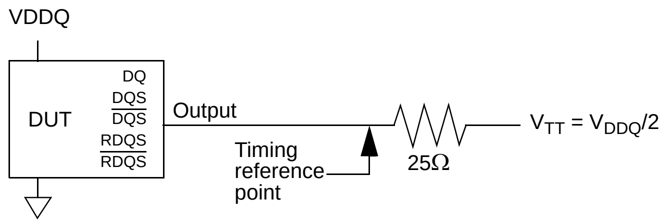
a. Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals.
For differential signals (e.g. DQS - $\overline{DQS}$) output slew rate is measured between DQS - $\overline{DQS}$ = -500 mV and DQS - $\overline{DQS}$ = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

b. Input slew rate for single ended signals is measured from dc-level to ac-level: from VIL(dc) to VIH(ac) for rising edges and from VIH(dc) and VIL(ac) for falling edges.
For differential signals (e.g. CK - $\overline{CK}$) slew rate for rising edges is measured from CK - $\overline{CK}$ = -250 mV to CK - $\overline{CK}$ = +500 mV(250mV to -500 mV for falling egdes).

c. VID is the magnitude of the difference between the input voltage on CK and the input voltage on $\overline{CK}$, or between DQS and $\overline{DQS}$ for differential strobe.

2. DDR2 SDRAM AC timing reference load

The following figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

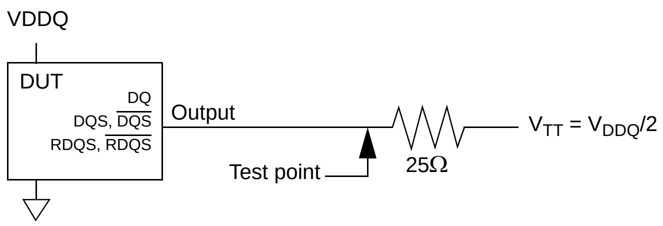


AC Timing Reference Load

The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. DQS) signal.

3. DDR2 SDRAM output slew rate test load

Output slew rate is characterized under the test conditions as shown below.



Slew Rate Test Load

4. Differential data strobe

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single

VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10 K ohm resistor to insure proper operation.

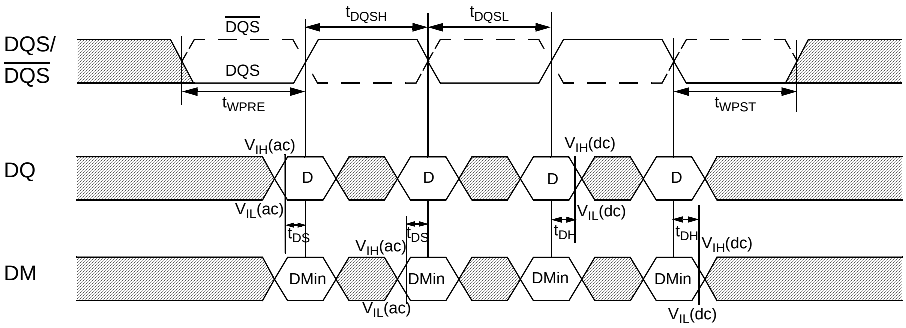


Figure -- Data input (write) timing

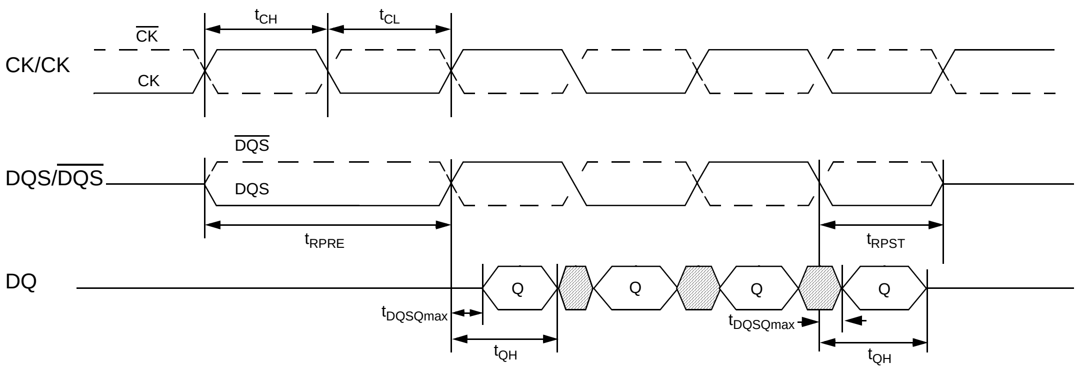


Figure -- Data output (read) timing

5. AC timings are for linear signal transitions. See System Derating for other signal transitions.

6. These parameters guarantee device behavior, but they are not necessarily tested on each device.
They may be guaranteed by device design or tester correlation.

7. All voltages referenced to VSS.

8. Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific Notes for dedicated AC parameters

1. User can choose which active power down exit timing to use via MRS(bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing where a lower power value is defined by each vendor data sheet.

2. AL = Additive Latency

3. This is a minimum requirement. Minimum read to precharge timing is AL + BL/2 providing the tRTP and tRAS(min) have been satisfied.

4. A minimum of two clocks (2 * tCK or 2 * nCK) is required irrespective of operating frequency

5. Timings are specified with command/address input slew rate of 1.0 V/ns. See System Derating for other slew rate values.

6. Timings are guaranteed with DQs, DM, and DQS's(DQS/RDQS in singled ended mode) input slew rate of 1.0 V/ns. See System Derating for other slew rate values.

7. Timings are specified with CK/$\overline{CK}$ differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode. See System Derating for other slew rate values.

8. tDS and tDH derating

tDS, tDH Derating Values for DDR2-400, DDR2-533(ALL units in 'ps', Note 1 applies to entire Table)

		DQS, DQS Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew rate V/ns	2.0	125	45	125	45	+125	+45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	83	21	83	21	+83	+21	95	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-11	-14	-11	-14	1	-2	13	10	25	22	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-13	-19	-1	-7	11	5	23	17	-	-	-	-
	0.7	-	-	-	-	-	-	-31	-42	-19	-19	-7	-8	5	-6	17	6	-	-
	0.6	-	-	-	-	-	-	-	-	-43	-59	-31	-47	-19	-35	-7	-23	5	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-74	-89	-62	-77	-50	-65	-38	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-127	-140	-115	-128	-103	-116

tDS, tDH Derating Values for DDR2-667, DDR2-800(ALL units in 'ps', Note 1 applies to entire Table)

		DQS, DQS Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew rate V/ns	2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
	0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
	0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

tDS, tDH Derating Values for DDR2-400, DDR2-533(ALL units in 'ps', Note 1 applies to entire Table)																			
		DQS, Single-ended Slew Rate																	
		2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ Slew rate V/ns	2.0	188	188	167	146	125	63	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	146	167	125	125	83	42	81	43	-	-	-	-	-	-	-	-	-	-
	1.0	63	125	42	83	0	0	-2	1	-7	-13	-	-	-	-	-	-	-	-
	0.9	-	-	31	69	-11	-14	-13	-13	-18	-27	-29	-45	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-27	-30	-32	-44	-43	-62	-60	-86	-	-	-	-
	0.7	-	-	-	-	-	-	-45	-53	-50	-67	-61	-85	-78	-109	-108	-152	-	-
	0.6	-	-	-	-	-	-	-	-	-74	-96	-85	-114	-102	-138	-132	-181	-183	-248
	0.5	-	-	-	-	-	-	-	-	-	-	-128	-156	-145	-180	-175	-223	-226	-288
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-210	-243	-240	-286	-291	-351

1) For all input signals the total tDS(setup time) and tDH(hold time) required is calculated by adding the datasheet value to the derating value listed in Table x.

Setup(tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vih(ac)min. Setup(tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded ' VREF(dc) to ac region', use nominal slew rate for derating value(see Fig a.) If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value(see Fig b.)

Hold(tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc) max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc) min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value(see Fig c.) If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value(see Fig d.)

Although for slow slew rates the total setup time might be negative(i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).
For slew rate in between the values listed in table x, the derating valued may obtained by linear interpolation.
These values are typically not subject to production test. They are verified by design and characterization.

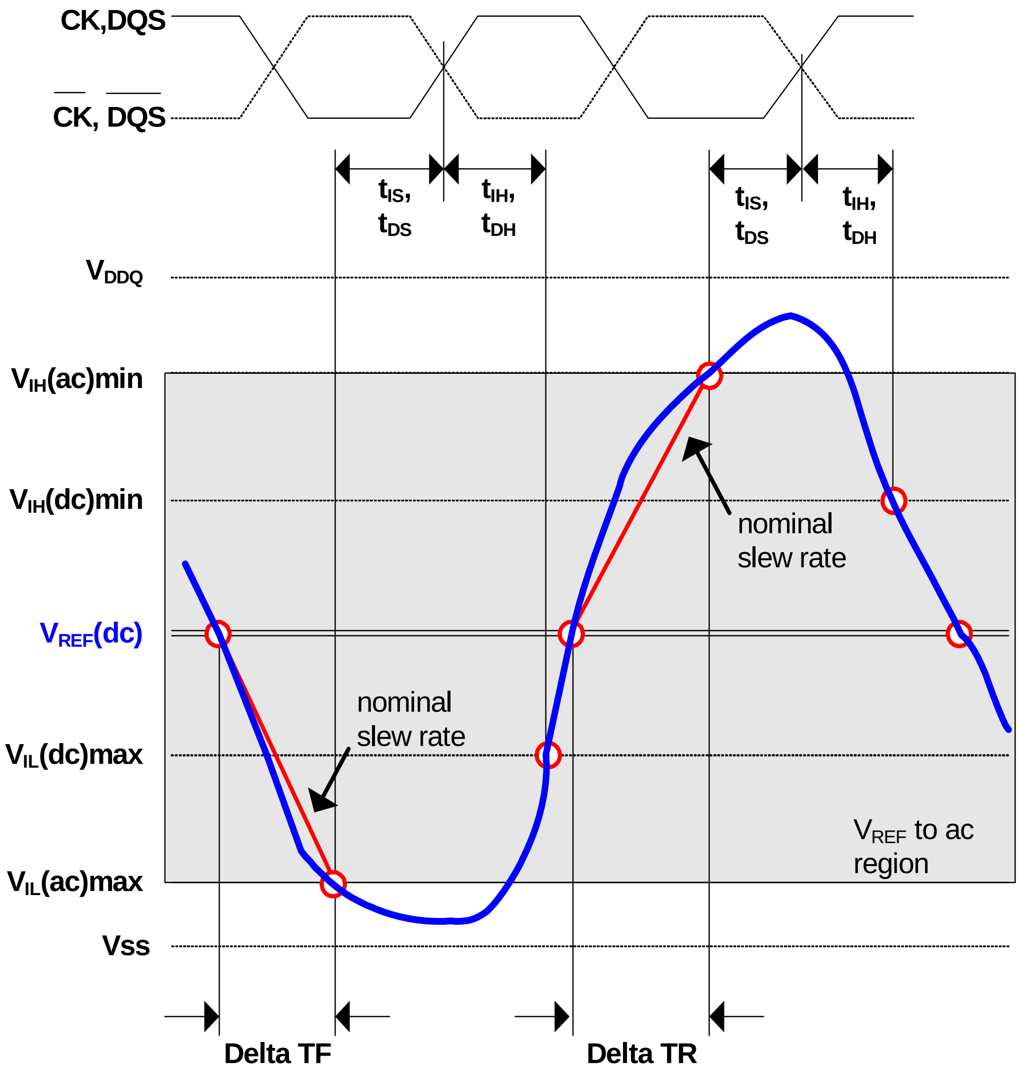
If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V_{REF}(dc) region', the slew rate of a tangent line to the actual signal from the dc level to V_{REF}(dc) level is used for derating value(see Fig d.)

Although for slow rates the total setup time might be negative(i.e. a valid input signal will not have reached $V_{IH/IL}$(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(ac).

For slew rates in between the values listed in table, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

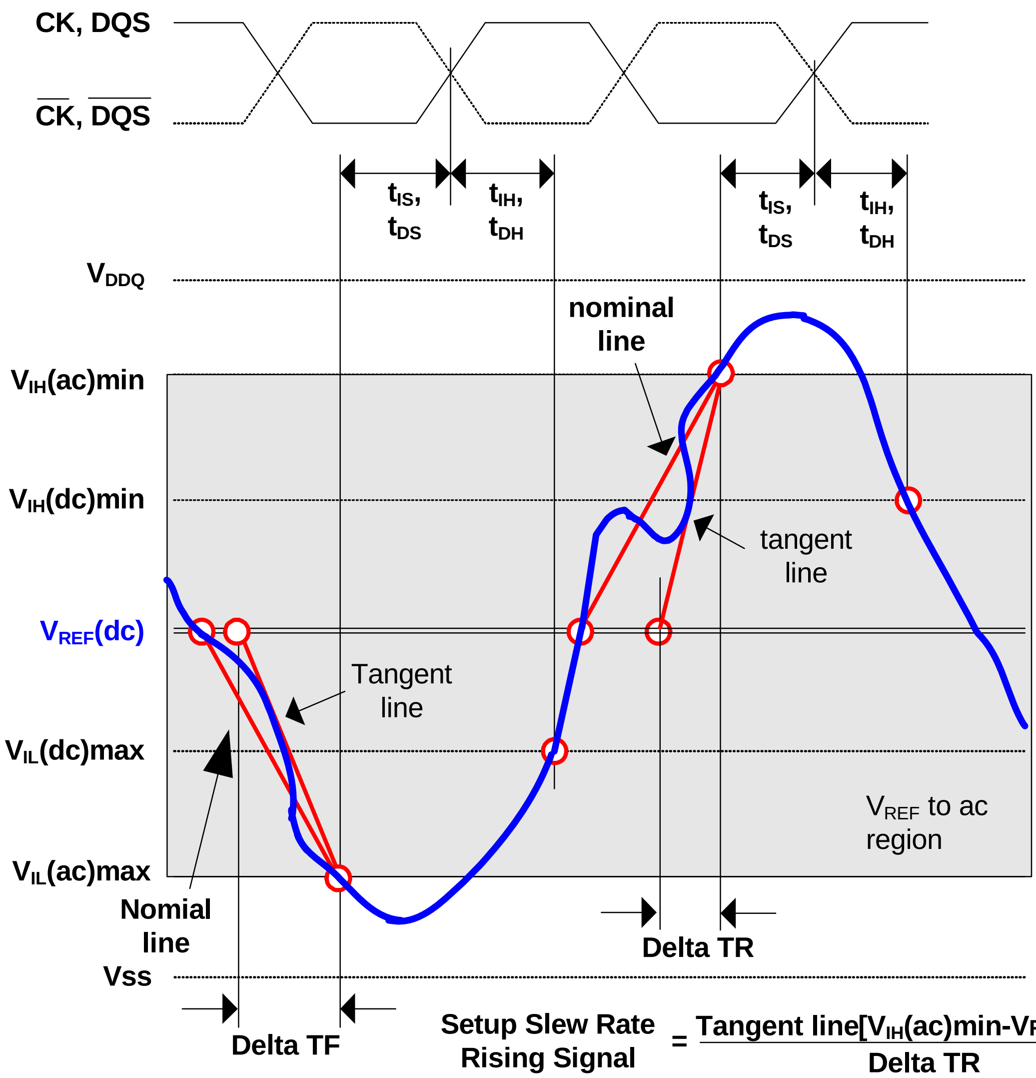
Fig. a Illustration of nominal slew rate for tIS,tDS



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF}(dc) - V_{IL}(ac)max}{\text{Delta TF}}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH}(ac)min - V_{REF}(dc)}{\text{Delta TR}}$$

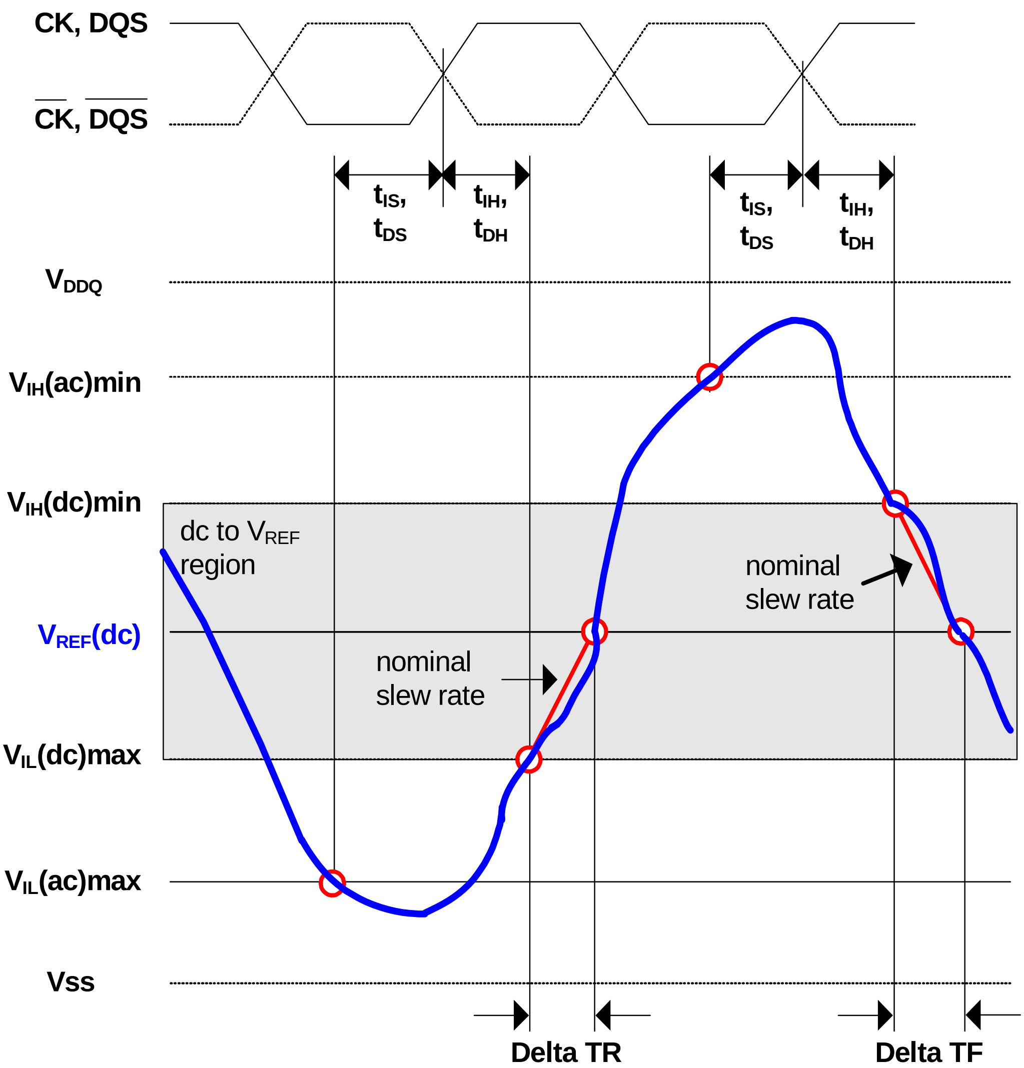
Fig. -b Illustration of tangent line for tIS,tDS



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{Tangent line}[V_{IH}(ac)min - V_{REF}(dc)]}{\text{Delta TR}}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{Tangent line}[V_{REF}(dc) - V_{IL}(ac)max]}{\text{Delta TF}}$$

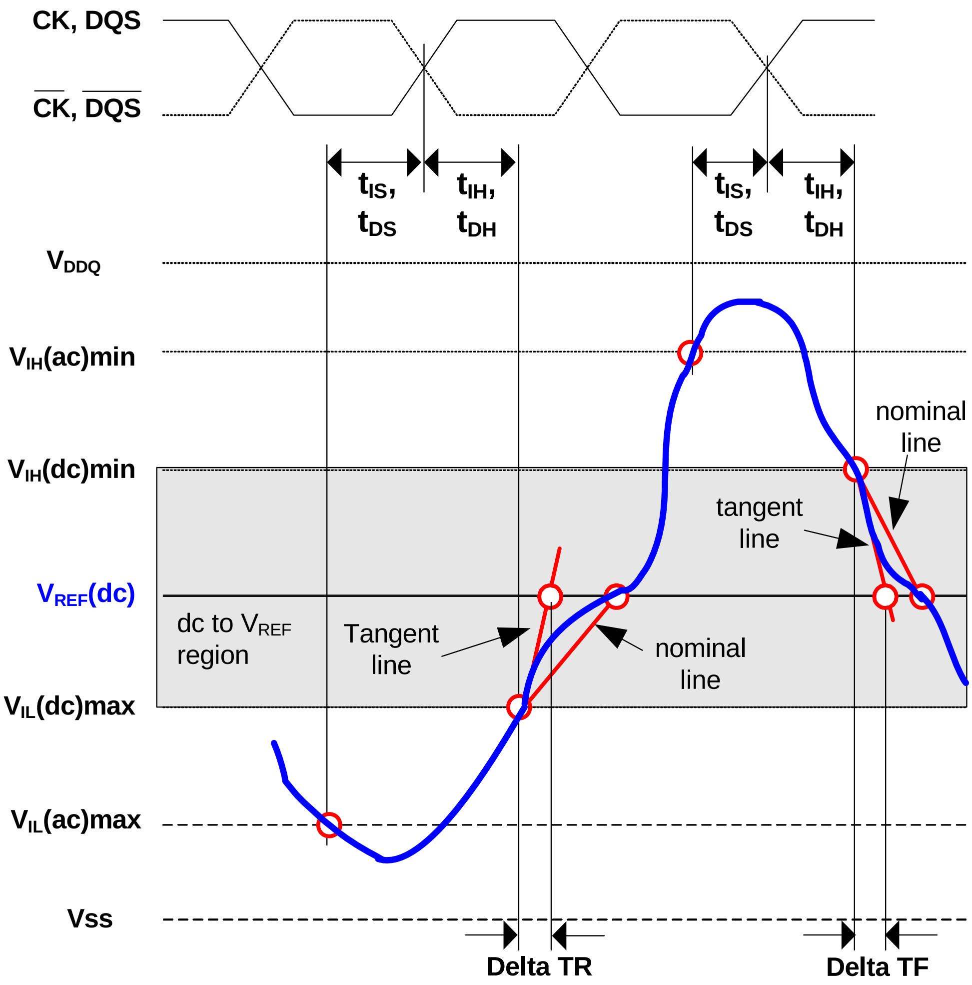
Fig. -c Illustration of nominal line for tIH, tDH



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF}(dc) - V_{IL}(dc)max}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH}(dc)min - V_{REF}(dc)}{\text{Delta TF}}$$

Fig. -d Illustration of tangent line for tIH , tDH



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{Tangent line}[V_{REF}(dc)-V_{IL}(ac)max]}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{Tangent line}[V_{IH}(ac)min-V_{REF}(dc)]}{\text{Delta TF}}$$

9. tIS and tIH (input setup and hold) derating

tIS, tIH Derating Values for DDR2-400, DDR2-533									
		CK, $\overline{CK}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	Units	Notes
Command / Address Slew rate(V/ns)	4.0	+187	+94	+217	+124	+247	+154	ps	1
	3.5	+179	+89	+209	+119	+239	+149	ps	1
	3.0	+167	+83	+197	+113	+227	+143	ps	1
	2.5	+150	+75	+180	+105	+210	+135	ps	1
	2.0	+125	+45	+155	+75	+185	+105	ps	1
	1.5	+83	+21	+113	+51	+143	+81	ps	1
	1.0	+0	0	+30	+30	+60	+60	ps	1
	0.9	-11	-14	+19	+16	+49	+46	ps	1
	0.8	-25	-31	+5	-1	+35	+29	ps	1
	0.7	-43	-54	-13	-24	+17	+6	ps	1
	0.6	-67	-83	-37	-53	-7	-23	ps	1
	0.5	-110	-125	-80	-95	-80	-65	ps	1
	0.4	-175	-188	-145	-158	-115	-128	ps	1
	0.3	-285	-292	-255	-262	-225	-232	ps	1
	0.25	-350	-375	-320	-345	-290	-315	ps	1
	0.2	-525	-500	-495	-470	-465	-440	ps	1
	0.15	-800	-708	-770	-678	-740	-648	ps	1
	0.1	-1450	-1125	-1420	-1095	-1390	-1065	ps	1

tIS, tIH Derating Values for DDR2-667, DDR2-800									
		CK, $\overline{CK}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	Units	Notes
Command / Address Slew rate(V/ns)	4.0	+150	+94	+180	+124	+210	+154	ps	1
	3.5	+143	+89	+173	+119	+203	+149	ps	1
	3.0	+133	+83	+163	+113	+193	+143	ps	1
	2.5	+120	+75	+150	+105	+180	+135	ps	1
	2.0	+100	+45	+130	+75	+150	+105	ps	1
	1.5	+67	+21	+97	+51	+127	+81	ps	1
	1.0	0	0	+30	+30	+60	+60	ps	1
	0.9	-5	-14	+25	+16	+55	+46	ps	1
	0.8	-13	-31	+17	-1	+47	+29	ps	1
	0.7	-22	-54	+8	-24	+38	+6	ps	1
	0.6	-34	-83	-4	-53	+26	-23	ps	1
	0.5	-60	-125	-30	-95	0	-65	ps	1
	0.4	-100	-188	-70	-158	-40	-128	ps	1
	0.3	-168	-292	-138	-262	-108	-232	ps	1
	0.25	-200	-375	-170	-345	-140	-315	ps	1
	0.2	-325	-500	-395	-470	-265	-440	ps	1
	0.15	-517	-708	-487	-678	-457	-648	ps	1
	0.1	-1000	-1125	-970	-1095	-940	-1065	ps	1

1) For all input signals the total tIS(setup time) and tIH(hold) time) required is calculated by adding the data-sheet value to the derating value listed in above Table.

Setup(tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF}(dc) and the first crossing of V_{IH}(ac)min. Setup(tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF}(dc) and the first crossing of V_{IL}(ac)max. If the actual signal is always earlier than the nominal slew rate for line between shaded 'V_{REF}(dc) to ac region', use nominal slew rate for derating value(see fig a.) If the actual signal is later than the nominal slew rate line anywhere between shaded 'V_{REF}(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value(see Fig b.)

Hold(tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of V_{REF}(dc). Hold(tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF}(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to V_{REF}(dc) region', use nominal slew rate for derating value(see Fig.c) If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V_{REF}(dc) region', the slew rate of a tangent line to the actual signal from the dc level to V_{REF}(dc) level is used for derating value(see Fig d.)

Although for slow rates the total setup time might be negative(i.e. a valid input signal will not have reached $V_{IH/IL}$(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(ac).

For slew rates in between the values listed in table, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

10. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

11. MIN (t CL, t CH) refers to the smaller of the actual clock LOW time and the actual clock HIGH time as provided to the device (i.e. this value can be greater than the minimum specification limits for t CL and t CH). For example, t CL and t CH are = 50% of the period, less the half period jitter (t JIT(HP)) of the clock source, and less the half period jitter due to crosstalk (t JIT(crosstalk)) into the clock traces.

12. t QH = t HP – t QHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock HIGH or clock LOW (tCH, tCL).
tQHS accounts for:
1) The pulse duration distortion of on-chip clock circuits; and
2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

13. tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS/ $\overline{\text{DQS}}$ and associated DQ in any given cycle.

14. t DAL = (nWR) + (tRP/tCK):
For each of the terms above, if not already an integer, round to the next highest integer. tCK refers to the application clock period. nWR refers to the t WR parameter stored in the MR.
Example: For DDR533 at t CK = 3.75 ns with t WR programmed to 4 clocks. tDAL = 4 + (15 ns / 3.75 ns) clocks =4 +(4)clocks=8clocks.

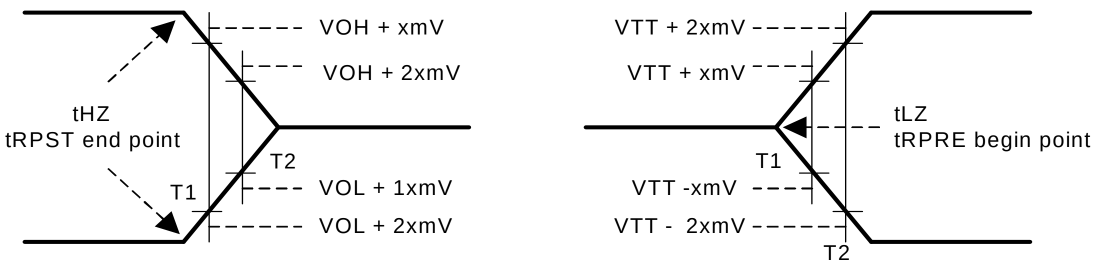
15. The clock frequency is allowed to change during self–refresh mode or precharge power-down mode.
In case of clock frequency change during precharge power-down, a specific procedure is required as described in section 2.9.

16. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.

17. ODT turn off time min is when the device starts to turn off ODT resistance.
ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

18. tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begins driving (tLZ). Below figure shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

19. tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). Below figure shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE). Below Figure shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

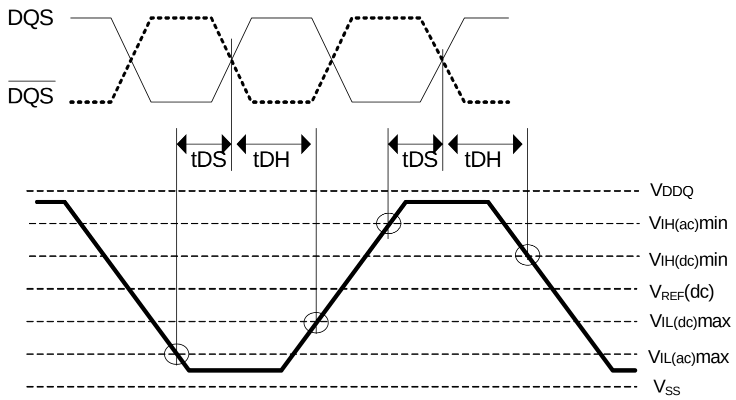


tHZ , tRPST end point = 2*T1-T2 tLZ , tRPRE begin point = 2*T1-T2

20. Input waveform timing with differential data strobe enabled MR[bit10] =0, is referenced from the input signal crossing at the V_{IH}(ac) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the V_{IL}(ac) level to the differential data strobe crosspoint for a falling signal applied to the device under test.

21. Input waveform timing with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the V_{IH}(dc) level to the differential data strobe crosspoint for a rising signal and V_{IL}(dc) to the differential data strobe crosspoint for a falling signal applied to the device under test.

Differential Input waveform timing



22. Input waveform timing is referenced from the input signal crossing at the V_{IH}(ac) level for a rising signal and V_{IL}(ac) for a falling signal applied to the device under test.

23. Input waveform timing is referenced from the input signal crossing at the V_{IL}(dc) level for a rising signal and V_{IH}(dc) for a falling signal applied to the device under test.

24. tWTR is at least two clocks (2 x tCK or 2 x nCK) independent of operation frequency.

25. Input waveform timing with single-ended data strobe enabled MR[bit10] = 1, is referenced from the input signal crossing at the VIH (ac) level to the single-ended data strobe crossing VIH/L (dc) at the start of its transition for a rising signal, and from the input signal crossing at the VIL (ac) level to the single-ended data strobe crossing VIH/L (dc) at the start of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between Vil(dc)max and Vih (dc) min.

26. Input waveform timing with single-ended data strobe enabled MR[bit10] = 1, is referenced from the input signal crossing at the VIH(dc) level to the single-ended data strobe crossing VIH/L(ac) at the end of its transition for a rising signal, and from the input signal crossing at the VIL(dc) level to the single-ended data strobe crossing VIH/L(ac) at the end of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between Vil(dc)max and Vih (dc) min.

27. tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.

28. If tDS or tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

29. These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT (per), tJIT (cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

30. These parameters are measured from a data strobe signal ((L/U/R)DQS/DQS) crossing to its respective clock signal (CK/CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT (per), tJIT (cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

31. These parameters are measured from a data signal ((L/U) DM, (L/U) DQ0, (L/U) DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS/DQS) crossing.

32. For these parameters, the DDR2 SDRAM device is characterized and verified to support

tnPARAM = RU {tPARAM / tCK (avg)}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.
For example, the device will support tnRP = RU {tRP / tCK (avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2-667 5-5-5, of which tRP = 15ns, the device will support tnRP =RU {tRP / tCK (avg)} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm+5 is valid even if (Tm+5 - Tm) is less than 15ns due to input clock jitter.

33. tDAL [nCK] = WR [nCK] + tnRP [nCK] = WR + RU {tRP [ps] / tCK (avg) [ps]}, where WR is the value programmed in the mode register set.

34. New units, ‘tCK (avg)’ and ‘nCK’, are introduced in DDR2-667 and DDR2-800.
Unit ‘tCK (avg)’ represents the actual tCK (avg) of the input clock under operation.
Unit ‘nCK’, represents one clock cycle of the input clock, counting the actual clock edges.
Note that in DDR2-400 and DDR2-533, ‘tCK’, is used for both concepts.
ex) tXP = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm+2, even if (Tm+2 - Tm) is 2 x tCK (avg) + tERR(2per),min.

35. Input clock jitter spec parameter. These parameters and the ones in the table below are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2-667 and DDR2-800 only. The jitter specified is a random jitter meeting a Gaussian distribution.

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		min	max	min	max		
Clock period jitter	tJIT (per)	-125	125	-100	100	ps	35
Clock period jitter during DLL locking period	tJIT (per, lck)	-100	100	-80	80	ps	35
Cycle to cycle clock period jitter	tJIT (cc)	-250	250	-200	200	ps	35
Cycle to cycle clock period jitter during DLL locking period	tJIT (cc, lck)	-200	200	-160	160	ps	35
Cumulative error across 2 cycles	tERR(2per)	-175	175	-150	150	ps	35
Cumulative error across 3 cycles	tERR(3per)	-225	225	-175	175	ps	35
Cumulative error across 4 cycles	tERR(4per)	-250	250	-200	200	ps	35
Cumulative error across 5 cycles	tERR(5per)	-250	250	-200	200	ps	35
Cumulative error across n cycles, n=6...10, inclusive	tERR(6~10per)	-350	350	-300	300	ps	35
Cumulative error across n cycles, n=11...50, inclusive	tERR(11~50per)	-450	450	-450	450	ps	35
Duty cycle jitter	tJIT (duty)	-125	125	-100	100	ps	35

36. These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min and max of SPEC values are to be used for calculations in the table below.)

Parameter	Symbol	min	max	Units
Absolute clock period	tCK (abs)	tCK (avg), min + tJIT (per), min	tCK (avg), max + tJIT (per), max	ps
Absolute clock HIGH pulse width	tCH (abs)	tCH (avg), min * tCK (avg), min + tJIT (per), min	tCH (avg), max * tCK (avg), max + tJIT (per), max	ps
Absolute clock LOW pulse width	tCL (abs)	tCL (avg), min * tCK (avg), min + tJIT (per), min	tCL (avg), max * tCK (avg), max + tJIT (per), max	ps

Example: For DDR2-667, tCH (abs), min = (0.48 x 3000 ps) - 125 ps = 1315 ps

37. tHP is the minimum of the absolute half period of the actual input clock. tHP is an input parameter but not an input specification parameter. It is used in conjunction with tQHS to derive the DRAM output timing tQH.
The value to be used for tQH calculation is determined by the following equation;
tHP = Min (tCH (abs), tCL (abs)),
where,
tCH (abs) is the minimum of the actual instantaneous clock HIGH time;
tCL (abs) is the minimum of the actual instantaneous clock LOW time;

38. tQHS accounts for:
1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual tHP at the input is transferred to the output; and
2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to n-channel variation of the output drivers

39. tQH = tHP ? tQHS, where:
tHP is the minimum of the absolute half period of the actual input clock; and
tQHS is the specification value under the max column.
{The less half-pulse width distortion present, the larger the tQH value is; and the larger the valid data eye will be.}
Examples:
1) If the system provides tHP of 1315 ps into a DDR2-667 SDRAM, the DRAM provides tQH of 975 ps minimum.
2) If the system provides tHP of 1420 ps into a DDR2-667 SDRAM, the DRAM provides tQH of 1080 ps minimum.

40. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 ps and tERR(6-10per), max = + 293 ps, then tDQSCK, min (derated) = tDQSCK, min - tERR(6-10per),max = -

400 ps - 293 ps = - 693 ps and tDQSCK, max (derated) = tDQSCK, max - tERR(6-10per),min = 400 ps + 272 ps = + 672 ps. Similarly, tLZ (DQ) for DDR2-667 derates to tLZ (DQ), min (derated) = - 900 ps - 293 ps = - 1193 ps and tLZ (DQ), max (derated) = 450 ps + 272 ps = + 722 ps. (Caution on the min/max usage!)

41. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT (per) of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tJIT (per), min = - 72 ps and tJIT (per), max = + 93 ps, then tRPRE, min (derated) = tRPRE, min + tJIT (per), min = 0.9 x tCK (avg) - 72 ps = + 2178 ps and tRPRE, max (derated) = tRPRE, max + tJIT (per), max = 1.1 x tCK (avg) + 93 ps = + 2843 ps. (Caution on the min/max usage!)

42. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT (duty) of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tJIT (duty), min = - 72 ps and tJIT (duty), max = + 93 ps, then tRPST, min (derated) = tRPST, min + tJIT (duty), min = 0.4 x tCK (avg) - 72 ps = + 928 ps and tRPST, max (derated) = tRPST, max + tJIT (duty), max = 0.6 x tCK (avg) + 93 ps = + 1592 ps. (Caution on the min/max usage!)

43. When the device is operated with input clock jitter, this parameter needs to be derated by {- tJIT (duty), max - tERR(6-10per),max} and {- tJIT (duty), min - tERR(6-10per),min} of the actual input clock.(output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 ps, tERR(6-10per), max = + 293 ps, tJIT (duty), min = - 106 ps and tJIT (duty), max = + 94 ps, then tAOF, min (derated) = tAOF, min + {- tJIT (duty), max - tERR(6-10per),max} = - 450 ps + {- 94 ps - 293 ps} = - 837 ps and tAOF, max (derated) = tAOF, max + {- tJIT (duty), min - tERR(6-10per),min} = 1050 ps + {106 ps + 272 ps} = + 1428 ps. (Caution on the min/max usage!)

44. For tAOFD of DDR2-400/533, the 1/2 clock of tCK in the 2.5 x tCK assumes a tCH, input clock HIGH pulse width of 0.5 relative to tCK. tAOF, min and tAOF, max should each be derated by the same amount as the actual amount of tCH offset present at the DRAM input with respect to 0.5. For example, if an input clock has a worst case tCH of 0.45, the tAOF, min should be derated by subtracting 0.05 x tCK from it, whereas if an input clock has a worst case tCH of 0.55, the tAOF, max should be derated by adding 0.05 x tCK to it. Therefore, we have;
tAOF, min (derated) = tAC, min - [0.5 - Min(0.5, tCH, min)] x tCK
tAOF, max (derated) = tAC, max + 0.6 + [Max(0.5, tCH, max) - 0.5] x tCK
or
tAOF, min (derated) = Min (tAC, min, tAC, min - [0.5 - tCH, min] x tCK)
tAOF, max (derated) = 0.6 + Max (tAC, max, tAC, max + [tCH, max - 0.5] x tCK)
where tCH, min and tCH, max are the minimum and maximum of tCH actually measured at the DRAM input balls.

45. For tAOFD of DDR2-667/800, the 1/2 clock of nCK in the 2.5 x nCK assumes a tCH (avg), average input clock HIGH pulse width of 0.5 relative to tCK (avg). tAOF, min and tAOF, max should each be derated by the same amount as the actual amount of tCH (avg) offset present at the DRAM input with respect

to 0.5. For example, if an input clock has a worst case tCH (avg) of 0.48, the tAOF, min should be derated by subtracting 0.02 x tCK (avg) from it, whereas if an input clock has a worst case tCH (avg) of 0.52, the tAOF, max should be derated by adding 0.02 x tCK (avg) to it. Therefore, we have;

tAOF, min (derated) = tAC, min - [0.5 - Min(0.5, tCH (avg), min)] x tCK (avg)

tAOF, max (derated) = tAC, max + 0.6 + [Max(0.5, tCH (avg), max) - 0.5] x tCK (avg)

or

tAOF, min (derated) = Min (tAC, min, tAC, min - [0.5 - tCH (avg), min] x tCK (avg))

tAOF, max (derated) = 0.6 + Max (tAC, max, tAC, max + [tCH (avg), max - 0.5] x tCK (avg))

where tCH (avg), min and tCH (avg), max are the minimum and maximum of tCH (avg) actually measured at the DRAM input balls.

Note that these deratings are in addition to the tAOF derating per input clock jitter, i.e. tJIT (duty) and tERR(6-10per). However tAC values used in the equations shown above are from the timing parameter table and are not derated. Thus the final derated values for tAOF are;

tAOF, min (derated _ final) = tAOF, min (derated) + {- tJIT (duty), max - tERR(6-10per),max}

tAOF, max (derated _ final) = tAOF, max (derated) + {- tJIT (duty), min - tERR(6-10per),min}

512Mb DDR2 SDRAM

DDR2-1066

For purposes of IDD testing, the following parameters are to be utilized

Speed Bin (CL-tRCD-tRP)	DDR2-1066	Units
	7-7-7	
CL(IDD)	7	tCK
tRCD(IDD)	13.125	ns
tRC(IDD)	58.125	ns
tRRD(IDD)-x16	10	ns
tFAW-x16	45	ns
tCK(IDD)	1.875	ns
tRASmin(IDD)	45	ns
tRASmax(IDD)	70000	ns
tRP(IDD)	13.125	ns
tRFC(IDD)-256Mb	75	ns
tRFC(IDD)-512Mb	105	ns
tRFC(IDD)-1Gb	127.5	ns

Detailed IDD7

The detailed timings are shown below for IDD7. Changes will be required if timing parameter changes are made to the specification.

Legend: A = Active; RA = Read with Autoprecharge; D = Deselect

IDD7: Operating Current: All Bank Interleave Read operation

All banks are being interleaved at minimum tRC(IDD) without violating tRRD(IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOUT = 0mA

Timing Patterns for 4 bank devices x16

-DDR2-1066 7-7-7: A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D D D D D

3.5. Input/Output Capacitance

Parameter	Symbol	DDR2- 1066		Units
		Min	Max	
Input capacitance, CK and $\overline{CK}$	CCK	1.0	2.0	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	x	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	1.75	pF
Input capacitance delta, all other input-only pins	CDI	x	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	2.5	3.5	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	x	0.5	pF

4. Electrical Characteristics & AC Timing Specification

(-40℃ $\leq T_{CASE} \leq$ 95℃; V_{DDQ} = 1.8 V +/- 0.1V; V_{DD} = 1.8V +/- 0.1V)

Refresh Parameters by Device Density

Parameter	Symbol		256Mb	512Mb	1Gb	2Gb	4Gb	Units
Refresh to Active /Refresh command time	tRFC		75	105	127.5	195	327.5	ns
Average periodic refresh interval	tREFI	-40℃ $\leq T_{CASE} \leq$ 85℃	7.8	7.8	7.8	7.8	7.8	us
		85℃ < $T_{CASE} \leq$ 95℃	3.9	3.9	3.9	3.9	3.9	us

DDR2 SDRAM speed bins and tRCD, tRP and tRC for corresponding bin

Speed	DDR2-1066	Units
Bin(CL-tRCD-tRP)	7-7-7	
Parameter	min	
CAS Latency	7	tCK
tRCD : ACT to RD(A) or WT(A) Delay	13.125	ns
tRP : PRE to ACT Delay	13.125	ns
tRAS : ACT to PRE Delay	45 min / 70000 max	ns
tRC : ACT to ACT Delay	58.125	ns
tCK(avg) @ CL=7	1.875 min / 7.5 max	ns

Timing Parameters by Speed Grade

(Refer to notes for information related to this table at the following pages of this table)

Parameter	Symbol	DDR2-1066		Unit	Note
		min	max		
DQ output access time from CK/$\overline{\text{CK}}$	tAC	-350	+350	ps	35
DQS output access time from CK/$\overline{\text{CK}}$	tDQSCK	-325	+325	ps	35
CK high-level width	tCH	0.48	0.52	tCK	30, 31
CK low-level width	tCL	0.48	0.52	tCK	30, 31
CK half period	tHP	min (tCL,tCH)	-	ps	32
Clock cycle time, CL=x	tCK	1875	7500	ps	30, 31
DQ and DM input setup time (differential strobe)	tDS (base)	0	-	ps	6,7,8, 17, 23, 26
DQ and DM input hold time (differential strobe)	tDH (base)	75	-	ps	6,7,8, 16, 23, 26
Control & Address input pulse width for each input	tIPW	0.6	-	tCK(avg)	
DQ and DM input pulse width for each input	tDIPW	0.35	-	tCK(avg)	
Data-out high-impedance time from CK/$\overline{\text{CK}}$	tHZ	-	tAC max	ps	15, 35
DQS low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQS)	tAC min	tAC max	ps	15, 35
DQ low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQ)	2*tAC min	tAC max	ps	15, 35
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	175	ps	11
DQ hold skew factor	tQHS	-	250	ps	33
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	ps	34
First DQS latching transition to associated clock edge	tDQSS	-0.25	+ 0.25	tCK(avg)	25
DQS input high pulse width	tDQSH	0.35	-	tCK(avg)	
DQS input low pulse width	tDQSL	0.35	-	tCK(avg)	
DQS falling edge to CK setup time	tDSS	0.2	-	tCK(avg)	25
DQS falling edge hold time from CK	tDSH	0.2	-	tCK(avg)	25
Mode register set command cycle time	tMRD	2	-	tCK	
Write postamble	tWPST	0.4	0.6	tCK(avg)	10
Write preamble	tWPRE	0.35	-	tCK(avg)	
Address and control input setup time	tIS(base)	125	-	ps	5,7,9, 19, 24
Address and control input hold time	tIH(base)	200	-	ps	5,7,9, 20, 24

-Continue-

(Refer to notes for information related to this table at the following pages of this table)

Parameter	Symbol	DDR2-1066		Unit	Note
		min	max		
Read preamble	tRPRE	0.9	1.1	tCK(avg)	16, 36
Read postamble	tRPST	0.4	0.6	tCK(avg)	16, 37
Active to active command period for 2KB page size products	tRRD	10	-	ns	4, 27
Four Active Window for 2KB page size products	tFAW	45	-	ns	27
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay	tCCD	2		tCK	
Write recovery time	tWR	15	-	ns	27
Auto precharge write recovery + precharge time	tDAL	WR+tRP	-	tCK	28
Internal write to read command delay	tWTR	7.5	-	ns	21, 27
Internal read to precharge command delay	tRTP	7.5		ns	3, 27
Exit self refresh to a non-read command	tXSNR	tRFC + 10		ns	27
Exit self refresh to a read command	tXSRD	200	-	tCK	
Exit precharge power down to any non-read command	tXP	3	-	tCK	
Exit active power down to read command	tXARD	3		tCK	1
Exit active power down to read command (Slow exit, Lower power)	tXARDS	10 - AL		tCK	1, 2
CKE minimum pulse width (high and low pulse width)	tCKE	3		tCK	22
ODT turn-on delay	tAOND	2	2	tCK	13
ODT turn-on	tAON	tAC(min)	tAC(max) +2.575	ns	6, 13, 35
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	3tCK+ tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	tCK	14, 39
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	ns	14, 38, 39
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK avg+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	4		tCK	
ODT power down exit latency	tAXPD	11		tCK	
OCD drive mode output delay	tOIT	0	12	ns	27
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK(avg) +tIH		ns	12

General notes, which may apply for all AC parameters

1. Slew Rate Measurement Levels

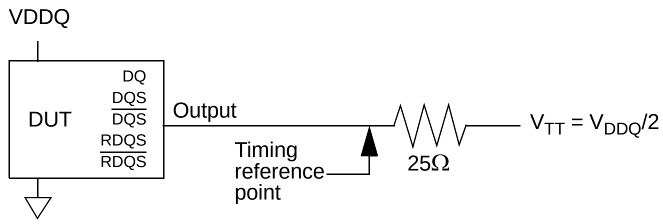
a. Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals.
For differential signals (e.g. DQS - $\overline{\text{DQS}}$) output slew rate is measured between DQS - $\overline{\text{DQS}}$ = -500 mV and DQS - $\overline{\text{DQS}}$ = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

b. Input slew rate for single ended signals is measured from dc-level to ac-level: from VIL(dc) to VIH(ac) for rising edges and from
VIH(dc) and VIL(ac) for falling edges.
For differential signals (e.g. CK - $\overline{\text{CK}}$) slew rate for rising edges is measured from CK - $\overline{\text{CK}}$ = -250 mV to CK - $\overline{\text{CK}}$ = +500 mV(250mV to -500 mV for falling egdes).

c. VID is the magnitude of the difference between the input voltage on CK and the input voltage on $\overline{\text{CK}}$, or between DQS and $\overline{\text{DQS}}$ for differential strobe.

2. DDR2 SDRAM AC timing reference load

The following figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

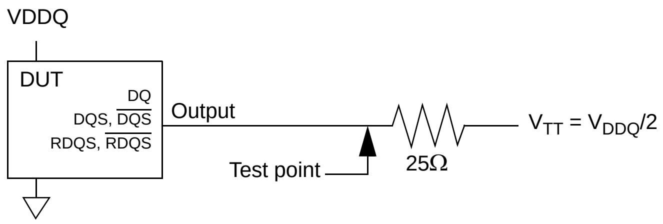


AC Timing Reference Load

The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. DQS) signal.

3. DDR2 SDRAM output slew rate test load

Output slew rate is characterized under the test conditions as shown below.



Slew Rate Test Load

4. Differential data strobe

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single

VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 ohm to 10 K ohm resistor to insure proper operation.

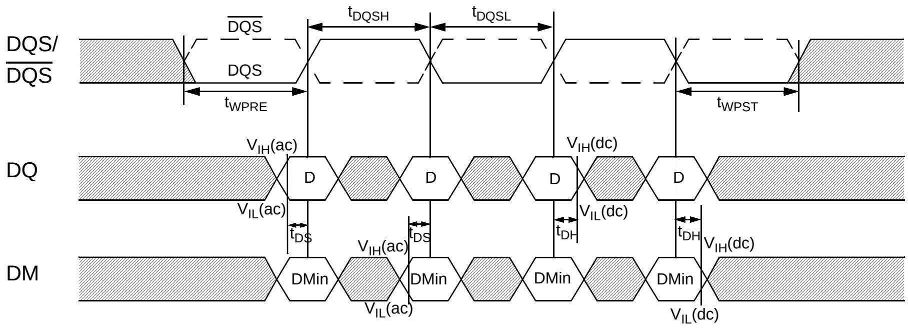


Figure -- Data input (write) timing

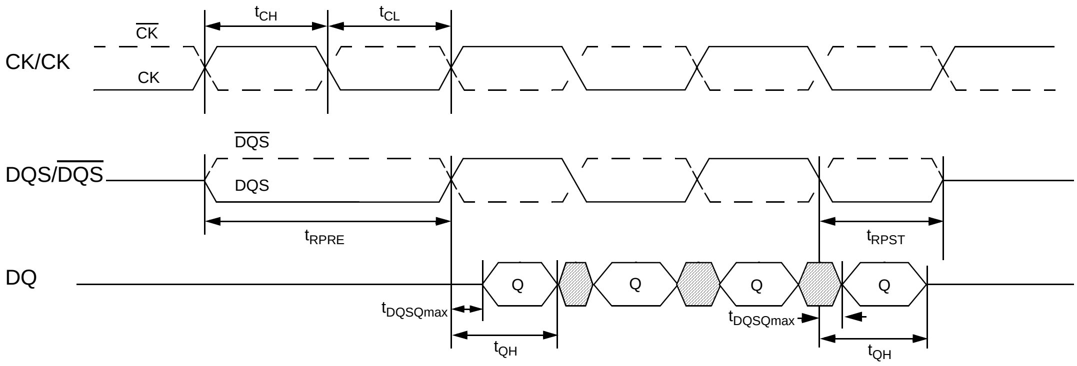


Figure -- Data output (read) timing

5. AC timings are for linear signal transitions. See System Derating for other signal transitions.

6. All voltages referenced to VSS.

7. These parameters guarantee device behavior, but they are not necessarily tested on each device.
They may be guaranteed by device design or tester correlation.

8. Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

Specific Notes for dedicated AC parameters

1. User can choose which active power down exit timing to use via MRS(bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing where a lower power value is defined by each vendor data sheet.

2. AL = Additive Latency

3. This is a minimum requirement. Minimum read to precharge timing is AL + BL/2 providing the tRTP and tRAS(min) have been satisfied.

4. A minimum of two clocks (2 * tCK) is required irrespective of operating frequency

5. Timings are guaranteed with command/address input slew rate of 1.0 V/ns. See System Derating for other slew rate values.

6. Timings are guaranteed with data, mask, and (DQS/RDQS in singled ended mode) input slew rate of 1.0 V/ns.

See System Derating for other slew rate values.

7. Timings are guaranteed with CK/$\overline{CK}$ differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differen tial slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode. See System Derating for other slew rate values.

tDS, tDH Derating Values for DDR2-1066(ALL units in 'ps', Note 1 applies to entire Table)																			
		DQS, $\overline{DQS}$ Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		△ tDS	△ tDH	△ tDS	△ tDH	△ tDS	△ tDH	△ tDS	△ tDH	△ tDS	△ tDH	△ tDS	△ tDH	△ tDS	△ tDH	△ tDS	△ tDH	△ tDS	△ tDH
DQ Slew rate V/ns	2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
	0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
	0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

1) For all input signals the total tIS(setup time) and tIH(hold) time) required is calculated by adding the data-sheet value to the derating value listed in above Table.

Setup(tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF}(dc) and the first crossing of V_{IH}(ac)min. Setup(tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF}(dc) and the first crossing of V_{IL}(ac)max. If the actual signal is always earlier than the nominal slew rate for line between shaded 'V_{REF}(dc) to ac region', use nominal slew rate for derating value(see fig a.) If the actual signal is later than the nominal slew rate line anywhere between shaded 'V_{REF}(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value(see Fig b.)

Hold(tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of V_{REF}(dc). Hold(tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF}(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to V_{REF}(dc) region', use nominal slew rate for derating value(see Fig.c)

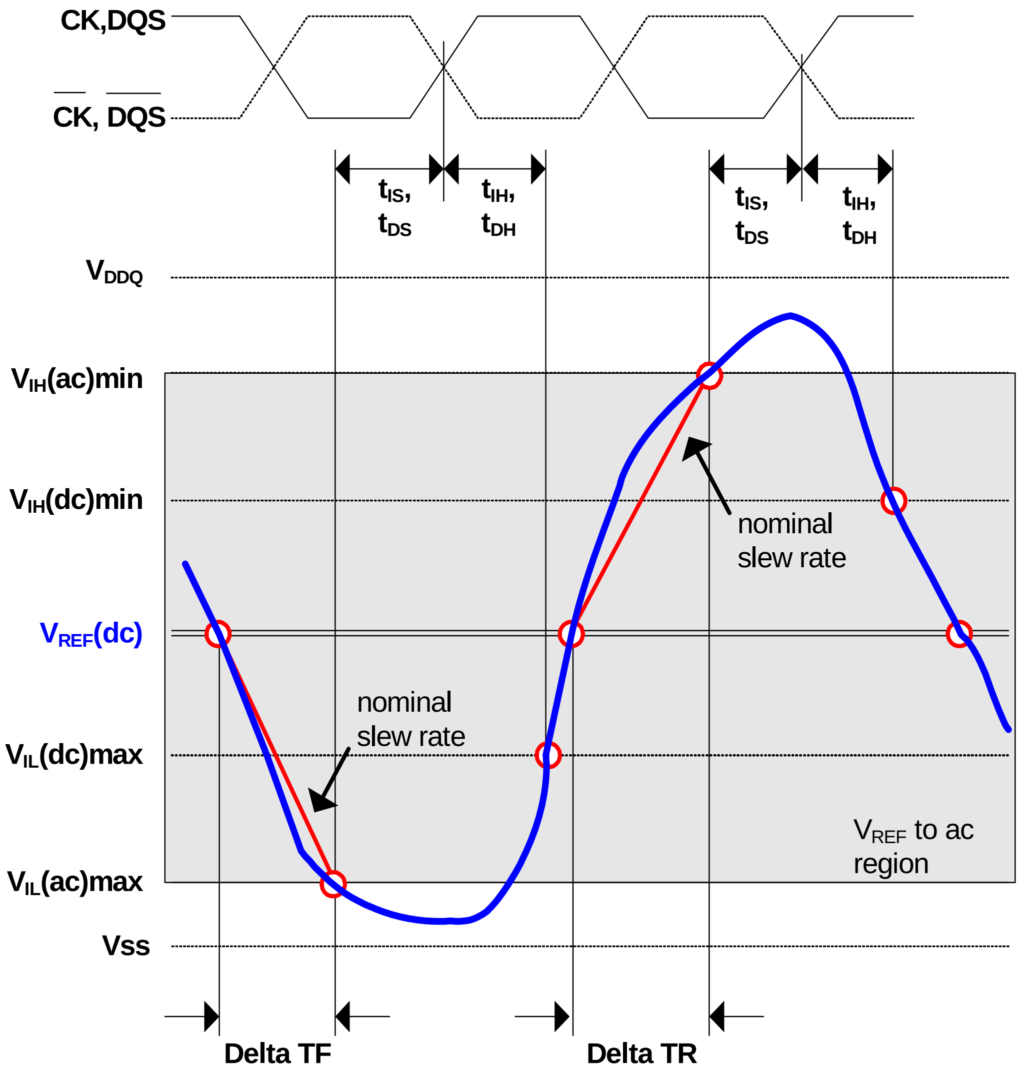
If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V_{REF}(dc) region', the slew rate of a tangent line to the actual signal from the dc level to V_{REF}(dc) level is used for derating value(see Fig d.)

Although for slow rates the total setup time might be negative(i.e. a valid input signal will not have reached $V_{IH/IL}$(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(ac).

For slew rates in between the values listed in table, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

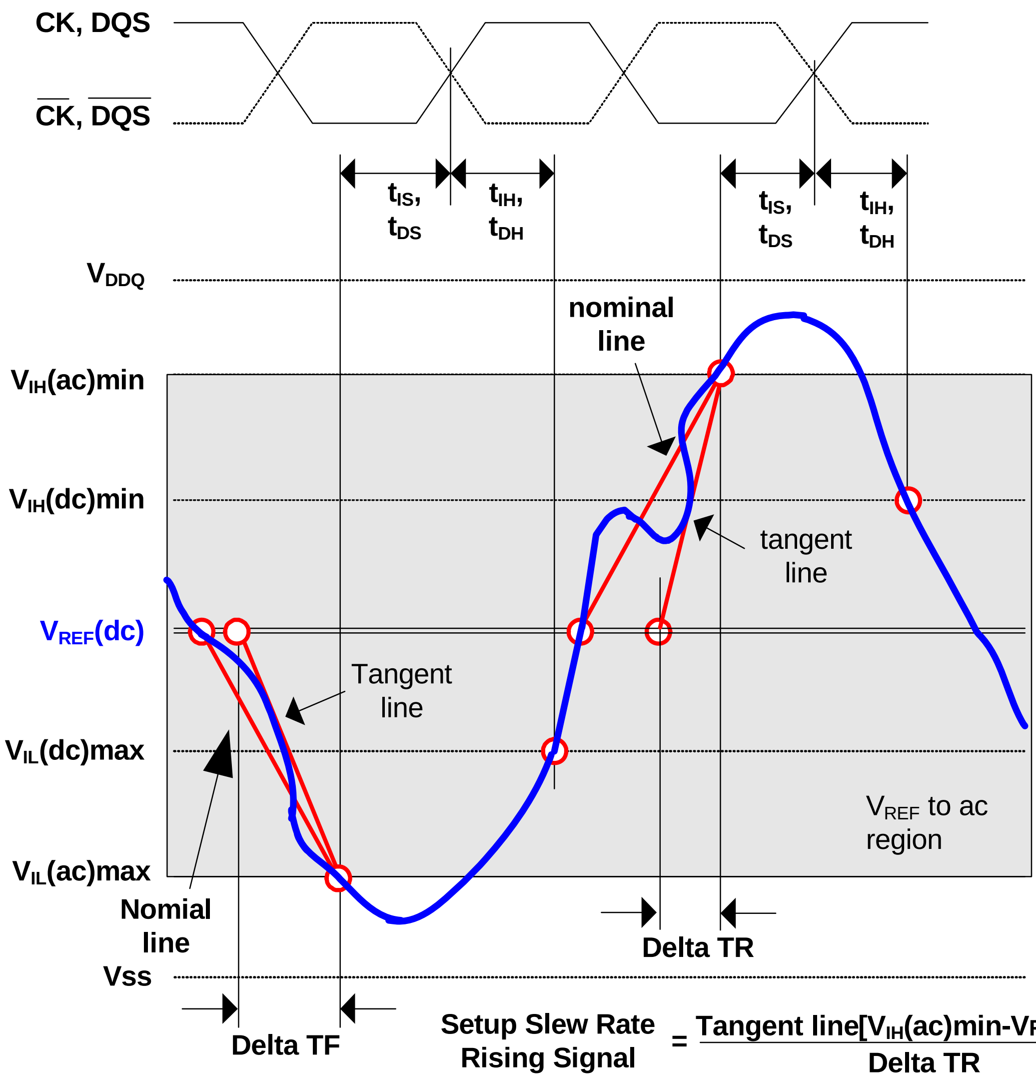
Fig. a Illustration of nominal slew rate for tIS,tDS



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF}(dc) - V_{IL}(ac)max}{\text{Delta TF}}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH}(ac)min - V_{REF}(dc)}{\text{Delta TR}}$$

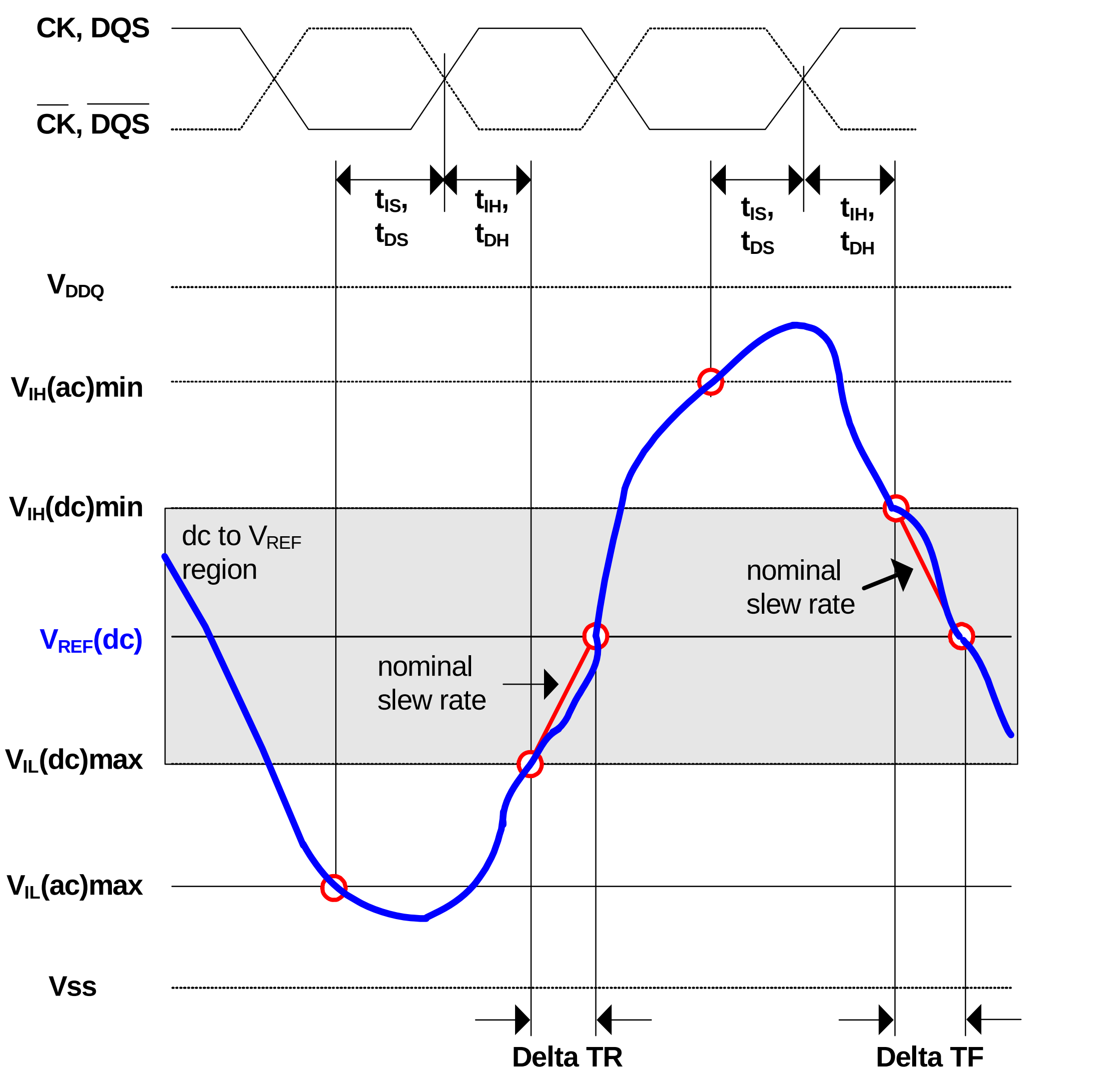
Fig. -b Illustration of tangent line for tIS,tDS



Setup Slew Rate Rising Signal = Tangent line[V_{IH}(ac)min-V_{REF}(dc)] / Delta TR

Setup Slew Rate Falling Signal = Tangent line[V_{REF}(dc)-V_{IL}(ac)max] / Delta TF

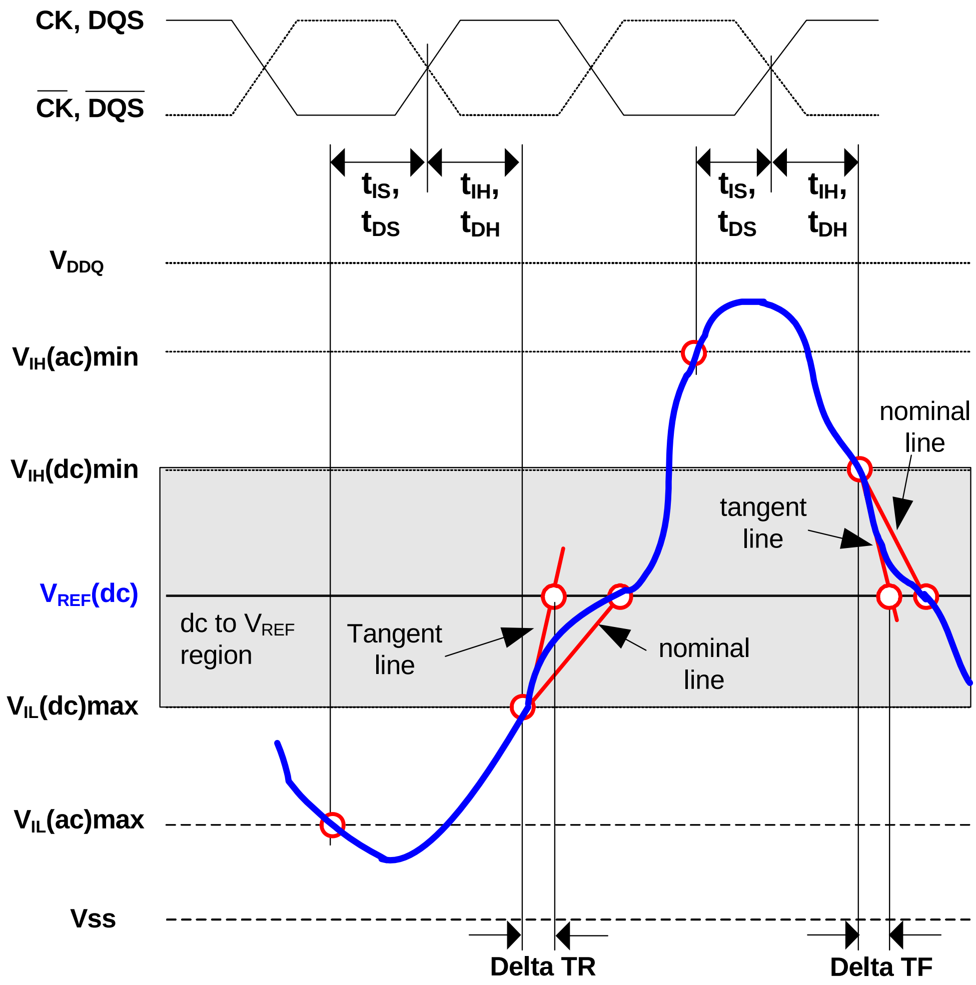
Fig. -c Illustration of nominal line for tIH, tDH



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF}(dc) - V_{IL}(dc)max}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH}(dc)min - V_{REF}(dc)}{\text{Delta TF}}$$

Fig. -d Illustration of tangent line for tIH , tDH



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{Tangent line}[V_{REF}(dc) - V_{IL}(ac)max]}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{Tangent line}[V_{IH}(ac)min - V_{REF}(dc)]}{\text{Delta TF}}$$

10. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

11. tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / DQS and associated DQ in any given cycle.

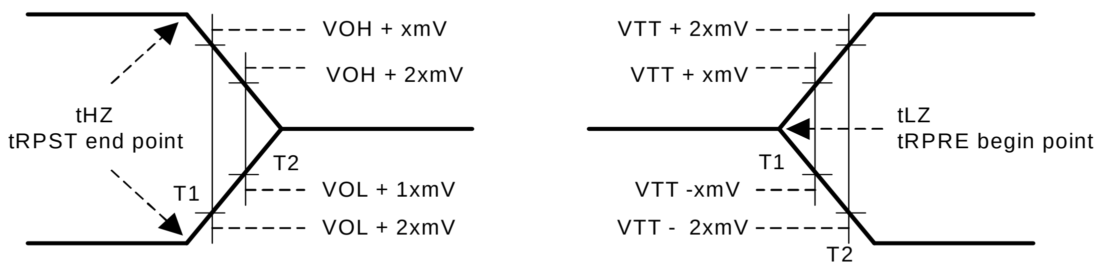
12. The clock frequency is allowed to change during self–refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required as described in section ***Input clock frequency change during precharge power down***.

13. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND, which is interpreted as 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

14. ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD, which is interpreted as 0.5 x tCK(avg) [ns] after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges. For DDR2-1066, this is 0.9375 [ns] (= 0.5 x 1.875 [ns]) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

15. tHZ and tLZ transitions occur in the same access time as valid data transitions. Thesed parameters are referenced to a specific voltage level which specifies when the device output is no longer driving(tHZ), or begins driving (tLZ). Below figure shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistenet.

16. tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). Below figure shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE). Below Figure shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

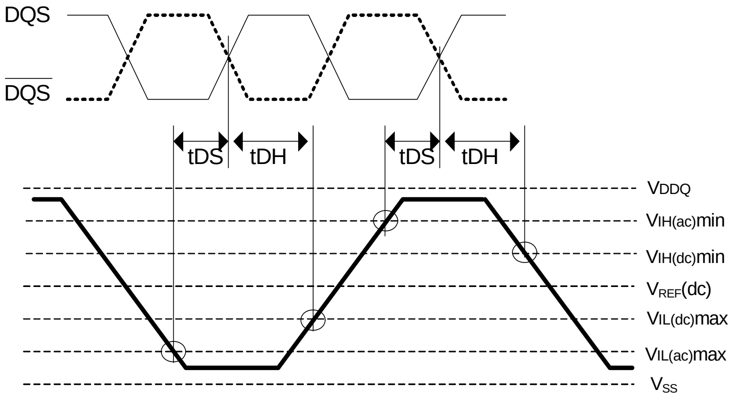


tHZ , tRPST end point = 2*T1-T2   tLZ , tRPRE begin point = 2*T1-T2

17. Input waveform timing tDS with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the VIH(ac) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the VIL(ac) level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between Vil(dc)max and Vih(dc)min.

18. Input waveform timing tDH with differential data strobe enabled MR[bit10]=0, is referenced from the differential data strobe crosspoint to the input signal crossing at the VIH(dc) level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the VIL(dc) level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between Vil(dc)max and Vih(dc)min.

Differential Input waveform timing



19. Input waveform timing is referenced from the input signal crossing at the VIH(ac) level for a rising signal and VIL(ac) for a falling signal applied to the device under test.

20. Input waveform timing is referenced from the input signal crossing at the VIL(dc) level for a rising signal and VIH(dc) for a falling signal applied to the device under test.

21. tWTR is at lease two clocks (2 x nCK) independent of operation frequency.

22. tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2* tCK + tIH.

23. If tDS or tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

24. These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

25. These parameters are measured from a data strobe signal ((L/U/R)DQS/$\overline{\text{DQS}}$) crossing to its respective clock signal (CK/$\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

26. These parameters are measured from a data signal ((L/U) DM, (L/U) DQ0, (L/U) DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS/DQS) crossing.

27. For these parameters, the DDR2 SDRAM device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.
For example, the device will support tnRP = RU {tRP / tCK(avg)}, which is in clock cycles, if all input clock jitterspecifications are met. This means: For DDR2-1066 7-7-7, of which tRP = 13.125ns, the device will support tnRP =RU{tRP / tCK(avg)} = 7, i.e. as long as the input clock jitter specifications are met, Pre-charge command at Tm and Active command at Tm+7 is valid even if (Tm+7 - Tm) is less than 13.127ns due to input clock jitter.

28. Specific Note 28 tDAL [nCK] = WR [nCK] + tnRP [nCK] = WR + RU {tRP [ps] / tCK(avg) [ps] }, where WR is the value programmed in the mode register set and RU stands for round up.
Example: For DDR2-1066 7-7-7 at tCK(avg) = 1.875 ns with WR programmed to 8 nCK,
tDAL = 8 + RU {13.125 ns / 1.875 ns} [nCK] = 8 + 7 [nCK] = 15 [nCK]

29.New units, 'tCK(avg)' and 'nCK', are introduced in DDR2-1066.
Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation.
Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
ex) tXP = 3 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm+3, even if (Tm+3 - Tm) is 3 x tCK(avg) + tERR(3per),min.

30. Input clock jitter spec parameter. These parameters and the ones in the table below are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2-1066. The jitter specified is a random jitter meeting a Gaussian distribution.

Parameter	Symbol	DDR2-1066		Units	Notes
		min	max		
Clock period jitter	tJIT(per)	-90	90	ps	30
Clock period jitter during DLL locking period	tJIT(per,lck)	-80	80	ps	30
Cycle to cycle clock period jitter	tJIT(cc)	-180	180	ps	30
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	-160	160	ps	30
Cumulative error across 2 cycles	tERR(2per)	-132	132	ps	30
Cumulative error across 3 cycles	tERR(3per)	-157	157	ps	30
Cumulative error across 4 cycles	tERR(4per)	-175	175	ps	30
Cumulative error across 5 cycles	tERR(5per)	-188	188	ps	30
Cumulative error across n cycles, n=6...10, inclusive	tERR(6~10per)	-250	250	ps	30
Cumulative error across n cycles, n=11...50, inclusive	tERR(11~50per)	-425	425	ps	30
Duty cycle jitter	tJIT(duty)	-75	75	ps	30

31. These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min and max of SPEC values are to be used for calculations in the table below.

Parameter	Symbol	min	max	Units
Absolute clock period	tCK(abs)	tCK(avg),min+tJIT(per),min	tCK(avg),max+tJIT(per),max	ps
Absolute clock HIGH pulse width	tCH(abs)	tCH(avg),min x tCK(avg),min + tJIT(duty),min	tCH(avg),max x tCK(avg),max + tJIT(duty),max	ps
Absolute clock LOW pulse width	tCL(abs)	tCL(avg),min x tCK(avg),min + tJIT(duty),min	tCL(avg),max x tCK(avg),max + tJIT(duty),max	ps

Example: For DDR2-1066, tCH(abs),min = (0.48 x 1875 ps) - 75 ps = 825 ps

32. tHP is the minimum of the absolute half period of the actual input clock. tHP is an input parameter but not an input specification parameter. It is used in conjunction with tQHS to derive the DRAM output timing tQH.

The value to be used for tQH calculation is determined by the following equation;
tHP = Min (tCH(abs), tCL(abs)),
where,
tCH(abs) is the minimum of the actual instantaneous clock HIGH time;
tCL(abs) is the minimum of the actual instantaneous clock LOW time;

33. tQHS accounts for:
1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual tHP at the input is transferred to the output; and
2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to n-channel variation of the output drivers

34. tQH = tHP - tQHS, where:
tHP is the minimum of the absolute half period of the actual input clock; and
tQHS is the specification value under the max column.
{The less half-pulse width distortion present, the larger the tQH value is; and the larger the valid data eye will be.}
Examples:
1) If the system provides tHP of 1315 ps into a DDR2-1066 SDRAM, the DRAM provides tQH of 575 ps minimum.
2) If the system provides tHP of 900 ps into a DDR2-1066 SDRAM, the DRAM provides tQH of 650 ps minimum.

35. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-1066 SDRAM has tERR(6-10per),min = - 202 ps and tERR(6-10per),max = + 223 ps,
then tDQSCK,min(derated) = tDQSCK,min - tERR(6-10per),max = - 300 ps - 223 ps = - 523 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(6-10per),min = 300 ps + 202 ps = + 502 ps. Similarly, tLZ(DQ) for DDR2-1066 derates to tLZ(DQ),min(derated) = - 700 ps - 223 ps = - 923 ps and tLZ(DQ),max(derated) = 350 ps + 202 ps = + 552 ps. (Caution on the min/max usage!)

36. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per) of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-1066 SDRAM has tJIT(per),min = - 72 ps and tJIT(per),max = + 63 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),min = 0.9 x tCK(avg) - 72 ps = + 1615.5 ps and tRPRE,max(derated) = tRPRE,max + tJIT(per),max = 1.1 x tCK(avg) + 63 ps = + 2125.5 ps. (Caution on the min/max usage!)

37. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(duty) of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-1066 SDRAM has tJIT(duty),min = - 72 ps and tJIT(duty),max = + 63 ps, then tRPST,min(derated) = tRPST,min + tJIT(duty),min = 0.4 x tCK(avg) - 72 ps = + 678 ps and tRPST,max(derated) = tRPST,max + tJIT(duty),max = 0.6 x tCK(avg) + 63 ps = + 1188 ps. (Caution on the min/max usage!)

38 When the device is operated with input clock jitter, this parameter needs to be derated by { - tJIT(duty),max - tERR(6-10per),max } and { - tJIT(duty),min - tERR(6-10per),min } of the actual input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-1066 SDRAM has tERR(6-10per),min = - 202 ps, tERR(6-10per),max = + 223 ps, tJIT(duty),min = - 66 ps and tJIT(duty),max = + 74 ps, then tAOF,min(derated) = tAOF,min + { - tJIT(duty),max - tERR(6-10per),max } = - 350 ps + { - 74 ps - 223 ps} = - 647 ps and tAOF,max(derated) = tAOF,max + { - tJIT(duty),min - tERR(6-10per),min } = 950 ps + { 66 ps + 202 ps } = + 1218 ps. (Caution on the min/max usage!)

39. For tAOFD of DDR2-1066, the 1/2 clock of nCK in the 2.5 x nCK assumes a tCH(avg), average input clock HIGH pulse width of 0.5 relative to tCK(avg). tAOF,min and tAOF,max should each be derated by the same amount as the actual amount of tCH(avg) offset present at the DRAM input with respect to 0.5. For example, if an input clock has a worst case tCH(avg) of 0.48, the tAOF,min should be derated by subtracting 0.02 x tCK(avg) from it, whereas if an input clock has a worst case tCH(avg) of 0.52, the tAOF,max should be derated by adding 0.02 x tCK(avg) to it. Therefore, we have;

tAOF,min(derated) = tAC,min - [0.5 - Min(0.5, tCH(avg),min)] x tCK(avg)

tAOF,max(derated) = tAC,max + 0.6 + [Max(0.5, tCH(avg),max) - 0.5] x tCK(avg)

or

tAOF,min(derated) = Min(tAC,min, tAC,min - [0.5 - tCH(avg),min] x tCK(avg))

tAOF,max(derated) = 0.6 + Max(tAC,max, tAC,max + [tCH(avg),max - 0.5] x tCK(avg))

where tCH(avg),min and tCH(avg),max are the minimum and maximum of tCH(avg) actually measured at the DRAM input balls.

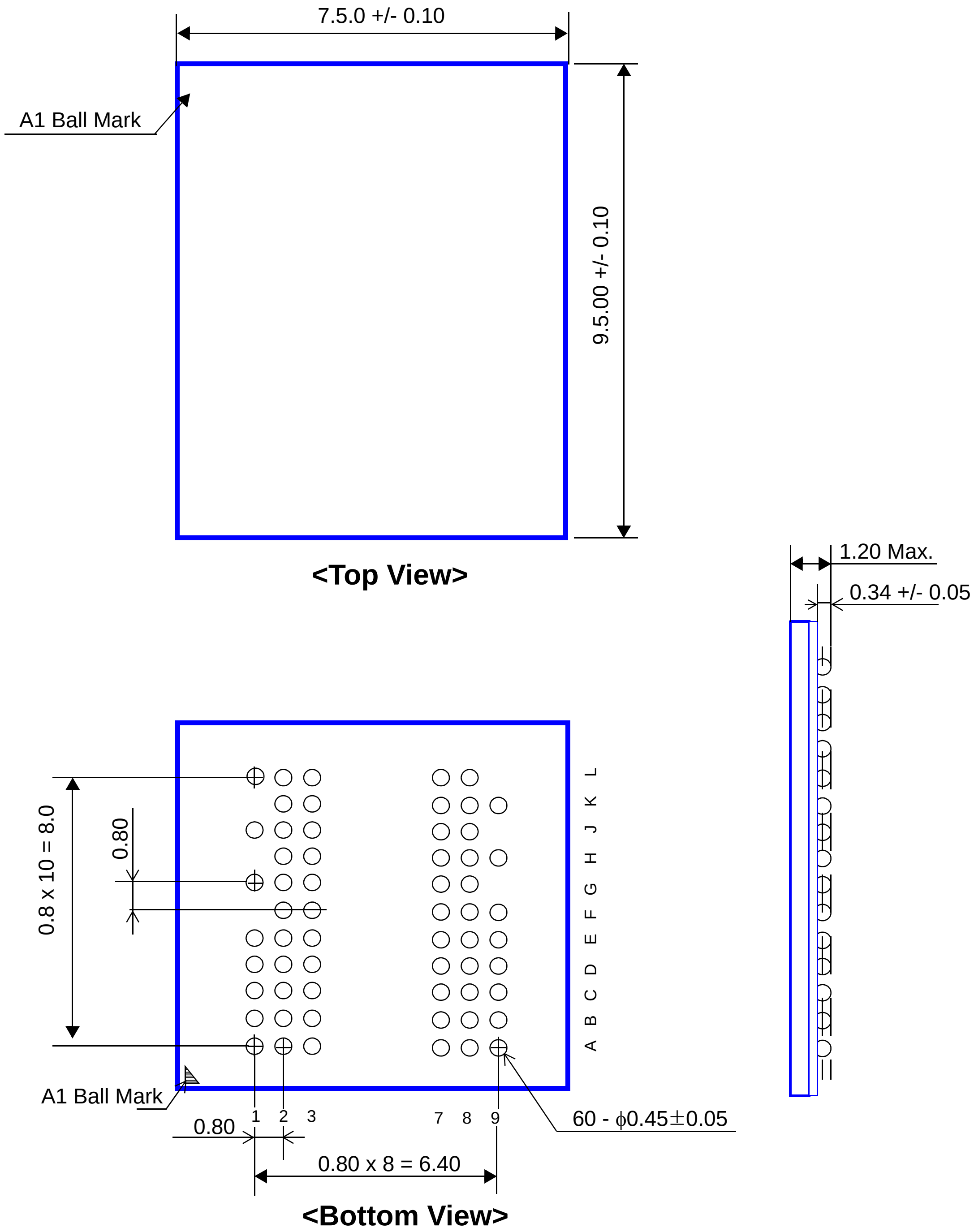
Note that these deratings are in addition to the tAOF derating per input clock jitter, i.e. tJIT(duty) and tERR(6-10per). However tAC values used in the equations shown above are from the timing parameter table and are not derated.
Thus the final derated values for
tAOF are;

tAOF,min(derated_final) = tAOF,min(derated) + { - tJIT(duty),max - tERR(6-10per),max }

tAOF,max(derated_final) = tAOF,max(derated) + { - tJIT(duty),min - tERR(6-10per),min }

Package Dimension(x8)

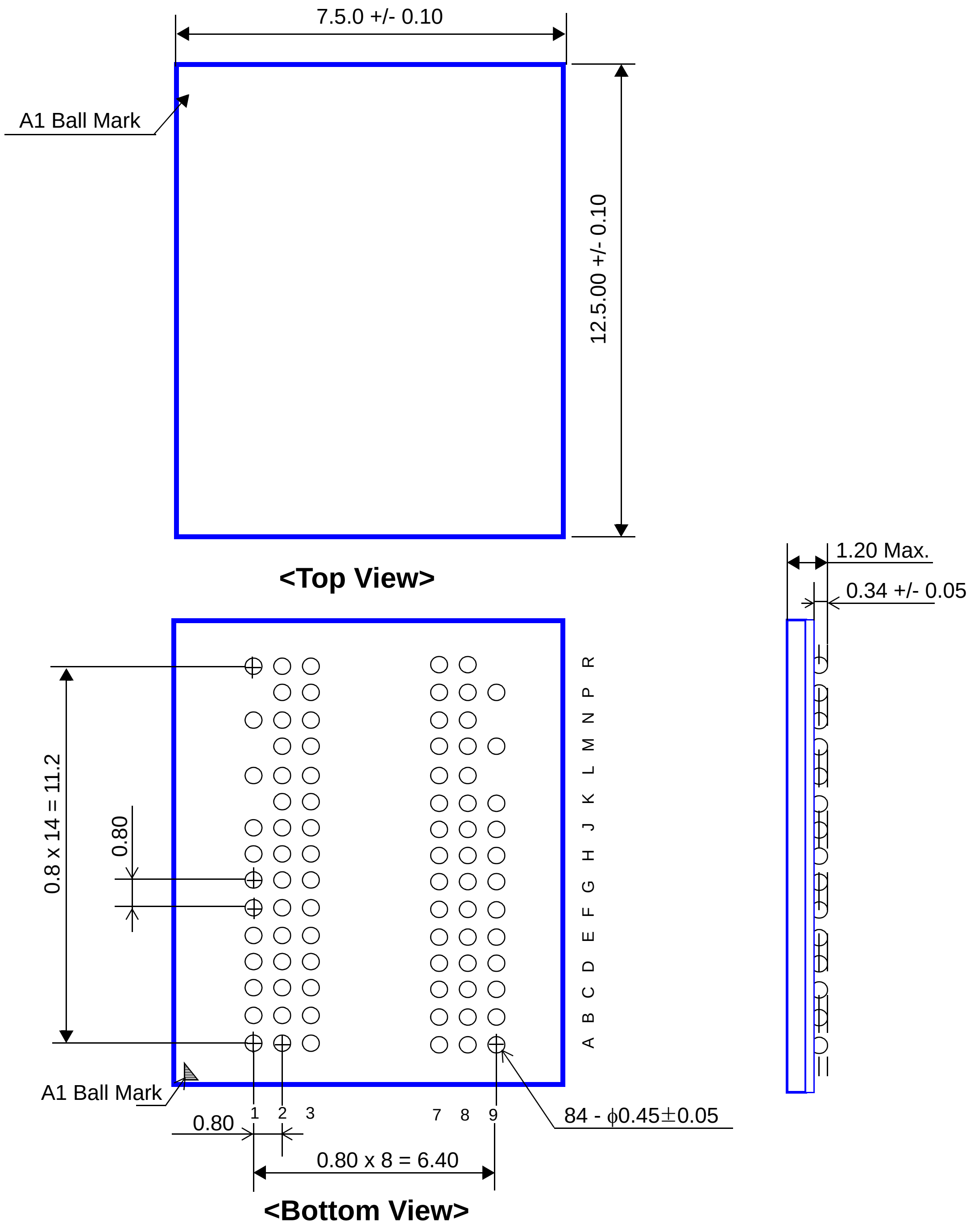
60Ball Fine Pitch Ball Grid Array Outline



note: all dimension units are Millimeters.

Package Dimension(x16)

84Ball Fine Pitch Ball Grid Array Outline



note: all dimension units are Millimeters.