Z86117/717

CMOS Z8® 2K ROM/OTP 8-BIT MICROCONTROLLER

FEATURES

Z8® Core

- 8-Bit CMOS Microcontroller
- 20-Pin SOIC and SSOP Style Packages
- 144 Bytes On-Chip RAM
- 2 Kbytes On-Chip OTP/Masked ROM

On-Chip Features

- Dedicated Ports for Opto-Transistor Output, CMOS Level Schmitt-Triggered Inputs
- High Drive Ports (V_{OL} = 0.8V I_{OL} = 10 mA, 6 Pins Typical) With Internal 100K Pull-Up or Pull-Down Resistors
- Oscillator Filter
- V_{CC} 3.0V-5.5V = OTP (Z86717)
  V_{CC} 2.7V-5.5V = ROM (Z86117)
- External Reset
- Hardwired Watch-Dog Timer
- Fifteen Input/Output Lines
- On-Chip Oscillator (Crystal, Ceramic Resonator, LC, or External Clock Drive)

Performance

- Similar to Z86C08 Product Family
- Speed: Up to 4 MHz Operation
- Low Power Consumption: 33 mW (Typical)
- Two Standby Modes: STOP and HALT
- 250 ns Cycle Time
- ESD Protection Circuitry

GENERAL DESCRIPTION

The Z86117/717 are members of Zilog's Z8® family of microcontrollers with 144 bytes of RAM and 2 Kbytes of OTP/Masked ROM and most closely compares to the Z86C08 MCU devices. The devices are offered in 20-pin SOIC and SSOP style packages and manufactured in CMOS technology. These devices offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion. Two basic address spaces are used to support this configuration: Program Memory and 124 bytes of general-purpose registers.

Enhancements to the Z86117/717 microcontrollers include on-board pull-down and pull-up resistors and high drive ports capable of up to 10 mA current sinking per pin (6 pins max). The addition of a hardwired Watch-Dog Timer (WDT) ensures operational reliability in a variety of application environments. Detailed sinking current specifications are shown in the DC Electrical Characteristics section below.

To unburden the system from coping with real-time tasks, such as counting/timing and I/O data communications, the Z86117/717 offers two on-chip counter/timers with a large number of user selectable modes.

The Z86117/717 features high drive ports (I_{OL} = 10 mA at V_{OL} = 0.8V, 6 pins maximum) providing increased current sinking capabilities. A hardwired Watch-Dog Timer, activating upon release of external reset, STOP mode, and WDT time-out, ensures operational reliability across a broad range of applications. The oscillator filter out high-frequency noise from the oscillator input pin.

GENERAL DESCRIPTION (Continued)

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.; B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

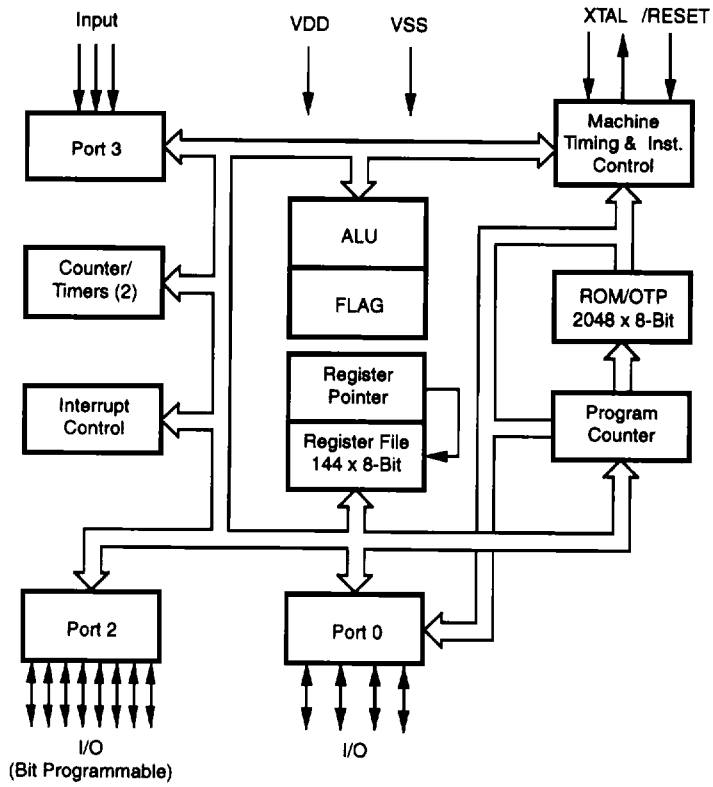

Figure 1. Z86117/717 Functional Block Diagram

PIN DESCRIPTIONS

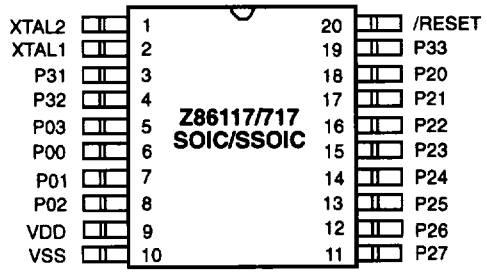

Figure 2. Standard Mode Pin Configuration

Table 1. Standard Mode Pin Identification

Pin #	Symbol	Function	Direction
1	XTAL2	Crystal Oscillator Clock	Output
2	XTAL1	Crystal Oscillator Clock	Input
3	P31	Port 3, Pin 1	Input
4	P32	Port 3, Pin 2	Input
5-8	P00-P02	Port 0, Pins 0,1,2,3	In/Output
9	V_{DD}	Power Supply	Input
10	V_{SS}	Ground	Input
11-14	P24-P27	Port 2, Pins 4,5,6,7	In/Output
15-18	P20-P23	Port 2, Pins 0,1,2,3	In/Output
19	P33	Port 3, Pin 3	Input
20	/RESET	Reset	Input

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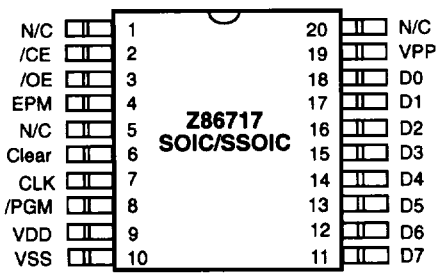

Figure 3. OTP Mode Pin Configuration

Table 2. OTP Mode Pin Identification

Pin #	Symbol	Function	Direction
1	N/C	No Connection	
2	/CE	Chip Enable	Input
3	/OE	Output Enable	Input
4	EPM	EPROM Prog. Mode	Input
5	N/C	No Connection	
6	Clear	Clear Clock	Input
7	Clock	Address	Input
8	/PGM	Pgr Mode	Input
9	V_{DD}	Power Supply	Input
10	V_{SS}	Ground	Input
11-18	D7-D0	Data 0,1,2,3,4,5,6,7	In/Output
19	V_{PP}	Prog. Voltage	Input
20	N/C	No Connection	

PIN DESCRIPTION (Continued)

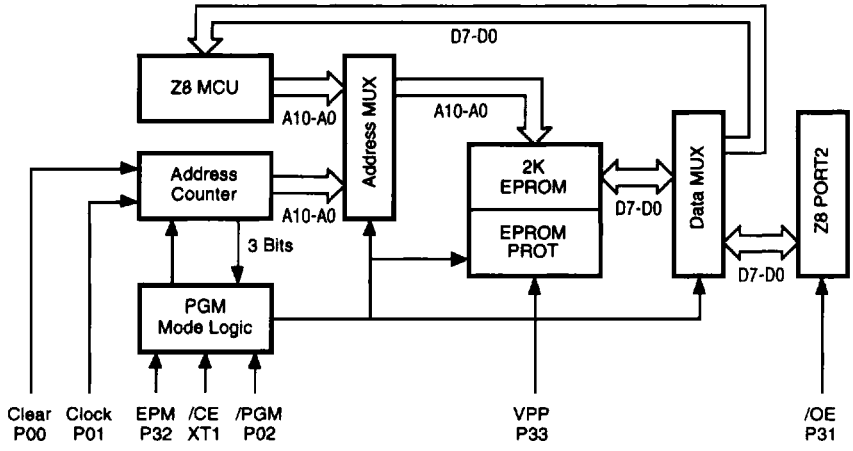

Figure 4. Z86717 OTP Mode Block Diagram

PIN FUNCTIONS

Z86717 OTP Programming Mode

D7-D0 *Data Bus.* The data can be read from, or written to the EPROM through this data bus.

V_{CC} *Power Supply.* It is 5V during the EPROM Read mode and 6V during the other mode.

/CE *Chip Enable (active Low).* This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

/OE *Output Enable (active Low).* This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} *Program Voltage.* This pin supplies the program voltage.

Clear *Clear (active High).* This pin resets the internal address counter at the High level.

Clock *Address Clock.* This pin is a clock input. The internal address counter increases by one clock signal.

/PGM *Program Mode (active Low).* A Low level at this pin programs the data to the EPROM through the Data Bus.

PIN FUNCTIONS

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (4 MHz max) to the on-chip clock oscillator and buffer.

Port 0 (P03-P00). Port 0 is a 4-bit I/O programmable, bi-directional, CMOS compatible I/O port. These four I/O lines can be configured under software control to be input or output (Figure 5). When Port 0 is configured as an input port, all lines have a 100 kOhm (typical) internal pull-down resistor.

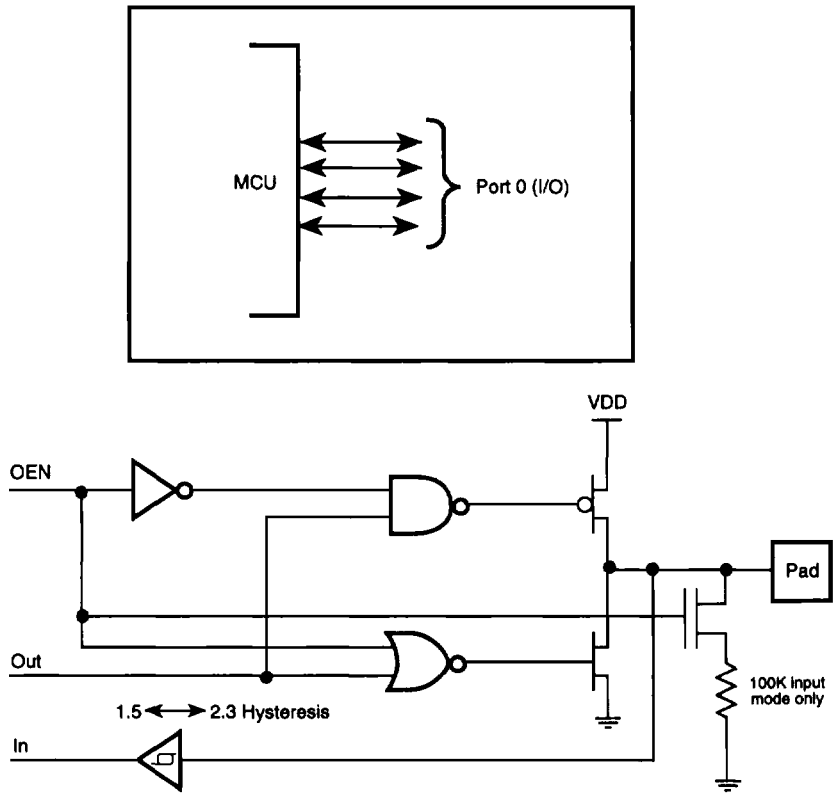

Figure 5. Port 0 Configuration (P03-P00)

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit I/O, bit programmable, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be input or output, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. When P23-P20 are configured as inputs, they have 100 kOhm (typical) pull-down resistors (Figure 6a). P24 has a 100K pull-up resistor in input mode (Figure 6b) while P27-P25 have neither a pull-up or pull-down resistors. These resisters are not applied in any output mode.

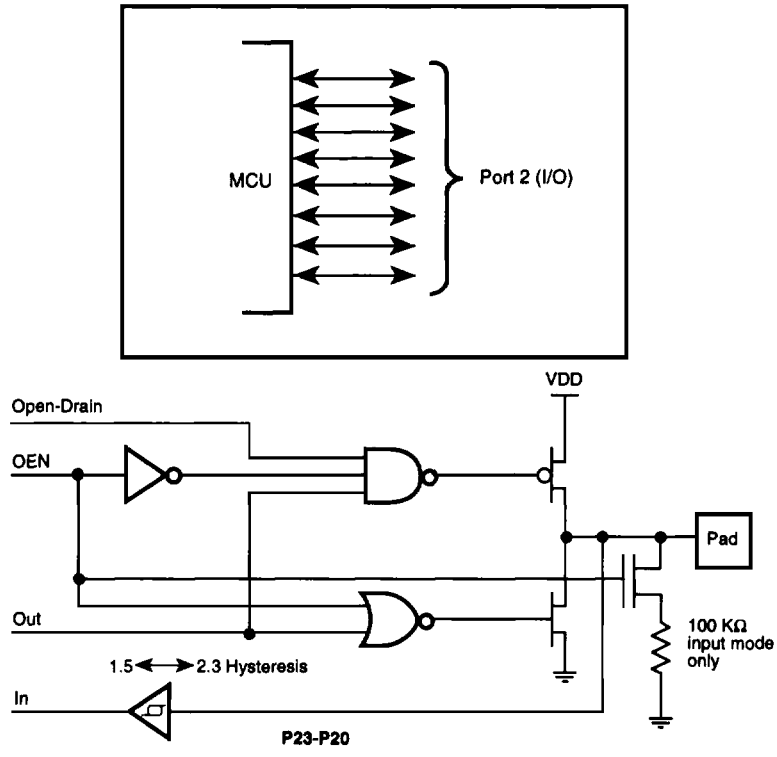

Figure 6a. Port 2, P23-P20 Configuration

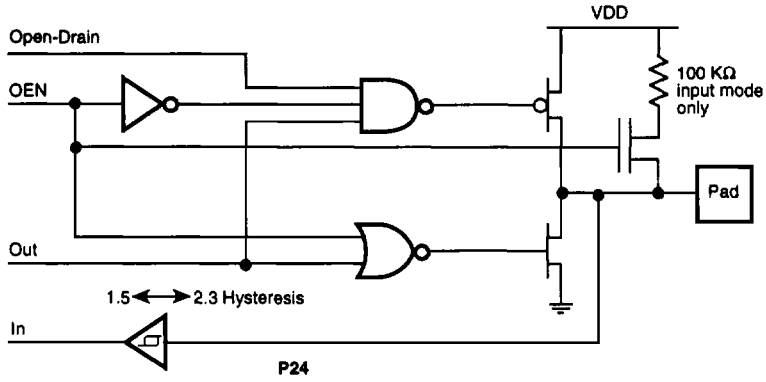

Figure 6b. Port 2, P24 Configuration

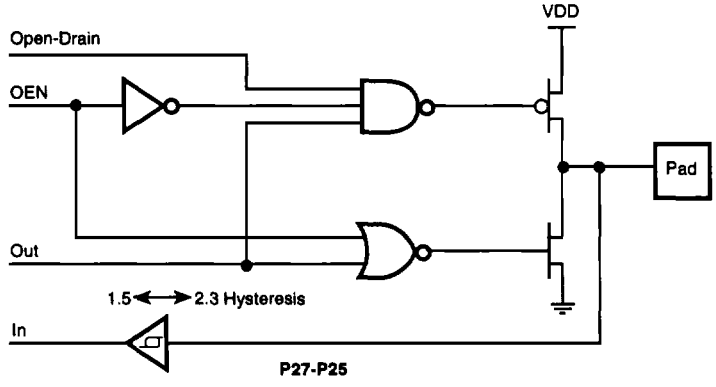

Figure 6c. Port 2, P27-P25 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P33-P31). Port 3 is a 3-bit, CMOS compatible port with three fixed input (P33-P31) lines. These three input lines can also be used as the interrupt sources IRQ3-IRQ0 and as the timer input signal (T_{IN}). P31, P32, and P33 provide ≈100 kOhm (typical) internal pull-down resistor (Figure 7).

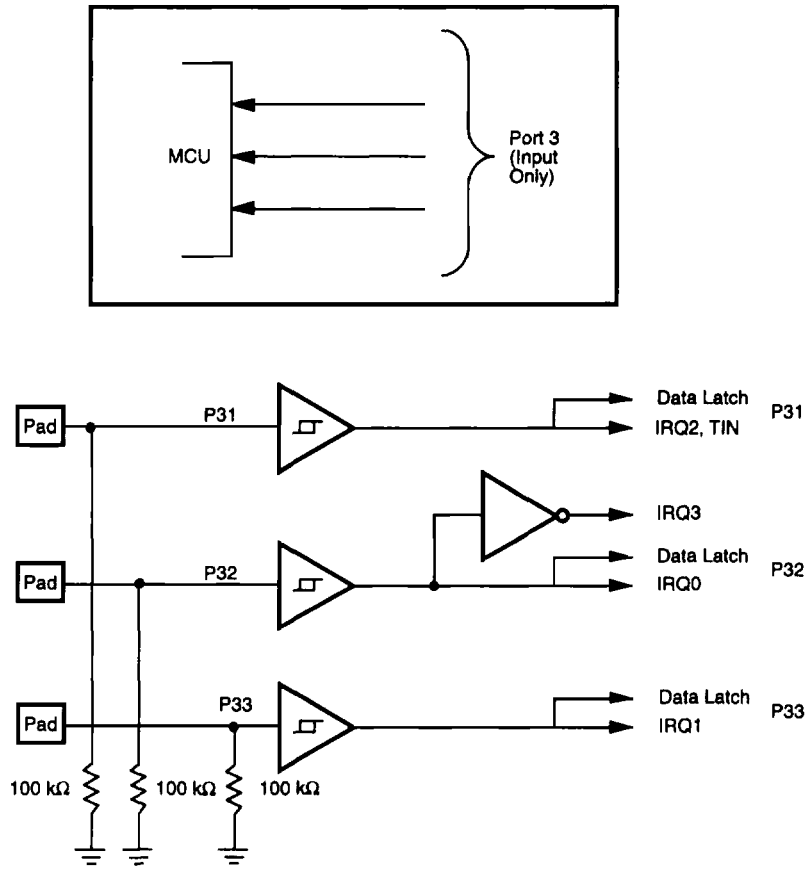

Figure 7. Port 3 Configuration

FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z86117/717 MCUs to enhance the standard Z8 architectural core to provide the user with increased design flexibility.

/RESET (*Input, active Low*). This instruction initializes the MCU. Reset is accomplished by Watch-Dog Timer time-out, Stop-Mode Recovery (SMR), or external reset. During SMR and Watch-Dog Timer time-out, the internally generated reset drives the reset pin Low for 15 ms (typical). Any devices driving the reset line should be open-drain in order to avoid damage in the event of a conflict during reset conditions. There is no condition internal to the MCU that will not allow an external reset to occur.

To avoid asynchronous and noisy reset problems, the MCU is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clock cycles, or for the duration of the external reset, whichever is longer.

Program execution begins at location 000CH, five to ten TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is 5 ms. Reset values are shown in Table.

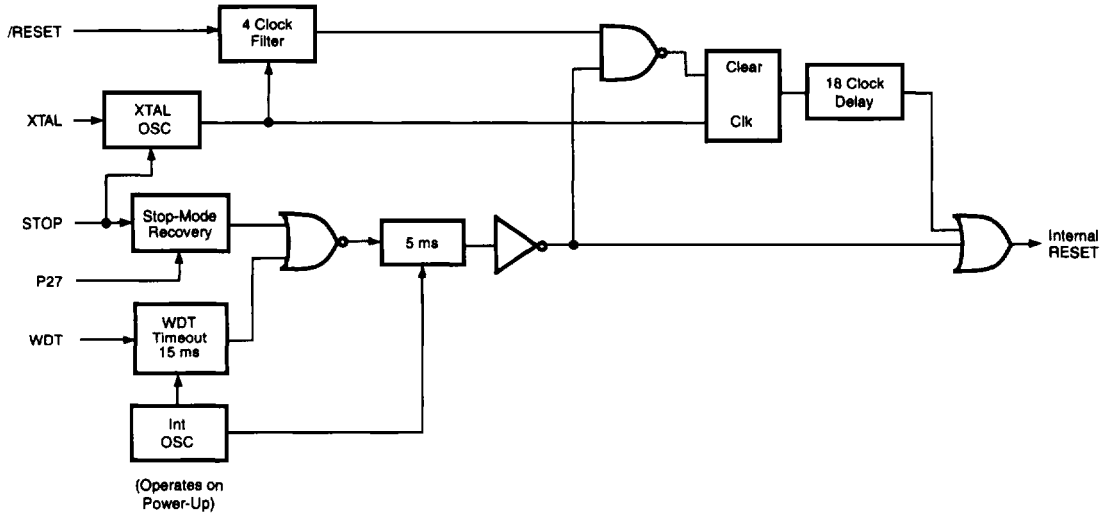

Figure 8. Internal Reset Configuration

FUNCTIONAL DESCRIPTION (Continued)

Table 3. Z86117/717 Control Registers

Addr.	Reg.	Reset Values D7	D6	D5	D4	D3	D2	D1	D0	Comments
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F7*	P3M	U	U	U	U	U	U	1	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
FB	IMR	0	U	U	U	U	U	U	U	
FC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	U	U	U	U	U	U	U	U	
FF	SPL	U	U	U	U	U	U	U	U	

Note:
* A reset after a Low on P27 to exit STOP mode may affect device reliability.

Program Memory. The Z86117/717 can address up to 2 Kbytes of internal program memory (Figure 9). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-2047 are ROM/OTP.

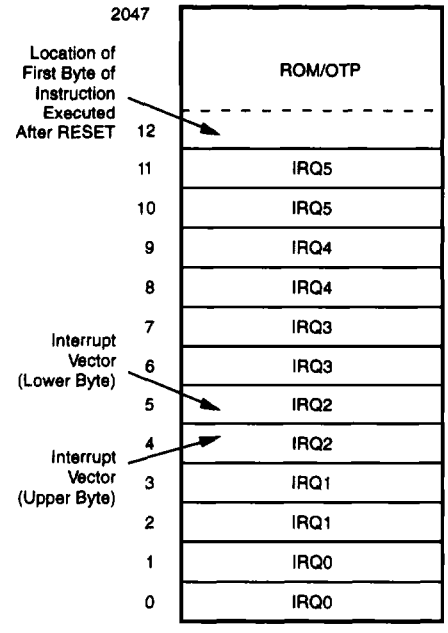

Figure 9. Program Memory Map

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 15 control and status registers: R0-R3, R4-R127 and R241-R255, respectively (Figure 10). The Z86117/717 instructions can access registers directly or indirectly via an 8-bit address field. This allows short, 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 11) addresses the starting location of the active working-register group.

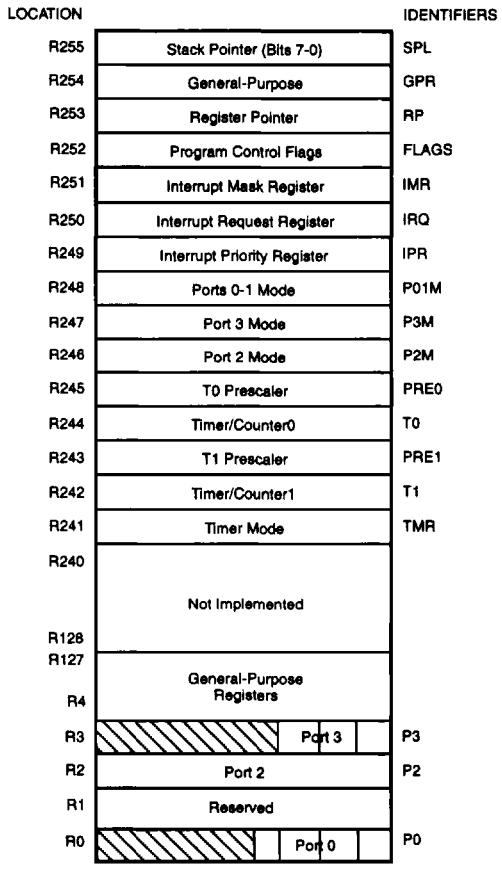

Figure 10. Register File

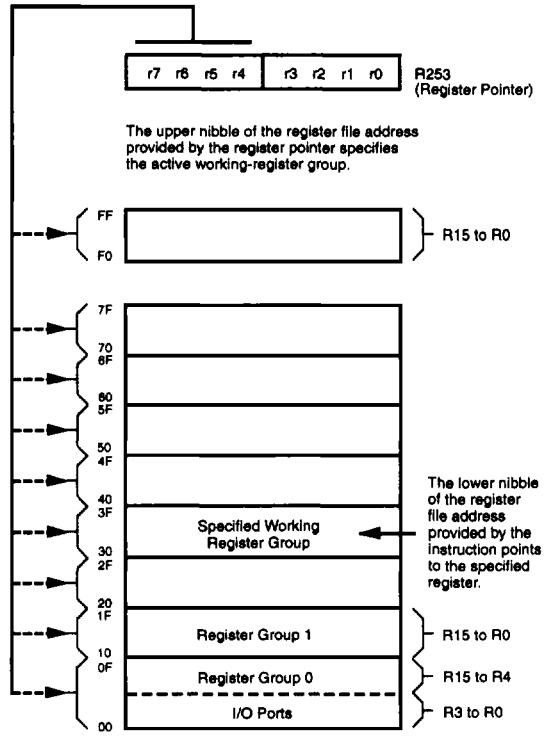

Figure 11. Register Pointer

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FUNCTIONAL DESCRIPTION (Continued)

Stack Pointer. The Z86117/717 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however the T0 can only be driven by the internal clock source (Figure 12).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or not retriggerable, or as a gate input for the internal clock.

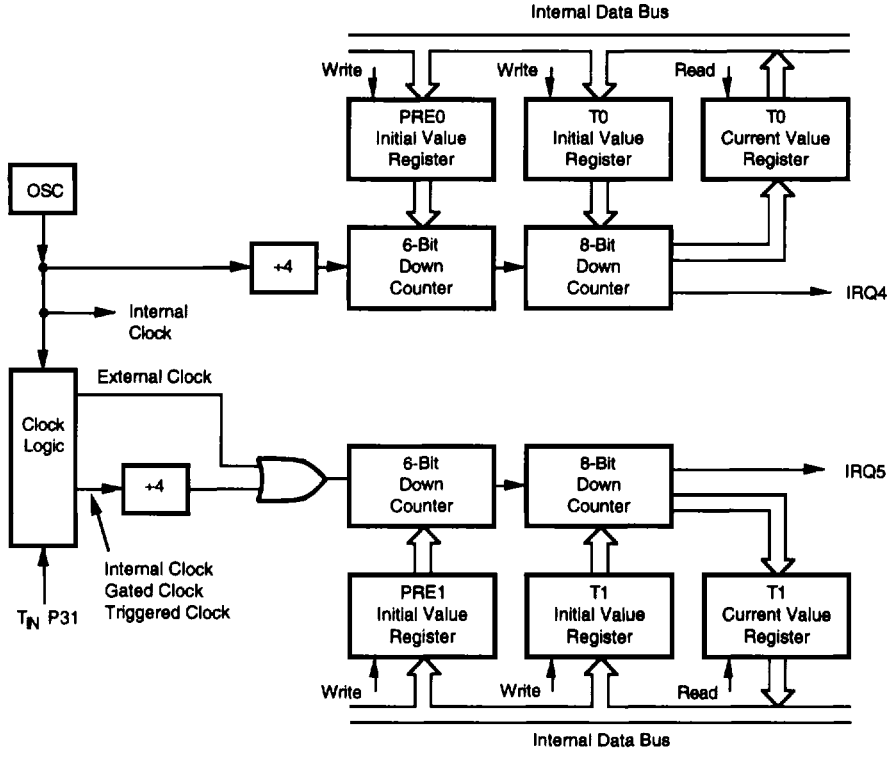


Figure 12. Counter/Timers Block Diagram

Interrupts. The Z86117/717 has six interrupts from five different sources. These interrupts are maskable and prioritized (Figure 13). The five sources are divided as follows: the falling edge of P31, P33, the rising and falling edge of P32, and the two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86117/717 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the Interrupt Service Routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register is polled to determine which of the interrupt requests needs service.

Table 4. Interrupt Types, Sources, and Vectors

Source	Name	Vector	Location	Comments
P32	IRQ0	0,1	External	(F)Edge
P33	IRQ1	2,3	External	(F)Edge
P31	IRQ2	4,5	External	(F)Edge
P32	IRQ3	6,7	External	(R)Edge
T0	IRQ4	8,9	Internal	
T1	IRQ5	10,11	Internal	

Notes:
F = Falling edge triggered
R = Rising edge triggered

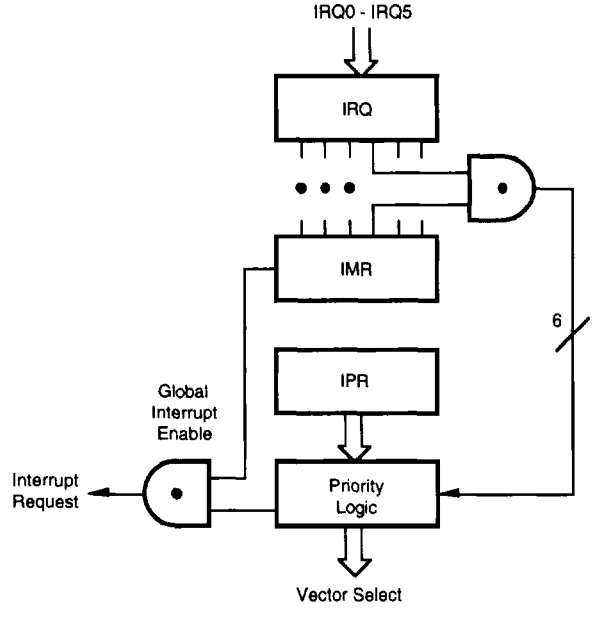


Figure 13. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86117/717 on-chip oscillator has a parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 4 MHz max, with a series resistance (RS) less than or equal to 100 Ohms. There is no divide-by-two circuit for the clock.

The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors from each pin to ground (Figure 14). Capacitance is between 10 pF to 250 pF and is specified by the crystal manufacturer, ceramic resonator and PCB layout.

HALT Mode. Turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The device can be recovered by interrupts, either externally or internally generated, external RESET, or WDT time-out. After the interrupt service routine, the program continues from the instruction after the HALT. With External RESET or WDT time-out, program execution begins at 000CH.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 150 µA (typical). The STOP mode can be released by three methods. The first method is a RESET of the device by removing V_{DD}. The second method is if P27 is configured as an input line when the device executes the STOP instruction. A low input condition on P27 releases the STOP mode. The third method is allowing the WDT to time out.

Program execution under both conditions begins at location 000C (HEX). However, when P27 is used to release the STOP mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as an output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instructions:

```
LD      ; P2M, #80H
NOP     ;
STOP    ;
```

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction. i.e.:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP mode
                or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT mode
```

In STOP or HALT mode, the value of each output line prior to the HALT or STOP instruction is retained during execution.

Watch-Dog Timer (WDT). The Watch-Dog Timer is hardwired in the Z86117/Z86717. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags. The WDT is clocked using the internal RC oscillator. WDT operates upon release of external reset.

Opcode WDT (5FH). Upon release of external reset, the WDT is enabled, and subsequent execution clears the WDT counter. This must be done at least every 10 ms, otherwise, the WDT times out and generates a reset. The generated reset is 5.0 ms, plus 18 XTAL clock cycles.

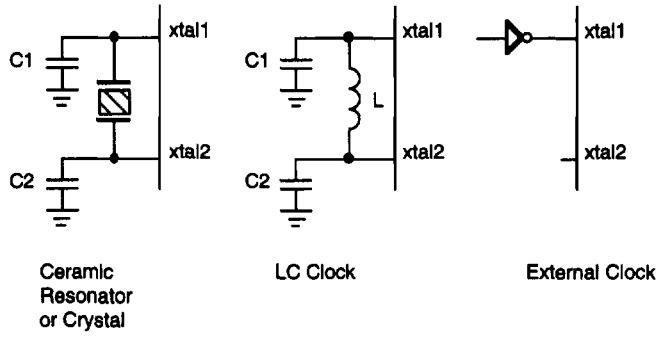


Figure 14. Oscillator Configuration

Internal Pull-Up and Pull-Down Resistances. The Pull-up and Pull-Down Resistance is achieved through a Voltage Dependent Resistance configuration.

ROM/EPROM Protect. ROM/EPROM Protect fully protects the Z86117/717 ROM/EPROM code from being read externally. When ROM/EPROM Protect is selected, the Z86117/717 will disable the instructions LDC and LDCI (Z86717 and Z86117 do not support the instructions of LDE and LDEI).

Note: When using the Z86717 in a noisy environment, it is suggested that the voltages on the EPM and CE pins be clamped to V_{CC} through a diode to V_{CC} to prevent accidentally entering the OTP mode. The V_{PP} requires both a diode and a 100 pF capacitor.

User Modes. The programming voltage of each mode of the Z86717 is shown in Table 5.

Table 5. Z86717 OTP Programming Table

Programming Modes	V_{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V_{CC}*
EPROM READ1	V_{IH}	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V
EPROM READ2	V_{IH}	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V
PROGRAM	V_H	X	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.0V
PROGRAM VERIFY	V_H	X	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
EPROM PROTECT	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.0V

Notes:
V_H = 12.5V ±0.5V
V_{IH} = As per specific Z8 DC specification.
V_{IL} = As per specific Z8 DC specification.
X = Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
* V_{CC} has a tolerance of ±0.25V.

FUNCTIONAL DESCRIPTION (Continued)

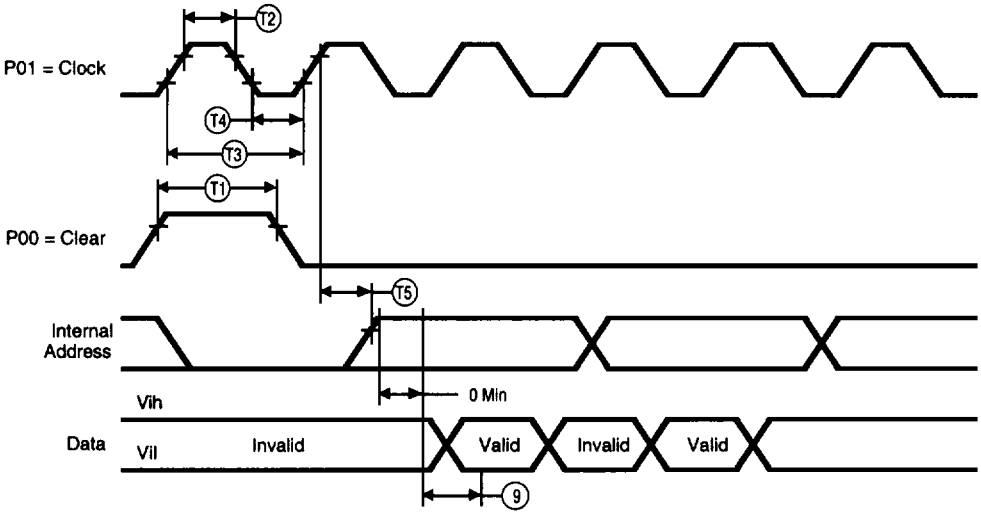
Internal Address Counter. The address of Z86717 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 16 shows the set-up time of the serial address input.

Programming Waveform. Figures 15, 16 and 17 show the programming waveforms of each mode. Table 6 shows the timing of programming waveforms.

Programming Algorithm. Figure 20 shows the flow chart of the Z86717 programming algorithm.

Table 6. Z86717 Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	30 ns Min
T3 Input Clock Period	70 ns Min
T4 Input Clock Low	30 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max

Figure 15. Z86717 Address Counter Waveform

FUNCTIONAL DESCRIPTION (Continued)

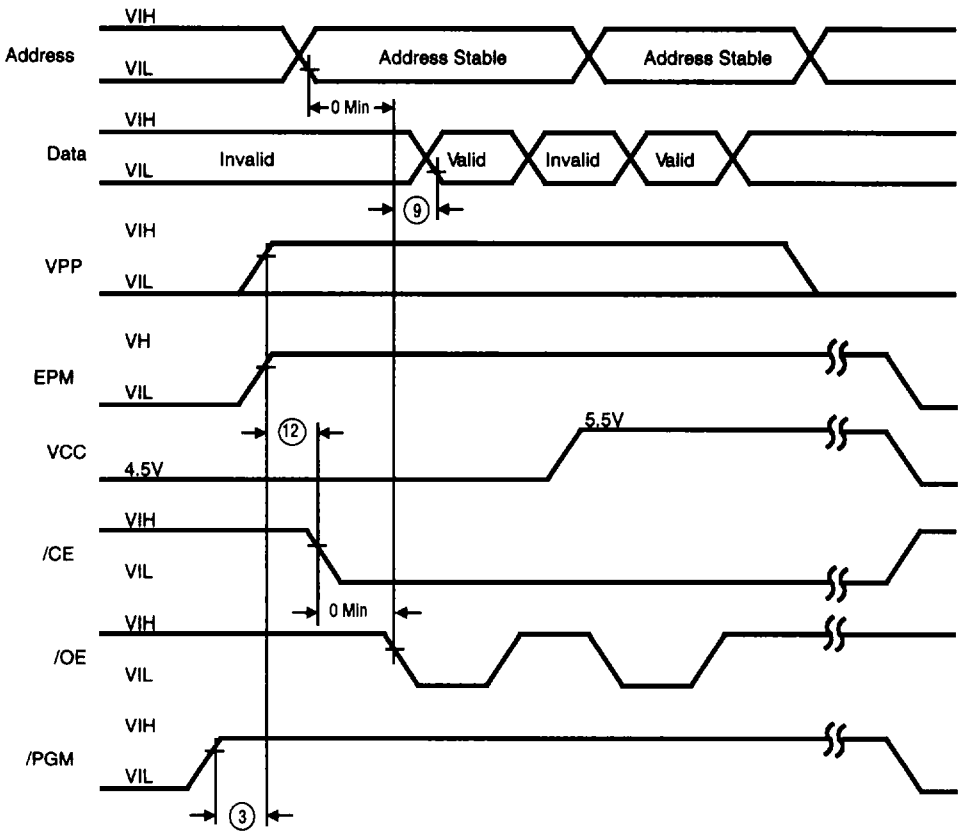


Figure 16. Z86717 Programming Waveform (EPROM Read)

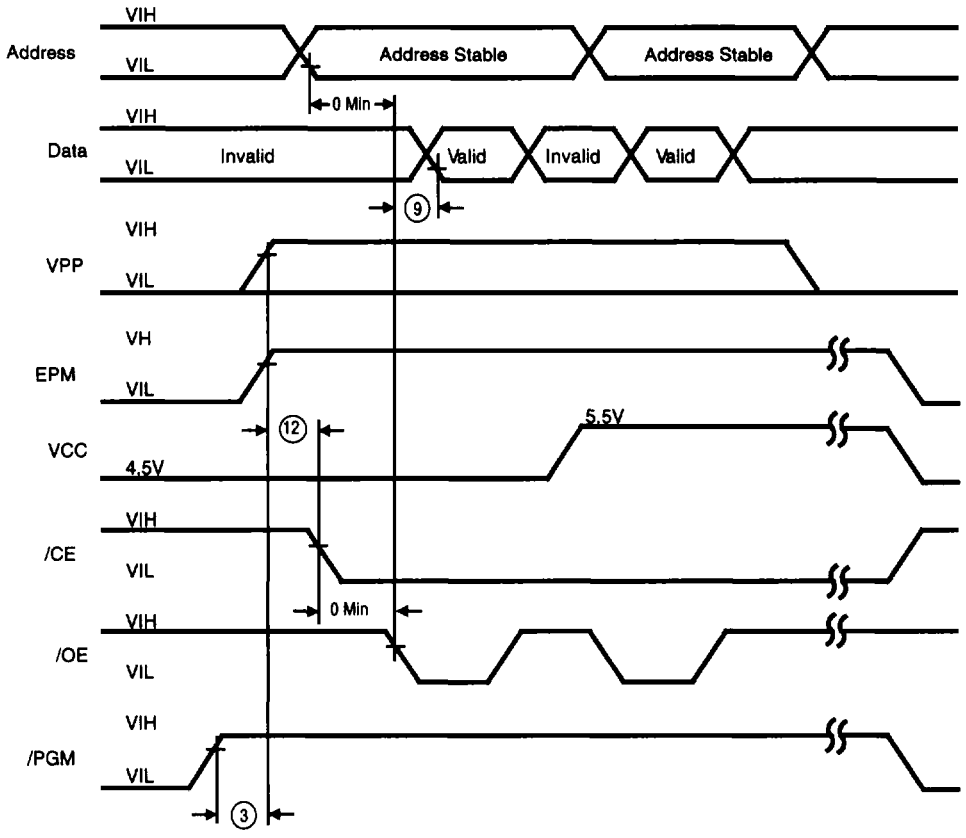


Figure 17. Z86717 Programming Waveform (Program and Verify)

FUNCTIONAL DESCRIPTION (Continued)

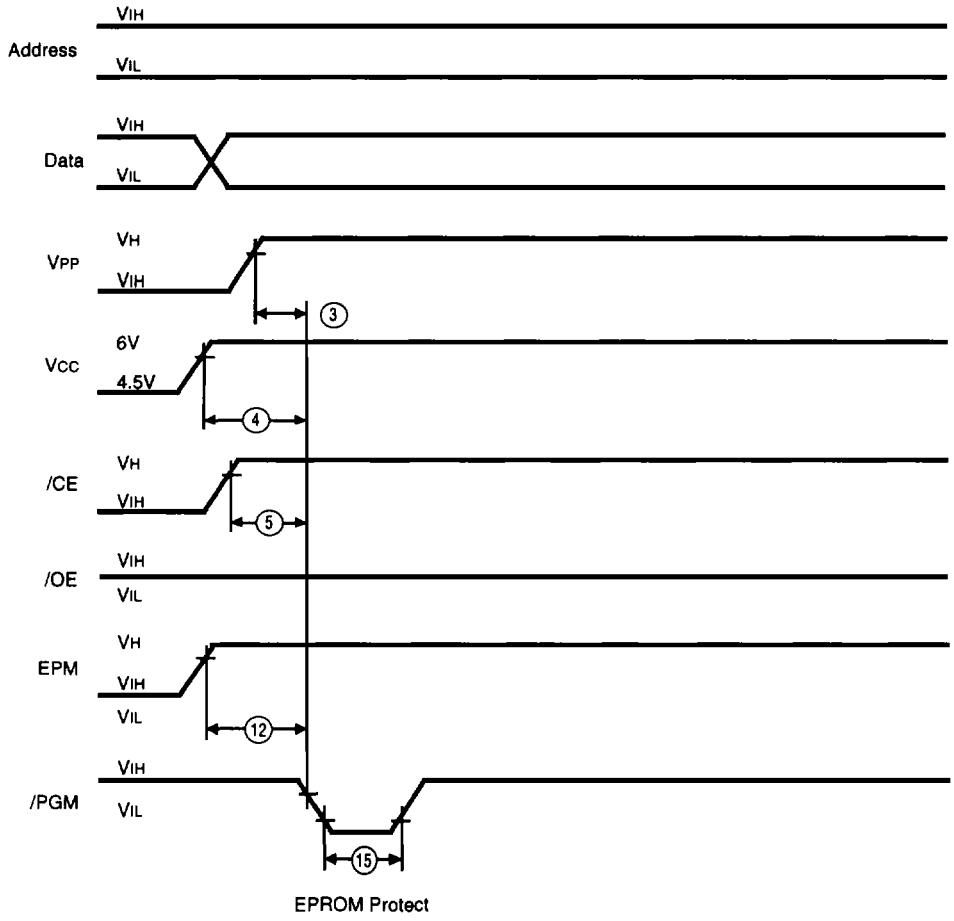


Figure 18. Z86717 Programming Waveform (EPROM Protect)

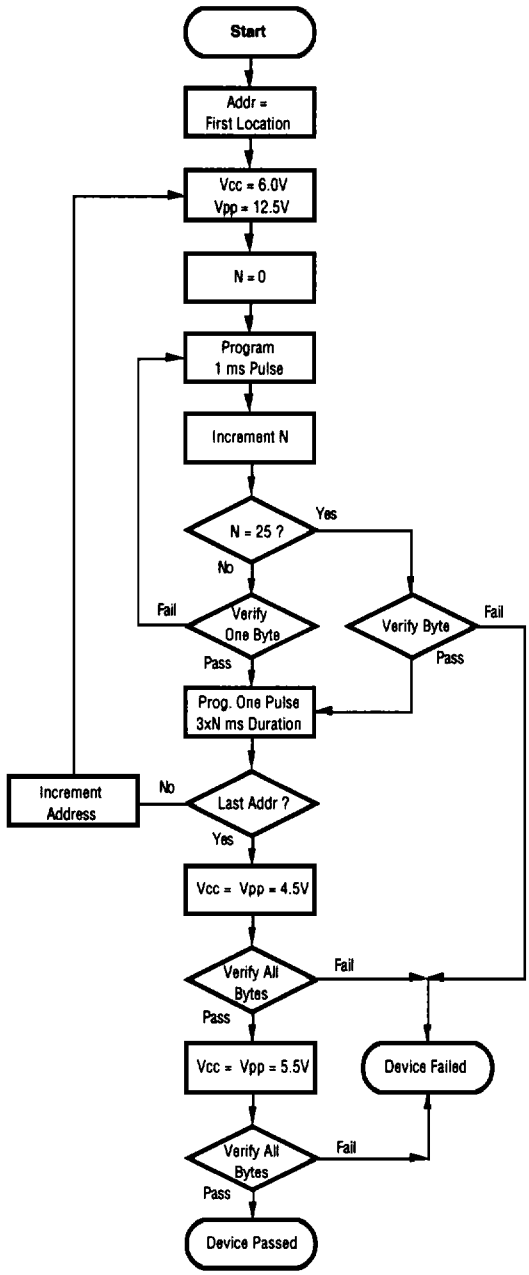


Figure 19. Z86717 Programming Algorithm

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 20).

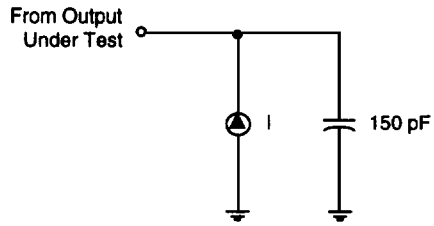


Figure 20. Test Load Diagram

ABSOLUTE MAXIMUM RATINGS

Sym	Parameter	Min	Max	Units
V_{DD}	Supply Voltage*	–0.3	+7	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp	†	†	C

Notes:
* Voltages on all pins with respect to GND
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

T_A = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min.	Max.
Input Capacitance	0	10 pF
Output Capacitance	0	20 pF
I/O Capacitance	0	25 pF

V_{CC} SPECIFICATION

V_{CC} = 3.0V to 5.5V = OTP (Z86717)
V_{CC} = 2.7V to 5.5V = ROM (Z86117)

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{DD}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
	Max Input Voltage	3.0V		12		V	V_{IN} = 250 µA
		5.5V		12		V	V_{IN} = 250 µA
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{DD}	V_{DD} + 0.3	2.0	V	Driven by External Clock Generator
		5.5V	0.7 V_{DD}	V_{DD} + 0.3	3.0	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS} – 0.3	0.2 V_{DD}	0.8	V	Driven by External Clock Generator
		5.5V	V_{SS} – 0.3	0.2 V_{DD}	1.5	V	Driven by External Clock Generator
V_{IH}	Input High Voltage Schmitt-Triggered	3.0V	0.7 V_{DD}	V_{DD} + 0.3	1.6	V	
		5.5V	0.7 V_{DD}	V_{DD} + 0.3	2.6	V	
V_{IL}	Input Low Voltage Schmitt-Triggered	3.0V	V_{SS} – 0.3	0.2 V_{DD}	1.0	V	
		5.5V	V_{SS} – 0.3	0.2 V_{DD}	1.7	V	
V_{RH}	Reset Input High Voltage	3.8V	V_{CC} + 0.3	3.8	V_{CC} + 0.3	V	
V_{RI}	Reset Input Low Voltage	–0.3	0.8	–0.3	0.8	V	
V_{OH}	Output High Voltage	3.0V	V_{DD} – 0.4		2.8	V	I_{OH} = –2.0 mA
		5.5V	V_{DD} – 0.4		5.5	V	I_{OH} = –2.0 mA
V_{OL1}	Output Low Voltage	3.0V		0.5	0.13	V	I_{OL} = +5.0 mA
		5.5V		0.4	0.07	V	I_{OL} = +8.0 mA
V_{OL2}	Output Low Voltage	3.0V		1.5	0.8	V	I_{OL} = 7.0 mA, 6 Pin Max
		5.5V		0.8	0.3	V	I_{OL} = 10.0 mA, 6 Pin Max
I_{IL}	Input Leakage	3.0V	–1.0	1.0	0.4	µA	V_{IN} = 0V, V_{CC}
		5.5V	–1.0	1.0	0.4	µA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	3.0V	–1.0	1.0	0.4	µA	V_{IN} = 0V, V_{CC}
		5.5V	–1.0	1.0	0.4	µA	V_{IN} = 0V, V_{CC}

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DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{DD}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
I_{DD}	Supply Current	3.0V		1.5	0.41	mA	All Output and I/O Pins Floating @ 1 MHz
		5.5V		3.0	1.44	mA	All Output and I/O Pins Floating @ 1 MHz
		3.0V		2.0	0.93	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		4.0	2.60	mA	All Output and I/O Pins Floating @ 2 MHz
		3.0V		3.0	1.64	mA	All Output and I/O Pins Floating @ 4 MHz
		5.5V		6.0	4.28	mA	All Output and I/O Pins Floating @ 4 MHz
I_{DD1}	Standby Current	3.0V		0.6	0.15	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz
		5.5V		1.3	0.70	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz
		3.0V		0.8	0.20	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		1.5	0.80	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		3.0V		1.0	0.3	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
		5.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz
I_{DD2}	Standby Current	3.0V		200	150	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running
		5.5V		200	150	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running
I_{PU}	Pull-Up Current (100K) Port P24	3.0V		-35	-13	µA	
		5.5V		-100	-57	µA	
I_{PD}	Pull-Down Current (100K)	3.0V		40	20	µA	
		5.5V		125	80	µA	

AC ELECTRICAL CHARACTERISTICS
Timing Diagrams

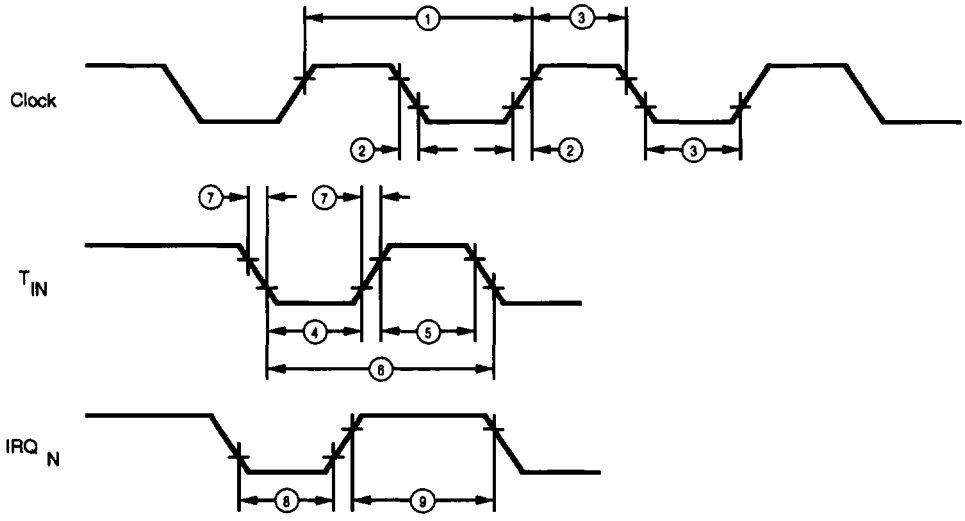

Figure 21. Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

				T_A = 0°C to +70°C					
				1 MHz		4 MHz			
No	Symbol	Parameter	V_{DD}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	1,000	100,000	250	100,000	ns	[1]
			5.5V	1,000	100,000	250	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25	ns	[1]
			5.5V		25		25	ns	
3	TwC	Input Clock Width	3.0V		475		100	ns	[1]
			5.5V		475		100	ns	[1]
4	TwTinL	Timer Input Low Width	3.0V		100		100	ns	[1]
			5.5V		70		70	ns	[1]
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			[1]
			5.5V	4TpC		4TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	3.0V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.0V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer Time Out Timer	3.0V	25		25		ms	[1]
			5.5V	10		10		ms	[1]

Notes:
[1] Timing Reference uses 0.7 V_{DD} for a logic 1 and 0.2 V_{DD} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31)

Z8® CONTROL REGISTER DIAGRAMS

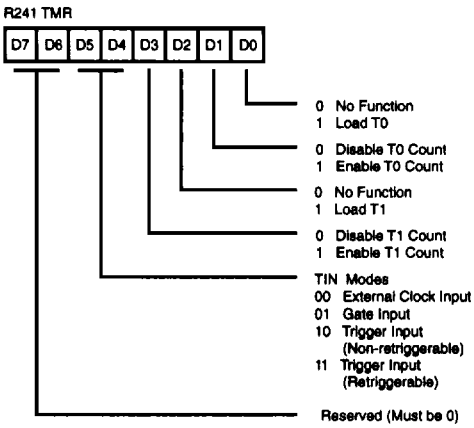

Figure 22. Timer Mode Register ($F1_H$: Read/Write)

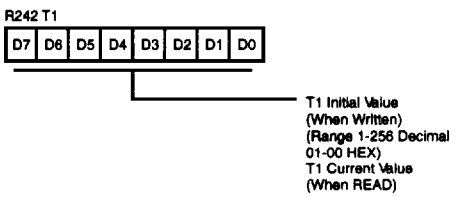

Figure 23. Counter Timer 1 Register ($F2_H$: Read/Write)

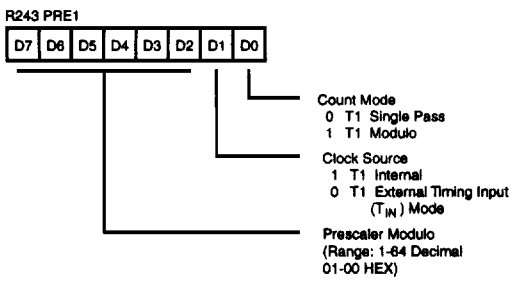

Figure 24. Prescaler 1 Register ($F3_H$: Write Only)

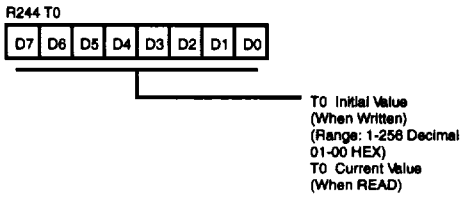

Figure 25. Counter/Timer 0 Register ($F4_H$: Read/Write)

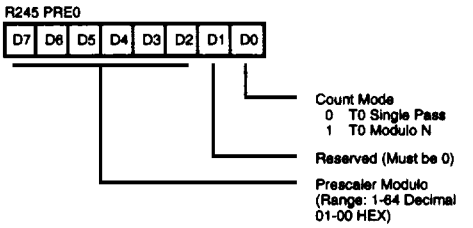

Figure 26. Prescaler 0 Register ($F5_H$: Write Only)

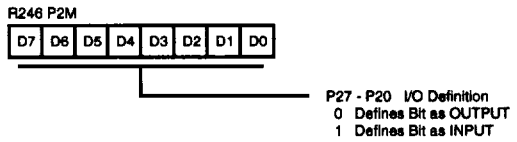

Figure 27. Port 2 Mode Register ($F6_H$: Write Only)

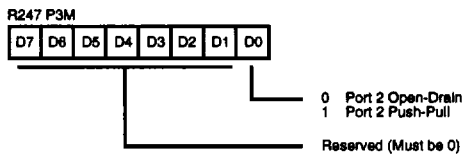

Figure 28. Port 3 Mode Register ($F7_H$: Write Only)

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Z8® CONTROL REGISTER DIAGRAMS (Continued)

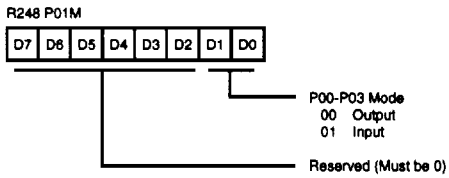

Figure 29. Port 0 and 1 Mode Register ($F8_H$: Write Only)

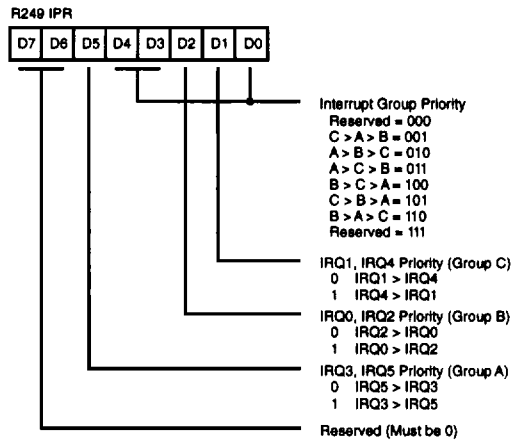

Figure 30. Interrupt Priority Register ($F9_H$: Write Only)

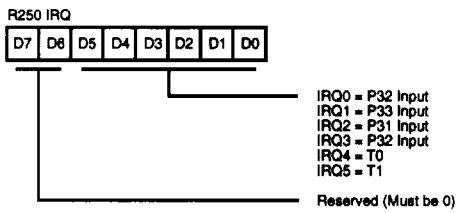

Figure 31. Interrupt Request Register (FA_H: Read/Write)

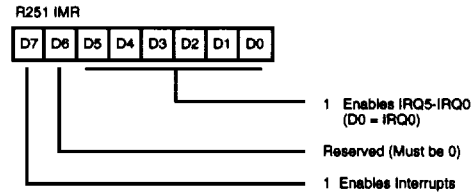

Figure 32. Interrupt Mask Register (FB_H: Read/Write)

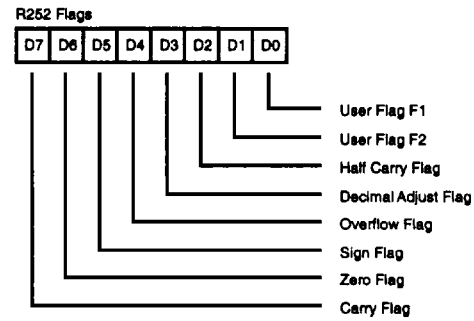

Figure 33. Flag Register (FC_H: Read/Write)

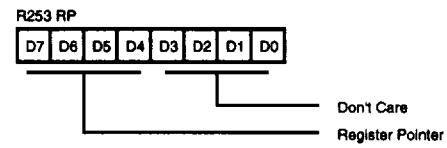

Figure 34. Register Pointer (FD_H: Read/Write)

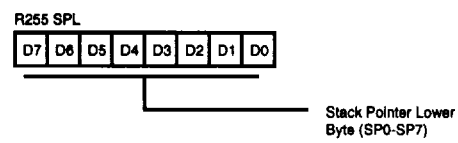

Figure 35. Stack Pointer (FF_H: Read/Write)

DEVICE CHARACTERISTICS

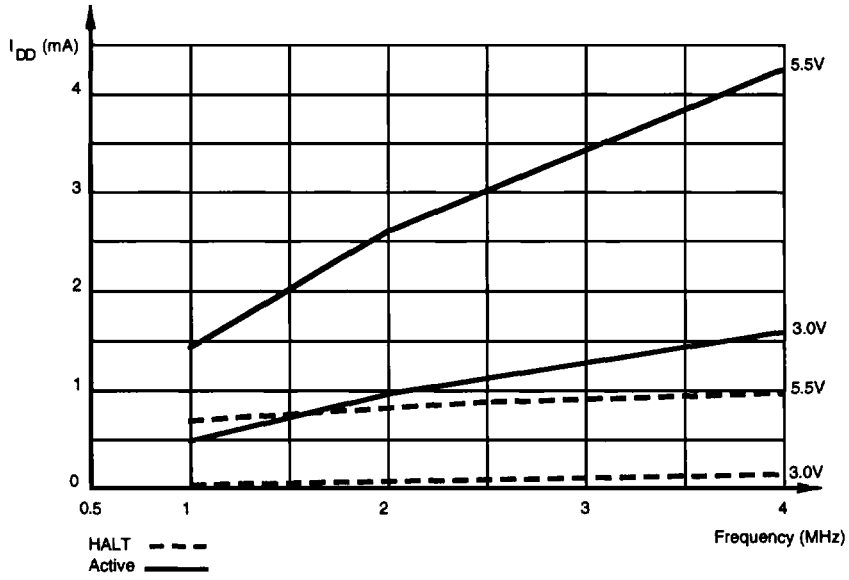

Figure 36. Typical I_{DD} vs Frequency

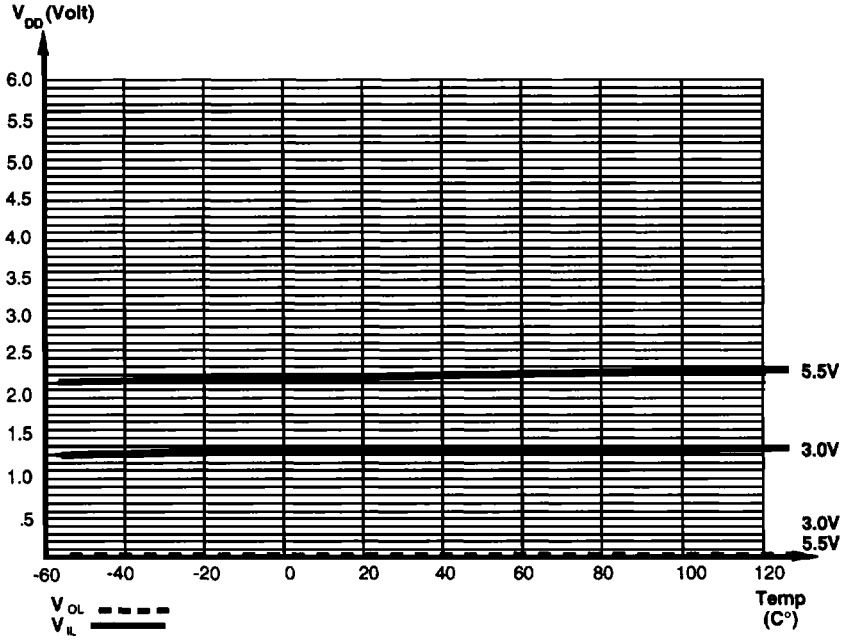

Figure 37. V_{IL}, V_{OL} vs Temperature

DEVICE CHARACTERISTICS (Continued)

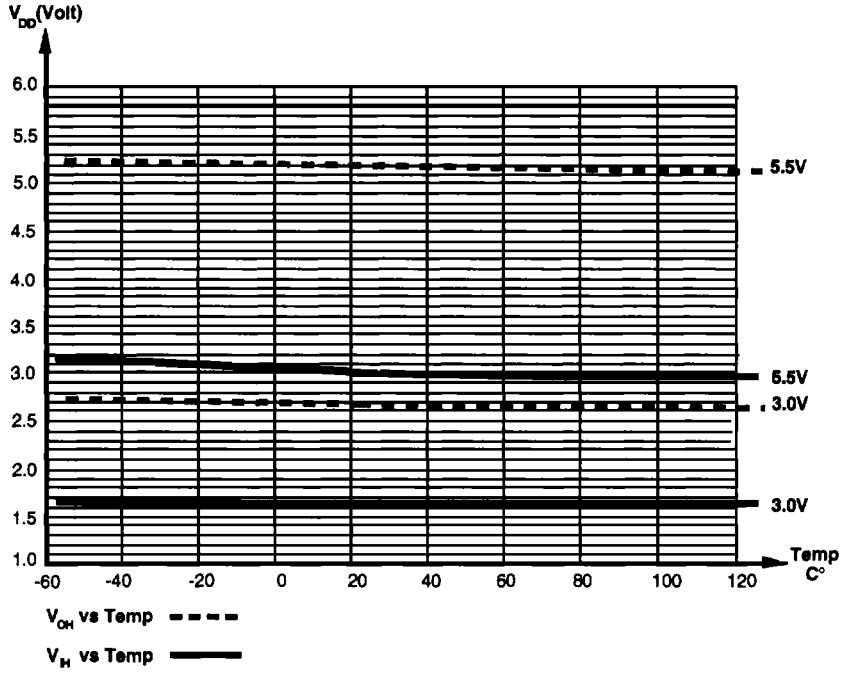

Figure 38. V_{IH}, V_{OH} vs Temperature

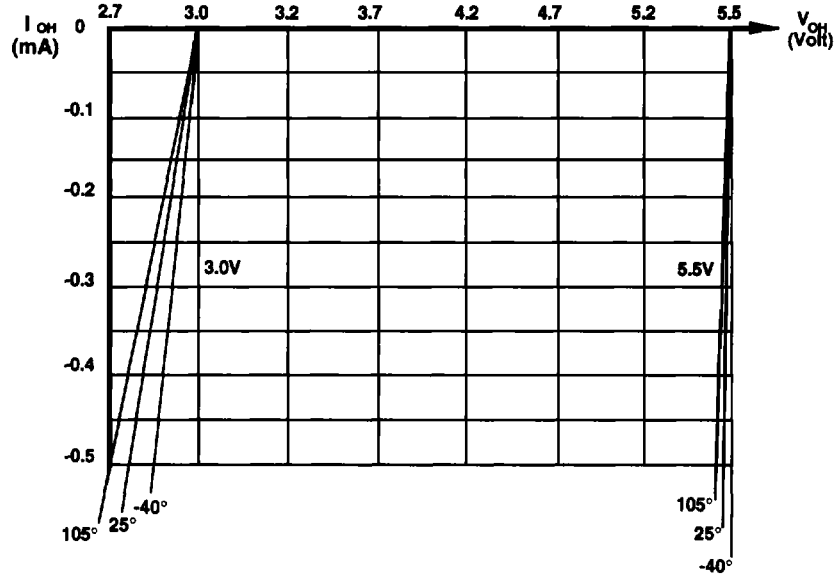

Figure 39. Typical I_{OH} vs V_{OH}

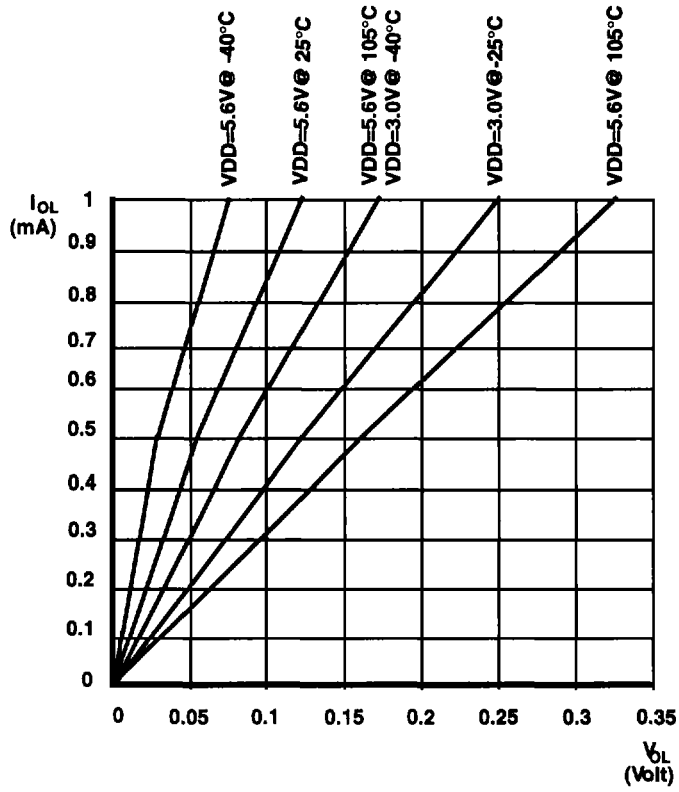

Figure 40. Typical I_{OL} vs V_{OL}

DEVICE CHARACTERISTICS (Continued)

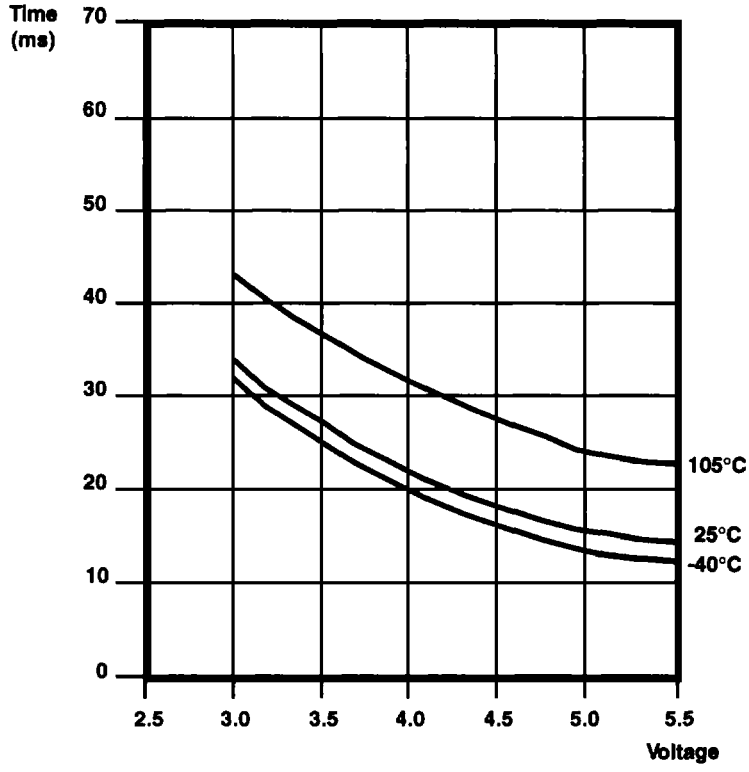

Figure 41. Typical WDT Time-Out Period vs V_{DD} Over Temperature

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

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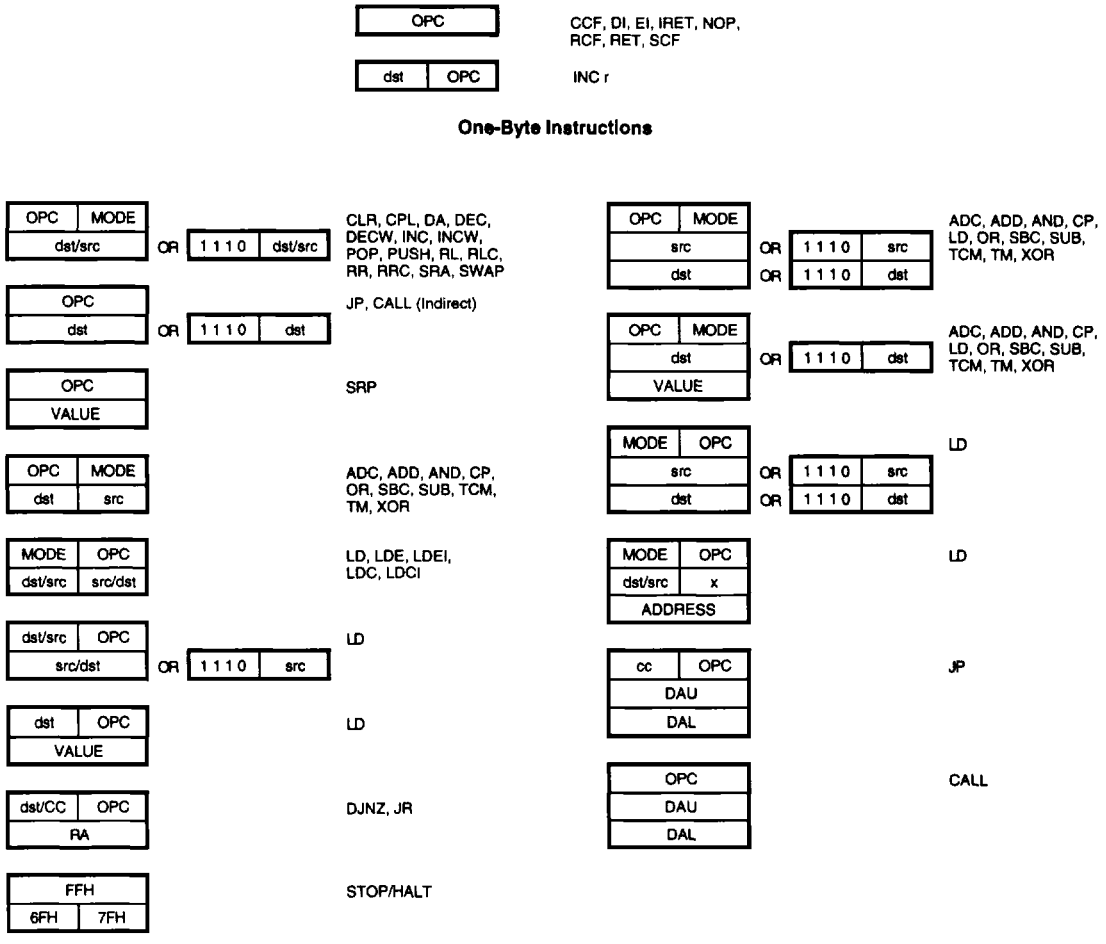
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	—	Always true	—
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1
0000	F	Never true (always false)	—

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "---". For example:

dst --- dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst(7)

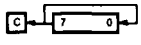
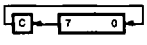
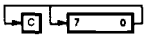
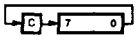
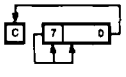
refers to bit 7 of the destination operand.

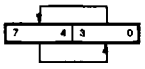
INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst ← dst + src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst ← dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst ← dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP ← SP – 2 @SP ← PC, PC ← dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C ← NOT C			EF	*	-	-	-	-	-
CLR dst dst ← 0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst ← NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst ← DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst ← dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst ← dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7) ← 0			8F	-	-	-	-	-	-
DJNZr, dst r ← r – 1 if r ≠ 0 PC ← PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7) ← 1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst ← dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-
INCW dst dst ← dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) ← 1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC ← dst	DA IRR		CD C = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC ← PC + dst Range: +127, –128	RA		CB C = 0 – F	-	-	-	-	-	-
LD dst, src dst ← src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst ← src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst ← src r ← r + 1;rr ← rr + 1	Ir	Irr	C3	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
OR dst, src dst ← dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst ← @SP; SP ← SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP ← SP – 1; @SP ← src	R IR		70 71	-	-	-	-	-	-
RCF C ← 0			CF	0	-	-	-	-	-
RET PC ← @SP; SP ← SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst ← dst ← src – C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP dst RP ← src	Im		31	-	-	-	-	-	-
STOP			6F	1	-	-	-	-	-
SUB dst, src dst ← dst – src	†		2[ ]	*	*	*	*	1	*

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst ← dst XOR src	†		B[ ]	-	*	*	0	-	-
WDT			5F	-	X	X	X	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

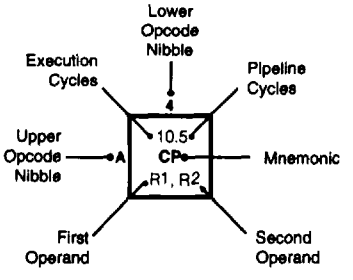
Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

13

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2					3	1	



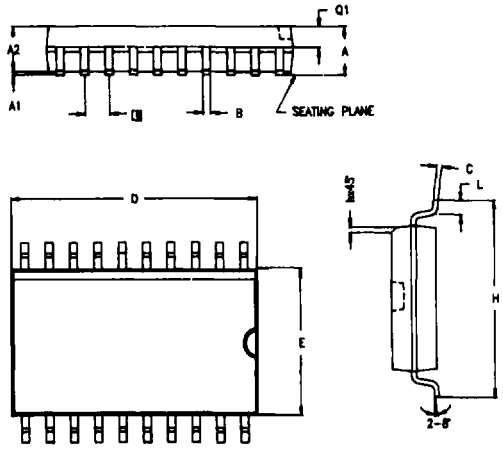
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

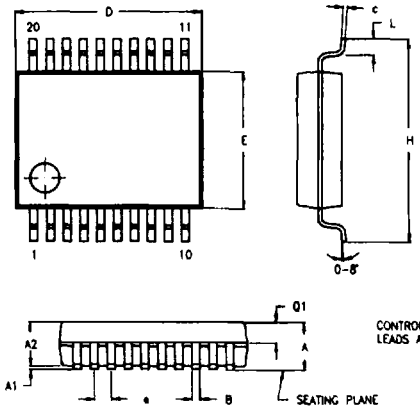
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.008	.012
D	12.80	12.95	.496	.510
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.80	1.00	.024	.038
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

20-Pin SOIC Package Diagram



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

20-Pin SSOP Package Diagram

ORDERING INFORMATION

Z86117/717

4 MHz	
20-Pin SOIC	**20-Pin SSOP**
Z8611704SSC	Z8611704HSC
Z8671704SSC	Z8671704HSC

For fast results, contact your local Zilog sales offices for assistance in ordering the part desired.

CODES

Package
H = Small Outline SSOP
S = SOIC

Temperature
S = 0°C to +70°C

Speed
04 = 4 MHz

Environmental
C = Plastic Standard

Example:

Z 86117 04 S S C is an 86117, 4 MHz, SOIC, 0°C to +70°C, Plastic Standard Flow