



# 128Kx32 SRAM MODULE, SMD 5962-93187 & 5962-95595

## FEATURES

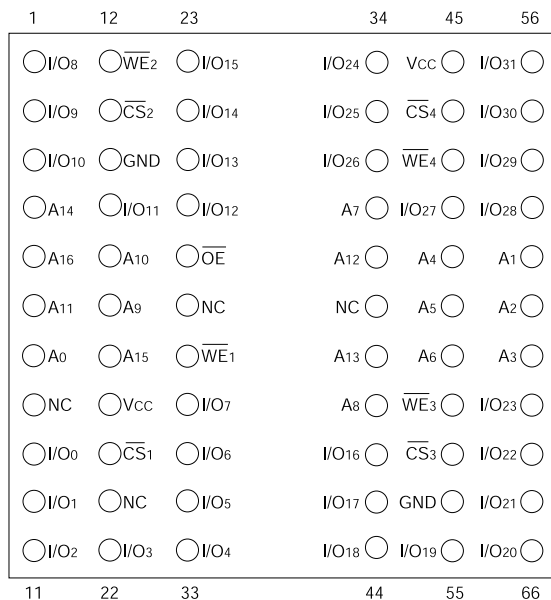
- Access Times of 15, 17, 20, 25, 35, 45, 55ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400)
  - 68 lead, 40mm CQFP (G4T)<sup>1</sup>, 3.56mm (0.140") (Package 502)
  - 68 lead, 22.4mm CQFP (G2U), 3.56mm (0.140"), (Package 510)
  - 68 lead, 22.4mm (0.880") square, CQFP (G2L), 5.08mm (0.200") high, (Package 528).
  - 68 lead, 23.9mm Low Profile CQFP (G1U)<sup>1</sup>, 3.57mm (0.140"), (Package 519)
  - 68 lead, 23.9mm Low Profile CQFP (G1T), 4.06mm (0.160"), (Package 524)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8

- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight:
  - WS128K32-XG1UX<sup>1</sup> - 5 grams typical
  - WS128K32-XG1TX - 5 grams typical
  - WS128K32-XG2UX - 8 grams typical
  - WS128K32-XG2LX - 8 grams typical
  - WS128K32-XH1X - 13 grams typical
  - WS128K32-XG4TX<sup>1</sup> - 20 grams typical
- All devices are upgradeable to 512Kx32

*Note 1: Package Not Recommended For New Design*

**FIG. 1 PIN CONFIGURATION FOR WS128K32N-XH1X**

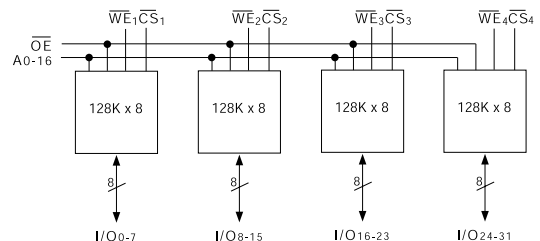
### TOP VIEW



### PIN DESCRIPTION

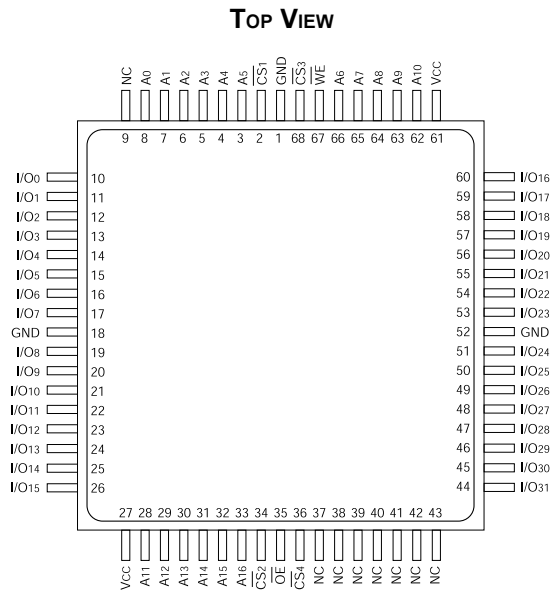
I/O <sub>0-31</sub>	Data Inputs/Outputs
A <sub>0-16</sub>	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V <sub>CC</sub>	Power Supply
GND	Ground
NC	Not Connected

### BLOCK DIAGRAM





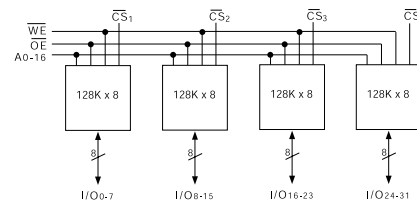
**FIG. 2 PIN CONFIGURATION FOR WS128K32-XG4TX<sup>1</sup>**



**PIN DESCRIPTION**

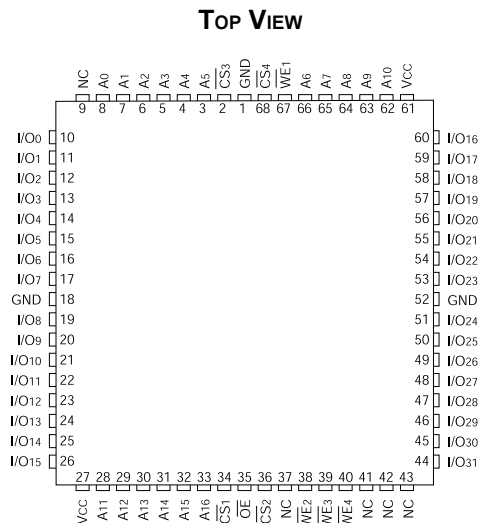
I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

**BLOCK DIAGRAM**



*Note 1: Package Not Recommended For New Design*

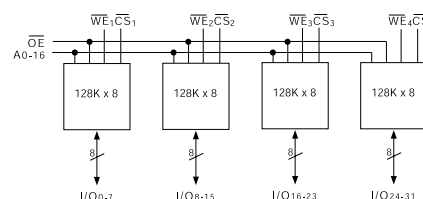
**FIG. 3 PIN CONFIGURATION FOR WS128K32-XG2UX, WS128K32-XG2LX, WS128K32-XG1TX AND WS128K32-XG1UX<sup>1</sup>**



**PIN DESCRIPTION**

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

**BLOCK DIAGRAM**



*Note 1: Package Not Recommended For New Design*



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	V <sub>CC</sub> +0.5	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V
Operating Temp. (Mil.)	T <sub>A</sub>	-55	+125	°C

**TRUTH TABLE**

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

**CAPACITANCE  
(TA = +25°C)**

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	50	pF
$\overline{WE}$ 1-4 capacitance HIP (PGA) H1 CQFP G4T CQFP G2U/G2L CQFP G1U/G1T	C <sub>WE</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	20 50 20 20	pF
$\overline{CS}$ 1-4 capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	20	pF
Data I/O capacitance	C <sub>I/O</sub>	V <sub>IO</sub> = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	50	pF

*This parameter is guaranteed by design but not tested.*

**DC CHARACTERISTICS  
(VCC = 5.0V, GND = 0V, TA = -55°C TO +125°C)**

Parameter	Sym	Conditions	-15		-17		-20		-25		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I <sub>II</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10		10		10		10	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, V_{OUT} = GND \text{ to } V_{CC}$		10		10		10		10	μA
Operating Supply Current	I <sub>CC</sub>	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$		600		600		600		600	mA
Standby Current	I <sub>SB</sub>	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$		80		80		80		60	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5	2.4		2.4		2.4		2.4		V

Parameter	Sym	Conditions	-35		-45		-55		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I <sub>II</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10		10		10	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, V_{OUT} = GND \text{ to } V_{CC}$		10		10		10	μA
Operating Supply Current	I <sub>CC</sub>	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$		600		600		600	mA
Standby Current	I <sub>SB</sub>	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$		60		60		60	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA, V <sub>CC</sub> = 4.5		0.4		0.4		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA, V <sub>CC</sub> = 4.5	2.4		2.4		2.4		V

**NOTE:** DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

**DATA RETENTION CHARACTERISTICS (FOR WS128K32L-XXX ONLY)  
(TA = -55°C TO +125°C), (TA = -40°C TO +85°C)**

Characteristic	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V <sub>CC</sub>	V <sub>CC</sub> = 2.0V	2	-	-	V
Data Retention Quiescent Current	I <sub>CCDR</sub>	CS ≥ V <sub>CC</sub> - 0.2V	-	1	2	mA
Chip Disable to Data Retention Time (1)	T <sub>CDR</sub>	V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V	0	-	-	ns
Operation Recovery Time (1)	T <sub>R</sub>	or V <sub>IN</sub> - 0.2V	T <sub>RC</sub>	-	-	ns

**NOTE:** Parameter guaranteed, but not tested.



**AC CHARACTERISTICS**  
(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C TO +125°C)

Parameter	Symbol	-15		-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	15		17		20		25		35		45		55		ns
Address Access Time	t <sub>AA</sub>		15		17		20		25		35		45		55	ns
Output Hold from Address Change	t <sub>OH</sub>	0		0		0		0		0		0		0		ns
Chip Select Access Time	t <sub>ACS</sub>		15		17		20		25		35		45		55	ns
Output Enable to Output Valid	t <sub>OE</sub>		10		10		12		15		20		25		30	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	3		3		3		3		3		3		3		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	0		0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		12		12		12		12		20		20		20	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		12		12		12		12		20		20		20	ns

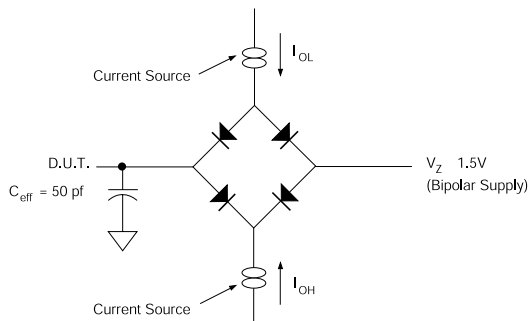
1. This parameter is guaranteed by design but not tested.

**AC CHARACTERISTICS**  
(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C TO +125°C)

Parameter	Symbol	-15		-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	15		17		20		25		35		45		55		ns
Chip Select to End of Write	t <sub>CW</sub>	14		14		15		20		25		30		45		ns
Address Valid to End of Write	t <sub>AW</sub>	14		15		15		20		25		30		45		ns
Data Valid to End of Write	t <sub>DW</sub>	10		10		12		15		20		25		25		ns
Write Pulse Width	t <sub>WP</sub>	14		14		15		20		25		30		45		ns
Address Setup Time	t <sub>AS</sub>	0		0		0		0		0		0		0		ns
Address Hold Time	t <sub>AH</sub>	0		0		0		0		0		0		0		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	3		3		3		3		4		4		4		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		10		10		12		15		20		25		25	ns
Data Hold Time	t <sub>DH</sub>	0		0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

**FIG. 4 AC TEST CIRCUIT**



**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

**Notes:**  
V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75 Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



FIG. 5 TIMING WAVEFORM - READ CYCLE

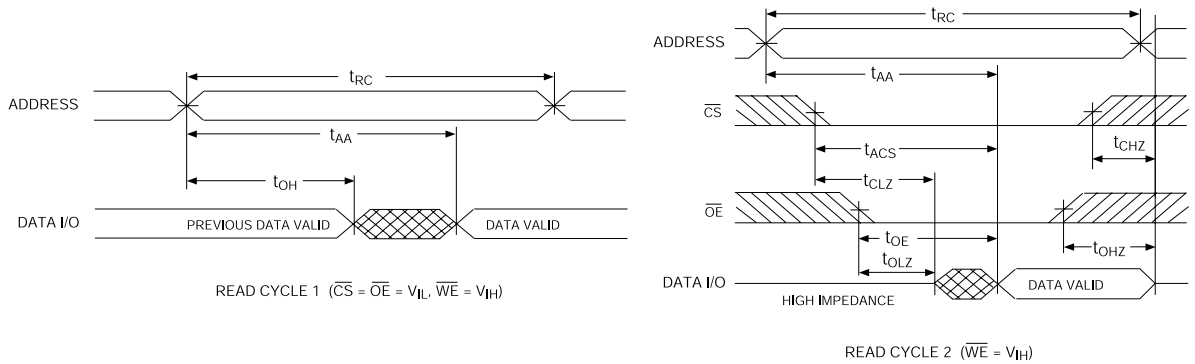


FIG. 6 WRITE CYCLE -  $\overline{WE}$  CONTROLLED

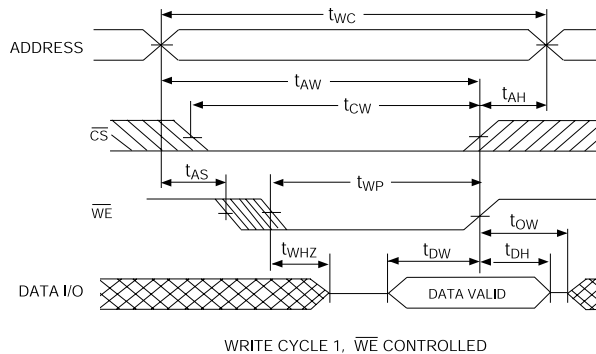
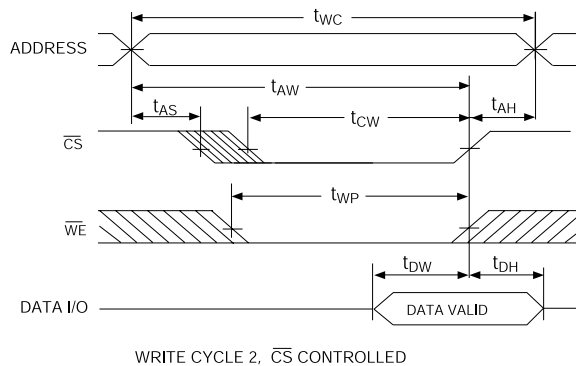
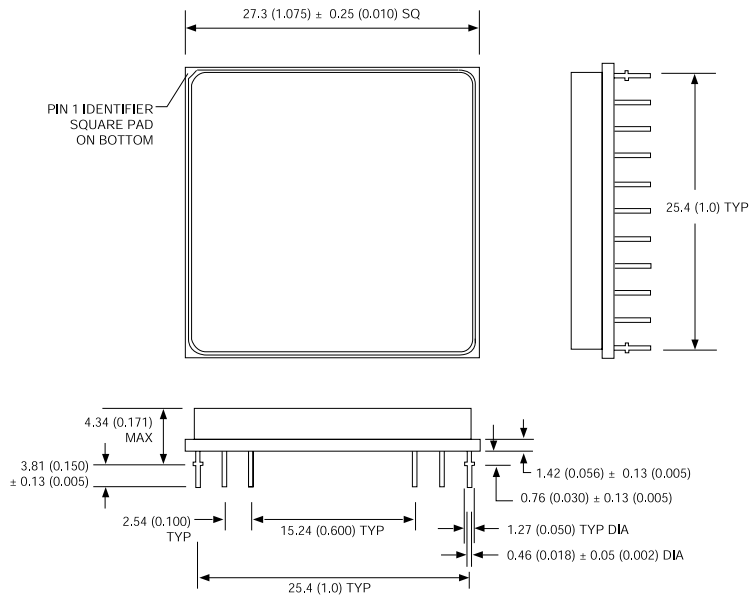


FIG. 7 WRITE CYCLE -  $\overline{CS}$  CONTROLLED



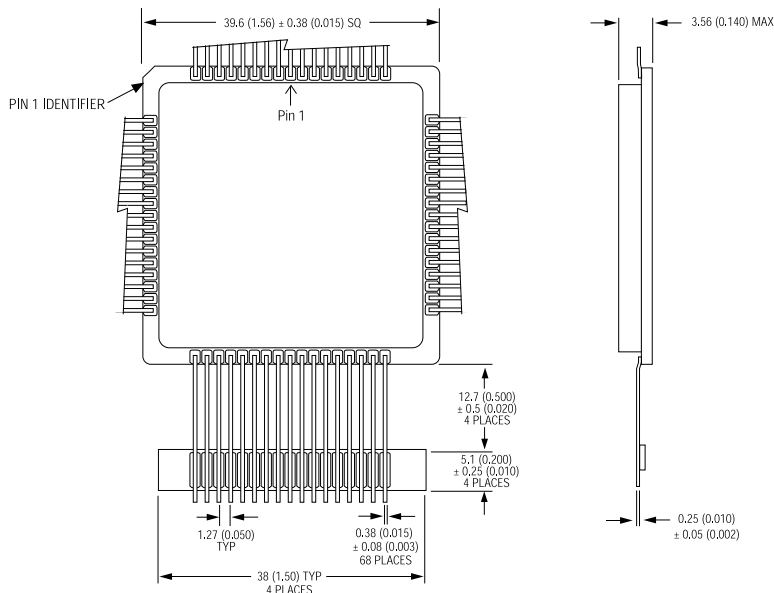


**PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)<sup>1</sup>**

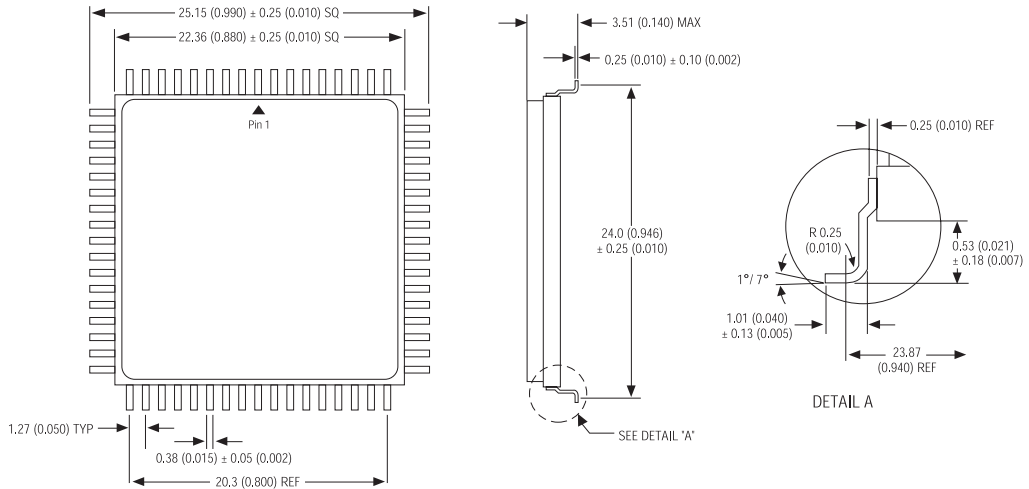


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

Note 1: Package Not Recommended For New Designs

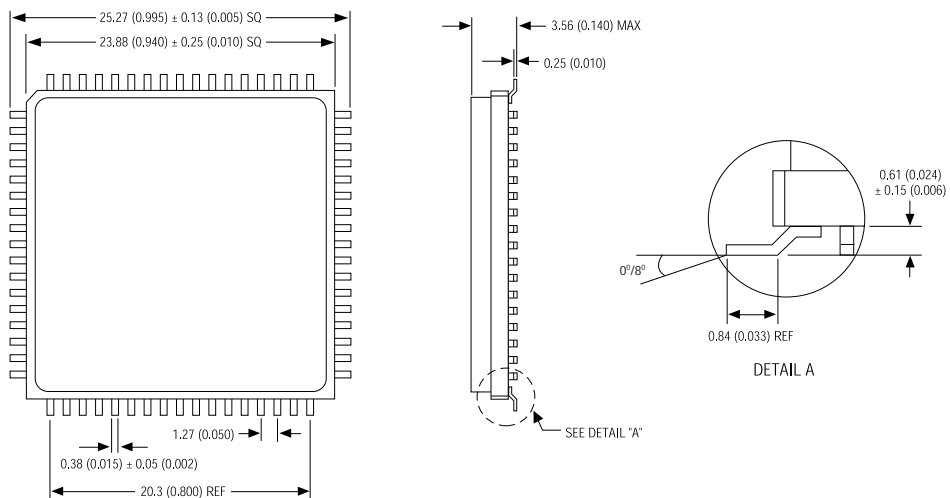


**PACKAGE 510: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2U)**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)<sup>1</sup>**

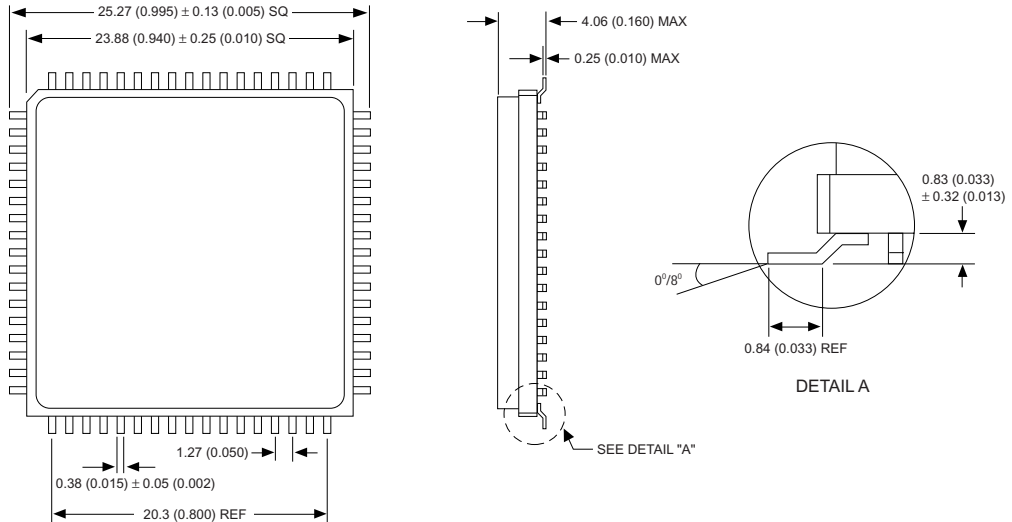


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

Note 1: Package Not Recommended For New Designs

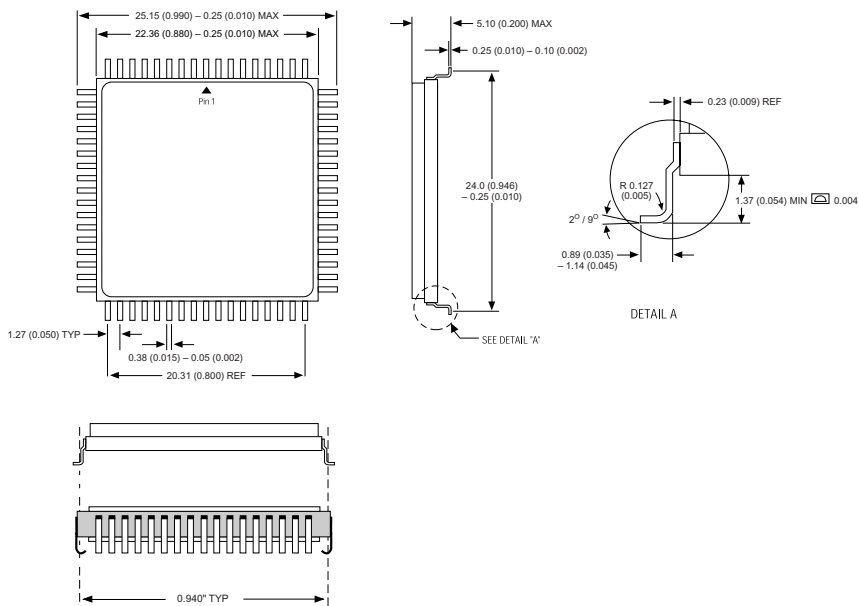


PACKAGE 524: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 528: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2L)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES





ORDERING INFORMATION

W S 128K 32 X - XXX X X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:

- H1 = 1.075" sq. Ceramic Hex-In-line Package, HIP (Package 400)
- G2U = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 510)
- G2L = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 528)
- G1U<sup>1</sup> = 23.9mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 519)
- G1T = 23.9mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 524)
- G4T<sup>1</sup> = 40 mm Low Profile CQFP (Package 502)

ACCESS TIME (ns)

IMPROVEMENT MARK:

- N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrades
- L = Low Power

ORGANIZATION, 128Kx32

User configurable as 256Kx16 or 512Kx8

SRAM

WHITE ELECTRONIC DESIGNS CORPORATION

\* Low Power Data Retention only available in G2T Package Type

Note 1: Package Not Recommended For New Designs



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 32 SRAM Module	55ns	66 pin HIP (H1)	5962-93187 05H4X
128K x 32 SRAM Module	45ns	66 pin HIP (H1)	5962-93187 06H4X
128K x 32 SRAM Module	35ns	66 pin HIP (H1)	5962-93187 07H4X
128K x 32 SRAM Module	25ns	66 pin HIP (H1)	5962-93187 08H4X
128K x 32 SRAM Module	20ns	66 pin HIP (H1)	5962-93187 09H4X
128K x 32 SRAM Module	17ns	66 pin HIP (H1)	5962-93187 10H4X
128K x 32 SRAM Module	15ns	66 pin HIP (H1)	5962-93187 11H4X
128K x 32 SRAM Module	55ns	68 lead CQFP Low Profile (G4T) <sup>1</sup>	5962-95595 05HYX <sup>1</sup>
128K x 32 SRAM Module	45ns	68 lead CQFP Low Profile (G4T) <sup>1</sup>	5962-95595 06HYX <sup>1</sup>
128K x 32 SRAM Module	35ns	68 lead CQFP Low Profile (G4T) <sup>1</sup>	5962-95595 07HYX <sup>1</sup>
128K x 32 SRAM Module	25ns	68 lead CQFP Low Profile (G4T) <sup>1</sup>	5962-95595 08HYX <sup>1</sup>
128K x 32 SRAM Module	20ns	68 lead CQFP Low Profile (G4T) <sup>1</sup>	5962-95595 09HYX <sup>1</sup>
128K x 32 SRAM Module	17ns	68 lead CQFP Low Profile (G4T) <sup>1</sup>	5962-95595 10HYX <sup>1</sup>
128K x 32 SRAM Module	15ns	68 lead CQFP Low Profile (G4T) <sup>1</sup>	5962-95595 11HYX <sup>1</sup>
128K x 32 SRAM Module	55ns	68 lead CQFP/J (G2U)	5962-95595 05HMX
128K x 32 SRAM Module	45ns	68 lead CQFP/J (G2U)	5962-95595 06HMX
128K x 32 SRAM Module	35ns	68 lead CQFP/J (G2U)	5962-95595 07HMX
128K x 32 SRAM Module	25ns	68 lead CQFP/J (G2U)	5962-95595 08HMX
128K x 32 SRAM Module	20ns	68 lead CQFP/J (G2U)	5962-95595 09HMX
128K x 32 SRAM Module	17ns	68 lead CQFP/J (G2U)	5962-95595 10HMX
128K x 32 SRAM Module	15ns	68 lead CQFP/J (G2U)	5962-95595 11HMX
128K x 32 SRAM Module	55ns	68 lead CQFP/J(G1U) <sup>1</sup>	5962-95595 05H9X
128K x 32 SRAM Module	45ns	68 lead CQFP/J (G1U) <sup>1</sup>	5962-95595 06H9X
128K x 32 SRAM Module	35ns	68 lead CQFP/J (G1U) <sup>1</sup>	5962-95595 07H9X
128K x 32 SRAM Module	25ns	68 lead CQFP/J (G1U) <sup>1</sup>	5962-95595 08H9X
128K x 32 SRAM Module	20ns	68 lead CQFP/J (G1U) <sup>1</sup>	5962-95595 09H9X
128K x 32 SRAM Module	17ns	68 lead CQFP/J (G1U) <sup>1</sup>	5962-95595 10H9X
128K x 32 SRAM Module	15ns	68 lead CQFP/J (G1U) <sup>1</sup>	5962-95595 11H9X
128K x 32 SRAM Module	55ns	68 lead CQFP/J (G2L)	5962-95595 05HAX
128K x 32 SRAM Module	45ns	68 lead CQFP/J(G2L)	5962-95595 06HAX
128K x 32 SRAM Module	35ns	68 lead CQFP/J(G2L)	5962-95595 07HAX
128K x 32 SRAM Module	25ns	68 lead CQFP/J(G2L)	5962-95595 08HAX
128K x 32 SRAM Module	20ns	68 lead CQFP/J(G2L)	5962-95595 09HAX
128K x 32 SRAM Module	17ns	68 lead CQFP/J(G2L)	5962-95595 010HAX
128K x 32 SRAM Module	15ns	68 lead CQFP/J(G2L)	5962-95595 011HAX

Note 1: Package Not Recommended For New Design