AT&T Microelectronics

T7513B PCM Codec with Filters

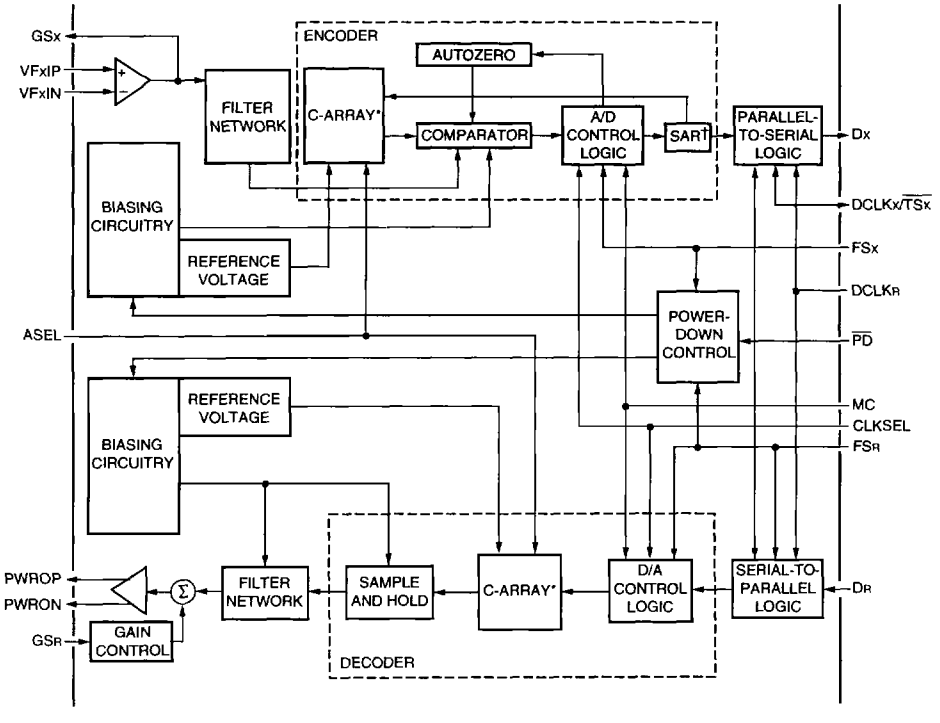
Features

- Direct replacement for the industry-standard 2913 device
- Low-power, latch-up-free CMOS technology
  — 65 mW typical operating power dissipation
  — 5 mW typical powerdown dissipation
- Pin-selectable μ-law or A-law operation
- On-chip sample and hold, autozero, and precision voltage reference; no external components required
- Differential architecture for high-noise immunity and PSRR
- Two timing modes:
  — Fixed data rate: 2.048 MHz, 1.544 MHz, or 1.536 MHz
  — Variable data rate: 64 kHz to 2.048 MHz
- Meets or exceeds D3/D4 (as per AT&T PUB 43801) and CCITT G.711—G.714 requirements
- Operating temperature range: –40 °C to +85 °C
- Pin selectable master clock rates of 2.048 MHz, 1.544 MHz, or 1.536 MHz

Description

The T7513B PCM Codec with Filters is a single-chip integrated circuit that provides analog-to-digital and digital-to-analog conversion. In addition, it provides the transmit and receive filtering necessary to interface a voice telephone circuit to a time-division multiplexed system. The T7513B device is a direct replacement for the T7513 or T7513A, offering enhanced functionality and significantly reduced power consumption. The T7513B device is available in a 20-pin, plastic DIP or in a 20-pin, plastic SOJ package for surface mounting.

Description (continued)



* Capacitor array.
† Successive approximation register.

Figure 1. Block Diagram

Pin Information

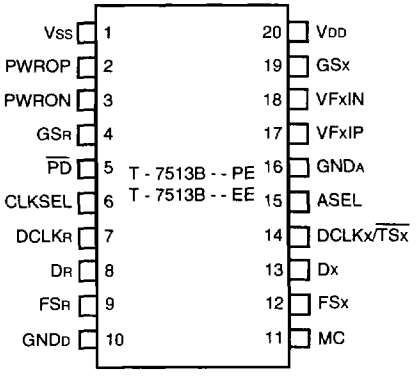


Figure 2. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	V_{SS}	—	**–5 V Supply (±5%).**
2	PWROP	O	**Noninverting Output of Receive Power Amplifiers.** This pin can drive transformer hybrids or high-impedance loads directly in either a differential or single-ended configuration.
3	PWRON	O	**Inverting Output of Receive Power Amplifiers.** Functionally identical and complementary to PWROP.
4	GS_R	I	**Receive Gain Setting Input.** Receive gain can be adjusted from 0 dB to –12 dB by varying the voltage at GS_R.
5	$\overline{PD}$	I	**Powerdown (Active-Low).** A TTL low on this pin places both the transmit and receive sections of the chip in powerdown mode. When high or floating, the device functions normally. A pull-up device is included.
6	CLKSEL	I	**Clock Select Input.** Must be tied to V_{SS} (2.048 MHz), GND_D (1.544 MHz), or V_{DD} (1.536 MHz) to reflect the frequency applied to the MC input.
7	$DCLK_R$	I	**Receive Data Clock.** When this pin is tied to V_{SS}, fixed-data-rate operation is selected. When this pin is not tied to V_{SS}, $DCLK_R$ is the TTL-level receive data clock, which operates at data rates from 64 kHz to 2.048 MHz.
8	D_R	I	**Receive PCM Input.** Data is clocked in on this input on the first eight consecutive negative transitions of $DCLK_R$ (variable-data-rate mode) or MC (fixed-data-rate mode) following the rising edge of FS_R. A pull-up device is included.
9	FS_R	I	**8 kHz Receive Frame-Synchronization Clock.** In the fixed-data-rate mode, FS_R is an edge trigger and must be high for a minimum of one MC cycle. In the variable-data-rate mode, it must be held high for a minimum of eight $DCLK_R$ cycles. For proper device operation, this clock should be derived from MC. This means that FSx and FS_R must both be an exact submultiple of MC. Depending on the MC frequency used (2.048 MHz, 1.544 MHz, or 1.536 MHz), the divide-down must be 256, 193, or 192. If the T7513B is used as a digital-to-analog converter only, it is still necessary to tie FSx to FS_R. Failure to do this can result in improper conversion. A pull-down device is included.
10	GND_D	—	**Digital Ground.** Internally separate from GND_A.
11	MC	I	**Master Clock Input.** The MC frequency must be 2.048 MHz, 1.544 MHz, or 1.536 MHz depending on the voltage at the CLKSEL input. In the fixed-data-rate mode, this input also acts as the transmit and receive data clock. A pull-down device is included.
12	FSx	I	**8 kHz Transmit Frame-Synchronization Clock.** Operates independently of, but in a manner analogous to, FS_R. For proper device operation, this clock should be derived from MC. This means that FSx and FS_R must both be an exact submultiple of MC. Depending on the MC frequency used (2.048 MHz, 1.544 MHz, or 1.536 MHz), the divide-down must be 256, 193, or 192. If the T7513B is used as a digital-to-analog converter only, it is still necessary to tie FSx to FS_R. Failure to do this can result in improper conversion. A pull-down device is included.
13	Dx	O	**Transmit PCM Output.** Data is clocked out on this lead on the first eight consecutive positive transitions of DCLKx (variable-data-rate mode) or MC (fixed-data-rate mode) following the rising edge of FSx. Dx remains in a high-impedance state unless the transmit time slot is activated by the rising edge of FSx.
14	DCLKx/$\overline{TSx}$	I/O	**Transmit Data Clock/Time-Slot Enable Strobe.** In the variable-data-rate mode, DCLKx is a TTL-level input that operates between 64 kHz and 2.048 MHz as the transmit data clock. In the fixed-data-rate mode, this pin is an open-drain output providing a time-slot enable strobe for use with an external 3-state buffer.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Name/Function
15	ASEL	I	**μ-law/A-law Select Input.** When this pin is tied to Vss, A-law operation is selected. When this pin is tied to V_{DD} or GND_D, μ-law companding is selected.
16	GND_A	—	**Analog Ground.** Internally separate from GND_D.
17	VFxIP	I	**Noninverting Analog Input to Operational Amplifier.** Noninverting analog input to the uncommitted operational amplifier at the transmit filter input.
18	VFxIN	I	**Inverting Analog Input to Operational Amplifier.** Inverting analog input to the uncommitted operational amplifier at the transmit filter input.
19	GSx	O	**Output of Transmit-Side Operational Amplifier.** Output of transmit-side, uncommitted operational amplifier. Internally, this pin is the positive input to the transmit differential filters.
20	V_{DD}	—	**+5 V Supply (±5%).**

Functional Description

Powerdown and Standby Modes

The T7513B Codec is powered up whenever the following criteria are met: V_{DD} and Vss power supply voltages are applied, all required clocks are active (MC for fixed-data-rate mode; MC, DCLKx, and $DCLK_R$ for variable-data-rate mode), a TTL-high is applied to $\overline{PD}$, and both the FSx and FS_R synchronization signals are applied.

On the transmit channel, the digital outputs Dx and $\overline{TSx}$ are held in a high-impedance state for approximately 500 μs after powerup. After this delay, during which the control circuits are initialized, the digital outputs are functional and occur in the proper time slot.

The encoder analog circuitry includes an autozero circuit that requires about 60 ms to reach an equilibrium value after powerup. Although the digital outputs are active after approximately four frames, the PCM output is not initially a valid representation of the analog input.

To further protect the integrity of the PCM highway, the T7513B Codec includes a lost-clock detection circuit, which places the Dx and $\overline{TSx}$ outputs in a high-impedance state approximately 20 μs after an interruption of MC.

The T7513B device provides two powerdown modes of operation that reduce power consumption when the device is inactive. Full powerdown mode is activated by placing a TTL-low signal on the $\overline{PD}$ input. In this mode, the power consumption is reduced to approximately 5 mW. The standby mode is automatically entered whenever both FSx and FS_R have been TTL-low for approximately 300 ms. Reactivating either or both of the frame-synchronization signals restores full operation. The standby power is approximately 10 mW. During both powerdown and standby operation, the digital outputs Dx and $\overline{TSx}$ and the analog outputs PWROP and PWRON enter a high-impedance state. The digital outputs become active immediately upon exiting standby or within approximately 500 μs after leaving powerdown. In both cases, approximately 60 ms is required to recover analog functionality.

Digital Interface

The T7513B digital interface uses a common master clock and independent synchronization and timing signals for the transmit and receive channels. Permissible master clock frequencies are 2.048 MHz, 1.544 MHz, or 1.536 MHz. The chosen MC frequency must be reflected in the setting of the CLKSEL input. Two operating modes are provided for the PCM interface: fixed data rate and variable data rate.

The fixed-data-rate mode is selected by strapping $DCLK_R$ to Vss. In the fixed-data-rate mode, data I/O is synchronized by the FSx and FS_R inputs, but data timing for both channels is controlled by MC. Because bit timing is determined by MC, the only available bit rates are 2.048 MHz, 1.544 MHz, and 1.536 MHz. FSx and FS_R must be high for a minimum of one MC cycle and can be operated independently. When in the fixed-data-rate mode, the DCLKx pin becomes an open-drain output that can be used to enable an external 3-state buffer. The internal Dx buffer automatically enters a high-impedance state whenever Dx is inactive. Fixed-data-rate timing is illustrated in Figures 8 and 9.

Functional Description (continued)

Digital Interface (continued)

The variable-data-rate mode is selected by connecting DCLKx and DCLKR to the system transmit and receive data clocks, respectively. In this mode, DCLKx and DCLKR are independent, asynchronous clocks that can vary in frequency from 64 kHz to 2.048 MHz and that need to be synchronized to MC only at the beginning of each frame (see Figures 10 and 11 for details). Data transmission on the Dx lead is initiated on the rising edge of FSx, with bit timing determined by DCLKx. FSx is required to be high for a minimum of eight DCLKx cycles in order for the full PCM word to be transmitted. If FSx is held higher longer than eight cycles, the Dx data is repeated as long as FSx is high.

Receive data transfer is initiated on the rising edge of the FSR pulse, with bit timing being controlled by DCLKR. Variable-data-rate timing is illustrated in Figures 10 and 11. FSR must be held high for a minimum of eight DLCKR periods; if it is longer, no additional bits are read and conversion proceeds.

Companding Laws

The T7513B supports both μ-law and A-law operation. A-law operation is selected by strapping the ASEL input to Vss. For μ-law operation, ASEL should be tied to either VDD or GNDD; it should never be left floating. Alternate bit inversion is used for A-law transmission.

To overcome the inherently noisy nature of A-law companding, the T7513B device has an encoder squelch circuit that is enabled during A-law operation. This circuit clamps the sign bit of the encoder output high after eight consecutive frames in which the magnitude of the encoded signal has been equal to ±1 LSB. Squelching is immediately disengaged whenever the encoder output exceeds 1 LSB in magnitude. The squelch circuit is disabled during μ-law operation.

Transmission Levels

Zero-transmission-level points in Table 2 are specified relative to the digital milliwatt sequence prescribed by CCITT recommendation G.711 for a codec configured with unity-gain, single-ended input (GSx tied to VFxIN, input at VFxIP) and maximum-gain, single-ended output (GSR tied to PWRON, output measured between PWROP and GNDA). Under these conditions, an analog input of 1.064 Vrms for μ-law or 1.068 Vrms for A-law applied to VFxIP produces a 0 dBm digital code, while a 0 dBm code input at DR produces an output of 1.503 Vrms for μ-law or 1.509 for A-law at PWROP.

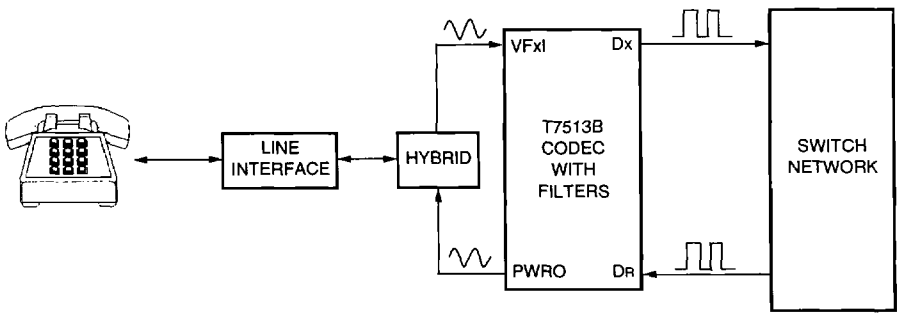


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Figure 3. PCM System Block Diagram

Functional Description (continued)

Transmission Levels (continued)

Table 2. Zero-Transmission-Level Points

Parameter	Symbol	Test Condition	Value	Unit
Zero-transmission-level Point (transmit channel at 0 dBm0, μ-law)	0TLP1x	Referenced to 600 Ω Referenced to 900 Ω	2.76 1.00	dBm dBm
Zero-transmission-level Point (transmit channel at 0 dBm0, A-law)	0TLP2x	Referenced to 600 Ω Referenced to 900 Ω	2.79 1.03	dBm dBm
Zero-transmission-level Point (receive channel at 0 dBm0, μ-law)	0TLP1R	Referenced to 600 Ω Referenced to 900 Ω	5.76 4.00	dBm dBm
Zero-transmission-level Point (receive channel at 0 dBm0, A-law)	0TLP2R	Referenced to 600 Ω Referenced to 900 Ω	5.79 4.03	dBm dBm

Analog Input

The analog input section of the T7513B device includes an uncommitted input amplifier for added flexibility in interfacing with transmission systems. Possible applications include two- to four-wire conversion and/or gain adjustment. A schematic of the input circuit is shown in Figure 4. A conventional, single-ended, unity-gain configuration is achieved by simply connecting GSx to VFxIN and applying the analog signal between VFxIP and GNDA. If the analog signal is ac coupled into VFxIP, an impedance of 1 MΩ or less should be connected between VFxIP and GNDA. The load impedance to ground at the GSx output should be greater than 10 kΩ in parallel with less than 50 pF.

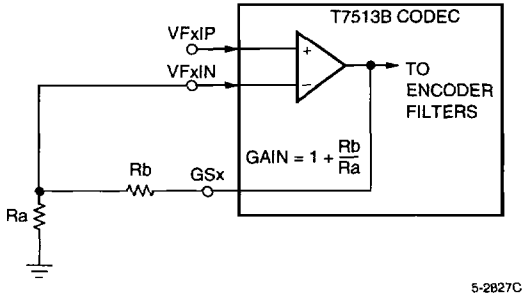

Figure 4. Analog Inputs

Analog Output

The analog output of the T7513B device is provided via a set of low-impedance complementary outputs, PWROP and PWRON. Either of the outputs can be used as a single-ended output to drive loads as low as 300 Ω, or the outputs can be used together to provide a 600 Ω differential drive capability. Receive gain is set by interpolating the voltage at the buffered, high-impedance GSR input between the voltages at the PWROP and PWRON nodes with a resistive divider network. Gain varies from 0 dB to −12 dB, according to the relationship shown in the equation:

$$A = \left(\frac{1 + \left[\frac{R1}{R2}\right]}{4 + \left[\frac{R1}{R2}\right]} \right)$$

where R1 and R2 are connected as shown in Figure 5 and the output is taken single-ended. The maximum gain (A = 1) is achieved with GSR tied to PWRON (R1/R2 = ∞), and the minimum output (A = 1/4) is achieved by connecting GSR to PWROP (R1/R2 = 0). For proper device operation, it is recommended that R1 and R2 be chosen such that R1 + R2 > 10 kΩ and that the parallel combination of R1 and R2 is less than 100 kΩ.

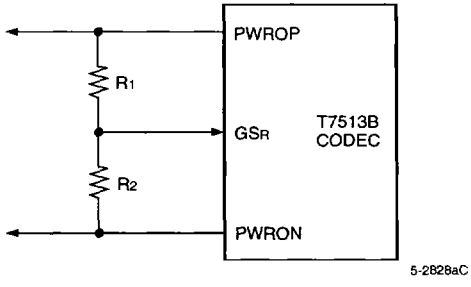

Figure 5. Analog Outputs

Absolute Maximum Ratings

Stresses in excess of Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability. External leads can be bonded or soldered at temperatures up to 300 °C.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–55	150	°C
Positive Power Supply Voltage	V_{DD}	—	7.5	V
Negative Power Supply Voltage	V_{SS}	–7.5	—	V
Voltage on Pins 2, 3, 4, 6, 7, 15, 17, 18, and 19 with Respect to Ground	—	–0.5 V + V_{SS}	+0.5 V + V_{DD}	V
Voltage on Pins 5, 8, 9, 11, 12, 13, and 14 with Respect to Ground	—	–0.5 V	+0.5 V + V_{DD}	V
Maximum Power Dissipation (package limit)	P_{DISS}	—	600	mW

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 3. HBM ESD Threshold Voltage

Device	Voltage
T7513B	>4000 V

Electrical Characteristics

For all tests, T_A = –40 °C to +85 °C, V_{DD} = 5 V ± 5%, V_{SS} = –5 V ± 5%, and GND_A = GND_D = 0 V, unless otherwise noted. Typical values are for T_A = 25 °C and nominal supply values.

dc Characteristics

Table 4. Digital Interface

Parameter			Symbol	Test Conditions	T_A (°C)	Min	Typ	Max	Unit
Input Current	Pins 5, 8	Low	I_{IL}	$GND_D \le V_{IN} \le V_{IL}$	–40 to 0	–120	—	—	µA
					0 to 85	–80	—	—	µA
		High	I_{IH}	$V_{IH} \le V_{IN} \le V_{DD}$	—	—	—	10	µA
	Pins 6, 7, 15	Low	I_{IL}	$V_{SS} \le V_{IN} \le V_{IL}$	—	–10	—	—	µA
		High	I_{IH}	$V_{IH} \le V_{IN} \le V_{DD}$	—	—	—	10	µA
	Pins 9, 11, 12	Low	I_{IL}	$GND_D \le V_{IN} \le V_{IL}$	—	–10	—	—	µA
		High	I_{IH}	$V_{IH} \le V_{IN} \le V_{DD}$	–40 to 0	—	—	150	µA
					0 to 85	—	—	110	µA
	Pin 14	Low	I_{IL}	$GND_D \le V_{IN} \le V_{IL}$	—	–20	—	—	µA
		High	I_{IH}	$V_{IH} \le V_{IN} \le V_{DD}$	—	—	—	20	µA
Input Voltage		Low	V_{IL}	—	—	—	—	0.8	V
		High	V_{IH}	—	—	2.0	—	—	V
Output Voltage		Low	V_{OL}	I_{OL} = 1 mA	—	—	—	0.4	V
		High	V_{OH}	I_{OH} = 1 mA	—	2.4	—	—	V
		High	V_{OHC}	I_{OHC} = 0.1 mA	—	3.5	—	—	V
Digital Input Capacitance			C_I	—	—	—	—	5	pF
Output Leakage Current			IL	—	—	–50	—	50	µA

Electrical Characteristics (continued)

dc Characteristics (continued)

Table 5. Power Dissipation

All measurements are made at fMC = fDCLK = 2.048 MHz, outputs unloaded.

Parameter	Symbol	Min	Typ	Max	Unit
Operating Current:					
V_{DD}	I_{DD1}	—	7	9	mA
V_{SS}	I_{SS1}	–8	–6	—	mA
Powerdown Current:					
V_{DD}	I_{DD0}	—	0.5	1	mA
V_{SS}	I_{SS0}	–1	–0.5	—	mA
Operating Voltage:					
Positive	V_{DD}	4.75	5.0	5.25	V
Negative	V_{SS}	–5.25	–5.0	–4.75	V
Dissipation:					
Operating Power	P_1	—	65	90	mW
Standby	P_S	—	10	22	mW
Powerdown	P_0	—	5	11	mW

Table 6. Analog Interface—Transmit Filter Input Stage

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current, VFxIP, VFxIN	I_{BXI}	$-2.17\ V \le V_{IN} \le 2.17\ V$	–100	—	100	nA
Input Resistance, VFxIP, VFxIN	R_{IXI}	—	10	—	—	MΩ
Input Offset Voltage, VFxIP, VFxIN	V_{OSXI}	—	–25	—	25	mV
Common-mode Rejection, VFxIP	CMRR	$-2.17\ V \le V_{IN} \le 2.17\ V$	55	—	—	dB
dc Open-loop Voltage Gain, GSx	A_{VOL}	—	5000	—	—	—
Open-loop Unity Gain Bandwidth, GSx	fc	—	—	1	—	MHz
Load Capacitance, GSx	C_{LXI}	—	—	—	50	pF
Minimum Load Resistance, GSx	R_{LXI}	—	10	—	—	kΩ

Table 7. Analog Interface—Receive Filter Driver Amplifier Stage

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Resistance, PWROP, PWRON	R_{ORA}	—	—	1	2	Ω
Single-ended Output dc Offset, PWROP, PWRON	V_{OSRA}	Relative to GND_A	–120	±30	+120	mV
Load Capacitance, PWROP, PWRON	C_{LRA}	—	—	—	100	pF
Input Leakage Current, GS_R	I_{BGSR}	$-2.17\ V \le V_{IN} \le 2.17\ V$	–100	—	100	nA
Input Resistance, GS_R	R_{IGSR}	—	10	—	—	MΩ

Electrical Characteristics (continued)

ac Transmission Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity-gain, noninverting. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The receive output is measured single-ended maximum-gain configuration. All output levels are sin(x)/x-corrected.

Note: For unity-gain input, GSx is connected to VFxIN, and the signal input is at VFxIP; for maximum-gain output, GS_R is connected to PWRON, and the output is at PWROP.

Table 8. Gain and Dynamic Range

Parameter	Symbol	Test Conditions	T_A (°C)	Min	Typ	Max	Unit
Encoder Milliwatt Response (transmit gain tolerance)	EmW	Signal input of 1.064 Vrms, μ-law; Signal input of 1.068 Vrms, A-law; ±5% supplies	–40 to 0	–0.25	±0.04	0.25	dBm0
			0 to 85	–0.18	±0.04	0.18	dBm0
Decoder Milliwatt Response (receive gain tolerance)	DmW	Measured relative to 0TLPR (1.503 Vrms, μ-law; 1.509 Vrms, A-law); PCM input of 0 dBm0, 1020 Hz; ±5% supplies; load = 10 kΩ	–40 to 0	–0.30	±0.04	0.30	dBm0
			0 to 85	–0.18	±0.04	0.18	dBm0
Relative Gain: PWROP to PWRON	—	D_R = 0 dBm0, f = 300 Hz—3400 Hz	—	—	±0.01	—	dB
Relative Phase: –PWROP to PWRON	—	D_R = 0 dBm0, f = 300 Hz—3500 Hz	—	—	±0.25	—	Deg

Table 9. Gain Tracking—Reference Level = 1.02 kHz, 0 dBm0

Parameter	Symbol	Test Conditions	T_A (°C)	Min	Max	Unit
Transmit Gain Tracking Error (sinusoidal input, μ-law)	GT1x	+3 dBm0 to –37 dBm0	—	–0.25	0.25	dB
		–37 dBm0 to –50 dBm0	—	–0.50	0.50	dB
Transmit Gain Tracking Error (sinusoidal input, A-law)	GT2x	+3 dBm0 to –37 dBm0	—	–0.25	0.25	dB
		–37 dBm0 to –50 dBm0	—	–0.50	0.50	dB
Receive Gain Tracking Error (sinusoidal input, μ-law)	$GT1_R$	+3 dBm0 to 0 dBm0	–40 to 0	–0.60	0.60	dB
			0 to 85	–0.25	0.25	dB
		0 dBm0 to –37 dBm0	—	–0.25	0.25	dB
		–37 dBm0 to –50 dBm0	—	–0.50	0.50	dB
Receive Gain Tracking Error (sinusoidal input, A-law)	$GT2_R$	+3 dBm0 to 0 dBm0	–40 to 0	–0.60	0.60	dB
			0 to 85	–0.25	0.25	dB
		0 dBm0 to –37 dBm0	—	–0.25	0.25	dB
		–37 dBm0 to –50 dBm0	—	–0.50	0.50	dB

Electrical Characteristics (continued)

ac Transmission Characteristics (continued)

Table 10. Distortion

Parameter	Sym	Test Conditions	T_A (°C)	Min*	Typ	Max	Unit
Transmit Signal to Distortion (sinusoidal input = 1.02 kHz):	SD_X	μ-law, 3 dBm0 ≤ VFxI ≤ –30 dBm0	—	36, (34)	—	—	dB
		A-law, 3 dBm0 ≤ VFxI ≤ –30 dBm0	—	35, (33)	—	—	dB
		μ-law, –30 dBm0 < VFxI ≤ –40 dBm0	—	30, (28)	—	—	dB
		A-law, –30 dBm0 < VFxI ≤ –40 dBm0	—	29, (27)	—	—	dB
		μ-law, –40 dBm0 < VFxI ≤ –45 dBm0	—	25, (22)	—	—	dB
		A-law, –40 dBm0 < VFxI ≤ –45 dBm0	—	25, (22)	—	—	dB
Receive Signal to Distortion (sinusoidal input = 1.02 kHz):	SD_R	μ-law, 3 dBm0 ≤ DF_{RI} ≤ 0 dBm0	–40 to 0	26, (25)	—	—	dB
			0 to 85	36, (34)	—	—	dB
		A-law, 3 dBm0 ≤ DF_{RI} ≤ 0 dBm0	–40 to 0	26, (25)	—	—	dB
			0 to 85	35, (33)	—	—	dB
		μ-law, 0 dBm0 ≤ DF_{RI} ≤ –30 dBm0	—	36, (34)	—	—	dB
		A-law, 0 dBm0 ≤ DF_{RI} ≤ –30 dBm0	—	35, (33)	—	—	dB
		μ-law, –30 dBm0 ≤ DF_{RI} ≤ –40 dBm0	—	30, (28)	—	—	dB
		A-law, –30 dBm0 ≤ DF_{RI} ≤ –40 dBm0	—	29, (27)	—	—	dB
		μ-law, –40 dBm0 ≤ DF_{RI} ≤ –45 dBm0	—	25, (23)	—	—	dB
		A-law, –40 dBm0 ≤ DF_{RI} ≤ –45 dBm0	—	25, (23)	—	—	dB
Transmit Single-frequency Distortion Products	DP_X	0 MHz ≤ input ≤ 2 MHz	—	—	—	–28	dBm0
		0.2 kHz ≤ input ≤ 3.4 kHz	—	—	—	–40	dBm0
Receive Single-frequency Distortion Products	DP_R	0 MHz ≤ input ≤ 2 MHz	—	—	—	–28	dBm0
		0.2 kHz ≤ input ≤ 3.4 kHz	—	—	—	–40	dBm0
Transmit Absolute Delay	D_{AX}	—	—	—	340	—	μs
Receive Absolute Delay	D_{AR}	—	—	—	100	—	μs
Delay Distortion (analog to analog, measured relative to minimum)	D_{DAA}	f = 500 Hz	—	—	260		μs
		f = 1 kHz	—	—	10		μs
		f = 1.5 kHz	—	—	10		μs
		f = 2 kHz	—	—	40		μs
		f = 2.5 kHz	—	—	110		μs
		f = 3 kHz	—	—	290		μs
Intermodulation (end to end)	—	CCITT G.712 (8.1)	—	—	–50	–35	dB
Intermodulation (end to end)	—	CCITT G.712 (8.2)	—	—	–60	–49	dBm0
Spurious Out-of-band Signals (end to end)	—	CCITT G.712 (7.1)	—	—	–35	–25	dBm0

* Limits in parentheses are for operation with MC = 1.544 Mbits only.

Electrical Characteristics (continued)

ac Transmission Characteristics (continued)

Table 11. Noise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Idle Channel Noise (C-message weighted)	N_{XC}	μ-law	—	—	18	dBrnC0
Receive Idle Channel Noise (C-message weighted)	N_{RC}	μ-law	—	4	13	dBrnC0
Transmit Idle Channel Noise (psophometric weighted)	N_{XP}	A-law (squelched)	—	—	–89	dBm0p
Receive Idle Channel Noise (psophometric weighted)	N_{XR}	A-law	—	–81	–75	dBm0p
V_{DD} Power Supply Rejection (transmit channel)	PSR1	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz signal at Dx	—	–45	–30	dB
V_{SS} Power Supply Rejection (transmit channel)	PSR2	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz signal at Dx	—	–45	–30	dB
V_{DD} Power Supply Rejection (receive channel)	PSR3	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz signal at PWROP	—	–45	–30	dB
V_{SS} Power Supply Rejection (receive channel)	PSR4	Idle channel; 100 mVpp, 1.02 kHz signal on dc supply; measured 1.02 kHz signal at PWROP	—	–45	–30	dB
Crosstalk (transmit to receive, single-ended outputs): μ-law	CT_{XR}	VFxIP = 2.76 dBm0; 1.02 kHz signal measured at PWROP, D_R = idle code	—	–80	–70	dB
Crosstalk (receive to transmit, single-ended outputs): μ-law	CT_{RX}	DR = 0 dBm0; 1.02 kHz signal measured at DX; VFxIP = GND_A 1.02 kHz signal measured at Dx	—	–80	–70	dB

Electrical Characteristics (continued)

ac Transmission Characteristics (continued)

Table 12. Receive Gain Relative to Gain at 1.02 kHz (GRR, 0 dBm0 signal input at D_R) (See Figure 6.)

Frequency (Hz)	Min	Typ	Max	Unit
Below 3000	–0.125	±0.04	0.125	dB
3140	–0.57	±0.04	0.125	dB
3380	–0.885	–0.58	0.015	dB
3860	—	–10.7	–8.98	dB
4600 and above	—	—	–28	dB

Table 13. Transmit Gain Relative to Gain at 1.02 kHz (GRX, 0 dBm0 signal input, unity-gain input configuration) (See Figure 7.)

Frequency (Hz)	Min	Typ	Max	Unit
16.67	—	–50	–30	dB
40	—	–34	–26	dB
50	—	–36	–30	dB
60	—	–50	–30	dB
200	–1.8	–0.5	0	dB
300 to 3000	–0.125	±0.04	0.125	dB
3140	–0.57	0.01	0.125	dB
3380	–0.885	–0.7	0.015	dB
3860	—	–9.9	–8.98	dB
4600 and above	—	—	–32	dB

Electrical Characteristics (continued)

ac Transmission Characteristics (continued)

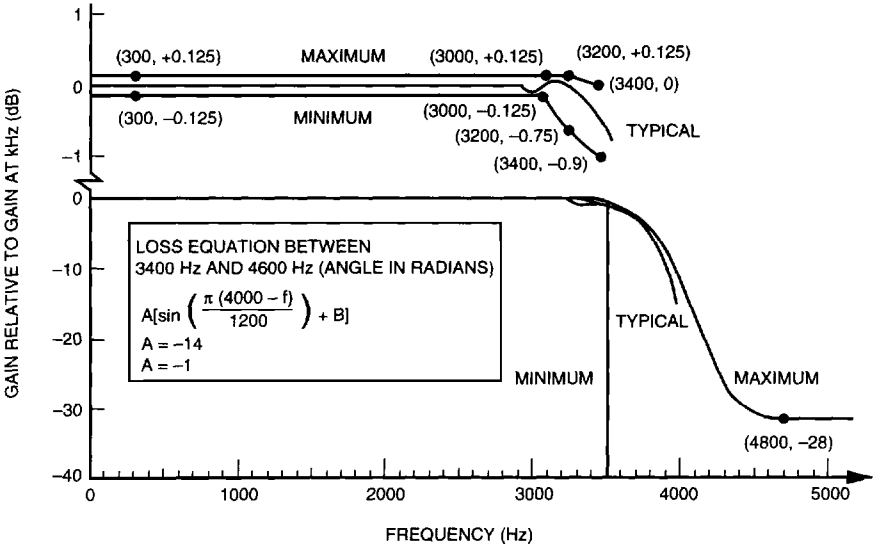

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Figure 6. Receive Filter Characteristics

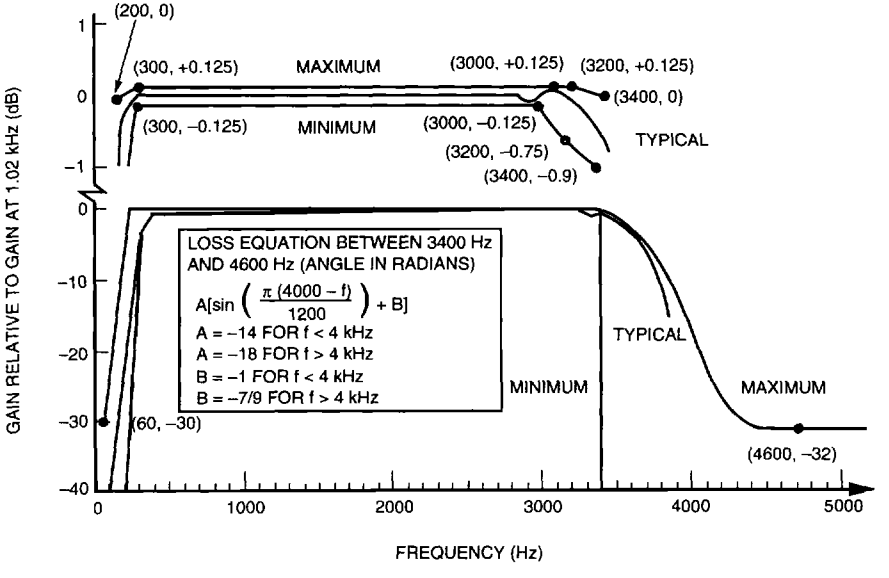

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Figure 7. Transmit Filter Characteristics

Timing Characteristics

Table 14. Clock Section (See Figures 8, 9, 10, and 11.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tMCHMCH	Clock Period, MC	f_{MC} = 2.048 MHz	—	488	—	ns
tMCHMCL1	Clock Pulse Width, MC	—	195	—	—	ns
tDCHDCH	Data Clock Pulse Width	64 kHz ≤ fDCLK ≤ 2.048 MHz	195	—	—	ns
tCDC	Clock Duty Cycle, MC	—	40	50	60	%
tMCH1MCH2 tMCL2MCL1	Clock Rise and Fall Time	—	0	—	30	ns

Table 15. Transmit Section, Fixed-Data-Rate Mode (See Figure 8.)

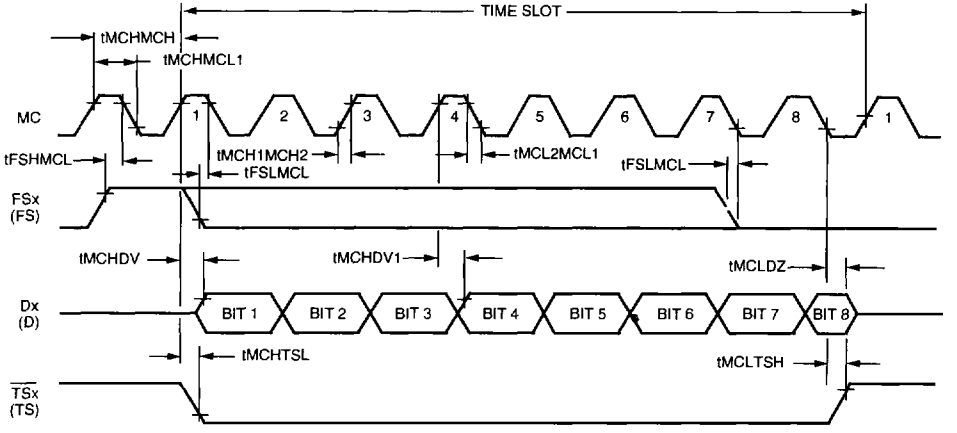
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tMCHDV	Data Enabled on TS Entry	0 < C_{LOAD} < 100 pF	0	—	145	ns
tMCHDV1	Data Delay from MC	0 < C_{LOAD} < 100 pF	—	—	145	ns
tMCLDZ*	Data Float on TS Exit	C_{LOAD} = 0	60	—	215	ns
tMCHTSL	Time-slot X to Enable	0 < C_{LOAD} < 100 pF	0	—	145	ns
tMCLTSH	Time-slot X to Disable	C_{LOAD} = 0	60	—	215	ns
tFSHMCL	Frame-sync Delay High	—	100	—	tMCHMCH – 100	ns
tFSLMCL	Frame-sync Delay Low	—	100	—	tMCHMCH – 100	ns

* Timing parameter tMCLDZ is referenced to a high-impedance state.

Table 16. Receive Section, Fixed-Data-Rate Mode (See Figure 9.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tDVMCL	Receive Data Setup	—	10	—	—	ns
tMCLDV	Receive Data Hold	—	60	—	—	ns
tFSHMCL	Frame-sync Delay High	—	100	—	tMCHMCH – 100	ns
tFSLMCL	Frame-sync Delay Low	—	100	—	tMCHMCH – 100	ns

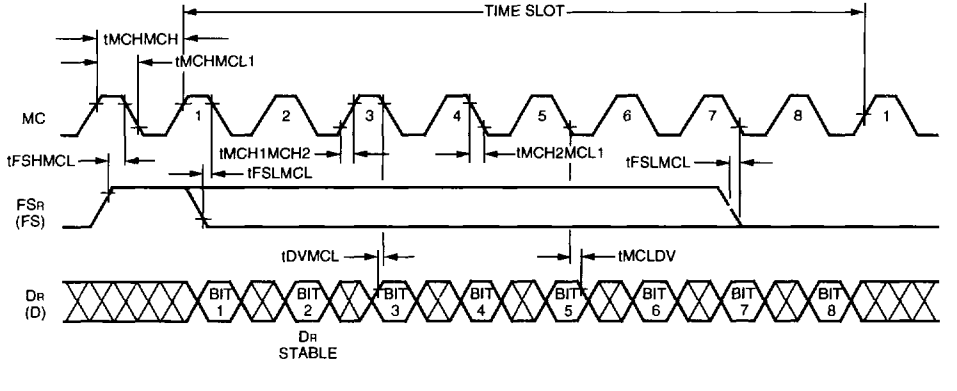
Timing Characteristics (continued)



Notes:
All timing parameters referenced to V_{IH} and V_{IL}, except tMCLDZ, which references a high-impedance state.

Bit 1 = sign bit.

Figure 8. Fixed-Data-Rate Transmit Timing



Notes:
All timing parameters referenced to V_{IH} and V_{IL}.

Bit 1 = sign bit.

Figure 9. Fixed-Data-Rate Receive Timing

Timing Characteristics (continued)

Table 17. Transmit Section, Variable-Data-Rate Mode* (See Figure 10.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tFSHDCL	Time-slot Delay from DCLKx*	—	140	—	tDCHDCH – 140	ns
tFSHMCL	Frame-sync Delay	—	100	—	tMCHMCH – 100	ns
tDCHDV	Data Delay from DCLKx	0 < CLOAD < 100 pF	0	—	100	ns
tFSHDV	Time-slot to Dx Active†	0 < CLOAD < 100 pF	0	—	50	ns
tFSLDX	Time-slot to Dx Inactive†	0 < CLOAD < 100 pF	0	—	80	ns
tDCHDCH	Data Clock Period < 2.048 MHz	64 kHz < fDCLKx	488	—	15620	ns
tFSHDV1	Data Delay from FSx	—	0	—	140	ns

* tFSLX minimum requirements override tFSHDCL maximum specifications for 64 kHz operation.
† Timing parameters tFSHDV and tFSLDX are referenced to a high-impedance state.

Table 18. Receive Section, Variable-Data-Rate Mode* (See Figure 11.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tFSHDCL	Time-slot Delay from DCLKR*	—	140	—	tDCHDCH – 140	ns
tFSHMCL	Frame-sync Delay	—	100	—	tMCHMCH – 100	ns
tDVDCL	Data Setup Time	—	10	—	—	ns
tDCLDX	Data Hold Time	—	60	—	—	ns
tDCHDCH	Data Clock Period	64 kHz < fDCLKx < 2.048 MHz	488	—	15620	ns
tDCLFSL	Time-slot End Receive Time	—	60	—	—	ns

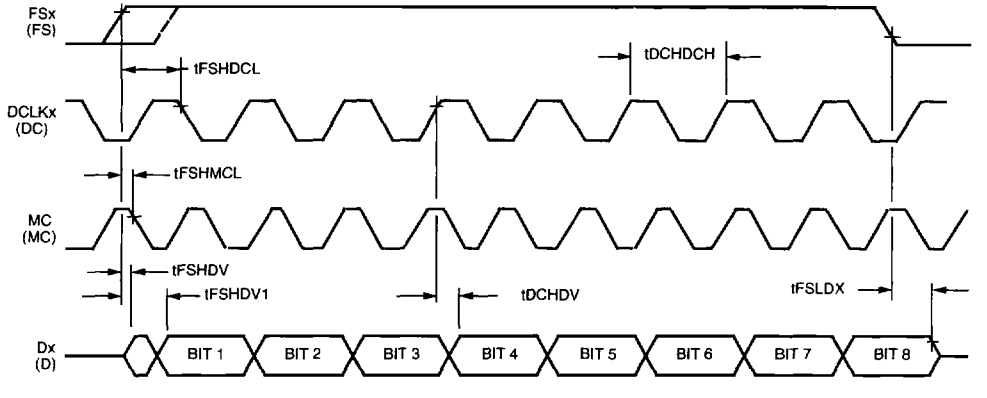
* tFSLX minimum requirements override tFSHDCL maximum specifications for 64 kHz operation.

Table 19. 64 kHz Operation, Variable-Data-Rate Mode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tFSLX*	Transmit Frame-sync Minimum Downtime	FSx is TTL-high for remainder of frame	488	—	—	ns
tFSLR†	Receive Frame-sync Minimum Downtime	FSR is TTL-high for remainder of frame	1952	—	—	ns
tDCLK	Data Clock Pulse Width	—	—	—	10	µs

* tFSLX minimum requirements override tFSHDCL maximum specifications for 64 kHz operation.
† tFSLR minimum requirements override tFSHDCL maximum specifications for 64 kHz operation.

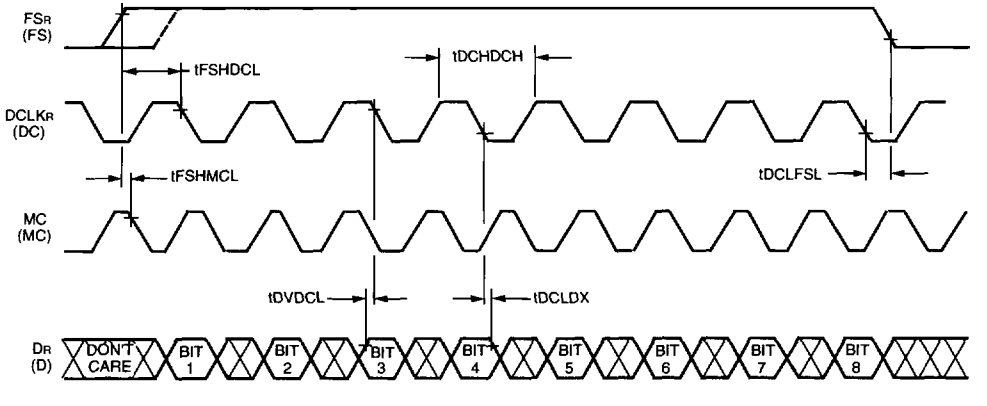
Timing Characteristics (continued)



Notes:
All timing parameters referenced to V_{IH} and V_{IL}, except tFSHDV and tFSLDX, which reference a high-impedance state.

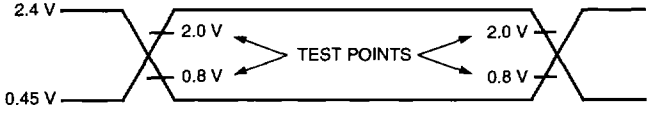
Bit 1 = sign bit.

Figure 10. Variable-Data-Rate Transmit Timing



Note: Bit 1 = sign bit.

Figure 11. Variable-Data-Rate Receive Timing



Notes:
ac testing inputs are driven at 2.4 V for a logic of 1 and 0.45 V for a logic 0.

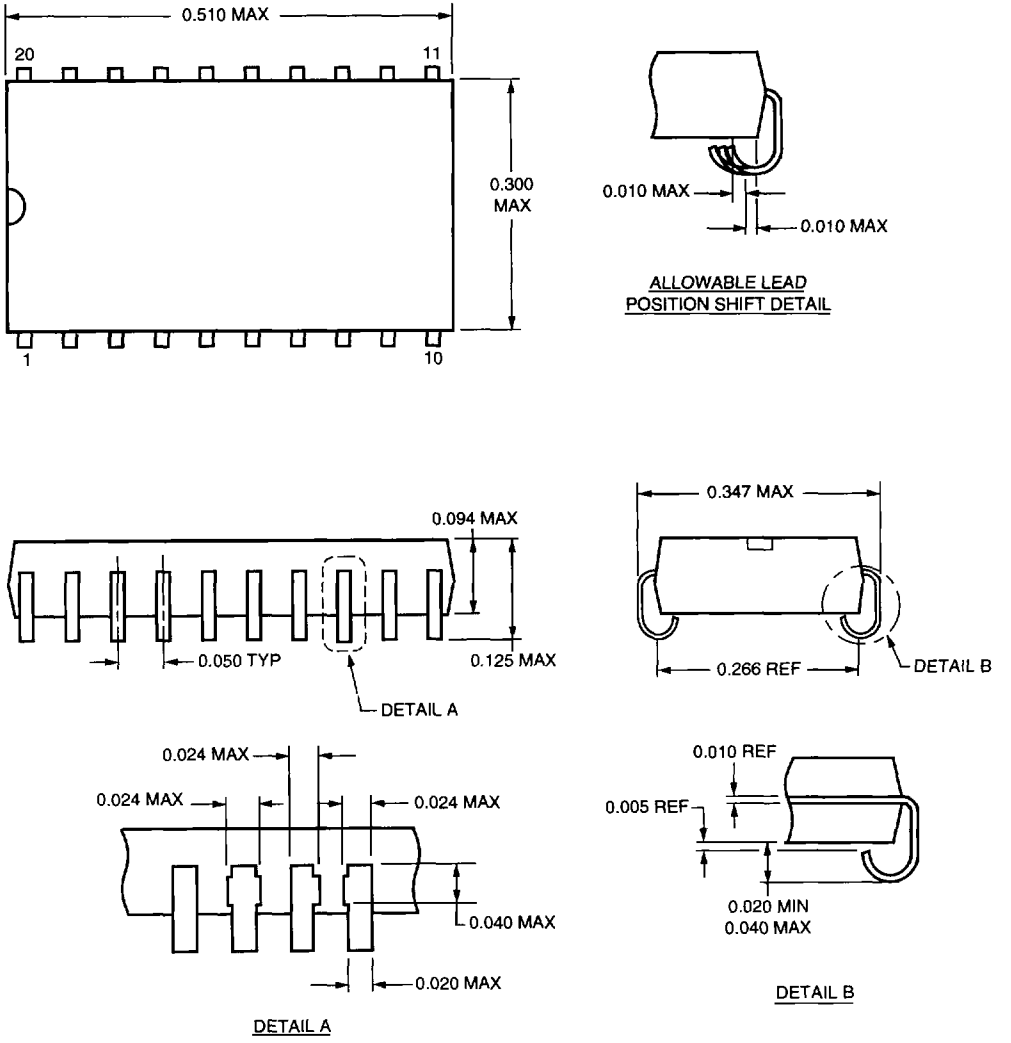
Timing measurements are made at 2.0 V for a logic 1 and 0.8 V for a logic 0.

Figure 12. ac Testing Input/Output Waveform

Outline Diagrams

20-Pin SOJ

Dimensions are shown in inches.



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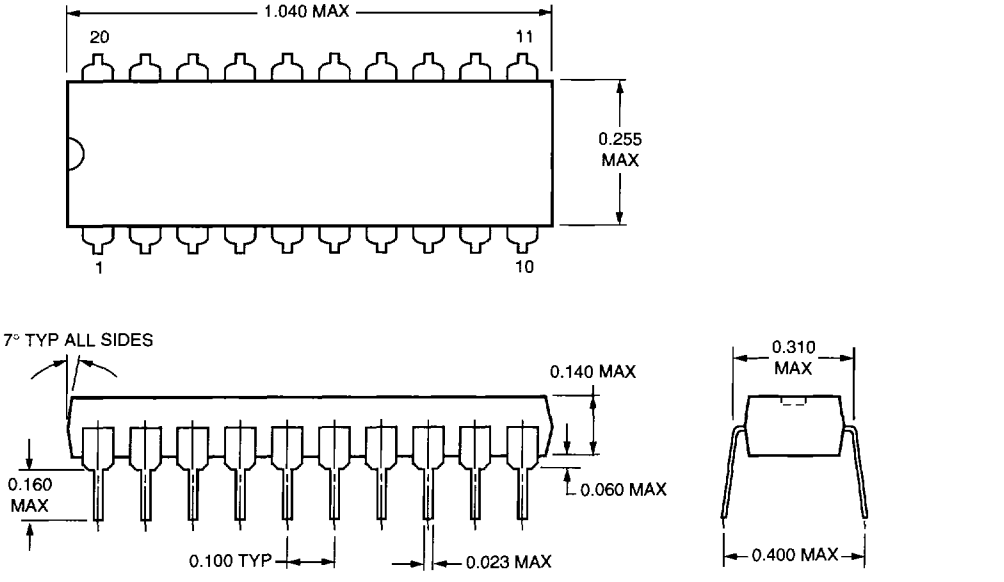
Outline Diagrams (continued)

20-Pin DIP

Dimensions are shown in inches.



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