

# 2.25Mb ZBT™ SRAM

MT55L128L18F, MT55L64L32F,  
MT55L64L36F

3.3V V<sub>DD</sub>, Selectable Burst Mode

## FEATURES

- High frequency and 100 percent bus utilization
- Fast cycle times: 10ns, 10.5ns, 11ns and 12ns
- Single +3.3V  $\pm 5\%$  power supply
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs eliminate the need to control OE#
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or Interleaved Burst Modes
- Burst feature (optional)
- Pin/function compatibility with 4.5Mb, 9Mb and 18Mb ZBT SRAM family
- Automatic power-down

## OPTIONS

- Timing (Cycle/Access)
  - 10ns (100 MHz)/7.5ns
  - 10.5ns (95 MHz)/8ns
  - 11ns (90 MHz)/8.5ns
  - 12ns (83 MHz)/9ns
- Configurations
  - 128K x 18
  - 64K x 32
  - 64K x 36
- Package
  - 100-pin TQFP
- Options
  - Standard version
  - Low-power version

## MARKING

	-10
	-10.5
	-11
	-12
MT55L128L18F	
MT55L64L32F	
MT55L64L36F	

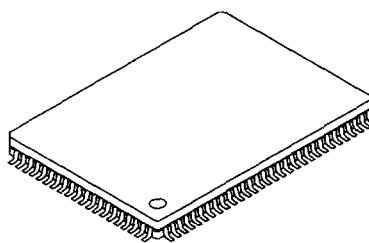
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None  
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## VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT55L128L18FT-x	128K x 18, Flow-Through, LVTTTL
MT55L64L32FT-x	64K x 32, Flow-Through, LVTTTL
MT55L64L36FT-x	64K x 36, Flow-Through, LVTTTL

100-Pin TQFP\*  
(SA-1)



\*JEDEC-standard MS-026 BHA (LQFP).

## GENERAL DESCRIPTION

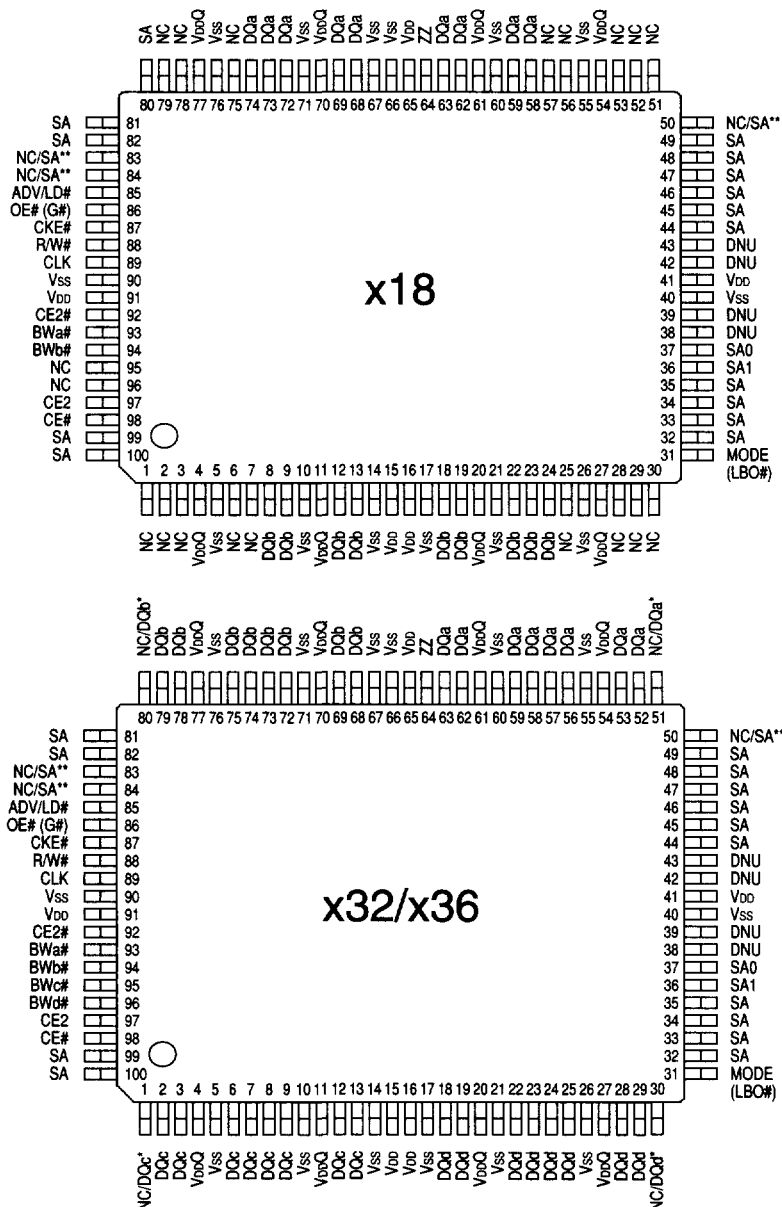
The Micron Zero Bus Turnaround™ (ZBT™) SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

The MT55L128L18F, MT55L64L32F and MT55L64L36F SRAMs integrate a 128K x 18, 64K x 32 or 64K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles when transitioning from READ to WRITE, or vice versa. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc# and BWD#) and read/write (R/W#).

Asynchronous inputs include the output enable (OE#, which may be tied LOW for control signal minimization), clock (CLK) and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW or left unconnected if burst is unused. The flow-through data-out (Q) is enabled by OE#. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

All READ, WRITE and DESELECT cycles are initiated by the ADV/LD# input. Subsequent burst addresses can be

PIN ASSIGNMENT (Top View)  
100-Pin TQFP  
(SA-1)



\* NC for x32 version, DQx for x36 version.

\*\* Pins 50, 83 and 84 are reserved for address expansion.

## GENERAL DESCRIPTION (continued)

internally generated as controlled by the burst advance pin (ADV/LD#). Use of burst mode is optional. It is allowable to give an address for each individual READ and WRITE cycle. BURST cycles wrap around after the fourth access from a base address.

To allow for continuous, 100 percent use of the data bus, the flow-through ZBT SRAM uses a LATE WRITE cycle. For example, if a WRITE cycle begins in clock cycle one, the address is present on rising edge one. BYTE WRITES need to be asserted on the same cycle as the address. The write data associated with the address is required one cycle later, or on the rising edge of clock cycle two.

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles.

Individual byte enables allow individual bytes to be written. During a BYTE WRITE cycle, BWA# controls DQa pins; BWb# controls DQb pins; BWC# controls DQc pins; and BWD# controls DQd pins. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD# is LOW. Parity/ECC bits are only available on the x18 and x36 versions.

The SRAM operates from a +3.3V power supply, and all inputs and outputs are LVTTTL-compatible. The device is ideally suited for systems requiring high bandwidth and zero bus turnaround delays.

Please refer to the Micron Web site ([www.micron.com./mti/msp/html/sramprod.html](http://www.micron.com./mti/msp/html/sramprod.html)) for the latest data sheet revisions.

## PIN ASSIGNMENT TABLE

PIN #	x18	x32	x36
1	NC	NC	DQc
2	NC	DQc	DQc
3	NC	DQc	DQc
4		VDDQ	
5		VSS	
6	NC	DQc	DQc
7	NC	DQc	DQc
8	DQb	DQc	DQc
9	DQb	DQc	DQc
10		VSS	
11		VDDQ	
12	DQb	DQc	DQc
13	DQb	DQc	DQc
14		VSS	
15		VDD	
16		VDD	
17		VSS	
18	DQb	DQd	DQd
19	DQb	DQd	DQd
20		VDDQ	
21		VSS	
22	DQb	DQd	DQd
23	DQb	DQd	DQd
24	DQb	DQd	DQd
25	NC	DQd	DQd

PIN #	x18	x32	x36
26		VSS	
27		VDDQ	
28	NC	DQd	DQd
29	NC	DQd	DQd
30	NC	NC	DQd
31		MODE (LBO#)	
32		SA	
33		SA	
34		SA	
35		SA	
36		SA1	
37		SA0	
38		DNU	
39		DNU	
40		VSS	
41		VDD	
42		DNU	
43		DNU	
44		SA	
45		SA	
46		SA	
47		SA	
48		SA	
49		SA	
50		NC/SA*	

PIN #	x18	x32	x36
51	NC	NC	DQa
52	NC	DQa	DQa
53	NC	DQa	DQa
54		VDDQ	
55		VSS	
56	NC	DQa	DQa
57	NC	DQa	DQa
58		DQa	
59		DQa	
60		VSS	
61		VDDQ	
62		DQa	
63		DQa	
64		ZZ	
65		VDD	
66		VSS	
67		VSS	
68	DQa	DQb	DQb
69	DQa	DQb	DQb
70		VDDQ	
71		VSS	
72	DQa	DQb	DQb
73	DQa	DQb	DQb
74	DQa	DQb	DQb
75	NC	DQb	DQb

PIN #	x18	x32	x36
76		VSS	
77		VDDQ	
78	NC	DQb	DQb
79	NC	DQb	DQb
80	SA	NC	DQb
81		SA	
82		SA	
83		NC/SA*	
84		NC/SA*	
85		ADV/LD#	
86		OE# (G#)	
87		CKE#	
88		R/W#	
89		CLK	
90		VSS	
91		VDD	
92		CE2#	
93		BWA#	
94		BWB#	
95	NC	BWC#	BWC#
96	NC	BWD#	BWD#
97		CE2	
98		CE#	
99		SA	
100		SA	

\* Pins 50, 83 and 84 are reserved for address expansion.

The block diagram illustrates the internal architecture of the 128Kx9x2 SRAM. Key components and their interconnections are as follows:

- Inputs:** SA0, SA1, SA (17-bit address bus), MODE, ADV/LD#, CLK, CKE#, BWa#, BWb#, R/W#, OE#, CE#, CE2#, and CE2#.
- Internal Registers and Logic:**
  - ADDRESS REGISTER:** Receives the 17-bit address (SA0, SA1, SA) and outputs a 15-bit address to the BURST LOGIC.
  - WRITE ADDRESS REGISTER:** Receives the 17-bit address (SA1, SA0) and outputs a 17-bit address to the BURST LOGIC.
  - BURST LOGIC:** Receives the 15-bit address from the ADDRESS REGISTER and the 17-bit address from the WRITE ADDRESS REGISTER. It outputs a 17-bit address to the WRITE REGISTRY AND DATA COHERENCY CONTROL LOGIC.
  - WRITE REGISTRY AND DATA COHERENCY CONTROL LOGIC:** Receives the 17-bit address from the BURST LOGIC and the 17-bit address from the WRITE ADDRESS REGISTER. It outputs a 17-bit address to the WRITE DRIVERS.
  - WRITE DRIVERS:** Receives the 17-bit address from the WRITE REGISTRY AND DATA COHERENCY CONTROL LOGIC and outputs a 17-bit address to the MEMORY ARRAY.
  - MEMORY ARRAY:** Receives the 17-bit address from the WRITE DRIVERS and outputs a 17-bit address to the SENSE AMPS.
  - SENSE AMPS:** Receives the 17-bit address from the MEMORY ARRAY and outputs a 17-bit address to the DATA STEERING.
  - DATA STEERING:** Receives the 17-bit address from the SENSE AMPS and outputs a 17-bit address to the OUTPUT BUFFERS.
  - OUTPUT BUFFERS:** Receives the 17-bit address from the DATA STEERING and outputs a 17-bit address to the INPUT REGISTER.
  - INPUT REGISTER:** Receives the 17-bit address from the OUTPUT BUFFERS and outputs a 17-bit address to the BURST LOGIC.
- Outputs:** DQs (Data Bus).

128K x 18, 64K x 32/36 LVTTTL, Flow-Through ZBT SRAM  
MT55L128L18F.pm6 – Rev. 2/96

## PIN DESCRIPTIONS

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 44-49, 80-82, 99, 100	37 36 32-35, 44-49, 81, 82, 99, 100	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Pins 50, 83 and 84 are reserved as address bits for the higher-density 4.5Mb, 9Mb and 18Mb ZBT SRAMs, respectively. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
93 94 — —	93 94 95 96	BWa# BWb# BWc# BWD#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITES need to be asserted on the same cycle as the address. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWD# controls DQd pins.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW).
92	92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# LOW). This input can be used for memory depth expansion.
86	86	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
85	85	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
87	87	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE# is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.

## PIN DESCRIPTIONS (continued)

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
88	88	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
38, 39, 42, 43	38, 39, 42, 43	DNU	—	Do Not Use: These signals may either be unconnected or wired to GND to minimize thermal impedance.
(a) 58, 59, 62, 63, 68, 69, 72-74 (b) 8, 9, 12, 13, 18, 19, 22-24	(a) 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
N/A	51 80 1 30	NC/DQa NC/DQb NC/DQc NC/DQd	NC/ I/O	No Connect/Data Bits: On the x32 version, these pins are no connect (NC) and can be left floating or connected to GND to minimize thermal impedance. On the x36 version, these bits are DQs.
31	31	MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
1-3, 6, 7, 25, 28-30, 51-53, 56, 57, 75, 78, 79, 95, 96	N/A	NC	NC	No Connect: These pins can be left floating or connected to GND to minimize thermal impedance.
50, 83, 84	50, 83, 84	NC/SA	NC	No Connect: NC pins 50, 83 and 84 are reserved for address bits for the 4.5Mb, 9Mb and 18Mb ZBT SRAMs, respectively. These pins can be left floating or connected to GND to minimize thermal impedance.
15, 16, 41, 65, 91	15, 16, 41, 65, 91	V <sub>DD</sub>	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	V <sub>DDQ</sub>	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90	5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90	V <sub>SS</sub>	Supply	Ground: GND.

## INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

## LINEAR BURST ADDRESS TABLE (MODE = LOW)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

## PARTIAL TRUTH TABLE FOR READ/WRITE COMMANDS (x18)

FUNCTION	R/W#	BWa#	BWb#
READ	H	X	X
WRITE Byte "a"	L	L	H
WRITE Byte "b"	L	H	L
WRITE All Bytes	L	L	L
WRITE ABORT/NOP	L	H	H

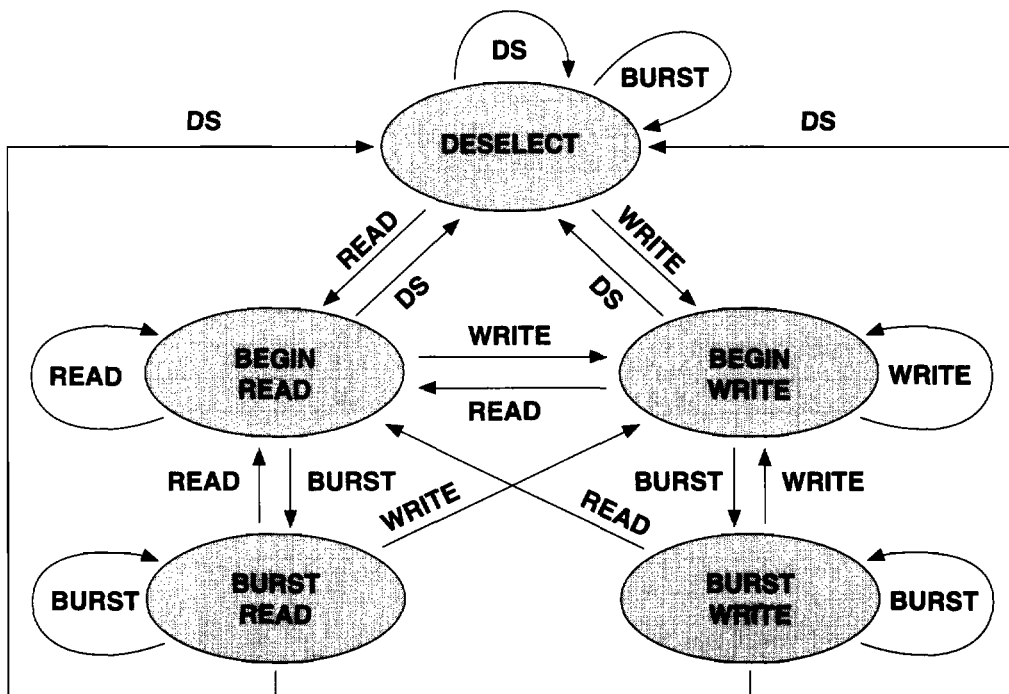
**NOTE:** Using R/W# and byte write(s), any one or more bytes may be written.

## PARTIAL TRUTH TABLE FOR READ/WRITE COMMANDS (x32/x36)

FUNCTION	R/W#	BWa#	BWb#	BWc#	BWd#
READ	H	X	X	X	X
WRITE Byte "a"	L	L	H	H	H
WRITE Byte "b"	L	H	L	H	H
WRITE Byte "c"	L	H	H	L	H
WRITE Byte "d"	L	H	H	H	L
WRITE All Bytes	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

**NOTE:** Using R/W# and byte write(s), any one or more bytes may be written.

## STATE DIAGRAM FOR ZBT SRAM



## KEY:

COMMAND	ACTION
DS	Deselect
READ	New READ
WRITE	New WRITE
BURST	BURST READ, BURST WRITE or CONTINUE DESELECT

- NOTE:**
1. A STALL or IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE# HIGH only blocks the clock (CLK) input and does not change the state of the device.
  2. States change on the rising edge of the clock (CLK).



## TRUTH TABLE

(Notes 5-10)

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ZZ	ADV/LD#	R/W#	BWx	OE#	CKE#	CLK	DQ	NOTES
DESELECT CYCLE	None	H	X	X	L	L	X	X	X	L	L→H	High-Z	
DESELECT CYCLE	None	X	H	X	L	L	X	X	X	L	L→H	High-Z	
DESELECT CYCLE	None	X	X	L	L	L	X	X	X	L	L→H	High-Z	
CONTINUE DESELECT CYCLE	None	X	X	X	L	H	X	X	X	L	L→H	High-Z	1
READ CYCLE (Begin Burst)	External	L	L	H	L	L	H	X	L	L	L→H	Q	
READ CYCLE (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L→H	Q	1, 11
NOP/DUMMY READ (Begin Burst)	External	L	L	H	L	L	H	X	H	L	L→H	High-Z	2
DUMMY READ (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L→H	High-Z	1, 2, 11
WRITE CYCLE (Begin Burst)	External	L	L	H	L	L	L	L	X	L	L→H	D	3
WRITE CYCLE (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L→H	D	1, 3, 11
NOP/WRITE ABORT (Begin Burst)	None	L	L	H	L	L	L	H	X	L	L→H	High-Z	2, 3
WRITE ABORT (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L→H	High-Z	1, 2, 3, 11
IGNORE CLOCK EDGE (Stall)	Current	X	X	X	L	X	X	X	X	H	L→H	-	4
SNOOZE MODE	None	X	X	X	H	X	X	X	X	X	X	High-Z	

- NOTE:**
1. CONTINUE BURST cycles, whether READ or WRITE, use the same control inputs. The type of cycle performed (READ or WRITE) is chosen in the initial BEGIN BURST cycle. A CONTINUE DESELECT cycle can only be entered if a DESELECT cycle is executed first.
  2. DUMMY READ and WRITE ABORT cycles can be considered NOPs because the device performs no external operation. A WRITE ABORT means a WRITE command is given, but no operation is performed.
  3. OE# may be wired LOW to minimize the number of control signals to the SRAM. The device will automatically turn off the output drivers during a WRITE cycle. Some users may use OE# when the bus turn-on and turn-off times do not meet their requirements.
  4. If an IGNORE CLOCK EDGE command occurs during a READ operation, the DQ bus will remain active (Low-Z). If it occurs during a WRITE cycle, the bus will remain in High-Z. No WRITE operations will be performed during the IGNORE CLOCK EDGE cycle.
  5. X means "Don't Care." H means logic HIGH. L means logic LOW. BWx = H means all byte write signals (BWA#, BWb#, BWc# and BWD#) are HIGH. BWx = L means one or more byte write signals are LOW.
  6. BWA# enables WRITES to Byte "a" (DQa pins); BWb# enables WRITES to Byte "b" (DQb pins); BWc# enables WRITES to Byte "c" (DQc pins); BWD# enables WRITES to Byte "d" (DQd pins).
  7. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
  8. Wait states are inserted by setting CKE# HIGH.
  9. This device contains circuitry that will ensure that the outputs will be in High-Z during power-up.
  10. The device incorporates a 2-bit burst counter. Address wraps to the initial address every fourth BURST cycle.
  11. The address counter is incremented for all CONTINUE BURST cycles.

MICRON

128K x 18, 64K x 32/36  
LVTTTL, FLOW-THROUGH ZBT SRAM

NEW

ZBT SRAM

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on V<sub>DD</sub> Supply Relative to V<sub>SS</sub> ..... -0.5V to +4.6V  
 Voltage on V<sub>DDQ</sub> Supply Relative to V<sub>SS</sub> ..... -0.5V to V<sub>DD</sub>  
 V<sub>IN</sub> ..... -0.5V to V<sub>DD</sub> + 0.5V  
 Storage Temperature (plastic) ..... -55°C to +150°C  
 Junction Temperature\*\* ..... +150°C  
 Short Circuit Output Current ..... 100mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

\*\*Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See Micron Technical Note TN-05-14 for more information.

**DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS**

(0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>DD</sub>, V<sub>DDQ</sub> = +3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V <sub>IH</sub>	2.0	V <sub>DD</sub> + 0.3	V	1, 2
Input High (Logic 1) Voltage	DQ pins	V <sub>IH</sub>	2.0	V <sub>DD</sub> + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V <sub>IL</sub>	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	I <sub>LI</sub>	-1.0	1.0	μA	3
Output Leakage Current	Output(s) disabled, 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	I <sub>LO</sub>	-1.0	1.0	μA	
Output High Voltage	I <sub>OH</sub> = -4.0mA	V <sub>OH</sub>	2.4		V	1, 4
Output Low Voltage	I <sub>OL</sub> = 8.0mA	V <sub>OL</sub>		0.4	V	1, 4
Supply Voltage		V <sub>DD</sub>	3.135	3.465	V	1
Isolated Output Buffer Supply		V <sub>DDQ</sub>	3.135	V <sub>DD</sub>	V	1, 5

**CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	T <sub>A</sub> = 25°C; f = 1 MHz V <sub>DD</sub> = 3.3V	C <sub>I</sub>	3	4	pF	6
Input/Output Capacitance (DQ)		C <sub>O</sub>	4	5	pF	6
Address Capacitance		C <sub>A</sub>	3	3.5	pF	6

- NOTE:**
1. All voltages referenced to V<sub>SS</sub> (GND).
  2. Overshoot: V<sub>IH</sub> ≤ +4.6V for t ≤ <sup>1</sup>/<sub>2</sub> KHKH/2 for I ≤ 20mA  
 Undershoot: V<sub>IL</sub> ≥ -0.7V for t ≤ <sup>1</sup>/<sub>2</sub> KHKH/2 for I ≤ 20mA  
 Power-up: V<sub>IH</sub> ≤ +3.465V and V<sub>DD</sub> ≤ 3.135V for t ≤ 200ms
  3. MODE pin has an internal pull-up, and input leakage = ±10μA.
  4. The load used for V<sub>OH</sub>, V<sub>OL</sub> testing is shown in Figure 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
  5. V<sub>DDQ</sub> should never exceed V<sub>DD</sub>. V<sub>DD</sub> and V<sub>DDQ</sub> can be externally wired together to the same power supply.
  6. This parameter is sampled.

## IDD OPERATING CONDITIONS AND MAXIMUM LIMITS

DESCRIPTION	CONDITIONS	SYM	TYP	MAX				UNITS	NOTES
				-10	-10.5	-11	-12		
Power Supply Current: Operating	Device selected; All inputs $\leq V_{IL}$ or $\geq V_{IH}$ ; Cycle time $\geq 1\text{KC (MIN)}$ ; $V_{DD} = \text{MAX}$ ; Outputs open	I <sub>DD</sub>	TBD	300	300	275	250	mA	1, 2, 3
Power Supply Current: Idle	Device selected; $V_{DD} = \text{MAX}$ ; $\text{CKE}\# \geq V_{IH}$ ; All inputs $\leq V_{SS} + 0.2$ or $\geq V_{DD} - 0.2$ ; Cycle time $\geq 1\text{KC (MIN)}$	I <sub>DD1</sub>	TBD	12	12	11	10	mA	1, 2, 3
CMOS Standby	Device deselected; $V_{DD} = \text{MAX}$ ; All inputs $\leq V_{SS} + 0.2$ or $\geq V_{DD} - 0.2$ ; All inputs static; CLK frequency = 0	I <sub>SB2</sub>	TBD	10	10	10	10	mA	2, 3
CMOS Standby (P Version)	Device deselected; $V_{DD} = \text{MAX}$ ; All inputs $\leq V_{SS} + 0.2$ or $\geq V_{DD} - 0.2$ ; All inputs static; CLK frequency = 0	I <sub>SB2P</sub>	TBD	1	1	1	1	mA	2, 3, 4
TTL Standby	Device deselected; $V_{DD} = \text{MAX}$ ; All inputs $\leq V_{IL}$ or $\geq V_{IH}$ ; All inputs static; CLK frequency = 0	I <sub>SB3</sub>	TBD	25	25	25	25	mA	2, 3
Clock Running	Device deselected; $V_{DD} = \text{MAX}$ ; All inputs $\leq V_{SS} + 0.2$ or $\geq V_{DD} - 0.2$ ; Cycle time $\geq 1\text{KC (MIN)}$	I <sub>SB4</sub>	TBD	65	65	65	60	mA	2, 3
Snooze Mode	ZZ $V_{IH}$	I <sub>SB2Z</sub>	TBD	10	10	10	10	mA	3
Snooze Mode (P Version)	ZZ $V_{IH}$	I <sub>SB2ZP</sub>	TBD	1	1	1	1	mA	4

## THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TQFP TYP	UNITS	NOTES
Thermal Resistance (Junction to Ambient)	Still air, soldered on 4.25 x 1.125 inch, 4-layer printed circuit board	$\theta_{JA}$	28	°C/W	5
Thermal Resistance (Junction to Case)		$\theta_{JC}$	4	°C/W	5

- NOTE:**
1. I<sub>DD</sub> is specified with no output current and increases with faster cycle times. I<sub>DDQ</sub> increases with faster cycle times and greater output loading.
  2. "Device deselected" means device is in a deselected cycle as defined in the truth table. "Device selected" means device is active (not in deselected mode).
  3. Typical values are measured at 3.3V, 25°C and 12ns cycle time.
  4. Consult factory for availability of low-power version of this device.
  5. This parameter is sampled.

## AC ELECTRICAL CHARACTERISTICS

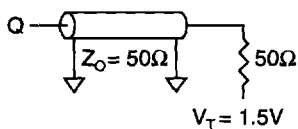
(Notes 5, 7, 8) ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{DD}, V_{DDQ} = +3.3\text{V} \pm 5\%$ )

DESCRIPTION	SYMBOL	-10		-10.5		-11		-12		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock											
Clock cycle time	<sup>1</sup> KHKH	10		10.5		11		12		ns	
Clock frequency	<sup>1</sup> KF		100		95		90		83	MHz	
Clock HIGH time	<sup>1</sup> KHKL	3.0		3.0		3.5		4.0		ns	
Clock LOW time	<sup>1</sup> KLKH	3.0		3.0		3.5		4.0		ns	
Output Times											
Clock to output valid	<sup>1</sup> KHQV		7.5		8.0		8.5		9.0	ns	
Clock to output invalid	<sup>1</sup> KHQX	3.0		3.0		3.0		3.0		ns	1
Clock to output in Low-Z	<sup>1</sup> KHQX1	4.0		4.0		4.0		4.0		ns	1, 2, 3, 4
Clock to output in High-Z	<sup>1</sup> KHQZ		5.0		5.0		5.0		5.0	ns	1, 2, 3, 4
OE# to output valid	<sup>1</sup> GLQV		5.0		5.0		5.0		5.0	ns	5
OE# to output in Low-Z	<sup>1</sup> GLQX	0		0		0		0		ns	1, 2, 3, 4
OE# to output in High-Z	<sup>1</sup> GHQZ		5.0		5.0		5.0		5.0	ns	1, 2, 3, 4
Setup Times											
Address	<sup>1</sup> AVKH	2.0		2.0		2.2		2.5		ns	6
Clock enable (CKE#)	<sup>1</sup> EVKH	2.0		2.0		2.2		2.5		ns	6
Control signals	<sup>1</sup> CVKH	2.0		2.0		2.2		2.5		ns	6
Data-in	<sup>1</sup> DVKH	2.0		2.0		2.2		2.5		ns	6
Hold Times											
Address	<sup>1</sup> KHAX	0.5		0.5		0.5		0.5		ns	6
Clock enable (CKE#)	<sup>1</sup> KHEX	0.5		0.5		0.5		0.5		ns	6
Control signals	<sup>1</sup> KHCX	0.5		0.5		0.5		0.5		ns	6
Data-in	<sup>1</sup> KHDX	0.5		0.5		0.5		0.5		ns	6

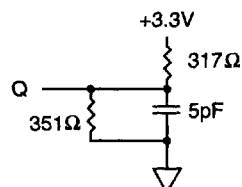
- NOTE:**
1. Refer to Technical Note TN-55-01, "Designing with ZBT SRAMs," for a more thorough discussion on these parameters.
  2. This parameter is sampled.
  3. Output loading is specified with  $C_L = 5\text{pF}$  as in Figure 2.
  4. Transition is measured  $\pm 200\text{mV}$  from steady state voltage.
  5. OE# can be considered a "Don't Care" during WRITES; however, controlling OE# can help fine-tune a system for turnaround timing.
  6. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when they are being registered into the device. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when ADV/LD# is LOW to remain enabled.
  7. Test conditions as specified with the output loading as shown in Figure 1 unless otherwise noted.
  8. A WRITE cycle is defined by R/W# LOW having been registered into the device at ADV/LD# LOW. A READ cycle is defined by R/W# HIGH with ADV/LD# LOW. Both cases must meet setup and hold times.

## AC TEST CONDITIONS

Input pulse levels .....	V <sub>ss</sub> to 3.0V
Input rise and fall times .....	1.0ns
Input timing reference levels .....	1.5V
Output reference levels .....	1.5V
Output load .....	See Figures 1 and 2



**Figure 1**  
**OUTPUT LOAD EQUIVALENT**



**Figure 2**  
**OUTPUT LOAD EQUIVALENT**

**SNOOZE MODE**

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to  $I_{SB2Z}$ . The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become disabled and all outputs go to High-Z.

The ZZ pin is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ

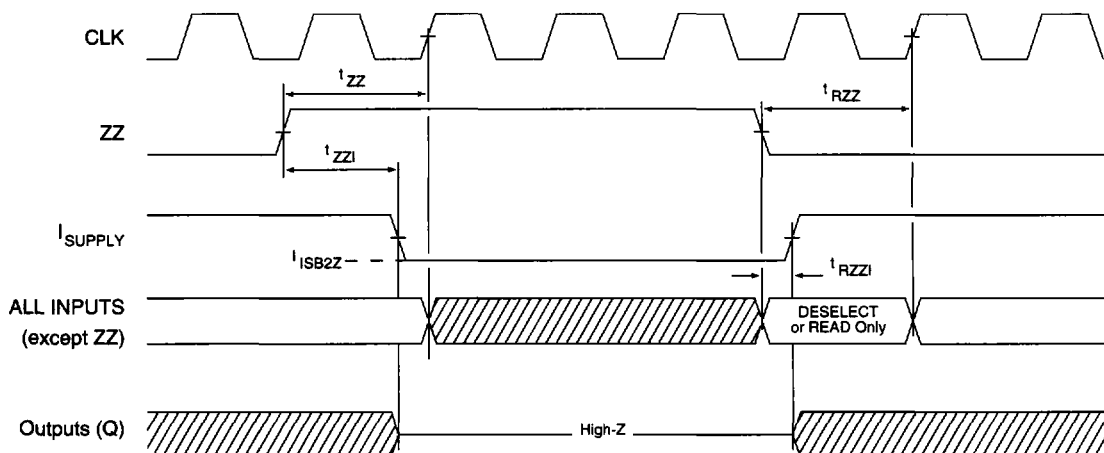
pin becomes a logic HIGH,  $I_{SB2Z}$  is guaranteed after the time  $t_{ZZI}$  is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during  $t_{RZZ}$ , only a DESELECT or READ cycle should be given.

**SNOOZE MODE ELECTRICAL CHARACTERISTICS**

( $V_{DD}$ ,  $V_{DDQ} = +3.3V \pm 5\%$ )

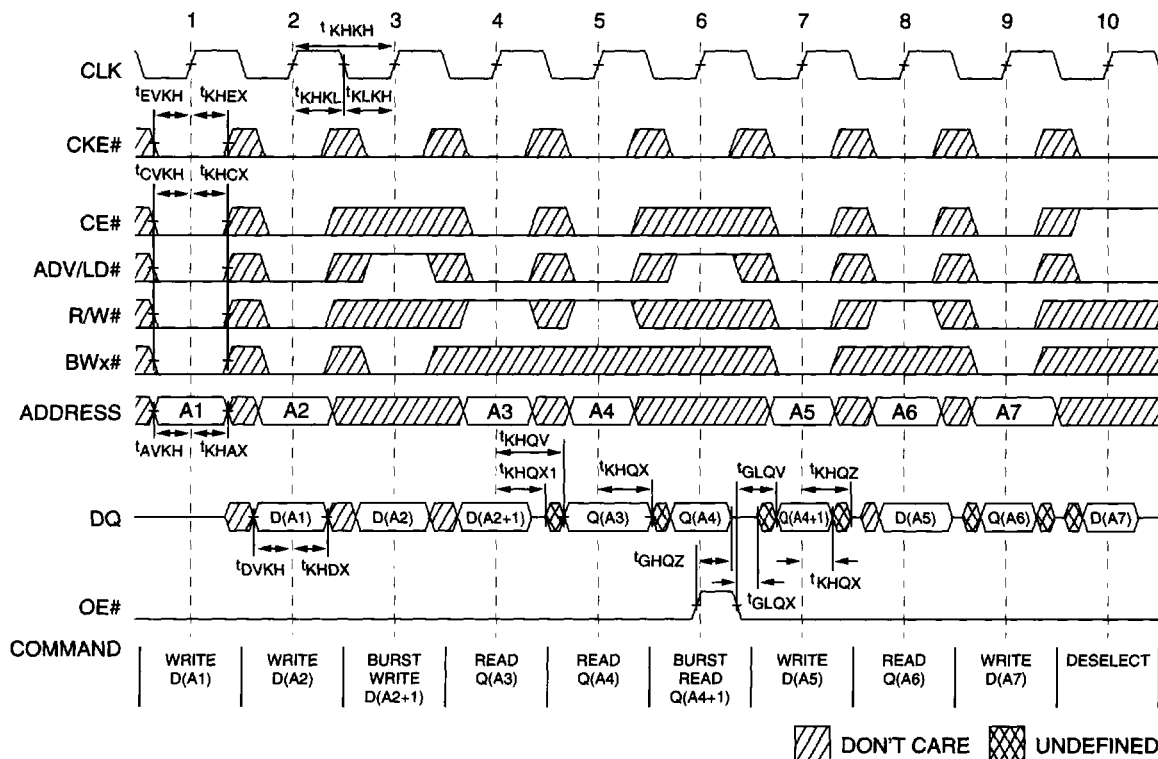
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	$I_{SB2Z}$		10	mA	
Current during SNOOZE MODE (P Version)	$ZZ \geq V_{IH}$	$I_{SB2ZP}$		1	mA	
ZZ active to input ignored		$t_{ZZ}$	0	$t_{KHKH}$	ns	1
ZZ inactive to input sampled		$t_{RZZ}$	0	$t_{KHKH}$	ns	1
ZZ active to snooze current		$t_{ZZI}$		$t_{KHKH}$	ns	1
ZZ inactive to exit snooze current		$t_{RZZI}$	0		ns	1

**NOTE:** 1. This parameter is sampled.

**SNOOZE MODE WAVEFORM**

DON'T CARE

### READ/WRITE TIMING



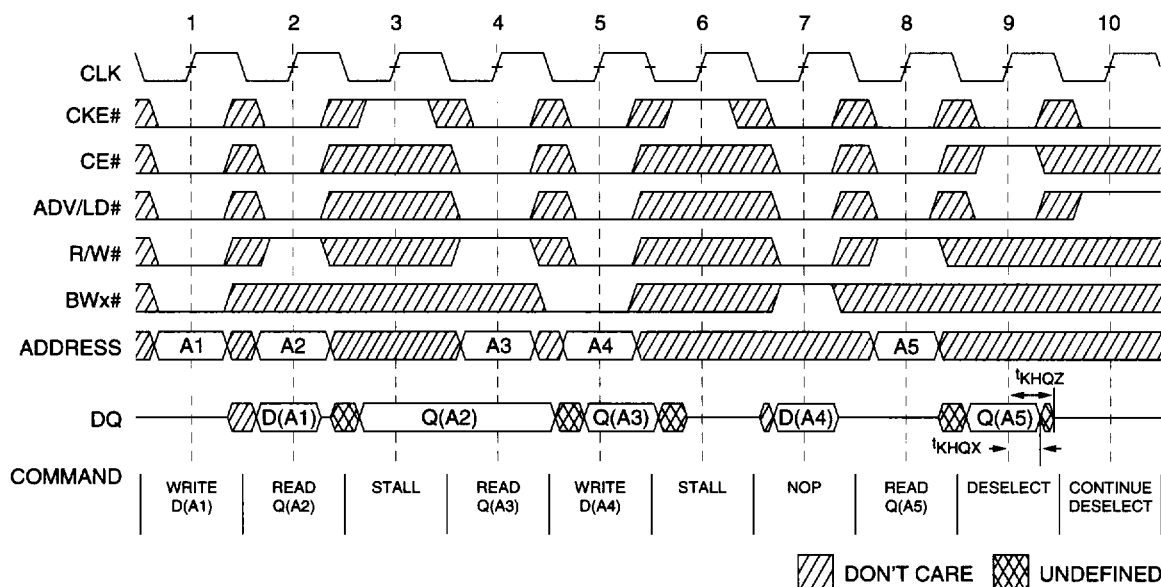
### READ/WRITE TIMING PARAMETERS

SYMBOL	-10		-10.5		-11		-12		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{KHKH}$	10		10.5		11		12		ns
$t_{KF}$		100		95		90		83	MHz
$t_{KHKL}$	3.0		3.0		3.5		4.0		ns
$t_{KLKH}$	3.0		3.0		3.5		4.0		ns
$t_{KHQV}$		7.5		8.0		8.5		9.0	ns
$t_{KHQX}$	3.0		3.0		3.0		3.0		ns
$t_{KHQX1}$	4.0		4.0		4.0		4.0		ns
$t_{KHQZ}$		5.0		5.0		5.0		5.0	ns
$t_{GLQV}$		5.0		5.0		5.0		5.0	ns
$t_{GLQX}$	0		0		0		0		ns

SYMBOL	-10		-10.5		-11		-12		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{GHQZ}$		5.0		5.0		5.0		5.0	ns
$t_{AVKH}$	2.0		2.0		2.2		2.5		ns
$t_{EVKH}$	2.0		2.0		2.2		2.5		ns
$t_{CVKH}$	2.0		2.0		2.2		2.5		ns
$t_{DVKH}$	2.0		2.0		2.2		2.5		ns
$t_{KHAX}$	0.5		0.5		0.5		0.5		ns
$t_{KHEX}$	0.5		0.5		0.5		0.5		ns
$t_{KHCX}$	0.5		0.5		0.5		0.5		ns
$t_{KHDX}$	0.5		0.5		0.5		0.5		ns

- NOTE:**
- For this waveform, ZZ is tied LOW.
  - Burst sequence order is determined by MODE (0 = linear, 1 = interleaved). BURST operations are optional.
  - CE# represents three signals. When CE# = 0, it represents CE# = 0, CE2# = 0, CE2 = 1.
  - Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

## NOP, STALL AND DESELECT CYCLES



## NOP, STALL AND DESELECT TIMING PARAMETERS

SYMBOL	-10		-10.5		-11		-12		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{KHQX}$	3.0		3.0		3.0		3.0		ns
$t_{KHQZ}$		5.0		5.0		5.0		5.0	ns

**NOTE:**

1. The IGNORE CLOCK EDGE or STALL cycle (clock 3) illustrates CKE# being used to create a "pause." A WRITE is not performed during this cycle.
2. For this waveform, ZZ and OE# are tied LOW.
3. CE# represents three signals. When CE# = 0, it represents CE# = 0, CE2# = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.