# WIDE DRAM

# 512K x 8 DRAM

## LOW POWER, EXTENDED REFRESH

## FEATURES

- Industry-standard x8 pinouts, timing, functions and packages
- Address entry: ten row-addresses, nine column-addresses
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply*
- All device pins are TTL-compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST-PAGE-MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C8513 only)
- 1,024-cycle refresh distributed accross 128ms
- Low-power, 1mW standby; 350mW active, typical

## OPTIONS

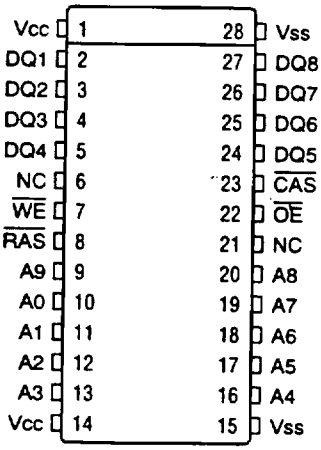
| | MARKING |
|---|---|
| • Timing | |
| 60ns access | -6* |
| 70ns access | -7 |
| 80ns access | -8 |
| • MASKED WRITE | |
| Not available | 8512 L |
| Available | 8513 L |
| • Packages | |
| Plastic SOJ (400 mil) | DJ |
| Plastic TSOP (400 mil) | TG |
| Plastic ZIP (375 mil) | Z |

- Part Number Example: MT4C8512DJ-7 L

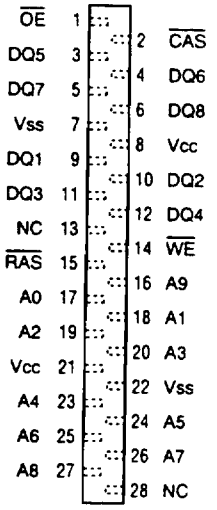
*60ns specifications are limited to a Vcc range of ±5%.

## PIN ASSIGNMENT (Top View)

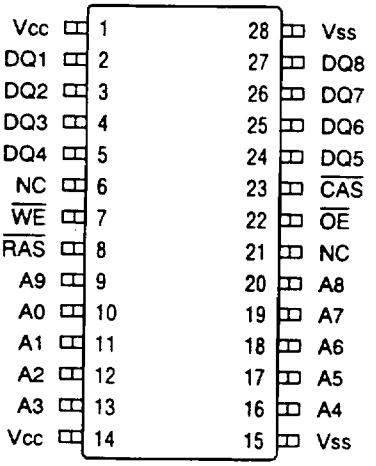
### 28-Pin SOJ (SDB-1)




### 28-Pin ZIP (SDA-1)




### 28-Pin TSOP (SDE-1)

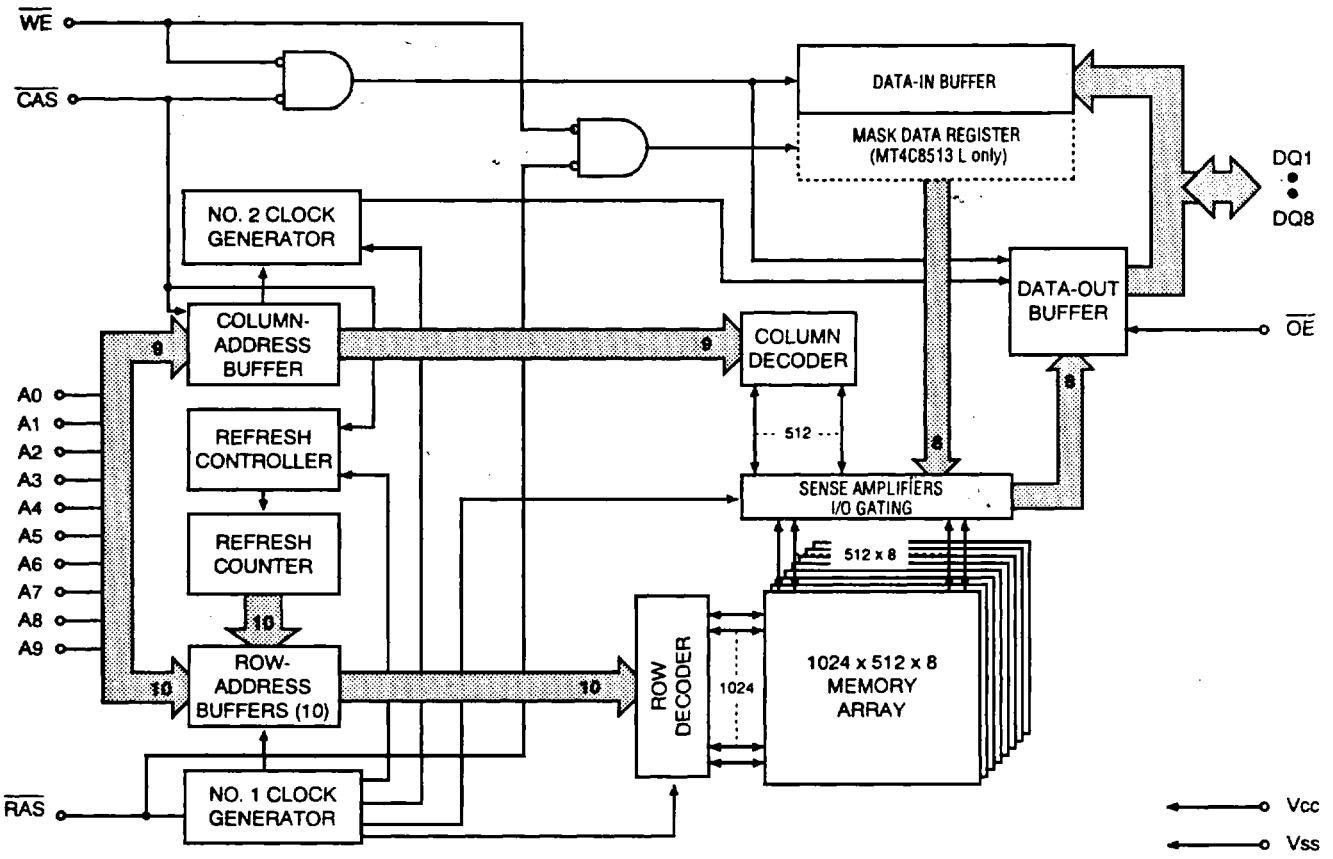



## GENERAL DESCRIPTION

The MT4C8512/3 L are randomly accessed solid-state memories containing 4,194,304 bits organized in a x8 configuration. Each byte is uniquely addressed through the 19 address bits during READ or WRITE cycles. The address is entered first by $\overline{RAS}$ latching 10 bits (A0-A9) and then $\overline{CAS}$ latching 9 bits (A0-A8).

The MT4C8513 L has NONPERSISTENT MASKED WRITE allowing it to perform WRITE-PER-BIT accesses.

## FUNCTIONAL BLOCK DIAGRAM



## PIN DESCRIPTIONS

| SOJ/TSOP PIN NUMBERS | ZIP PIN NUMBERS | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|---|
| 8 | 15 | $\overline{RAS}$ | Input | Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 10 row-address bits and strobe the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C8513 L only). |
| 23 | 2 | $\overline{CAS}$ | Input | Column-address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. |
| 7 | 14 | $\overline{WE}$ | Input | Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a mask enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED WRITE cycle (MT4C8513 L). |
| 22 | 1 | $\overline{OE}$ | Input | Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state. |
| 10-13, 16-20, 9 | 17, 18, 19, 20, 23, 24, 25, 26, 27, 16 | A0-A9 | Input | Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 512K available words. |
| 2-5, 24-27 | 9, 10, 11, 12, 3, 4, 5, 6 | DQ1-DQ8 | Input | Data I/O: Includes inputs, outputs or High-Z and/or output masked data input (for MASKED WRITE cycle only). |
| 6, 21 | 13, 28 | NC | - | No Connect: These pins should be either left unconnected or tied to ground. |
| 1, 14 | 8, 21 | Vcc | Supply | Power Supply: +5V ±10%* |
| 15, 28 | 7, 22 | Vss | Supply | Ground |

*60ns specifications are limited to a Vcc range of ±5%.

## FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 19 address bits during READ or WRITE cycles. First $\overline{RAS}$ is used to latch 10 bits (A0-A9) then, $\overline{CAS}$ latches 9 bits ( A0-A8).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BBU MODE is a CBR REFRESH performed at the extended refresh rate with CMOS input levels. This mode provides a very low-current, data-retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

## MASKED WRITE ACCESS CYCLE (MT4C8513 L ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In NONPERSISTENT MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C8513 L MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

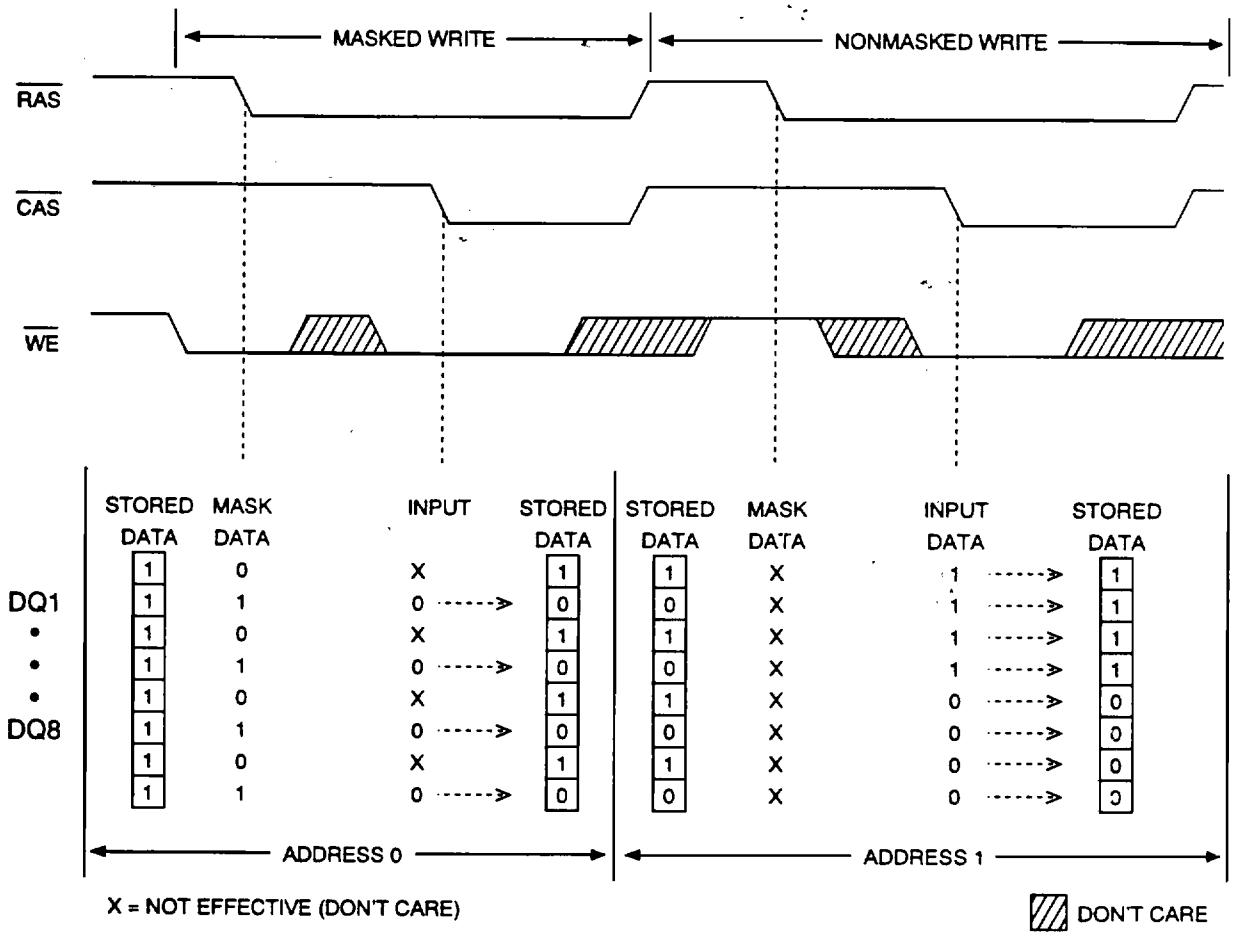



**Figure 1**
**MT4C8513 L MASKED WRITE EXAMPLE**

## TRUTH TABLE

| FUNCTION | | RAS | CAS | WE | OE | ADDRESSES $^tR$ | ADDRESSES $^tC$ | DQs | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| Standby | | H | H→X | X | X | X | X | High-Z | |
| READ | | L | L | H | L | ROW | COL | Data-Out | |
| EARLY-WRITE | | L | L | L | X | ROW | COL | Data-In | 1 |
| READ-WRITE | | L | L | H→L | L→H | ROW | COL | Data-Out, Data-In | 1 |
| FAST-PAGE- | 1st Cycle | L | H→L | H | L | ROW | COL | Data-Out | |
| MODE READ | 2nd Cycle | L | H→L | H | L | n/a | COL | Data-Out | |
| FAST-PAGE- | 1st Cycle | L | H→L | L | X | ROW | COL | Data-In | 1 |
| MODE WRITE | 2nd Cycle | L | H→L | L | X | n/a | COL | Data-In | 1 |
| FAST-PAGE-MODE | 1st Cycle | L | H→L | H→L | L→H | ROW | COL | Data-Out, Data-In | 1 |
| READ-WRITE | 2nd Cycle | L | H→L | H→L | L→H | n/a | COL | Data-Out, Data-In | 1 |
| HIDDEN | READ | L→H→L | L | H | L | ROW | COL | Data-Out | |
| REFRESH | WRITE | L→H→L | L | L | X | ROW | COL | Data-In | 1, 2 |
| RAS-ONLY REFRESH | | L | H | X | X | ROW | n/a | High-Z | |
| CBR REFRESH | | H→L | L | X | X | X | X | High-Z | |
| BBU REFRESH | | H→L | L | X | X | X | X | High-Z | |

**NOTE:** 1. Data-in will be dependent on the mask provided (MT4C8513 L only). Refer to Figure 1.
2. EARLY-WRITE only.

## ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss ..... -1V to +7V
Operating Temperature, $T_A$ (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation ..... 1W
Short Circuit Output Current ..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ $T_A$ ≤ 70°C; Vcc = 5V ±10%**)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Supply Voltage | Vcc | 4.5 | 5.5 | V | 1 |
| Input High (Logic 1) Voltage, all inputs | VIH | 2.4 | Vcc+1 | V | 1 |
| Input Low (Logic 0) Voltage, all inputs | VIL | -1.0 | 0.8 | V | 1 |
| INPUT LEAKAGE CURRENT<br>Any input 0V ≤ VIN ≤ Vcc<br>(All other pins not under test = 0V) | II | -2 | 2 | µA | |
| OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) | IOZ | -10 | 10 | µA | |
| OUTPUT LEVELS<br>Output High Voltage (IOUT = -5mA) | VOH | 2.4 | | V | |
| Output Low Voltage (IOUT = 4.2mA) | VOL | | 0.4 | V | |

| | | MAX | | | | |
|---|---|---|---|---|---|---|
| PARAMETER/CONDITION | SYMBOL | -6** | -7 | -8 | UNITS | NOTES |
| STANDBY CURRENT: TTL<br>($\overline{RAS}$ = $\overline{CAS}$ = VIH) | ICC1 | 2 | 2 | 2 | mA | |
| STANDBY CURRENT: CMOS<br>($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V) | ICC2 | 200 | 200 | 200 | µA | 25 |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC$ = $^tRC$ [MIN]) | ICC3 | 120 | 110 | 100 | mA | 3, 4, 31 |
| OPERATING CURRENT: FAST-PAGE-MODE<br>Average power supply current<br>($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: $^tPC$ = $^tPC$ [MIN]; $^tCP$, $^tASC$ = 10ns) | ICC4 | 100 | 90 | 80 | mA | 3, 4, 31 |
| REFRESH CURRENT: $\overline{RAS}$-ONLY<br>Average power supply current<br>($\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH: $^tRC$ = $^tRC$ [MIN]) | ICC5 | 120 | 110 | 100 | mA | 3, 31 |
| REFRESH CURRENT: CBR<br>Average power supply current<br>($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC$ = $^tRC$ [MIN]) | ICC6 | 110 | 100 | 90 | mA | 3 |
| REFRESH CURRENT: BBU<br>Average power supply current during BBU REFRESH:<br>$\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = $^tRAS$ (MIN) to 300ns; $\overline{WE}$, A0-A9 and DIN = Vcc - 0.2V (DIN may be left open), $^tRC$ = 125µs (1,024 rows at 125µs = 128ms) | ICC7 | 300 | 300 | 300 | µA | 3, 5, 30 |

**60ns specifications are limited to a Vcc range of ±5%.

## CAPACITANCE

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance: A0-A9 | $C_{I1}$ | 5 | pF | 2 |
| Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ | $C_{I2}$ | 7 | pF | 2 |
| Input/Output Capacitance: DQ (SOJ, TSOP) | $C_{IO}$ | 7 | pF | 2 |
| Input/Output Capacitance: DQ (ZIP) | $C_{IO}$ | 9 | pF | 2 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ $T_A$ ≤ +70°C; Vcc = 5V ±10%*)

| AC CHARACTERISTICS | | -6* | | -7 | | -8 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Random READ or WRITE cycle time | $t_{RC}$ | 110 | | 130 | | 150 | | ns | |
| READ-WRITE cycle time | $t_{RWC}$ | 150 | | 175 | | 195 | | ns | |
| FAST-PAGE-MODE READ or WRITE cycle time | $t_{PC}$ | 35 | | 40 | | 45 | | ns | |
| FAST-PAGE-MODE READ-WRITE cycle time | $t_{PRWC}$ | 85 | | 95 | | 100 | | ns | |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | | 60 | | 70 | | 80 | ns | 14 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | | 15 | | 20 | | 20 | ns | 15 |
| Output Enable time | $t_{OE}$ | | 15 | | 20 | | 20 | ns | |
| Access time from column-address | $t_{AA}$ | | 30 | | 35 | | 40 | ns | |
| Access time from $\overline{CAS}$ precharge | $t_{CPA}$ | | 35 | | 40 | | 45 | ns | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 60 | 100,000 | 70 | 100,000 | 80 | 100,000 | ns | |
| $\overline{RAS}$ pulse width (FAST-PAGE-MODE) | $t_{RASP}$ | 60 | 100,000 | 70 | 100,000 | 80 | 100,000 | ns | |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 15 | | 20 | | 20 | | ns | |
| $\overline{RAS}$ precharge time | $t_{RP}$ | 40 | | 50 | | 60 | | ns | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 15 | 100,000 | 20 | 100,000 | 20 | 100,000 | ns | |
| $\overline{CAS}$ hold time | $t_{CSH}$ | 60 | | 70 | | 80 | | ns | |
| $\overline{CAS}$ precharge time | $t_{CPN}$ | 10 | | 10 | | 10 | | ns | 16 |
| $\overline{CAS}$ precharge time (FAST-PAGE-MODE) | $t_{CP}$ | 10 | | 10 | | 10 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | 20 | 45 | 20 | 50 | 20 | 60 | ns | 17 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | 10 | | 10 | | 10 | | ns | |
| Row-address setup time | $t_{ASR}$ | 0 | | 0 | | 0 | | ns | |
| Row-address hold time | $t_{RAH}$ | 10 | | 10 | | 10 | | ns | |
| $\overline{RAS}$ to column-address delay time | $t_{RAD}$ | 15 | 30 | 15 | 35 | 15 | 40 | ns | 18 |
| Column-address setup time | $t_{ASC}$ | 0 | | 0 | | 0 | | ns | |
| Column-address hold time | $t_{CAH}$ | 10 | | 15 | | 15 | | ns | |
| Column-address hold time (referenced to $\overline{RAS}$) | $t_{AR}$ | 50 | | 55 | | 60 | | ns | |
| Column-address to $\overline{RAS}$ lead time | $t_{RAL}$ | 30 | | 35 | | 40 | | ns | |
| Read command setup time | $t_{RCS}$ | 0 | | 0 | | 0 | | ns | 26 |
| Read command hold time (referenced to $\overline{CAS}$) | $t_{RCH}$ | 0 | | 0 | | 0 | | ns | 19, 26 |

*60ns specifications are limited to a Vcc range of ±5%.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ $T_A$ ≤ +70°C; Vcc = 5V ±10%*)

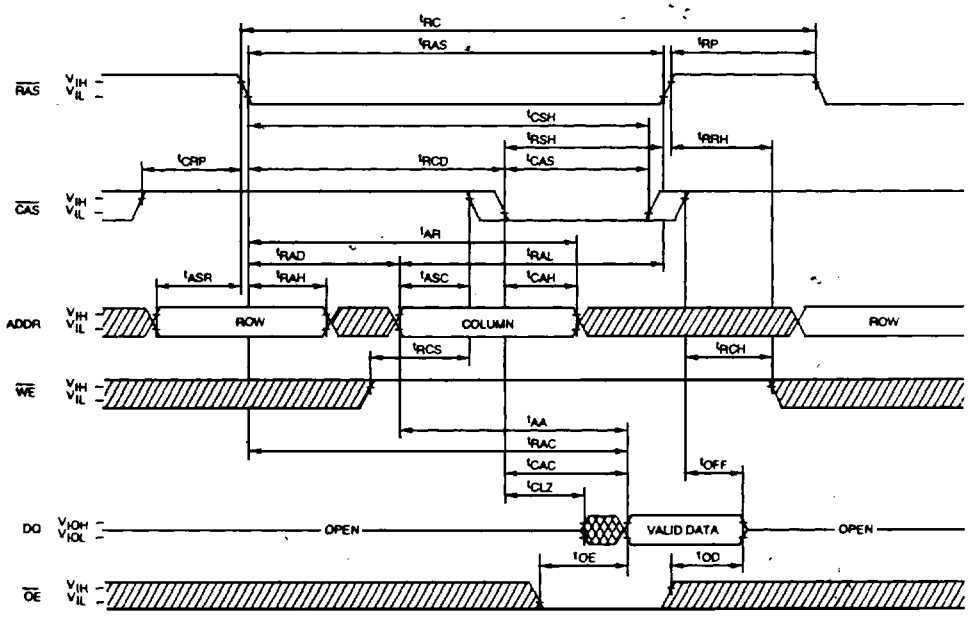
| AC CHARACTERISTICS | | -6* | | -7 | | -8 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Read command hold time (referenced to $\overline{RAS}$) | tRRH | 0 | | 0 | | 0 | | ns | 19 |
| $\overline{CAS}$ to output in Low-Z | tCLZ | 3 | | 3 | | 3 | | ns | 32 |
| Output buffer turn-off delay | tOFF | 3 | 15 | 3 | 15 | 3 | 15 | ns | 20, 29, 32 |
| Output disable time | tOD | 3 | 15 | 3 | 15 | 3 | 15 | ns | 29, 32 |
| Write command setup time | tWCS | 0 | | 0 | | 0 | | ns | 21, 26 |
| Write command hold time | tWCH | 10 | | 10 | | 10 | | ns | 26 |
| Write command hold time (referenced to $\overline{RAS}$) | tWCR | 45 | | 55 | | 60 | | ns | 26 |
| Write command pulse width | tWP | 10 | | 10 | | 10 | | ns | 26 |
| Write command to $\overline{RAS}$ lead time | tRWL | 15 | | 20 | | 20 | | ns | 26 |
| Write command to $\overline{CAS}$ lead time | tCWL | 15 | | 20 | | 20 | | ns | 26 |
| Data-in setup time | tDS | 0 | | 0 | | 0 | | ns | 22 |
| Data-in hold time | tDH | 10 | | 15 | | 15 | | ns | 22 |
| Data-in hold time (referenced to $\overline{RAS}$) | tDHR | 45 | | 55 | | 60 | | ns | |
| $\overline{RAS}$ to $\overline{WE}$ delay time | tRWD | 85 | | 95 | | 105 | | ns | 21 |
| Column-address to $\overline{WE}$ delay time | tAWD | 55 | | 60 | | 65 | | ns | 21 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | tCWD | 40 | | 45 | | 45 | | ns | 21 |
| Transition time (rise or fall) | tT | 3 | 50 | 3 | 50 | 3 | 50 | ns | 9, 10 |
| Refresh period (1,024 cycles) | tREF | | 16 | | 128 | | 128 | ms | |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | tRPC | 10 | | 10 | | 10 | | ns | |
| $\overline{CAS}$ setup time (CBR REFRESH) | tCSR | 10 | | 10 | | 10 | | ns | 5 |
| $\overline{CAS}$ hold time (CBR REFRESH) | tCHR | 10 | | 10 | | 10 | | ns | 5 |
| MASKED WRITE command to $\overline{RAS}$ setup time | tWRS | 0 | | 0 | | 0 | | ns | 26 |
| $\overline{WE}$ hold time to $\overline{RAS}$ (MASKED WRITE) | tWRH | 10 | | 15 | | 15 | | ns | 26 |
| MASKED Data to $\overline{RAS}$ setup time | tMS | 0 | | 0 | | 0 | | ns | 26, 27 |
| MASKED Data to $\overline{RAS}$ hold time | tMH | 15 | | 15 | | 15 | | ns | 26, 27 |
| $\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle | tOEH | 15 | | 20 | | 20 | | ns | 28 |
| $\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle | tORD | 0 | | 0 | | 0 | | ns | |

*60ns specifications are limited to a Vcc range of ±5%.

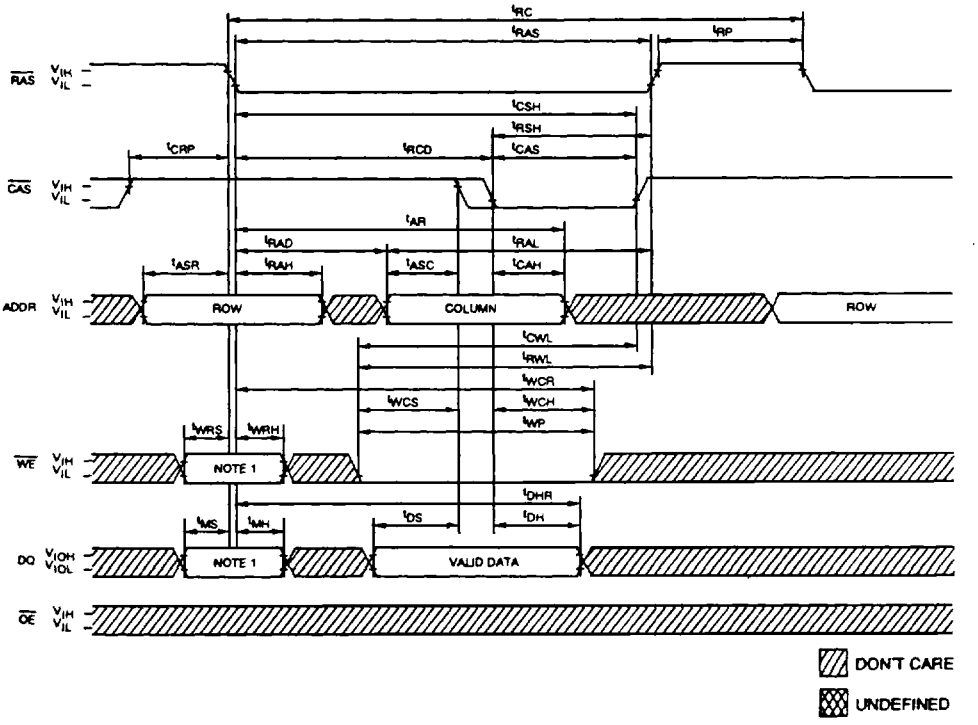
## NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = 5V ±10%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the $^tREF$ refresh requirement is exceeded.
8. AC characteristics assume $^tT$ = 5ns.
9. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$).
10. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
11. If $\overline{CAS}$ = $V_{IH}$, data output is high impedance.
12. If $\overline{CAS}$ = $V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, $V_{OH}$ = 2.0V and $V_{OL}$ = 0.8V.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If $^tRCD$ is greater than the maximum recommended value shown in this table, $^tRAC$ will increase by the amount that $^tRCD$ exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for $^tCPN$.
17. Operation within the $^tRCD$ (MAX) limit ensures that $^tRAC$ (MAX) can be met. $^tRCD$ (MAX) is specified as a reference point only; if $^tRCD$ is greater than the specified $^tRCD$ (MAX) limit, access time is controlled exclusively by $^tCAC$.
18. Operation within the $^tRAD$ limit ensures that $^tRCD$ (MAX) can be met. $^tRAD$ (MAX) is specified as a reference point only; if $^tRAD$ is greater than the specified $^tRAD$ (MAX) limit, access time is controlled exclusively by $^tAA$.
19. Either $^tRCH$ or $^tRRH$ must be satisfied for a READ cycle.
20. $^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to $V_{OH}$ or $V_{OL}$.
21. $^tWCS$, $^tRWD$, $^tAWD$ and $^tCWD$ are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C8513 L only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both $^tOD$ and $^tOEH$ met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after $^tOEH$ is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once $^tOD$ or $^tOFF$ occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
30. BBU current is reduced as $^tRAS$ is reduced from its maximum specification during BBU cycle.
31. Column-address changed once while $\overline{RAS}$ = $V_{IL}$ and $\overline{CAS}$ = $V_{IH}$.
32. The 3ns minimum is a parameter guaranteed by design.

## READ CYCLE

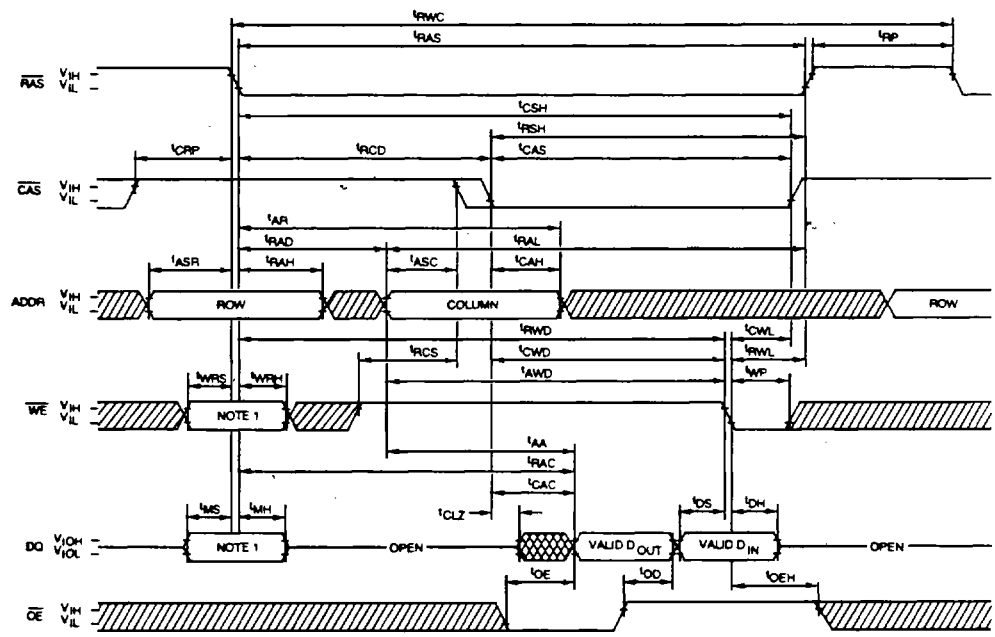



## EARLY-WRITE CYCLE

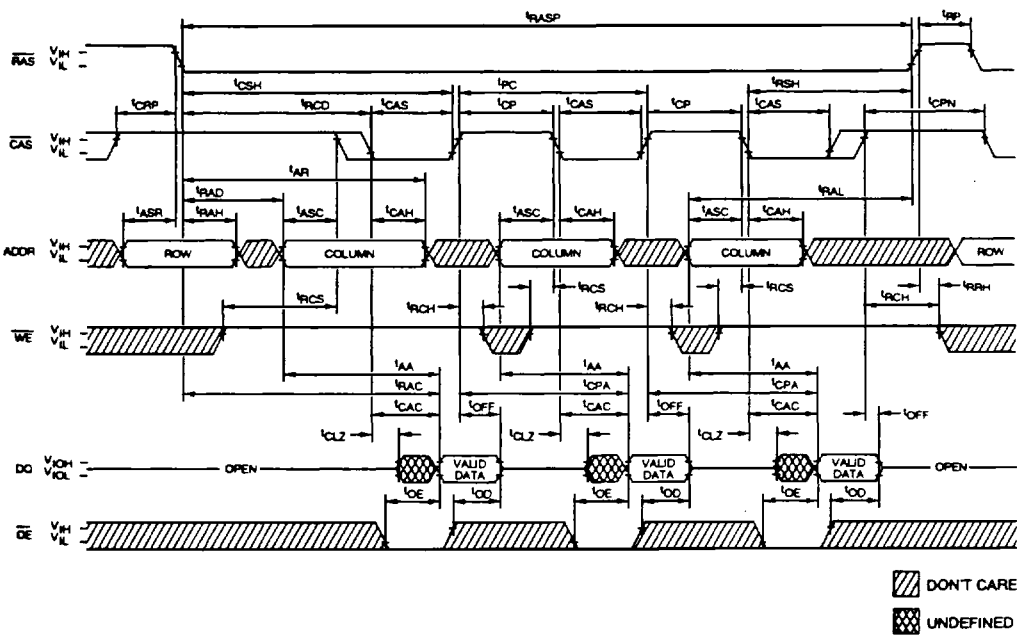



**NOTE:** 1. Applies to MT4C8513 L only; $\overline{WE}$ and DQ inputs on MT4C8512 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

## READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

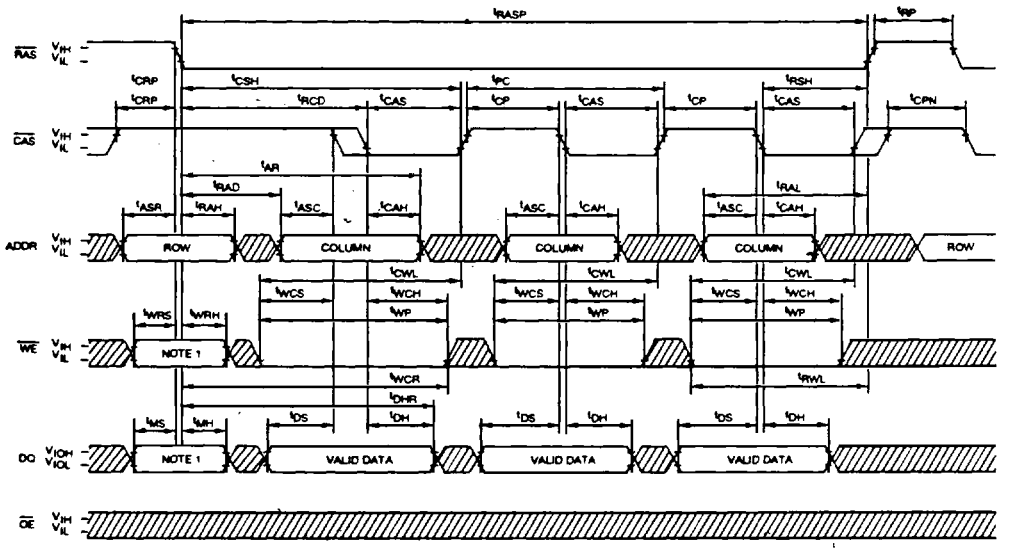



## FAST-PAGE-MODE READ CYCLE

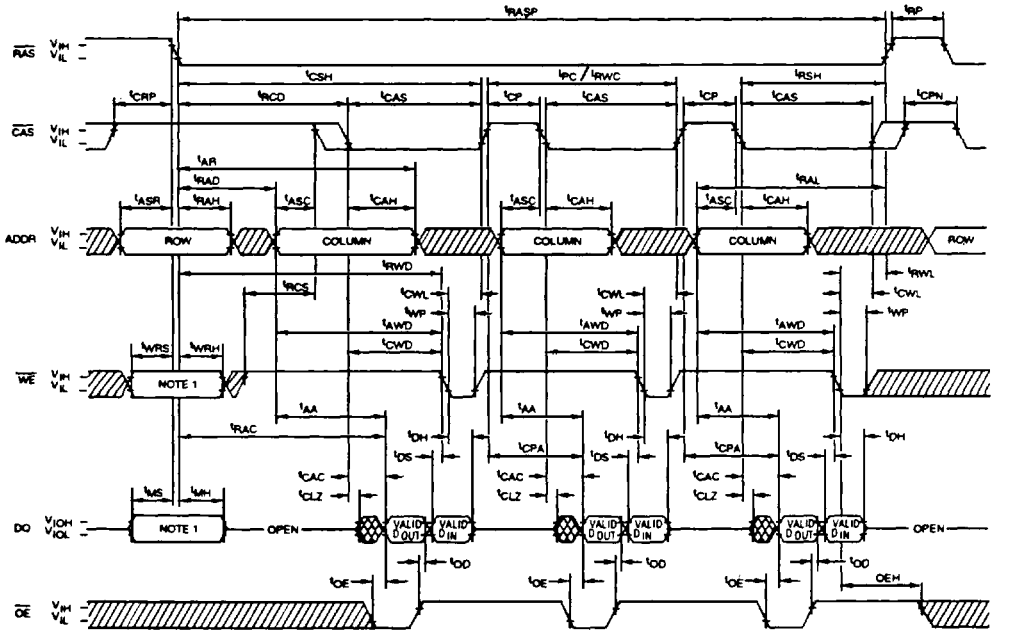



**NOTE:** 1. Applies to MT4C8513 L only; $\overline{WE}$ and DQ inputs on MT4C8512 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

## FAST-PAGE-MODE EARLY-WRITE CYCLE

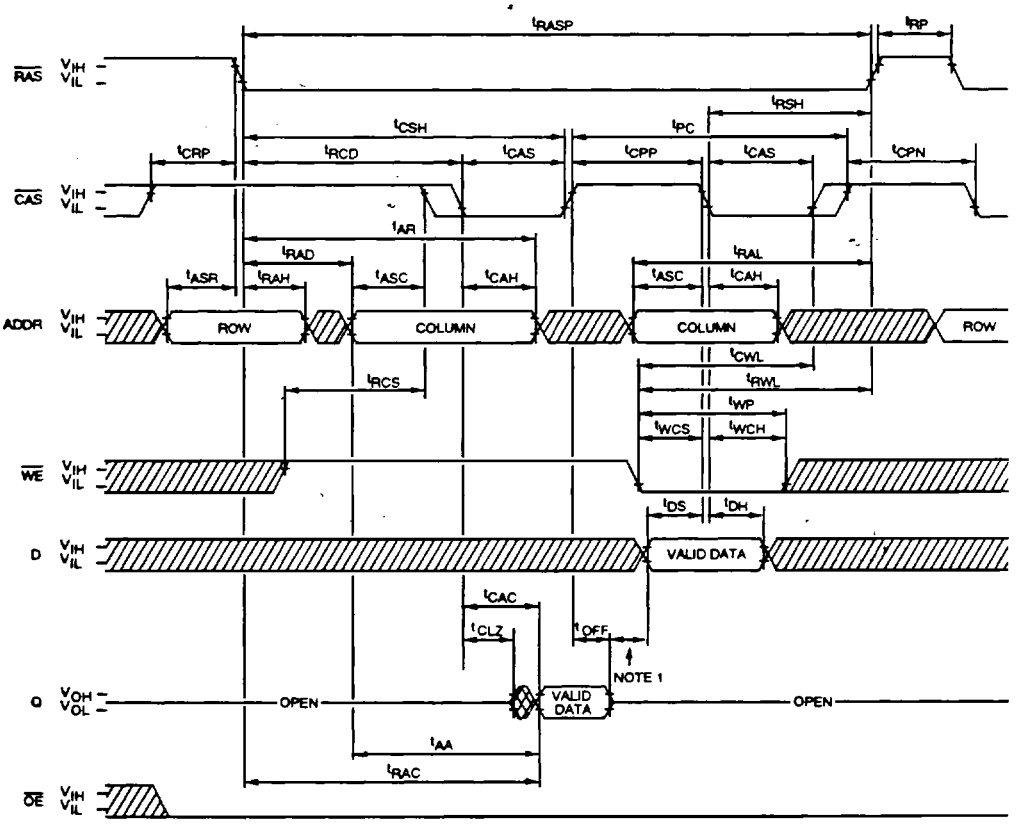



## FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



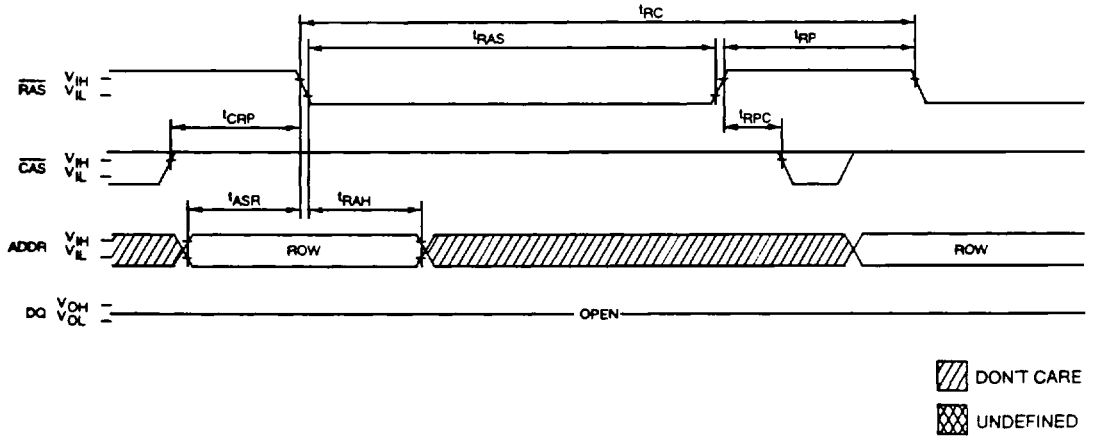

**NOTE:** 1. Applies to MT4C8513 L only; $\overline{WE}$ and DQ inputs on MT4C8512 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

## FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

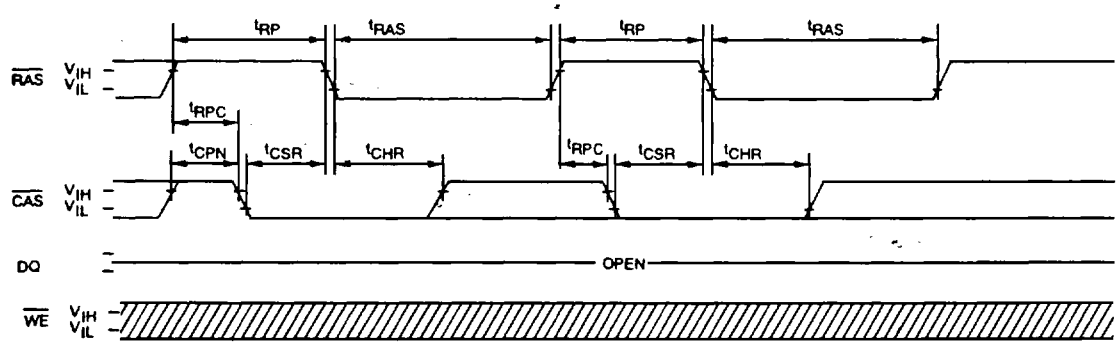



**NOTE:** 1. Do not drive data prior to High-Z; that is completion of tOFF. tCPP is equal to tOFF + tDS(MIN) + guardband between data-out and driving new data-in.

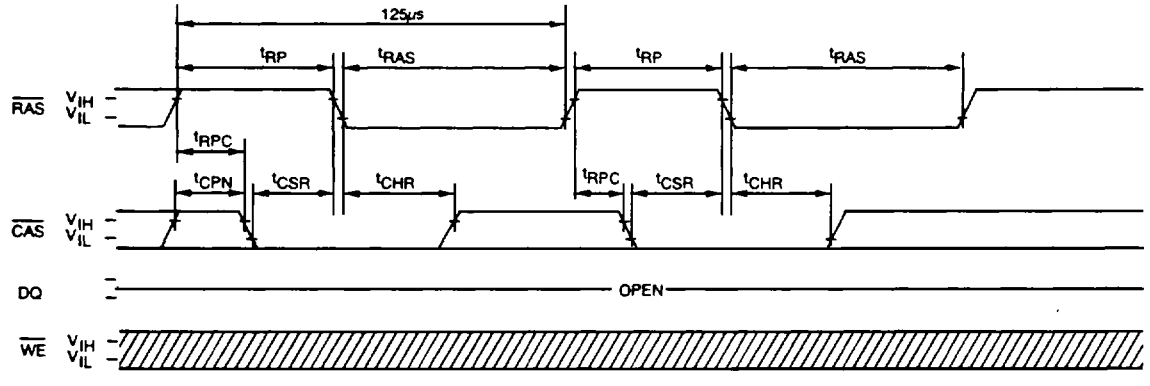
## RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



## CBR REFRESH CYCLE
(A0-A9; $\overline{OE}$ = DON'T CARE)




## BBU REFRESH CYCLE
(A0-A9; $\overline{OE}$ = DON'T CARE)




DON'T CARE

UNDEFINED

## HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)