

Revision History

Revision .2 (Mar. 1998)

- Some Parameters values & Characteristics of comp. level are changed as below :
 - Input leakage currents (Inputs) : $\pm 5\mu\text{A}$ to $\pm 1\mu\text{A}$.
 - Input leakage currents (I/O) : $\pm 5\mu\text{A}$ to $\pm 1\mu\text{A}$.
 - C_{in} to be measured at $V_{DD} = 3.3\text{V}$, $T_A = 23^\circ\text{C}$, $f = 1\text{MHz}$, $V_{REF} = 1.4\text{V} \pm 200\text{mV}$.
 - AC Operating Condition is changed as defined :
 - $V_{IH}(\text{max}) = 5.6\text{V AC}$. The overshoot voltage duration is $\leq 3\text{ns}$.
 - $V_{IL}(\text{min}) = -2.0\text{V AC}$. The undershoot voltage duration is $\leq 3\text{ns}$.
- 2K/32ms is changed to 4K/64ms.

Revision .3 (April 1998)

- Self refresh current(I_{CC6}) is changed.

KMM466S204CT

144pin SDRAM SODIMM

KMM466S204CT SDRAM SODIMM

2Mx64 SDRAM SODIMM based on 1Mx16, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S204CT is a 2M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S204CT consists of eight CMOS 1M x 16 bit Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The KMM466S204CT is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
KMM466S204CT-F0	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,050mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	BA0
13	DQ4	14	DQ36	Voltage Key				107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	*BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	*A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A10/AP	Address input (Multiplexed)
BA0	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS1	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

- * These pins are not used in this module.
- ** These pins should be NC in the system which does not support SPD.

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REV. 4 May '98

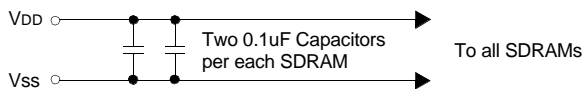
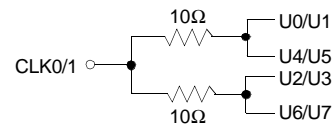
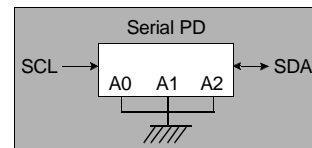
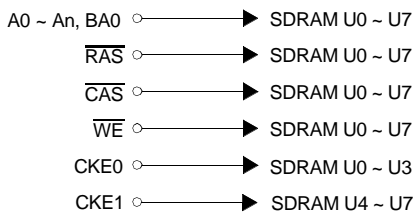
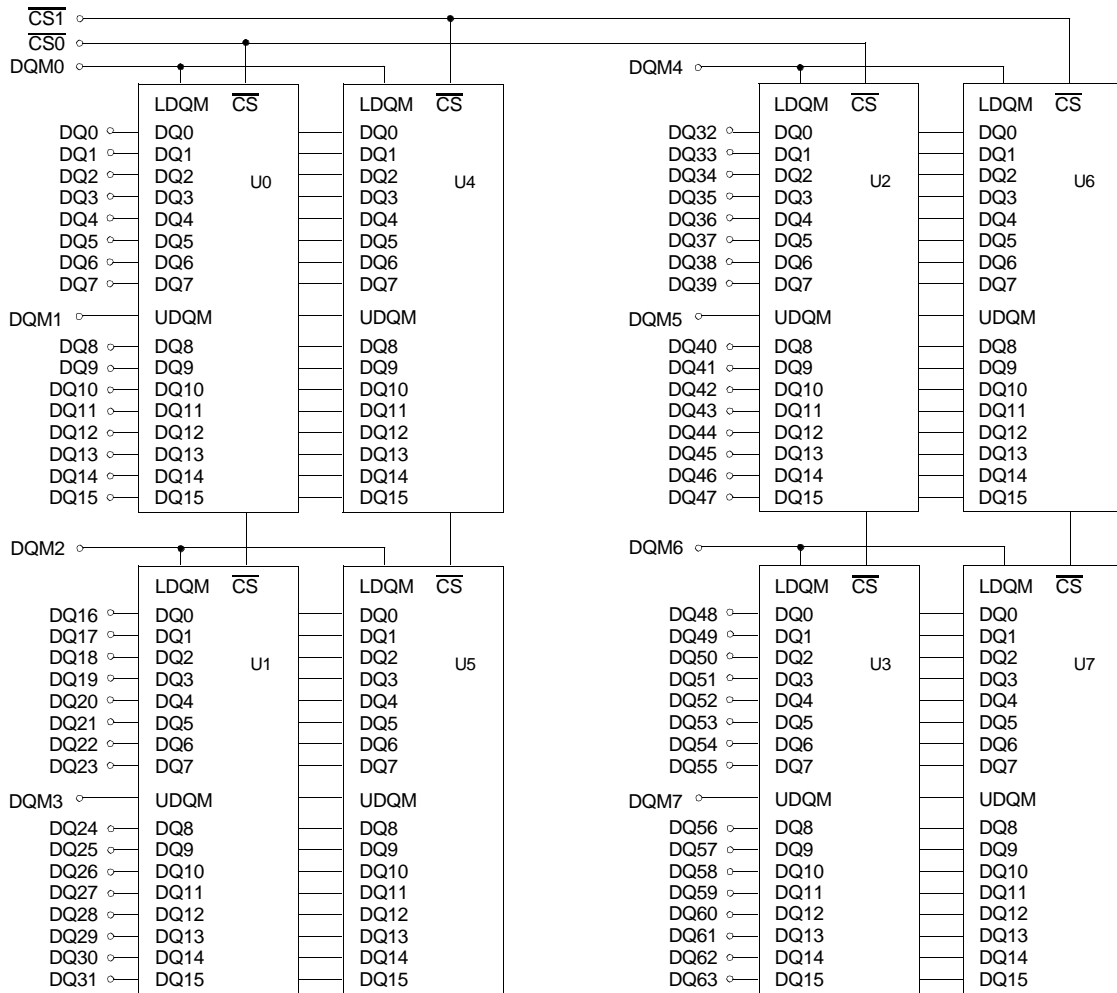
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
\overline{CS}	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+ t_{ss} prior to valid command.
A0 ~ A10/AP	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, Column address : CA0 ~ CA7
BA0	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
\overline{RAS}	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with \overline{RAS} low. Enables row access & precharge.
\overline{CAS}	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with \overline{CAS} low. Enables column access.
\overline{WE}	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from \overline{CAS} , \overline{WE} active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
V _{DD} /V _{SS}	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

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FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{ss}	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to V _{ss}	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _d	8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{ss} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DDQ} +0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-8	-	8	uA	3
Input leakage current (I/O pins)	I _{IL}	-3	-	3	uA	3,4

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
 4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A ₀ ~ A ₁₀ /AP, BA0)	C _{IN1}	40	60	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN2}	40	60	pF
Input capacitance (CKE0 ~ CKE1)	C _{IN3}	25	35	pF
Input capacitance (CLK0 ~ CLK1)	C _{IN4}	25	35	pF
Input capacitance ($\overline{\text{CS0}}$ ~ $\overline{\text{CS1}}$)	C _{IN5}	25	35	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	15	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	10	20	pF

DC CHARACTERISTICS(Recommended operating condition unless otherwise noted, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	CAS Latency	Version	Unit	Note
				-0		
Operating current (One bank active)	I _{CC1}	Burst length = 1 t _{RC} ≥ t _{RC} (min) I _{OL} = 0 mA		420	mA	1
Precharge standby current in power-down mode	I _{CC2P}	CKE ≤ V _{IL} (max), t _{CC} = 15ns		8	mA	
	I _{CC2PS}	CKE & CLK ≤ V _{IL} (max), t _{CC} = ∞		8		
Precharge standby current in non power-down mode	I _{CC2N}	CKE ≥ V _{IH} (min), \overline{CS} ≥ V _{IH} (min), t _{CC} = 15ns Input signals are changed one time during 30ns		120	mA	
	I _{CC2NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), t _{CC} = ∞ Input signals are stable		32		
Active standby current in power-down mode	I _{CC3P}	CKE ≤ V _{IL} (max), t _{CC} = 15ns		16	mA	
	I _{CC3PS}	CKE & CLK ≤ V _{IL} (max), t _{CC} = ∞		8		
Active standby current in non power-down mode (One bank active)	I _{CC3N}	CKE ≥ V _{IH} (min), \overline{CS} ≥ V _{IH} (min), t _{CC} = 15ns Input signals are changed one time during 30ns		200	mA	
	I _{CC3NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), t _{CC} = ∞ Input signals are stable		120	mA	
Operating current (Burst mode)	I _{CC4}	I _{OL} = 0 mA Page burst 2Banks activated t _{CCD} = 2CLKs	3	560	mA	1
			2	500		
Refresh current	I _{CC5}	t _{RC} ≥ t _{RC} (min)		640	mA	2
Self refresh current	I _{CC6}	CKE ≤ 0.2V		2	mA	

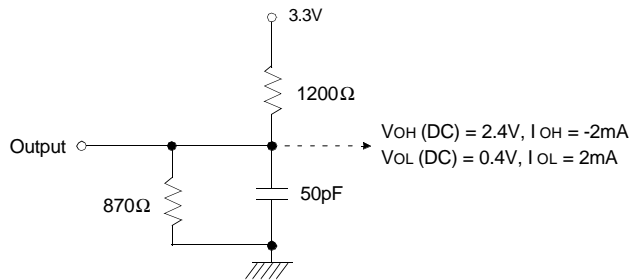
- Notes :** 1. Measured with outputs open.
2. Refresh period is 64ms.

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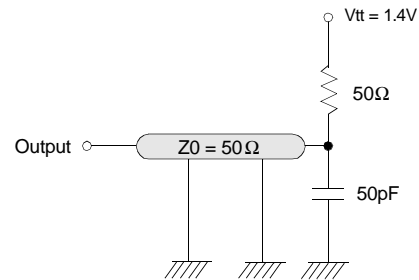
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AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
AC input levels (V_{ih}/v_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-0		
Row active to row active delay	$t_{RRD}(\min)$	20	ns	1
\overline{RAS} to \overline{CAS} delay	$t_{RCD}(\min)$	26	ns	1
Row precharge time	$t_{RP}(\min)$	26	ns	1
Row active time	$t_{RAS}(\min)$	50	ns	1
Row cycle time	$t_{RAS}(\max)$	100	us	
	$t_{RC}(\min)$	80	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	12	ns	2
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)
REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.

Parameter		Symbol	-0		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tcc	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tsac		7	ns	1,2
	CAS latency=2			8		
Output data hold time	CAS latency=3	toH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tss	2.5		ns	3
Input hold time		tSH	1		ns	3
CLK to output in Low-Z		tsLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			8		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time $(tr \& \text{tf}) = 1ns$.
 If $tr \& \text{tf}$ is longer than 1ns, transient time compensation should be considered,
 i.e., $[(tr + \text{tf})/2-1]ns$ should be added to the parameter.

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FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S204CT- F0

(Unit : Number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	12ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	2
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	7	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	DQM	BA	A10/AP	A9 ~ A0	Note
Register	Mode register set	H	X	L	L	L	L	X		OP code		1,2
Refresh	Auto refresh	H	H	L	L	L	H	X		X		3
	Self refresh		Entry									L
		Exit	L	H	L	H	H	H	X	X		3
	H				X	X	X	3				
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable									H		4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable									H		4,5
Burst stop		H	X	L	H	H	L	X		X		6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	Both banks								X	H		
Clock suspend or active power down	Entry	H	L	H	X	X	X	X		X		
				L	V	V	V					
Precharge power down mode	Entry	H	L	H	X	X	X	X		X		
				L	H	H	H					
	Exit	L	H	H	X	X	X	X		X		
				L	V	V	V					
DQM		H		X				V		X		7
No operation command		H	X	H	X	X	X	X		X		
				L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A10/AP, BA0 : Program keys. (@ MRS)

2. MRS can be issued only at both banks precharge state.

A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at both banks precharge state.

4. BA0 : Bank select address.

If "Low" at read, write, row active and precharge, bank A is selected.

If "High" at read, write, row active and precharge, bank B is selected.

If A10/AP is "High" at row precharge, BA0 is ignored and both banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),

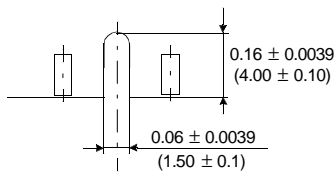
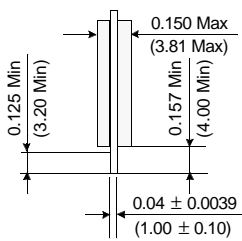
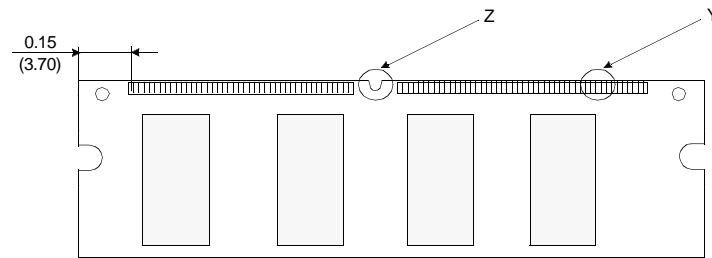
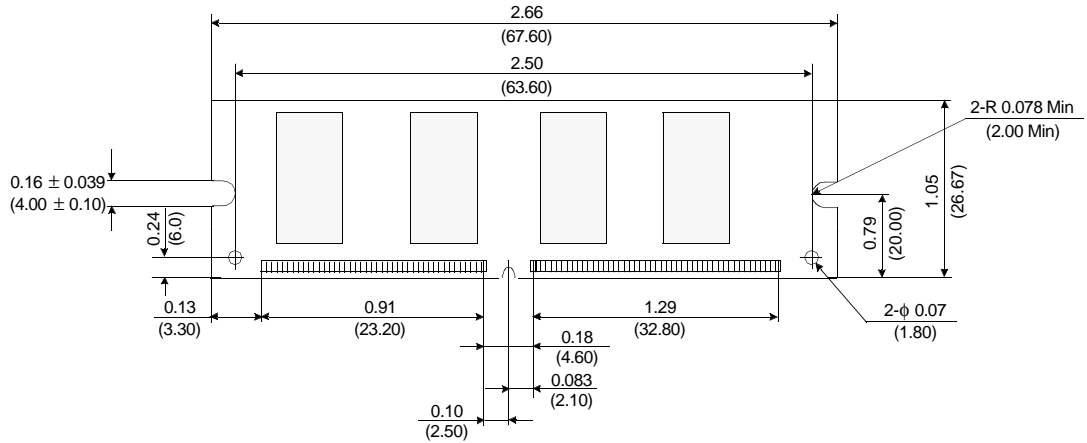
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

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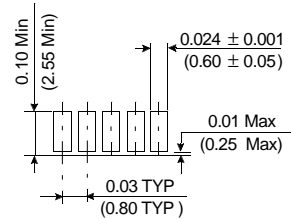
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PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 1Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S1020CT

SERIAL PRESENCE DETECT

SDRAM MODULE

KMM466S204CT-F0

- Organization : 2Mx64
- Composition : 1Mx16 *8
- Used component part # : KM416S1020CT-F10
- # of banks in module : 2 bank
- # of banks in component : 2 banks
- Feature : 1,050mil height & double sided component
- Refresh : 2K/32ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-0	-0	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	11	0Bh	1
4	# of column address on this assembly	8	08h	1
5	# of module banks on this assembly	2 bank	02h	
6	Data width of this assembly	64 bits	40h	
7 Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	7ns	70h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	2 banks	02h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	13ns	D0h	2
24	SDRAM access time from clock @CAS latency of 2	8ns	80h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	26ns	1Ah	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	26ns	1Ah	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module bank density	2 bank of 8MB	02h	
32-61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	F7h	

SERIAL PRESENCE DETECT

SDRAM MODULE

Byte #	Function Described	Function Supported	Hex value	Note
		-0	-0	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71 Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Samsung memory)	K	4Bh	
74	Manufacturer part # (Samsung memory)	M	4Dh	
75	Manufacturer part # (Memory module)	M	4Dh	
76	Manufacturer part # (Memory type & edge connector)	4	34h	
77	Manufacturer part # (Data bits)	Blank	20h	
78 Manufacturer part # (Data bits)	6	36h	
79 Manufacturer part # (Data bits)	6	36h	
80	Manufacturer part # (Mode & operating voltage)	S	53h	
81	Manufacturer part # (Module density)	Blank	20h	
82 Manufacturer part # (Module density)	2	32h	
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0	30h	
84	Manufacturer part # (Compositon component)	4	34h	
85	Manufacturer part # (Component revision)	C	43h	
86	Manufacturer part # (Package type)	T	54h	
87	Manufacturer part # (PCB revision)	Blank	20h	
88	Manufacturer part # (Hyphen)	" - "	2Dh	
89	Manufacturer part # (Power)	F	46h	
90	Manufacturer part # (Minimum cycle time)	0	30h	
91	Manufacturer revision code (For PCB)	Blank(Mother PCB)	20h	
92 Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	-	FFh	
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	-	FFh	

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.