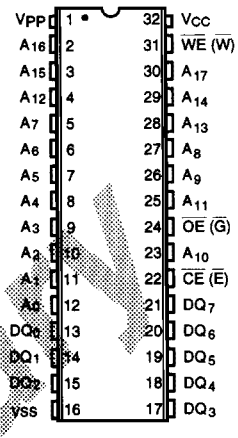
FEATURES

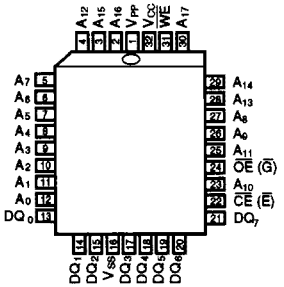
- **Fast access times**
  - **— 100 ns maximum access time**
- **Low CMOS power consumption**
  - **— 30 mA (Active)**
  - **— 100 µA (Standby)**
- **Compatible with JEDEC-standard byte-wide pinouts**
  - **— 32-Pin DIP**
  - **— 32-Pin PLCC**
  - **— 32-Pin TSOP**
- **10,000 rewrites per byte**
- **Program and erase voltage 12.0V ±5%**
- **Pulse Chip Erase**
  - **— One second typical pulse chip-erase**
- **Pulse Programming**
  - **— 10µs typical byte-program**
  - **— Less than 3 seconds typical chip program**
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **Automatic write/erase pulse stop timer**
- **On-chip address and data latches**
- **Latch-up protected to 100 mA from -1V to Vcc + 1V**
- **ESD Protected to 2000V**

PIN CONFIGURATION

DIP



PLCC



OVERVIEW

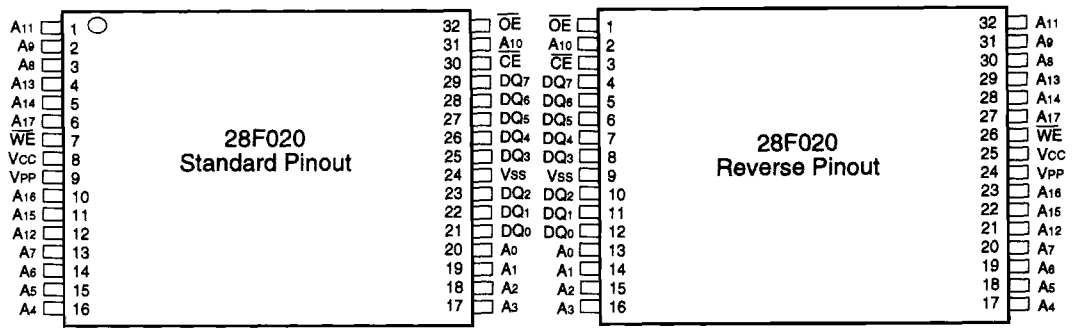
The XL28F020 is a 2 Megabit "Flash" electrically erasable, electrically programmable read only memory organized as 256K bytes of 8 bits each. The XL28F020 is packaged in 32-Pin DIP, TSOP and PLCC. It is designed to erase and program in-system or in standard EPROM programmers.

The XL28F020 offers access times as fast as 100 ns, allowing operation of most popular microprocessors without wait states. To eliminate bus contention, the XL28F020 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) control pins.

EXEL's Flash memories provide EPROM functionality with in-system reprogrammability. The XL28F020 uses a command register to manage the functionality, while maintaining a standard 32-Pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

EXEL's Flash technology reliably maintains memory contents even after 10,000 erase and program cycles. The EXEL memory cell is designed to optimize the erase and programming mechanisms. The XL28F020 uses 12V ± 5% Vpp supply to perform the Erase and Program functions.

TSOP PACKAGES



The XL28F020 is byte programmable using 10µs programming pulses according to standard pulse programming algorithm. It takes less than two seconds to program the entire chip. The entire chip is bulk erased using 10ms erase pulse according to standard pulse erase algorithm. Typical erasure time at room temperature is less than one second.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register latches address and data needed for the programming and erase operations. For system design simplification, the XL28F020 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ signal, whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

PIN DESCRIPTION

A_0 - A_{17}
Address Inputs for memory locations. Internal latches hold addresses during write cycles.

DQ_0 - DQ_7
Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)
The Chip Enable is an active low input signal which activates the chip's control logic and input buffers. Chip Enable high deselects the device and switches the chip to stand-by mode.

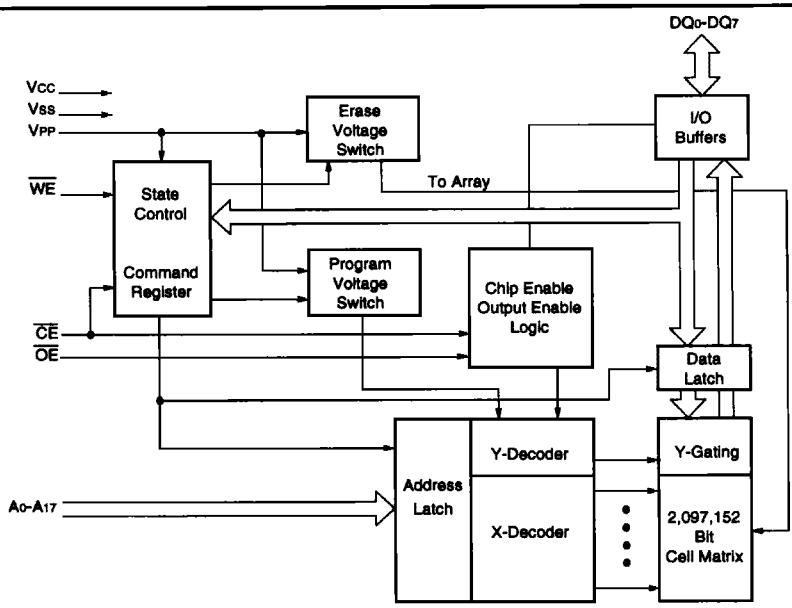
$\overline{OE}$ ($\overline{G}$)
The Output Enable is an active low input signal which gates the outputs of the device through the data buffers during memory read cycles.

$\overline{WE}$ ($\overline{W}$)
The Write Enable is an active low input signal which controls the write function of the command register to the memory array. The target address is latched in on the falling edge of the Write Enable signal and the appropriate data is latched in on the rising edge of the same signal.

V_{PP}
Power supply for erase and programming functions. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq 12V$.

V_{CC}
Power supply for device operation. (5V ± 10%)

V_{SS}
Ground



BLOCK DIAGRAM

7

PRODUCT SELECTOR GUIDE

Family Part No.:	XL28F020			
Ordering part No.: ±10% V_{CC} Tolerance	-100	-120	-150	-200
Max Access Time (ns) t_{ACC}	100	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns) t_{CE}	100	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns) t_{OE}	40	50	55	55

DEVICE OPERATION

The XL28F020 uses 100% TTL-level control inputs to manage the command register. Erase and program operations require 12V ±5% power supply.

Read Only Memory

Without high V_{PP} voltage, the XL28F020 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and program operations are enabled via the command register. In addition, two-cycle commands are required for erase and program operations. The traditional read, standby, output disable, and Auto select modes are also available via the register.

Overview of Pulse Erase/Program Operations

Pulse Erase Sequence

A multiple step command sequence is required to pulse erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Pulse Erase Algorithm.

1. Erase Set-up: Write the Erase Set-up command to the command register.

2. Erase: Write the Erase command (same as Set-up command) to the command register again. The second command starts internal erase operation. A system software routine must then time-out (10 ms) prior to issuing the Erase-verify command. An integrated stop timer prevents any possibility of over erasure.

3. Erase-verify: Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs data of the addressed byte in order to command the array data with FFH data (Byte erased). After successful data verification, the Erase-verify command is written again with a new address information. Each byte of the array must be verified prior to programming.

If data of an addressed location is not verified, the Erase sequence must be repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Pulse Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of data. Refer to the Pulse Programming Algorithm for programming steps.

1. Program Set-up: Write the Program Set-up command to the command register.

2. Program: Write the Program command to the command register followed by Address and Data. A system software routine must then time-out 10 µs prior to issuing the Program-verify command. An integrated stop time prevents any possibility of over programming.

3. Program-verify: Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the data that was just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence must be repeated for subsequent addressses.

If programmed data is not verified, the Program sequence must be repeated until a successful comparison verified or the sequence is repeated 25 times.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2V (typically 3.7V). If $V_{CC} < V_{LKO}$,the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2V.

Data Protection

The XL28F020 is designed to offer protection against accidental erasure of the device, caused by spurious system level signals that may exist during power transitions. The XL28F020 powers up in the read mode. Also with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down sequences or system noise.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a Low while $\overline{OE}$ is High.

Power-Up Write Inhibit

During power up, the device ignors any command while the $\overline{WE}=\overline{CE}=V_{IL}$ and $\overline{OE}=V_{IH}$. The internal state machine is automatically reset to the read mode upon power-up.

FUNCTIONAL DESCRIPTION

Description of User Modes

Table 1. XL28F020 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	X	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (9EH)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (BDH)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	X	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:
X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2V$, See DC Characteristics for voltage levels of V_{PPH}, $0V < An < V_{CC} + 2V$, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:
1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC} +2.0V$. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics table. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via the command register. Refer to Table 2 for details.
3. $11.5 \leq V_{ID} \leq 13.0V$
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ MODE ($V_{PP} < V_{CC} + 2V$)

Read

The XL28F020 functions as a read only memory device when $V_{PP} < V_{CC} + 2V$. The XL28F020 has two control pins. Both must be in proper states in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid data output. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time (t_{OE}) is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least tACC - tOE).

Standby Mode

The XL28F020 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at V_{CC}—0.5V), consumes less than 100µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode, outputs are in a high impedance state, independent of the $\overline{OE}$ input state.

If the device is deselected during internal erase, program, or program/erase verification cycles, the device will draw active current until the operation is terminated.

Output Disable

Device outputs are disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

Programming in a PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5V to 13.0V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0V$ while in Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. Table 2 lists the manufacture code and device code. All identifiers for manufacturer and device codes will exhibit odd parity with MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device).

Table 2. XL28F020 Auto Select Guide

Type	A_0	Code Hex	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	9E	1	0	0	1	1	1	1	0
Device Code	V_{IH}	BD	1	0	1	1	1	1	0	1

ERASE, PROGRAM, AND READ MODE (VPP = 12.0V ±5%)

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as the input to the internal state machine. The output of the state machine determines device operation.

The command register does not occupy an addressable memory location. The register is a latch that stores the command data, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ Low, while $\overline{OE}$ is High. Addresses are latched on the rising edge of the $\overline{WE}$ signal. Standard microprocessor write timings are used.

Register bits R_7 - R_0 correspond to the data inputs DQ_7 - DQ_0 (Refer to Table 3). Register bits R_7 - R_5 store command data. Other bits (R_4 to R_0) must be zero. The only exceptions are with the reset command, when FFH is written to the register; and the Auto select command, when 90H is written to the register.

The device requires the $\overline{OE}$ pin to be High for write operations. This condition eliminates bus contention possibiliy during programming operations. In order to write, $\overline{OE}$ must be High, with $\overline{CE}$ and $\overline{WE}$ Low. If any pin is not in the correct state, a write command will not be executed.

Refer to AC Write Characteristics and Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until a new command is written into the command register.

The command register defaults to 00H (Read Mode) upon V_{PP} power-up. This default state helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

7

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Command	X	X	X	X	X	X	X	X

Notes:
1. XL28F020 Command Definitions.
2. X=Appropriate Data or Register Command.

Table 4. XL28F020 Command Definition

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Notes 4,5)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H/90H	Read	00H/01H	9EH/BDH
Erase Set-up/Erase Chip	Write	X	20H	Write	X	20H
Erase-Verify	Write	EA	A0H	Read	X	EVD
Program Set-up/Program	Write	X	40H	Write	PA	PD
Program-Verify	Write	X	C0H	Read	X	PVD
Reset (Note 5)	Write	X	FFH	Write	X	FFH

Notes:
1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during the read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify.
   PA is latched on the Program command.
4. Wait 6µs after the first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.
5. Please refer to Reset Command section.

Pulse Erase Sequence

Set-up Erase/Erase Commands

Set up Pulse Erase

Set-up Pulse Erase is the first of a two-cycle pulse erase command. It is a command-only operation that stages the device for bulk chip erase. The array content is not altered with this command. The data 20H must be written to the command register in order to perform the Set-up Pulse Erase operation.

Pulse Erase

The second two-cycle pulse erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The pulse erase operation begins with the rising edge of the $\overline{WE}$ pulse. The pulse erase operation must be terminated by writing the (Erase-verify) command to the register after the device time erase out.

This two step sequence of the Set-up and Erase commands helps to ensure the memory contents are not accidentally erased. Also, chip erase can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

The Flash memory device must be fully programmed with 00H data prior to pulse erasure. This equalizes the charge on all memory cells, ensuring reliable erasure.

Pulse Erase-verify Command

The pulse erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Pulse Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Pulse Erase-verify operation, the XL28F020 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Pulse Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$ signal. The process must be repeated for each byte of the memory array until either all bytes in the array are verified or until the first location that fails the verify test (FFH data) or all bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip must be erased again (refer back to Set-up Pulse Erase/Pulse Erase section). Pulse Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Pulse erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The pulse erase-verify command must be written to the register in order to terminate the erase operation. During the internal pulse erase operation, the local microprocessor must be dedicated to run software time out routine (10ms long) as specified in Exel's time out Pulse erase algorithm.

Should a system interrupt occur during an pulse erase operation, always write the Pulse Erase-verify command prior to executing an interrupt sequence.

Pulse Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Pulse erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The XL28F020 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Pulse programming algorithm with the appropriate data pattern.

If the device is already programmed, data other than FFH will be read from address locations. Follow the Pulse Erase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Pulse programming algorithm. Erasure then continues with an initial pulse erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (1 second). Erase efficiency may be improved by storing the address of the last byte that failed to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase operations are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. Erasure typically occurs in one second. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Pulse Erase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Pulse programming algorithm (Figure 3) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Erase Set-Up	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-Verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, less than V_{CC} + 2.0V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.

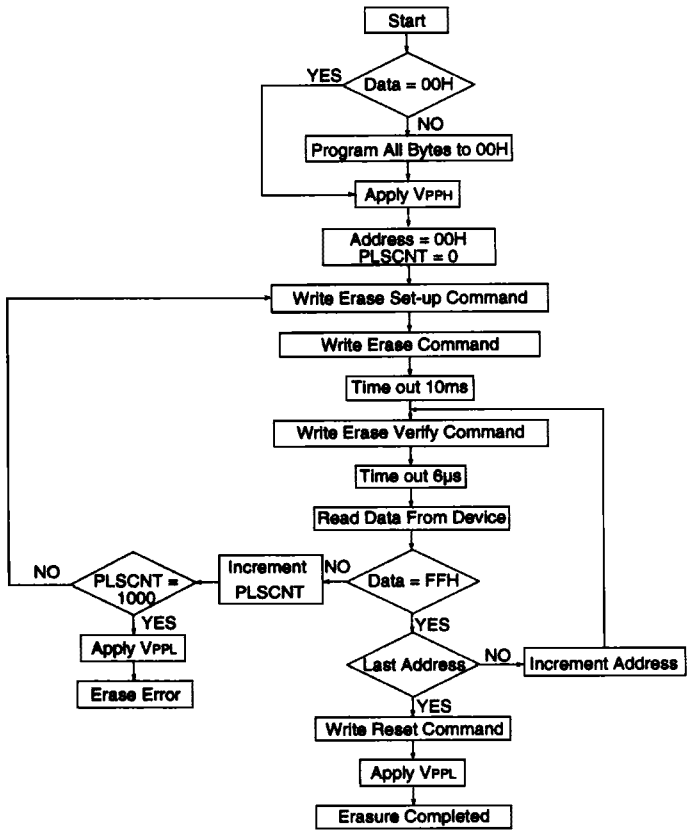
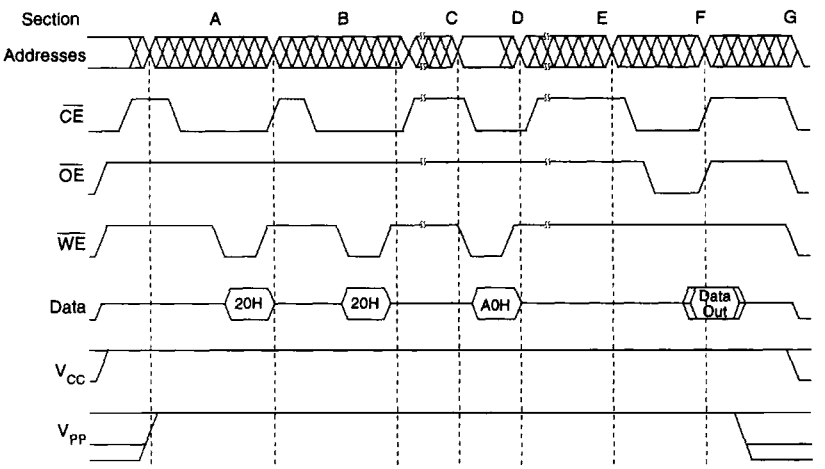


Figure 1. Pulse Erase Algorithm



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time-Out	Write	Time-Out	Read	Stand by
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Erase Set-up	Erase	Erase (10ms)	Erase-Verify	Transition (6µs)	Erase Verification	Proceed per Erase Algorithm

Figure 2. A.C. Waveforms For Pulse Erase Operations

Analysis of Pulse Erase Timing Waveform

Note: *This analysis does not include the requirement to program the entire array with 00H data prior to erasure. Refer to the Pulse Erase algorithm.*

Set-up Pulse Erase/Erase

This analysis illustrates the use of two-cycle pulse erase commands (section A&B in figure 2). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the pulse erase operation (section B) on the rising edge of this $\overline{WE}$ signal. All memory locations are erased in parallel. No address information is required. Internal erase occurs in section C.

Time-out

A software time out routine (10ms duration) must be initiated on the rising edge of the $\overline{WE}$ signal of section B.

Note: *An integrated stop timer prevents any possibility of over erasure by limiting each time-out period to10 miliseconds.*

Pulse Erase-verify

Upon completion of the erase software timing routine, the microprocessor must write the Pulse Erase-verify command (A0H). This command terminates the pulse erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Pulse Erase-verify command also stages the device for data verification (section F).

After each pulse erase operation, each byte must be verified. The byte address to be verified must be supplied with the Pulse Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ signal.

Another software time out routine (6 µs duration) must be executed to allow for the generation of internal voltages for margin checking and read operation (section E).

During Pulse Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D through F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, pulse erase the device again. Repeat sections A through F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically only 100 erase pulses are required.

Notes:

1. All address locations must be programmed to 00H prior to device erase. This equalizes the charge on all memory cells and ensures reliable erasure.

2. The pulse erase verify command must be written to terminate the erase operation. Should a system interrupt occur during an erase operation, always write the erase-verify command prior to executing an interrupt sequence.

Pulse Programming Sequence

Set-up Program/Program Command

Pulse Set-up Program

The XL28F020 can be programmed byte by byte. Bytes may be programmed sequentially or at random. Pulse Set-up Program is the first of a two-cycle program command. It stages the device for pulse byte programming. The Pulse Set-up Program operation is performed by writing 40H to the command register.

Pulse Program

Only after the pulse program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ signal. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Pulse Program-verify command to terminate the pulse programming operation. This two step sequence of the Pulse Set-up and Pulse Program commands helps to ensure that memory contents are not accidentally written. Also, pulse programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In the absence of this high voltage, memory contents cannot be programmed. Refer to AC Characteristics and Waveforms for specific timing parameters.

Pulse Program Verify Command

Following each pulse programming operation, programmed memo's location must be verified.

Write C0H into the command register to initiate the Pulse Program-verify operation. The rising edge of this $\overline{WE}$ signal terminates the pulse programming operation. The Pulse Program-verify operation stages the device for verification of the last programmed byte. Addresses were previously latched. No new information is required.

Pulse Margin verify

During the Pulse Program-verify operation, the XL28F020 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired location. Should the byte fail to verify, reprogram (refer to the Set-up Program/Program). Figure 5 and Table 7 indicate how instructions are combined with the bus operations to perform pulse byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Pulse Programming Algorithm

The XL28F020 Pulse programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Pulse programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second attempt. The entire sequence of pulse programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the pulse programming algorithm.

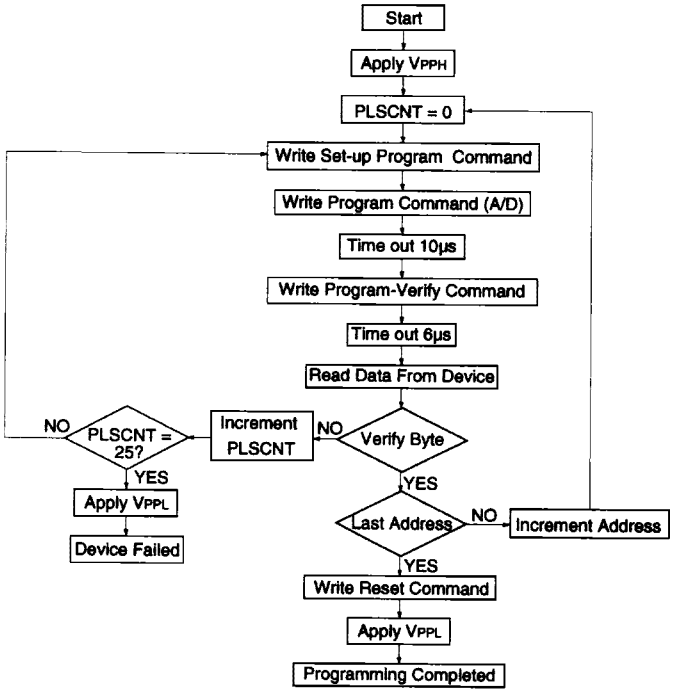


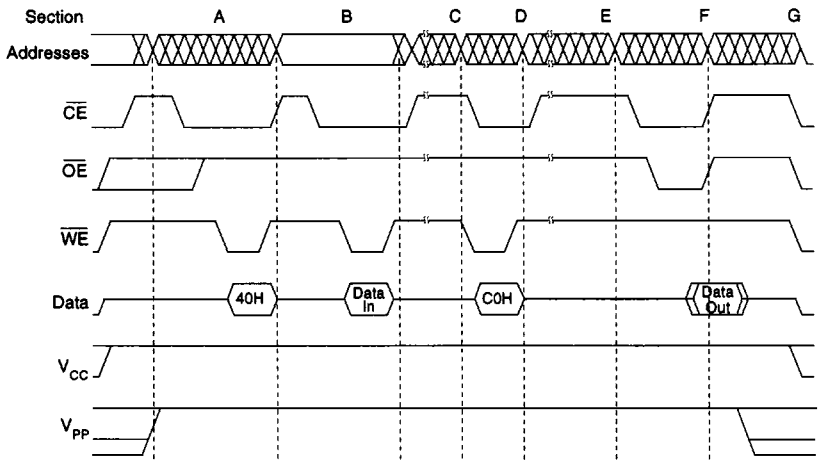
Figure 3. Pulse Programming Algorithm

Table 6. Pulse Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Program Set-Up	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH2})
Write	Program-Verify (Note 2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify programming
Standby		Compared data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, less than V_{CC} + 2.0V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time-Out	Write	Time-Out	Read	Stand by
Command	40H	Program Address, Program Data	N/A	C0H (Stops Prog.)	N/A	Compare Data	N/A
Function	Program Set-up	Program Command Latch Address & Data	Prog. (10µs)	Prog.-Verify	Transition (6µs)	Erase Verification	Proceed per Programming Algorithm

Figure 4. AC Waveforms for Pulse Programming Operations

7

Analysis of Pulse Program Timing Waveforms

Set-up Pulse Program/Pulse Program

Two-cycle write commands are required for pulse program operations (section A&B in figure 4). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ signal (section B) also initiates the internal programming cycle. The device is programmed on a byte by byte basis either sequentially or randomly.

Internal programming occurs in section C.

Time-out

A software time out routine (10 µs duration) must be initiated on the rising edge of the $\overline{WE}$ signal in section B.

Note: *An integrated stop timer prevents any possibility of overprogramming by limiting each time-out period of 10 µs.*

Pulse Program-verify

Upon completion of the pulse program time out routine, the microprocessor must write the pulse program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ signal (section D). The pulse program-verify command also stages the device for data verification (section F). Another software time out routine (6µs duration) must be executed to allow for the generation the of the internal voltages for margin checking and read operations (section E.)

During program-verification (section F) each byte just programmed is read to compare array data against original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Note: *The pulse program-verify operation must be written to terminate the pulse programming operation. Should a system interrupt occur during a pulse programming operation, always write the program-verify command prior to executing an interrupt sequence.*

Algorithm Timing Delays

There are four different timing delays associated with the Pulse erase and Pulse Program algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} is first turned on. The impedance on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased simultaneously and the 0.1µF/device. V_{PP} must reach its final value 1000ns before any command is written into the device.

2. The second delay time is the erase time pulse width (100ms). A software timing routine should be run by the local microprocessor to time out the delay. The pulse erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Pulse Erase-verify operation after each pulse.

3. A third delay time is required for each programming pulse width (10µs). The pulse programming algorithm is interactive and verifies each byte after a program pulse. The pulse program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the pulse programming operation.

4. A fourth timing delay associated with both the Pulse erase and Pulse Program algorithms is the write recovery time (6µs). During this time internal circuitry is changing voltage levels from the erase/program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible flase data (it may appear the device is not properly erased or programmed).

Note: *Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.*

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified separately. When a device is completely erased and verified, use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-up Sequence

V_{CC} Prior to V_{PP}

The XL28F020 powers-up in the Read only mode. When V_{CC} = 0V, the V_{PP} voltage is internally disabled from the device. With V_{PP} = 12V, the Flash device resets to the Read mode when V_{CC} rises above 2V.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the set-up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires two sequential reset commands. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

Exel's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not generally, a desired system design practice.

The XL28F020 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 9EH. A read cycle from address 0001H returns the device code BDH (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages ..... -65°C to +150°C
Plastic Package ..... -65°C to +125°C
Ambient Temperature
with Power Applied ..... -55°C to +125°C
Voltage with Respect to Ground
All pins except A_9 and V_{PP} (Note 1) ..... -2.0V to 7.0V
V_{CC} (Note 1) ..... -2.0V to 7.0V
A_9 (Note 2) ..... -2.0V to 14.0V
V_{PP} (Note 2) ..... -20V to 14.0V
Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, inputs may overshoot VSS to -2.0 V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on A_9 and V_{PP} pins is -0.5V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
  Case Temperature (Tc) ..... 0°C to +70°C
Industrial (I) Devices
  Case Temperature (Tc) ..... -40° to +85°C
V_{CC} Supply Voltage ..... +4.50 V to +5.50 V
V_{PP} Supply Voltages
  Read ..... -0.5 V to +12.6 V
  Program, Erase, and Verify ..... +11.4 V to +12.6 V

MAXIMUM OVERSHOOT

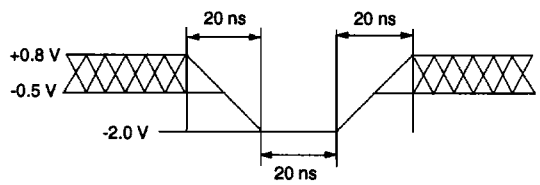


Figure 5. Maximum Negative Input Overshoot (Any Inputs)

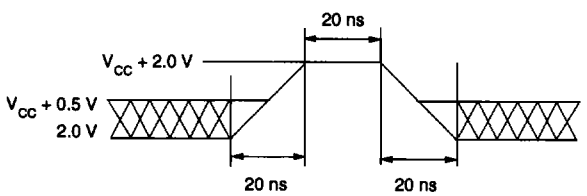


Figure 6. Maximum Positive Input Overshoot (Any Inputs except V_{PP})

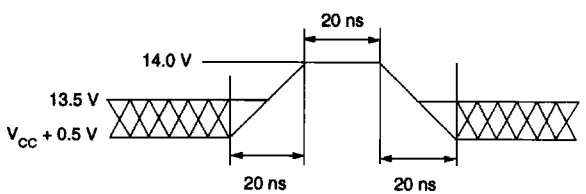


Figure 7. Maximum V_{PP} Overshoot

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1-3)

DC CHARACTERISTICS—TTL COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{IN} = V_{CC}$ or V_{SS}			±1	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{OUT} = V_{CC}$ or V_{SS}			±1	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max. $\overline{CE} = V_{IH}$		0.2	1	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC}=V_{CC}$ Max., $\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$ I_{OUT} = 0 mA, at 6MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
		$V_{PP} = V_{PPL}$			±1	
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.5 mA $V_{CC} = V_{CC}$ Min.	2.4			V
V_{ID}	A_9 Auto Select Voltage	$A_9 = V_{ID}$	11.5		13.0	V
I_{ID}	A_9 Auto Select Voltage	$A_9 = V_{ID}$ Max. $V_{CC} = V_{CC}$ Min.		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when $V_{PP} = V_{PPL}$	0		V_{CC} +2	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:
1. **Caution:** the XL28F020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{IN} = V_{CC}$ or V_{SS}			±1	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{OUT} = V_{CC}$ or V_{SS}			±1	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max. $\overline{CE} = V_{CC}$±0.5V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC}=V_{CC}$ Max., $\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$ I_{OUT} = 0 mA, at 6MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPL}$		70	200	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.5 mA $V_{CC} = V_{CC}$ Min.	0.85 V_{CC}			V
V_{OH2}		I_{OH} = -100 µA $V_{CC} = V_{CC}$ Min.	V_{CC} -0.4			
V_{ID}	A_9 Auto Select Voltage	$A_9 = V_{ID}$	11.5		13.0	V
I_{ID}	A_9 Auto Select Voltage	$A_9 = V_{ID}$ Max. $V_{CC} = V_{CC}$ Min.		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when $V_{PP} = V_{PPL}$	0		V_{CC} +2	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:
1. **Caution:** the XL28F020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:
1. Sampled, not 100% tested.
2. Test Conditions $T_A = 25°C$, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
AC CHARACTERISTICS—Read Only Operation (Notes)

Parameter Symbols				XL28F020					
JEDEC	Standard	Parameter Description		-100	-120	-150	-200	-250	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 3)	Min. Max.	100	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	100	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	100	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	40	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 2)	Min. Max.	0	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min. Max.	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 3)	Min. Max.	0	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 3)	Min. Max.	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	Min. Max.	0	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	6	ns
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 3)	Min. Max.	50	50	50	50	50	µs

Notes:
1. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10ns
   Input Pulse levels: 0.45 to 2.4V
   Timing Measurements Reference Level: Inputs:0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. Guaranteed by design, not tested.
3. Not 100% tested.

KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	Must be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High-Impedence "Off" State

SWITCHING WAVEFORMS

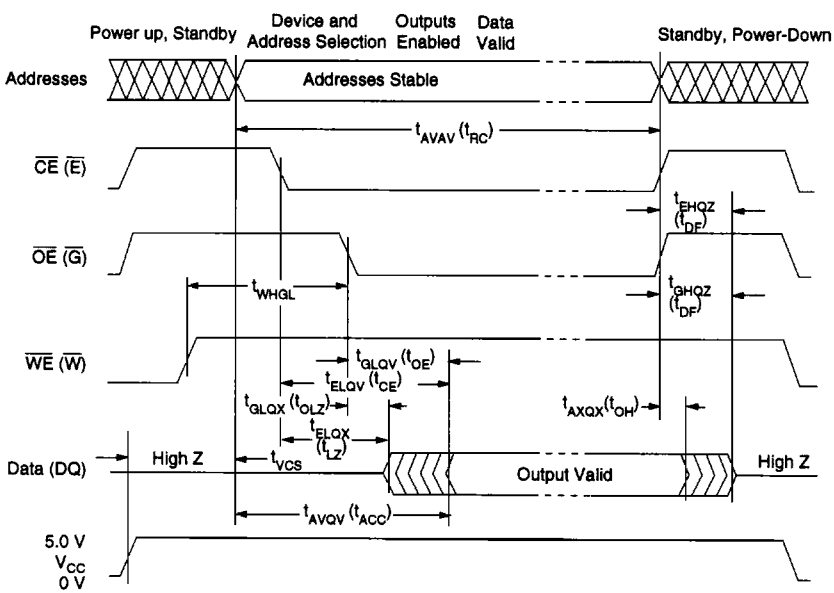


Figure 8. AC Waveforms for Read Operations

AC CHARACTERISTICS—Pulse Write/Erase/Program Operations (Notes 1-5)

Parameter Symbols				XL28F020					
JEDEC	Standard	Parameter Description		-100	-120	-150	-200	-250	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 5)	Min. Max.	100	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	0	ns
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min. Max.	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse	Min. Max.	20	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation (Note 3)	Min. Max.	10	10	10	10	10	µs
t_{WHWH2}		Duration of Erase Operation (Note 3)	Min. Max.	9.5	9.5	9.5	9.5	9.5	ms
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 5)	Min. Max.	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 5)	Min. Max.	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 5)	Min. Max.	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 10% V_{PPL} (Note 5)	Min. Max.	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 5)	Min. Max.	100	100	100	100	100	ns

Notes:
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.
2. Input Rise and Fall times: ≤ 10ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
3. Maximum pulse widths not required because the on-chip program erase stop timer will terminate the pulse widths internally on the device.
4. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip Enable Waveform.
5. Not 100% tested.

SWITCHING WAVEFORMS

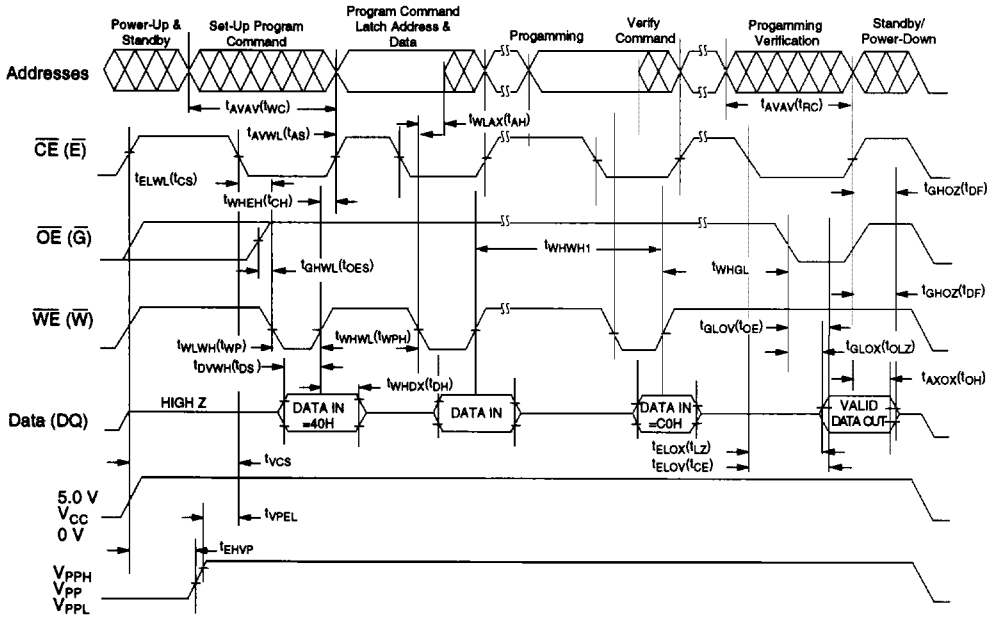


Figure 9. AC Waveforms for Pulse Programming Operation

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SWITCHING WAVEFORMS

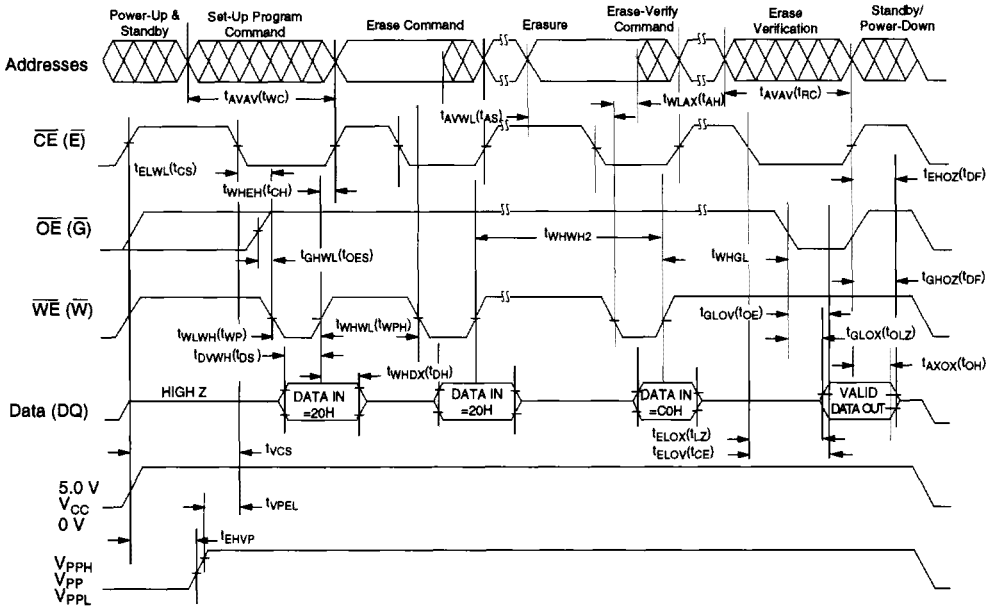
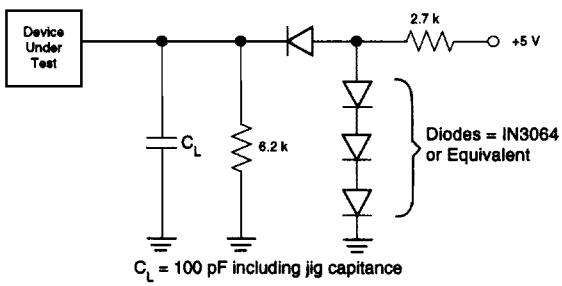
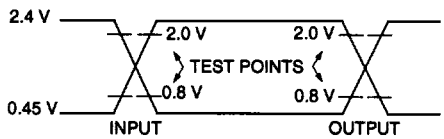


Figure 10. AC Waveforms for Pulse Erase Operation

SWITCHING TEST CIRCUIT



SWITCHING TEST WAVEFORMS



AC Testing: Inputs are driven at 2.4 V for a logic "1" and .45 V for a logic "0". Input pulse rise and fall times are 10 ns.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.(2)		
Chip Erase Time		1 (Note 1)	10	Seconds	Excludes 00H Programming prior to erasure
Chip Programming Time		4 (Note 1)	25	Seconds	Excludes system-level overhead
Write/Erase Cycle	10,000			Cycles	Pulse Programming

Notes:
1. 25°C, 12 V V_{PP}
2. Maximum time specified is lower than worst case. Worst case is derived from the Pulse Erase count (Pulse Erase = 1000 Max. and Pulse Write = 25 max.) or Auto Programming/Erase integral pulse counter (Auto Program = 6,000 pulses and Auto Erase = 6,000 pulses. Typical worst case for program and erase operations is significantly less than the actual device limit.
3. Typical worst case = 84µs. DQ_5 = "1" only after a byte

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	-1 V	13.5V
Input Voltage with respect to V_{SS} on all pins I/O pins	-1 V	V_{CC} + 1.0 V
Current	-100 mA	+100 mA
Includes all pins except VCC. Test Conditions: VCC = 5 V, one pin at a time.		

DATA RETENTION

Parameter	Min.	Units	Test Conditions
Min. Pattern Data Retention Time	10	Years	150°C
	20	Years	125°C