D • A • T • A • B • O • O • K

STD80/STDM80
0.5μm 5V/3.3V Standard Cell Library

April 1997

SAMSUNG

SAMSUNG ASIC

STD80/STDM80
0.5μm 5V/3.3V Standard Cell Library
Data Book

© 1997 Samsung Electronics Co., Ltd.
All rights reserved. No part of this document may be reproduced, in any form or by any means, without the prior written consent of the publisher. Samsung assumes no responsibility for any errors resulting from the use of the information contained herein, nor does it convey any license under the patent rights of Samsung or others. Samsung reserves the right to make changes in its products or product specification to improve function or design at any time, without notice.

SEC, STD80 and STDM80 are trademarks of Samsung Electronics Co., Ltd. Verilog is a registered trademark of Cadence Design Systems, Inc. Viewlogic is a registered trademark of Viewlogic Systems, Inc. Mentor is a registered trademark or Mentor Graphics Co. Synopsys is a registered trademark of Synopsys, Inc. Gards is a registered trademark of Silvar-Lisco.

Head Office

Samsung Electronics Co., Ltd
LSI Division, ASIC Team
San #24, Nongseo-ree,
Kiheung-eup, Yongin-shi,
Kyunggi-do, Korea

TEL 02-760-6500 (Hot Line)
FAX 02-760-6499

Marketing Team

Samsung Electronics Co., Ltd
Semiconductor Sales Division, LSI Export Team
15th Fl., Severance Bldg.
84-11, 5-Ka, Namdaemoon-Ro, Chung-Ku,
Seoul, Korea

TEL 02-259-4988
FAX 02-259-2494

Printed in the Republic of Korea

Introduction

This databook contains information about STD80/STDM80, 0.5μm 5V/3.3V DLM/TLM standard cell library developed by SEC (Samsung Electronics Corporation).

The “library” basically contains various kinds of internal and I/O cells and soft-macros which are used for developing ASIC (Application Specific Integrated Circuit). It also includes a design kit helping designers to work in a workstation platform, and all sorts of design environments needed for an automatic chip design.

There are seven chapters in this databook:

Chapter 1	Introduction to STD80/STDM80
Chapter 2	Electrical Characteristics
Chapter 3	Internal Macrocells
Chapter 4	Input/Output Cells
Chapter 5	Memory Compilers
Chapter 6	Datapath Compilers
Chapter 7	JTAG Boundary Scans.

In this databook each cell is followed by its AC electrical characteristics, and these characteristic values are almost equal when the corresponding cell is operated in a real chip.

The purpose of this databook is to prevent any misuse or misapplication of STD80/STDM80 cell library by providing precise information about the cell list, electrical data, directions for use, and matters demanding special attention.

Table of Contents

1 Introduction to STD80/STDM80

Library Description 1-1
Features 1-1
CAE Support 1-2
Product Family 1-2
- Internal Macrocells 1-2
- Macrofunctions 1-2
- Megafunctions 1-2
- Memory Compilers 1-2
- Datapath Compilers 1-2
- Input/Output Cells 1-3

V_{DD}/V_{SS} Rules and Guidelines 1-6
Power Dissipation 1-7
Propagation Delays 1-9
Delay Model 1-13
Testability Design Methodology 1-14
Maximum Fanouts 1-15
Product Line-Up 1-22
Packages 1-22
Dedicated Corner V_{DD}/V_{SS} Pads 1-23
External Design Interface Considerations 1-23
Crystal Oscillator Considerations 1-29

2 Electrical Characteristics

DC Electrical Characteristics 2-1
Input Buffer DC Curves 2-3
Output Drive Capabilities 2-5

3 Internal Macrocells

Overview 3-1
Summary Tables 3-2

Logic Cells

AD2/AD2D2 3-11
AD3/AD3D3 3-13
AD4/AD4D2 3-16

AD5/AD5D2 3-19
ND2/ND2D2 3-22
ND3/ND3D2 3-24
ND4/ND4D2 3-27
ND5/ND5D2 3-30
ND6/ND6D2 3-33
ND8/ND8D2 3-38
NR2/NR2D2 3-43
NR3/NR3D2 3-45
NR4/NR4D2 3-48
NR5/NR5D2 3-51
NR6/NR6D2 3-54
NR8/NR8D2 3-59
OR2/OR2D2 3-64
OR3/OR3D3 3-66
OR4/OR4D2 3-69
OR5/OR5D2 3-72
XN2/XN2D2 3-75
XN3/XN3D3 3-77
XO2/XO2D2 3-80
XO3/XO3D3 3-82
AO21/AO21D2 3-85
AO211/AO211D2 3-88
AO22/AO22D2 3-91
AO22A/AO22D2A 3-94
AO222/AO222D2 3-97
AO222A/AO222D2A 3-102
AO33/AO33D2 3-105
AO333/AO333D2 3-110
OA21/OA21D2 3-115
OA211/OA211D2 3-118
OA22/OA22D2 3-121
OA22A/OA22D2A 3-124
OA2222/OA2222D2 3-127
DL(1/2/3/4/5/10)D2/DL(1/2/3/4/5/10)D4 3-132
IV/IVD2/IVD3/IVD4/IVD6/IVD8 3-138
IVA/IVD2A/IVD3A/IVD4A 3-142
IVCD(11/13)/IVCD(22/26)/IVCD44 3-145
IVT/IVTD2/IVTD4/IVTD8 3-149
IVTN/IVTND2/IVTND4/IVTND8 3-153
NID/NID2/NID3/NID4/NID6/NID8 3-157
NIT/NITD2/NITD4/NITD8 3-161
NITN/NITND2/NITND4/NITND8 3-165

Flip-Flops

FD1/FD1D2 3-172
FD1CS/FD1CSD2 3-175
FD1S/FD1SD2 3-179
FD1Q/FD1QD2 3-182
FD1X2 3-184
FD1X4 3-186
YFD1/YFD1D2 3-189
FD2/FD2D2 3-192
FD2CS/FD2CSD2 3-195
FD2S/FD2SD2 3-199
FD2Q/FD2QD2 3-202
FD2X2 3-204
FD2X4 3-207
YFD2/YFD2D2 3-210
FD2T/FD2TD2 3-213
FD2TCS/FD2TCSD2 3-216
FD2TS/FD2TSD2 3-221
FD3/FD3D2 3-225
FD3CS/FD3CSD2 3-228
FD3S/FD3SD2 3-232
FD3Q/FD3QD2 3-235
FD3X2 3-237
FD3X4 3-240
YFD3/YFD3D2 3-243
FD4/FD4D2 3-246
FD4CS/FD4CSD2 3-250
FD4S/FD4SD2 3-256
FD4Q/FD4QD2 3-260
FD4X2 3-263
FD4X4 3-266
YFD4/YFD4D2 3-271
FD5/FD5D2 3-274
FD5S/FD5SD2 3-277
FD5X4 3-280
FD6/FD6D2 3-283
FD6S/FD6SD2 3-286
FD7/FD7D2 3-289
FD7S/FD7SD2 3-292
FD8/FD8D2 3-295
FD8S/FD8SD2 3-299
FDS2/FDS2D2 3-303
FDS2CS/FDS2CSD2 3-306

FDS2S/FDS2SD2 3-310
FDS3/FDS3D2 3-313
FG1 3-316
FG1X4 3-318
FG2 3-323
FG2X4 3-326
FJ1/FJ1D2 3-331
FJ1S/FJ1SD2 3-334
FJ2/FJ2D2 3-337
FJ2S/FJ2SD2 3-340
FJ4/FJ4D2 3-344
FJ4S/FJ4SD2 3-348
FT2/FT2D2 3-352
FT3/FT3D2 3-355

Latches

LD1/LD1D2 3-360
LD1S/LD1SD2 3-363
LD1Q/LD1QD2 3-368
LD1X4/LD1X4D2 3-371
YLD1/YLD1D2 3-380
LD1A 3-383
LD1B 3-385
LD2/LD2D2 3-388
LD2Q/LD2QD2 3-393
YLD2/YLD2D2 3-396
LD3/LD3D2 3-401
LD4/LD4D2 3-406
LD5/LD5D2 3-411
LD5S/LD5SD2 3-414
LD5X4/LD5X4D2 3-419
LD6/LD6D2 3-428
LD7/LD7D2 3-433
LD8/LD8D2 3-438
LDS2 3-443
LDS6 3-446
LS0/LS0D2 3-449
LS1 3-452
LS2 3-455

Bus Holder

BUSHOLDER 3-458

Internal Clock Drivers

CK2/CK4/CK6/CK8/CK12 3-459

Decoders

DC4 3-463
DC4I 3-466
DC8I 3-469

Adders

FA/FAD2 3-477
HA/HAD2 3-482

Multiplexers

MX2/MX2D3 3-486
MX2X4 3-489
YMX2/YMX2D2 3-494
MX2I/MX2ID2 3-497
MX2IA/MX2ID2A 3-500
MX2IX4 3-503
MX3I/MX3ID2 3-508
MX4/MX4D2 3-511
YMX4/YMX4D2 3-516
MX5/MX5D2 3-521
MX8/MX8D2 3-526
YMX8/YMX8D2 3-532

4 Input/Output Cells

Overview 4-1
Summary Tables 4-2

Input Buffers

PvIC/PvICD/PvICU 4-9
PvIL/PvILD/PvILU 4-13
PvIS/PvISD/PvISU 4-16
PvIT/PvITD/PvITU 4-20

Output Buffers

PvOByz 4-24
PvODyz 4-41
PvOTyz 4-64

Bi-Directional Buffers

PvBaDyz/PvBaUDyz 4-98
PvBaTyz/PvBaDTyz/PvBaUTyz 4-98

Input Clock Drivers

PSCKDCy/PSCKDCDy/PSCKDCUy 4-100
PSCKDLy/PSCKDLDy/PSCKDLUy 4-107
PSCKDSy/PSCKDSDy/PSCKDSUy 4-111
PSCKDTy/PSCKDTDy/PSCKDTUy 4-118

Oscillators

PSOSCK(1/2/16/26) 4-123
PSOSCM(1/2/3/4/5/6/16/26/36/46/56/66) 4-132

PCI Buffers

PSIPCIA/PLSIPCIA/PSIPCIA3/PHSIPCIA 4-148
PSOPCIA/PLSOPCIA/PSOPCIA3/PHSOPCIA 4-149
PSIPCIAU 4-150
PSOPCIAU 4-151

PCMCIA Buffers

PVIC(5/3) 4-155
PVIL(D/U)(5/3)/PVIT(D/U)(5/3) 4-155
PVOB(4/8/12)(5/3) 4-156
PVOD(4/8/12)(5/3) 4-156
PVOT(4/8/12)(5/3) 4-157
PVOT(8/12)SM(5/3) 4-157
PVBTT(4/8/12)(5/3) 4-158
PVBTDT8SM/PVBCT8SM(5/3) 4-158

CardBus I/O Buffers

PvITCBU 4-162
PvOTCBU/PvOTCCKCBU/PvOTCVSCBU 4-163
PvODCCKCBU 4-164
PvBTTCBU/PvBTCCKCBU/PvBTCVSCBU 4-165
PvBDCCKCBU 4-166
PLSCB 4-167

USB I/O Buffers

PBUSB/PBUSB1 4-170

Voltage Detector

VDET 4-173

Power Pads

VDD(5/3)(I/P/O/IP/OI/OP/T) 4-174
VSS(5/3)(I/P/O/IP/OI/OP/T) 4-174

5 Memory Compilers

Overview 5-1
Memory Compilers Selection Guide 5-2

CROM Gen 5-3
DROM Gen 5-10
SPSRAM Gen 5-17
SPSRAMA Gen 5-27
SPARAM Gen 5-39
DPSRAM Gen 5-48
DPSRAMA Gen 5-59

6 Datapath Compilers

Overview 6-1
Datapath Compilers Information 6-3

Macro Cells

Adder/Subtracter 6-5
Arithmetic Logic Unit 6-7
Array Multiplier 6-10
Barrel Shifter 6-16
Carry-Select Adder 6-19
Comparator 6-21
Decrementer 6-23
Fast Multiplier 6-25
Incrementer 6-27
Incrementer/Decrementer 6-29
Normalizer 6-31
One Detector 6-33
Parity 6-35
Priority Encoder 6-37
Register File 6-39
Saturating Adder 6-49
Zero Detector 6-51

Logic Cells

AND-OR 6-53
AND-OR-INVERT 6-55
Buffer/Inverter 6-57
Bus Holder 6-59
D Flip-Flop 6-60
Full Adder 6-72

Latch 6-74
Multiplexer 6-82
NAND/AND 6-85
NOR/OR 6-87
OR-AND 6-89
OR-AND-INVERT 6-91
Tri-State Buffer/Inverter 6-93
XNOR/XOR 6-95

7 JTAG Boundary Scans

Overview 7-1
Boundary Scan Architecture 7-2
Boundary Scan Register Macrocells 7-4
    JTBI1 7-5
    JTCK 7-12
    JTIN1 7-14
    JTINT1 7-18
    JTOUT1 7-24
JTAG Tap Controller Macrofunction 7-28
Instruction Register/Decoder Macrofunction 7-31
Implementation of IEEE P1149.1/JTAG 7-32
System Clock Considerations 7-32

Intrduction to STD80/STDM80 1

Table of Contents

Library Description 1-1

Features 1-1

CAE Support 1-2

Product Family 1-2

- Internal Macrocells 1-2
- Macrofunctions 1-2
- Megafunctions 1-2
- Memory Compilers 1-2
- Datapath Compilers 1-2
- Input/Output Cells 1-3

V_{DD}/V_{SS} Rules and Guidelines 1-6

Power Dissipation 1-7

Propagation Delays 1-9

Delay Model 1-13

Testability Design Methodology 1-14

Maximum Fanouts 1-15

Product Line-Up 1-22

Packages 1-22

Dedicated Corner V_{DD}/V_{SS} Pads 1-23

External Design Interface Considerations 1-23

Crystal Oscillator Considerations 1-29

LIBRARY DESCRIPTION

STD80 and STDM80 are 5V and 3.3V 0.5μm CMOS standard cell libraries supporting triple- and double-layer metal interconnections provided by Samsung Electronics.

Every types of internal macrocells and input/output buffers are contained in these cell libraries.

With the regard to the current increase of power mixture, 5V-to-3.3V and 3.3V-to-5V convertible cells having a level shifter inside are included in these libraries. In addition, the other interface (CMOS, TTL and Schmitt trigger) cells are fully equipped for your wide selection.

Various kinds of macrofunctions, megafunctions, memory and datapath compilers may satisfy the complicated design requirements. Moreover, core & megafunction cells such as MPU and DSP, and analog cells are under development.

We ensure the product reliability by preventing any possible noise, ESD and latch-up efficiently.

Every work operation in a design flow has been systematized and automated, and each stage is designed to go through enough reviews and verifications. It makes the design work easier and faster, and also prevents any errors or mistakes possible through a design flow.

FEATURES

- ❑ STD80: 5volt standard cell library
  STDM80: 3.3volt standard cell library
- ❑ Mixed 5V/3.3V I/O interface
- ❑ 0.5μm 5V HCMOS technology
  – Double and Triple layer metal options
- ❑ High basic cell usages
  – Up to 700,000 total number of gates
  – Maximum usage: 70% for triple layer metal
  – Maximum usage: 40% for double layer metal
- ❑ High speed
  – 0.2 ns (for STD80) and 0.3ns (for STDM80) delay of 2-input NAND with fanout = 2
- ❑ Fully configurable RAM, ROM and DPRAM
  – Up to 512K-bit ROM available
  – Up to 128K-bit RAM available
  – Up to 64K-bit DPRAM available
- ❑ Configurable Datapath elements available
  – 4 ~ 128-bit bus width
- ❑ Operating Temperature (T_A)
  – Commercial range: 0˚C to +70˚C
  – Industrial range: –40˚C to +85˚C
- ❑ ESD and latch-up protection
  – ESD: 2000V (Min.)
  – Latch-up: 300mA (Min.)
- ❑ Selectable output current drive capability
  – 1/2/4/8/12/16/20/24mA available for 5V
  – 1/2/4/6/8/10/12/16mA available for 3.3V
- ❑ TTL, CMOS, LVTTL, LVCMOS and Schmitt trigger I/Os
- ❑ X-tal oscillators
- ❑ PCI, PCMCIA buffers
- ❑ GTL, NTL, CardBus, SCSI, PECL, USB under-developed
- ❑ Various package options
- ❑ Fully integrated CAD software support
  – Verilog, Viewlogic, Mentor and Synopsys

CAE SUPPORT

STD80/STDM80 supports popular design platforms and environments such as Verilog, Viewlogic, Mentor and Synopsys for front-end logic design capture and simulation, and ArcCell for back-end placement and routing.

For a high simulation accuracy, STD80/STDM80 uses a proprietary delay calculator. Cell delay calculations are based on a matrix of delay parameters for each macrocell, and signal interconnection delay is based on the RC tree analysis.

PRODUCT FAMILY

STD80/STDM80 library include the following design elements:

(a) Internal Macrocells
(b) Input/Output Cells
(c) Macrofunctions
(d) Megafunctions
(e) Memory Compilers
(f) Datapath Compilers
(g) JTAG Boundary Scans.

< Internal Macrocells >

Macrocells are the lowest level of logic functions such as NAND, NOR and flip-flop used for logic designs. There are about 300 different types of internal macrocells. They usually come in two levels of drive strength (1X and 2X).

These macrocells have many levels of representations—logic symbol, logic model, timing model, transistor schematic, HSPICE netlist, physical layout, and placement and routing model.

< Macrofunctions >

Macrofunctions are netlists of logic function which have the complexity of a standard MSI circuit. Macrofunctions are logic building blocks. There are 44 kinds of 74XX (TTL) compatible functions in this library.

< Megafunctions >

Megafunctions are also netlists of logic function, but with a high logic complexity of a standard LSI circuit. Multipliers, barrel shifters, 82XX Intel functions, etc. are supported in this library.

< Memory Compilers>

Memory compilers of STDL80 consist of two ROMs (synchronous contact programmable and synchronous diffusion programmable), three single-port RAMs (synchronous and asynchronous) and three dual-port RAMs (synchronous and asynchronous).

In addition, a Register File and a FIFO are under-developed.

< Datapath Compilers >

Datapath compilers of STD80/STDM80 consist of 16 macro cells (Adder, ALU, Multiplier, etc.) and 14 primitive cells (NAND, NOR, DFF, LATCH, MUX, etc.)

< Input/Output Cells >

There are about one thousand different I/O buffers. Each I/O cell is implemented solely on the basic I/O cell architecture which forms the periphery of the masterslice.

A test logic is provided to enable the efficient parametric (threshold voltage) testing on input buffers including CMOS and TTL level converters, Schmitt trigger input buffers, clock drivers and oscillator buffers. Pull-up and pull-down resistors are optional features.

Three basic types of output buffers (non-inverting, tri-state and open drain) are available in a range of driving capabilities from 1mA to 24mA for 5V drive and 1mA to 16mA for 3.3V drive.Two levels of slew rate controls are provided for each buffer type (except 1mA and 2mA buffers) to reduce output power/ground bus noise and signal ringing, especially in simultaneous switching outputs.

Bi-directional buffers are combinations of input buffers and output buffers (tri-state or open drain) in a single unit. The I/O structure has been fully characterized for ESD protection and latch-up resistance.

For user's convenience, STD80/STDM80 library provides with three options of pull-down and pull-up resistances respectively. They are 50KΩ, 100KΩ, and 200KΩ (The default value is 100KΩ).

I/O Cell Drive Options

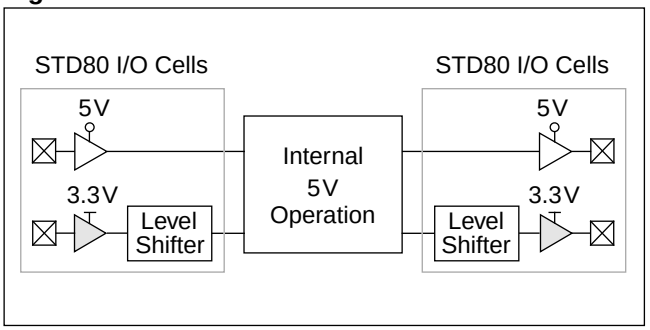
To provide designers with the greater flexibility, each I/O buffer can be selected among various current levels (e.g., 1mA, 2mA, ..., 24mA). The choice of current-level for I/O buffers affects their propagation delay and current noise.

The slew rate control helps decrease the system noise and output signal overshoot/undershoot caused by the switching of output buffers. The output edge rate can be slowed down by selecting the high slew rate control cells. STD80/STDM80 provides three different sets of output slew rate controls. Only one I/O slot is required for any slew rate control options.

5V/3.3V Mixed I/O Cells

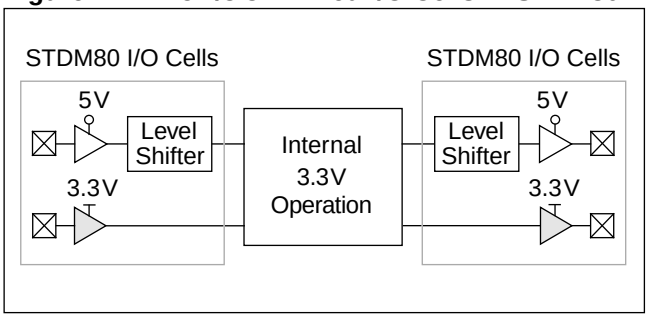
When designers intend to make transitions from 5V supplies to low voltage system, STD80 offers a solution of interfacing problems encountered in mixed 5V/3V environment. This solution provides great flexibility to different devices communicating each other. PCI and PCMCIA buffers are also available in this solution. You can see this in the following figure.

Figure 1-1. 5V/3.3V Mixed I/O Cells in STD80



In STDM80, level shifters are available to provide internal 3V core with great flexibility when it interfaces with a 5V device. Refer to the figure below.

Figure 1-2. 5V/3.3V Mixed I/O Cells in STDM80



PCI Buffers

In addition to input, output, bi-directional, slew rate controlled and Schmitt trigger I/O buffers, SEC ASIC now offers PCI (Peripheral Component Interconnect) I/O buffers. PCI is expected to be better suited to the more complex and feature-rich design than the existing local bus standards. 5V, 3.3V and Universal PCI buffers are included in the library.

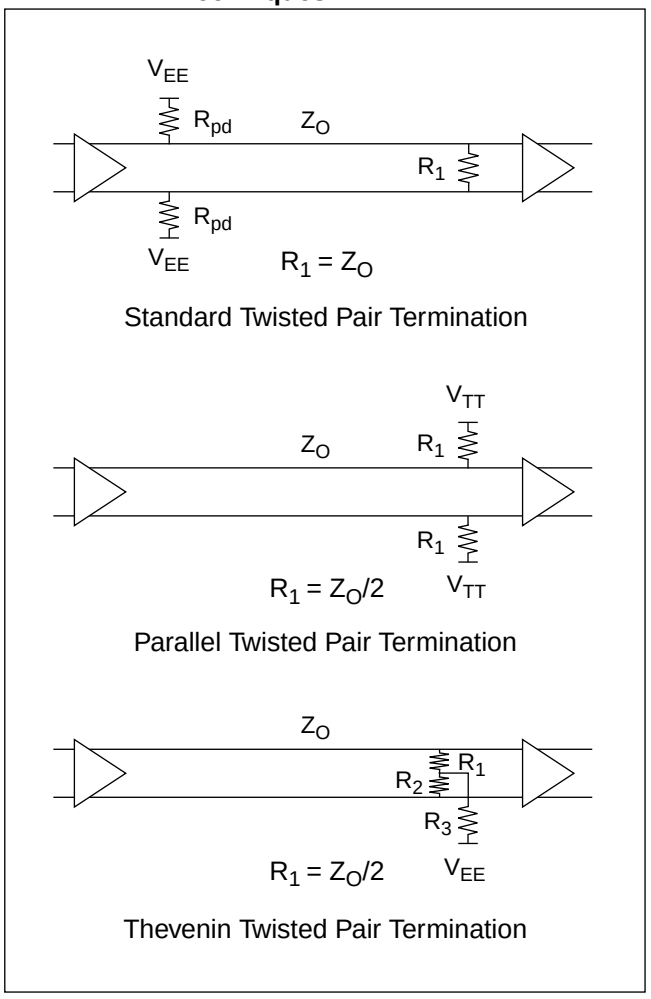
PECL

SEC ASIC's PECL (Positive Emitter Coupled Logic) buffer having 155MHz operating frequency is suited to ATM interface. It supports two voltage source modes; 5V and 3.3V.

The voltage swing level is about 0.8V, being similar to that of ECL, and the external terminator is needed. Its main features are the same as ECL; low noise, high speed and single ended/differential function.

In case of differential transmission, the external terminator is shown in the following figure.

Figure 1-3. Twisted Pair Termination Techniques

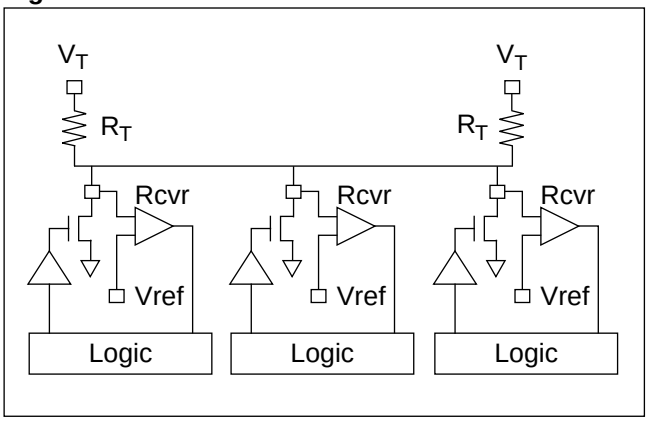


GTL (Gunning Transceiver Logic)

GTL and GTL+ interface I/Os are useful for implementing highly reliable system, satisfying fast and low-powered signal transfers and reducing noise in a switching circuitry.

In all 0.5μm cell libraries in SEC ASIC, GTL interface is fully supported.

Figure 1-4. GTL Interface

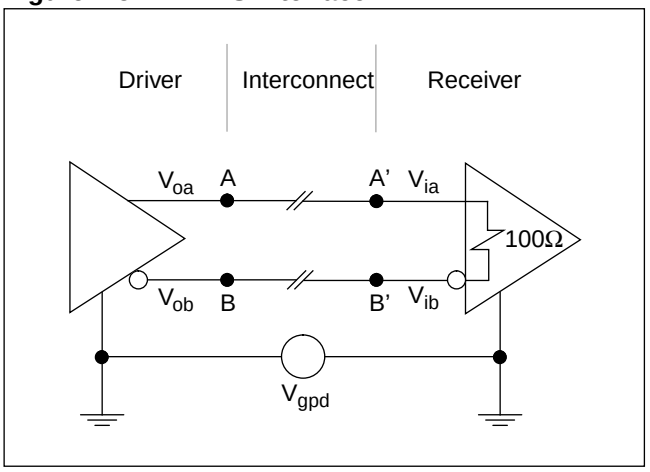


LVDS

LVDS (Low Voltage Differential Signals) buffer for SCI (Scalable Coherent Interface) system, shown in the following figure, enables high speed I/O interface with SEC ASIC's high frequency PLL.

This structure is designed for high speed point-to-point unidirectional interface. Its main characteristics are much the same as ECL's differential mode; low noise generation, high noise immunity and low level signalling.

Figure 1-5. LVDS Interface



USB (Universal Serial Bus)

Various kinds of peripheral equipments such as mouse, joy stick, keyboard, modem, scanner and printer improve the power of a computer. However, it is not easy to connect and use them properly in the computer.

USB specification established late in 1995 is a good solution for this problem, providing facile method of an expansion. SEC ASIC offers USB interfaced buffers in the 0.5μm technology.

USB is applicable only in STD cells.

Figure 1-6. Full Speed Device Cable and Resistor Connections

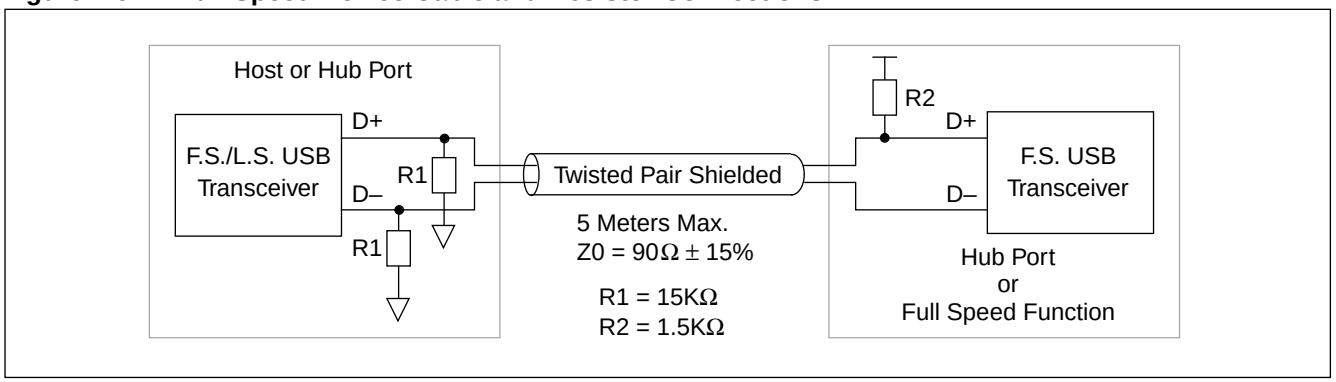
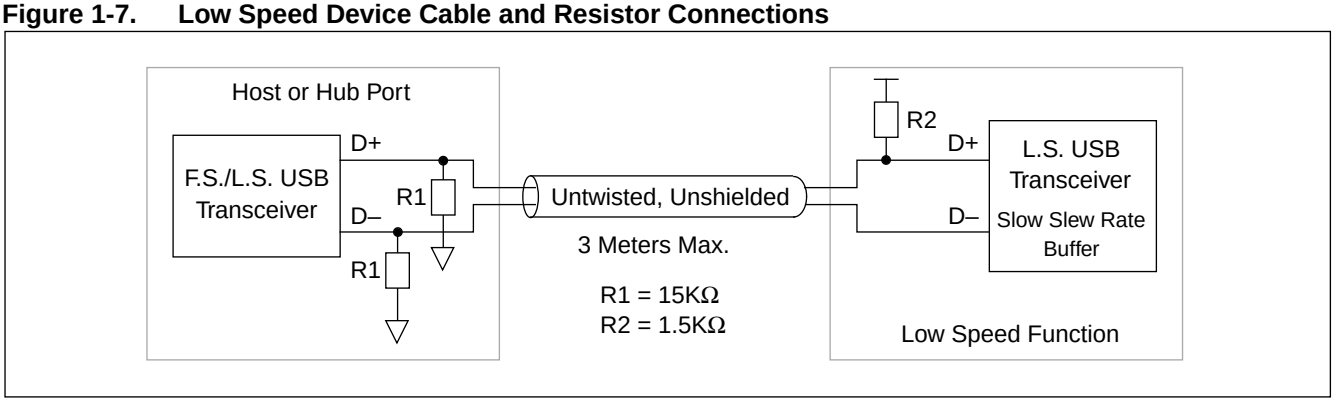


Figure 1-7. Low Speed Device Cable and Resistor Connections



LVTTL/LVCMOS

Low Voltage TTL and Low Voltage CMOS I/O buffers have various kinds of applications as normal TTL and CMOS I/O sets. Their key features are low voltage swing and low noise. Input voltage level is 5V compatible. Output high voltage is 2.4V ~ 3.5V in LVTTL and VDD–0.2V in LVCMOS.

SCSI

SCSI is widely used to extend peripherals, requires external terminator. SEC ASIC supports SCSI-3 fast-20 parallel interface and SCSI-3 parallel interface only in STD80. Both of them have fail-safe function. SCSI buffer is two times as big as normal buffers.

PCMCIA

PCMCIA (Personnel Computer Memory Card Industry Association) buffers guarantees an accurate logic level even when the internal or external voltage source level of a chip changes between 5V and 3.3V.

This buffers are designed for 16-bit external extension card of notebook PC.

CardBus Buffers

CardBus I/O buffers have 3.3V 32-bit bus width and 33MHz of transmission speed. They are for external CardBus type of extension card of notebook PC.

V_{DD}/V_{SS} RULES AND GUIDELINES

There are three types of V_{DD} and V_{SS} in STD80/STDM80, each with its related bus and pad cells. To support the use of mixed voltage, two different V_{DD} types are needed for 5V and 3.3V respectively.

(1) Core logic
– VSSI, VDD5I (for 5V)
(2) Input buffers (usable when requested)
– VSSP, VDD5P (for 5V), VDD3P (for 3.3V)
(3) Output buffers
– VSSO, VDD5O (for 5V), VDD3O (for 3.3V)

The number of V_{DD} and V_{SS} pads required for a specific design depends on the following factors:

- Number of input and output buffers
- Number of simultaneous switching inputs
- Number of simultaneous switching outputs
- Number of used gates and simultaneous switching gates
- Operating frequency of the design.

Core Logic V_{SS} Bus and VSSI Pad Allocation Guidelines

The purpose of these guidelines is to ensure that V_{DD}/V_{SS} bounce caused by a simultaneous gate switching is kept to minimum. The voltage bounce on the power bus can have a negative impact on a gate-switching speed and even on the functionality of macrocells like flip-flops and latches in an extreme case.

Because of variations in package inductance, the number of V_{DD}/V_{SS} pads required for a specific design is the function of the operating frequency of a chip, i.e., designs operating at high frequency should use more V_{DD}/V_{SS} pads.

- V_{DD} bus width and pad requirements are half of V_{SS}.
- V_{DD}/V_{SS} buses and pads should be distributed evenly in the core and on all sides of the chip.
- Whenever possible, at least one VSSI pad should be used on each side of the chip.
- The total number of core logic V_{DD} pads required is half of VSSI.

The number of VSSI pads required for a design can be calculated from the following expression:

G x S x F x 2.00e–5

,where
G = Total number of used gates,
S = % of simultaneous switching gates,
F = Switching frequency in MHz.

Input Buffer V_{DD}/V_{SS} Pad Allocation Guidelines

These guidelines ensure that an adequate input threshold voltage margin is maintained during a switching.

- One VSSP is required to support 32 input buffers, and one input buffer V_{DD} can support up to 64 inputs.
- For simultaneous switching inputs, one VSSP pad is required for every 20 inputs, and one input buffer V_{DD} pad for every 40 inputs.
- Input buffer V_{SS}/V_{DD} pads should be placed in such a way that they equally divide the input buffers on either side.

Output Buffer V_{DD}/V_{SS} Pad Allocation Guidelines

The number of VSSO pads required for a device can be calculated from the following expressions.

In 5V

$$\Sigma (I_{OL\ Simultaneous\ switching\ outputs}) / 40 + \Sigma (I_{OL\ Normal\ outputs}) / 64$$

In 3.3V

$$\Sigma (I_{OL\ Simultaneous\ switching\ outputs}) / 50 + \Sigma (I_{OL\ Normal\ outputs}) / 80$$

- The total number of output buffer V_{DD} pads required is half of VSSO.
- Output buffer V_{SS}/V_{DD} pads should be placed in such a way that output buffers are equally divided on either side.

POWER DISSIPATION

Estimation of Power Dissipation in CMOS Circuit

CMOS circuits have been traditionally considered to consume low power since they draw very small amount of current in a steady state. However, the recent revolution in a CMOS technology that allows very high gate density has changed the way the power dissipation should be understood. The power dissipation in a CMOS circuit is affected by various factors such as the number of gates, a switching frequency, the loading on the output of a gate, and so on.

Power dissipation is important when designers decide the amount of necessary power supply current for the device to operate in safety. Propagation delays and a reliability of the device also depend on the power dissipation which determines the temperature at which the die operates. To obtain a high speed and a reliability, designers must estimate the power dissipation of the device accurately and determine the appropriate environments including packages and system cooling methods.

This section describes the concept of two types of power dissipation (static and dynamic) in a CMOS circuit, the method of calculating them in the SEC STD80/STDM80 library, and finally their relationship with a temperature.

Static (DC) Power Dissipation

There are two types of static or DC current contributing to the total static power dissipation in CMOS circuits.

One is the leakage current of the gates resulted by a reverse bias between a well and a substrate region. There is no DC current path from power to ground in a CMOS because one of the transistor pair is always off, therefore, no static current except the leakage current flows through the internal gates of the device. The amount of this leakage current is, however, in the range of tens of nano amperes, which is negligible.

The other is DC current that flows through the input and output buffers when the circuit is interfaced with other devices, especially TTL. The current of pull-up/pull-down transistor included in the input buffers is about 50μA typically, which is also negligible. Therefore, only DC current that the output buffers source or sink has to be counted to estimate the total static power dissipation.

DC power dissipation of TTL output and bi-directional buffers is determined by the following formula:

$$P_{DC_TTL_OUTPUT} = \Sigma(V_{OL} \times I_{OL} \times t_L) + \Sigma((V_{DD} - V_{OH}) \times I_{OH} \times t_H)$$

,where

$t_H = T_{HIGH} / T$,

$t_L + t_H = 1$.

Dynamic (AC) Power Dissipation

When a CMOS gate changes its state, it draws switching current as a result of charging or discharging of a node capacitance, C_L. The energy associated with the switching current for a node capacitance, C_L, is

$$1 / 2 \times (C_L \times V_{DD}^2)$$

,where V_{DD} is a power supply voltage.

The switching occurs twice per cycle for periodic signals: once for charging a capacitance and once for discharging it. Hence, the dynamic power dissipation due to the switching current is the energy divided by the clock period and multiplied by the factor of two, or

$$C_L \times V_{DD} \times V_{DD} / T$$

,where T is a clock period.

As shown above, it is quite straight forward to calculate the dynamic power dissipation for a single gate. The dynamic power dissipation for an entire chip is, however, much more complicated to estimate since it depends on the degree of switching activity of the circuit. SEC has found that the degree of switching activity is 20% on the average and recommends to use this number to estimate the total dynamic power dissipation.

Power Dissipation in STD80/STDM80

This section describes the equations on how to estimate the power dissipation in STD80/STDM80. As explained in the previous section, the total power dissipation (P_{TOTAL}) consists of static power dissipation (P_{DC}) and dynamic power dissipation (P_{AC}).

$$P_{TOTAL} = P_{DC} + P_{AC}$$

Since only output buffers contribute to the static power dissipation,

$$P_{DC} = P_{DC_OUTPUT}$$

,where P_{DC} output is the static power dissipated when output buffers source or sink.

The dynamic power dissipation is caused by three components: input buffers (P_{AC_INPUT}), output buffers (P_{AC_OUTPUT}), and internal cells ($P_{AC_INTERNAL}$).

$$P_{AC} = P_{AC_INPUT} + P_{AC_OUTPUT} + P_{AC_INTERNAL}$$

Each term mentioned above is characterized by the following equations:

In STD80,

$P_{DC_OUTPUT} = 150 \times I_{OL} \times N_output$ [µW]
$P_{AC_INPUT} = 23 \times N_input \times F \times S$ [µW]
$P_{AC_OUTPUT} = 25 \times N_output \times F \times S \times C$ [µW]
$P_{AC_INTERNAL} = 2.3 \times N_internal \times F \times S$ [µW]

In STDM80,

$P_{DC_OUTPUT} = 150 \times I_{OL} \times N_output$ [µW]
$P_{AC_INPUT} = 9.8 \times N_input \times F \times S$ [µW]
$P_{AC_OUTPUT} = 25 \times N_output \times F \times S \times C$ [µW]
$P_{AC_INTERNAL} = 1.2 \times N_internal \times F \times S$ [µW]

,where
I_{OL} is source and sink current of output buffers in mA,
N_output is the number of output buffers used,
N_input is the number of input buffers used,
N_internal is the number of internal cells used,
F is the maximum operation frequency in MHz,
S is the estimated degree of a switching activity (typically 0.2),
C is the output load capacitance in pF.

Temperature and Power Dissipation

The total power dissipation, P_{TOTAL} can be used to find out the device temperature by the following equation:

$$\theta_{JA} = (T_J - T_A) / P_{TOTAL}$$

,where
θ_{JA} is the thermal impedance,
T_J is the junction temperature of the device,
T_A is the ambient temperature.

Thermal impedances of the SEC packages are given in the following table. The junction temperature, obtained by multiplying P_{TOTAL} by the appropriate θ_{JA} and adding T_A, determines the derating factor for the propagation delays and also indicates the reliability measures. Hence, designers can achieve the desired derating factor and reliability targets by choosing appropriate packages and system cooling methods.

Table 1-1. Thermal Impedances of SEC Packages

	QFP						
Pin Number	**64**	**80**	**100**	**120**	**160**	**208**	**240**
θ_{JA} [°C/W]	60	60	60	50	50	40	40

Maximum Junction Temperature (T_J)

The allowable maximum junction temperatures for plastic and ceramic packages are as follows:

Junction temperature for plastic package ≤ 125°C
Junction temperature for ceramic package ≤ 150°C.

PROPAGATION DELAYS

Interconnection wire length, temperature and supply voltage are the chief factors affecting propagation delays.

Wire Length Load

The loading due to interconnection wire length can be estimated with the following expression. The result is given in terms of number of equivalent standard loads.

$$C_{WL} = C_{FO} \times (0.049 \times \sqrt{A} + 0.48) + 0.079 \times \sqrt{A} + 0.33$$

,where

C_{FO} = Number of fanouts in a standard load,

A = Area of block size in mm^2,

C_{WL} = Number of equivalent standard loads due to an interconnection,

e.g.,

C_{FO} = 7 (standard load),

A = 25mm^2,

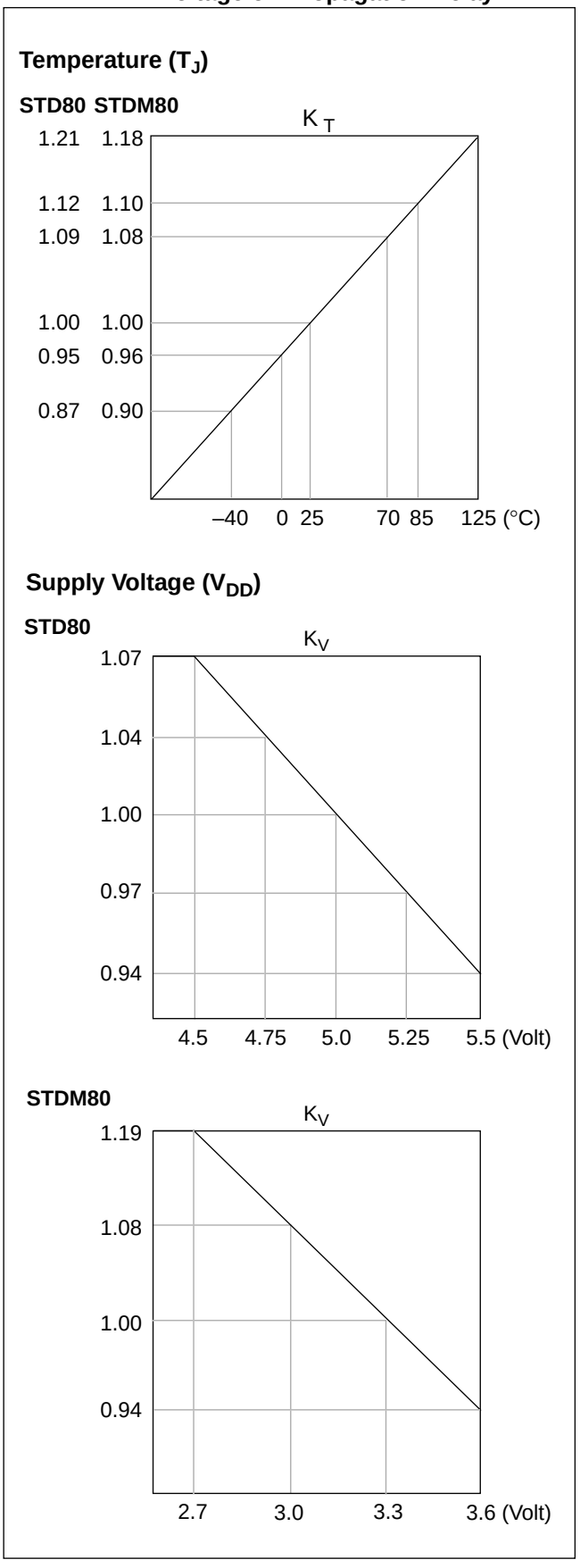
C_{WL} = 5.8 (standard load).

Temperature and Supply Voltage

The next figure describes propagation delay correction factors (K_T, K_V) as a function of on-chip junction temperature (T_J) as well as supply voltage (V_{DD}). As a result of increasing CMOS power dissipation, ambient and junction temperature are generally not the same.

The temperature of the die inside the package (junction temperature, T_J), is calculated using chip power dissipation and the thermal resistance to ambient temperature (θ_{JA}) of the package. Information on package thermal performance can be obtained from SEC application engineers.

Figure 1-8. Effect of Temperature and Supply Voltage on Propagation Delay



Best and Worst Case Conditions

A circuit should be designed to operate properly within a given specification level, either commercial or industrial. It is recommended that circuits be simulated for best case, normal case, and worst case conditions at each specification level.

The following expressions also allow for the effect of process variation on circuit performance.

Best case:

$T_{BC} = K_{PBC} \times K_T \times K_V \times T_{NOM} = K_{BC} \times T_{NOM}$

Worst case:

$T_{WC} = K_{PWC} \times K_T \times K_V \times T_{NOM} = K_{WC} \times T_{NOM}$

,where

T_{BC} = Best case propagation delay

T_{WC} = Worst case propagation delay

T_{NOM} = Normal propagation delay

($T_J = 25^oC$, $V_{DD} = 5V$ and typical process)

K_{PWC} = Worst case process correction factor

K_{PBC} = Best case process correction factor

With above equations, we can calculate the multipliers of K_{WC} and K_{BC} as follows.

Table 1-2. STD80 best case delay

Application	Best case delay			
	Parameter			K_{BC}
	V_{DD}	T_J	Proc.	
Industrial	5.5V	–40 ^{o}C	Min.	0.51
Commercial	5.25V	0 ^{o}C	Min.	0.56

Table 1-3. STD80 worst case delay

Application	Worst case delay			
	Parameter			K_{WC}
	V_{DD}	T_J	Proc.	
Industrial	4.5V	125 ^{o}C	Max.	1.77
Commercial	4.75V	115 ^{o}C	Max.	1.69

Table 1-4. STDM80 best case delay

Application	Best case delay			
	Parameter			K_{BC}
	V_{DD}	T_J	Proc.	
Industrial	3.6V	–40 ^{o}C	Min.	0.49
Commercial	3.6V	0 ^{o}C	Max.	0.52

Table 1-5. STDM80 worst case delay

Application	Worst case delay			
	Parameter			K_{WC}
	V_{DD}	T_J	Proc.	
Industrial	2.7V	125 ^{o}C	Max.	1.97
Commercial	3.0V	115 ^{o}C	Max.	1.77

Derating factors of STD80/STDM80

The multipliers can be applied to nominal delay data in order to estimate the effects of supply voltage, temperature and process. Nominal data are provided for conditions of $V_{DD} = 5V$, $T_A = 25°C$ and typical process.

The derating factors of STD80/STDM80 are as follows.

Table 1-6. STD80/STDM80 process derating factor

Process Factor (K_P)	Slow	Typ.	Fast
	1.40	1.00	0.60

Table 1-7. STD80 temperature derating factor

Temp. (^{o}C)	125	85	70	25	0	–40
K_T	1.21	1.12	1.09	1.00	0.95	0.87

Table 1-8. STDM80 temperature derating factor

Temp. (^{o}C)	125	85	70	25	0	–40
K_T	1.18	1.10	1.08	1.00	0.96	0.90

Table 1-9. STD80 voltage derating factor (K_V)

Voltage (V)	5.5	5.25	5	4.75	4.5
K_V	0.94	0.97	1.00	1.04	1.07

Table 1-10. STDM80 voltage derating factor (K_V)

Voltage (V)	3.6	3.3	3.0	2.7
K_V	0.94	1.00	1.08	1.19

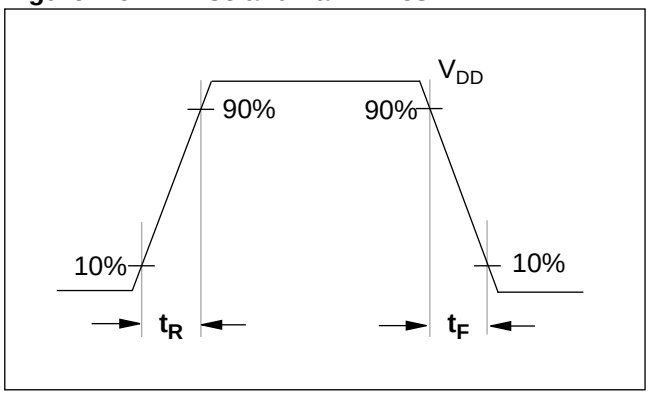
Timing Parameters

This section discusses issues involving timing parameters for primitive cells.

RISE / FALL TIMES

The definition of rise time (t_R) and fall time (t_F) is shown in the following figure.

Figure 1-9. Rise and Fall Times

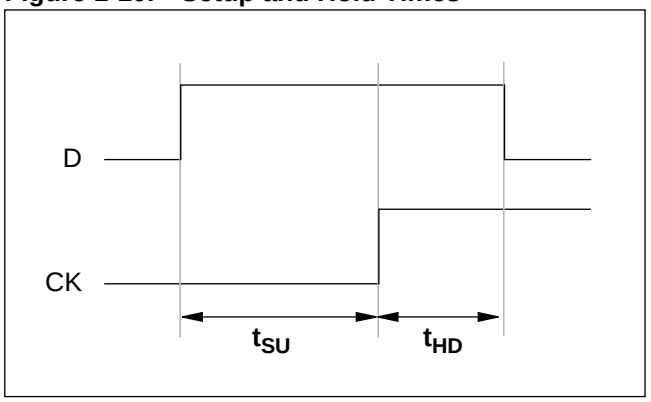


SETUP / HOLD TIMES

Setup time (t_{SU}) is a minimum period in which the input data to a flip-flop or a latch must be stable before the active edge of the clock occurs. Hold time (t_{HD}) is a minimum period in which the input data to a flip-flop or a latch must remain stable after the active edge of the clock has occurred.

The next figure shows the relationship between setup and hold times for a standard flip-flop triggered on the rising edge of the clock.

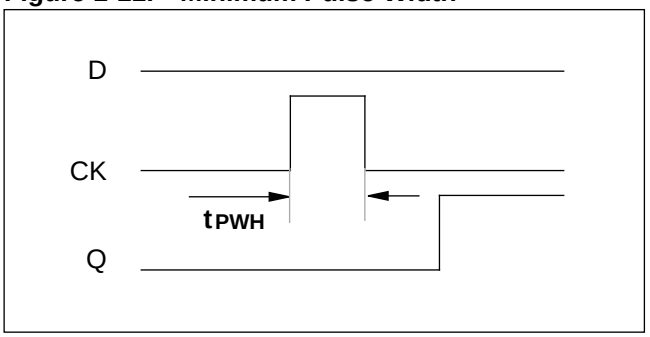
Figure 1-10. Setup and Hold Times



MINIMUM PULSE WIDTHS

Minimum clock pulse widths (t_{PWH}, t_{PWL}) are the time intervals during a clock signal is high or low, so that it ensures proper operation of a flip-flop or a latch.

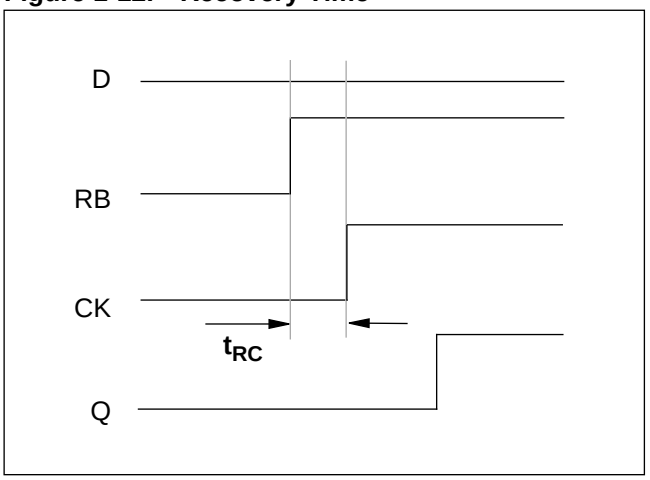
Figure 1-11. Minimum Pulse Width



RECOVERY TIMES

Recovery time (t_{RC}) is the minimum time after an asynchronous pin is disabled that an active clock edge will propagate data from input to output. If the active edge or clock occurs before the specified recovery time, the input data will not propagate.

Figure 1-12. Recovery Time

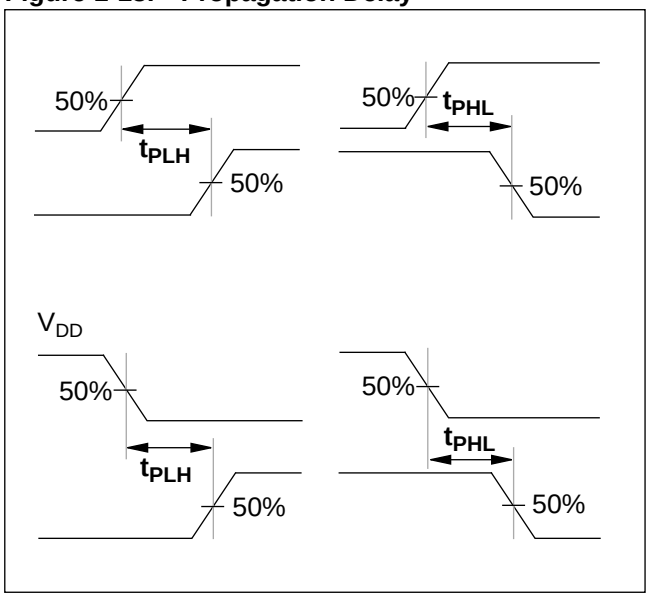


PROPAGATION DELAYS

A delay for a macrocell is considered to be a rising delay (t_{PLH}) if the signal on the output pin is rising. For a rising input and a rising output, the rising delay is the interval between the times the input becomes 50% of supply voltage (V_{DD}) and the output becomes 50% of V_{DD}.

If the input is falling and the output is rising, the rising delay is the interval between the times the input falls to 50% of V_{DD} and the output rises to 50% of V_{DD}. The converse is true for a falling delay (t_{PHL}).

Figure 1-13. Propagation Delay

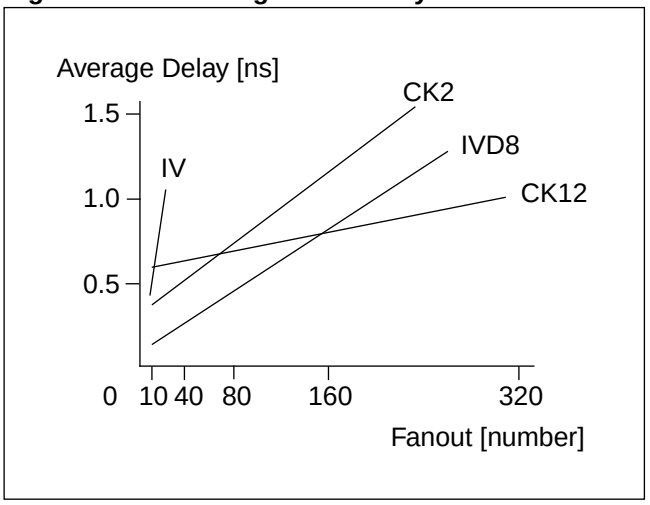


Proper Use of Buffers

Figure 1-14. Average Gate Delay in STD80 shows the average propagation delays of an internal inverter (IV), an 8X inverter (IVD8), a normal clock driver (CK2), and a high clock driver (CK12) in STD80.

Note that transistors uses in I/O slots are larger and have ON channel resistance about one order of magnitude lower than those of the N and P channel transistors in primitive cells. This makes them likely candidates for use as buffers for high fanout signals. For example, CK2 and CK12 buffers require one I/O slot location. Both can be used as high fanout internal buffers.

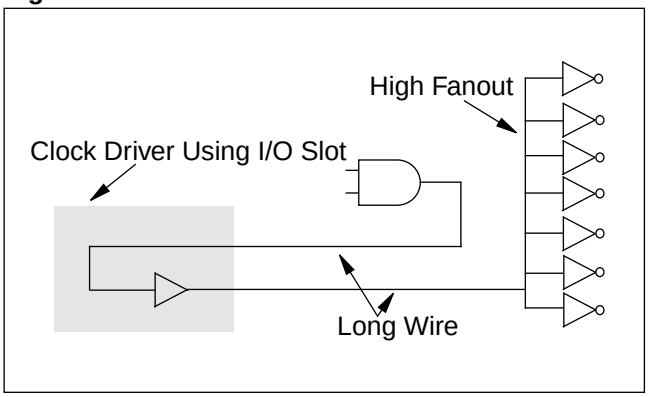
Figure 1-14. Average Gate Delay in STD80



One caution, emphasized in Figure 1-15. Use of I/O Slot for an Internal Buffer, shows that if you route to a buffer that uses an I/O slot from an internal element and back into internal logic, the additional wiring needed could increase propagation delays materially. Higher drive strength internal cells may be more appropriate than I/O slot buffers.

Realize also that using I/O slot cells for internal buffering removes those locations for use as external I/Os and uses two wiring channels, thereby increasing routability congestion on masterslice products.

Figure 1-15. Use of I/O Slot for an Internal Buffer



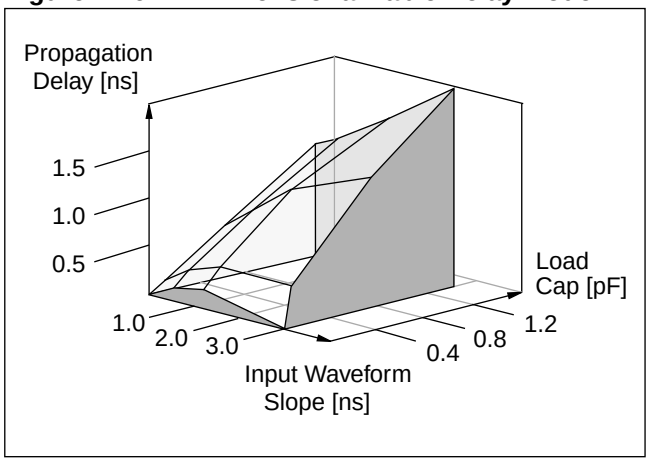
DELAY MODEL

The ASIC timing characteristics consist of the following components:

- Cell propagation delay from input to output transitions based on input waveform slope, fanout loads and distributed interconnection wire resistance and capacitance.
- Interconnection wire delay across the metal lines.
- Timing requirement parameters such as setup time, hold time, recovery time, skew time, minimum pulse width, etc.
- Derating factors for junction temperature, power supply voltage, and process variations.

Timing model for STD80/STDM80 focuses on how to characterize cell propagation delay time accurately. To accomplish this goal, 2-dimensional table look-up delay model has been adopted. The index variables of this table are input waveform slope and output load capacitance. See the figure below. SEC ASIC design automation system supports an n-dimensional table model even though we adopted 2-dimensional model for our 0.5μm cell-based products.

Figure 1-16. 2-Dimensional Table Delay Model



The Table 1-11. Table Delay Model Example shows an example of this model for 2-input NAND cell. The data in this table are high-to-low transition delay times from one of the two input pins to output pin. The number of points and values of the index variables can differ for each cell.

Table 1-11. Table Delay Model Example

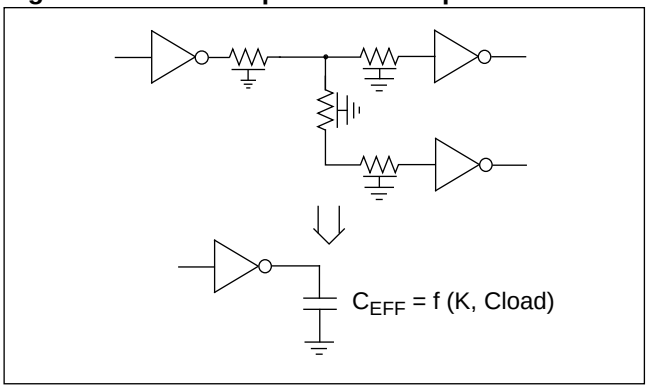
Slope \ Cap.	0.03	0.13	0.53	1.32
0.10	0.07	0.14	0.42	0.97
0.30	0.08	0.17	0.45	1.02
0.80	0.06	0.18	0.51	1.07
1.60	0.01	0.18	0.60	1.18

Notice that 4-by-4 table is used. Delay values between grid points and beyond this table are determined by linear interpolation and extrapolation methods. This general table delay model provides great flexibility as well as high accuracy since extensive software revisions are not required when a cell library is updated. The other timing components such as interconnection wire delay, timing requirement parameters and derating factors are characterized in a commonly-accepted way in industry.

The delay time due to the interconnection wire can be separated into two components. One is the signal propagation delay time across the metal lines. This delay time component is computed through conventional RC analysis based on $\prod$-model. The other is an additional delay on the driving cell due to the wire load. The traditional way to compute this is based on the lumped capacitance model, ignoring wire resistance.

For sub-micron technology, this approximation cannot be accepted any more. The wire resistance has a shielding effect on the driving cell from load capacitances. An effective capacitance C_{EFF}, a single capacitance approximating distributed interconnection wire resistance and capacitance, is derived, as illustrated in the following figure. The compensation factor K, extracted for each cell, is a function of the length of interconnection wires and the layout topology. All these effects are merged to determine the effective capacitance and this value is used as an index of the table delay model.

Figure 1-17. Concept of Effect Capacitance



The figure below summarizes the features of SEC ASIC's delay model.

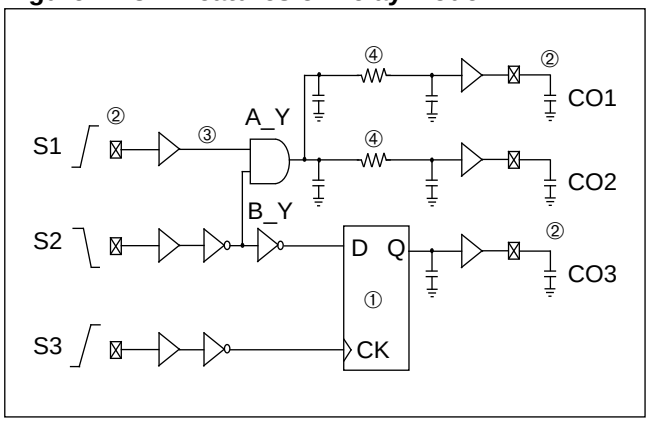
① 2-dimensional table delay model for output loading and input waveform slope effects is used. The slopes (t_R, t_F) and delay times (t_{PLH}, t_{PHL}) of all cell instances are calculated recursively.

② The input waveform slope of each primary input pad and the loading capacitance of each primary output pad can be assigned individually or by default.

③ Pin to pin delays of cells and interconnection wires are supported.

④ The effect of distributed interconnection wire resistance and capacitance on cell delay is analysed using the effective capacitance concept.

Figure 1-18. Features of Delay Model



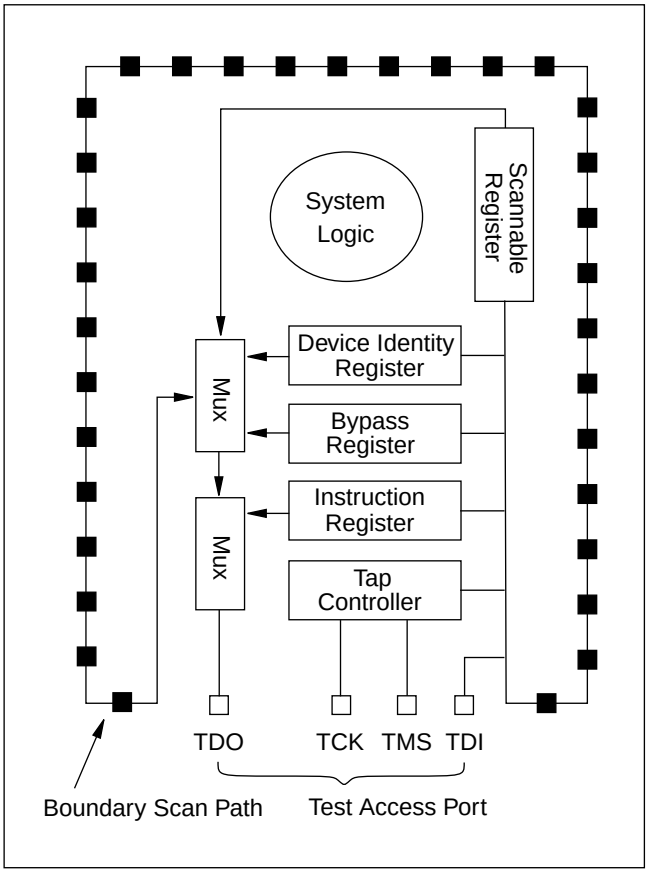
TESTABILITY DESIGN METHODOLOGY

Scan Design

- Multiplexed scan flip-flop that minimizes the area or delay overhead needed to implement scan design
- Automated design rules checking, scan insertion, and test pattern generation
- High fault coverage on synchronous designs

Boundary-Scan

- IEEE Std 1149.1
- 5 types of JTAG boundary-scan cells
- Boundary-Scan Description Language (BSDL) description for board testing
- Combination with internal scan design



MAXIMUM FANOUTS

Internal Macrocells

The maximum fanouts for STD80/STDM80 primitive cells are as follows. Note that these fanout limitation values are calculated when the rise and fall times of the input signal is 0.44ns (STD80)/0.39ns (STDM80). Depending on the rise and fall times, the maximum fanout limitations can be varied case by case.

In the following table the maximum fanout values for all pins of STD80/STDM80 internal macrocells are listed.

Table 1-12. Maximum Fanouts of Internal Macrocells (When t_R/t_F = 0.44ns (STD80)/0.39ns (STDM80))

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
Logic Cells			
AD2	Y	49	28
AD2D2	Y	106	59
AD3	Y	49	28
AD3D3	Y	161	84
AD4	Y	49	28
AD4D2	Y	105	58
AD5	Y	38	17
AD5D2	Y	78	34
ND2	Y	45	23
ND2D2	Y	95	48
ND3	Y	30	15
ND3D2	Y	63	30
ND4	Y	23	11
ND4D2	Y	47	22
ND5	Y	18	7
ND5D2	Y	36	16
ND6	Y	49	28
ND6D2	Y	104	55
ND8	Y	49	28
ND8D2	Y	105	56
NR2	Y	40	17
NR2D2	Y	87	37
NR3	Y	25	11
NR3D2	Y	54	23
NR4	Y	18	7
NR4D2	Y	38	15
NR5	Y	49	28
NR5D2	Y	104	59
NR6	Y	49	28
NR6D2	Y	104	58
NR8	Y	49	28
NR8D2	Y	104	58
OR2	Y	49	28
OR2D2	Y	104	55
OR3	Y	49	26
OR3D3	Y	147	71
OR4	Y	43	22
OR4D2	Y	89	44
OR5	Y	40	21
OR5D2	Y	89	45
XN2	Y	49	27
XN2D2	Y	103	54
XN3	Y	47	25
XN3D3	Y	134	65
XO2	Y	49	28
XO2D2	Y	102	55
XO3	Y	47	25
XO3D3	Y	134	65
AO21	Y	30	15
AO21D2	Y	64	31
AO211	Y	22	9
AO211D2	Y	44	18
AO22	Y	28	13
AO22D2	Y	57	27
AO22A	Y	27	13
AO22D2A	Y	55	27
AO222	Y	21	8
AO222D2	Y	105	59
AO222A	Y	26	10
AO222D2A	Y	52	21
AO33	Y	18	7
AO33D2	Y	106	58
AO333	Y	15	4
AO333D2	Y	107	60
OA21	Y	29	15
OA21D2	Y	61	31
OA211	Y	20	9
OA211D2	Y	40	19
OA22	Y	28	14
OA22D2	Y	59	29

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
OA22A	Y	29	15
OA22D2A	Y	59	31
OA2222	Y	49	28
OA2222D2	Y	104	55
DL1D2	Y	105	60
DL1D4	Y	222	113
DL2D2	Y	108	60
DL2D4	Y	219	114
DL3D2	Y	109	61
DL3D4	Y	226	111
DL4D2	Y	110	61
DL4D4	Y	228	110
DL5D2	Y	110	60
DL5D4	Y	228	109
DL10D2	Y	105	53
DL10D4	Y	207	97
IV	Y	53	29
IVD2	Y	114	65
IVD3	Y	175	101
IVD4	Y	231	144
IVD6	Y	324	190
IVD8	Y	403	234
IVA	Y	53	29
IVD2A	Y	114	65
IVD3A	Y	175	101
IVD4A	Y	231	144
IVCD11	Y	51	27
	YN	53	29
IVCD13	Y	47	24
	YN	175	100
IVCD22	Y	117	62
	YN	114	65
IVCD26	Y	101	53
	YN	324	190
IVCD44	Y	259	162
	YN	231	144
IVT	Y	43	23
IVTD2	Y	93	48
IVTD4	Y	177	90
IVTD8	Y	323	179
IVTN	Y	43	22
IVTND2	Y	87	46
IVTND4	Y	173	85

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
IVTND8	Y	336	158
NID	Y	49	28
NID2	Y	106	59
NID3	Y	161	90
NID4	Y	222	121
NID6	Y	331	163
NID8	Y	438	209
NIT	Y	43	23
NITD2	Y	91	47
NITD4	Y	180	96
NITD8	Y	323	203
NITN	Y	43	23
NITND2	Y	88	46
NITND4	Y	176	88
NITND8	Y	324	158
Flip-Flops			
FD1	All Pins	49	28
FD1D2	Q	105	58
	QN	107	60
FD1CS	Q	49	28
	QN	49	27
FD1CSD2	Q	105	58
	QN	104	55
FD1S	All Pins	49	28
FD1SD2	Q	105	58
	QN	106	60
FD1Q	Q	49	28
FD1QD2	Q	107	59
FD1X2	All Pins	49	28
FD1X4	All Pins	49	28
YFD1	Q	49	26
	QN	43	24
YFD1D2	Q	105	53
	QN	90	49
FD2	All Pins	49	28
FD2D2	Q	106	58
	QN	109	60
FD2CS	All Pins	49	27
FD2CSD2	Q	105	58
	QN	106	55
FD2S	All Pins	49	28
FD2SD2	Q	106	58
	QN	108	60

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
FD2Q	Q	49	28
FD2QD2	Q	107	58
FD2X2	All Pins	49	28
FD2X4	All Pins	49	28
YFD2	Q	48	26
	QN	40	21
YFD2D2	Q	103	51
	QN	80	42
FD2T	Q	49	27
	Z	28	15
FD2TD2	Q	106	58
	Z	52	26
FD2TCS	Q	48	27
	Z	28	12
FD2TCSD2	Q	104	57
	Z	52	26
FD2TS	Q	49	27
	Z	28	12
FD2TSD2	Q	106	58
	Z	52	26
FD3	All Pins	49	28
FD3D2	Q	107	58
	QN	107	59
FD3CS	Q	49	28
	QN	49	27
FD3CSD2	Q	106	59
	QN	105	55
FD3S	All Pins	49	28
FD3SD2	Q	106	59
	QN	106	58
FD3Q	Q	49	28
FD3QD2	Q	106	59
FD3X2	All Pins	49	28
FD3X4	All Pins	49	28
YFD3	Q	43	22
	QN	43	24
YFD3D2	Q	89	42
	QN	89	49
FD4	Q	49	27
	QN	49	28
FD4D2	All Pins	106	58
FD4CS	All Pins	49	27

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
FD4CSD2	Q	106	58
	QN	106	55
FD4S	All Pins	49	28
FD4SD2	All Pins	106	58
FD4Q	Q	49	28
FD4QD2	Q	106	59
FD4X2	All Pins	49	28
FD4X4	Qn	49	27
	QNn	49	28
YFD4	Q	43	22
	QN	39	20
YFD4D2	Q	88	41
	QN	80	42
FD5	All Pins	49	28
FD5D2	Q	105	60
	QN	106	59
FD5S	All Pins	49	28
FD5SD2	Q	105	58
	QN	106	59
FD5X4	All Pins	49	28
FD6	All Pins	49	28
FD6D2	Q	105	58
	QN	106	61
FD6S	All Pins	49	28
FD6SD2	Q	106	58
	QN	108	60
FD7	All Pins	49	28
FD7D2	Q	106	59
	QN	106	58
FD7S	All Pins	49	28
FD7SD2	All Pins	106	58
FD8	Q	49	27
	QN	49	28
FD8D2	Q	106	58
	QN	105	58
FD8S	All Pins	49	28
FD8SD2	Q	106	59
	QN	106	58
FDS2	All Pins	59	28
FDS2D2	Q	105	58
	QN	106	60
FDS2CS	Q	49	28
	QN	49	27

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
FDS2CSD2	Q	105	58
	QN	105	55
FDS2S	All Pins	49	28
FDS2SD2	Q	106	60
	QN	105	59
FDS3	All Pins	49	28
FDS3D2	Q	106	60
	QN	105	59
FG1	All Pins	49	28
FG1X4	All Pins	49	28
FG2	All Pins	49	28
FG2X4	All Pins	49	28
FJ1	All Pins	49	28
FJ1D2	Q	105	56
FJ1D2	QN	104	58
FJ1S	Q	50	28
	QN	49	28
FJ1SD2	Q	105	56
	QN	107	59
FJ2	Q	50	28
	QN	49	28
FJ2D2	Q	105	57
	QN	106	59
FJ2S	Q	50	28
	QN	49	28
FJ2SD2	Q	106	56
	QN	109	61
FJ4	Q	50	28
	QN	49	27
FJ4D2	Q	105	56
	QN	106	58
FJ4S	Q	50	28
	QN	49	28
FJ4SD2	Q	106	56
	QN	106	58
FT2	All Pins	49	28
FT2D2	Q	106	57
	QN	108	60
FT3	All Pins	49	28
FT3D2	Q	107	59
	QN	106	58
Latches			
LD1	All Pins	49	28

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
LD1D2	Q	106	60
	QN	105	58
LD1S	All Pins	49	28
LD1SD2	Q	106	60
	QN	106	58
LD1Q	Q	49	28
LD1QD2	Q	104	59
LD1X4	All Pins	49	28
LD1X4D2	Qn	106	59
	QNn	106	58
YLD1	Q	43	24
	QN	51	28
YLD1D2	Q	89	50
	QN	114	61
LD1A	Q	43	23
LD1B	QN	15	5
	ZN	43	23
LD2	All Pins	49	28
LD2D2	Q	105	58
	QN	108	60
LD2Q	Q	49	28
LD2QD2	Q	107	59
YLD2	Q	42	22
	QN	44	22
YLD2D2	Q	44	23
	QN	96	47
LD3	All Pins	49	28
LD3D2	Q	108	60
	QN	106	58
LD4	Q	49	28
	QN	49	27
LD4D2	Q	107	58
	QN	105	58
LD5	All Pins	49	28
LD5D2	Q	106	59
	QN	105	58
LD5S	All Pins	49	28
LD5SD2	Q	106	59
	QN	105	58
LD5X4	All Pins	49	28
LD5X4D2	Qn	106	59
	QNn	106	58
LD6	All Pins	49	28

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
LD6D2	Q	106	58
	QN	108	60
LD7	All Pins	49	28
LD7D2	Q	108	60
	QN	106	58
LD8	Q	49	28
	QN	49	27
LD8D2	Q	107	58
	QN	105	58
LDS2	All Pins	49	28
LDS6	All Pins	49	28
LS0	All Pins	39	20
LS0D2	All Pins	78	40
LS1	All Pins	18	8
LS2	All Pins	39	20
Bus Holder			
BUSHOLDER	Y	10,000	10,000
Internal Clock Drivers			
CK2	Y	Fig 1-19 (a)	Fig 1-20 (a)
CK4	Y	Fig 1-19 (b)	Fig 1-20 (b)
CK6	Y	–	Fig 1-20 (c)
CK8	Y	Fig 1-19 (c)	Fig 1-20 (d)
CK12	Y	Fig 1-19 (d)	–
Decoders			
DC4	All Pins	49	28
DC4I	YN(0/2)	43	23
	YN(1/3)	45	23
DC8I	All Pins	30	15
Adders			
FA	S	49	28
	CO	49	27
FAD2	S	103	55
	CO	103	54
HA	S	49	27
	CO	49	28
HAD2	S	103	54
	CO	106	59
Multiplexers			
MX2	Y	49	28
MX2D3	Y	152	76
MX2X4	All Pins	49	28
YMX2	Y	49	28
YMX2D2	Y	102	59

Cell Name	Output Pin	Maximum Fanout	
		STD80	STDM80
MX2I	YN	28	13
MX2ID2	YN	104	59
MX2IA	YN	28	13
MX2ID2A	YN	104	59
MX2IX4	All Pins	28	13
MX3I	YN	49	28
MX3ID2	YN	104	59
MX4	Y	48	26
MX4D2	Y	96	48
YMX4	Y	49	27
YMX4D2	Y	102	33
MX5	Y	49	27
MX5D2	Y	102	55
MX8	Y	45	22
MX8D2	Y	86	41
YMX8	Y	49	27
YMX8D2	Y	102	53

I/O Cells

The maximum fanouts for 5V and 3.3V I/O cells are as follows when the rise and fall times of the input signal is 0.40ns.

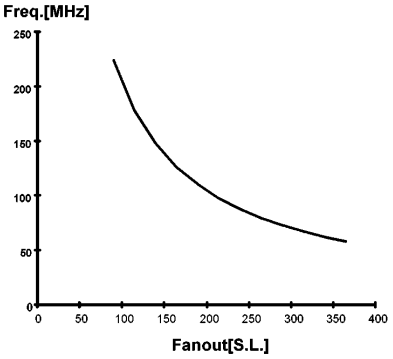
The graphs for fanout vs. frequency curve of STD80/STDM80 internal/input clock drivers are shown in the next page.

Table 1-13. Maximum Fanouts of I/O Cells (When t_R/t_F = 0.40ns)

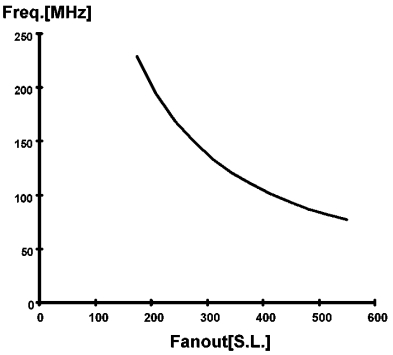
Cell Name	Output Pin	Maximum Fanouts	
		STD80	STDM80
PIC	PO	91	42
	Y	231	137
PICD	PO	92	42
	Y	237	141
PICU	PO	91	42
	Y	240	130
PIL PILD	PO	91	–
	Y	277	–
PILU	PO	91	–
	Y	281	–
PIS	PO	91	42
	Y	182	181
PISD	PO	91	42
	Y	179	150
PISU	PO	91	42
	Y	179	206
PITb	PO	91	–
	Y	180	–
PLIC	PO	69	–
	Y	293	–
PLICD	PO	69	–
	Y	317	–
PLICU	PO	69	–
	Y	302	–
PLIS	PO	69	–
	Y	348	–
PLISD	PO	69	–
	Y	361	–
PLISU	PO	69	–
	Y	246	–
PHIC	PO	–	34
	Y	–	141
PHICD	PO	–	34
	Y	–	143
PHICU	PO	–	34
	Y	–	137
PHIL	PO	–	34
	Y	–	136
PHILD	PO	–	34
	Y	–	156
PHILU	PO	–	34
	Y	–	135
PHIS	PO	–	34
	Y	–	131
PHISD	PO	–	34
	Y	–	144
PHISU	PO	–	34
	Y	–	145
PHIT PHITD	PO	–	34
	Y	–	144
PHITU	PO	–	34
	Y	–	148
PSCKDab2	Y	Fig 1-19 (a)	Fig 1-20 (a)
PSCKDab4	Y	Fig 1-19 (b)	Fig 1-20 (b)
PSCKDab6	Y	–	Fig 1-20 (c)
PSCKDab8	Y	Fig 1-19 (c)	Fig 1-20 (d)
PSCKDab12	Y	Fig 1-19 (d)	–
PSOSCK1 PSOSCK16	PADY	9	6
	YN	36	25
PSOSCK2 PSOSCK26	PADY	94	62
	YN	319	225
PSOSCM1 PSOSCM16	PADY	1097	778
	YN	888	633
PSOSCM2 PSOSCM26	PADY	1097	778
	YN	888	633
PSOSCM3 PSOSCM36	PADY	2194	1548
	YN	1596	1136
PSOSCM4 PSOSCM46	PADY	4356	3010
	YN	2389	1699
PSOSCM5 PSOSCM56	PADY	6592	4508
	YN	1257	894
PSOSCM6 PSOSCM66	PADY	8923	6054
	YN	4750	3369

Figure 1-19. Fanout (SL) vs. Frequency Curve of STD80 Clock Drivers

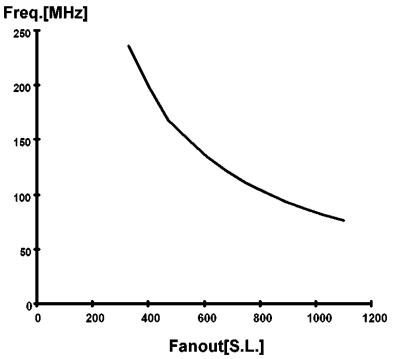
(a) CK2 PSCKDab2



(b) CK4 PSCKDab4



(c) CK8 PSCKDab8



(d) CK12 PSCKDab12

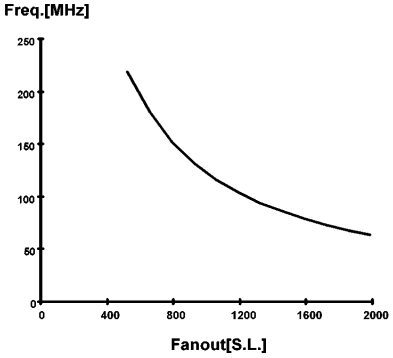
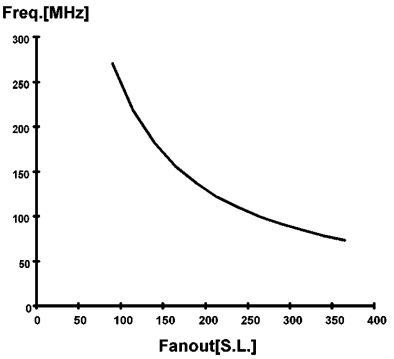
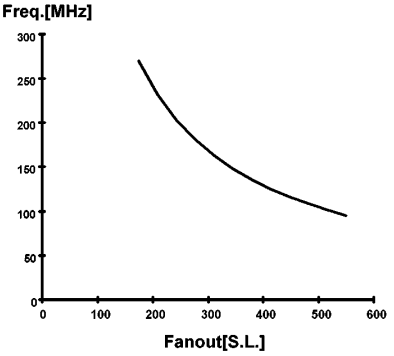


Figure 1-20. Fanout (SL) vs. Frequency Curve of STDM80 Clock Drivers

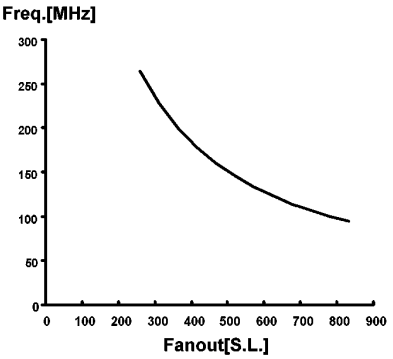
(a) CK2 PSCKDab2



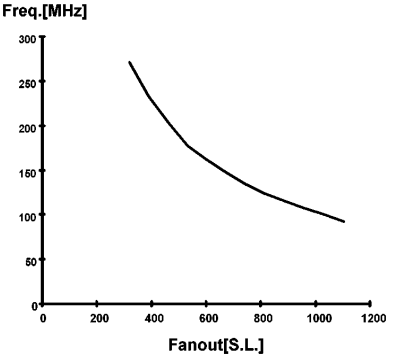
(b) CK4 PSCKDab4



(c) CK6 PSCKDab6



(d) CK8 PSCKDab8



PRODUCT LINE-UP

Table 1-14. Optimum Gates vs. Pad Numbers on STD80/STDM80

Ref. No	Estimated Gates	Total Pads		Maximum I/O Pads	
		TLM (70%)	DLM (40%)	TLM	DLM
01	10,000	57	75	41	59
02	15,000	70	93	54	77
03	20,000	81	107	65	91
04	30,000	99	131	83	115
05	40,000	114	151	98	135
06	50,000	128	169	112	153
07	60,000	140	186	124	170
08	70,000	151	201	135	185
09	80,000	162	214	146	198
10	90,000	172	227	156	211
11	100,000	181	240	175	224
12	120,000	198	263	182	247
13	140,000	214	284	198	268
14	160,000	229	303	213	287
15	180,000	243	322	227	306
16	200,000	256	339	240	323
17	250,000	287	379	271	363
18	300,000	314	416	298	400
19	350,000	339	449	323	433
20	400,000	363	480	347	464
21	450,000	385	509	369	493
22	500,000	406	537	390	521

NOTE: Chip size can be changed depending on the circuit design.

PACKAGES

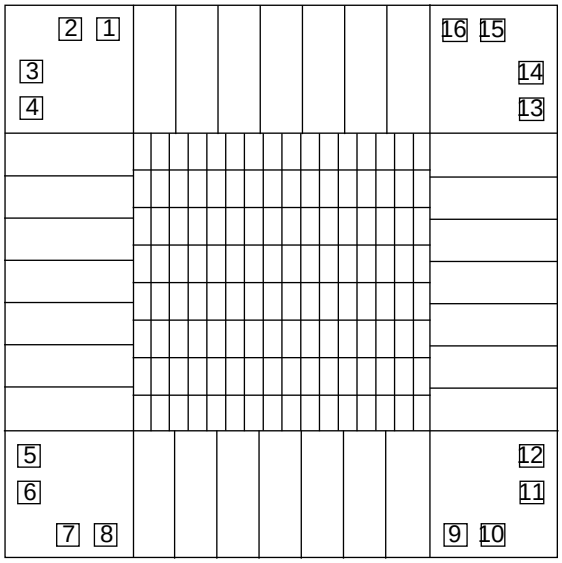
Type	DIP	SDIP	SOP	PLCC	QFP
Pin Count	24	24	28	28	44
	28	28	32	32	48
	40	30		44	60
	42	32		68	64
		40		84	80
		42			100
		48			128
		54			132
		56			160
		64			208
					240

NOTE: The selection of a package type and pin count is dependent on the size of a chip.

DEDICATED CORNER V_{DD}/V_{SS} PADS

The corner pads shown in the following figure are well-suited for double bonding purposes. Pad 1 and pad 2 can be bonded to the same package pin. Unlike normal I/O pads, these pads can only be used for V_{DD}/V_{SS} listed in Table 1-15. Use of Corner Pads.

Figure 1-21. V_{DD}/V_{SS} Corner Pads



NOTES:

1. There is no dedicated corner VSSI pad. Therefore, internal V_{SS} must be supplied using I/O pad type cell.
2. Corner pads are used to reduce the power/ground noise when some parts of the design cause noise problem especially while the other parts keep quiet.

Table 1-15. Use of Corner Pads

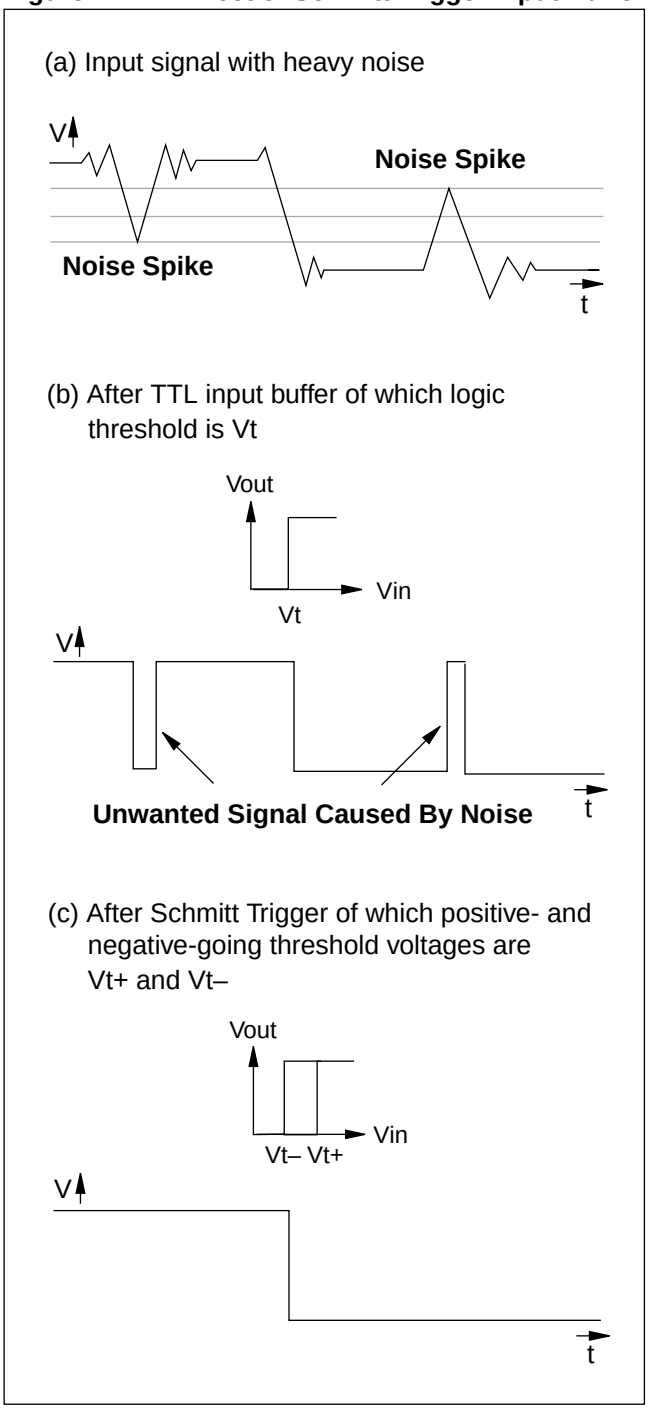
1	VSSO	9	VDD3O
2	VSSO	10	VDD3O
3	VSSI	11	VSSI
4	VSSI	12	VSSI
5	VDDI	13	VDDI
6	VDDI	14	VDDI
7	VDD5O	15	VSSO
8	VDD5O	16	VSSO

EXTERNAL DESIGN INTERFACE CONSIDERATIONS

This section briefly describes what you should consider when chips interface with outside world especially for a noise protection.

Input Buffer

Figure 1-22. Effect of Schmitt Trigger Input Buffer



Usually there are three types of input receivers in ASIC libraries; TTL input buffer, CMOS input buffer, and various Schmitt trigger input buffers.

TTL input buffer has relatively poor noise characteristics because of its shifted logic threshold voltage. CMOS input buffer is better than TTL against a noise because the logic threshold voltage is near 2.5volt. If an input signal has relatively large noise spikes, it could cause an unwanted input signal.

When an input signal is very noisy, the noise can be filtered by using a Schmitt trigger input buffer. As shown in Figure 1-22. Effect of Schmitt Trigger Input Buffer, Schmitt trigger input buffers have two different input thresholds for positive- and negative-going signals. This hysteresis between positive- and negative-going voltage signals can filter a noisy signal to a wanted one.

According to applications, the most suitable one can be chosen among the various Schmitt trigger input buffers having different levels of threshold voltage.

Output Pad Cell

As incoming signals to a chip have a noise, the noise can also be induced by the operation of the chip itself. There are several sources of a noise, but the greatest singular source of a noise is the switching of an output with high capacitive load.

Figure 1-23. Simple Model of Output Pad Cell

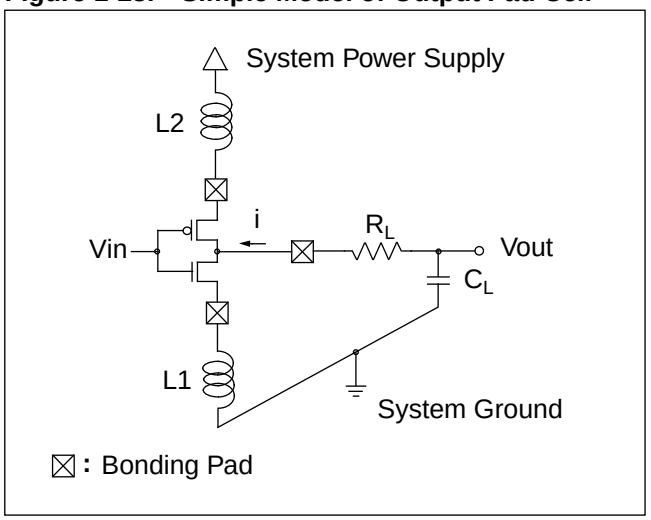


Figure 1-23. Simple Model of Output Pad Cell shows the simple model of an output driver considering the external interface. L1 and L2 are parasitic inductances of the package and C_L is an output load. Vout will fall as Vin rises and the current i flows through n-transistor discharging the loaded charge ($V_{DD} \times C_L$).

The details of this operations are described in Figure 1-24. Ground Bounce Phenomenon.

The important phenomenon which can be observed in this figure is that the voltage level Vn shifts relative to the system ground. Vn is the ground of the chip.

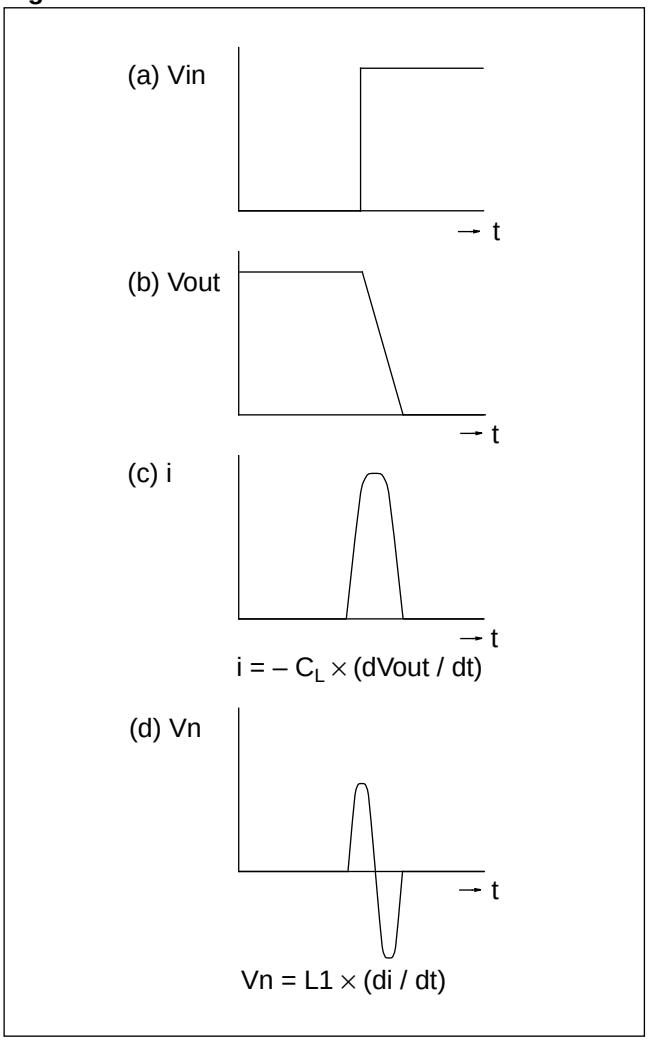
This phenomenon is called as a “ground bounce” that is the chip reference shift caused by the external inductance and the transient current flow to the ground.

The amount of voltage level shifted by the ground bounce is

$$Vn = -L \times (di / dt)$$

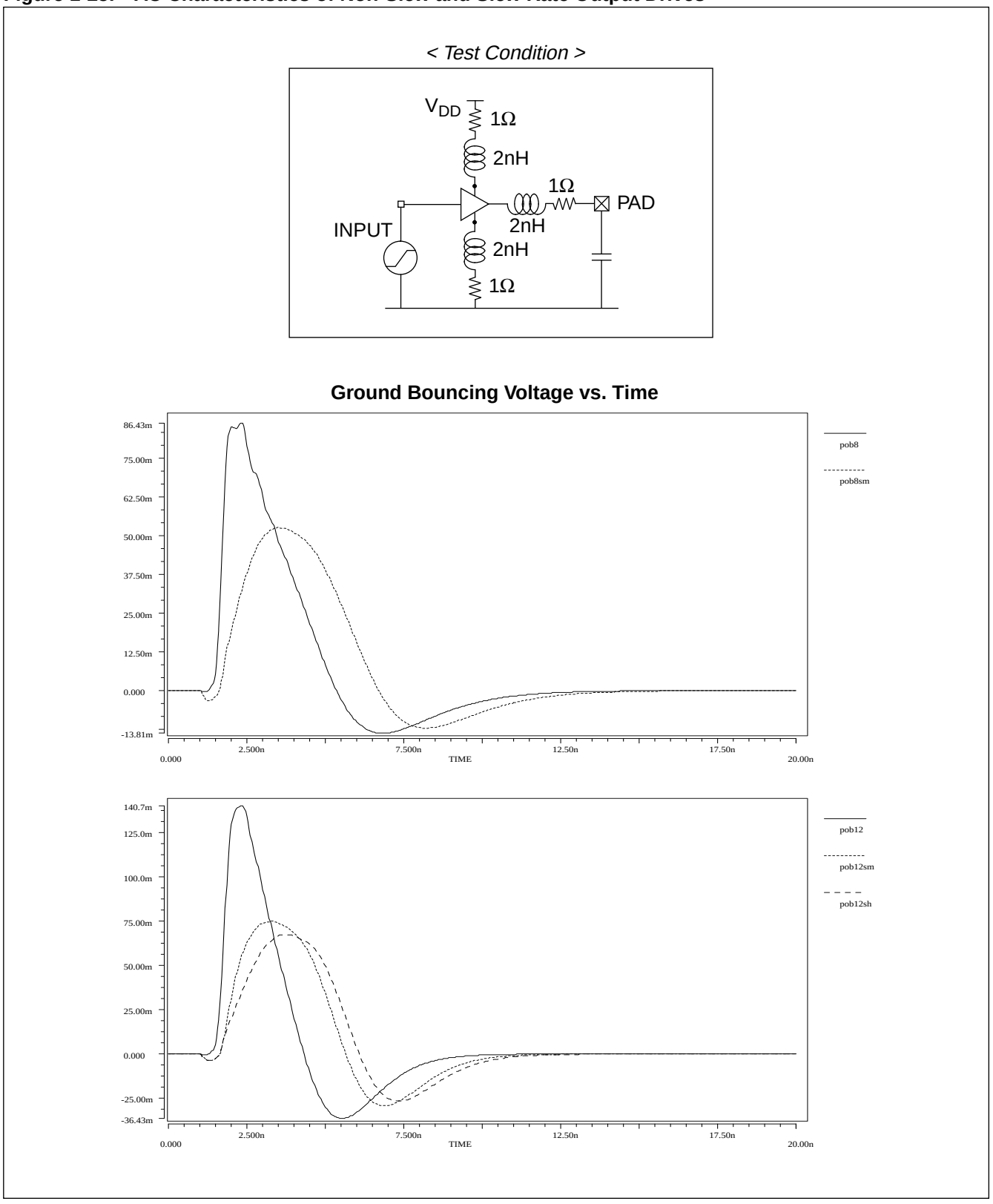
When the output driver makes a low-to-high transition, the similar noise problem is generated on the power.

Figure 1-24. Ground Bounce Phenomenon

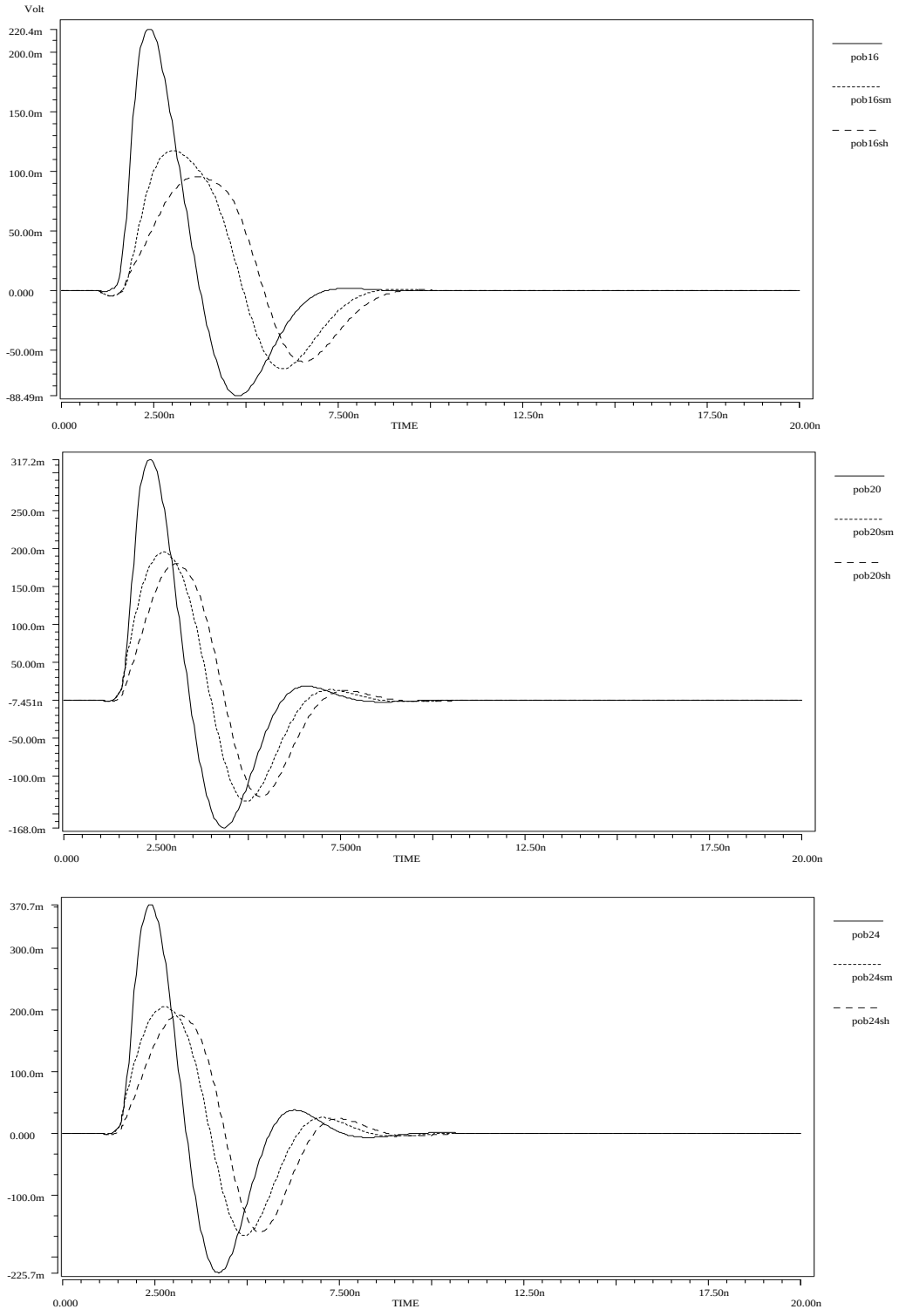


The following graphs show typical AC characteristics of non-slew and slew-rate output drives in STD80/STDM80. Using the slew-rate control, you can reduce the switching noise.

Figure 1-25. AC Characteristics of Non-Slew and Slew Rate Output Drives



Ground Bouncing Voltage vs. Time



Simultaneous Switching Outputs (SSOs)

If several output drivers switch from high to low simultaneously, the ground bouncing level becomes quite large because the current flowing through the inductance L is the total sum of the transient current of each output driver. The amount of total current and the level of ground bounce are proportional to the number of SSOs.

This ground bounce can cause two types of problems, a noise margin reduction and a generation of noise spike on the output pad.

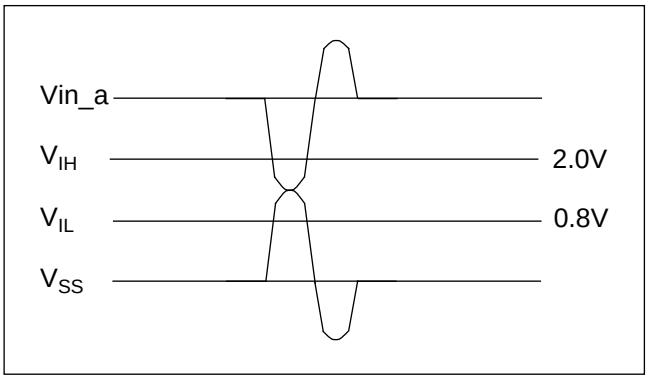
NOISE MARGIN REDUCTION

The ground bounce can cause a noise margin reduction when the same ground bus is used for both input buffers and output drivers as shown in Figure 1-27. The Figure of SSOs. The noise margin reduction can be explained using the circuit in the same figure.

As you can see, if outputs switch from high to low simultaneously, it results in a ground bounce or the rise of the chip ground level relative to system ground. The rise appears as the input voltage Vin_a is below V_{IH} causing false triggering of the input buffer. Vin is, in this case, not the same as Vin_a. Note that Vin is measured relative to the system ground, while Vin_a is measured relative to the local device ground.

This phenomenon is shown in Figure 1-26. Noise Margin Reduction due to SSOs. For a low-to-high transition, it is the low input levels (V_{IL}) that are affected.

Figure 1-26. Noise Margin Reduction due to SSOs

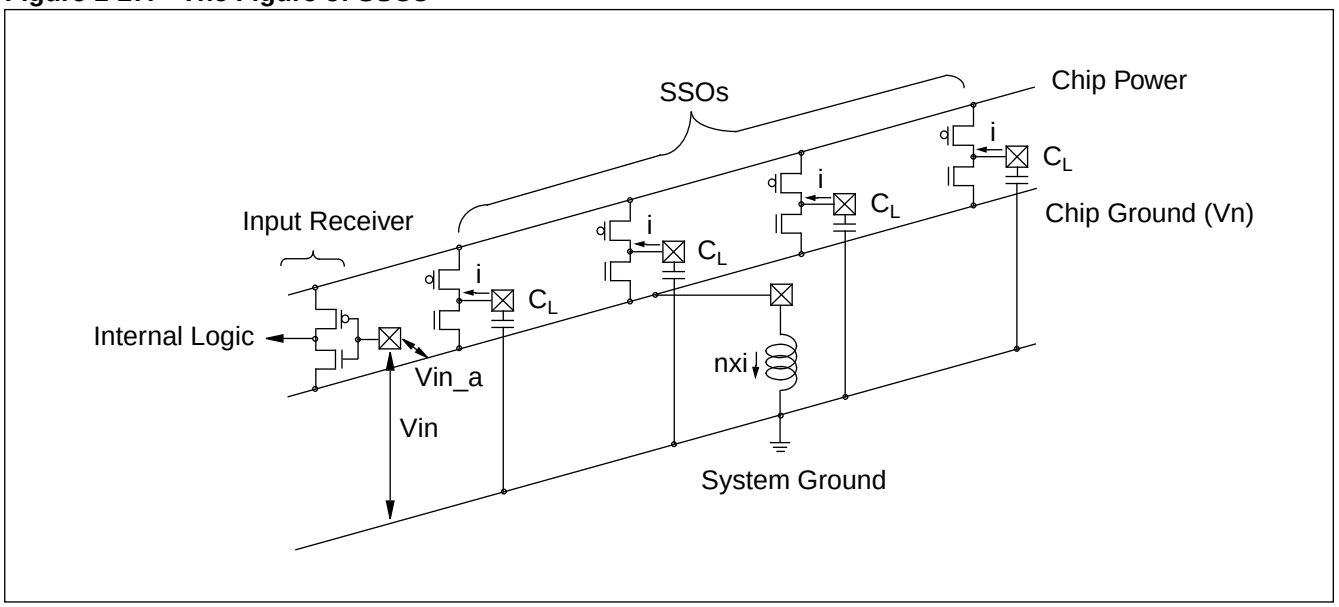


NOISE SPIKE GENERATION ON STABLE OUTPUT

If input and output power buses are separated, the problem of a noise margin reduction in the input buffer can be solved. However, ground bounce can cause another problem in spite of using separated power and ground bus.

The Figure 1-28. Noise Spike Induced by Ground Bounce shows a common octal driver application where ground bounce spikes will be observable on the one stable output. If the spike is considered as high by another chip, this ground bounce may upset that operation of interfacing device or cause system logic errors.

Figure 1-27. The Figure of SSOs



For example, suppose C_L = 100pF, V_{DD} = 3.3Volt, t_F = 5ns. From Figure 1-24. Ground Bounce Phenomenon, the maximum current flow occurs at time $0.5 \times t_F$. Then approximately,

$i = C_L \times (dv / dt) \cong C_L \times (\Delta V / \Delta t)$,
and

$i\ (max) = 100 \times 10^{-12} \times \{5 / (2.5 \times 10^{-9})\} = 200$ [mA].

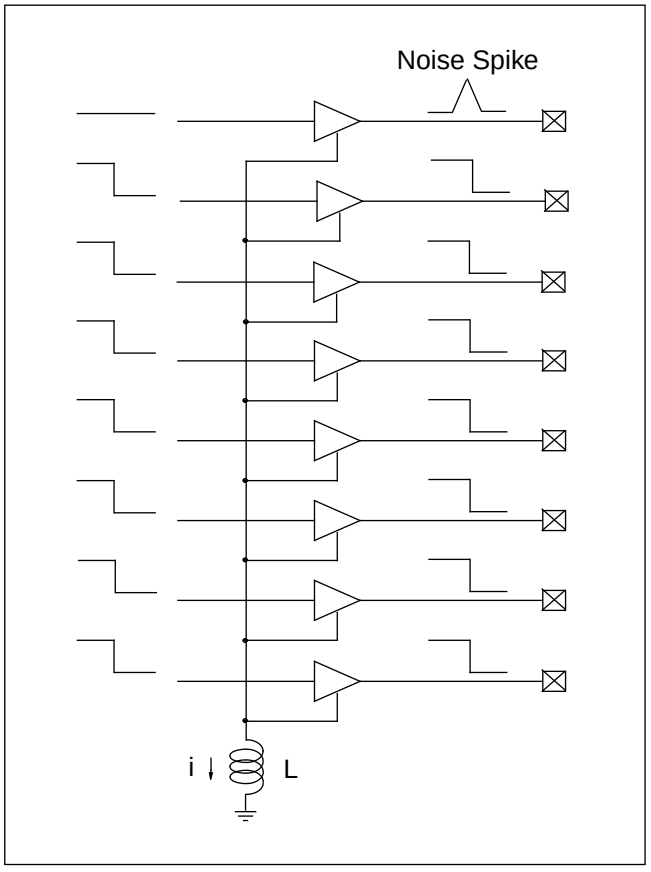
If the number of SSOs is 5, and L is 4nH,

$Vn = L \times (di / dt) \times N \cong L \times (\Delta i / \Delta t) \times N$ by approximation,

$Vn\ (max) = 4 \times 10^{-9} \times \{0.200 / (2.5 \times 10^{-9})\} \times 5 = 1.60$ [Volt].

From this calculation, 1.60V of noise spike is expected. This is about logic threshold voltage of TTL. This numerical estimate clearly shows that power bus noise control is one of the fundamental problems in a high-speed CMOS VLSI design. It is an important design consideration to prevent the noise from affecting the integrity of the logic operation of a chip.

Figure 1-28. Noise Spike Induced by Ground Bounce



How to Protect Ground Bounce?

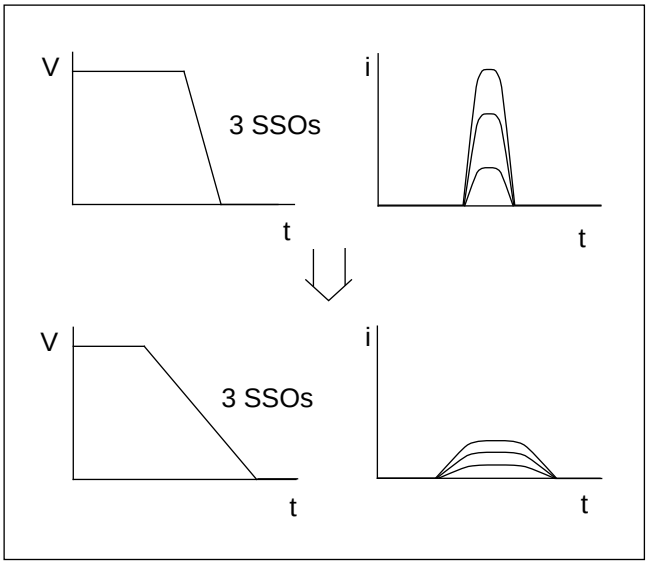
The fundamental solution to the ground bounce problem is to reduce the inductance of the package. However, in the boundary of a given packaging technology, the following guidelines can be used for reducing ground bounce:

(1) If possible, use separate power and ground buses for input buffers and output drivers.

(2) The number of ground and power pads should not be less than the required number of pads.

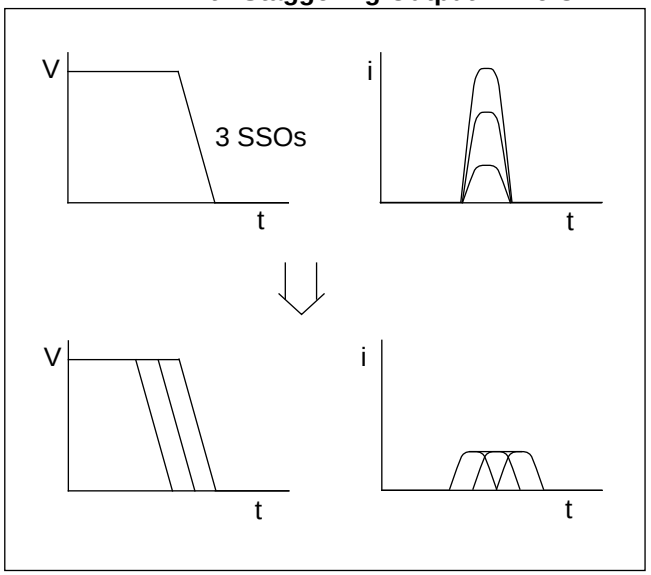
(3) If the design is not so much sensitive to speed, use slew rate control, i.e., increase switching time, to reduce the value of di / dt of an output driver. SEC supports two levels of slew rate controlled output buffers, SM and SH. You can see this effect in the following figure.

Figure 1-29. Effect on Reducing Peak Current with Slew-Rate Control



(4) If you cannot use a slew rate cell because of the speed requirement, you can stagger the output driver as shown in Figure 1-30. Effect on Reducing Peak Current with Staggering Output Drivers. This is not a general-purpose solution. It makes sense only when special relief in timing requirements exists from a system architecture.

Figure 1-30. Effect on Reducing Peak Current with Staggering Output Drivers



(5) High-drive outputs should be close to V_{SS} pins. SSOs should be placed particularly close to V_{SS} pins.

(6) SSOs should be appropriately placed in groups belonging to given V_{SS} pins.

(7) Noise-sensitive signals such as clock, asynchronous clear and preset should be located away from SSOs and high-drive outputs. Also, assign them to pins with low inductance and resistance, preferably near V_{SS}, if one is available away from SSOs or high-drive outputs.

(8) Place SSOs on low inductance pins, such as those located on the inner rows or middle positions of PGAs.

(9) Clock, preset and clear inputs must not be placed on the corners of a package, especially when the array is packaged in DIP.

(10) Output signals to be used as clock, preset or clear for other devices must be kept away from SSOs and close to V_{SS} pin.

These guidelines assist you in choosing the best package(s) for the application. Furthermore, the recommendations about pinout results in reliable and predictable devices that minimizes harmful DC and AC effects on the system.

CRYSTAL OSCILLATOR CONSIDERATIONS

Overview

STD80/STDM80 contains a circuit commonly referred to as an “on-chip oscillator.” The on-chip circuit itself is not an oscillator but an amplifier which is suitable for being used as the amplifier part of a feedback oscillator. With proper selection of off-chip components, this oscillator circuit performs better than any other types of clock oscillators.

It is very important to select suitable off-chip components to work with the on-chip oscillator circuitry. It should be noted, however, that SEC cannot assume the responsibility of writing specifications for the off-chip components of the complete oscillator circuit, nor of guaranteeing the performance of the finished design in production, anymore than a transistor manufacturer, whose data sheets show a number of suggested amplifier circuits, can assume responsibility for the operation, in production, of any of them.

We are often asked why we don’t publish a list of required crystal or ceramic resonator specifications, and recommend values for the other off-chip components. This has been done in the past, but sometimes with consequences that were not intended.

Suppose we suggest a maximum crystal resistance of 30 ohms for some given frequency. Then your crystal supplier tells you the 30 ohm crystals are going to cost twice as much as 50 ohm crystals. Fearing that SEC will not “guarantee operation” with 50 ohm crystals, you order the expensive ones.

In fact, SEC guarantees only what is embodied within an SEC product. Besides, there is no reason why 50 ohm crystals couldn’t be used, if the other off-chip components are suitably adjusted.

Should we recommend values for the other off-chip components? Should we do for 50 ohm crystals or 30 ohm crystals? With respect to what should we optimize their selection? Should we minimize start-up time or maximize frequency stability?

In many applications, neither start-up time nor frequency stability is particularly critical, and our “recommendations” are only restricting your system to unnecessary tolerances. It all depends on the application.

Oscillator Design Considerations

ASIC designers have a number of options for clocking the system. The main decision is whether to use the “on-chip” oscillator or an external oscillator. If the choice is to use the on-chip oscillator, what kinds of external components are to use an external oscillator, what type of oscillator would it be?

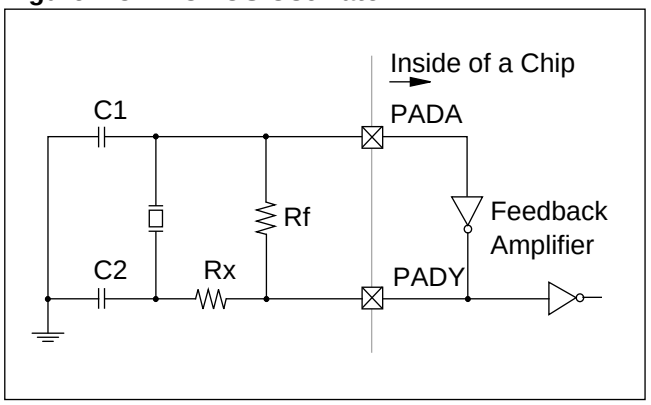
The decisions have to be based on both economic and technical requirements. In this section we will discuss some of the factors that should be considered.

ON-CHIP OSCILLATOR

In most cases, the on-chip amplifier with the appropriate external components provides the most economical solution to the clocking problem. Exceptions may arise in server environments when frequency tolerances are tighter than about 0.01%.

The external components that commonly used for CMOS gate oscillator are a positive reactance (normal crystal oscillator), two capacitors, C1 and C2, and two resistor Rf and Rx as shown in the figure below.

Figure 1-31. CMOS Oscillator



CRYSTAL SPECIFICATIONS

Specifications for an appropriate crystal are not very critical, unless the frequency is. Any fundamental-mode crystal of medium or better quality can be used.

We are often asked what maximum crystal resistance should be specified. The best answer to that question is the lower the better, but use what is available.

The crystal resistance will have some effect on start-up time and steady-state amplitude, but not so much that it can’t be compensated for by appropriate selection of the capacitances, C1 and C2.

Similar questions are asked about specifications of load capacitance and shunt capacitance. The best advice we can give is to understand what these parameters mean and how they affect the operation of the circuit (that being the purpose of this application note), and then to decide for yourself if such specifications are meaningful in your frequency tolerances are tighter than about 0.1%.

Part of the problem is that crystal manufacturers are accustomed to talking “ppm” tolerances with radio engineers and simply won’t take your order until you’ve filled out their list of frequency tolerance requirements, both for yourself and to the crystal manufacturer. Don’t pay for 0.003% crystals if your actual frequency tolerance is 1%.

OSCILLATION FREQUENCY

The oscillation frequency is determined 99.5% by the crystal and up to about 0.5% by the circuit external to the crystal.

The on-chip amplifier has little effect on the frequency, which is as it should be, since the amplifier parameterizes temperature and process dependent.

The influence of the on-chip amplifier on the frequency is by means of its input and output (pin-to-ground) capacitances, which parallel C1 and C2, and the PADA-to-PADY (pin-to-pin) capacitance, which parallels the crystal. The input and pin-to-pin capacitances are about 7 pF each.

Internal phase deviations capacitance of 25 to 30 pF. These deviations from the ideal have less effect in the positive reactance oscillator (with the inverting amplifier) than in a comparable series resonant oscillator (with the non-inverting amplifier) for two reasons: first, the effect of the output capacitor; second, the positive reactance oscillator is less sensitive, frequency-wise, to such phase errors.

C1 / C2 SELECTION

Optimal values for the capacitors C1 and C2 depend on whether a quartz crystal or ceramic resonator is being used, and also on application-specific requirements on start-up time and frequency tolerance.

Start-up time is sometimes more critical in microcontroller systems than frequency stability, because of various reset and initialization requirements.

Less commonly, accuracy of the oscillator frequency is also critical, for example, when the oscillator is being used as a time base. As a general rule, fast start-up and stable frequency tend to pull the oscillator design in opposite directions.

Considerations of both start-up time and frequency stability over temperature suggest that C1 and C2 should be about equal and at least 20pF. (But they don't have to be either.)

Increasing the value of these capacitances above some 40 or 50pF improves frequency stability. It also tends to increase the start-up time. These is a maximum value (several hundred pH, depending on the value of R1 of the quartz or ceramic resonator) above which the oscillator won't start up at all.

If the on-chip amplifier is a simple inverter, the user can select values for C1 and C2 between some 20 and 100pF, depending on whether start-up time or frequency stability is the more critical parameter in a specific application.

RF / RX SELECTION

A CMOS inverter might work better in this application since a large Rf (1mega-ohm) can be used to hold the inverter in its linear region.

Logic gates tend to have a fairly low output resistance, which testabilizes the oscillator. For that reason a resistor Rx (several k-ohm) is often added to the feedback network, as shown in Figure 1-31. CMOS Oscillator.

At higher frequencies a 20 or 30pF capacitor is sometimes used in the Rx position, to compensate for some of the internal propagation delay.

PIN CAPACITANCE

Internal pin-to-ground and pin-to-pin capacitances, and PADA and PADY have some effect on the oscillator. These capacitances are normally taken to be in the range of 5 to 10pF, but they are extremely difficult to evaluate. Any measurement of one such capacitance necessarily include effects from the others.

One advantage of the positive reactance oscillator is that the pin-to ground cap. is paralleled by an external bulk capacitance, so a precise determination of their value is unnecessary.

We would suggest that there is little justification for more precision than to assign them a value of 7pF (PADA-to-ground and PADA-to-PADY). This value is probably not in error by more than 3 or 4pF.

The PADY-to-ground cap. is not entirely a "pin capacitance", but more like an "equivalent output capacitance" of some 25 to 30pF, having to include the effect of internal phase delays. This value varies to some extent with temperature, process, and frequency.

PLACEMENT OF COMPONENTS

Noise glitches arising at PADA or PADY pins at the wrong time can cause a miscount in the internal clock-generating circuitry. These kinds of glitches can be produced through capacitive coupling between the oscillator components and PCB traces carrying digital signals with fast rise and fall times.

For this reason, the oscillator components should be mounted close to the chip and have short, direct traces to the PADA, PADY, and V_{SS} pins.

If possible, use dedicated V_{SS} and V_{DD} pin for only crystal feedback amplifier.

Troubleshooting Oscillator Problems

The first thing to consider in case of difficulty is that there may be significant differences in stray caps between the test jig and the actual application, particularly if the actual application is on a multi-layer board.

Noise glitches, that are not present in the test jig but are in the application board, are another possibility. Capacitive coupling between the oscillator circuitry and other signal has already been mentioned as a source of miscounts in the internal clocking circuitry. Inductive coupling is also doubtful, if there is strong current nearby. These problems are a function of the PCB layout.

Surrounding oscillator components with “quit” traces (for example, VCC and ground) will alleviate capacitive coupling to signals having fast transition time. To minimize inductive coupling, the PCB layout should minimize the areas of the loops formed by oscillator components.

The loops demanding to be checked are as follows:

PADA through the resonator to PADY;
PADA through C1 to the V_{SS} pin;
PADY through C2 to the V_{SS} pin.

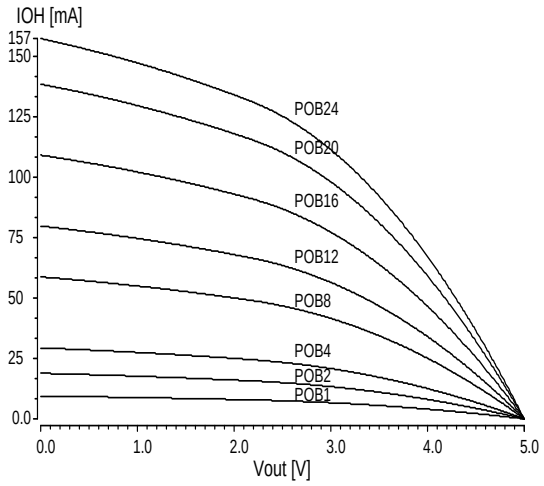
It is not unusual to find that the ground ends of C1 and C2 eventually connect up to the V_{SS} pin only after looping around the farthest ends of the board. Not good.

Finally, it should not be overlooked that software problems sometimes imitate the symptoms of a slow-starting oscillator or incorrect frequency. Never underestimate the perversity of a software problem.

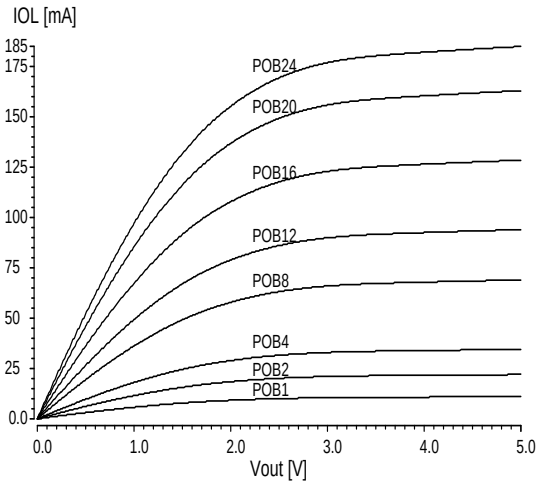
OUTPUT DRIVE CAPABILITIES

IV Characteristics

V_{DD} = 5V, T_A = 25°C, Typical Process

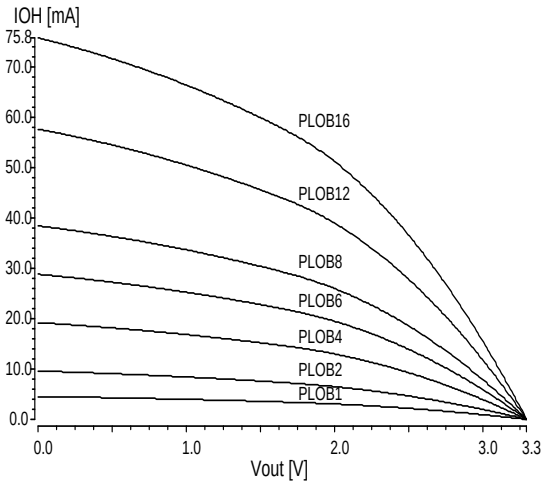


P-TR Characteristics

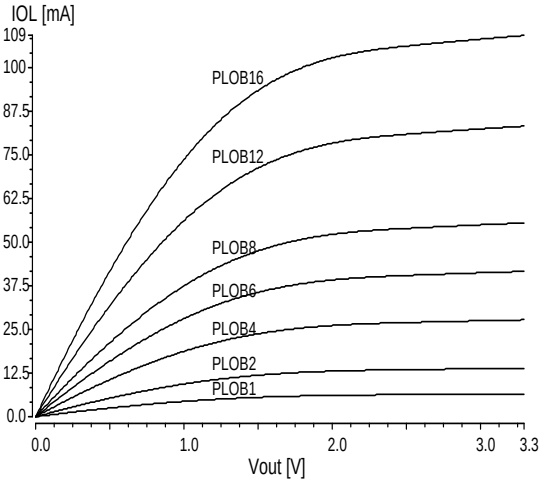


N-TR Characteristics

V_{DD} = 3.3V, T_A = 25°C, Typical Process



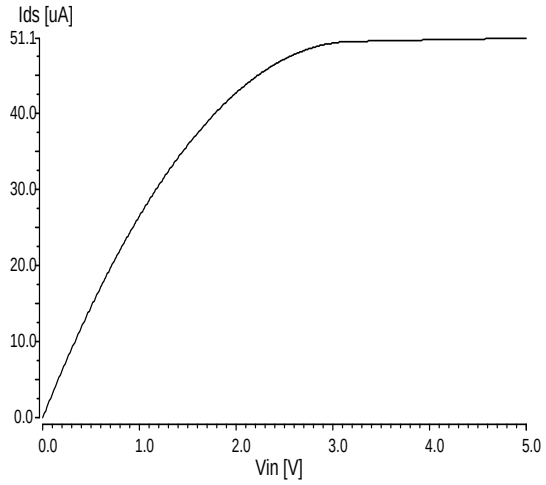
P-TR Characteristics



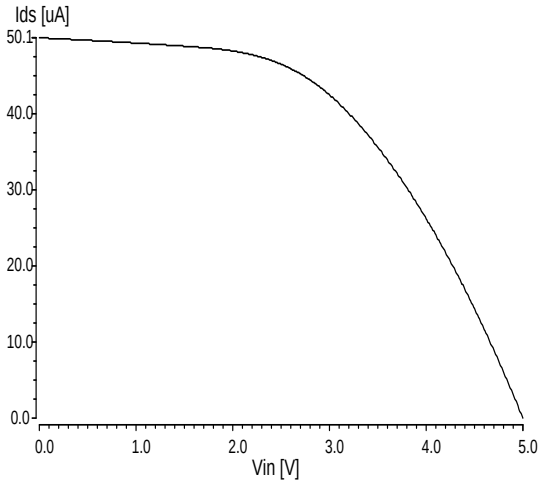
N-TR Characteristics

Input Buffer Pull-Down/Pull-Up Characteristics

V_{DD} = 5V, T_A = 25°C, Typical Process

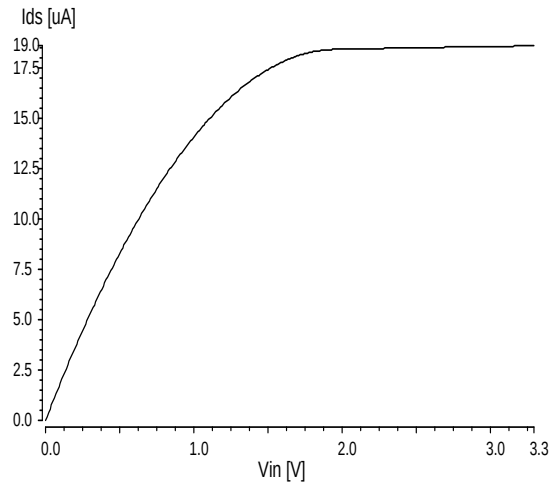


Pull-Down

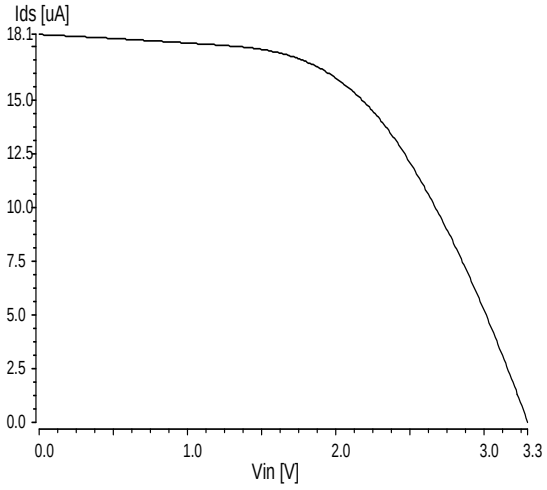


Pull-Up

V_{DD} = 3.3V, T_A = 25°C, Typical Process



Pull-Down

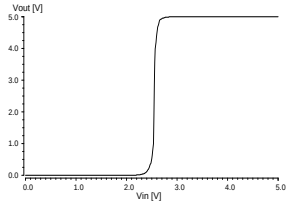


Pull-Up

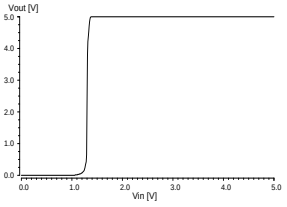
INPUT BUFFER DC CURVES

Input Buffer Transfer Curves

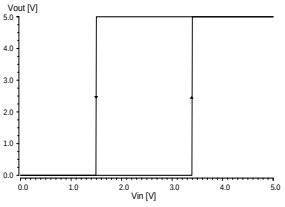
V_{DD} = 5V, T_A = 25°C, Typical Process



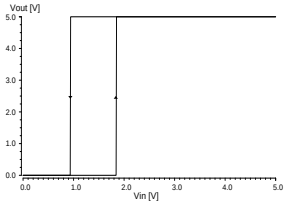
CMOS



TTL

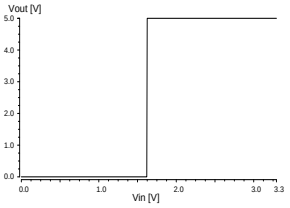


CMOS Schmitt Trigger

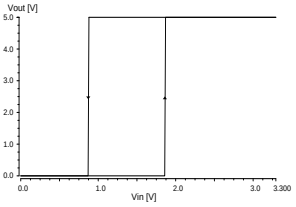


TTL Schmitt Trigger

V_{DD} = 3.3V, T_A = 25°C, Typical Process



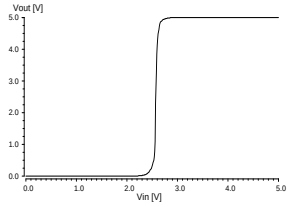
CMOS



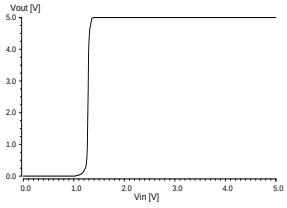
CMOS Schmitt Trigger

Input Clock Drivers Transfer Curves

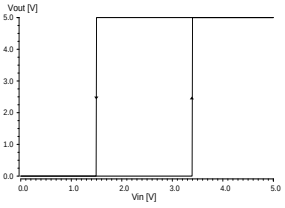
V_{DD} = 5V, T_A = 25°C, Typical Process



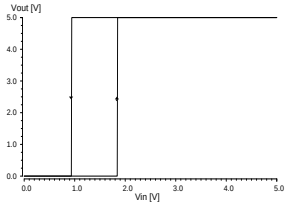
CMOS



TTL

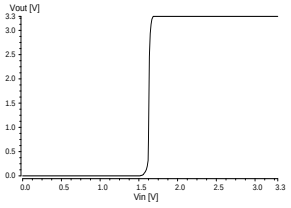


CMOS Schmitt Trigger

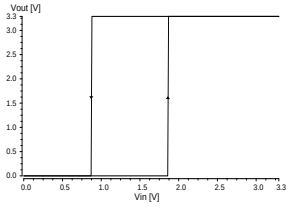


TTL Schmitt Trigger

V_{DD} = 3.3V, T_A = 25°C, Typical Process



CMOS



CMOS Schmitt Trigger

V_{DD} = 3.3V ± 10%, T_A = 0 to 70°C

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	High level input voltage				V
	CMOS interface		$0.7V_{DD}$		
	CMOS schmitt trigger			2.1	
V_{IL}	Low level input voltage				V
	CMOS interface			$0.3V_{DD}$	
	CMOS schmitt trigger		0.8		
I_{IH}	High level input current				µA
	Input buffer	$V_{IN} = V_{DD}$	–10	10	
	Input buffer with pull-down		10	200	
I_{IL}	Low level input current				µA
	Input buffer	$V_{IN} = V_{SS}$	–10	10	
	Input buffer with pull-up		–200	–10	
V_{OH}	High level output voltage				V
	Type B1 to B16	I_{OH} = –1µA	V_{DD} – 0.05		
	Type B1	I_{OH} = –0.5mA	2.4		
	Type B2	I_{OH} = –1mA			
	Type B4	I_{OH} = –2mA			
	Type B6	I_{OH} = –3mA			
	Type B8	I_{OH} = –4mA			
	Type B10	I_{OH} = –5mA			
	Type B12	I_{OH} = –6mA			
	Type B16	I_{OH} = –8mA			
V_{OL}	Low level output voltage				V
	Type B1 to B16	I_{OL} = 1µA		0.05	
	Type B1	I_{OL} = 1mA		0.4	
	Type B2	I_{OL} = 2mA			
	Type B4	I_{OL} = 4mA			
	Type B6	I_{OL} = 6mA			
	Type B8	I_{OL} = 8mA			
	Type B10	I_{OL} = 10mA			
	Type B12	I_{OL} = 12mA			
	Type B16	I_{OL} = 16mA			

Absolute Maximum Ratings

Symbol	Parameter	Ratingtd	Unit
V_{DD}	DC supply voltage	–0.3 to 7	V
V_{IN}	DC input voltage	–0.3 to V_{DD} + 0.3	
I_{IN}	DC input current	±10	mA
T_{STG}	Storage temperature	–40 to 125	°C

Recommended Operating Conditions

Symbol	Parameter		Rating	Unit
V_{DD}	DC supply voltage	5V	4.75 to 5.25	V
		3.3V	3.0 to 3.6	
T_A	Commercial temperature		0 to 70	°C
	Industrial temperature		–40 to 85	

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ± 5%, T_A = 0 to 70°C

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	High level input voltage				
	TTL interface		2.0		V
	TTL schmitt trigger			2.1	
	CMOS interface		$0.7V_{DD}$		
	CMOS schmitt trigger			4.0	
V_{IL}	Low level input voltage				
	TTL interface			0.8	V
	TTL schmitt trigger		0.8		
	CMOS interface			$0.3V_{DD}$	
	CMOS schmitt trigger		1.0		
I_{IH}	High level input current				
	Input buffer	$V_{IN} = V_{DD}$	–10	10	µA
	Input buffer with pull-down		10	200	
I_{IL}	Low level input current				
	Input buffer	$V_{IN} = V_{SS}$	–10	10	µA
	Input buffer with pull-up		–200	–10	
V_{OH}	High level output voltage				
	Type B1 to B24[Note1]	I_{OH} = –1µA	V_{DD} – 0.05		V
	Type B1	I_{OH} = –1mA	2.4		
	Type B2	I_{OH} = –2mA			
	Type B4	I_{OH} = –4mA			
	Type B8	I_{OH} = –8mA			
	Type B12	I_{OH} = –12mA			
	Type B16	I_{OH} = –16mA			
	Type B20	I_{OH} = –20mA			
	Type B24	I_{OH} = –24mA			
V_{OL}	Low level output voltage				
	Type B1 to B24	I_{OL} = 1µA		0.05	V
	Type B1	I_{OL} = 1mA		0.4	
	Type B2	I_{OL} = 2mA			
	Type B4	I_{OL} = 4mA			
	Type B8	I_{OL} = 8mA			
	Type B12	I_{OL} = 12mA			
	Type B16	I_{OL} = 16mA			
	Type B20	I_{OL} = 20mA			
	Type B24	I_{OL} = 24mA			
I_{OZ}	Tri-state output leakage current	$V_{OUT} = V_{SS}$ or V_{DD}	–10	10	µA
I_{DD}	Quiescent supply current	$V_{IN} = V_{SS}$ or V_{DD}		100[Note2]	µA

NOTES:

1. Type B1 means 1mA output driver cells, and Type B24 means 24mA output driver cells.
2. This value depends on the customer design.

Contents

DC Electrical Characteristics 2-1
Input Buffer DC Curves 2-3
Output Drive Capabilities 2-5

Electrical Characteristics 2

Internal Macrocells 3

Contents

Overview 3-1
Summary Tables 3-2
Logic Cells 3-7
Flip-Flops 3-169
Latches 3-358
Bus Holder 3-458
Internal Clock Drivers 3-459
Decoders 3-462
Adders 3-476
Multiplexers 3-485

OVERVIEW

The third chapter contains data sheets of logic cells, flip-flops, latches, bus holder, internal clock drivers, decoders, adders and multiplexers.

The electrical characteristics of each cell follows its basic cell data.

Summary tables in the following pages list the whole STD80/STDM80 internal macrocells by the type and show their reference page numbers for your convenience. Moreover, you can find the more detailed description tables on the leading pages of each category.

SUMMARY TABLES

Logic Cells

Cell Type	Cell Name	Page
AND Cell	AD2/AD2D2	3-11
	AD3/AD3D3	3-13
	AD4/AD4D2	3-16
	AD5/AD5D2	3-19
NAND Cell	ND2/ND2D2	3-22
	ND3/ND3D2	3-24
	ND4/ND4D2	3-27
	ND5/ND5D2	3-30
	ND6/ND6D2	3-33
	ND8/ND8D2	3-38
NOR Cell	NR2/NR2D2	3-43
	NR3/NR3D2	3-45
	NR4/NR4D2	3-48
	NR5/NR5D2	3-51
	NR6/NR6D2	3-54
	NR8/NR8D2	3-59
OR Cell	OR2/OR2D2	3-64
	OR3/OR3D3	3-66
	OR4/OR4D2	3-69
	OR5/OR5D2	3-72
Exclusive-NOR Cell	XN2/XN2D2	3-75
	XN3/XN3D3	3-77
Exclusive-OR Cell	XO2/XO2D2	3-80
	XO3/XO3D3	3-82
Combinational Cell of AND and NOR	AO21/AO21D2	3-85
	AO211/AO211D2	3-88
	AO22/AO22D2	3-91
	AO22A/AO22D2A	3-94
	AO222/AO222D2	3-97
	AO222A/AO222D2A	3-102
	AO33/AO33D2	3-105
	AO333/AO333D2	3-110

Cell Type	Cell Name	Page
Combinational Cell of OR and NAND	OA21/OA21D2	3-115
	OA211/OA211D2	3-118
	OA22/OA22D2	3-121
	OA22A/OA22D2A	3-124
	OA2222/OA2222D2	3-127
Delay Cell	DL(1/2/3/4/5/10)D2/DL(1/2/3/4/5/10)D4	3-132
Inverter	IV/IVD2/IVD3/IVD4/IVD6/IVD8	3-138
	IVA/IVD2A/IVD3A/IVD4A	3-142
	IVCD(11/13)/IVCD(22/26)/IVCD44	3-145
Inverting Tri-State Buffer	IVT/IVTD2/IVTD4/IVTD8	3-149
	IVTN/IVTND2/IVTND4/IVTND8	3-153
Non-Inverting Buffer	NID/NID2/NID3/NID4/NID6/NID8	3-157
	NIT/NITD2/NITD4/NITD8	3-161
	NITN/NITND2/NITND4/NITND8	3-165

Flip-Flops

Cell Type	Cell Name	Page
D Flip-Flop	FD1/FD1D2	3-172
	FD1CS/FD1CSD2	3-175
	FD1S/FD1SD2	3-179
	FD1Q/FD1QD2	3-182
	FD1X2	3-184
	FD1X4	3-186
	YFD1/YFD1D2	3-189
D Flip-Flop with Reset	FD2/FD2D2	3-192
	FD2CS/FD2CSD2	3-195
	FD2S/FD2SD2	3-199
	FD2Q/FD2QD2	3-202
	FD2X2	3-204
	FD2X4	3-207
	YFD2/YFD2D2	3-210
D Flip-Flop with Reset, Tri-State Output	FD2T/FD2TD2	3-213
	FD2TCS/FD2TCSD2	3-216
	FD2TS/FD2TSD2	3-221

Cell Type	Cell Name	Page
D Flip-Flop with Set	FD3/FD3D2	3-225
	FD3CS/FD3CSD2	3-228
	FD3S/FD3SD2	3-232
	FD3Q/FD3QD2	3-235
	FD3X2	3-237
	FD3X4	3-240
	YFD3/YFD3D2	3-243
D Flip-Flop with Reset, Set	FD4/FD4D2	3-246
	FD4CS/FD4CSD2	3-250
	FD4S/FD4SD2	3-256
	FD4Q/FD4QD2	3-260
	FD4X2	3-263
	FD4X4	3-266
	YFD4/YFD4D2	3-271
D Flip-Flop with Negative Edge Trigger	FD5/FD5D2	3-274
	FD5S/FD5SD2	3-277
	FD5X4	3-280
	FD6/FD6D2	3-283
	FD6S/FD6SD2	3-286
	FD7/FD7D2	3-289
	FD7S/FD7SD2	3-292
	FD8/FD8D2	3-295
	FD8S/FD8SD2	3-299
D Flip-Flop with Synchronous Clear	FDS2/FDS2D2	3-303
	FDS2CS/FDS2CSD2	3-306
	FDS2S/FDS2SD2	3-310
	FDS3/FDS3D2	3-313
D Flip-Flop with CK Enable	FG1	3-316
	FG1X4	3-318
	FG2	3-323
	FG2X4	3-326

Cell Type	Cell Name	Page
JK Flip-Flop	FJ1/FJ1D2	3-331
	FJ1S/FJ1SD2	3-334
	FJ2/FJ2D2	3-337
	FJ2S/FJ2SD2	3-340
	FJ4/FJ4D2	3-344
	FJ4S/FJ4SD2	3-348
Toggle Flip-Flop	FT2/FT2D2	3-352
	FT3/FT3D2	3-355

Latches

Cell Type	Cell Name	Page
D Latch with Active High	LD1/LD1D2	3-360
	LD1S/LD1SD2	3-363
	LD1Q/LD1QD2	3-368
	LD1X4/LD1X4D2	3-371
	YLD1/YLD1D2	3-380
	LD1A	3-383
	LD1B	3-385
D Latch with Active High, Reset	LD2/LD2D2	3-388
	LD2Q/LD2QD2	3-393
	YLD2/YLD2D2	3-396
	LD3/LD3D2	3-401
	LD4/LD4D2	3-406
D Latch with Active Low	LD5/LD5D2	3-411
	LD5S/LD5SD2	3-414
	LD5X4/LD5X4D2	3-419
	LD6/LD6D2	3-428
	LD7/LD7D2	3-433
	LD8/LD8D2	3-438
D Latch with Synchronous Clear	LDS2	3-443
	LDS6	3-446
SR Latch	LS0/LS0D2	3-449
	LS1	3-452
	LS2	3-455

Bus Holder

Cell Type	Cell Name	Page
Bus Holder	BUSHOLDER	3-458

Internal Clock Drivers

Cell Type	Cell Name		Page
	STD80	STDM80	
Internal Clock Driver	CK(2/4/8/12)	CK(2/4/6/8)	3-459

Decoders

Cell Type	Cell Name	Page
Non-Inverting Decoder	DC4	3-463
Inverting Decoder	DC4I	3-466
	DC8I	3-469

Adders

Cell Type	Cell Name	Page
Full Adder	FA/FAD2	3-477
Half Adder	HA/HAD2	3-482

Multiplexers

Cell Type	Cell Name	Page
2 > 1 Non-Inverting Mux	MX2/MX2D3	3-486
	MX2X4	3-489
	YMX2/YMX2D2	3-494
2 > 1 Inverting Mux	MX2I/MX2ID2	3-497
	MX2IA/MX2ID2A	3-500
	MX2IX4	3-503
3 > 1 Inverting Mux	MX3I/MX3ID2	3-508
4 > 1 Non-Inverting Mux	MX4/MX4D2	3-511
	YMX4/YMX4D2	3-516
5 > 1 Non-Inverting Mux	MX5/MX5D2	3-521
8 > 1 Non-Inverting Mux	MX8/MX8D2	3-526
	YMX8/YMX8D2	3-532

Cell List

Cell Name	Function Description
AD2	2-Input AND
AD2D2	2-Input AND with 2X Drive
AD3	3-Input AND
AD3D3	3-Input AND with 3X Drive
AD4	4-Input AND
AD4D2	4-Input AND with 2X Drive
AD5	5-Input AND
AD5D2	5-Input AND with 2X Drive
ND2	2-Input NAND
ND2D2	2-Input NAND with 2X Drive
ND3	3-Input NAND
ND3D2	3-Input NAND with 2X Drive
ND4	4-Input NAND
ND4D2	4-Input NAND with 2X Drive
ND5	5-Input NAND
ND5D2	5-Input NAND with 2X Drive
ND6	6-Input NAND
ND6D2	6-Input NAND with 2X Drive
ND8	8-Input NAND
ND8D2	8-Input NAND with 2X Drive
NR2	2-Input NOR
NR2D2	2-Input NOR with 2X Drive
NR3	3-Input NOR
NR3D2	3-Input NOR with 2X Drive
NR4	4-Input NOR
NR4D2	4-Input NOR with 2X Drive
NR5	5-Input NOR
NR5D2	5-Input NOR with 2X Drive
NR6	6-Input NOR
NR6D2	6-Input NOR with 2X Drive
NR8	8-Input NOR
NR8D2	8-Input NOR with 2X Drive
OR2	2-Input OR
OR2D2	2-Input OR with 2X Drive

Cell List (Continued)

Cell Name	Function Description
OR3	3-Input OR
OR3D3	3-Input OR with 3X Drive
OR4	4-Input OR
OR4D2	4-Input OR with 2X Drive
OR5	5-Input OR
OR5D2	5-Input OR with 2X Drive
XN2	2-Input Exclusive-NOR
XN2D2	2-Input Exclusive-NOR with 2X Drive
XN3	3-Input Exclusive-NOR
XN3D3	3-Input Exclusive-NOR with 3X Drive
XO2	2-Input Exclusive-OR
XO2D2	2-Input Exclusive-OR with 2X Drive
XO3	3-Input Exclusive-OR
XO3D3	3-Input Exclusive-OR with 3X Drive
AO21	2-AND into 2-NOR
AO21D2	2-AND into 2-NOR with 2X Drive
AO211	2-AND into 3-NOR
AO211D2	2-AND into 3-NOR with 2X Drive
AO22	Two 2-ANDs into 2-NOR
AO22D2	Two 2-ANDs into 2-NOR with 2X Drive
AO22A	2-AND and 2-NOR into 2-NOR
AO22D2A	2-AND and 2-NOR into 2-NOR with 2X Drive
AO222	Three 2-ANDs into 3-NOR
AO222D2	Three 2-ANDs into 3-NOR with 2X Drive
AO222A	Inverting 2-of-3 Majority
AO222D2A	Inverting 2-of-3 Majority with 2X Drive
AO33	Two 3-ANDs into 2-NOR
AO33D2	Two 3-ANDs into 2-NOR with 2X Drive
AO333	Three 3-ANDs into 3-NOR
AO333D2	Three 3-ANDs into 3-NOR with 2X Drive
OA21	2-OR into 2-NAND
OA21D2	2-OR into 2-NAND with 2X Drive
OA211	2-OR into 3-NAND
OA211D2	2-OR into 3-NAND with 2X Drive

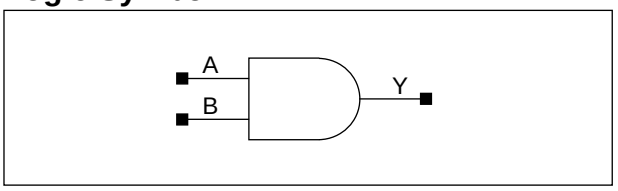
Cell List (Continued)

Cell Name	Function Description
OA22	Two 2-ORs into 2-NAND
OA22D2	Two 2-ORs into 2-NAND with 2X Drive
OA22A	2-OR and 2-NAND into 2-NAND
OA22D2A	2-OR and 2-NAND into 2-NAND with 2X Drive
OA2222	Four 2-ORs into 4-NAND
OA2222D2	Four 2-ORs into 4-NAND with 2X Drive
DL1D2	1 ns Delay Cell with 2X Drive
DL1D4	1 ns Delay Cell with 4X Drive
DL2D2	2 ns Delay Cell with 2X Drive
DL2D4	2 ns Delay Cell with 4X Drive
DL3D2	3 ns Delay Cell with 2X Drive
DL3D4	3 ns Delay Cell with 4X Drive
DL4D2	4 ns Delay Cell with 2X Drive
DL4D4	4 ns Delay Cell with 4X Drive
DL5D2	5 ns Delay Cell with 2X Drive
DL5D4	5 ns Delay Cell with 4X Drive
DL10D2	10 ns Delay Cell with 2X Drive
DL10D4	10 ns Delay Cell with 4X Drive
IV	Inverter
IVD2	Inverter with 2X Drive
IVD3	Inverter with 3X Drive
IVD4	Inverter with 4X Drive
IVD6	Inverter with 6X Drive
IVD8	Inverter with 8X Drive
IVA	Inverter with 2X P-Transistor, 1X N-Transistor
IVD2A	Inverter with 4X P-Transistor, 2X N-Transistor
IVD3A	Inverter with 6X P-Transistor, 3X N-Transistor
IVD4A	Inverter with 8X P-Transistor, 4X N-Transistor
IVCD11	1X Inverter into 1X Inverter
IVCD13	1X Inverter into 3X Inverter
IVCD22	2X Inverter into 2X Inverter
IVCD26	2X Inverter into 6X Inverter
IVCD44	4X Inverter into 4X Inverter
IVT	Inverting Tri-State Buffer with Enable High

Cell List (Continued)

Cell Name	Function Description
IVTD2	Inverting Tri-State Buffer with Enable High, 2X Drive
IVTD4	Inverting Tri-State Buffer with Enable High, 4X Drive
IVTD8	Inverting Tri-State Buffer with Enable High, 8X Drive
IVTN	Inverting Tri-State Buffer with Enable Low
IVTND2	Inverting Tri-State Buffer with Enable Low, 2X Drive
IVTND4	Inverting Tri-State Buffer with Enable Low, 4X Drive
IVTND8	Inverting Tri-State Buffer with Enable Low, 8X Drive
NID	Non-Inverting Buffer
NID2	Non-Inverting Buffer with 2X Drive
NID3	Non-Inverting Buffer with 3X Drive
NID4	Non-Inverting Buffer with 4X Drive
NID6	Non-Inverting Buffer with 6X Drive
NID8	Non-Inverting Buffer with 8X Drive
NIT	Non-Inverting Tri-State Buffer with Enable High
NITD2	Non-Inverting Tri-State Buffer with Enable High, 2X Drive
NITD4	Non-Inverting Tri-State Buffer with Enable High, 4X Drive
NITD8	Non-Inverting Tri-State Buffer with Enable High, 8X Drive
NITN	Non-Inverting Tri-State Buffer with Enable Low
NITND2	Non-Inverting Tri-State Buffer with Enable Low, 2X Drive
NITND4	Non-Inverting Tri-State Buffer with Enable Low, 4X Drive
NITND8	Non-Inverting Tri-State Buffer with Enable Low, 8X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Cell Data

Input Load (SL)				Gate Count	
STD80					
AD2		*AD2D2*		*AD2*	*AD2D2*
A	B	A	B		
0.7	0.6	0.7	0.6	1.3	1.7
STDM80					
AD2/AD2D2		*AD2D2*		*AD2*	*AD2D2*
A	B	A	B		
0.8	0.8	0.7	0.8	1.3	1.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.20 + 0.029*SL	0.21 + 0.024*SL	0.22 + 0.024*SL
	t_{PHL}	0.30	0.22 + 0.039*SL	0.23 + 0.037*SL	0.23 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
B to Y	t_{PLH}	0.24	0.19 + 0.029*SL	0.19 + 0.024*SL	0.20 + 0.024*SL
	t_{PHL}	0.32	0.24 + 0.039*SL	0.25 + 0.037*SL	0.25 + 0.037*SL
	t_R	0.20	0.10 + 0.048*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.06 + 0.069*SL

STD80 AD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.25 + 0.018*SL	0.26 + 0.014*SL	0.28 + 0.012*SL
	t_{PHL}	0.30	0.26 + 0.022*SL	0.27 + 0.019*SL	0.27 + 0.018*SL
	t_R	0.17	0.12 + 0.022*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.15	0.09 + 0.029*SL	0.09 + 0.031*SL	0.06 + 0.034*SL
B to Y	t_{PLH}	0.26	0.23 + 0.018*SL	0.23 + 0.014*SL	0.25 + 0.012*SL
	t_{PHL}	0.32	0.28 + 0.022*SL	0.28 + 0.019*SL	0.29 + 0.018*SL
	t_R	0.17	0.12 + 0.022*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.09 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

AD2/AD2D2

2-Input AND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AD2

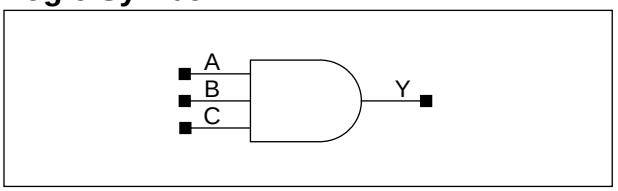
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.37	0.29 + 0.039*SL	0.30 + 0.035*SL	0.31 + 0.033*SL
	t_{PHL}	0.41	0.31 + 0.048*SL	0.32 + 0.045*SL	0.33 + 0.044*SL
	t_R	0.28	0.14 + 0.068*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.28	0.12 + 0.080*SL	0.11 + 0.081*SL	0.10 + 0.083*SL
B to Y	t_{PLH}	0.36	0.28 + 0.039*SL	0.29 + 0.035*SL	0.30 + 0.034*SL
	t_{PHL}	0.43	0.34 + 0.048*SL	0.34 + 0.045*SL	0.35 + 0.044*SL
	t_R	0.28	0.14 + 0.068*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.10 + 0.082*SL

STDM80 AD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.39	0.34 + 0.025*SL	0.35 + 0.021*SL	0.37 + 0.018*SL
	t_{PHL}	0.41	0.35 + 0.029*SL	0.37 + 0.024*SL	0.38 + 0.022*SL
	t_R	0.22	0.15 + 0.034*SL	0.15 + 0.035*SL	0.15 + 0.034*SL
	t_F	0.20	0.12 + 0.039*SL	0.12 + 0.038*SL	0.12 + 0.039*SL
B to Y	t_{PLH}	0.38	0.33 + 0.025*SL	0.34 + 0.021*SL	0.36 + 0.018*SL
	t_{PHL}	0.43	0.37 + 0.029*SL	0.39 + 0.024*SL	0.40 + 0.022*SL
	t_R	0.22	0.15 + 0.033*SL	0.15 + 0.034*SL	0.15 + 0.034*SL
	t_F	0.20	0.12 + 0.039*SL	0.13 + 0.038*SL	0.12 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Cell Data

Input Load (SL)						Gate Count	
STD80							
AD3			*AD3D3*			*AD3*	*AD3D3*
A	B	C	A	B	C		
0.7	0.6	0.6	0.7	0.6	0.6	1.7	2.3
STDM80							
AD3			*AD3D3*			*AD3*	*AD3D3*
A	B	C	A	B	C		
0.8	0.8	0.8	0.8	0.8	0.8	1.7	2.3

AD3/AD3D3

3-Input AND with 1X/3X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.34	0.28 + 0.030*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_{PHL}	0.32	0.24 + 0.039*SL	0.24 + 0.037*SL	0.24 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.067*SL	0.06 + 0.069*SL
B to Y	t_{PLH}	0.33	0.26 + 0.033*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_{PHL}	0.34	0.26 + 0.039*SL	0.26 + 0.037*SL	0.26 + 0.037*SL
	t_R	0.23	0.13 + 0.046*SL	0.13 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.22	0.10 + 0.060*SL	0.09 + 0.067*SL	0.06 + 0.069*SL
C to Y	t_{PLH}	0.32	0.25 + 0.032*SL	0.26 + 0.026*SL	0.29 + 0.024*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.037*SL	0.28 + 0.037*SL
	t_R	0.23	0.15 + 0.039*SL	0.13 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.23	0.10 + 0.062*SL	0.09 + 0.066*SL	0.07 + 0.069*SL

STD80 AD3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.41	0.38 + 0.016*SL	0.39 + 0.012*SL	0.43 + 0.008*SL
	t_{PHL}	0.35	0.32 + 0.015*SL	0.33 + 0.013*SL	0.34 + 0.012*SL
	t_R	0.23	0.19 + 0.019*SL	0.20 + 0.015*SL	0.19 + 0.017*SL
	t_F	0.16	0.12 + 0.019*SL	0.12 + 0.020*SL	0.10 + 0.022*SL
B to Y	t_{PLH}	0.41	0.37 + 0.017*SL	0.38 + 0.012*SL	0.42 + 0.008*SL
	t_{PHL}	0.37	0.34 + 0.016*SL	0.34 + 0.013*SL	0.36 + 0.012*SL
	t_R	0.23	0.20 + 0.014*SL	0.20 + 0.016*SL	0.19 + 0.017*SL
	t_F	0.17	0.12 + 0.021*SL	0.13 + 0.020*SL	0.10 + 0.022*SL
C to Y	t_{PLH}	0.39	0.36 + 0.016*SL	0.37 + 0.012*SL	0.41 + 0.008*SL
	t_{PHL}	0.38	0.35 + 0.016*SL	0.36 + 0.014*SL	0.37 + 0.012*SL
	t_R	0.23	0.20 + 0.014*SL	0.20 + 0.016*SL	0.19 + 0.017*SL
	t_F	0.17	0.13 + 0.020*SL	0.13 + 0.020*SL	0.11 + 0.022*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.40 + 0.045*SL	0.42 + 0.038*SL	0.44 + 0.034*SL
	t_{PHL}	0.44	0.34 + 0.050*SL	0.35 + 0.046*SL	0.36 + 0.044*SL
	t_R	0.32	0.18 + 0.071*SL	0.19 + 0.068*SL	0.18 + 0.070*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.080*SL	0.11 + 0.082*SL
B to Y	t_{PLH}	0.49	0.40 + 0.045*SL	0.42 + 0.038*SL	0.45 + 0.035*SL
	t_{PHL}	0.46	0.36 + 0.050*SL	0.38 + 0.046*SL	0.38 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.19 + 0.068*SL	0.18 + 0.070*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.080*SL	0.12 + 0.082*SL
C to Y	t_{PLH}	0.49	0.40 + 0.045*SL	0.43 + 0.038*SL	0.45 + 0.034*SL
	t_{PHL}	0.48	0.38 + 0.050*SL	0.40 + 0.046*SL	0.41 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.19 + 0.069*SL	0.18 + 0.070*SL
	t_F	0.30	0.14 + 0.078*SL	0.14 + 0.079*SL	0.12 + 0.082*SL

STDM80 AD3D3

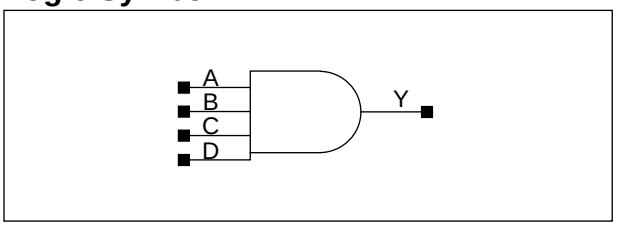
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.60	0.56 + 0.023*SL	0.57 + 0.018*SL	0.59 + 0.016*SL
	t_{PHL}	0.49	0.45 + 0.022*SL	0.46 + 0.019*SL	0.47 + 0.016*SL
	t_R	0.30	0.25 + 0.024*SL	0.26 + 0.024*SL	0.26 + 0.024*SL
	t_F	0.21	0.16 + 0.028*SL	0.16 + 0.027*SL	0.17 + 0.025*SL
B to Y	t_{PLH}	0.61	0.57 + 0.022*SL	0.58 + 0.019*SL	0.60 + 0.016*SL
	t_{PHL}	0.51	0.47 + 0.022*SL	0.48 + 0.019*SL	0.49 + 0.017*SL
	t_R	0.30	0.26 + 0.024*SL	0.26 + 0.024*SL	0.26 + 0.024*SL
	t_F	0.22	0.16 + 0.027*SL	0.17 + 0.026*SL	0.18 + 0.025*SL
C to Y	t_{PLH}	0.61	0.57 + 0.022*SL	0.58 + 0.019*SL	0.60 + 0.016*SL
	t_{PHL}	0.53	0.49 + 0.022*SL	0.50 + 0.019*SL	0.51 + 0.017*SL
	t_R	0.30	0.25 + 0.025*SL	0.26 + 0.024*SL	0.26 + 0.023*SL
	t_F	0.23	0.17 + 0.029*SL	0.18 + 0.025*SL	0.18 + 0.024*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

AD4/AD4D2

4-Input AND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Cell Data

Input Load (SL)								Gate Count	
STD80									
AD4				*AD4D2*				*AD4*	*AD4D2*
A	B	C	D	A	B	C	D		
0.6	0.6	0.6	0.7	0.7	0.6	0.6	0.6	2.0	2.3
STDM80									
AD4				*AD4D2*				*AD4*	*AD4D2*
A	B	C	D	A	B	C	D		
0.7	0.8	0.8	0.8	0.7	0.8	0.8	0.8	2.0	2.3

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.39	0.32 + 0.035*SL	0.33 + 0.027*SL	0.37 + 0.024*SL
	t_{PHL}	0.32	0.24 + 0.040*SL	0.24 + 0.037*SL	0.24 + 0.037*SL
	t_R	0.25	0.16 + 0.047*SL	0.15 + 0.049*SL	0.13 + 0.051*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.06 + 0.069*SL
B to Y	t_{PLH}	0.39	0.31 + 0.037*SL	0.33 + 0.027*SL	0.37 + 0.024*SL
	t_{PHL}	0.34	0.26 + 0.039*SL	0.26 + 0.037*SL	0.26 + 0.037*SL
	t_R	0.25	0.17 + 0.044*SL	0.16 + 0.048*SL	0.13 + 0.051*SL
	t_F	0.23	0.10 + 0.064*SL	0.09 + 0.066*SL	0.07 + 0.069*SL
C to Y	t_{PLH}	0.38	0.31 + 0.035*SL	0.33 + 0.027*SL	0.37 + 0.024*SL
	t_{PHL}	0.35	0.27 + 0.039*SL	0.28 + 0.037*SL	0.28 + 0.037*SL
	t_R	0.26	0.16 + 0.048*SL	0.16 + 0.048*SL	0.13 + 0.051*SL
	t_F	0.23	0.10 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
D to Y	t_{PLH}	0.38	0.31 + 0.035*SL	0.33 + 0.027*SL	0.36 + 0.024*SL
	t_{PHL}	0.37	0.29 + 0.040*SL	0.29 + 0.037*SL	0.29 + 0.037*SL
	t_R	0.25	0.16 + 0.046*SL	0.16 + 0.048*SL	0.13 + 0.051*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL

STD80 AD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.45	0.40 + 0.025*SL	0.42 + 0.018*SL	0.47 + 0.012*SL
	t_{PHL}	0.34	0.29 + 0.023*SL	0.30 + 0.019*SL	0.31 + 0.018*SL
	t_R	0.26	0.20 + 0.028*SL	0.21 + 0.024*SL	0.20 + 0.025*SL
	t_F	0.17	0.11 + 0.029*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
B to Y	t_{PLH}	0.46	0.41 + 0.025*SL	0.42 + 0.018*SL	0.48 + 0.012*SL
	t_{PHL}	0.35	0.31 + 0.023*SL	0.32 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.26	0.20 + 0.028*SL	0.21 + 0.024*SL	0.20 + 0.025*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
C to Y	t_{PLH}	0.45	0.40 + 0.025*SL	0.42 + 0.018*SL	0.47 + 0.012*SL
	t_{PHL}	0.37	0.32 + 0.023*SL	0.33 + 0.019*SL	0.34 + 0.018*SL
	t_R	0.26	0.20 + 0.029*SL	0.21 + 0.024*SL	0.20 + 0.025*SL
	t_F	0.18	0.12 + 0.029*SL	0.12 + 0.031*SL	0.08 + 0.034*SL
D to Y	t_{PLH}	0.45	0.40 + 0.025*SL	0.41 + 0.018*SL	0.47 + 0.012*SL
	t_{PHL}	0.38	0.33 + 0.023*SL	0.34 + 0.020*SL	0.36 + 0.018*SL
	t_R	0.26	0.20 + 0.029*SL	0.21 + 0.024*SL	0.20 + 0.025*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.031*SL	0.09 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AD4

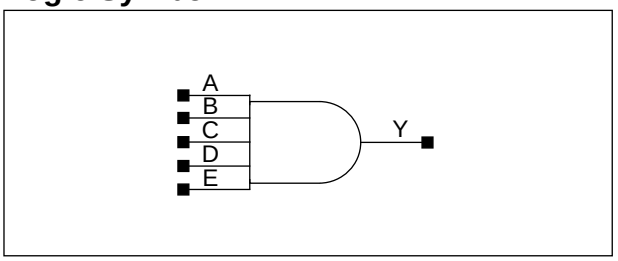
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.57	0.47 + 0.050*SL	0.49 + 0.041*SL	0.53 + 0.036*SL
	t_{PHL}	0.45	0.35 + 0.050*SL	0.36 + 0.046*SL	0.37 + 0.044*SL
	t_R	0.36	0.22 + 0.072*SL	0.23 + 0.070*SL	0.23 + 0.069*SL
	t_F	0.29	0.13 + 0.079*SL	0.13 + 0.080*SL	0.12 + 0.082*SL
B to Y	t_{PLH}	0.59	0.49 + 0.050*SL	0.52 + 0.041*SL	0.55 + 0.036*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.046*SL	0.39 + 0.044*SL
	t_R	0.36	0.22 + 0.073*SL	0.23 + 0.070*SL	0.23 + 0.069*SL
	t_F	0.29	0.14 + 0.078*SL	0.13 + 0.080*SL	0.12 + 0.082*SL
C to Y	t_{PLH}	0.60	0.50 + 0.050*SL	0.53 + 0.041*SL	0.56 + 0.036*SL
	t_{PHL}	0.49	0.39 + 0.050*SL	0.40 + 0.046*SL	0.41 + 0.044*SL
	t_R	0.36	0.22 + 0.072*SL	0.23 + 0.069*SL	0.23 + 0.069*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.079*SL	0.12 + 0.082*SL
D to Y	t_{PLH}	0.61	0.51 + 0.050*SL	0.54 + 0.041*SL	0.57 + 0.036*SL
	t_{PHL}	0.51	0.40 + 0.052*SL	0.42 + 0.046*SL	0.43 + 0.045*SL
	t_R	0.36	0.22 + 0.071*SL	0.23 + 0.069*SL	0.23 + 0.069*SL
	t_F	0.30	0.14 + 0.079*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

STDM80 AD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.62	0.56 + 0.033*SL	0.58 + 0.026*SL	0.61 + 0.022*SL
	t_{PHL}	0.44	0.38 + 0.030*SL	0.40 + 0.025*SL	0.41 + 0.023*SL
	t_R	0.32	0.24 + 0.039*SL	0.25 + 0.037*SL	0.26 + 0.035*SL
	t_F	0.21	0.13 + 0.039*SL	0.13 + 0.039*SL	0.14 + 0.038*SL
B to Y	t_{PLH}	0.65	0.58 + 0.033*SL	0.60 + 0.026*SL	0.63 + 0.022*SL
	t_{PHL}	0.47	0.40 + 0.030*SL	0.42 + 0.026*SL	0.44 + 0.023*SL
	t_R	0.32	0.25 + 0.038*SL	0.25 + 0.037*SL	0.26 + 0.035*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.038*SL	0.14 + 0.038*SL
C to Y	t_{PLH}	0.66	0.60 + 0.033*SL	0.62 + 0.026*SL	0.65 + 0.022*SL
	t_{PHL}	0.48	0.42 + 0.031*SL	0.44 + 0.026*SL	0.46 + 0.023*SL
	t_R	0.32	0.24 + 0.039*SL	0.25 + 0.037*SL	0.26 + 0.035*SL
	t_F	0.22	0.14 + 0.041*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
D to Y	t_{PLH}	0.67	0.60 + 0.033*SL	0.63 + 0.026*SL	0.65 + 0.022*SL
	t_{PHL}	0.50	0.44 + 0.031*SL	0.45 + 0.026*SL	0.47 + 0.023*SL
	t_R	0.32	0.24 + 0.039*SL	0.25 + 0.037*SL	0.26 + 0.035*SL
	t_F	0.23	0.15 + 0.039*SL	0.15 + 0.038*SL	0.15 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	x	x	x	0
x	0	x	x	x	0
x	x	0	x	x	0
x	x	x	0	x	0
x	x	x	x	0	0
1	1	1	1	1	1

Cell Data

Input Load (SL)										Gate Count	
STD80											
AD5					*AD5D2*					*AD5*	*AD5D2*
A	B	C	D	E	A	B	C	D	E		
0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	3.0	3.7
STDM80											
AD5					*AD5D2*					*AD5*	*AD5D2*
A	B	C	D	E	A	B	C	D	E		
0.7	0.8	0.8	0.8	0.8	0.7	0.8	0.8	0.8	0.8	3.0	3.7

AD5/AD5D2

5-Input AND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.39	0.30 + 0.044*SL	0.31 + 0.039*SL	0.32 + 0.038*SL
	t_{PHL}	0.38	0.30 + 0.040*SL	0.31 + 0.038*SL	0.31 + 0.037*SL
	t_R	0.35	0.19 + 0.080*SL	0.19 + 0.083*SL	0.15 + 0.086*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
B to Y	t_{PLH}	0.40	0.31 + 0.044*SL	0.33 + 0.039*SL	0.33 + 0.038*SL
	t_{PHL}	0.37	0.29 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.35	0.19 + 0.080*SL	0.19 + 0.083*SL	0.15 + 0.086*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
C to Y	t_{PLH}	0.41	0.32 + 0.045*SL	0.33 + 0.039*SL	0.34 + 0.038*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.27 + 0.038*SL	0.28 + 0.037*SL
	t_R	0.35	0.19 + 0.081*SL	0.19 + 0.083*SL	0.15 + 0.086*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
D to Y	t_{PLH}	0.34	0.25 + 0.042*SL	0.26 + 0.039*SL	0.27 + 0.038*SL
	t_{PHL}	0.39	0.31 + 0.039*SL	0.31 + 0.037*SL	0.32 + 0.037*SL
	t_R	0.33	0.17 + 0.081*SL	0.17 + 0.084*SL	0.15 + 0.086*SL
	t_F	0.30	0.18 + 0.062*SL	0.17 + 0.067*SL	0.14 + 0.069*SL
E to Y	t_{PLH}	0.36	0.27 + 0.042*SL	0.28 + 0.039*SL	0.29 + 0.038*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.33	0.17 + 0.081*SL	0.17 + 0.084*SL	0.15 + 0.086*SL
	t_F	0.30	0.17 + 0.063*SL	0.16 + 0.067*SL	0.14 + 0.069*SL

STD80 AD5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.41	0.36 + 0.025*SL	0.37 + 0.021*SL	0.39 + 0.019*SL
	t_{PHL}	0.38	0.34 + 0.023*SL	0.34 + 0.020*SL	0.36 + 0.018*SL
	t_R	0.29	0.22 + 0.035*SL	0.21 + 0.039*SL	0.18 + 0.043*SL
	t_F	0.19	0.13 + 0.030*SL	0.13 + 0.031*SL	0.09 + 0.034*SL
B to Y	t_{PLH}	0.42	0.37 + 0.026*SL	0.38 + 0.021*SL	0.41 + 0.019*SL
	t_{PHL}	0.37	0.32 + 0.023*SL	0.33 + 0.020*SL	0.34 + 0.018*SL
	t_R	0.29	0.22 + 0.035*SL	0.21 + 0.039*SL	0.18 + 0.043*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
C to Y	t_{PLH}	0.43	0.38 + 0.026*SL	0.39 + 0.021*SL	0.41 + 0.019*SL
	t_{PHL}	0.35	0.31 + 0.023*SL	0.31 + 0.020*SL	0.33 + 0.018*SL
	t_R	0.29	0.22 + 0.036*SL	0.21 + 0.039*SL	0.18 + 0.043*SL
	t_F	0.18	0.11 + 0.031*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
D to Y	t_{PLH}	0.35	0.30 + 0.023*SL	0.31 + 0.021*SL	0.33 + 0.019*SL
	t_{PHL}	0.39	0.35 + 0.020*SL	0.35 + 0.019*SL	0.36 + 0.018*SL
	t_R	0.26	0.18 + 0.041*SL	0.18 + 0.041*SL	0.16 + 0.043*SL
	t_F	0.25	0.19 + 0.029*SL	0.18 + 0.031*SL	0.15 + 0.034*SL
E to Y	t_{PLH}	0.37	0.32 + 0.027*SL	0.33 + 0.021*SL	0.35 + 0.019*SL
	t_{PHL}	0.37	0.33 + 0.020*SL	0.33 + 0.019*SL	0.34 + 0.018*SL
	t_R	0.26	0.19 + 0.034*SL	0.17 + 0.041*SL	0.16 + 0.043*SL
	t_F	0.24	0.19 + 0.029*SL	0.18 + 0.031*SL	0.15 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.57	0.44 + 0.065*SL	0.46 + 0.059*SL	0.47 + 0.057*SL
	t_{PHL}	0.50	0.40 + 0.051*SL	0.42 + 0.046*SL	0.43 + 0.044*SL
	t_R	0.51	0.27 + 0.121*SL	0.26 + 0.122*SL	0.25 + 0.124*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
B to Y	t_{PLH}	0.57	0.44 + 0.065*SL	0.46 + 0.059*SL	0.47 + 0.057*SL
	t_{PHL}	0.48	0.38 + 0.050*SL	0.40 + 0.046*SL	0.40 + 0.045*SL
	t_R	0.51	0.27 + 0.121*SL	0.26 + 0.122*SL	0.25 + 0.124*SL
	t_F	0.30	0.14 + 0.079*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
C to Y	t_{PLH}	0.57	0.44 + 0.065*SL	0.45 + 0.059*SL	0.47 + 0.057*SL
	t_{PHL}	0.46	0.36 + 0.050*SL	0.37 + 0.046*SL	0.38 + 0.044*SL
	t_R	0.51	0.27 + 0.121*SL	0.26 + 0.122*SL	0.25 + 0.124*SL
	t_F	0.30	0.14 + 0.080*SL	0.13 + 0.081*SL	0.13 + 0.082*SL
D to Y	t_{PLH}	0.49	0.37 + 0.062*SL	0.38 + 0.059*SL	0.39 + 0.057*SL
	t_{PHL}	0.50	0.41 + 0.048*SL	0.41 + 0.046*SL	0.42 + 0.044*SL
	t_R	0.48	0.24 + 0.122*SL	0.24 + 0.124*SL	0.23 + 0.125*SL
	t_F	0.36	0.20 + 0.080*SL	0.20 + 0.081*SL	0.19 + 0.082*SL
E to Y	t_{PLH}	0.50	0.38 + 0.063*SL	0.39 + 0.059*SL	0.40 + 0.057*SL
	t_{PHL}	0.48	0.38 + 0.048*SL	0.39 + 0.045*SL	0.39 + 0.045*SL
	t_R	0.49	0.24 + 0.122*SL	0.24 + 0.124*SL	0.23 + 0.125*SL
	t_F	0.36	0.20 + 0.080*SL	0.20 + 0.081*SL	0.19 + 0.082*SL

STDM80 AD5D2

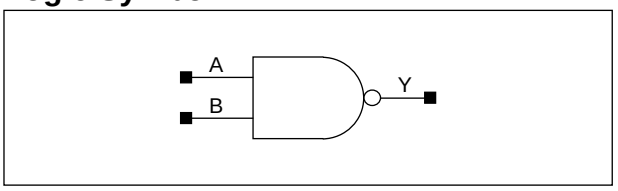
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.59	0.52 + 0.037*SL	0.53 + 0.033*SL	0.55 + 0.030*SL
	t_{PHL}	0.50	0.44 + 0.030*SL	0.46 + 0.026*SL	0.48 + 0.023*SL
	t_R	0.38	0.26 + 0.062*SL	0.26 + 0.061*SL	0.26 + 0.061*SL
	t_F	0.23	0.15 + 0.040*SL	0.16 + 0.038*SL	0.15 + 0.038*SL
B to Y	t_{PLH}	0.60	0.52 + 0.037*SL	0.53 + 0.033*SL	0.55 + 0.030*SL
	t_{PHL}	0.49	0.43 + 0.030*SL	0.44 + 0.026*SL	0.46 + 0.023*SL
	t_R	0.38	0.26 + 0.061*SL	0.26 + 0.061*SL	0.26 + 0.061*SL
	t_F	0.22	0.15 + 0.038*SL	0.15 + 0.039*SL	0.15 + 0.038*SL
C to Y	t_{PLH}	0.59	0.51 + 0.037*SL	0.53 + 0.033*SL	0.54 + 0.031*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.42 + 0.025*SL	0.43 + 0.023*SL
	t_R	0.38	0.26 + 0.060*SL	0.26 + 0.062*SL	0.27 + 0.060*SL
	t_F	0.22	0.14 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.039*SL
D to Y	t_{PLH}	0.50	0.42 + 0.037*SL	0.43 + 0.033*SL	0.45 + 0.030*SL
	t_{PHL}	0.51	0.45 + 0.027*SL	0.46 + 0.024*SL	0.47 + 0.022*SL
	t_R	0.35	0.23 + 0.064*SL	0.23 + 0.062*SL	0.23 + 0.062*SL
	t_F	0.29	0.22 + 0.037*SL	0.22 + 0.037*SL	0.21 + 0.038*SL
E to Y	t_{PLH}	0.50	0.43 + 0.038*SL	0.44 + 0.033*SL	0.46 + 0.031*SL
	t_{PHL}	0.48	0.43 + 0.026*SL	0.44 + 0.024*SL	0.45 + 0.022*SL
	t_R	0.35	0.23 + 0.064*SL	0.23 + 0.062*SL	0.23 + 0.062*SL
	t_F	0.29	0.21 + 0.037*SL	0.21 + 0.037*SL	0.21 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

ND2/ND2D2

2-Input NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Cell Data

Input Load (SL)				Gate Count	
STD80					
ND2		*ND2D2*		*ND2*	*ND2D2*
A	B	A	B		
1.1	1.1	2.0	2.0	1.0	1.7
STDM80					
ND2		*ND2D2*		*ND2*	*ND2D2*
A	B	A	B		
1.1	1.1	2.2	2.2	1.0	1.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 ND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.18	0.11 + 0.033*SL	0.13 + 0.025*SL	0.13 + 0.025*SL
	t_{PHL}	0.18	0.10 + 0.041*SL	0.11 + 0.038*SL	0.10 + 0.038*SL
	t_R	0.30	0.22 + 0.041*SL	0.21 + 0.046*SL	0.13 + 0.054*SL
	t_F	0.31	0.18 + 0.065*SL	0.17 + 0.071*SL	0.10 + 0.078*SL
B to Y	t_{PLH}	0.16	0.09 + 0.037*SL	0.11 + 0.026*SL	0.12 + 0.025*SL
	t_{PHL}	0.21	0.12 + 0.044*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
	t_R	0.28	0.19 + 0.044*SL	0.19 + 0.046*SL	0.11 + 0.054*SL
	t_F	0.32	0.19 + 0.065*SL	0.18 + 0.071*SL	0.11 + 0.078*SL

STD80 ND2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.13	0.09 + 0.020*SL	0.10 + 0.015*SL	0.13 + 0.012*SL
	t_{PHL}	0.15	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.019*SL
	t_R	0.24	0.20 + 0.022*SL	0.20 + 0.022*SL	0.15 + 0.027*SL
	t_F	0.24	0.17 + 0.033*SL	0.17 + 0.034*SL	0.13 + 0.039*SL
B to Y	t_{PLH}	0.13	0.09 + 0.020*SL	0.10 + 0.015*SL	0.13 + 0.012*SL
	t_{PHL}	0.15	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.019*SL
	t_R	0.25	0.20 + 0.023*SL	0.20 + 0.021*SL	0.15 + 0.027*SL
	t_F	0.24	0.17 + 0.033*SL	0.17 + 0.034*SL	0.13 + 0.039*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 ND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.15 + 0.037*SL	0.16 + 0.034*SL	0.16 + 0.035*SL
	t_{PHL}	0.24	0.13 + 0.052*SL	0.14 + 0.050*SL	0.14 + 0.050*SL
	t_R	0.33	0.21 + 0.063*SL	0.19 + 0.070*SL	0.16 + 0.073*SL
	t_F	0.35	0.17 + 0.091*SL	0.15 + 0.096*SL	0.14 + 0.098*SL
B to Y	t_{PLH}	0.21	0.13 + 0.040*SL	0.14 + 0.035*SL	0.14 + 0.035*SL
	t_{PHL}	0.25	0.15 + 0.052*SL	0.15 + 0.050*SL	0.15 + 0.050*SL
	t_R	0.31	0.18 + 0.064*SL	0.16 + 0.070*SL	0.14 + 0.073*SL
	t_F	0.36	0.18 + 0.089*SL	0.16 + 0.095*SL	0.14 + 0.098*SL

STDM80 ND2D2

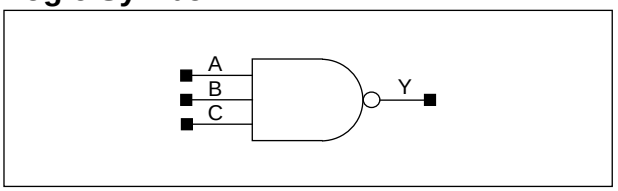
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.17	0.12 + 0.023*SL	0.14 + 0.019*SL	0.15 + 0.017*SL
	t_{PHL}	0.18	0.12 + 0.029*SL	0.14 + 0.025*SL	0.14 + 0.025*SL
	t_R	0.25	0.19 + 0.029*SL	0.18 + 0.032*SL	0.16 + 0.035*SL
	t_F	0.25	0.17 + 0.043*SL	0.16 + 0.046*SL	0.15 + 0.048*SL
B to Y	t_{PLH}	0.17	0.12 + 0.023*SL	0.14 + 0.018*SL	0.15 + 0.017*SL
	t_{PHL}	0.18	0.13 + 0.029*SL	0.14 + 0.025*SL	0.14 + 0.025*SL
	t_R	0.25	0.19 + 0.029*SL	0.18 + 0.032*SL	0.16 + 0.035*SL
	t_F	0.26	0.17 + 0.042*SL	0.16 + 0.046*SL	0.15 + 0.048*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

ND3/ND3D2

3-Input NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Cell Data

Input Load (SL)						Gate Count	
STD80							
ND3			*ND3D2*			*ND3*	*ND3D2*
A	B	C	A	B	C		
1.0	1.0	1.0	2.0	2.0	2.0	1.3	2.3
STDM80							
ND3			*ND3D2*			*ND3*	*ND3D2*
A	B	C	A	B	C		
1.1	1.1	1.1	2.2	2.2	2.3	1.3	2.3

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 ND3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.14 + 0.031*SL	0.15 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.25	0.15 + 0.050*SL	0.15 + 0.050*SL	0.14 + 0.051*SL
	t_R	0.35	0.27 + 0.039*SL	0.26 + 0.046*SL	0.18 + 0.054*SL
	t_F	0.43	0.24 + 0.096*SL	0.22 + 0.103*SL	0.19 + 0.107*SL
B to Y	t_{PLH}	0.17	0.10 + 0.035*SL	0.12 + 0.026*SL	0.13 + 0.025*SL
	t_{PHL}	0.28	0.18 + 0.051*SL	0.18 + 0.050*SL	0.17 + 0.051*SL
	t_R	0.30	0.22 + 0.040*SL	0.21 + 0.046*SL	0.14 + 0.054*SL
	t_F	0.45	0.26 + 0.095*SL	0.24 + 0.102*SL	0.19 + 0.107*SL
C to Y	t_{PLH}	0.19	0.12 + 0.033*SL	0.14 + 0.025*SL	0.14 + 0.025*SL
	t_{PHL}	0.27	0.17 + 0.051*SL	0.17 + 0.050*SL	0.16 + 0.051*SL
	t_R	0.32	0.24 + 0.040*SL	0.23 + 0.046*SL	0.16 + 0.054*SL
	t_F	0.44	0.25 + 0.093*SL	0.23 + 0.103*SL	0.19 + 0.107*SL

STD80 ND3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.13	0.09 + 0.021*SL	0.10 + 0.015*SL	0.13 + 0.012*SL
	t_{PHL}	0.22	0.17 + 0.027*SL	0.18 + 0.025*SL	0.17 + 0.025*SL
	t_R	0.26	0.22 + 0.023*SL	0.22 + 0.022*SL	0.17 + 0.027*SL
	t_F	0.34	0.25 + 0.046*SL	0.24 + 0.049*SL	0.20 + 0.053*SL
B to Y	t_{PLH}	0.17	0.13 + 0.018*SL	0.14 + 0.014*SL	0.16 + 0.012*SL
	t_{PHL}	0.20	0.15 + 0.026*SL	0.15 + 0.025*SL	0.15 + 0.025*SL
	t_R	0.31	0.27 + 0.018*SL	0.26 + 0.021*SL	0.21 + 0.027*SL
	t_F	0.33	0.24 + 0.046*SL	0.23 + 0.050*SL	0.19 + 0.053*SL
C to Y	t_{PLH}	0.15	0.12 + 0.018*SL	0.12 + 0.014*SL	0.15 + 0.012*SL
	t_{PHL}	0.21	0.16 + 0.027*SL	0.16 + 0.025*SL	0.16 + 0.025*SL
	t_R	0.28	0.24 + 0.020*SL	0.24 + 0.022*SL	0.19 + 0.027*SL
	t_F	0.34	0.25 + 0.046*SL	0.24 + 0.049*SL	0.20 + 0.053*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 ND3

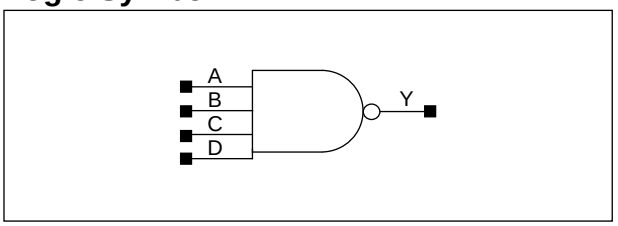
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.19 + 0.035*SL	0.19 + 0.035*SL	0.19 + 0.035*SL
	t_{PHL}	0.36	0.22 + 0.069*SL	0.22 + 0.069*SL	0.22 + 0.069*SL
	t_R	0.40	0.27 + 0.065*SL	0.25 + 0.070*SL	0.23 + 0.073*SL
	t_F	0.56	0.28 + 0.137*SL	0.28 + 0.139*SL	0.27 + 0.140*SL
B to Y	t_{PLH}	0.23	0.15 + 0.038*SL	0.16 + 0.035*SL	0.16 + 0.035*SL
	t_{PHL}	0.35	0.22 + 0.069*SL	0.22 + 0.068*SL	0.22 + 0.068*SL
	t_R	0.35	0.22 + 0.065*SL	0.20 + 0.071*SL	0.18 + 0.073*SL
	t_F	0.56	0.30 + 0.134*SL	0.28 + 0.138*SL	0.26 + 0.141*SL
C to Y	t_{PLH}	0.25	0.17 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.36	0.22 + 0.069*SL	0.22 + 0.069*SL	0.23 + 0.068*SL
	t_R	0.37	0.24 + 0.064*SL	0.22 + 0.071*SL	0.21 + 0.073*SL
	t_F	0.56	0.29 + 0.135*SL	0.28 + 0.138*SL	0.27 + 0.140*SL

STDM80 ND3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.14 + 0.022*SL	0.15 + 0.018*SL	0.16 + 0.017*SL
	t_{PHL}	0.28	0.21 + 0.034*SL	0.21 + 0.034*SL	0.21 + 0.034*SL
	t_R	0.28	0.22 + 0.030*SL	0.21 + 0.033*SL	0.20 + 0.035*SL
	t_F	0.42	0.29 + 0.064*SL	0.28 + 0.068*SL	0.27 + 0.069*SL
B to Y	t_{PLH}	0.22	0.18 + 0.020*SL	0.19 + 0.017*SL	0.19 + 0.017*SL
	t_{PHL}	0.28	0.21 + 0.035*SL	0.22 + 0.035*SL	0.22 + 0.034*SL
	t_R	0.33	0.27 + 0.031*SL	0.26 + 0.033*SL	0.25 + 0.034*SL
	t_F	0.41	0.27 + 0.067*SL	0.27 + 0.069*SL	0.26 + 0.069*SL
C to Y	t_{PLH}	0.21	0.16 + 0.021*SL	0.17 + 0.017*SL	0.18 + 0.017*SL
	t_{PHL}	0.29	0.22 + 0.035*SL	0.22 + 0.034*SL	0.22 + 0.034*SL
	t_R	0.30	0.24 + 0.030*SL	0.23 + 0.033*SL	0.22 + 0.035*SL
	t_F	0.41	0.28 + 0.066*SL	0.28 + 0.068*SL	0.27 + 0.069*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Cell Data

Input Load (SL)								Gate Count	
STD80									
ND4				*ND4D2*				*ND4*	*ND4D2*
A	B	C	D	A	B	C	D		
1.1	1.1	1.1	1.1	2.0	2.0	2.0	2.0	1.7	3.0
STDM80									
ND4				*ND4D2*				*ND4*	*ND4D2*
A	B	C	D	A	B	C	D		
1.1	1.1	1.1	1.1	2.4	2.2	2.3	2.3	1.7	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 ND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.14 + 0.032*SL	0.16 + 0.025*SL	0.16 + 0.025*SL
	t_{PHL}	0.32	0.20 + 0.062*SL	0.19 + 0.063*SL	0.19 + 0.063*SL
	t_R	0.37	0.29 + 0.041*SL	0.28 + 0.046*SL	0.21 + 0.054*SL
	t_F	0.56	0.30 + 0.127*SL	0.29 + 0.134*SL	0.27 + 0.136*SL
B to Y	t_{PLH}	0.19	0.12 + 0.033*SL	0.14 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.33	0.21 + 0.061*SL	0.21 + 0.062*SL	0.20 + 0.063*SL
	t_R	0.33	0.25 + 0.039*SL	0.23 + 0.047*SL	0.16 + 0.054*SL
	t_F	0.57	0.32 + 0.127*SL	0.30 + 0.133*SL	0.27 + 0.136*SL
C to Y	t_{PLH}	0.20	0.14 + 0.032*SL	0.15 + 0.025*SL	0.16 + 0.025*SL
	t_{PHL}	0.33	0.20 + 0.062*SL	0.20 + 0.063*SL	0.20 + 0.063*SL
	t_R	0.35	0.27 + 0.040*SL	0.26 + 0.046*SL	0.19 + 0.054*SL
	t_F	0.57	0.31 + 0.128*SL	0.30 + 0.133*SL	0.27 + 0.136*SL
D to Y	t_{PLH}	0.17	0.10 + 0.035*SL	0.12 + 0.026*SL	0.14 + 0.025*SL
	t_{PHL}	0.33	0.21 + 0.060*SL	0.21 + 0.062*SL	0.19 + 0.063*SL
	t_R	0.31	0.23 + 0.040*SL	0.21 + 0.047*SL	0.15 + 0.054*SL
	t_F	0.57	0.32 + 0.125*SL	0.30 + 0.132*SL	0.27 + 0.136*SL

STD80 ND4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.18	0.14 + 0.018*SL	0.15 + 0.014*SL	0.17 + 0.012*SL
	t_{PHL}	0.26	0.19 + 0.033*SL	0.20 + 0.031*SL	0.19 + 0.032*SL
	t_R	0.33	0.29 + 0.020*SL	0.29 + 0.022*SL	0.24 + 0.027*SL
	t_F	0.43	0.30 + 0.065*SL	0.30 + 0.065*SL	0.27 + 0.068*SL
B to Y	t_{PLH}	0.14	0.10 + 0.020*SL	0.11 + 0.015*SL	0.14 + 0.012*SL
	t_{PHL}	0.27	0.21 + 0.031*SL	0.21 + 0.031*SL	0.20 + 0.032*SL
	t_R	0.27	0.22 + 0.023*SL	0.22 + 0.022*SL	0.18 + 0.027*SL
	t_F	0.44	0.32 + 0.061*SL	0.31 + 0.064*SL	0.27 + 0.068*SL
C to Y	t_{PLH}	0.17	0.13 + 0.018*SL	0.14 + 0.014*SL	0.16 + 0.012*SL
	t_{PHL}	0.26	0.20 + 0.032*SL	0.20 + 0.031*SL	0.20 + 0.032*SL
	t_R	0.31	0.27 + 0.018*SL	0.27 + 0.022*SL	0.22 + 0.027*SL
	t_F	0.43	0.31 + 0.060*SL	0.30 + 0.065*SL	0.27 + 0.068*SL
D to Y	t_{PLH}	0.15	0.12 + 0.018*SL	0.13 + 0.015*SL	0.15 + 0.012*SL
	t_{PHL}	0.27	0.20 + 0.032*SL	0.21 + 0.031*SL	0.20 + 0.032*SL
	t_R	0.29	0.25 + 0.021*SL	0.25 + 0.022*SL	0.20 + 0.027*SL
	t_F	0.44	0.31 + 0.061*SL	0.31 + 0.065*SL	0.27 + 0.068*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 ND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.27	0.20 + 0.036*SL	0.20 + 0.036*SL	0.21 + 0.035*SL
	t_{PHL}	0.47	0.29 + 0.089*SL	0.30 + 0.088*SL	0.30 + 0.087*SL
	t_R	0.43	0.30 + 0.065*SL	0.29 + 0.070*SL	0.27 + 0.073*SL
	t_F	0.75	0.39 + 0.180*SL	0.39 + 0.181*SL	0.38 + 0.182*SL
B to Y	t_{PLH}	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.45	0.28 + 0.088*SL	0.28 + 0.088*SL	0.28 + 0.087*SL
	t_R	0.38	0.25 + 0.067*SL	0.23 + 0.071*SL	0.21 + 0.073*SL
	t_F	0.76	0.40 + 0.177*SL	0.40 + 0.180*SL	0.38 + 0.182*SL
C to Y	t_{PLH}	0.26	0.19 + 0.035*SL	0.19 + 0.035*SL	0.20 + 0.035*SL
	t_{PHL}	0.47	0.29 + 0.089*SL	0.29 + 0.088*SL	0.30 + 0.087*SL
	t_R	0.40	0.27 + 0.065*SL	0.26 + 0.070*SL	0.24 + 0.073*SL
	t_F	0.76	0.40 + 0.178*SL	0.39 + 0.181*SL	0.38 + 0.182*SL
D to Y	t_{PLH}	0.23	0.16 + 0.037*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_{PHL}	0.43	0.26 + 0.088*SL	0.26 + 0.087*SL	0.26 + 0.087*SL
	t_R	0.36	0.23 + 0.066*SL	0.21 + 0.071*SL	0.19 + 0.073*SL
	t_F	0.75	0.40 + 0.177*SL	0.39 + 0.181*SL	0.38 + 0.182*SL

STDM80 ND4D2

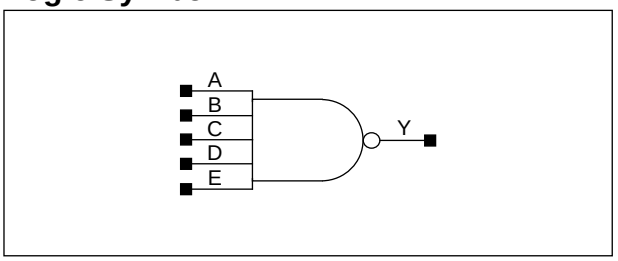
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.20 + 0.019*SL	0.20 + 0.018*SL	0.20 + 0.018*SL
	t_{PHL}	0.38	0.29 + 0.045*SL	0.30 + 0.045*SL	0.30 + 0.044*SL
	t_R	0.36	0.30 + 0.032*SL	0.29 + 0.033*SL	0.28 + 0.035*SL
	t_F	0.56	0.39 + 0.089*SL	0.38 + 0.090*SL	0.38 + 0.091*SL
B to Y	t_{PLH}	0.19	0.15 + 0.022*SL	0.16 + 0.018*SL	0.17 + 0.017*SL
	t_{PHL}	0.34	0.25 + 0.044*SL	0.26 + 0.044*SL	0.26 + 0.044*SL
	t_R	0.29	0.23 + 0.031*SL	0.22 + 0.033*SL	0.21 + 0.035*SL
	t_F	0.57	0.39 + 0.088*SL	0.39 + 0.089*SL	0.38 + 0.090*SL
C to Y	t_{PLH}	0.23	0.19 + 0.019*SL	0.19 + 0.017*SL	0.19 + 0.018*SL
	t_{PHL}	0.38	0.29 + 0.044*SL	0.29 + 0.044*SL	0.29 + 0.044*SL
	t_R	0.34	0.28 + 0.030*SL	0.27 + 0.033*SL	0.25 + 0.035*SL
	t_F	0.57	0.39 + 0.088*SL	0.39 + 0.089*SL	0.38 + 0.090*SL
D to Y	t_{PLH}	0.21	0.17 + 0.020*SL	0.18 + 0.017*SL	0.18 + 0.017*SL
	t_{PHL}	0.36	0.28 + 0.044*SL	0.27 + 0.044*SL	0.28 + 0.044*SL
	t_R	0.31	0.25 + 0.030*SL	0.24 + 0.033*SL	0.23 + 0.035*SL
	t_F	0.57	0.40 + 0.088*SL	0.39 + 0.089*SL	0.39 + 0.090*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

ND5/ND5D2

5-Input NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	x	x	x	1
x	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
1	1	1	1	1	0

Cell Data

Input Load (SL)										Gate Count	
STD80											
ND5					*ND5D2*					*ND5*	*ND5D2*
A	B	C	D	E	A	B	C	D	E		
1.0	1.0	1.0	1.0	1.0	2.0	2.0	2.0	2.0	2.0	2.0	3.7
STDM80											
ND5					*ND5D2*					*ND5*	*ND5D2*
A	B	C	D	E	A	B	C	D	E		
1.1	1.1	1.1	1.1	1.1	2.5	2.5	2.2	2.3	2.3	2.0	3.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 ND5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.17 + 0.030*SL	0.18 + 0.025*SL	0.18 + 0.025*SL
	t_{PHL}	0.44	0.29 + 0.076*SL	0.29 + 0.076*SL	0.29 + 0.076*SL
	t_R	0.42	0.33 + 0.042*SL	0.32 + 0.047*SL	0.26 + 0.054*SL
	t_F	0.77	0.45 + 0.160*SL	0.44 + 0.164*SL	0.43 + 0.165*SL
B to Y	t_{PLH}	0.22	0.16 + 0.030*SL	0.17 + 0.025*SL	0.18 + 0.025*SL
	t_{PHL}	0.44	0.29 + 0.076*SL	0.29 + 0.076*SL	0.29 + 0.076*SL
	t_R	0.40	0.31 + 0.042*SL	0.30 + 0.047*SL	0.24 + 0.054*SL
	t_F	0.77	0.46 + 0.159*SL	0.45 + 0.164*SL	0.43 + 0.165*SL
C to Y	t_{PLH}	0.21	0.15 + 0.031*SL	0.16 + 0.025*SL	0.17 + 0.025*SL
	t_{PHL}	0.44	0.29 + 0.074*SL	0.28 + 0.075*SL	0.28 + 0.076*SL
	t_R	0.38	0.29 + 0.041*SL	0.28 + 0.047*SL	0.21 + 0.054*SL
	t_F	0.78	0.46 + 0.160*SL	0.45 + 0.163*SL	0.43 + 0.165*SL
D to Y	t_{PLH}	0.20	0.14 + 0.032*SL	0.15 + 0.025*SL	0.16 + 0.025*SL
	t_{PHL}	0.43	0.28 + 0.073*SL	0.28 + 0.075*SL	0.27 + 0.076*SL
	t_R	0.35	0.27 + 0.041*SL	0.26 + 0.047*SL	0.19 + 0.054*SL
	t_F	0.78	0.46 + 0.159*SL	0.45 + 0.163*SL	0.43 + 0.165*SL
E to Y	t_{PLH}	0.19	0.12 + 0.034*SL	0.14 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.42	0.27 + 0.073*SL	0.27 + 0.075*SL	0.26 + 0.076*SL
	t_R	0.34	0.25 + 0.043*SL	0.24 + 0.047*SL	0.18 + 0.054*SL
	t_F	0.77	0.46 + 0.159*SL	0.45 + 0.163*SL	0.43 + 0.165*SL

STD80 ND5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.15 + 0.018*SL	0.16 + 0.014*SL	0.18 + 0.012*SL
	t_{PHL}	0.34	0.27 + 0.037*SL	0.26 + 0.038*SL	0.26 + 0.038*SL
	t_R	0.37	0.32 + 0.021*SL	0.32 + 0.022*SL	0.28 + 0.027*SL
	t_F	0.57	0.41 + 0.080*SL	0.40 + 0.081*SL	0.39 + 0.083*SL
B to Y	t_{PLH}	0.19	0.15 + 0.017*SL	0.16 + 0.014*SL	0.17 + 0.012*SL
	t_{PHL}	0.35	0.27 + 0.037*SL	0.27 + 0.038*SL	0.27 + 0.038*SL
	t_R	0.34	0.30 + 0.021*SL	0.30 + 0.022*SL	0.25 + 0.027*SL
	t_F	0.57	0.42 + 0.079*SL	0.41 + 0.081*SL	0.39 + 0.083*SL
C to Y	t_{PLH}	0.15	0.11 + 0.019*SL	0.12 + 0.015*SL	0.14 + 0.012*SL
	t_{PHL}	0.32	0.25 + 0.035*SL	0.25 + 0.037*SL	0.24 + 0.038*SL
	t_R	0.28	0.24 + 0.021*SL	0.24 + 0.022*SL	0.19 + 0.027*SL
	t_F	0.57	0.42 + 0.076*SL	0.41 + 0.080*SL	0.39 + 0.083*SL
D to Y	t_{PLH}	0.18	0.14 + 0.017*SL	0.15 + 0.014*SL	0.16 + 0.012*SL
	t_{PHL}	0.34	0.27 + 0.038*SL	0.27 + 0.037*SL	0.26 + 0.038*SL
	t_R	0.32	0.28 + 0.020*SL	0.28 + 0.022*SL	0.23 + 0.027*SL
	t_F	0.58	0.42 + 0.077*SL	0.41 + 0.081*SL	0.39 + 0.083*SL
E to Y	t_{PLH}	0.16	0.13 + 0.018*SL	0.13 + 0.014*SL	0.16 + 0.012*SL
	t_{PHL}	0.34	0.26 + 0.037*SL	0.26 + 0.037*SL	0.25 + 0.038*SL
	t_R	0.30	0.26 + 0.022*SL	0.26 + 0.022*SL	0.21 + 0.027*SL
	t_F	0.58	0.42 + 0.077*SL	0.42 + 0.080*SL	0.39 + 0.083*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 ND5

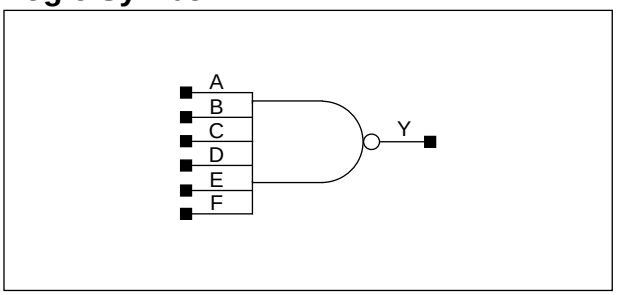
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.23 + 0.037*SL	0.23 + 0.036*SL	0.23 + 0.035*SL
	t_{PHL}	0.66	0.45 + 0.107*SL	0.45 + 0.107*SL	0.46 + 0.106*SL
	t_R	0.50	0.37 + 0.068*SL	0.36 + 0.071*SL	0.34 + 0.073*SL
	t_F	1.08	0.63 + 0.222*SL	0.63 + 0.223*SL	0.63 + 0.223*SL
B to Y	t_{PLH}	0.29	0.22 + 0.036*SL	0.22 + 0.036*SL	0.23 + 0.035*SL
	t_{PHL}	0.66	0.44 + 0.107*SL	0.44 + 0.107*SL	0.45 + 0.106*SL
	t_R	0.48	0.34 + 0.067*SL	0.33 + 0.071*SL	0.31 + 0.073*SL
	t_F	1.08	0.63 + 0.222*SL	0.63 + 0.223*SL	0.63 + 0.223*SL
C to Y	t_{PLH}	0.29	0.22 + 0.035*SL	0.22 + 0.035*SL	0.22 + 0.035*SL
	t_{PHL}	0.64	0.42 + 0.107*SL	0.42 + 0.107*SL	0.43 + 0.106*SL
	t_R	0.45	0.32 + 0.067*SL	0.30 + 0.071*SL	0.28 + 0.074*SL
	t_F	1.08	0.64 + 0.220*SL	0.63 + 0.223*SL	0.63 + 0.223*SL
D to Y	t_{PLH}	0.27	0.20 + 0.035*SL	0.20 + 0.035*SL	0.20 + 0.035*SL
	t_{PHL}	0.61	0.39 + 0.107*SL	0.40 + 0.106*SL	0.40 + 0.106*SL
	t_R	0.42	0.29 + 0.067*SL	0.28 + 0.071*SL	0.26 + 0.074*SL
	t_F	1.08	0.64 + 0.220*SL	0.63 + 0.223*SL	0.63 + 0.223*SL
E to Y	t_{PLH}	0.26	0.18 + 0.036*SL	0.19 + 0.035*SL	0.19 + 0.034*SL
	t_{PHL}	0.57	0.36 + 0.106*SL	0.36 + 0.106*SL	0.36 + 0.106*SL
	t_R	0.40	0.27 + 0.067*SL	0.25 + 0.071*SL	0.24 + 0.074*SL
	t_F	1.07	0.63 + 0.221*SL	0.62 + 0.224*SL	0.62 + 0.223*SL

STDM80 ND5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.22 + 0.018*SL	0.22 + 0.018*SL	0.22 + 0.018*SL
	t_{PHL}	0.52	0.41 + 0.054*SL	0.41 + 0.054*SL	0.41 + 0.054*SL
	t_R	0.41	0.35 + 0.033*SL	0.34 + 0.034*SL	0.33 + 0.035*SL
	t_F	0.79	0.57 + 0.110*SL	0.56 + 0.111*SL	0.56 + 0.111*SL
B to Y	t_{PLH}	0.25	0.21 + 0.018*SL	0.22 + 0.018*SL	0.22 + 0.018*SL
	t_{PHL}	0.52	0.41 + 0.054*SL	0.41 + 0.054*SL	0.41 + 0.054*SL
	t_R	0.39	0.32 + 0.033*SL	0.32 + 0.034*SL	0.31 + 0.035*SL
	t_F	0.79	0.57 + 0.109*SL	0.56 + 0.111*SL	0.56 + 0.111*SL
C to Y	t_{PLH}	0.21	0.17 + 0.020*SL	0.18 + 0.017*SL	0.18 + 0.017*SL
	t_{PHL}	0.43	0.32 + 0.053*SL	0.32 + 0.053*SL	0.33 + 0.053*SL
	t_R	0.31	0.25 + 0.033*SL	0.24 + 0.034*SL	0.23 + 0.036*SL
	t_F	0.78	0.56 + 0.109*SL	0.56 + 0.111*SL	0.55 + 0.112*SL
D to Y	t_{PLH}	0.24	0.20 + 0.018*SL	0.21 + 0.018*SL	0.21 + 0.017*SL
	t_{PHL}	0.49	0.38 + 0.054*SL	0.39 + 0.053*SL	0.39 + 0.054*SL
	t_R	0.36	0.30 + 0.032*SL	0.29 + 0.033*SL	0.28 + 0.035*SL
	t_F	0.79	0.57 + 0.109*SL	0.57 + 0.110*SL	0.56 + 0.111*SL
E to Y	t_{PLH}	0.23	0.19 + 0.019*SL	0.19 + 0.017*SL	0.19 + 0.017*SL
	t_{PHL}	0.46	0.36 + 0.054*SL	0.36 + 0.053*SL	0.36 + 0.053*SL
	t_R	0.34	0.27 + 0.031*SL	0.27 + 0.033*SL	0.25 + 0.035*SL
	t_F	0.79	0.57 + 0.109*SL	0.57 + 0.110*SL	0.56 + 0.111*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	x	x	x	x	x	1
x	0	x	x	x	x	1
x	x	0	x	x	x	1
x	x	x	0	x	x	1
x	x	x	x	0	x	1
x	x	x	x	x	0	1
1	1	1	1	1	1	0

Cell Data

Input Load (SL)												Gate Count	
STD80													
ND6						*ND6D2*						*ND6*	*ND6D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.6	0.4	0.5	0.6	0.6	0.6	0.6	0.4	0.6	0.6	0.6	0.6	4.0	4.3
STDM80													
ND6						*ND6D2*						*ND6*	*ND6D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.7	0.8	0.8	0.8	0.7	0.7	0.7	0.8	0.8	0.8	0.7	0.7	4.0	4.3

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 ND6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.39	0.34 + 0.026*SL	0.34 + 0.024*SL	0.34 + 0.024*SL
	t_{PHL}	0.56	0.47 + 0.043*SL	0.48 + 0.038*SL	0.49 + 0.037*SL
	t_R	0.18	0.09 + 0.047*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.25	0.13 + 0.062*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
B to Y	t_{PLH}	0.35	0.30 + 0.026*SL	0.30 + 0.024*SL	0.30 + 0.024*SL
	t_{PHL}	0.58	0.50 + 0.043*SL	0.51 + 0.038*SL	0.52 + 0.037*SL
	t_R	0.18	0.09 + 0.046*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
C to Y	t_{PLH}	0.37	0.32 + 0.026*SL	0.32 + 0.024*SL	0.32 + 0.024*SL
	t_{PHL}	0.57	0.49 + 0.042*SL	0.50 + 0.038*SL	0.51 + 0.037*SL
	t_R	0.18	0.09 + 0.045*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
D to Y	t_{PLH}	0.38	0.33 + 0.027*SL	0.33 + 0.024*SL	0.33 + 0.024*SL
	t_{PHL}	0.61	0.52 + 0.043*SL	0.53 + 0.038*SL	0.54 + 0.037*SL
	t_R	0.19	0.10 + 0.045*SL	0.09 + 0.050*SL	0.07 + 0.052*SL
	t_F	0.25	0.13 + 0.064*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
E to Y	t_{PLH}	0.40	0.35 + 0.026*SL	0.35 + 0.024*SL	0.35 + 0.024*SL
	t_{PHL}	0.60	0.51 + 0.043*SL	0.52 + 0.038*SL	0.53 + 0.037*SL
	t_R	0.19	0.10 + 0.047*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.25	0.12 + 0.064*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
F to Y	t_{PLH}	0.42	0.37 + 0.025*SL	0.37 + 0.024*SL	0.37 + 0.024*SL
	t_{PHL}	0.58	0.50 + 0.043*SL	0.51 + 0.038*SL	0.52 + 0.037*SL
	t_R	0.19	0.10 + 0.045*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 ND6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.40	0.37 + 0.016*SL	0.37 + 0.013*SL	0.38 + 0.012*SL
	t_{PHL}	0.59	0.54 + 0.024*SL	0.54 + 0.021*SL	0.57 + 0.018*SL
	t_R	0.14	0.10 + 0.019*SL	0.09 + 0.024*SL	0.07 + 0.026*SL
	t_F	0.21	0.15 + 0.032*SL	0.15 + 0.031*SL	0.12 + 0.034*SL
B to Y	t_{PLH}	0.36	0.33 + 0.016*SL	0.34 + 0.013*SL	0.34 + 0.012*SL
	t_{PHL}	0.61	0.56 + 0.025*SL	0.57 + 0.021*SL	0.59 + 0.018*SL
	t_R	0.14	0.10 + 0.023*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.21	0.15 + 0.029*SL	0.15 + 0.031*SL	0.12 + 0.034*SL
C to Y	t_{PLH}	0.38	0.35 + 0.016*SL	0.36 + 0.013*SL	0.36 + 0.012*SL
	t_{PHL}	0.60	0.55 + 0.025*SL	0.56 + 0.021*SL	0.58 + 0.018*SL
	t_R	0.14	0.10 + 0.022*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.21	0.14 + 0.033*SL	0.15 + 0.031*SL	0.12 + 0.034*SL
D to Y	t_{PLH}	0.39	0.36 + 0.017*SL	0.36 + 0.013*SL	0.38 + 0.012*SL
	t_{PHL}	0.63	0.58 + 0.025*SL	0.59 + 0.021*SL	0.62 + 0.018*SL
	t_R	0.15	0.11 + 0.018*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.21	0.15 + 0.033*SL	0.15 + 0.031*SL	0.12 + 0.034*SL
E to Y	t_{PLH}	0.41	0.38 + 0.017*SL	0.38 + 0.013*SL	0.39 + 0.012*SL
	t_{PHL}	0.62	0.57 + 0.025*SL	0.58 + 0.021*SL	0.61 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.21	0.15 + 0.031*SL	0.15 + 0.031*SL	0.12 + 0.034*SL
F to Y	t_{PLH}	0.43	0.39 + 0.017*SL	0.40 + 0.013*SL	0.41 + 0.012*SL
	t_{PHL}	0.61	0.56 + 0.026*SL	0.57 + 0.021*SL	0.60 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.21	0.15 + 0.031*SL	0.15 + 0.031*SL	0.12 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 ND6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.53	0.46 + 0.035*SL	0.46 + 0.034*SL	0.46 + 0.033*SL
	t_{PHL}	0.81	0.70 + 0.055*SL	0.72 + 0.048*SL	0.74 + 0.045*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.071*SL	0.10 + 0.072*SL
	t_F	0.33	0.17 + 0.082*SL	0.17 + 0.080*SL	0.17 + 0.081*SL
B to Y	t_{PLH}	0.49	0.42 + 0.035*SL	0.42 + 0.034*SL	0.42 + 0.033*SL
	t_{PHL}	0.81	0.70 + 0.055*SL	0.72 + 0.048*SL	0.74 + 0.045*SL
	t_R	0.25	0.12 + 0.067*SL	0.11 + 0.071*SL	0.10 + 0.072*SL
	t_F	0.33	0.17 + 0.082*SL	0.17 + 0.079*SL	0.17 + 0.081*SL
C to Y	t_{PLH}	0.51	0.44 + 0.035*SL	0.44 + 0.034*SL	0.45 + 0.033*SL
	t_{PHL}	0.81	0.70 + 0.055*SL	0.73 + 0.048*SL	0.75 + 0.045*SL
	t_R	0.25	0.12 + 0.069*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.33	0.17 + 0.082*SL	0.17 + 0.079*SL	0.17 + 0.081*SL
D to Y	t_{PLH}	0.53	0.45 + 0.036*SL	0.46 + 0.034*SL	0.46 + 0.033*SL
	t_{PHL}	0.85	0.74 + 0.055*SL	0.76 + 0.048*SL	0.79 + 0.045*SL
	t_R	0.26	0.12 + 0.068*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.33	0.17 + 0.081*SL	0.17 + 0.080*SL	0.17 + 0.081*SL
E to Y	t_{PLH}	0.55	0.48 + 0.036*SL	0.48 + 0.034*SL	0.49 + 0.033*SL
	t_{PHL}	0.86	0.75 + 0.055*SL	0.77 + 0.048*SL	0.79 + 0.045*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.34	0.18 + 0.081*SL	0.18 + 0.079*SL	0.17 + 0.080*SL
F to Y	t_{PLH}	0.57	0.49 + 0.036*SL	0.50 + 0.034*SL	0.50 + 0.033*SL
	t_{PHL}	0.86	0.75 + 0.055*SL	0.77 + 0.048*SL	0.79 + 0.045*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.33	0.17 + 0.083*SL	0.18 + 0.079*SL	0.17 + 0.081*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 ND6D2

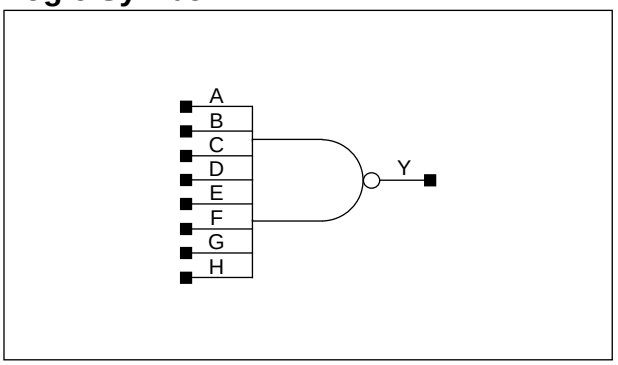
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.53	0.49 + 0.022*SL	0.50 + 0.018*SL	0.51 + 0.017*SL
	t_{PHL}	0.86	0.79 + 0.034*SL	0.81 + 0.028*SL	0.83 + 0.025*SL
	t_R	0.18	0.12 + 0.033*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.27	0.19 + 0.042*SL	0.19 + 0.040*SL	0.21 + 0.038*SL
B to Y	t_{PLH}	0.49	0.45 + 0.022*SL	0.46 + 0.018*SL	0.47 + 0.017*SL
	t_{PHL}	0.86	0.79 + 0.034*SL	0.81 + 0.028*SL	0.83 + 0.025*SL
	t_R	0.18	0.12 + 0.032*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.27	0.18 + 0.044*SL	0.20 + 0.039*SL	0.20 + 0.038*SL
C to Y	t_{PLH}	0.52	0.47 + 0.022*SL	0.48 + 0.018*SL	0.49 + 0.017*SL
	t_{PHL}	0.86	0.80 + 0.034*SL	0.81 + 0.028*SL	0.84 + 0.025*SL
	t_R	0.18	0.12 + 0.032*SL	0.11 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.27	0.19 + 0.042*SL	0.19 + 0.040*SL	0.20 + 0.038*SL
D to Y	t_{PLH}	0.53	0.49 + 0.022*SL	0.50 + 0.019*SL	0.51 + 0.017*SL
	t_{PHL}	0.91	0.84 + 0.034*SL	0.85 + 0.028*SL	0.88 + 0.025*SL
	t_R	0.19	0.12 + 0.032*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.27	0.19 + 0.042*SL	0.20 + 0.039*SL	0.20 + 0.038*SL
E to Y	t_{PLH}	0.55	0.51 + 0.022*SL	0.52 + 0.019*SL	0.53 + 0.017*SL
	t_{PHL}	0.91	0.84 + 0.034*SL	0.86 + 0.028*SL	0.88 + 0.025*SL
	t_R	0.19	0.12 + 0.032*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.27	0.18 + 0.043*SL	0.20 + 0.039*SL	0.20 + 0.038*SL
F to Y	t_{PLH}	0.57	0.53 + 0.022*SL	0.54 + 0.019*SL	0.55 + 0.017*SL
	t_{PHL}	0.91	0.84 + 0.034*SL	0.86 + 0.028*SL	0.88 + 0.025*SL
	t_R	0.19	0.13 + 0.032*SL	0.12 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.27	0.19 + 0.044*SL	0.20 + 0.039*SL	0.21 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

ND8/ND8D2

8-Input NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	x	x	x	x	x	x	x	1
x	0	x	x	x	x	x	x	1
x	x	0	x	x	x	x	x	1
x	x	x	0	x	x	x	x	1
x	x	x	x	0	x	x	x	1
x	x	x	x	x	0	x	x	1
x	x	x	x	x	x	0	x	1
x	x	x	x	x	x	x	0	1
1	1	1	1	1	1	1	1	0

Cell Data

Input Load (SL)																Gate Count	
STD80																	
ND8								*ND8D2*								*ND8*	*ND8D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
0.6	0.4	0.6	0.4	0.4	0.4	0.5	0.6	0.6	0.4	0.6	0.4	0.6	0.5	0.6	0.4	4.7	4.7
STDM80																	
ND8								*ND8D2*								*ND8*	*ND8D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
0.7	0.5	0.7	0.7	0.6	0.6	0.6	0.7	0.7	0.8	0.8	0.8	0.7	0.6	0.7	0.6	4.7	4.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 ND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.40	0.35 + 0.026*SL	0.35 + 0.024*SL	0.35 + 0.024*SL
	t_{PHL}	0.64	0.55 + 0.043*SL	0.56 + 0.038*SL	0.57 + 0.037*SL
	t_R	0.18	0.09 + 0.047*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.25	0.13 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
B to Y	t_{PLH}	0.37	0.32 + 0.025*SL	0.33 + 0.024*SL	0.33 + 0.024*SL
	t_{PHL}	0.65	0.56 + 0.042*SL	0.57 + 0.038*SL	0.58 + 0.037*SL
	t_R	0.18	0.09 + 0.046*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.25	0.13 + 0.064*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
C to Y	t_{PLH}	0.39	0.34 + 0.025*SL	0.34 + 0.024*SL	0.34 + 0.024*SL
	t_{PHL}	0.64	0.56 + 0.043*SL	0.57 + 0.038*SL	0.58 + 0.037*SL
	t_R	0.18	0.09 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.26	0.12 + 0.066*SL	0.13 + 0.066*SL	0.09 + 0.069*SL
D to Y	t_{PLH}	0.35	0.30 + 0.026*SL	0.30 + 0.024*SL	0.31 + 0.024*SL
	t_{PHL}	0.64	0.56 + 0.043*SL	0.57 + 0.038*SL	0.58 + 0.037*SL
	t_R	0.18	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.25	0.13 + 0.063*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
E to Y	t_{PLH}	0.38	0.33 + 0.026*SL	0.34 + 0.024*SL	0.34 + 0.024*SL
	t_{PHL}	0.67	0.58 + 0.043*SL	0.59 + 0.038*SL	0.60 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.050*SL	0.07 + 0.052*SL
	t_F	0.26	0.13 + 0.064*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
F to Y	t_{PLH}	0.40	0.35 + 0.026*SL	0.36 + 0.024*SL	0.36 + 0.024*SL
	t_{PHL}	0.67	0.58 + 0.043*SL	0.59 + 0.038*SL	0.61 + 0.037*SL
	t_R	0.19	0.10 + 0.045*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
G to Y	t_{PLH}	0.42	0.37 + 0.027*SL	0.37 + 0.024*SL	0.37 + 0.024*SL
	t_{PHL}	0.67	0.58 + 0.043*SL	0.59 + 0.038*SL	0.60 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.26	0.13 + 0.064*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
H to Y	t_{PLH}	0.43	0.38 + 0.027*SL	0.38 + 0.024*SL	0.38 + 0.024*SL
	t_{PHL}	0.66	0.57 + 0.043*SL	0.58 + 0.038*SL	0.60 + 0.037*SL
	t_R	0.19	0.10 + 0.046*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.26	0.13 + 0.062*SL	0.12 + 0.066*SL	0.09 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 ND8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.41	0.38 + 0.016*SL	0.39 + 0.013*SL	0.39 + 0.012*SL
	t_{PHL}	0.67	0.62 + 0.025*SL	0.63 + 0.021*SL	0.65 + 0.018*SL
	t_R	0.14	0.10 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.21	0.15 + 0.032*SL	0.15 + 0.031*SL	0.12 + 0.034*SL
B to Y	t_{PLH}	0.38	0.35 + 0.016*SL	0.36 + 0.013*SL	0.37 + 0.012*SL
	t_{PHL}	0.68	0.63 + 0.025*SL	0.64 + 0.021*SL	0.66 + 0.018*SL
	t_R	0.14	0.10 + 0.023*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.21	0.15 + 0.031*SL	0.15 + 0.031*SL	0.13 + 0.034*SL
C to Y	t_{PLH}	0.40	0.37 + 0.016*SL	0.37 + 0.013*SL	0.38 + 0.012*SL
	t_{PHL}	0.67	0.62 + 0.025*SL	0.63 + 0.021*SL	0.66 + 0.018*SL
	t_R	0.14	0.10 + 0.020*SL	0.09 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.21	0.15 + 0.031*SL	0.15 + 0.031*SL	0.13 + 0.034*SL
D to Y	t_{PLH}	0.36	0.33 + 0.016*SL	0.34 + 0.013*SL	0.35 + 0.012*SL
	t_{PHL}	0.68	0.63 + 0.025*SL	0.64 + 0.021*SL	0.66 + 0.018*SL
	t_R	0.14	0.10 + 0.019*SL	0.09 + 0.024*SL	0.07 + 0.026*SL
	t_F	0.21	0.15 + 0.032*SL	0.15 + 0.031*SL	0.13 + 0.034*SL
E to Y	t_{PLH}	0.44	0.41 + 0.017*SL	0.42 + 0.013*SL	0.43 + 0.012*SL
	t_{PHL}	0.69	0.64 + 0.025*SL	0.65 + 0.021*SL	0.68 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.22	0.16 + 0.030*SL	0.15 + 0.031*SL	0.13 + 0.034*SL
F to Y	t_{PLH}	0.42	0.38 + 0.017*SL	0.39 + 0.013*SL	0.40 + 0.012*SL
	t_{PHL}	0.70	0.65 + 0.025*SL	0.66 + 0.021*SL	0.69 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.22	0.15 + 0.031*SL	0.15 + 0.031*SL	0.13 + 0.034*SL
G to Y	t_{PLH}	0.43	0.40 + 0.017*SL	0.41 + 0.013*SL	0.42 + 0.012*SL
	t_{PHL}	0.70	0.65 + 0.026*SL	0.66 + 0.021*SL	0.69 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.22	0.16 + 0.030*SL	0.15 + 0.031*SL	0.13 + 0.034*SL
H to Y	t_{PLH}	0.40	0.36 + 0.017*SL	0.37 + 0.013*SL	0.38 + 0.012*SL
	t_{PHL}	0.70	0.65 + 0.026*SL	0.66 + 0.021*SL	0.69 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.22	0.15 + 0.031*SL	0.15 + 0.031*SL	0.13 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 ND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.55	0.48 + 0.035*SL	0.48 + 0.034*SL	0.49 + 0.033*SL
	t_{PHL}	0.94	0.83 + 0.055*SL	0.85 + 0.048*SL	0.87 + 0.045*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.071*SL	0.10 + 0.072*SL
	t_F	0.33	0.17 + 0.082*SL	0.18 + 0.079*SL	0.17 + 0.080*SL
B to Y	t_{PLH}	0.52	0.45 + 0.035*SL	0.45 + 0.034*SL	0.45 + 0.033*SL
	t_{PHL}	0.92	0.81 + 0.056*SL	0.83 + 0.048*SL	0.85 + 0.045*SL
	t_R	0.25	0.12 + 0.067*SL	0.11 + 0.071*SL	0.10 + 0.072*SL
	t_F	0.33	0.17 + 0.082*SL	0.18 + 0.079*SL	0.17 + 0.080*SL
C to Y	t_{PLH}	0.54	0.47 + 0.035*SL	0.47 + 0.034*SL	0.47 + 0.033*SL
	t_{PHL}	0.93	0.82 + 0.056*SL	0.85 + 0.048*SL	0.87 + 0.045*SL
	t_R	0.25	0.12 + 0.068*SL	0.11 + 0.071*SL	0.10 + 0.072*SL
	t_F	0.33	0.17 + 0.082*SL	0.18 + 0.079*SL	0.17 + 0.080*SL
D to Y	t_{PLH}	0.50	0.43 + 0.035*SL	0.43 + 0.034*SL	0.43 + 0.033*SL
	t_{PHL}	0.90	0.79 + 0.055*SL	0.81 + 0.048*SL	0.83 + 0.045*SL
	t_R	0.25	0.12 + 0.068*SL	0.11 + 0.071*SL	0.10 + 0.072*SL
	t_F	0.33	0.17 + 0.082*SL	0.18 + 0.079*SL	0.17 + 0.080*SL
E to Y	t_{PLH}	0.54	0.46 + 0.036*SL	0.47 + 0.034*SL	0.47 + 0.033*SL
	t_{PHL}	0.94	0.83 + 0.055*SL	0.85 + 0.048*SL	0.87 + 0.045*SL
	t_R	0.26	0.13 + 0.066*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.34	0.17 + 0.081*SL	0.18 + 0.079*SL	0.17 + 0.080*SL
F to Y	t_{PLH}	0.56	0.49 + 0.036*SL	0.49 + 0.034*SL	0.50 + 0.033*SL
	t_{PHL}	0.96	0.85 + 0.056*SL	0.87 + 0.048*SL	0.90 + 0.045*SL
	t_R	0.26	0.13 + 0.066*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.34	0.17 + 0.081*SL	0.18 + 0.079*SL	0.17 + 0.080*SL
G to Y	t_{PLH}	0.58	0.51 + 0.036*SL	0.51 + 0.034*SL	0.51 + 0.033*SL
	t_{PHL}	0.98	0.87 + 0.056*SL	0.89 + 0.048*SL	0.91 + 0.045*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.34	0.18 + 0.080*SL	0.18 + 0.079*SL	0.18 + 0.080*SL
H to Y	t_{PLH}	0.59	0.52 + 0.036*SL	0.53 + 0.034*SL	0.53 + 0.033*SL
	t_{PHL}	0.98	0.87 + 0.056*SL	0.89 + 0.048*SL	0.91 + 0.045*SL
	t_R	0.26	0.13 + 0.066*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.34	0.17 + 0.082*SL	0.18 + 0.079*SL	0.17 + 0.080*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

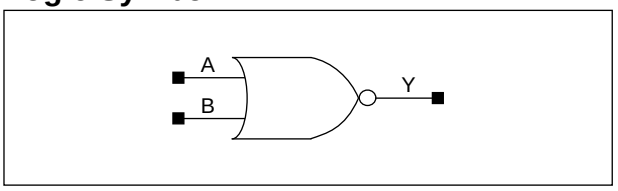
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 ND8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.56	0.51 + 0.022*SL	0.52 + 0.019*SL	0.54 + 0.017*SL
	t_{PHL}	0.99	0.92 + 0.034*SL	0.94 + 0.028*SL	0.97 + 0.025*SL
	t_R	0.18	0.12 + 0.033*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.28	0.19 + 0.043*SL	0.20 + 0.039*SL	0.21 + 0.038*SL
B to Y	t_{PLH}	0.52	0.48 + 0.022*SL	0.49 + 0.018*SL	0.50 + 0.017*SL
	t_{PHL}	0.97	0.91 + 0.034*SL	0.92 + 0.028*SL	0.95 + 0.025*SL
	t_R	0.18	0.12 + 0.032*SL	0.11 + 0.034*SL	0.11 + 0.034*SL
	t_F	0.28	0.19 + 0.042*SL	0.20 + 0.039*SL	0.21 + 0.038*SL
C to Y	t_{PLH}	0.55	0.50 + 0.021*SL	0.51 + 0.018*SL	0.52 + 0.017*SL
	t_{PHL}	0.99	0.92 + 0.034*SL	0.94 + 0.029*SL	0.96 + 0.025*SL
	t_R	0.18	0.12 + 0.033*SL	0.12 + 0.033*SL	0.11 + 0.035*SL
	t_F	0.28	0.19 + 0.043*SL	0.20 + 0.039*SL	0.21 + 0.038*SL
D to Y	t_{PLH}	0.50	0.46 + 0.021*SL	0.47 + 0.018*SL	0.48 + 0.017*SL
	t_{PHL}	0.95	0.89 + 0.034*SL	0.90 + 0.028*SL	0.93 + 0.025*SL
	t_R	0.18	0.12 + 0.033*SL	0.11 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.28	0.19 + 0.043*SL	0.20 + 0.039*SL	0.21 + 0.038*SL
E to Y	t_{PLH}	0.60	0.56 + 0.022*SL	0.57 + 0.019*SL	0.58 + 0.017*SL
	t_{PHL}	1.05	0.98 + 0.034*SL	0.99 + 0.028*SL	1.02 + 0.025*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.28	0.20 + 0.042*SL	0.20 + 0.039*SL	0.21 + 0.038*SL
F to Y	t_{PLH}	0.57	0.52 + 0.022*SL	0.53 + 0.019*SL	0.55 + 0.017*SL
	t_{PHL}	1.03	0.96 + 0.034*SL	0.98 + 0.028*SL	1.00 + 0.025*SL
	t_R	0.19	0.13 + 0.033*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.28	0.20 + 0.042*SL	0.21 + 0.039*SL	0.21 + 0.038*SL
G to Y	t_{PLH}	0.59	0.54 + 0.022*SL	0.55 + 0.019*SL	0.57 + 0.017*SL
	t_{PHL}	1.04	0.97 + 0.034*SL	0.99 + 0.029*SL	1.02 + 0.025*SL
	t_R	0.19	0.12 + 0.033*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.28	0.19 + 0.043*SL	0.21 + 0.039*SL	0.21 + 0.038*SL
H to Y	t_{PLH}	0.55	0.50 + 0.022*SL	0.51 + 0.018*SL	0.52 + 0.017*SL
	t_{PHL}	1.00	0.94 + 0.034*SL	0.95 + 0.029*SL	0.98 + 0.025*SL
	t_R	0.19	0.12 + 0.033*SL	0.13 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.28	0.20 + 0.042*SL	0.21 + 0.039*SL	0.21 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Cell Data

Input Load (SL)				Gate Count	
STD80					
NR2		*NR2D2*		*NR2*	*NR2D2*
A	B	A	B		
0.9	0.6	1.3	1.3	1.0	1.7
STDM80					
NR2		*NR2D2*		*NR2*	*NR2D2*
A	B	A	B		
1.1	1.1	2.2	2.2	1.0	1.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NR2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.11 + 0.042*SL	0.12 + 0.037*SL	0.12 + 0.038*SL
	t_{PHL}	0.24	0.17 + 0.039*SL	0.17 + 0.036*SL	0.16 + 0.037*SL
	t_R	0.36	0.22 + 0.070*SL	0.20 + 0.080*SL	0.14 + 0.086*SL
	t_F	0.34	0.25 + 0.050*SL	0.22 + 0.062*SL	0.15 + 0.069*SL
B to Y	t_{PLH}	0.20	0.11 + 0.045*SL	0.13 + 0.037*SL	0.13 + 0.038*SL
	t_{PHL}	0.21	0.12 + 0.044*SL	0.13 + 0.037*SL	0.13 + 0.037*SL
	t_R	0.37	0.24 + 0.069*SL	0.21 + 0.079*SL	0.14 + 0.086*SL
	t_F	0.28	0.17 + 0.054*SL	0.15 + 0.062*SL	0.09 + 0.069*SL

STD80 NR2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.15	0.10 + 0.025*SL	0.11 + 0.020*SL	0.12 + 0.019*SL
	t_{PHL}	0.16	0.12 + 0.024*SL	0.13 + 0.019*SL	0.14 + 0.018*SL
	t_R	0.28	0.21 + 0.035*SL	0.21 + 0.037*SL	0.15 + 0.043*SL
	t_F	0.24	0.19 + 0.029*SL	0.19 + 0.028*SL	0.13 + 0.034*SL
B to Y	t_{PLH}	0.15	0.10 + 0.025*SL	0.11 + 0.020*SL	0.12 + 0.019*SL
	t_{PHL}	0.16	0.12 + 0.024*SL	0.13 + 0.019*SL	0.14 + 0.018*SL
	t_R	0.28	0.21 + 0.035*SL	0.21 + 0.037*SL	0.15 + 0.043*SL
	t_F	0.24	0.19 + 0.029*SL	0.19 + 0.028*SL	0.13 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NR2

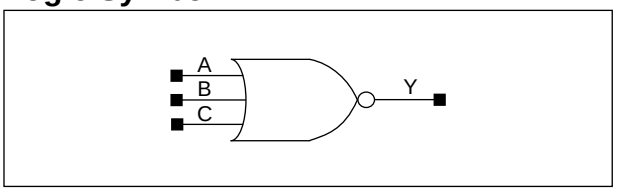
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.17 + 0.059*SL	0.18 + 0.057*SL	0.18 + 0.057*SL
	t_{PHL}	0.29	0.20 + 0.045*SL	0.20 + 0.045*SL	0.20 + 0.044*SL
	t_R	0.47	0.23 + 0.117*SL	0.22 + 0.122*SL	0.20 + 0.125*SL
	t_F	0.36	0.21 + 0.075*SL	0.20 + 0.079*SL	0.18 + 0.082*SL
B to Y	t_{PLH}	0.27	0.15 + 0.059*SL	0.16 + 0.057*SL	0.16 + 0.057*SL
	t_{PHL}	0.24	0.15 + 0.047*SL	0.16 + 0.045*SL	0.16 + 0.044*SL
	t_R	0.47	0.24 + 0.115*SL	0.22 + 0.121*SL	0.20 + 0.125*SL
	t_F	0.29	0.15 + 0.074*SL	0.13 + 0.079*SL	0.11 + 0.082*SL

STDM80 NR2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.14 + 0.033*SL	0.15 + 0.029*SL	0.15 + 0.028*SL
	t_{PHL}	0.19	0.14 + 0.027*SL	0.15 + 0.022*SL	0.16 + 0.021*SL
	t_R	0.32	0.21 + 0.054*SL	0.20 + 0.059*SL	0.19 + 0.060*SL
	t_F	0.23	0.17 + 0.033*SL	0.16 + 0.036*SL	0.14 + 0.038*SL
B to Y	t_{PLH}	0.20	0.14 + 0.033*SL	0.15 + 0.029*SL	0.15 + 0.028*SL
	t_{PHL}	0.19	0.14 + 0.027*SL	0.15 + 0.022*SL	0.16 + 0.021*SL
	t_R	0.32	0.21 + 0.054*SL	0.20 + 0.059*SL	0.19 + 0.060*SL
	t_F	0.23	0.17 + 0.033*SL	0.16 + 0.036*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	1
1	x	x	0
x	1	x	0
x	x	1	0

Cell Data

Input Load (SL)						Gate Count	
STD80							
NR3			*NR3D2*			*NR3*	*NR3D2*
A	B	C	A	B	C		
0.9	0.7	0.5	1.6	0.9	1.6	1.3	2.3
STDM80							
NR3			*NR3D2*			*NR3*	*NR3D2*
A	B	C	A	B	C		
1.1	1.1	1.1	2.3	2.2	2.2	1.3	2.3

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NR3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.17 + 0.056*SL	0.18 + 0.054*SL	0.17 + 0.054*SL
	t_{PHL}	0.27	0.19 + 0.040*SL	0.20 + 0.038*SL	0.20 + 0.037*SL
	t_R	0.52	0.29 + 0.113*SL	0.27 + 0.122*SL	0.23 + 0.125*SL
	t_F	0.41	0.29 + 0.059*SL	0.28 + 0.063*SL	0.22 + 0.069*SL
B to Y	t_{PLH}	0.28	0.17 + 0.057*SL	0.18 + 0.053*SL	0.17 + 0.054*SL
	t_{PHL}	0.25	0.17 + 0.040*SL	0.18 + 0.037*SL	0.18 + 0.037*SL
	t_R	0.53	0.31 + 0.111*SL	0.29 + 0.120*SL	0.24 + 0.125*SL
	t_F	0.35	0.25 + 0.050*SL	0.22 + 0.063*SL	0.16 + 0.069*SL
C to Y	t_{PLH}	0.26	0.15 + 0.056*SL	0.16 + 0.053*SL	0.14 + 0.054*SL
	t_{PHL}	0.21	0.12 + 0.044*SL	0.14 + 0.037*SL	0.14 + 0.037*SL
	t_R	0.53	0.31 + 0.110*SL	0.29 + 0.120*SL	0.23 + 0.125*SL
	t_F	0.28	0.17 + 0.057*SL	0.16 + 0.063*SL	0.10 + 0.069*SL

STD80 NR3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.16 + 0.029*SL	0.16 + 0.027*SL	0.16 + 0.027*SL
	t_{PHL}	0.20	0.16 + 0.023*SL	0.17 + 0.019*SL	0.17 + 0.018*SL
	t_R	0.38	0.27 + 0.051*SL	0.26 + 0.058*SL	0.22 + 0.063*SL
	t_F	0.31	0.26 + 0.025*SL	0.25 + 0.029*SL	0.20 + 0.034*SL
B to Y	t_{PLH}	0.19	0.13 + 0.031*SL	0.14 + 0.027*SL	0.14 + 0.027*SL
	t_{PHL}	0.15	0.09 + 0.027*SL	0.11 + 0.020*SL	0.13 + 0.018*SL
	t_R	0.39	0.28 + 0.053*SL	0.27 + 0.057*SL	0.22 + 0.063*SL
	t_F	0.21	0.16 + 0.029*SL	0.16 + 0.028*SL	0.11 + 0.034*SL
C to Y	t_{PLH}	0.21	0.16 + 0.029*SL	0.16 + 0.027*SL	0.16 + 0.027*SL
	t_{PHL}	0.20	0.16 + 0.023*SL	0.17 + 0.019*SL	0.17 + 0.018*SL
	t_R	0.38	0.28 + 0.050*SL	0.26 + 0.058*SL	0.22 + 0.063*SL
	t_F	0.31	0.25 + 0.026*SL	0.25 + 0.029*SL	0.20 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NR3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.45	0.28 + 0.086*SL	0.28 + 0.085*SL	0.29 + 0.085*SL
	t_{PHL}	0.32	0.23 + 0.048*SL	0.23 + 0.046*SL	0.24 + 0.045*SL
	t_R	0.74	0.38 + 0.180*SL	0.37 + 0.185*SL	0.35 + 0.186*SL
	t_F	0.44	0.29 + 0.077*SL	0.28 + 0.080*SL	0.26 + 0.082*SL
B to Y	t_{PLH}	0.42	0.25 + 0.086*SL	0.25 + 0.085*SL	0.25 + 0.085*SL
	t_{PHL}	0.30	0.21 + 0.045*SL	0.21 + 0.045*SL	0.22 + 0.044*SL
	t_R	0.75	0.39 + 0.178*SL	0.38 + 0.183*SL	0.36 + 0.186*SL
	t_F	0.37	0.22 + 0.076*SL	0.21 + 0.080*SL	0.19 + 0.082*SL
C to Y	t_{PLH}	0.35	0.19 + 0.083*SL	0.18 + 0.084*SL	0.18 + 0.084*SL
	t_{PHL}	0.25	0.16 + 0.046*SL	0.17 + 0.044*SL	0.17 + 0.044*SL
	t_R	0.74	0.38 + 0.179*SL	0.36 + 0.184*SL	0.34 + 0.187*SL
	t_F	0.31	0.15 + 0.076*SL	0.14 + 0.079*SL	0.12 + 0.082*SL

STDM80 NR3D2

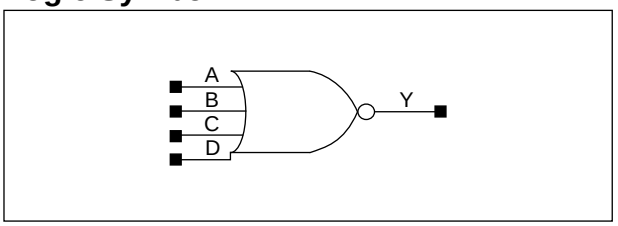
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.33	0.24 + 0.044*SL	0.24 + 0.043*SL	0.24 + 0.043*SL
	t_{PHL}	0.24	0.19 + 0.024*SL	0.20 + 0.023*SL	0.20 + 0.022*SL
	t_R	0.51	0.33 + 0.087*SL	0.32 + 0.090*SL	0.31 + 0.092*SL
	t_F	0.30	0.23 + 0.036*SL	0.23 + 0.037*SL	0.22 + 0.039*SL
B to Y	t_{PLH}	0.24	0.16 + 0.042*SL	0.16 + 0.042*SL	0.16 + 0.042*SL
	t_{PHL}	0.18	0.12 + 0.028*SL	0.14 + 0.022*SL	0.15 + 0.021*SL
	t_R	0.50	0.32 + 0.087*SL	0.32 + 0.090*SL	0.30 + 0.092*SL
	t_F	0.21	0.14 + 0.033*SL	0.13 + 0.037*SL	0.12 + 0.038*SL
C to Y	t_{PLH}	0.32	0.24 + 0.044*SL	0.24 + 0.043*SL	0.24 + 0.043*SL
	t_{PHL}	0.24	0.19 + 0.024*SL	0.19 + 0.023*SL	0.20 + 0.022*SL
	t_R	0.51	0.34 + 0.086*SL	0.32 + 0.090*SL	0.31 + 0.092*SL
	t_F	0.30	0.23 + 0.035*SL	0.22 + 0.038*SL	0.22 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

NR4/NR4D2

4-Input NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	0	1
1	x	x	x	0
x	1	x	x	0
x	x	1	x	0
x	x	x	1	0

Cell Data

Input Load (SL)								Gate Count	
STD80									
NR4				*NR4D2*				*NR4*	*NR4D2*
A	B	C	D	A	B	C	D		
0.6	0.8	0.9	0.9	1.6	1.3	1.3	1.6	1.7	2.3
STDM80									
NR4				*NR4D2*				*NR4*	*NR4D2*
A	B	C	D	A	B	C	D		
1.1	1.1	1.1	1.0	2.2	2.1	2.2	2.1	1.7	2.3

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NR4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.17 + 0.067*SL	0.17 + 0.069*SL	0.15 + 0.071*SL
	t_{PHL}	0.21	0.13 + 0.044*SL	0.14 + 0.037*SL	0.14 + 0.037*SL
	t_R	0.71	0.40 + 0.153*SL	0.39 + 0.161*SL	0.34 + 0.165*SL
	t_F	0.29	0.17 + 0.055*SL	0.16 + 0.063*SL	0.10 + 0.069*SL
B to Y	t_{PLH}	0.35	0.21 + 0.070*SL	0.21 + 0.070*SL	0.20 + 0.071*SL
	t_{PHL}	0.25	0.17 + 0.040*SL	0.18 + 0.037*SL	0.18 + 0.037*SL
	t_R	0.73	0.42 + 0.152*SL	0.40 + 0.161*SL	0.36 + 0.165*SL
	t_F	0.35	0.23 + 0.056*SL	0.22 + 0.063*SL	0.16 + 0.069*SL
C to Y	t_{PLH}	0.38	0.24 + 0.072*SL	0.24 + 0.071*SL	0.24 + 0.071*SL
	t_{PHL}	0.28	0.20 + 0.040*SL	0.20 + 0.038*SL	0.21 + 0.037*SL
	t_R	0.72	0.41 + 0.154*SL	0.40 + 0.161*SL	0.36 + 0.165*SL
	t_F	0.41	0.29 + 0.060*SL	0.28 + 0.063*SL	0.22 + 0.069*SL
D to Y	t_{PLH}	0.39	0.25 + 0.072*SL	0.25 + 0.071*SL	0.25 + 0.071*SL
	t_{PHL}	0.29	0.21 + 0.040*SL	0.21 + 0.039*SL	0.23 + 0.037*SL
	t_R	0.71	0.40 + 0.155*SL	0.38 + 0.162*SL	0.36 + 0.165*SL
	t_F	0.46	0.33 + 0.062*SL	0.33 + 0.065*SL	0.29 + 0.069*SL

STD80 NR4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.21 + 0.037*SL	0.22 + 0.035*SL	0.21 + 0.035*SL
	t_{PHL}	0.21	0.17 + 0.023*SL	0.17 + 0.019*SL	0.19 + 0.018*SL
	t_R	0.52	0.38 + 0.073*SL	0.37 + 0.079*SL	0.33 + 0.082*SL
	t_F	0.33	0.27 + 0.027*SL	0.27 + 0.030*SL	0.23 + 0.034*SL
B to Y	t_{PLH}	0.26	0.19 + 0.037*SL	0.19 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.19	0.14 + 0.024*SL	0.15 + 0.020*SL	0.16 + 0.018*SL
	t_R	0.52	0.37 + 0.073*SL	0.36 + 0.079*SL	0.32 + 0.082*SL
	t_F	0.27	0.22 + 0.029*SL	0.22 + 0.029*SL	0.17 + 0.034*SL
C to Y	t_{PLH}	0.26	0.19 + 0.037*SL	0.19 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.19	0.14 + 0.024*SL	0.15 + 0.020*SL	0.16 + 0.018*SL
	t_R	0.52	0.37 + 0.074*SL	0.36 + 0.079*SL	0.32 + 0.082*SL
	t_F	0.28	0.22 + 0.029*SL	0.22 + 0.029*SL	0.18 + 0.034*SL
D to Y	t_{PLH}	0.29	0.21 + 0.037*SL	0.22 + 0.035*SL	0.21 + 0.035*SL
	t_{PHL}	0.21	0.17 + 0.023*SL	0.17 + 0.019*SL	0.19 + 0.018*SL
	t_R	0.52	0.38 + 0.074*SL	0.37 + 0.079*SL	0.33 + 0.082*SL
	t_F	0.33	0.27 + 0.028*SL	0.27 + 0.030*SL	0.23 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NR4

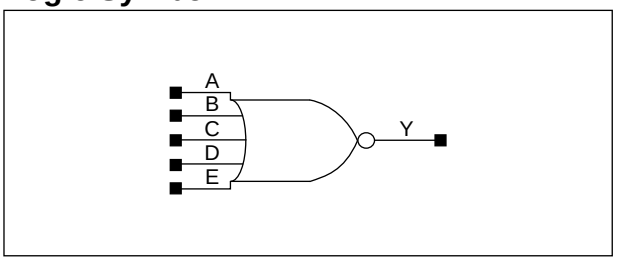
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.41	0.20 + 0.109*SL	0.19 + 0.112*SL	0.19 + 0.112*SL
	t_{PHL}	0.26	0.17 + 0.046*SL	0.17 + 0.044*SL	0.17 + 0.044*SL
	t_R	1.02	0.53 + 0.243*SL	0.52 + 0.248*SL	0.50 + 0.250*SL
	t_F	0.31	0.16 + 0.075*SL	0.15 + 0.079*SL	0.12 + 0.082*SL
B to Y	t_{PLH}	0.53	0.30 + 0.114*SL	0.30 + 0.113*SL	0.30 + 0.112*SL
	t_{PHL}	0.31	0.21 + 0.046*SL	0.22 + 0.045*SL	0.22 + 0.044*SL
	t_R	1.06	0.58 + 0.239*SL	0.56 + 0.245*SL	0.55 + 0.247*SL
	t_F	0.37	0.22 + 0.076*SL	0.21 + 0.080*SL	0.19 + 0.082*SL
C to Y	t_{PLH}	0.61	0.38 + 0.114*SL	0.38 + 0.113*SL	0.39 + 0.112*SL
	t_{PHL}	0.33	0.24 + 0.048*SL	0.24 + 0.047*SL	0.25 + 0.045*SL
	t_R	1.06	0.58 + 0.240*SL	0.56 + 0.245*SL	0.55 + 0.247*SL
	t_F	0.44	0.28 + 0.079*SL	0.28 + 0.080*SL	0.26 + 0.083*SL
D to Y	t_{PLH}	0.64	0.41 + 0.114*SL	0.42 + 0.113*SL	0.42 + 0.112*SL
	t_{PHL}	0.34	0.24 + 0.051*SL	0.25 + 0.048*SL	0.26 + 0.047*SL
	t_R	1.05	0.57 + 0.241*SL	0.56 + 0.245*SL	0.55 + 0.247*SL
	t_F	0.50	0.33 + 0.082*SL	0.33 + 0.082*SL	0.33 + 0.083*SL

STDM80 NR4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.44	0.32 + 0.058*SL	0.33 + 0.057*SL	0.33 + 0.057*SL
	t_{PHL}	0.25	0.20 + 0.024*SL	0.20 + 0.023*SL	0.21 + 0.023*SL
	t_R	0.76	0.53 + 0.113*SL	0.51 + 0.119*SL	0.49 + 0.122*SL
	t_F	0.33	0.25 + 0.038*SL	0.25 + 0.038*SL	0.25 + 0.039*SL
B to Y	t_{PLH}	0.37	0.25 + 0.057*SL	0.26 + 0.056*SL	0.26 + 0.056*SL
	t_{PHL}	0.22	0.17 + 0.025*SL	0.18 + 0.023*SL	0.18 + 0.022*SL
	t_R	0.75	0.52 + 0.115*SL	0.50 + 0.120*SL	0.49 + 0.123*SL
	t_F	0.27	0.20 + 0.038*SL	0.20 + 0.038*SL	0.19 + 0.039*SL
C to Y	t_{PLH}	0.37	0.26 + 0.057*SL	0.26 + 0.056*SL	0.26 + 0.056*SL
	t_{PHL}	0.22	0.17 + 0.025*SL	0.18 + 0.023*SL	0.18 + 0.022*SL
	t_R	0.75	0.52 + 0.116*SL	0.51 + 0.120*SL	0.49 + 0.123*SL
	t_F	0.28	0.20 + 0.037*SL	0.20 + 0.038*SL	0.19 + 0.039*SL
D to Y	t_{PLH}	0.44	0.33 + 0.059*SL	0.33 + 0.057*SL	0.33 + 0.057*SL
	t_{PHL}	0.25	0.20 + 0.024*SL	0.20 + 0.023*SL	0.21 + 0.023*SL
	t_R	0.76	0.53 + 0.113*SL	0.52 + 0.119*SL	0.50 + 0.122*SL
	t_F	0.33	0.25 + 0.038*SL	0.25 + 0.039*SL	0.25 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	1
1	x	x	x	x	0
x	1	x	x	x	0
x	x	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0

Cell Data

Input Load (SL)										Gate Count	
STD80											
NR5					*NR5D2*					*NR5*	*NR5D2*
A	B	C	D	E	A	B	C	D	E		
0.6	0.4	0.5	0.4	0.4	0.6	0.4	0.5	0.4	0.4	3.7	3.7
STDM80											
NR5					*NR5D2*					*NR5*	*NR5D2*
A	B	C	D	E	A	B	C	D	E		
0.7	0.8	0.8	0.8	0.7	0.7	0.8	0.8	0.8	0.7	3.7	3.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NR5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.56	0.50 + 0.029*SL	0.51 + 0.025*SL	0.52 + 0.024*SL
	t_{PHL}	0.42	0.34 + 0.039*SL	0.35 + 0.037*SL	0.35 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.068*SL	0.07 + 0.069*SL
B to Y	t_{PLH}	0.54	0.48 + 0.029*SL	0.49 + 0.025*SL	0.50 + 0.024*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.037*SL	0.30 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.068*SL	0.07 + 0.069*SL
C to Y	t_{PLH}	0.56	0.50 + 0.029*SL	0.51 + 0.025*SL	0.52 + 0.024*SL
	t_{PHL}	0.40	0.33 + 0.039*SL	0.33 + 0.037*SL	0.33 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.22	0.08 + 0.066*SL	0.08 + 0.068*SL	0.07 + 0.069*SL
D to Y	t_{PLH}	0.47	0.41 + 0.029*SL	0.42 + 0.025*SL	0.43 + 0.024*SL
	t_{PHL}	0.39	0.31 + 0.039*SL	0.31 + 0.037*SL	0.31 + 0.037*SL
	t_R	0.20	0.11 + 0.048*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.068*SL	0.07 + 0.069*SL
E to Y	t_{PLH}	0.46	0.40 + 0.029*SL	0.41 + 0.025*SL	0.42 + 0.024*SL
	t_{PHL}	0.42	0.34 + 0.039*SL	0.34 + 0.037*SL	0.34 + 0.037*SL
	t_R	0.20	0.11 + 0.048*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.09 + 0.067*SL	0.07 + 0.069*SL

STD80 NR5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.58	0.55 + 0.019*SL	0.56 + 0.014*SL	0.58 + 0.012*SL
	t_{PHL}	0.42	0.37 + 0.022*SL	0.38 + 0.019*SL	0.39 + 0.018*SL
	t_R	0.18	0.14 + 0.021*SL	0.13 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
B to Y	t_{PLH}	0.57	0.53 + 0.019*SL	0.54 + 0.014*SL	0.56 + 0.012*SL
	t_{PHL}	0.37	0.32 + 0.022*SL	0.33 + 0.019*SL	0.34 + 0.018*SL
	t_R	0.18	0.14 + 0.022*SL	0.13 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.15	0.09 + 0.032*SL	0.09 + 0.032*SL	0.07 + 0.034*SL
C to Y	t_{PLH}	0.59	0.55 + 0.019*SL	0.56 + 0.014*SL	0.58 + 0.012*SL
	t_{PHL}	0.40	0.36 + 0.022*SL	0.36 + 0.019*SL	0.37 + 0.018*SL
	t_R	0.18	0.13 + 0.023*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.16	0.10 + 0.029*SL	0.09 + 0.031*SL	0.07 + 0.034*SL
D to Y	t_{PLH}	0.49	0.45 + 0.018*SL	0.46 + 0.014*SL	0.49 + 0.012*SL
	t_{PHL}	0.38	0.34 + 0.023*SL	0.34 + 0.019*SL	0.35 + 0.018*SL
	t_R	0.18	0.13 + 0.022*SL	0.13 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
E to Y	t_{PLH}	0.48	0.44 + 0.019*SL	0.45 + 0.014*SL	0.48 + 0.012*SL
	t_{PHL}	0.41	0.37 + 0.022*SL	0.37 + 0.019*SL	0.39 + 0.018*SL
	t_R	0.18	0.13 + 0.022*SL	0.13 + 0.023*SL	0.10 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STDM80 NR5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.85	0.77 + 0.040*SL	0.79 + 0.035*SL	0.80 + 0.034*SL
	t_{PHL}	0.56	0.47 + 0.048*SL	0.48 + 0.045*SL	0.48 + 0.044*SL
	t_R	0.29	0.16 + 0.066*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.28	0.12 + 0.080*SL	0.11 + 0.081*SL	0.10 + 0.083*SL
B to Y	t_{PLH}	0.76	0.68 + 0.040*SL	0.69 + 0.035*SL	0.70 + 0.034*SL
	t_{PHL}	0.51	0.42 + 0.049*SL	0.43 + 0.045*SL	0.43 + 0.044*SL
	t_R	0.29	0.16 + 0.068*SL	0.16 + 0.068*SL	0.14 + 0.071*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
C to Y	t_{PLH}	0.82	0.74 + 0.040*SL	0.75 + 0.035*SL	0.77 + 0.034*SL
	t_{PHL}	0.55	0.45 + 0.048*SL	0.46 + 0.045*SL	0.46 + 0.044*SL
	t_R	0.29	0.16 + 0.067*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.28	0.12 + 0.079*SL	0.11 + 0.081*SL	0.10 + 0.083*SL
D to Y	t_{PLH}	0.64	0.56 + 0.040*SL	0.57 + 0.035*SL	0.58 + 0.033*SL
	t_{PHL}	0.53	0.43 + 0.048*SL	0.44 + 0.045*SL	0.45 + 0.044*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.28	0.13 + 0.078*SL	0.12 + 0.081*SL	0.10 + 0.083*SL
E to Y	t_{PLH}	0.65	0.57 + 0.040*SL	0.59 + 0.035*SL	0.60 + 0.033*SL
	t_{PHL}	0.56	0.46 + 0.048*SL	0.47 + 0.045*SL	0.48 + 0.044*SL
	t_R	0.28	0.15 + 0.068*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.28	0.12 + 0.080*SL	0.12 + 0.081*SL	0.11 + 0.082*SL

STDM80 NR5D2

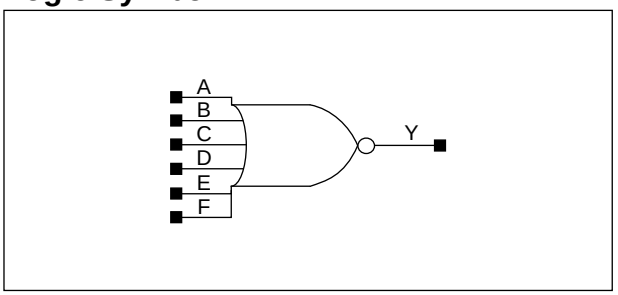
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.89	0.84 + 0.026*SL	0.85 + 0.021*SL	0.87 + 0.019*SL
	t_{PHL}	0.56	0.50 + 0.029*SL	0.52 + 0.025*SL	0.53 + 0.022*SL
	t_R	0.24	0.17 + 0.034*SL	0.17 + 0.033*SL	0.17 + 0.034*SL
	t_F	0.20	0.12 + 0.039*SL	0.12 + 0.038*SL	0.12 + 0.039*SL
B to Y	t_{PLH}	0.79	0.74 + 0.026*SL	0.76 + 0.021*SL	0.78 + 0.019*SL
	t_{PHL}	0.51	0.46 + 0.029*SL	0.47 + 0.024*SL	0.48 + 0.022*SL
	t_R	0.24	0.17 + 0.033*SL	0.17 + 0.034*SL	0.17 + 0.033*SL
	t_F	0.20	0.12 + 0.041*SL	0.13 + 0.037*SL	0.12 + 0.039*SL
C to Y	t_{PLH}	0.86	0.80 + 0.026*SL	0.82 + 0.021*SL	0.84 + 0.019*SL
	t_{PHL}	0.55	0.49 + 0.029*SL	0.50 + 0.024*SL	0.52 + 0.022*SL
	t_R	0.24	0.17 + 0.034*SL	0.17 + 0.033*SL	0.17 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.12 + 0.038*SL	0.12 + 0.039*SL
D to Y	t_{PLH}	0.67	0.62 + 0.025*SL	0.63 + 0.021*SL	0.65 + 0.019*SL
	t_{PHL}	0.53	0.47 + 0.029*SL	0.48 + 0.024*SL	0.50 + 0.022*SL
	t_R	0.23	0.16 + 0.035*SL	0.16 + 0.034*SL	0.16 + 0.034*SL
	t_F	0.20	0.12 + 0.038*SL	0.12 + 0.038*SL	0.12 + 0.039*SL
E to Y	t_{PLH}	0.68	0.63 + 0.025*SL	0.65 + 0.021*SL	0.66 + 0.019*SL
	t_{PHL}	0.56	0.50 + 0.029*SL	0.51 + 0.024*SL	0.53 + 0.022*SL
	t_R	0.23	0.16 + 0.035*SL	0.16 + 0.034*SL	0.16 + 0.034*SL
	t_F	0.20	0.13 + 0.037*SL	0.12 + 0.038*SL	0.12 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

NR6/NR6D2

6-Input NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	0	0	0	1
1	x	x	x	x	x	0
x	1	x	x	x	x	0
x	x	1	x	x	x	0
x	x	x	1	x	x	0
x	x	x	x	1	x	0
x	x	x	x	x	1	0

Cell Data

Input Load (SL)												Gate Count	
STD80													
NR6						*NR6D2*						*NR6*	*NR6D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.6	0.4	0.4	0.6	0.6	0.4	0.6	0.4	0.4	0.6	0.6	0.4	4.3	4.7
STDM80													
NR6						*NR6D2*						*NR6*	*NR6D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.7	0.8	0.8	0.7	0.8	0.8	0.7	0.8	0.8	0.7	0.7	0.8	4.3	4.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NR6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.55	0.48 + 0.034*SL	0.49 + 0.026*SL	0.52 + 0.024*SL
	t_{PHL}	0.45	0.37 + 0.041*SL	0.37 + 0.038*SL	0.38 + 0.037*SL
	t_R	0.24	0.15 + 0.047*SL	0.14 + 0.048*SL	0.11 + 0.052*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
B to Y	t_{PLH}	0.55	0.49 + 0.033*SL	0.50 + 0.026*SL	0.53 + 0.024*SL
	t_{PHL}	0.42	0.33 + 0.041*SL	0.34 + 0.038*SL	0.35 + 0.037*SL
	t_R	0.24	0.15 + 0.044*SL	0.14 + 0.048*SL	0.11 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
C to Y	t_{PLH}	0.55	0.48 + 0.033*SL	0.50 + 0.026*SL	0.52 + 0.024*SL
	t_{PHL}	0.40	0.32 + 0.040*SL	0.33 + 0.038*SL	0.33 + 0.037*SL
	t_R	0.24	0.15 + 0.047*SL	0.14 + 0.048*SL	0.11 + 0.052*SL
	t_F	0.23	0.10 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
D to Y	t_{PLH}	0.54	0.48 + 0.033*SL	0.49 + 0.026*SL	0.52 + 0.024*SL
	t_{PHL}	0.43	0.35 + 0.040*SL	0.36 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.24	0.15 + 0.047*SL	0.14 + 0.048*SL	0.11 + 0.052*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
E to Y	t_{PLH}	0.55	0.48 + 0.033*SL	0.50 + 0.026*SL	0.52 + 0.024*SL
	t_{PHL}	0.42	0.34 + 0.040*SL	0.35 + 0.038*SL	0.35 + 0.037*SL
	t_R	0.24	0.15 + 0.046*SL	0.14 + 0.048*SL	0.11 + 0.052*SL
	t_F	0.23	0.10 + 0.065*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
F to Y	t_{PLH}	0.55	0.49 + 0.033*SL	0.50 + 0.026*SL	0.53 + 0.024*SL
	t_{PHL}	0.39	0.31 + 0.040*SL	0.32 + 0.038*SL	0.32 + 0.037*SL
	t_R	0.24	0.15 + 0.046*SL	0.14 + 0.049*SL	0.11 + 0.052*SL
	t_F	0.23	0.09 + 0.065*SL	0.09 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NR6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.57	0.53 + 0.022*SL	0.54 + 0.016*SL	0.58 + 0.012*SL
	t_{PHL}	0.44	0.39 + 0.023*SL	0.40 + 0.020*SL	0.41 + 0.018*SL
	t_R	0.22	0.17 + 0.023*SL	0.17 + 0.023*SL	0.15 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
B to Y	t_{PLH}	0.58	0.53 + 0.022*SL	0.55 + 0.016*SL	0.59 + 0.012*SL
	t_{PHL}	0.41	0.36 + 0.023*SL	0.37 + 0.020*SL	0.38 + 0.018*SL
	t_R	0.22	0.17 + 0.025*SL	0.17 + 0.023*SL	0.15 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
C to Y	t_{PLH}	0.57	0.53 + 0.023*SL	0.54 + 0.016*SL	0.58 + 0.012*SL
	t_{PHL}	0.39	0.35 + 0.023*SL	0.35 + 0.020*SL	0.37 + 0.018*SL
	t_R	0.22	0.17 + 0.025*SL	0.17 + 0.023*SL	0.15 + 0.026*SL
	t_F	0.17	0.10 + 0.033*SL	0.10 + 0.031*SL	0.08 + 0.034*SL
D to Y	t_{PLH}	0.57	0.52 + 0.022*SL	0.54 + 0.016*SL	0.58 + 0.012*SL
	t_{PHL}	0.42	0.38 + 0.023*SL	0.38 + 0.020*SL	0.40 + 0.018*SL
	t_R	0.22	0.17 + 0.026*SL	0.17 + 0.023*SL	0.15 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.08 + 0.034*SL
E to Y	t_{PLH}	0.58	0.53 + 0.022*SL	0.54 + 0.016*SL	0.59 + 0.012*SL
	t_{PHL}	0.42	0.37 + 0.023*SL	0.38 + 0.020*SL	0.39 + 0.018*SL
	t_R	0.22	0.17 + 0.023*SL	0.17 + 0.024*SL	0.15 + 0.026*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.08 + 0.034*SL
F to Y	t_{PLH}	0.58	0.54 + 0.022*SL	0.55 + 0.016*SL	0.59 + 0.012*SL
	t_{PHL}	0.39	0.34 + 0.023*SL	0.35 + 0.019*SL	0.36 + 0.018*SL
	t_R	0.22	0.17 + 0.023*SL	0.17 + 0.024*SL	0.15 + 0.026*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.032*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NR6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.79	0.70 + 0.046*SL	0.72 + 0.038*SL	0.75 + 0.035*SL
	t_{PHL}	0.61	0.51 + 0.051*SL	0.52 + 0.046*SL	0.54 + 0.044*SL
	t_R	0.33	0.19 + 0.070*SL	0.20 + 0.068*SL	0.19 + 0.069*SL
	t_F	0.30	0.14 + 0.079*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
B to Y	t_{PLH}	0.78	0.68 + 0.046*SL	0.71 + 0.038*SL	0.73 + 0.035*SL
	t_{PHL}	0.58	0.48 + 0.051*SL	0.49 + 0.046*SL	0.50 + 0.044*SL
	t_R	0.33	0.19 + 0.071*SL	0.20 + 0.068*SL	0.19 + 0.069*SL
	t_F	0.30	0.15 + 0.078*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
C to Y	t_{PLH}	0.77	0.68 + 0.046*SL	0.70 + 0.038*SL	0.72 + 0.035*SL
	t_{PHL}	0.56	0.46 + 0.050*SL	0.47 + 0.046*SL	0.48 + 0.044*SL
	t_R	0.33	0.19 + 0.071*SL	0.20 + 0.068*SL	0.19 + 0.070*SL
	t_F	0.30	0.14 + 0.079*SL	0.13 + 0.080*SL	0.12 + 0.082*SL
D to Y	t_{PLH}	0.79	0.70 + 0.045*SL	0.72 + 0.038*SL	0.74 + 0.035*SL
	t_{PHL}	0.59	0.49 + 0.050*SL	0.50 + 0.046*SL	0.51 + 0.044*SL
	t_R	0.33	0.19 + 0.071*SL	0.20 + 0.069*SL	0.19 + 0.069*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.12 + 0.082*SL
E to Y	t_{PLH}	0.80	0.70 + 0.045*SL	0.73 + 0.038*SL	0.75 + 0.035*SL
	t_{PHL}	0.58	0.48 + 0.050*SL	0.49 + 0.046*SL	0.50 + 0.044*SL
	t_R	0.33	0.19 + 0.071*SL	0.20 + 0.068*SL	0.19 + 0.070*SL
	t_F	0.29	0.13 + 0.081*SL	0.13 + 0.080*SL	0.12 + 0.082*SL
F to Y	t_{PLH}	0.78	0.69 + 0.046*SL	0.71 + 0.038*SL	0.73 + 0.035*SL
	t_{PHL}	0.55	0.45 + 0.050*SL	0.46 + 0.046*SL	0.47 + 0.044*SL
	t_R	0.34	0.20 + 0.070*SL	0.20 + 0.068*SL	0.19 + 0.069*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

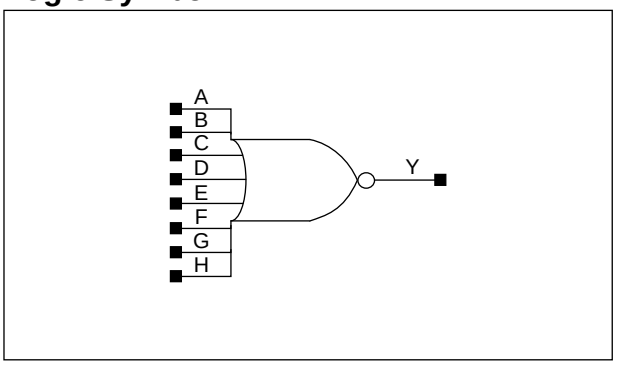
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NR6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.82	0.76 + 0.030*SL	0.78 + 0.024*SL	0.81 + 0.021*SL
	t_{PHL}	0.60	0.54 + 0.031*SL	0.55 + 0.026*SL	0.57 + 0.023*SL
	t_R	0.28	0.20 + 0.036*SL	0.21 + 0.036*SL	0.21 + 0.035*SL
	t_F	0.22	0.14 + 0.041*SL	0.14 + 0.038*SL	0.14 + 0.038*SL
B to Y	t_{PLH}	0.81	0.75 + 0.030*SL	0.77 + 0.024*SL	0.79 + 0.020*SL
	t_{PHL}	0.57	0.51 + 0.030*SL	0.52 + 0.026*SL	0.54 + 0.023*SL
	t_R	0.28	0.20 + 0.037*SL	0.21 + 0.035*SL	0.22 + 0.034*SL
	t_F	0.22	0.13 + 0.042*SL	0.15 + 0.038*SL	0.14 + 0.038*SL
C to Y	t_{PLH}	0.80	0.74 + 0.030*SL	0.76 + 0.024*SL	0.78 + 0.020*SL
	t_{PHL}	0.55	0.48 + 0.031*SL	0.50 + 0.025*SL	0.52 + 0.023*SL
	t_R	0.28	0.20 + 0.037*SL	0.21 + 0.035*SL	0.22 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.13 + 0.039*SL	0.14 + 0.038*SL
D to Y	t_{PLH}	0.82	0.76 + 0.030*SL	0.78 + 0.024*SL	0.80 + 0.020*SL
	t_{PHL}	0.58	0.52 + 0.030*SL	0.53 + 0.025*SL	0.55 + 0.023*SL
	t_R	0.28	0.20 + 0.037*SL	0.21 + 0.036*SL	0.22 + 0.034*SL
	t_F	0.21	0.13 + 0.039*SL	0.13 + 0.039*SL	0.14 + 0.038*SL
E to Y	t_{PLH}	0.83	0.77 + 0.029*SL	0.79 + 0.024*SL	0.81 + 0.020*SL
	t_{PHL}	0.57	0.51 + 0.030*SL	0.52 + 0.025*SL	0.54 + 0.023*SL
	t_R	0.28	0.20 + 0.038*SL	0.21 + 0.036*SL	0.22 + 0.034*SL
	t_F	0.21	0.12 + 0.042*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
F to Y	t_{PLH}	0.82	0.75 + 0.030*SL	0.77 + 0.024*SL	0.80 + 0.020*SL
	t_{PHL}	0.54	0.48 + 0.030*SL	0.49 + 0.025*SL	0.51 + 0.023*SL
	t_R	0.28	0.20 + 0.038*SL	0.21 + 0.036*SL	0.22 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.13 + 0.039*SL	0.13 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	0	0	0	0	0	0	1
1	x	x	x	x	x	x	x	0
x	1	x	x	x	x	x	x	0
x	x	1	x	x	x	x	x	0
x	x	x	1	x	x	x	x	0
x	x	x	x	1	x	x	x	0
x	x	x	x	x	1	x	x	0
x	x	x	x	x	x	1	x	0
x	x	x	x	x	x	x	1	0

Cell Data

Input Load (SL)																Gate Count	
STD80																	
NR8								*NR8D2*								*NR8*	*NR8D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
0.6	0.5	0.5	0.4	0.4	0.6	0.6	0.6	0.6	0.5	0.5	0.4	0.4	0.6	0.6	0.6	4.3	4.7
STDM80																	
NR8								*NR8D2*								*NR8*	*NR8D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
0.7	0.7	0.7	0.8	0.8	0.7	0.7	0.7	0.7	0.8	0.7	0.8	0.8	0.7	0.7	0.7	4.3	4.7

NR8/NR8D2

8-Input NOR with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NR8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.66	0.60 + 0.029*SL	0.61 + 0.025*SL	0.62 + 0.024*SL
	t_{PHL}	0.45	0.37 + 0.039*SL	0.38 + 0.037*SL	0.38 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
B to Y	t_{PLH}	0.65	0.59 + 0.029*SL	0.60 + 0.025*SL	0.61 + 0.024*SL
	t_{PHL}	0.44	0.36 + 0.040*SL	0.37 + 0.037*SL	0.37 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.22	0.10 + 0.060*SL	0.09 + 0.068*SL	0.07 + 0.069*SL
C to Y	t_{PLH}	0.63	0.57 + 0.030*SL	0.58 + 0.025*SL	0.59 + 0.024*SL
	t_{PHL}	0.42	0.35 + 0.039*SL	0.35 + 0.037*SL	0.35 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
D to Y	t_{PLH}	0.59	0.53 + 0.030*SL	0.54 + 0.025*SL	0.55 + 0.024*SL
	t_{PHL}	0.39	0.31 + 0.039*SL	0.32 + 0.037*SL	0.32 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.09 + 0.068*SL	0.07 + 0.069*SL
E to Y	t_{PLH}	0.62	0.56 + 0.029*SL	0.57 + 0.025*SL	0.58 + 0.024*SL
	t_{PHL}	0.38	0.30 + 0.040*SL	0.31 + 0.037*SL	0.31 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.068*SL	0.07 + 0.069*SL
F to Y	t_{PLH}	0.68	0.62 + 0.029*SL	0.63 + 0.025*SL	0.64 + 0.024*SL
	t_{PHL}	0.43	0.35 + 0.039*SL	0.36 + 0.037*SL	0.36 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.22	0.09 + 0.066*SL	0.08 + 0.068*SL	0.07 + 0.069*SL
G to Y	t_{PLH}	0.66	0.60 + 0.029*SL	0.61 + 0.025*SL	0.62 + 0.024*SL
	t_{PHL}	0.42	0.34 + 0.039*SL	0.34 + 0.037*SL	0.34 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.068*SL	0.07 + 0.069*SL
H to Y	t_{PLH}	0.69	0.63 + 0.029*SL	0.64 + 0.025*SL	0.65 + 0.024*SL
	t_{PHL}	0.44	0.36 + 0.039*SL	0.37 + 0.037*SL	0.37 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.22	0.09 + 0.066*SL	0.09 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NR8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.68	0.64 + 0.019*SL	0.65 + 0.015*SL	0.68 + 0.012*SL
	t_{PHL}	0.44	0.40 + 0.022*SL	0.41 + 0.019*SL	0.42 + 0.018*SL
	t_R	0.19	0.14 + 0.022*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
B to Y	t_{PLH}	0.67	0.63 + 0.019*SL	0.64 + 0.015*SL	0.67 + 0.012*SL
	t_{PHL}	0.44	0.39 + 0.023*SL	0.40 + 0.019*SL	0.41 + 0.018*SL
	t_R	0.19	0.14 + 0.024*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
C to Y	t_{PLH}	0.65	0.61 + 0.019*SL	0.62 + 0.015*SL	0.64 + 0.012*SL
	t_{PHL}	0.42	0.37 + 0.022*SL	0.38 + 0.019*SL	0.39 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.16	0.10 + 0.029*SL	0.09 + 0.031*SL	0.07 + 0.034*SL
D to Y	t_{PLH}	0.61	0.57 + 0.019*SL	0.58 + 0.015*SL	0.61 + 0.012*SL
	t_{PHL}	0.39	0.34 + 0.022*SL	0.35 + 0.019*SL	0.36 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.09 + 0.031*SL	0.07 + 0.034*SL
E to Y	t_{PLH}	0.65	0.61 + 0.020*SL	0.62 + 0.014*SL	0.65 + 0.012*SL
	t_{PHL}	0.38	0.33 + 0.022*SL	0.34 + 0.019*SL	0.35 + 0.018*SL
	t_R	0.19	0.15 + 0.021*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.15	0.09 + 0.032*SL	0.09 + 0.032*SL	0.07 + 0.034*SL
F to Y	t_{PLH}	0.71	0.68 + 0.019*SL	0.69 + 0.014*SL	0.71 + 0.012*SL
	t_{PHL}	0.43	0.38 + 0.022*SL	0.39 + 0.019*SL	0.40 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.022*SL	0.12 + 0.026*SL
	t_F	0.15	0.09 + 0.029*SL	0.09 + 0.032*SL	0.07 + 0.034*SL
G to Y	t_{PLH}	0.69	0.65 + 0.019*SL	0.66 + 0.014*SL	0.69 + 0.012*SL
	t_{PHL}	0.41	0.37 + 0.022*SL	0.37 + 0.019*SL	0.38 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.022*SL	0.12 + 0.026*SL
	t_F	0.15	0.09 + 0.029*SL	0.09 + 0.032*SL	0.07 + 0.034*SL
H to Y	t_{PLH}	0.72	0.68 + 0.019*SL	0.69 + 0.014*SL	0.72 + 0.012*SL
	t_{PHL}	0.44	0.39 + 0.023*SL	0.40 + 0.019*SL	0.41 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.16	0.10 + 0.029*SL	0.09 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NR8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.05	0.97 + 0.041*SL	0.98 + 0.035*SL	1.00 + 0.034*SL
	t_{PHL}	0.60	0.50 + 0.049*SL	0.51 + 0.045*SL	0.52 + 0.044*SL
	t_R	0.30	0.17 + 0.068*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.28	0.13 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
B to Y	t_{PLH}	1.01	0.93 + 0.041*SL	0.95 + 0.036*SL	0.96 + 0.034*SL
	t_{PHL}	0.59	0.50 + 0.048*SL	0.51 + 0.045*SL	0.51 + 0.044*SL
	t_R	0.30	0.17 + 0.067*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.28	0.13 + 0.078*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
C to Y	t_{PLH}	0.93	0.85 + 0.041*SL	0.87 + 0.035*SL	0.88 + 0.034*SL
	t_{PHL}	0.58	0.48 + 0.048*SL	0.49 + 0.045*SL	0.49 + 0.044*SL
	t_R	0.30	0.17 + 0.067*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.28	0.12 + 0.080*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D to Y	t_{PLH}	0.83	0.75 + 0.041*SL	0.76 + 0.036*SL	0.78 + 0.034*SL
	t_{PHL}	0.54	0.45 + 0.048*SL	0.46 + 0.045*SL	0.46 + 0.044*SL
	t_R	0.30	0.17 + 0.068*SL	0.17 + 0.068*SL	0.15 + 0.071*SL
	t_F	0.28	0.12 + 0.081*SL	0.12 + 0.081*SL	0.11 + 0.083*SL
E to Y	t_{PLH}	0.88	0.80 + 0.041*SL	0.81 + 0.035*SL	0.82 + 0.034*SL
	t_{PHL}	0.53	0.43 + 0.048*SL	0.44 + 0.045*SL	0.45 + 0.044*SL
	t_R	0.30	0.17 + 0.066*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.10 + 0.083*SL
F to Y	t_{PLH}	1.07	0.98 + 0.041*SL	1.00 + 0.035*SL	1.01 + 0.034*SL
	t_{PHL}	0.58	0.48 + 0.048*SL	0.49 + 0.045*SL	0.50 + 0.044*SL
	t_R	0.30	0.17 + 0.066*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.28	0.12 + 0.080*SL	0.11 + 0.081*SL	0.11 + 0.083*SL
G to Y	t_{PLH}	0.98	0.90 + 0.041*SL	0.92 + 0.035*SL	0.93 + 0.034*SL
	t_{PHL}	0.56	0.46 + 0.048*SL	0.47 + 0.045*SL	0.48 + 0.044*SL
	t_R	0.30	0.17 + 0.066*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.28	0.12 + 0.079*SL	0.11 + 0.081*SL	0.10 + 0.083*SL
H to Y	t_{PLH}	1.10	1.02 + 0.041*SL	1.04 + 0.035*SL	1.05 + 0.034*SL
	t_{PHL}	0.58	0.49 + 0.048*SL	0.50 + 0.045*SL	0.50 + 0.044*SL
	t_R	0.30	0.17 + 0.066*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.28	0.13 + 0.078*SL	0.12 + 0.081*SL	0.10 + 0.083*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NR8D2

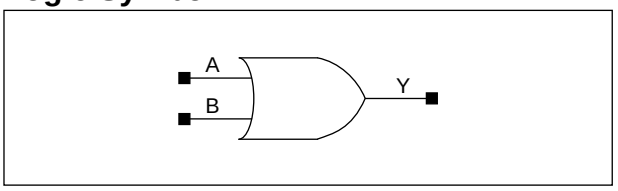
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.08	1.02 + 0.026*SL	1.04 + 0.022*SL	1.06 + 0.019*SL
	t_{PHL}	0.60	0.54 + 0.029*SL	0.55 + 0.025*SL	0.57 + 0.022*SL
	t_R	0.24	0.17 + 0.034*SL	0.17 + 0.034*SL	0.18 + 0.033*SL
	t_F	0.21	0.12 + 0.040*SL	0.14 + 0.037*SL	0.12 + 0.038*SL
B to Y	t_{PLH}	1.04	0.99 + 0.026*SL	1.00 + 0.021*SL	1.02 + 0.019*SL
	t_{PHL}	0.59	0.53 + 0.029*SL	0.54 + 0.025*SL	0.56 + 0.022*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.20	0.12 + 0.041*SL	0.13 + 0.037*SL	0.13 + 0.038*SL
C to Y	t_{PLH}	0.96	0.90 + 0.026*SL	0.92 + 0.022*SL	0.94 + 0.019*SL
	t_{PHL}	0.57	0.51 + 0.029*SL	0.53 + 0.024*SL	0.54 + 0.022*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.20	0.12 + 0.041*SL	0.13 + 0.037*SL	0.12 + 0.039*SL
D to Y	t_{PLH}	0.86	0.80 + 0.027*SL	0.82 + 0.021*SL	0.84 + 0.019*SL
	t_{PHL}	0.54	0.48 + 0.029*SL	0.49 + 0.025*SL	0.51 + 0.022*SL
	t_R	0.24	0.17 + 0.034*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.037*SL	0.12 + 0.038*SL
E to Y	t_{PLH}	0.92	0.87 + 0.027*SL	0.88 + 0.021*SL	0.90 + 0.019*SL
	t_{PHL}	0.52	0.47 + 0.029*SL	0.48 + 0.024*SL	0.49 + 0.022*SL
	t_R	0.25	0.18 + 0.033*SL	0.18 + 0.033*SL	0.18 + 0.034*SL
	t_F	0.20	0.12 + 0.037*SL	0.12 + 0.039*SL	0.12 + 0.038*SL
F to Y	t_{PLH}	1.11	1.06 + 0.026*SL	1.07 + 0.021*SL	1.09 + 0.019*SL
	t_{PHL}	0.58	0.52 + 0.029*SL	0.53 + 0.024*SL	0.54 + 0.022*SL
	t_R	0.25	0.19 + 0.032*SL	0.18 + 0.034*SL	0.18 + 0.033*SL
	t_F	0.19	0.12 + 0.039*SL	0.12 + 0.038*SL	0.11 + 0.039*SL
G to Y	t_{PLH}	1.03	0.98 + 0.026*SL	0.99 + 0.021*SL	1.01 + 0.019*SL
	t_{PHL}	0.56	0.50 + 0.029*SL	0.51 + 0.024*SL	0.53 + 0.022*SL
	t_R	0.25	0.18 + 0.034*SL	0.19 + 0.033*SL	0.18 + 0.033*SL
	t_F	0.19	0.11 + 0.039*SL	0.12 + 0.038*SL	0.11 + 0.039*SL
H to Y	t_{PLH}	1.15	1.09 + 0.026*SL	1.11 + 0.021*SL	1.13 + 0.019*SL
	t_{PHL}	0.58	0.53 + 0.029*SL	0.54 + 0.024*SL	0.55 + 0.022*SL
	t_R	0.25	0.18 + 0.032*SL	0.18 + 0.033*SL	0.18 + 0.033*SL
	t_F	0.20	0.12 + 0.038*SL	0.12 + 0.038*SL	0.12 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

OR2/OR2D2

2-Input OR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Cell Data

Input Load (SL)				Gate Count	
STD80					
OR2		*OR2D2*		*OR2*	*OR2D2*
A	B	A	B		
0.4	0.7	0.4	0.7	1.3	1.7
STDM80					
OR2		*OR2D2*		*OR2*	*OR2D2*
A	B	A	B		
0.8	0.8	0.8	0.8	1.3	1.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 OR2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.17 + 0.026*SL	0.17 + 0.024*SL	0.17 + 0.024*SL
	t_{PHL}	0.41	0.33 + 0.042*SL	0.33 + 0.038*SL	0.35 + 0.037*SL
	t_R	0.19	0.10 + 0.047*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
B to Y	t_{PLH}	0.25	0.20 + 0.027*SL	0.20 + 0.024*SL	0.20 + 0.024*SL
	t_{PHL}	0.40	0.32 + 0.042*SL	0.33 + 0.038*SL	0.34 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.25	0.12 + 0.064*SL	0.12 + 0.066*SL	0.09 + 0.069*SL

STD80 OR2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.20 + 0.017*SL	0.21 + 0.013*SL	0.22 + 0.012*SL
	t_{PHL}	0.43	0.38 + 0.025*SL	0.39 + 0.021*SL	0.42 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.21	0.14 + 0.032*SL	0.15 + 0.031*SL	0.12 + 0.034*SL
B to Y	t_{PLH}	0.26	0.23 + 0.018*SL	0.24 + 0.013*SL	0.25 + 0.012*SL
	t_{PHL}	0.43	0.38 + 0.025*SL	0.39 + 0.021*SL	0.41 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.21	0.15 + 0.031*SL	0.15 + 0.031*SL	0.12 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 OR2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.23 + 0.036*SL	0.24 + 0.033*SL	0.24 + 0.033*SL
	t_{PHL}	0.54	0.43 + 0.055*SL	0.45 + 0.048*SL	0.47 + 0.045*SL
	t_R	0.25	0.12 + 0.068*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.33	0.16 + 0.082*SL	0.17 + 0.079*SL	0.16 + 0.081*SL
B to Y	t_{PLH}	0.33	0.26 + 0.036*SL	0.27 + 0.034*SL	0.27 + 0.033*SL
	t_{PHL}	0.56	0.45 + 0.055*SL	0.47 + 0.048*SL	0.49 + 0.045*SL
	t_R	0.26	0.13 + 0.066*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.33	0.16 + 0.081*SL	0.17 + 0.079*SL	0.16 + 0.081*SL

STDM80 OR2D2

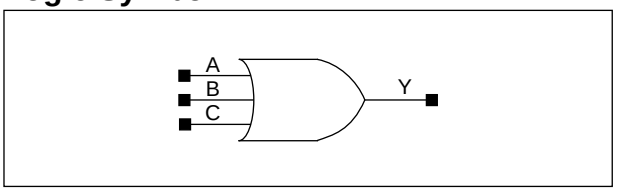
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.31	0.26 + 0.022*SL	0.27 + 0.018*SL	0.28 + 0.017*SL
	t_{PHL}	0.58	0.51 + 0.034*SL	0.53 + 0.029*SL	0.56 + 0.025*SL
	t_R	0.18	0.12 + 0.032*SL	0.11 + 0.034*SL	0.11 + 0.034*SL
	t_F	0.27	0.18 + 0.042*SL	0.19 + 0.039*SL	0.20 + 0.038*SL
B to Y	t_{PLH}	0.33	0.29 + 0.023*SL	0.30 + 0.018*SL	0.31 + 0.017*SL
	t_{PHL}	0.61	0.54 + 0.034*SL	0.55 + 0.028*SL	0.58 + 0.025*SL
	t_R	0.19	0.12 + 0.033*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.27	0.18 + 0.043*SL	0.19 + 0.040*SL	0.20 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

OR3/OR3D3

3-Input OR with 1X/3X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
1	x	x	1
x	1	x	1
x	x	1	1

Cell Data

Input Load (SL)						Gate Count	
STD80							
OR3			*OR3D3*			*OR3*	*OR3D3*
A	B	C	A	B	C		
0.4	0.6	0.7	0.4	0.6	0.6	1.7	2.3
STDM80							
OR3			*OR3D3*			*OR3*	*OR3D3*
A	B	C	A	B	C		
0.8	0.7	0.7	0.8	0.7	0.7	1.7	2.3

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 OR3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.17 + 0.027*SL	0.18 + 0.024*SL	0.18 + 0.024*SL
	t_{PHL}	0.50	0.41 + 0.046*SL	0.42 + 0.040*SL	0.45 + 0.037*SL
	t_R	0.19	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.30	0.16 + 0.066*SL	0.17 + 0.065*SL	0.13 + 0.069*SL
B to Y	t_{PLH}	0.26	0.20 + 0.027*SL	0.21 + 0.024*SL	0.21 + 0.024*SL
	t_{PHL}	0.52	0.43 + 0.047*SL	0.44 + 0.040*SL	0.47 + 0.037*SL
	t_R	0.20	0.12 + 0.040*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.30	0.17 + 0.065*SL	0.17 + 0.065*SL	0.13 + 0.069*SL
C to Y	t_{PLH}	0.27	0.22 + 0.027*SL	0.23 + 0.024*SL	0.23 + 0.024*SL
	t_{PHL}	0.52	0.43 + 0.047*SL	0.44 + 0.040*SL	0.47 + 0.037*SL
	t_R	0.21	0.12 + 0.041*SL	0.11 + 0.048*SL	0.07 + 0.052*SL
	t_F	0.30	0.17 + 0.065*SL	0.17 + 0.065*SL	0.13 + 0.069*SL

STD80 OR3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.25 + 0.013*SL	0.26 + 0.010*SL	0.28 + 0.008*SL
	t_{PHL}	0.65	0.61 + 0.021*SL	0.62 + 0.017*SL	0.66 + 0.012*SL
	t_R	0.16	0.13 + 0.013*SL	0.13 + 0.015*SL	0.11 + 0.017*SL
	t_F	0.32	0.28 + 0.022*SL	0.28 + 0.021*SL	0.27 + 0.021*SL
B to Y	t_{PLH}	0.30	0.28 + 0.013*SL	0.28 + 0.010*SL	0.30 + 0.008*SL
	t_{PHL}	0.67	0.63 + 0.021*SL	0.64 + 0.017*SL	0.69 + 0.012*SL
	t_R	0.17	0.14 + 0.013*SL	0.14 + 0.014*SL	0.11 + 0.017*SL
	t_F	0.32	0.27 + 0.023*SL	0.28 + 0.021*SL	0.27 + 0.021*SL
C to Y	t_{PLH}	0.32	0.29 + 0.011*SL	0.29 + 0.010*SL	0.32 + 0.008*SL
	t_{PHL}	0.68	0.63 + 0.022*SL	0.64 + 0.017*SL	0.69 + 0.012*SL
	t_R	0.17	0.15 + 0.013*SL	0.15 + 0.014*SL	0.12 + 0.017*SL
	t_F	0.32	0.27 + 0.023*SL	0.28 + 0.021*SL	0.27 + 0.021*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 OR3

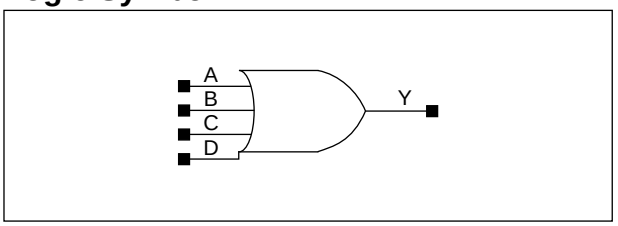
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.24 + 0.036*SL	0.25 + 0.034*SL	0.25 + 0.033*SL
	t_{PHL}	0.69	0.57 + 0.063*SL	0.60 + 0.053*SL	0.63 + 0.048*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.39	0.22 + 0.085*SL	0.24 + 0.081*SL	0.24 + 0.080*SL
B to Y	t_{PLH}	0.35	0.27 + 0.037*SL	0.28 + 0.034*SL	0.28 + 0.033*SL
	t_{PHL}	0.75	0.63 + 0.063*SL	0.66 + 0.053*SL	0.69 + 0.048*SL
	t_R	0.26	0.12 + 0.070*SL	0.13 + 0.069*SL	0.10 + 0.072*SL
	t_F	0.40	0.22 + 0.086*SL	0.24 + 0.080*SL	0.25 + 0.079*SL
C to Y	t_{PLH}	0.36	0.29 + 0.037*SL	0.30 + 0.034*SL	0.30 + 0.034*SL
	t_{PHL}	0.79	0.66 + 0.063*SL	0.69 + 0.053*SL	0.73 + 0.048*SL
	t_R	0.27	0.13 + 0.068*SL	0.13 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.40	0.22 + 0.086*SL	0.24 + 0.080*SL	0.25 + 0.079*SL

STDM80 OR3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.36	0.32 + 0.016*SL	0.33 + 0.014*SL	0.34 + 0.012*SL
	t_{PHL}	0.95	0.89 + 0.029*SL	0.90 + 0.024*SL	0.92 + 0.021*SL
	t_R	0.19	0.14 + 0.022*SL	0.14 + 0.022*SL	0.14 + 0.022*SL
	t_F	0.41	0.35 + 0.032*SL	0.36 + 0.029*SL	0.37 + 0.027*SL
B to Y	t_{PLH}	0.38	0.35 + 0.017*SL	0.36 + 0.014*SL	0.37 + 0.012*SL
	t_{PHL}	1.01	0.95 + 0.029*SL	0.97 + 0.024*SL	0.99 + 0.021*SL
	t_R	0.20	0.15 + 0.020*SL	0.15 + 0.022*SL	0.15 + 0.022*SL
	t_F	0.41	0.35 + 0.032*SL	0.36 + 0.028*SL	0.37 + 0.027*SL
C to Y	t_{PLH}	0.40	0.36 + 0.017*SL	0.37 + 0.014*SL	0.38 + 0.013*SL
	t_{PHL}	1.05	0.99 + 0.029*SL	1.00 + 0.024*SL	1.02 + 0.021*SL
	t_R	0.20	0.16 + 0.022*SL	0.16 + 0.022*SL	0.16 + 0.022*SL
	t_F	0.41	0.35 + 0.032*SL	0.36 + 0.029*SL	0.37 + 0.027*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

Cell Data

Input Load (SL)								Gate Count	
STD80									
OR4				*OR4D2*				*OR4*	*OR4D2*
A	B	C	D	A	B	C	D		
0.4	0.7	0.7	0.5	0.4	0.7	0.7	0.4	2.7	3.0
STDM80									
OR4				*OR4D2*				*OR4*	*OR4D2*
A	B	C	D	A	B	C	D		
0.8	0.8	0.7	0.8	0.8	0.8	0.8	0.8	2.7	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 OR4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.19 + 0.025*SL	0.19 + 0.025*SL	0.19 + 0.025*SL
	t_{PHL}	0.41	0.32 + 0.041*SL	0.33 + 0.039*SL	0.34 + 0.039*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.051*SL	0.09 + 0.054*SL
	t_F	0.28	0.14 + 0.071*SL	0.13 + 0.075*SL	0.11 + 0.078*SL
B to Y	t_{PLH}	0.27	0.22 + 0.026*SL	0.22 + 0.025*SL	0.22 + 0.025*SL
	t_{PHL}	0.40	0.32 + 0.041*SL	0.32 + 0.039*SL	0.33 + 0.039*SL
	t_R	0.23	0.14 + 0.044*SL	0.13 + 0.051*SL	0.10 + 0.054*SL
	t_F	0.29	0.14 + 0.072*SL	0.14 + 0.075*SL	0.11 + 0.078*SL
C to Y	t_{PLH}	0.27	0.21 + 0.027*SL	0.22 + 0.025*SL	0.22 + 0.025*SL
	t_{PHL}	0.41	0.33 + 0.043*SL	0.33 + 0.039*SL	0.34 + 0.039*SL
	t_R	0.21	0.12 + 0.046*SL	0.11 + 0.051*SL	0.08 + 0.054*SL
	t_F	0.29	0.15 + 0.072*SL	0.14 + 0.075*SL	0.12 + 0.078*SL
D to Y	t_{PLH}	0.24	0.18 + 0.027*SL	0.19 + 0.025*SL	0.19 + 0.025*SL
	t_{PHL}	0.42	0.33 + 0.043*SL	0.34 + 0.039*SL	0.35 + 0.039*SL
	t_R	0.20	0.11 + 0.047*SL	0.10 + 0.052*SL	0.08 + 0.054*SL
	t_F	0.29	0.15 + 0.073*SL	0.14 + 0.075*SL	0.12 + 0.078*SL

STD80 OR4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.27	0.24 + 0.014*SL	0.25 + 0.013*SL	0.25 + 0.012*SL
	t_{PHL}	0.45	0.40 + 0.023*SL	0.41 + 0.020*SL	0.42 + 0.019*SL
	t_R	0.20	0.15 + 0.023*SL	0.15 + 0.023*SL	0.11 + 0.027*SL
	t_F	0.25	0.18 + 0.034*SL	0.17 + 0.035*SL	0.14 + 0.039*SL
B to Y	t_{PLH}	0.30	0.27 + 0.013*SL	0.27 + 0.013*SL	0.28 + 0.012*SL
	t_{PHL}	0.44	0.40 + 0.023*SL	0.40 + 0.020*SL	0.41 + 0.019*SL
	t_R	0.20	0.16 + 0.022*SL	0.16 + 0.023*SL	0.12 + 0.027*SL
	t_F	0.25	0.18 + 0.033*SL	0.17 + 0.036*SL	0.15 + 0.039*SL
C to Y	t_{PLH}	0.29	0.25 + 0.017*SL	0.26 + 0.013*SL	0.27 + 0.012*SL
	t_{PHL}	0.45	0.40 + 0.024*SL	0.41 + 0.021*SL	0.42 + 0.019*SL
	t_R	0.18	0.13 + 0.023*SL	0.13 + 0.023*SL	0.10 + 0.027*SL
	t_F	0.25	0.18 + 0.034*SL	0.17 + 0.036*SL	0.15 + 0.038*SL
D to Y	t_{PLH}	0.26	0.23 + 0.015*SL	0.23 + 0.013*SL	0.24 + 0.012*SL
	t_{PHL}	0.45	0.40 + 0.024*SL	0.41 + 0.021*SL	0.43 + 0.019*SL
	t_R	0.17	0.13 + 0.020*SL	0.12 + 0.024*SL	0.09 + 0.027*SL
	t_F	0.25	0.18 + 0.035*SL	0.18 + 0.036*SL	0.15 + 0.038*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 OR4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.33	0.26 + 0.036*SL	0.26 + 0.035*SL	0.26 + 0.035*SL
	t_{PHL}	0.54	0.43 + 0.057*SL	0.45 + 0.052*SL	0.46 + 0.051*SL
	t_R	0.30	0.16 + 0.071*SL	0.15 + 0.074*SL	0.14 + 0.075*SL
	t_F	0.38	0.19 + 0.096*SL	0.19 + 0.097*SL	0.18 + 0.098*SL
B to Y	t_{PLH}	0.37	0.29 + 0.036*SL	0.30 + 0.035*SL	0.30 + 0.035*SL
	t_{PHL}	0.57	0.45 + 0.056*SL	0.47 + 0.052*SL	0.48 + 0.050*SL
	t_R	0.30	0.16 + 0.070*SL	0.15 + 0.074*SL	0.14 + 0.075*SL
	t_F	0.38	0.19 + 0.096*SL	0.19 + 0.097*SL	0.18 + 0.098*SL
C to Y	t_{PLH}	0.35	0.28 + 0.037*SL	0.28 + 0.035*SL	0.28 + 0.035*SL
	t_{PHL}	0.58	0.46 + 0.059*SL	0.48 + 0.052*SL	0.50 + 0.050*SL
	t_R	0.28	0.13 + 0.072*SL	0.13 + 0.074*SL	0.12 + 0.075*SL
	t_F	0.39	0.20 + 0.097*SL	0.20 + 0.096*SL	0.19 + 0.097*SL
D to Y	t_{PLH}	0.32	0.25 + 0.036*SL	0.25 + 0.035*SL	0.25 + 0.035*SL
	t_{PHL}	0.56	0.44 + 0.059*SL	0.46 + 0.052*SL	0.48 + 0.050*SL
	t_R	0.28	0.13 + 0.071*SL	0.12 + 0.074*SL	0.12 + 0.075*SL
	t_F	0.39	0.20 + 0.096*SL	0.20 + 0.096*SL	0.19 + 0.097*SL

STDM80 OR4D2

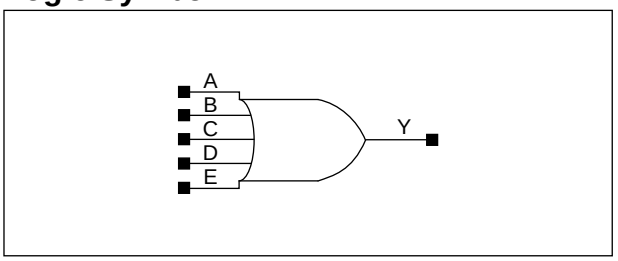
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.31 + 0.020*SL	0.32 + 0.018*SL	0.33 + 0.018*SL
	t_{PHL}	0.62	0.55 + 0.032*SL	0.56 + 0.029*SL	0.57 + 0.027*SL
	t_R	0.24	0.17 + 0.034*SL	0.17 + 0.035*SL	0.16 + 0.036*SL
	t_F	0.32	0.22 + 0.047*SL	0.22 + 0.048*SL	0.22 + 0.048*SL
B to Y	t_{PLH}	0.38	0.34 + 0.020*SL	0.35 + 0.019*SL	0.36 + 0.018*SL
	t_{PHL}	0.64	0.57 + 0.032*SL	0.58 + 0.029*SL	0.60 + 0.027*SL
	t_R	0.24	0.18 + 0.033*SL	0.17 + 0.035*SL	0.17 + 0.036*SL
	t_F	0.32	0.22 + 0.048*SL	0.22 + 0.047*SL	0.22 + 0.048*SL
C to Y	t_{PLH}	0.36	0.32 + 0.022*SL	0.33 + 0.019*SL	0.34 + 0.018*SL
	t_{PHL}	0.64	0.57 + 0.034*SL	0.59 + 0.030*SL	0.61 + 0.027*SL
	t_R	0.22	0.15 + 0.033*SL	0.15 + 0.035*SL	0.14 + 0.036*SL
	t_F	0.33	0.23 + 0.049*SL	0.24 + 0.048*SL	0.24 + 0.047*SL
D to Y	t_{PLH}	0.33	0.29 + 0.022*SL	0.30 + 0.019*SL	0.31 + 0.018*SL
	t_{PHL}	0.62	0.55 + 0.034*SL	0.57 + 0.030*SL	0.59 + 0.027*SL
	t_R	0.21	0.14 + 0.035*SL	0.14 + 0.035*SL	0.13 + 0.036*SL
	t_F	0.33	0.23 + 0.048*SL	0.23 + 0.048*SL	0.24 + 0.047*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

OR5/OR5D2

5-Input OR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	0
1	x	x	x	x	1
x	1	x	x	x	1
x	x	1	x	x	1
x	x	x	1	x	1
x	x	x	x	1	1

Cell Data

Input Load (SL)										Gate Count	
STD80											
OR5					*OR5D2*					*OR5*	*OR5D2*
A	B	C	D	E	A	B	C	D	E		
0.4	0.6	0.7	0.7	0.5	0.4	0.6	0.7	0.7	0.4	3.0	3.3
STDM80											
OR5					*OR5D2*					*OR5*	*OR5D2*
A	B	C	D	E	A	B	C	D	E		
0.8	0.8	0.8	0.7	0.8	0.8	0.8	0.8	0.8	0.8	3.0	3.3

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 OR5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.20 + 0.026*SL	0.21 + 0.025*SL	0.20 + 0.025*SL
	t_{PHL}	0.51	0.41 + 0.045*SL	0.42 + 0.042*SL	0.43 + 0.041*SL
	t_R	0.23	0.14 + 0.044*SL	0.12 + 0.051*SL	0.09 + 0.054*SL
	t_F	0.34	0.19 + 0.075*SL	0.18 + 0.077*SL	0.14 + 0.082*SL
B to Y	t_{PLH}	0.28	0.23 + 0.027*SL	0.24 + 0.025*SL	0.23 + 0.025*SL
	t_{PHL}	0.52	0.43 + 0.045*SL	0.44 + 0.042*SL	0.45 + 0.041*SL
	t_R	0.23	0.14 + 0.045*SL	0.13 + 0.050*SL	0.10 + 0.054*SL
	t_F	0.34	0.20 + 0.070*SL	0.18 + 0.078*SL	0.14 + 0.082*SL
C to Y	t_{PLH}	0.30	0.25 + 0.027*SL	0.25 + 0.025*SL	0.25 + 0.025*SL
	t_{PHL}	0.53	0.43 + 0.045*SL	0.44 + 0.042*SL	0.45 + 0.041*SL
	t_R	0.24	0.15 + 0.044*SL	0.14 + 0.050*SL	0.10 + 0.054*SL
	t_F	0.34	0.19 + 0.074*SL	0.18 + 0.077*SL	0.14 + 0.082*SL
D to Y	t_{PLH}	0.26	0.21 + 0.027*SL	0.21 + 0.025*SL	0.21 + 0.025*SL
	t_{PHL}	0.42	0.33 + 0.045*SL	0.33 + 0.041*SL	0.34 + 0.041*SL
	t_R	0.21	0.11 + 0.048*SL	0.11 + 0.051*SL	0.08 + 0.054*SL
	t_F	0.30	0.15 + 0.078*SL	0.14 + 0.079*SL	0.12 + 0.082*SL
E to Y	t_{PLH}	0.23	0.18 + 0.026*SL	0.18 + 0.025*SL	0.18 + 0.025*SL
	t_{PHL}	0.42	0.33 + 0.045*SL	0.34 + 0.041*SL	0.35 + 0.041*SL
	t_R	0.20	0.11 + 0.048*SL	0.10 + 0.051*SL	0.08 + 0.054*SL
	t_F	0.30	0.15 + 0.078*SL	0.14 + 0.080*SL	0.12 + 0.082*SL

STD80 OR5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.25 + 0.014*SL	0.26 + 0.013*SL	0.26 + 0.012*SL
	t_{PHL}	0.57	0.51 + 0.026*SL	0.52 + 0.022*SL	0.55 + 0.019*SL
	t_R	0.20	0.15 + 0.023*SL	0.15 + 0.024*SL	0.12 + 0.027*SL
	t_F	0.32	0.26 + 0.031*SL	0.25 + 0.033*SL	0.20 + 0.038*SL
B to Y	t_{PLH}	0.31	0.28 + 0.014*SL	0.28 + 0.013*SL	0.29 + 0.012*SL
	t_{PHL}	0.59	0.54 + 0.025*SL	0.54 + 0.022*SL	0.57 + 0.019*SL
	t_R	0.20	0.17 + 0.018*SL	0.16 + 0.023*SL	0.12 + 0.027*SL
	t_F	0.32	0.25 + 0.032*SL	0.25 + 0.033*SL	0.20 + 0.038*SL
C to Y	t_{PLH}	0.32	0.30 + 0.013*SL	0.30 + 0.013*SL	0.31 + 0.012*SL
	t_{PHL}	0.59	0.54 + 0.026*SL	0.55 + 0.022*SL	0.57 + 0.019*SL
	t_R	0.21	0.17 + 0.020*SL	0.17 + 0.023*SL	0.13 + 0.027*SL
	t_F	0.32	0.26 + 0.030*SL	0.25 + 0.034*SL	0.20 + 0.038*SL
D to Y	t_{PLH}	0.29	0.25 + 0.017*SL	0.26 + 0.013*SL	0.27 + 0.012*SL
	t_{PHL}	0.45	0.40 + 0.023*SL	0.41 + 0.021*SL	0.42 + 0.019*SL
	t_R	0.18	0.14 + 0.022*SL	0.13 + 0.023*SL	0.10 + 0.027*SL
	t_F	0.25	0.18 + 0.034*SL	0.18 + 0.036*SL	0.15 + 0.039*SL
E to Y	t_{PLH}	0.26	0.23 + 0.015*SL	0.23 + 0.013*SL	0.24 + 0.012*SL
	t_{PHL}	0.45	0.41 + 0.023*SL	0.41 + 0.021*SL	0.43 + 0.019*SL
	t_R	0.17	0.13 + 0.021*SL	0.12 + 0.024*SL	0.09 + 0.027*SL
	t_F	0.25	0.18 + 0.035*SL	0.18 + 0.036*SL	0.15 + 0.039*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 OR5

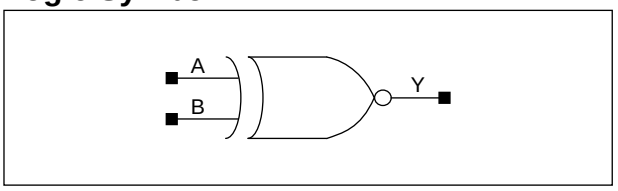
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.28 + 0.036*SL	0.28 + 0.035*SL	0.28 + 0.035*SL
	t_{PHL}	0.70	0.57 + 0.063*SL	0.59 + 0.057*SL	0.61 + 0.054*SL
	t_R	0.30	0.17 + 0.068*SL	0.15 + 0.074*SL	0.14 + 0.075*SL
	t_F	0.45	0.25 + 0.100*SL	0.25 + 0.101*SL	0.24 + 0.102*SL
B to Y	t_{PLH}	0.38	0.31 + 0.036*SL	0.31 + 0.035*SL	0.32 + 0.035*SL
	t_{PHL}	0.76	0.64 + 0.062*SL	0.65 + 0.057*SL	0.68 + 0.054*SL
	t_R	0.30	0.16 + 0.071*SL	0.15 + 0.073*SL	0.14 + 0.075*SL
	t_F	0.45	0.25 + 0.099*SL	0.25 + 0.101*SL	0.24 + 0.102*SL
C to Y	t_{PLH}	0.40	0.32 + 0.038*SL	0.33 + 0.036*SL	0.33 + 0.035*SL
	t_{PHL}	0.80	0.67 + 0.062*SL	0.69 + 0.057*SL	0.71 + 0.054*SL
	t_R	0.31	0.17 + 0.071*SL	0.16 + 0.073*SL	0.15 + 0.075*SL
	t_F	0.45	0.25 + 0.100*SL	0.25 + 0.101*SL	0.24 + 0.102*SL
D to Y	t_{PLH}	0.35	0.27 + 0.036*SL	0.28 + 0.035*SL	0.28 + 0.035*SL
	t_{PHL}	0.58	0.46 + 0.061*SL	0.48 + 0.055*SL	0.49 + 0.053*SL
	t_R	0.28	0.13 + 0.072*SL	0.13 + 0.074*SL	0.12 + 0.075*SL
	t_F	0.41	0.20 + 0.103*SL	0.20 + 0.102*SL	0.20 + 0.103*SL
E to Y	t_{PLH}	0.32	0.24 + 0.036*SL	0.25 + 0.035*SL	0.25 + 0.035*SL
	t_{PHL}	0.57	0.44 + 0.061*SL	0.46 + 0.055*SL	0.48 + 0.053*SL
	t_R	0.28	0.14 + 0.068*SL	0.12 + 0.074*SL	0.11 + 0.075*SL
	t_F	0.41	0.21 + 0.101*SL	0.20 + 0.102*SL	0.20 + 0.103*SL

STDM80 OR5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.37	0.33 + 0.021*SL	0.34 + 0.018*SL	0.34 + 0.018*SL
	t_{PHL}	0.81	0.74 + 0.035*SL	0.76 + 0.031*SL	0.78 + 0.028*SL
	t_R	0.24	0.18 + 0.033*SL	0.17 + 0.035*SL	0.16 + 0.036*SL
	t_F	0.41	0.32 + 0.045*SL	0.32 + 0.046*SL	0.31 + 0.047*SL
B to Y	t_{PLH}	0.40	0.36 + 0.021*SL	0.36 + 0.019*SL	0.37 + 0.018*SL
	t_{PHL}	0.88	0.81 + 0.035*SL	0.82 + 0.031*SL	0.84 + 0.028*SL
	t_R	0.25	0.18 + 0.034*SL	0.18 + 0.034*SL	0.17 + 0.036*SL
	t_F	0.41	0.32 + 0.044*SL	0.31 + 0.046*SL	0.31 + 0.047*SL
C to Y	t_{PLH}	0.42	0.37 + 0.021*SL	0.38 + 0.019*SL	0.39 + 0.018*SL
	t_{PHL}	0.92	0.85 + 0.035*SL	0.86 + 0.031*SL	0.88 + 0.028*SL
	t_R	0.26	0.19 + 0.033*SL	0.19 + 0.035*SL	0.18 + 0.035*SL
	t_F	0.41	0.32 + 0.044*SL	0.31 + 0.046*SL	0.31 + 0.047*SL
D to Y	t_{PLH}	0.37	0.32 + 0.021*SL	0.33 + 0.019*SL	0.34 + 0.018*SL
	t_{PHL}	0.65	0.58 + 0.034*SL	0.59 + 0.030*SL	0.61 + 0.027*SL
	t_R	0.22	0.15 + 0.033*SL	0.15 + 0.035*SL	0.14 + 0.036*SL
	t_F	0.33	0.23 + 0.050*SL	0.24 + 0.047*SL	0.24 + 0.048*SL
E to Y	t_{PLH}	0.34	0.29 + 0.022*SL	0.30 + 0.019*SL	0.31 + 0.018*SL
	t_{PHL}	0.62	0.56 + 0.034*SL	0.57 + 0.030*SL	0.59 + 0.027*SL
	t_R	0.21	0.14 + 0.035*SL	0.14 + 0.035*SL	0.13 + 0.036*SL
	t_F	0.33	0.24 + 0.049*SL	0.24 + 0.047*SL	0.24 + 0.048*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Cell Data

Input Load (SL)				Gate Count	
STD80					
XN2		*XN2D2*		*XN2*	*XN2D2*
A	B	A	B		
0.8	1.5	0.8	1.5	2.7	3.0
STDM80					
XN2		*XN2D2*		*XN2*	*XN2D2*
A	B	A	B		
0.8	1.5	0.8	1.5	2.7	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 XN2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.47	0.41 + 0.029*SL	0.42 + 0.025*SL	0.43 + 0.024*SL
	t_{PHL}	0.50	0.41 + 0.044*SL	0.42 + 0.039*SL	0.44 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.29	0.16 + 0.062*SL	0.16 + 0.064*SL	0.11 + 0.069*SL
B to Y	t_{PLH}	0.34	0.28 + 0.029*SL	0.29 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.40	0.30 + 0.045*SL	0.32 + 0.039*SL	0.34 + 0.037*SL
	t_R	0.21	0.11 + 0.048*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.26	0.12 + 0.068*SL	0.13 + 0.066*SL	0.10 + 0.069*SL

STD80 XN2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.48	0.44 + 0.020*SL	0.45 + 0.015*SL	0.48 + 0.012*SL
	t_{PHL}	0.51	0.46 + 0.027*SL	0.47 + 0.021*SL	0.50 + 0.018*SL
	t_R	0.18	0.14 + 0.022*SL	0.13 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.21	0.14 + 0.034*SL	0.15 + 0.031*SL	0.13 + 0.034*SL
B to Y	t_{PLH}	0.34	0.30 + 0.022*SL	0.31 + 0.015*SL	0.34 + 0.012*SL
	t_{PHL}	0.39	0.34 + 0.026*SL	0.35 + 0.021*SL	0.38 + 0.018*SL
	t_R	0.18	0.14 + 0.018*SL	0.13 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.21	0.14 + 0.034*SL	0.14 + 0.032*SL	0.12 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

XN2/XN2D2

2-Input Exclusive-NOR with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 XN2

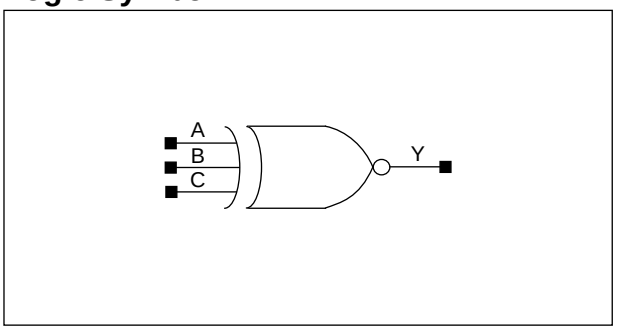
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.64	0.56 + 0.040*SL	0.57 + 0.035*SL	0.59 + 0.034*SL
	t_{PHL}	0.71	0.60 + 0.057*SL	0.62 + 0.049*SL	0.64 + 0.045*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.34	0.18 + 0.081*SL	0.18 + 0.079*SL	0.18 + 0.080*SL
B to Y	t_{PLH}	0.46	0.38 + 0.041*SL	0.40 + 0.035*SL	0.41 + 0.034*SL
	t_{PHL}	0.54	0.42 + 0.059*SL	0.45 + 0.050*SL	0.47 + 0.046*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.34	0.18 + 0.084*SL	0.19 + 0.080*SL	0.19 + 0.080*SL

STDM80 XN2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.65	0.60 + 0.026*SL	0.61 + 0.021*SL	0.63 + 0.019*SL
	t_{PHL}	0.72	0.65 + 0.035*SL	0.66 + 0.029*SL	0.69 + 0.025*SL
	t_R	0.23	0.16 + 0.035*SL	0.16 + 0.034*SL	0.16 + 0.034*SL
	t_F	0.28	0.19 + 0.042*SL	0.20 + 0.040*SL	0.21 + 0.038*SL
B to Y	t_{PLH}	0.46	0.41 + 0.026*SL	0.43 + 0.021*SL	0.44 + 0.019*SL
	t_{PHL}	0.53	0.46 + 0.037*SL	0.48 + 0.030*SL	0.51 + 0.026*SL
	t_R	0.23	0.16 + 0.035*SL	0.16 + 0.034*SL	0.16 + 0.034*SL
	t_F	0.28	0.19 + 0.045*SL	0.20 + 0.041*SL	0.22 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Data

Input Load (SL)						Gate Count	
STD80							
XN3			*XN3D3*			*XN3*	*XN3D3*
A	B	C	A	B	C		
1.0	0.8	1.5	1.0	0.8	1.5	4.3	5.0
STDM80							
XN3			*XN3D3*			*XN3*	*XN3D3*
A	B	C	A	B	C		
1.5	0.8	1.5	1.5	0.8	1.5	4.3	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 XN3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.36	0.29 + 0.035*SL	0.31 + 0.028*SL	0.35 + 0.024*SL
	t_{PHL}	0.42	0.32 + 0.050*SL	0.33 + 0.042*SL	0.38 + 0.037*SL
	t_R	0.24	0.14 + 0.047*SL	0.14 + 0.050*SL	0.12 + 0.052*SL
	t_F	0.29	0.15 + 0.070*SL	0.16 + 0.068*SL	0.15 + 0.069*SL
B to Y	t_{PLH}	0.66	0.60 + 0.030*SL	0.61 + 0.025*SL	0.62 + 0.024*SL
	t_{PHL}	0.77	0.68 + 0.044*SL	0.69 + 0.039*SL	0.71 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.066*SL	0.13 + 0.065*SL	0.09 + 0.069*SL
C to Y	t_{PLH}	0.54	0.48 + 0.030*SL	0.49 + 0.025*SL	0.50 + 0.024*SL
	t_{PHL}	0.64	0.55 + 0.044*SL	0.56 + 0.039*SL	0.57 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.064*SL	0.13 + 0.065*SL	0.09 + 0.069*SL

STD80 XN3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.40	0.36 + 0.018*SL	0.37 + 0.014*SL	0.43 + 0.008*SL
	t_{PHL}	0.49	0.44 + 0.024*SL	0.45 + 0.019*SL	0.51 + 0.013*SL
	t_R	0.24	0.21 + 0.019*SL	0.21 + 0.017*SL	0.22 + 0.017*SL
	t_F	0.30	0.25 + 0.027*SL	0.26 + 0.023*SL	0.27 + 0.022*SL
B to Y	t_{PLH}	0.70	0.66 + 0.019*SL	0.67 + 0.014*SL	0.73 + 0.008*SL
	t_{PHL}	0.83	0.79 + 0.018*SL	0.79 + 0.016*SL	0.83 + 0.012*SL
	t_R	0.29	0.25 + 0.018*SL	0.25 + 0.016*SL	0.25 + 0.016*SL
	t_F	0.23	0.19 + 0.023*SL	0.19 + 0.020*SL	0.18 + 0.022*SL
C to Y	t_{PLH}	0.59	0.56 + 0.015*SL	0.57 + 0.012*SL	0.60 + 0.008*SL
	t_{PHL}	0.69	0.65 + 0.019*SL	0.66 + 0.016*SL	0.70 + 0.012*SL
	t_R	0.21	0.17 + 0.017*SL	0.18 + 0.015*SL	0.16 + 0.017*SL
	t_F	0.23	0.19 + 0.023*SL	0.19 + 0.021*SL	0.18 + 0.022*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 XN3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.50	0.40 + 0.047*SL	0.43 + 0.040*SL	0.46 + 0.036*SL
	t_{PHL}	0.56	0.42 + 0.066*SL	0.45 + 0.056*SL	0.50 + 0.050*SL
	t_R	0.33	0.18 + 0.075*SL	0.19 + 0.070*SL	0.20 + 0.070*SL
	t_F	0.38	0.19 + 0.095*SL	0.22 + 0.085*SL	0.25 + 0.082*SL
B to Y	t_{PLH}	0.95	0.87 + 0.041*SL	0.89 + 0.036*SL	0.90 + 0.034*SL
	t_{PHL}	1.07	0.93 + 0.071*SL	0.97 + 0.057*SL	1.02 + 0.051*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.14 + 0.070*SL
	t_F	0.50	0.33 + 0.086*SL	0.35 + 0.079*SL	0.35 + 0.078*SL
C to Y	t_{PLH}	0.78	0.70 + 0.041*SL	0.71 + 0.036*SL	0.73 + 0.034*SL
	t_{PHL}	0.89	0.75 + 0.071*SL	0.79 + 0.058*SL	0.84 + 0.051*SL
	t_R	0.30	0.16 + 0.067*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.50	0.33 + 0.085*SL	0.34 + 0.079*SL	0.35 + 0.078*SL

STDM80 XN3D3

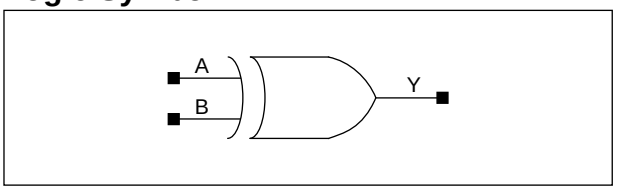
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.57	0.52 + 0.024*SL	0.53 + 0.020*SL	0.55 + 0.017*SL
	t_{PHL}	0.70	0.63 + 0.033*SL	0.65 + 0.027*SL	0.68 + 0.023*SL
	t_R	0.31	0.25 + 0.027*SL	0.26 + 0.025*SL	0.27 + 0.024*SL
	t_F	0.41	0.34 + 0.036*SL	0.36 + 0.031*SL	0.37 + 0.029*SL
B to Y	t_{PLH}	1.02	0.98 + 0.020*SL	0.99 + 0.016*SL	1.01 + 0.014*SL
	t_{PHL}	1.19	1.13 + 0.033*SL	1.15 + 0.027*SL	1.17 + 0.023*SL
	t_R	0.25	0.21 + 0.023*SL	0.21 + 0.023*SL	0.21 + 0.022*SL
	t_F	0.49	0.42 + 0.035*SL	0.43 + 0.030*SL	0.45 + 0.027*SL
C to Y	t_{PLH}	0.85	0.81 + 0.020*SL	0.82 + 0.017*SL	0.84 + 0.014*SL
	t_{PHL}	1.01	0.95 + 0.033*SL	0.97 + 0.027*SL	0.99 + 0.023*SL
	t_R	0.25	0.20 + 0.026*SL	0.21 + 0.022*SL	0.21 + 0.023*SL
	t_F	0.49	0.42 + 0.035*SL	0.43 + 0.029*SL	0.45 + 0.027*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

XO2/XO2D2

2-Input Exclusive-OR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Cell Data

Input Load (SL)				Gate Count	
STD80					
XO2		*XO2D2*		*XO2*	*XO2D2*
A	B	A	B		
0.7	1.0	0.7	1.0	2.7	3.0
STDM80					
XO2		*XO2D2*		*XO2*	*XO2D2*
A	B	A	B		
0.8	1.5	0.8	1.5	2.7	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 XO2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.47	0.41 + 0.030*SL	0.42 + 0.025*SL	0.43 + 0.024*SL
	t_{PHL}	0.51	0.42 + 0.044*SL	0.43 + 0.038*SL	0.45 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.066*SL	0.09 + 0.069*SL
B to Y	t_{PLH}	0.34	0.28 + 0.029*SL	0.29 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.40	0.31 + 0.044*SL	0.32 + 0.039*SL	0.34 + 0.037*SL
	t_R	0.21	0.12 + 0.047*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL

STD80 XO2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.47	0.44 + 0.019*SL	0.44 + 0.015*SL	0.47 + 0.012*SL
	t_{PHL}	0.51	0.46 + 0.026*SL	0.47 + 0.021*SL	0.50 + 0.018*SL
	t_R	0.18	0.14 + 0.021*SL	0.13 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.21	0.14 + 0.034*SL	0.15 + 0.031*SL	0.13 + 0.033*SL
B to Y	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.015*SL	0.34 + 0.012*SL
	t_{PHL}	0.39	0.34 + 0.026*SL	0.35 + 0.021*SL	0.38 + 0.018*SL
	t_R	0.18	0.13 + 0.022*SL	0.13 + 0.024*SL	0.11 + 0.026*SL
	t_F	0.20	0.14 + 0.034*SL	0.14 + 0.032*SL	0.12 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 XO2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.64	0.55 + 0.041*SL	0.57 + 0.035*SL	0.58 + 0.033*SL
	t_{PHL}	0.71	0.60 + 0.057*SL	0.62 + 0.049*SL	0.65 + 0.045*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.068*SL	0.14 + 0.071*SL
	t_F	0.34	0.18 + 0.081*SL	0.19 + 0.079*SL	0.17 + 0.080*SL
B to Y	t_{PLH}	0.46	0.38 + 0.042*SL	0.39 + 0.036*SL	0.41 + 0.034*SL
	t_{PHL}	0.54	0.43 + 0.057*SL	0.45 + 0.048*SL	0.47 + 0.045*SL
	t_R	0.29	0.16 + 0.069*SL	0.16 + 0.068*SL	0.14 + 0.071*SL
	t_F	0.34	0.18 + 0.081*SL	0.18 + 0.079*SL	0.17 + 0.080*SL

STDM80 XO2D2

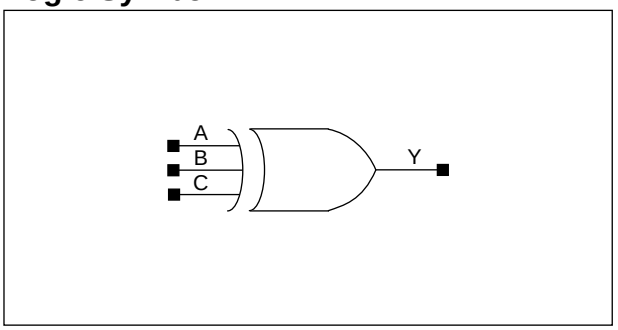
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.65	0.59 + 0.026*SL	0.61 + 0.021*SL	0.62 + 0.019*SL
	t_{PHL}	0.72	0.65 + 0.036*SL	0.67 + 0.029*SL	0.70 + 0.025*SL
	t_R	0.23	0.16 + 0.036*SL	0.16 + 0.034*SL	0.16 + 0.034*SL
	t_F	0.28	0.19 + 0.043*SL	0.20 + 0.040*SL	0.21 + 0.038*SL
B to Y	t_{PLH}	0.46	0.41 + 0.027*SL	0.42 + 0.022*SL	0.44 + 0.019*SL
	t_{PHL}	0.54	0.47 + 0.036*SL	0.49 + 0.029*SL	0.51 + 0.025*SL
	t_R	0.23	0.16 + 0.036*SL	0.16 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.27	0.19 + 0.044*SL	0.20 + 0.040*SL	0.21 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

XO3/XO3D3

3-Input Exclusive-OR with 1X/3X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Data

Input Load (SL)						Gate Count	
STD80							
XO3			*XO3D3*			*XO3*	*XO3D3*
A	B	C	A	B	C		
1.5	0.8	1.5	1.5	0.7	1.5	4.3	5.0
STDM80							
XO3			*XO3D3*			*XO3*	*XO3D3*
A	B	C	A	B	C		
1.5	0.8	1.5	1.5	0.8	1.5	4.3	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 XO3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.34	0.28 + 0.029*SL	0.29 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.44	0.34 + 0.052*SL	0.36 + 0.043*SL	0.41 + 0.037*SL
	t_R	0.21	0.12 + 0.046*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.31	0.16 + 0.071*SL	0.17 + 0.067*SL	0.16 + 0.069*SL
B to Y	t_{PLH}	0.66	0.60 + 0.031*SL	0.61 + 0.025*SL	0.62 + 0.024*SL
	t_{PHL}	0.77	0.68 + 0.044*SL	0.69 + 0.039*SL	0.71 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.065*SL	0.09 + 0.069*SL
C to Y	t_{PLH}	0.54	0.48 + 0.031*SL	0.49 + 0.025*SL	0.51 + 0.024*SL
	t_{PHL}	0.63	0.55 + 0.044*SL	0.56 + 0.039*SL	0.57 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.26	0.13 + 0.064*SL	0.13 + 0.066*SL	0.09 + 0.069*SL

STD80 XO3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.37	0.34 + 0.015*SL	0.35 + 0.011*SL	0.38 + 0.008*SL
	t_{PHL}	0.50	0.45 + 0.024*SL	0.46 + 0.019*SL	0.53 + 0.013*SL
	t_R	0.19	0.16 + 0.016*SL	0.16 + 0.016*SL	0.15 + 0.017*SL
	t_F	0.32	0.27 + 0.026*SL	0.27 + 0.023*SL	0.29 + 0.021*SL
B to Y	t_{PLH}	0.71	0.68 + 0.015*SL	0.69 + 0.012*SL	0.72 + 0.008*SL
	t_{PHL}	0.83	0.79 + 0.019*SL	0.80 + 0.016*SL	0.83 + 0.012*SL
	t_R	0.20	0.17 + 0.015*SL	0.17 + 0.016*SL	0.16 + 0.017*SL
	t_F	0.23	0.19 + 0.022*SL	0.19 + 0.021*SL	0.18 + 0.022*SL
C to Y	t_{PLH}	0.59	0.56 + 0.015*SL	0.57 + 0.012*SL	0.61 + 0.008*SL
	t_{PHL}	0.69	0.65 + 0.019*SL	0.66 + 0.016*SL	0.70 + 0.012*SL
	t_R	0.21	0.17 + 0.017*SL	0.18 + 0.015*SL	0.16 + 0.017*SL
	t_F	0.23	0.19 + 0.023*SL	0.19 + 0.021*SL	0.18 + 0.022*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 XO3

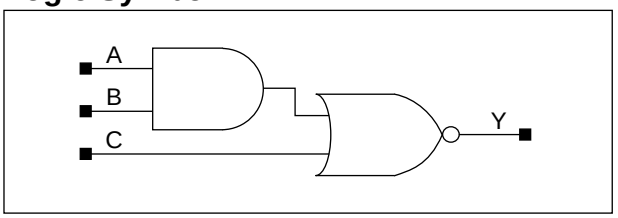
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.46	0.38 + 0.041*SL	0.40 + 0.035*SL	0.41 + 0.033*SL
	t_{PHL}	0.61	0.47 + 0.069*SL	0.51 + 0.057*SL	0.55 + 0.051*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.42	0.23 + 0.093*SL	0.26 + 0.084*SL	0.28 + 0.081*SL
B to Y	t_{PLH}	0.96	0.87 + 0.042*SL	0.89 + 0.036*SL	0.91 + 0.034*SL
	t_{PHL}	1.07	0.93 + 0.071*SL	0.97 + 0.058*SL	1.02 + 0.051*SL
	t_R	0.30	0.16 + 0.067*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.50	0.32 + 0.087*SL	0.35 + 0.079*SL	0.36 + 0.078*SL
C to Y	t_{PLH}	0.78	0.70 + 0.042*SL	0.72 + 0.036*SL	0.73 + 0.034*SL
	t_{PHL}	0.89	0.75 + 0.071*SL	0.79 + 0.058*SL	0.84 + 0.051*SL
	t_R	0.30	0.17 + 0.066*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.49	0.32 + 0.086*SL	0.34 + 0.079*SL	0.35 + 0.078*SL

STDM80 XO3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.51	0.47 + 0.020*SL	0.48 + 0.016*SL	0.49 + 0.014*SL
	t_{PHL}	0.73	0.66 + 0.033*SL	0.68 + 0.027*SL	0.71 + 0.023*SL
	t_R	0.24	0.20 + 0.024*SL	0.20 + 0.024*SL	0.20 + 0.022*SL
	t_F	0.44	0.37 + 0.036*SL	0.39 + 0.030*SL	0.41 + 0.028*SL
B to Y	t_{PLH}	1.03	0.99 + 0.020*SL	1.00 + 0.017*SL	1.02 + 0.014*SL
	t_{PHL}	1.20	1.13 + 0.033*SL	1.15 + 0.027*SL	1.18 + 0.023*SL
	t_R	0.25	0.21 + 0.024*SL	0.21 + 0.023*SL	0.21 + 0.023*SL
	t_F	0.49	0.42 + 0.035*SL	0.43 + 0.030*SL	0.45 + 0.027*SL
C to Y	t_{PLH}	0.86	0.82 + 0.020*SL	0.83 + 0.017*SL	0.84 + 0.014*SL
	t_{PHL}	1.02	0.95 + 0.033*SL	0.97 + 0.027*SL	1.00 + 0.023*SL
	t_R	0.26	0.21 + 0.024*SL	0.21 + 0.023*SL	0.21 + 0.023*SL
	t_F	0.49	0.42 + 0.036*SL	0.44 + 0.030*SL	0.45 + 0.027*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	Y
x	x	1	0
0	x	0	1
x	0	0	1
1	1	x	0

Cell Data

Input Load (SL)						Gate Count	
STD80							
AO21			*AO21D2*			*AO21*	*AO21D2*
A	B	C	A	B	C		
0.5	0.5	0.8	0.9	0.9	1.6	1.3	2.7
STDM80							
AO21			*AO21D2*			*AO21*	*AO21D2*
A	B	C	A	B	C		
1.0	1.0	1.0	2.0	2.1	1.9	1.3	2.7

AO21/AO21D2

2-AND into 2-NOR with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AO21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.14 + 0.046*SL	0.15 + 0.041*SL	0.14 + 0.041*SL
	t_{PHL}	0.25	0.14 + 0.057*SL	0.14 + 0.054*SL	0.14 + 0.055*SL
	t_R	0.44	0.29 + 0.075*SL	0.26 + 0.087*SL	0.19 + 0.095*SL
	t_F	0.38	0.19 + 0.097*SL	0.17 + 0.106*SL	0.13 + 0.111*SL
B to Y	t_{PLH}	0.21	0.11 + 0.050*SL	0.13 + 0.041*SL	0.13 + 0.041*SL
	t_{PHL}	0.27	0.16 + 0.057*SL	0.16 + 0.054*SL	0.16 + 0.055*SL
	t_R	0.41	0.26 + 0.077*SL	0.24 + 0.087*SL	0.17 + 0.095*SL
	t_F	0.39	0.20 + 0.095*SL	0.18 + 0.105*SL	0.12 + 0.111*SL
C to Y	t_{PLH}	0.25	0.16 + 0.044*SL	0.17 + 0.041*SL	0.16 + 0.041*SL
	t_{PHL}	0.29	0.21 + 0.037*SL	0.21 + 0.037*SL	0.21 + 0.037*SL
	t_R	0.41	0.25 + 0.081*SL	0.23 + 0.090*SL	0.18 + 0.095*SL
	t_F	0.39	0.26 + 0.060*SL	0.26 + 0.064*SL	0.21 + 0.069*SL

STD80 AO21D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.14 + 0.025*SL	0.15 + 0.021*SL	0.15 + 0.021*SL
	t_{PHL}	0.19	0.13 + 0.029*SL	0.14 + 0.027*SL	0.14 + 0.027*SL
	t_R	0.38	0.30 + 0.037*SL	0.29 + 0.042*SL	0.23 + 0.048*SL
	t_F	0.28	0.19 + 0.046*SL	0.18 + 0.050*SL	0.14 + 0.054*SL
B to Y	t_{PLH}	0.17	0.11 + 0.029*SL	0.12 + 0.022*SL	0.13 + 0.021*SL
	t_{PHL}	0.21	0.15 + 0.031*SL	0.16 + 0.027*SL	0.16 + 0.027*SL
	t_R	0.34	0.27 + 0.037*SL	0.26 + 0.042*SL	0.20 + 0.048*SL
	t_F	0.29	0.20 + 0.048*SL	0.20 + 0.049*SL	0.14 + 0.054*SL
C to Y	t_{PLH}	0.21	0.17 + 0.023*SL	0.17 + 0.022*SL	0.17 + 0.021*SL
	t_{PHL}	0.25	0.21 + 0.020*SL	0.21 + 0.018*SL	0.21 + 0.018*SL
	t_R	0.34	0.26 + 0.040*SL	0.25 + 0.044*SL	0.21 + 0.048*SL
	t_F	0.32	0.27 + 0.028*SL	0.26 + 0.030*SL	0.23 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AO21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.31	0.18 + 0.062*SL	0.18 + 0.063*SL	0.18 + 0.063*SL
	t_{PHL}	0.33	0.18 + 0.073*SL	0.18 + 0.072*SL	0.19 + 0.072*SL
	t_R	0.56	0.30 + 0.129*SL	0.28 + 0.135*SL	0.26 + 0.139*SL
	t_F	0.47	0.19 + 0.137*SL	0.19 + 0.140*SL	0.17 + 0.142*SL
B to Y	t_{PLH}	0.28	0.16 + 0.063*SL	0.16 + 0.063*SL	0.16 + 0.063*SL
	t_{PHL}	0.34	0.19 + 0.072*SL	0.19 + 0.072*SL	0.20 + 0.072*SL
	t_R	0.53	0.27 + 0.129*SL	0.26 + 0.135*SL	0.23 + 0.139*SL
	t_F	0.47	0.20 + 0.135*SL	0.19 + 0.140*SL	0.17 + 0.142*SL
C to Y	t_{PLH}	0.37	0.24 + 0.064*SL	0.25 + 0.063*SL	0.25 + 0.063*SL
	t_{PHL}	0.34	0.25 + 0.047*SL	0.25 + 0.045*SL	0.26 + 0.045*SL
	t_R	0.56	0.29 + 0.131*SL	0.28 + 0.136*SL	0.26 + 0.139*SL
	t_F	0.42	0.26 + 0.078*SL	0.26 + 0.081*SL	0.24 + 0.083*SL

STDM80 AO21D2

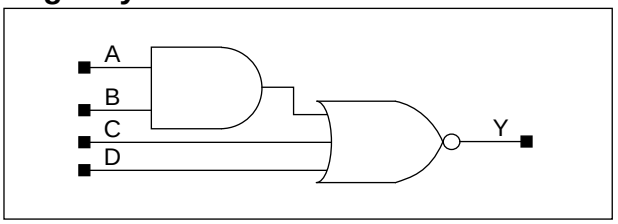
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.19 + 0.031*SL	0.19 + 0.032*SL	0.19 + 0.031*SL
	t_{PHL}	0.25	0.18 + 0.037*SL	0.18 + 0.035*SL	0.19 + 0.035*SL
	t_R	0.44	0.32 + 0.062*SL	0.31 + 0.065*SL	0.29 + 0.068*SL
	t_F	0.32	0.19 + 0.066*SL	0.19 + 0.067*SL	0.18 + 0.068*SL
B to Y	t_{PLH}	0.22	0.15 + 0.034*SL	0.16 + 0.031*SL	0.16 + 0.031*SL
	t_{PHL}	0.26	0.18 + 0.036*SL	0.19 + 0.035*SL	0.19 + 0.035*SL
	t_R	0.40	0.28 + 0.061*SL	0.27 + 0.066*SL	0.25 + 0.068*SL
	t_F	0.33	0.20 + 0.064*SL	0.20 + 0.066*SL	0.19 + 0.068*SL
C to Y	t_{PLH}	0.32	0.25 + 0.033*SL	0.26 + 0.032*SL	0.26 + 0.032*SL
	t_{PHL}	0.29	0.24 + 0.023*SL	0.24 + 0.022*SL	0.25 + 0.022*SL
	t_R	0.44	0.31 + 0.064*SL	0.30 + 0.067*SL	0.29 + 0.068*SL
	t_F	0.34	0.26 + 0.037*SL	0.26 + 0.039*SL	0.26 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

AO211/AO211D2

2-AND into 3-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	1	x	0
x	x	x	1	0
x	0	0	0	1
0	x	0	0	1

Cell Data

Input Load (SL)								Gate Count	
STD80									
AO211				*AO211D2*				*AO211*	*AO211D2*
A	B	C	D	A	B	C	D		
0.5	0.5	0.8	0.9	0.9	0.9	1.3	1.6	1.7	3.3
STDM80									
AO211				*AO211D2*				*AO211*	*AO211D2*
A	B	C	D	A	B	C	D		
1.0	1.0	1.0	1.1	2.0	2.1	2.0	2.0	1.7	3.3

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AO211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.18 + 0.056*SL	0.17 + 0.058*SL	0.16 + 0.060*SL
	t_{PHL}	0.26	0.15 + 0.057*SL	0.15 + 0.054*SL	0.15 + 0.055*SL
	t_R	0.64	0.40 + 0.123*SL	0.38 + 0.132*SL	0.31 + 0.138*SL
	t_F	0.40	0.21 + 0.098*SL	0.19 + 0.107*SL	0.15 + 0.111*SL
B to Y	t_{PLH}	0.27	0.15 + 0.060*SL	0.15 + 0.058*SL	0.14 + 0.060*SL
	t_{PHL}	0.28	0.17 + 0.056*SL	0.18 + 0.054*SL	0.17 + 0.055*SL
	t_R	0.61	0.36 + 0.124*SL	0.34 + 0.132*SL	0.28 + 0.138*SL
	t_F	0.41	0.22 + 0.097*SL	0.20 + 0.106*SL	0.15 + 0.111*SL
C to Y	t_{PLH}	0.35	0.23 + 0.060*SL	0.24 + 0.059*SL	0.23 + 0.060*SL
	t_{PHL}	0.30	0.22 + 0.038*SL	0.22 + 0.037*SL	0.22 + 0.037*SL
	t_R	0.63	0.38 + 0.128*SL	0.37 + 0.134*SL	0.33 + 0.138*SL
	t_F	0.39	0.27 + 0.060*SL	0.26 + 0.064*SL	0.22 + 0.069*SL
D to Y	t_{PLH}	0.36	0.24 + 0.060*SL	0.24 + 0.059*SL	0.24 + 0.060*SL
	t_{PHL}	0.32	0.24 + 0.039*SL	0.25 + 0.038*SL	0.25 + 0.037*SL
	t_R	0.62	0.37 + 0.128*SL	0.35 + 0.135*SL	0.32 + 0.138*SL
	t_F	0.45	0.32 + 0.063*SL	0.32 + 0.064*SL	0.28 + 0.069*SL

STD80 AO211D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.17 + 0.030*SL	0.17 + 0.029*SL	0.16 + 0.031*SL
	t_{PHL}	0.19	0.13 + 0.029*SL	0.14 + 0.027*SL	0.14 + 0.027*SL
	t_R	0.52	0.40 + 0.060*SL	0.39 + 0.065*SL	0.33 + 0.071*SL
	t_F	0.28	0.19 + 0.046*SL	0.18 + 0.050*SL	0.14 + 0.054*SL
B to Y	t_{PLH}	0.20	0.13 + 0.033*SL	0.14 + 0.030*SL	0.13 + 0.031*SL
	t_{PHL}	0.21	0.14 + 0.032*SL	0.16 + 0.027*SL	0.16 + 0.027*SL
	t_R	0.48	0.35 + 0.061*SL	0.34 + 0.065*SL	0.29 + 0.071*SL
	t_F	0.29	0.20 + 0.046*SL	0.19 + 0.049*SL	0.14 + 0.054*SL
C to Y	t_{PLH}	0.29	0.23 + 0.033*SL	0.23 + 0.031*SL	0.23 + 0.031*SL
	t_{PHL}	0.25	0.21 + 0.020*SL	0.21 + 0.018*SL	0.21 + 0.018*SL
	t_R	0.51	0.38 + 0.064*SL	0.37 + 0.067*SL	0.34 + 0.071*SL
	t_F	0.32	0.26 + 0.029*SL	0.26 + 0.030*SL	0.23 + 0.034*SL
D to Y	t_{PLH}	0.31	0.25 + 0.033*SL	0.25 + 0.031*SL	0.25 + 0.031*SL
	t_{PHL}	0.28	0.24 + 0.020*SL	0.24 + 0.019*SL	0.24 + 0.018*SL
	t_R	0.50	0.37 + 0.065*SL	0.36 + 0.068*SL	0.33 + 0.071*SL
	t_F	0.39	0.33 + 0.032*SL	0.33 + 0.031*SL	0.30 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

AO211/AO211D2

2-AND into 3-NOR with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AO211

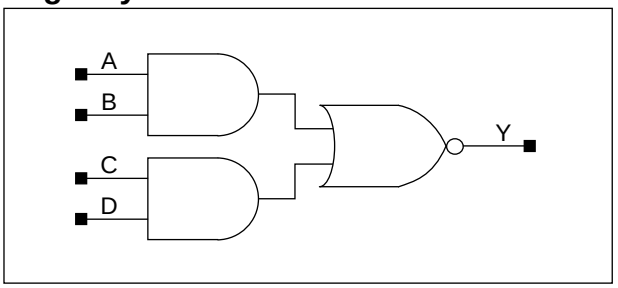
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.40	0.21 + 0.092*SL	0.21 + 0.093*SL	0.21 + 0.093*SL
	t_{PHL}	0.35	0.20 + 0.073*SL	0.20 + 0.072*SL	0.21 + 0.071*SL
	t_R	0.89	0.49 + 0.201*SL	0.47 + 0.206*SL	0.45 + 0.209*SL
	t_F	0.50	0.22 + 0.138*SL	0.22 + 0.141*SL	0.20 + 0.142*SL
B to Y	t_{PLH}	0.37	0.19 + 0.091*SL	0.18 + 0.094*SL	0.18 + 0.093*SL
	t_{PHL}	0.36	0.21 + 0.072*SL	0.21 + 0.072*SL	0.22 + 0.071*SL
	t_R	0.85	0.44 + 0.201*SL	0.43 + 0.206*SL	0.41 + 0.209*SL
	t_F	0.50	0.23 + 0.136*SL	0.22 + 0.140*SL	0.20 + 0.143*SL
C to Y	t_{PLH}	0.54	0.35 + 0.095*SL	0.36 + 0.094*SL	0.36 + 0.094*SL
	t_{PHL}	0.36	0.26 + 0.046*SL	0.27 + 0.045*SL	0.27 + 0.044*SL
	t_R	0.92	0.52 + 0.199*SL	0.51 + 0.204*SL	0.49 + 0.206*SL
	t_F	0.43	0.28 + 0.079*SL	0.27 + 0.081*SL	0.26 + 0.083*SL
D to Y	t_{PLH}	0.58	0.39 + 0.095*SL	0.39 + 0.094*SL	0.39 + 0.094*SL
	t_{PHL}	0.38	0.29 + 0.048*SL	0.29 + 0.046*SL	0.30 + 0.045*SL
	t_R	0.91	0.51 + 0.201*SL	0.50 + 0.205*SL	0.49 + 0.206*SL
	t_F	0.50	0.34 + 0.080*SL	0.33 + 0.081*SL	0.32 + 0.083*SL

STDM80 AO211D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.31	0.22 + 0.043*SL	0.21 + 0.047*SL	0.21 + 0.047*SL
	t_{PHL}	0.27	0.19 + 0.036*SL	0.20 + 0.035*SL	0.20 + 0.035*SL
	t_R	0.70	0.50 + 0.099*SL	0.49 + 0.101*SL	0.48 + 0.103*SL
	t_F	0.34	0.21 + 0.066*SL	0.21 + 0.067*SL	0.20 + 0.068*SL
B to Y	t_{PLH}	0.27	0.19 + 0.042*SL	0.17 + 0.046*SL	0.17 + 0.047*SL
	t_{PHL}	0.27	0.20 + 0.035*SL	0.20 + 0.035*SL	0.20 + 0.035*SL
	t_R	0.63	0.43 + 0.100*SL	0.43 + 0.101*SL	0.42 + 0.103*SL
	t_F	0.35	0.22 + 0.064*SL	0.21 + 0.067*SL	0.20 + 0.068*SL
C to Y	t_{PLH}	0.45	0.36 + 0.048*SL	0.36 + 0.048*SL	0.36 + 0.047*SL
	t_{PHL}	0.30	0.25 + 0.023*SL	0.25 + 0.022*SL	0.26 + 0.022*SL
	t_R	0.73	0.53 + 0.098*SL	0.53 + 0.100*SL	0.51 + 0.102*SL
	t_F	0.34	0.27 + 0.038*SL	0.27 + 0.038*SL	0.26 + 0.039*SL
D to Y	t_{PLH}	0.51	0.41 + 0.049*SL	0.42 + 0.048*SL	0.42 + 0.047*SL
	t_{PHL}	0.33	0.28 + 0.024*SL	0.28 + 0.024*SL	0.29 + 0.023*SL
	t_R	0.73	0.53 + 0.098*SL	0.52 + 0.101*SL	0.51 + 0.102*SL
	t_F	0.42	0.34 + 0.039*SL	0.34 + 0.039*SL	0.34 + 0.040*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	1	1	0
0	x	0	x	1
0	x	x	0	1
x	0	x	0	1
x	0	0	x	1

Cell Data

Input Load (SL)								Gate Count	
STD80									
AO22				*AO22D2*				*AO22*	*AO22D2*
A	B	C	D	A	B	C	D		
0.5	0.5	0.9	0.9	0.9	0.9	1.6	1.6	1.7	3.0
STDM80									
AO22				*AO22D2*				*AO22*	*AO22D2*
A	B	C	D	A	B	C	D		
1.0	1.0	1.0	1.0	2.1	2.0	2.1	2.1	1.7	3.0

AO22/AO22D2

Two 2-ANDs into 2-NOR with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AO22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.13 + 0.047*SL	0.14 + 0.041*SL	0.14 + 0.041*SL
	t_{PHL}	0.28	0.17 + 0.057*SL	0.17 + 0.054*SL	0.16 + 0.055*SL
	t_R	0.43	0.27 + 0.081*SL	0.26 + 0.088*SL	0.19 + 0.095*SL
	t_F	0.42	0.23 + 0.095*SL	0.21 + 0.105*SL	0.16 + 0.111*SL
B to Y	t_{PLH}	0.24	0.15 + 0.044*SL	0.16 + 0.040*SL	0.15 + 0.041*SL
	t_{PHL}	0.26	0.14 + 0.057*SL	0.15 + 0.054*SL	0.14 + 0.055*SL
	t_R	0.46	0.30 + 0.078*SL	0.28 + 0.088*SL	0.21 + 0.095*SL
	t_F	0.41	0.22 + 0.096*SL	0.20 + 0.106*SL	0.16 + 0.111*SL
C to Y	t_{PLH}	0.26	0.17 + 0.046*SL	0.18 + 0.041*SL	0.18 + 0.041*SL
	t_{PHL}	0.42	0.31 + 0.055*SL	0.31 + 0.055*SL	0.31 + 0.055*SL
	t_R	0.42	0.26 + 0.081*SL	0.24 + 0.090*SL	0.19 + 0.095*SL
	t_F	0.59	0.39 + 0.103*SL	0.38 + 0.107*SL	0.35 + 0.111*SL
D to Y	t_{PLH}	0.28	0.19 + 0.044*SL	0.20 + 0.041*SL	0.19 + 0.041*SL
	t_{PHL}	0.40	0.29 + 0.055*SL	0.29 + 0.055*SL	0.29 + 0.055*SL
	t_R	0.44	0.28 + 0.081*SL	0.26 + 0.090*SL	0.21 + 0.095*SL
	t_F	0.59	0.38 + 0.106*SL	0.38 + 0.108*SL	0.35 + 0.111*SL

STD80 AO22D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.18	0.13 + 0.026*SL	0.14 + 0.022*SL	0.14 + 0.021*SL
	t_{PHL}	0.22	0.16 + 0.030*SL	0.17 + 0.027*SL	0.17 + 0.027*SL
	t_R	0.36	0.28 + 0.039*SL	0.27 + 0.043*SL	0.22 + 0.048*SL
	t_F	0.33	0.23 + 0.047*SL	0.23 + 0.050*SL	0.18 + 0.055*SL
B to Y	t_{PLH}	0.20	0.15 + 0.024*SL	0.16 + 0.021*SL	0.16 + 0.021*SL
	t_{PHL}	0.20	0.14 + 0.029*SL	0.15 + 0.028*SL	0.15 + 0.027*SL
	t_R	0.38	0.31 + 0.039*SL	0.30 + 0.043*SL	0.24 + 0.048*SL
	t_F	0.32	0.22 + 0.046*SL	0.21 + 0.051*SL	0.17 + 0.055*SL
C to Y	t_{PLH}	0.21	0.17 + 0.024*SL	0.17 + 0.022*SL	0.18 + 0.021*SL
	t_{PHL}	0.35	0.30 + 0.028*SL	0.30 + 0.028*SL	0.30 + 0.027*SL
	t_R	0.34	0.26 + 0.040*SL	0.25 + 0.044*SL	0.21 + 0.048*SL
	t_F	0.48	0.37 + 0.051*SL	0.37 + 0.052*SL	0.35 + 0.055*SL
D to Y	t_{PLH}	0.23	0.18 + 0.023*SL	0.19 + 0.022*SL	0.19 + 0.021*SL
	t_{PHL}	0.33	0.27 + 0.029*SL	0.28 + 0.028*SL	0.28 + 0.027*SL
	t_R	0.36	0.28 + 0.041*SL	0.27 + 0.044*SL	0.23 + 0.048*SL
	t_F	0.47	0.37 + 0.051*SL	0.37 + 0.053*SL	0.35 + 0.055*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AO22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.18 + 0.062*SL	0.17 + 0.063*SL	0.17 + 0.063*SL
	t_{PHL}	0.34	0.20 + 0.073*SL	0.20 + 0.072*SL	0.20 + 0.071*SL
	t_R	0.56	0.30 + 0.132*SL	0.29 + 0.136*SL	0.26 + 0.139*SL
	t_F	0.51	0.25 + 0.134*SL	0.23 + 0.140*SL	0.21 + 0.142*SL
B to Y	t_{PLH}	0.32	0.20 + 0.062*SL	0.19 + 0.063*SL	0.19 + 0.063*SL
	t_{PHL}	0.33	0.18 + 0.073*SL	0.19 + 0.072*SL	0.19 + 0.072*SL
	t_R	0.59	0.33 + 0.131*SL	0.32 + 0.136*SL	0.29 + 0.139*SL
	t_F	0.51	0.24 + 0.137*SL	0.23 + 0.140*SL	0.21 + 0.142*SL
C to Y	t_{PLH}	0.51	0.38 + 0.065*SL	0.39 + 0.064*SL	0.39 + 0.063*SL
	t_{PHL}	0.73	0.57 + 0.076*SL	0.58 + 0.073*SL	0.59 + 0.072*SL
	t_R	0.56	0.29 + 0.135*SL	0.29 + 0.137*SL	0.27 + 0.139*SL
	t_F	0.74	0.46 + 0.142*SL	0.46 + 0.142*SL	0.46 + 0.142*SL
D to Y	t_{PLH}	0.53	0.40 + 0.065*SL	0.41 + 0.063*SL	0.41 + 0.063*SL
	t_{PHL}	0.72	0.57 + 0.076*SL	0.58 + 0.073*SL	0.59 + 0.072*SL
	t_R	0.59	0.32 + 0.135*SL	0.31 + 0.138*SL	0.30 + 0.139*SL
	t_F	0.74	0.46 + 0.142*SL	0.46 + 0.142*SL	0.46 + 0.142*SL

STDM80 AO22D2A

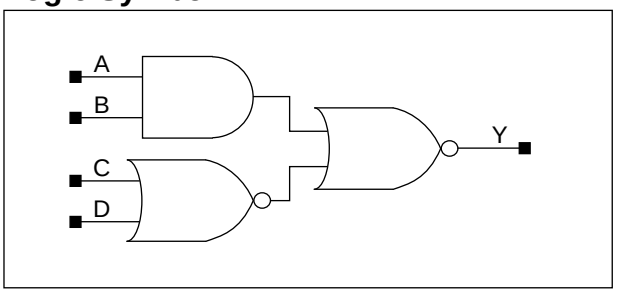
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.17 + 0.032*SL	0.18 + 0.031*SL	0.17 + 0.032*SL
	t_{PHL}	0.27	0.19 + 0.037*SL	0.20 + 0.036*SL	0.20 + 0.036*SL
	t_R	0.43	0.30 + 0.064*SL	0.30 + 0.066*SL	0.28 + 0.068*SL
	t_F	0.38	0.25 + 0.066*SL	0.24 + 0.068*SL	0.23 + 0.070*SL
B to Y	t_{PLH}	0.26	0.20 + 0.031*SL	0.20 + 0.031*SL	0.20 + 0.032*SL
	t_{PHL}	0.26	0.18 + 0.038*SL	0.19 + 0.037*SL	0.19 + 0.036*SL
	t_R	0.46	0.33 + 0.063*SL	0.32 + 0.066*SL	0.31 + 0.068*SL
	t_F	0.37	0.24 + 0.067*SL	0.23 + 0.069*SL	0.23 + 0.070*SL
C to Y	t_{PLH}	0.52	0.46 + 0.033*SL	0.46 + 0.032*SL	0.46 + 0.032*SL
	t_{PHL}	0.71	0.64 + 0.039*SL	0.64 + 0.038*SL	0.65 + 0.037*SL
	t_R	0.46	0.32 + 0.066*SL	0.32 + 0.068*SL	0.31 + 0.069*SL
	t_F	0.59	0.45 + 0.070*SL	0.45 + 0.071*SL	0.45 + 0.071*SL
D to Y	t_{PLH}	0.50	0.44 + 0.033*SL	0.44 + 0.033*SL	0.44 + 0.032*SL
	t_{PHL}	0.72	0.64 + 0.038*SL	0.65 + 0.037*SL	0.65 + 0.037*SL
	t_R	0.43	0.30 + 0.066*SL	0.29 + 0.067*SL	0.28 + 0.069*SL
	t_F	0.59	0.45 + 0.071*SL	0.45 + 0.071*SL	0.45 + 0.070*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

AO22A/AO22D2A

2-AND and 2-NOR into 2-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	0	0	0
Other States				1

Cell Data

Input Load (SL)								Gate Count	
STD80									
AO22A				*AO22D2A*				*AO22A*	*AO22D2A*
A	B	C	D	A	B	C	D		
0.9	0.9	0.6	0.6	1.4	1.8	0.7	0.7	2.7	4.0
STDM80									
AO22A				*AO22D2A*				*AO22A*	*AO22D2A*
A	B	C	D	A	B	C	D		
1.0	1.0	0.7	0.7	2.1	2.0	0.7	0.7	2.7	4.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AO22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.13 + 0.047*SL	0.14 + 0.041*SL	0.14 + 0.041*SL
	t_{PHL}	0.28	0.17 + 0.056*SL	0.17 + 0.054*SL	0.16 + 0.055*SL
	t_R	0.43	0.28 + 0.080*SL	0.26 + 0.088*SL	0.19 + 0.095*SL
	t_F	0.42	0.23 + 0.096*SL	0.21 + 0.105*SL	0.16 + 0.111*SL
B to Y	t_{PLH}	0.24	0.15 + 0.044*SL	0.16 + 0.040*SL	0.15 + 0.041*SL
	t_{PHL}	0.26	0.14 + 0.056*SL	0.15 + 0.054*SL	0.14 + 0.055*SL
	t_R	0.46	0.30 + 0.079*SL	0.28 + 0.088*SL	0.21 + 0.095*SL
	t_F	0.41	0.22 + 0.097*SL	0.20 + 0.106*SL	0.16 + 0.111*SL
C to Y	t_{PLH}	0.35	0.26 + 0.044*SL	0.27 + 0.042*SL	0.27 + 0.042*SL
	t_{PHL}	0.55	0.43 + 0.058*SL	0.44 + 0.056*SL	0.44 + 0.055*SL
	t_R	0.38	0.21 + 0.088*SL	0.20 + 0.093*SL	0.18 + 0.095*SL
	t_F	0.58	0.36 + 0.109*SL	0.36 + 0.110*SL	0.35 + 0.111*SL
D to Y	t_{PLH}	0.36	0.27 + 0.044*SL	0.28 + 0.042*SL	0.28 + 0.041*SL
	t_{PHL}	0.54	0.43 + 0.058*SL	0.43 + 0.056*SL	0.44 + 0.055*SL
	t_R	0.40	0.22 + 0.090*SL	0.22 + 0.093*SL	0.20 + 0.095*SL
	t_F	0.58	0.36 + 0.110*SL	0.36 + 0.110*SL	0.35 + 0.111*SL

STD80 AO22D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.18	0.13 + 0.026*SL	0.14 + 0.022*SL	0.14 + 0.021*SL
	t_{PHL}	0.22	0.16 + 0.031*SL	0.17 + 0.027*SL	0.17 + 0.027*SL
	t_R	0.36	0.28 + 0.039*SL	0.27 + 0.043*SL	0.22 + 0.048*SL
	t_F	0.32	0.23 + 0.047*SL	0.22 + 0.050*SL	0.18 + 0.055*SL
B to Y	t_{PLH}	0.20	0.15 + 0.024*SL	0.16 + 0.021*SL	0.16 + 0.021*SL
	t_{PHL}	0.20	0.14 + 0.029*SL	0.15 + 0.027*SL	0.15 + 0.027*SL
	t_R	0.38	0.31 + 0.039*SL	0.30 + 0.043*SL	0.24 + 0.048*SL
	t_F	0.32	0.22 + 0.047*SL	0.21 + 0.051*SL	0.17 + 0.055*SL
C to Y	t_{PLH}	0.37	0.32 + 0.024*SL	0.33 + 0.021*SL	0.33 + 0.021*SL
	t_{PHL}	0.53	0.47 + 0.029*SL	0.48 + 0.028*SL	0.48 + 0.028*SL
	t_R	0.33	0.23 + 0.047*SL	0.24 + 0.046*SL	0.21 + 0.049*SL
	t_F	0.46	0.35 + 0.055*SL	0.35 + 0.054*SL	0.34 + 0.055*SL
D to Y	t_{PLH}	0.36	0.31 + 0.023*SL	0.32 + 0.022*SL	0.32 + 0.021*SL
	t_{PHL}	0.54	0.48 + 0.029*SL	0.48 + 0.028*SL	0.49 + 0.028*SL
	t_R	0.30	0.21 + 0.044*SL	0.21 + 0.046*SL	0.19 + 0.049*SL
	t_F	0.46	0.35 + 0.055*SL	0.35 + 0.055*SL	0.34 + 0.055*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

AO22A/AO22D2A

2-AND and 2-NOR into 2-NOR with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AO22A

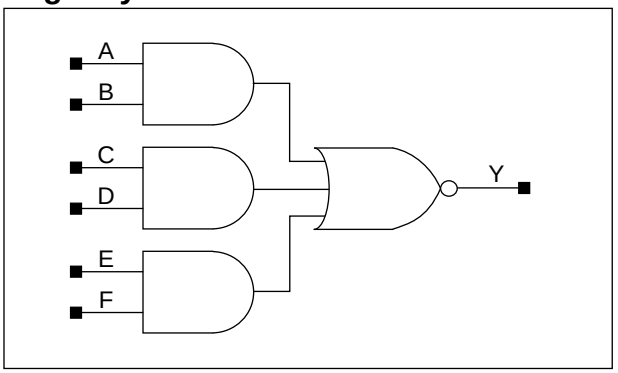
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.18 + 0.062*SL	0.17 + 0.063*SL	0.17 + 0.063*SL
	t_{PHL}	0.34	0.20 + 0.073*SL	0.20 + 0.072*SL	0.20 + 0.071*SL
	t_R	0.56	0.30 + 0.132*SL	0.29 + 0.136*SL	0.26 + 0.139*SL
	t_F	0.51	0.25 + 0.134*SL	0.23 + 0.140*SL	0.21 + 0.142*SL
B to Y	t_{PLH}	0.32	0.20 + 0.062*SL	0.19 + 0.063*SL	0.19 + 0.063*SL
	t_{PHL}	0.33	0.18 + 0.073*SL	0.19 + 0.072*SL	0.19 + 0.072*SL
	t_R	0.59	0.33 + 0.131*SL	0.32 + 0.136*SL	0.29 + 0.139*SL
	t_F	0.51	0.24 + 0.137*SL	0.23 + 0.140*SL	0.21 + 0.142*SL
C to Y	t_{PLH}	0.51	0.38 + 0.065*SL	0.39 + 0.064*SL	0.39 + 0.063*SL
	t_{PHL}	0.73	0.57 + 0.076*SL	0.58 + 0.073*SL	0.59 + 0.072*SL
	t_R	0.56	0.29 + 0.135*SL	0.29 + 0.137*SL	0.27 + 0.139*SL
	t_F	0.74	0.46 + 0.142*SL	0.46 + 0.142*SL	0.46 + 0.142*SL
D to Y	t_{PLH}	0.53	0.40 + 0.065*SL	0.41 + 0.063*SL	0.41 + 0.063*SL
	t_{PHL}	0.72	0.57 + 0.076*SL	0.58 + 0.073*SL	0.59 + 0.072*SL
	t_R	0.59	0.32 + 0.135*SL	0.31 + 0.138*SL	0.30 + 0.139*SL
	t_F	0.74	0.46 + 0.142*SL	0.46 + 0.142*SL	0.46 + 0.142*SL

STDM80 AO22D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.17 + 0.032*SL	0.18 + 0.031*SL	0.17 + 0.032*SL
	t_{PHL}	0.27	0.19 + 0.037*SL	0.20 + 0.036*SL	0.20 + 0.036*SL
	t_R	0.43	0.30 + 0.064*SL	0.30 + 0.066*SL	0.28 + 0.068*SL
	t_F	0.38	0.25 + 0.066*SL	0.24 + 0.068*SL	0.23 + 0.070*SL
B to Y	t_{PLH}	0.26	0.20 + 0.031*SL	0.20 + 0.031*SL	0.20 + 0.032*SL
	t_{PHL}	0.26	0.18 + 0.038*SL	0.19 + 0.037*SL	0.19 + 0.036*SL
	t_R	0.46	0.33 + 0.063*SL	0.32 + 0.066*SL	0.31 + 0.068*SL
	t_F	0.37	0.24 + 0.067*SL	0.23 + 0.069*SL	0.23 + 0.070*SL
C to Y	t_{PLH}	0.52	0.46 + 0.033*SL	0.46 + 0.032*SL	0.46 + 0.032*SL
	t_{PHL}	0.71	0.64 + 0.039*SL	0.64 + 0.038*SL	0.65 + 0.037*SL
	t_R	0.46	0.32 + 0.066*SL	0.32 + 0.068*SL	0.31 + 0.069*SL
	t_F	0.59	0.45 + 0.070*SL	0.45 + 0.071*SL	0.45 + 0.071*SL
D to Y	t_{PLH}	0.50	0.44 + 0.033*SL	0.44 + 0.033*SL	0.44 + 0.032*SL
	t_{PHL}	0.72	0.64 + 0.038*SL	0.65 + 0.037*SL	0.65 + 0.037*SL
	t_R	0.43	0.30 + 0.066*SL	0.29 + 0.067*SL	0.28 + 0.069*SL
	t_F	0.59	0.45 + 0.071*SL	0.45 + 0.071*SL	0.45 + 0.070*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	x	x	x	x	0
x	x	1	1	x	x	0
x	x	x	x	1	1	0
Other States						1

Cell Data

Input Load (SL)												Gate Count	
STD80													
AO222						*AO222D2*						*AO222*	*AO222D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.4	0.5	0.5	0.5	0.8	0.8	0.4	0.4	0.4	0.4	0.6	0.6	2.7	4.0
STDM80													
AO222						*AO222D2*						*AO222*	*AO222D2*
A	B	C	D	E	F	A	B	C	D	E	F		
1.1	1.0	1.0	1.0	1.0	1.0	0.8	0.8	0.7	0.7	0.7	0.7	2.7	4.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AO222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.18 + 0.055*SL	0.18 + 0.058*SL	0.16 + 0.060*SL
	t_{PHL}	0.30	0.19 + 0.055*SL	0.19 + 0.054*SL	0.19 + 0.055*SL
	t_R	0.68	0.42 + 0.129*SL	0.41 + 0.134*SL	0.37 + 0.138*SL
	t_F	0.47	0.28 + 0.098*SL	0.26 + 0.106*SL	0.21 + 0.111*SL
B to Y	t_{PLH}	0.31	0.20 + 0.053*SL	0.19 + 0.058*SL	0.18 + 0.060*SL
	t_{PHL}	0.28	0.17 + 0.056*SL	0.17 + 0.055*SL	0.17 + 0.055*SL
	t_R	0.72	0.46 + 0.128*SL	0.45 + 0.133*SL	0.40 + 0.138*SL
	t_F	0.47	0.27 + 0.100*SL	0.25 + 0.106*SL	0.21 + 0.111*SL
C to Y	t_{PLH}	0.39	0.27 + 0.061*SL	0.27 + 0.060*SL	0.27 + 0.060*SL
	t_{PHL}	0.45	0.33 + 0.056*SL	0.33 + 0.055*SL	0.34 + 0.055*SL
	t_R	0.70	0.45 + 0.128*SL	0.43 + 0.134*SL	0.40 + 0.138*SL
	t_F	0.65	0.44 + 0.104*SL	0.43 + 0.108*SL	0.41 + 0.111*SL
D to Y	t_{PLH}	0.41	0.29 + 0.060*SL	0.29 + 0.060*SL	0.29 + 0.060*SL
	t_{PHL}	0.42	0.31 + 0.056*SL	0.31 + 0.055*SL	0.32 + 0.055*SL
	t_R	0.73	0.47 + 0.129*SL	0.46 + 0.134*SL	0.43 + 0.138*SL
	t_F	0.65	0.44 + 0.105*SL	0.43 + 0.108*SL	0.41 + 0.111*SL
E to Y	t_{PLH}	0.45	0.32 + 0.062*SL	0.32 + 0.060*SL	0.33 + 0.060*SL
	t_{PHL}	0.56	0.44 + 0.060*SL	0.45 + 0.057*SL	0.47 + 0.055*SL
	t_R	0.70	0.44 + 0.130*SL	0.43 + 0.135*SL	0.40 + 0.138*SL
	t_F	0.84	0.62 + 0.107*SL	0.62 + 0.109*SL	0.61 + 0.110*SL
F to Y	t_{PLH}	0.46	0.34 + 0.061*SL	0.34 + 0.060*SL	0.35 + 0.060*SL
	t_{PHL}	0.54	0.42 + 0.060*SL	0.42 + 0.057*SL	0.44 + 0.055*SL
	t_R	0.73	0.47 + 0.130*SL	0.46 + 0.135*SL	0.43 + 0.138*SL
	t_F	0.84	0.62 + 0.109*SL	0.62 + 0.109*SL	0.61 + 0.110*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AO222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.56	0.53 + 0.017*SL	0.54 + 0.013*SL	0.55 + 0.012*SL
	t_{PHL}	0.48	0.44 + 0.022*SL	0.44 + 0.019*SL	0.45 + 0.018*SL
	t_R	0.16	0.13 + 0.018*SL	0.12 + 0.022*SL	0.08 + 0.026*SL
	t_F	0.16	0.09 + 0.031*SL	0.09 + 0.031*SL	0.07 + 0.034*SL
B to Y	t_{PLH}	0.60	0.57 + 0.017*SL	0.57 + 0.013*SL	0.59 + 0.012*SL
	t_{PHL}	0.46	0.42 + 0.021*SL	0.42 + 0.019*SL	0.43 + 0.018*SL
	t_R	0.17	0.12 + 0.021*SL	0.12 + 0.022*SL	0.09 + 0.026*SL
	t_F	0.16	0.10 + 0.029*SL	0.09 + 0.031*SL	0.07 + 0.034*SL
C to Y	t_{PLH}	0.66	0.62 + 0.018*SL	0.63 + 0.013*SL	0.64 + 0.012*SL
	t_{PHL}	0.58	0.54 + 0.022*SL	0.54 + 0.019*SL	0.55 + 0.018*SL
	t_R	0.16	0.13 + 0.019*SL	0.12 + 0.022*SL	0.08 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D to Y	t_{PLH}	0.69	0.66 + 0.017*SL	0.67 + 0.013*SL	0.68 + 0.012*SL
	t_{PHL}	0.56	0.51 + 0.022*SL	0.52 + 0.019*SL	0.53 + 0.018*SL
	t_R	0.17	0.13 + 0.022*SL	0.13 + 0.022*SL	0.09 + 0.026*SL
	t_F	0.16	0.10 + 0.029*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
E to Y	t_{PLH}	0.71	0.68 + 0.017*SL	0.69 + 0.013*SL	0.70 + 0.012*SL
	t_{PHL}	0.65	0.60 + 0.022*SL	0.61 + 0.019*SL	0.62 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.12 + 0.022*SL	0.08 + 0.026*SL
	t_F	0.17	0.11 + 0.029*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
F to Y	t_{PLH}	0.75	0.72 + 0.018*SL	0.73 + 0.013*SL	0.74 + 0.012*SL
	t_{PHL}	0.63	0.58 + 0.022*SL	0.59 + 0.019*SL	0.60 + 0.018*SL
	t_R	0.17	0.13 + 0.022*SL	0.13 + 0.022*SL	0.09 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AO222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.40	0.23 + 0.089*SL	0.21 + 0.094*SL	0.21 + 0.094*SL
	t_{PHL}	0.37	0.22 + 0.074*SL	0.23 + 0.072*SL	0.23 + 0.072*SL
	t_R	0.95	0.54 + 0.205*SL	0.54 + 0.208*SL	0.52 + 0.210*SL
	t_F	0.59	0.32 + 0.136*SL	0.30 + 0.140*SL	0.28 + 0.143*SL
B to Y	t_{PLH}	0.43	0.25 + 0.091*SL	0.24 + 0.093*SL	0.24 + 0.093*SL
	t_{PHL}	0.36	0.21 + 0.073*SL	0.21 + 0.073*SL	0.22 + 0.072*SL
	t_R	1.00	0.59 + 0.205*SL	0.58 + 0.208*SL	0.56 + 0.210*SL
	t_F	0.58	0.31 + 0.137*SL	0.30 + 0.141*SL	0.29 + 0.142*SL
C to Y	t_{PLH}	0.61	0.42 + 0.096*SL	0.42 + 0.094*SL	0.43 + 0.094*SL
	t_{PHL}	0.58	0.43 + 0.075*SL	0.43 + 0.073*SL	0.44 + 0.072*SL
	t_R	1.02	0.62 + 0.200*SL	0.61 + 0.204*SL	0.60 + 0.206*SL
	t_F	0.81	0.53 + 0.140*SL	0.53 + 0.142*SL	0.53 + 0.142*SL
D to Y	t_{PLH}	0.64	0.45 + 0.095*SL	0.46 + 0.094*SL	0.46 + 0.094*SL
	t_{PHL}	0.57	0.42 + 0.075*SL	0.42 + 0.073*SL	0.43 + 0.072*SL
	t_R	1.06	0.66 + 0.201*SL	0.65 + 0.204*SL	0.64 + 0.206*SL
	t_F	0.82	0.53 + 0.141*SL	0.53 + 0.141*SL	0.53 + 0.142*SL
E to Y	t_{PLH}	0.72	0.53 + 0.097*SL	0.53 + 0.095*SL	0.54 + 0.094*SL
	t_{PHL}	0.73	0.57 + 0.081*SL	0.58 + 0.077*SL	0.60 + 0.074*SL
	t_R	1.03	0.63 + 0.199*SL	0.62 + 0.204*SL	0.60 + 0.206*SL
	t_F	1.05	0.76 + 0.145*SL	0.76 + 0.144*SL	0.77 + 0.142*SL
F to Y	t_{PLH}	0.75	0.56 + 0.095*SL	0.57 + 0.094*SL	0.57 + 0.094*SL
	t_{PHL}	0.72	0.56 + 0.081*SL	0.57 + 0.077*SL	0.59 + 0.074*SL
	t_R	1.07	0.67 + 0.200*SL	0.66 + 0.204*SL	0.64 + 0.206*SL
	t_F	1.05	0.76 + 0.144*SL	0.77 + 0.143*SL	0.77 + 0.142*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AO222D2

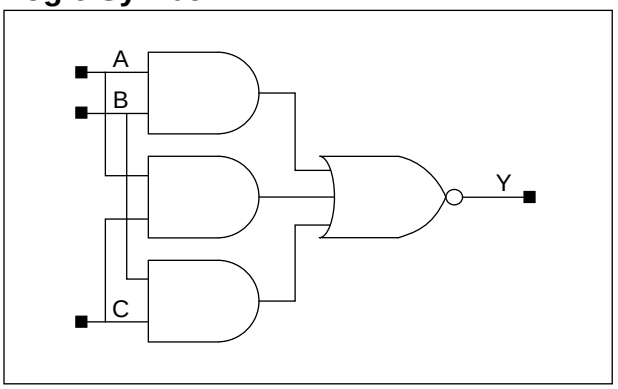
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.80	0.75 + 0.023*SL	0.76 + 0.019*SL	0.78 + 0.017*SL
	t_{PHL}	0.64	0.59 + 0.029*SL	0.60 + 0.024*SL	0.61 + 0.022*SL
	t_R	0.21	0.15 + 0.031*SL	0.15 + 0.032*SL	0.13 + 0.033*SL
	t_F	0.20	0.12 + 0.041*SL	0.13 + 0.037*SL	0.13 + 0.038*SL
B to Y	t_{PLH}	0.86	0.81 + 0.023*SL	0.82 + 0.019*SL	0.84 + 0.017*SL
	t_{PHL}	0.63	0.58 + 0.029*SL	0.59 + 0.024*SL	0.60 + 0.022*SL
	t_R	0.21	0.15 + 0.030*SL	0.15 + 0.032*SL	0.14 + 0.033*SL
	t_F	0.20	0.12 + 0.039*SL	0.12 + 0.038*SL	0.12 + 0.039*SL
C to Y	t_{PLH}	1.01	0.97 + 0.023*SL	0.98 + 0.019*SL	0.99 + 0.017*SL
	t_{PHL}	0.78	0.72 + 0.028*SL	0.73 + 0.024*SL	0.75 + 0.022*SL
	t_R	0.21	0.15 + 0.032*SL	0.15 + 0.032*SL	0.14 + 0.033*SL
	t_F	0.20	0.12 + 0.039*SL	0.13 + 0.038*SL	0.12 + 0.038*SL
D to Y	t_{PLH}	1.08	1.03 + 0.023*SL	1.04 + 0.019*SL	1.06 + 0.017*SL
	t_{PHL}	0.77	0.71 + 0.029*SL	0.72 + 0.024*SL	0.74 + 0.022*SL
	t_R	0.21	0.15 + 0.031*SL	0.15 + 0.031*SL	0.14 + 0.033*SL
	t_F	0.20	0.12 + 0.039*SL	0.13 + 0.038*SL	0.12 + 0.038*SL
E to Y	t_{PLH}	1.13	1.09 + 0.023*SL	1.10 + 0.019*SL	1.11 + 0.017*SL
	t_{PHL}	0.86	0.80 + 0.029*SL	0.82 + 0.024*SL	0.83 + 0.022*SL
	t_R	0.21	0.15 + 0.031*SL	0.15 + 0.032*SL	0.14 + 0.033*SL
	t_F	0.21	0.13 + 0.038*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
F to Y	t_{PLH}	1.19	1.15 + 0.023*SL	1.16 + 0.019*SL	1.17 + 0.017*SL
	t_{PHL}	0.85	0.79 + 0.029*SL	0.81 + 0.024*SL	0.82 + 0.022*SL
	t_R	0.21	0.15 + 0.031*SL	0.15 + 0.031*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

AO222A/AO222D2A

Inverting 2-of-3 Majority with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
1	1	x	0
1	x	1	0
x	1	1	0
0	0	x	1
0	x	0	1
x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
STD80							
AO222A			*AO222D2A*			*AO222A*	*AO222D2A*
A	B	C	A	B	C		
0.9	1.2	1.6	1.7	2.5	3.2	2.7	5.0
STDM80							
AO222A			*AO222D2A*			*AO222A*	*AO222D2A*
A	B	C	A	B	C		
2.2	2.2	2.1	4.5	4.4	4.2	2.7	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AO222A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.24 + 0.053*SL	0.24 + 0.051*SL	0.25 + 0.050*SL
	t_{PHL}	0.45	0.33 + 0.059*SL	0.34 + 0.057*SL	0.35 + 0.055*SL
	t_R	0.64	0.42 + 0.107*SL	0.41 + 0.112*SL	0.38 + 0.116*SL
	t_F	0.60	0.39 + 0.105*SL	0.39 + 0.108*SL	0.37 + 0.111*SL
B to Y	t_{PLH}	0.39	0.28 + 0.055*SL	0.28 + 0.051*SL	0.29 + 0.050*SL
	t_{PHL}	0.52	0.39 + 0.065*SL	0.40 + 0.060*SL	0.44 + 0.055*SL
	t_R	0.63	0.42 + 0.106*SL	0.41 + 0.113*SL	0.38 + 0.116*SL
	t_F	0.76	0.54 + 0.108*SL	0.54 + 0.109*SL	0.53 + 0.110*SL
C to Y	t_{PLH}	0.41	0.30 + 0.054*SL	0.31 + 0.051*SL	0.31 + 0.050*SL
	t_{PHL}	0.49	0.36 + 0.065*SL	0.37 + 0.059*SL	0.41 + 0.055*SL
	t_R	0.59	0.38 + 0.103*SL	0.36 + 0.111*SL	0.32 + 0.116*SL
	t_F	0.78	0.57 + 0.107*SL	0.57 + 0.108*SL	0.54 + 0.110*SL

STD80 AO222D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.31	0.25 + 0.029*SL	0.25 + 0.027*SL	0.26 + 0.026*SL
	t_{PHL}	0.39	0.33 + 0.030*SL	0.34 + 0.029*SL	0.35 + 0.028*SL
	t_R	0.54	0.44 + 0.052*SL	0.43 + 0.056*SL	0.40 + 0.059*SL
	t_F	0.51	0.40 + 0.052*SL	0.40 + 0.053*SL	0.38 + 0.055*SL
B to Y	t_{PLH}	0.34	0.28 + 0.029*SL	0.28 + 0.027*SL	0.29 + 0.026*SL
	t_{PHL}	0.45	0.38 + 0.034*SL	0.38 + 0.031*SL	0.42 + 0.028*SL
	t_R	0.54	0.43 + 0.053*SL	0.43 + 0.056*SL	0.40 + 0.059*SL
	t_F	0.64	0.53 + 0.055*SL	0.53 + 0.055*SL	0.52 + 0.055*SL
C to Y	t_{PLH}	0.36	0.30 + 0.029*SL	0.31 + 0.027*SL	0.31 + 0.026*SL
	t_{PHL}	0.42	0.35 + 0.034*SL	0.36 + 0.031*SL	0.39 + 0.028*SL
	t_R	0.49	0.39 + 0.051*SL	0.38 + 0.056*SL	0.34 + 0.059*SL
	t_F	0.66	0.56 + 0.053*SL	0.56 + 0.054*SL	0.54 + 0.055*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STM80 AO222A

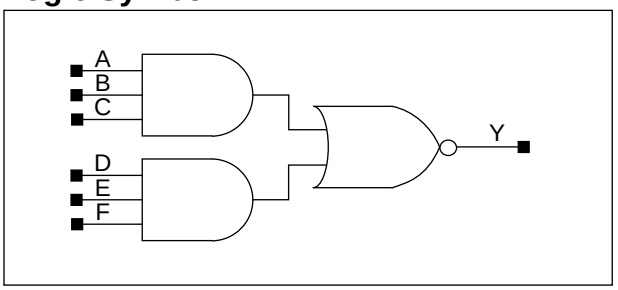
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.52	0.35 + 0.085*SL	0.36 + 0.082*SL	0.37 + 0.080*SL
	t_{PHL}	0.58	0.42 + 0.079*SL	0.43 + 0.075*SL	0.45 + 0.073*SL
	t_R	0.92	0.58 + 0.170*SL	0.58 + 0.172*SL	0.57 + 0.173*SL
	t_F	0.77	0.49 + 0.141*SL	0.49 + 0.142*SL	0.49 + 0.142*SL
B to Y	t_{PLH}	0.61	0.44 + 0.083*SL	0.45 + 0.081*SL	0.46 + 0.080*SL
	t_{PHL}	0.67	0.50 + 0.087*SL	0.52 + 0.080*SL	0.54 + 0.076*SL
	t_R	0.94	0.60 + 0.166*SL	0.59 + 0.171*SL	0.58 + 0.172*SL
	t_F	0.97	0.68 + 0.144*SL	0.69 + 0.143*SL	0.69 + 0.142*SL
C to Y	t_{PLH}	0.64	0.47 + 0.082*SL	0.48 + 0.079*SL	0.49 + 0.078*SL
	t_{PHL}	0.65	0.48 + 0.087*SL	0.50 + 0.080*SL	0.53 + 0.076*SL
	t_R	0.85	0.52 + 0.164*SL	0.50 + 0.169*SL	0.49 + 0.171*SL
	t_F	0.99	0.71 + 0.141*SL	0.70 + 0.142*SL	0.71 + 0.141*SL

STDM80 AO222D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.44	0.36 + 0.044*SL	0.36 + 0.042*SL	0.37 + 0.041*SL
	t_{PHL}	0.51	0.43 + 0.041*SL	0.43 + 0.039*SL	0.44 + 0.038*SL
	t_R	0.76	0.59 + 0.084*SL	0.59 + 0.085*SL	0.58 + 0.086*SL
	t_F	0.64	0.50 + 0.071*SL	0.50 + 0.071*SL	0.50 + 0.071*SL
B to Y	t_{PLH}	0.52	0.44 + 0.043*SL	0.44 + 0.041*SL	0.45 + 0.040*SL
	t_{PHL}	0.58	0.49 + 0.045*SL	0.50 + 0.042*SL	0.52 + 0.040*SL
	t_R	0.77	0.61 + 0.082*SL	0.60 + 0.084*SL	0.59 + 0.085*SL
	t_F	0.81	0.67 + 0.072*SL	0.67 + 0.072*SL	0.67 + 0.072*SL
C to Y	t_{PLH}	0.55	0.47 + 0.042*SL	0.47 + 0.041*SL	0.48 + 0.039*SL
	t_{PHL}	0.56	0.47 + 0.045*SL	0.48 + 0.042*SL	0.50 + 0.039*SL
	t_R	0.68	0.52 + 0.080*SL	0.51 + 0.083*SL	0.50 + 0.085*SL
	t_F	0.83	0.69 + 0.071*SL	0.69 + 0.071*SL	0.69 + 0.071*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	1	0
Other States						1

Cell Data

Input Load (SL)												Gate Count	
STD80													
AO33						*AO33D2*						*AO33*	*AO33D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.5	0.6	0.6	1.0	1.0	1.0	0.4	0.4	0.4	0.6	0.6	0.6	2.3	3.7
STDM80													
AO33						*AO33D2*						*AO33*	*AO33D2*
A	B	C	D	E	F	A	B	C	D	E	F		
1.0	1.1	1.0	1.0	1.0	1.0	0.8	0.8	0.8	0.7	0.7	0.7	2.3	3.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AO33

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.17 + 0.044*SL	0.17 + 0.041*SL	0.17 + 0.041*SL
	t_{PHL}	0.40	0.25 + 0.073*SL	0.25 + 0.073*SL	0.25 + 0.073*SL
	t_R	0.51	0.35 + 0.082*SL	0.33 + 0.089*SL	0.27 + 0.095*SL
	t_F	0.68	0.39 + 0.143*SL	0.38 + 0.149*SL	0.35 + 0.152*SL
B to Y	t_{PLH}	0.27	0.19 + 0.043*SL	0.19 + 0.041*SL	0.19 + 0.041*SL
	t_{PHL}	0.39	0.25 + 0.074*SL	0.25 + 0.073*SL	0.25 + 0.073*SL
	t_R	0.53	0.37 + 0.081*SL	0.35 + 0.089*SL	0.29 + 0.095*SL
	t_F	0.68	0.39 + 0.144*SL	0.38 + 0.149*SL	0.35 + 0.152*SL
C to Y	t_{PLH}	0.28	0.20 + 0.042*SL	0.20 + 0.041*SL	0.19 + 0.041*SL
	t_{PHL}	0.38	0.23 + 0.074*SL	0.23 + 0.073*SL	0.23 + 0.073*SL
	t_R	0.56	0.40 + 0.081*SL	0.38 + 0.088*SL	0.32 + 0.095*SL
	t_F	0.68	0.39 + 0.143*SL	0.38 + 0.150*SL	0.35 + 0.152*SL
D to Y	t_{PLH}	0.31	0.22 + 0.044*SL	0.22 + 0.042*SL	0.22 + 0.041*SL
	t_{PHL}	0.64	0.49 + 0.073*SL	0.49 + 0.073*SL	0.50 + 0.073*SL
	t_R	0.49	0.33 + 0.084*SL	0.31 + 0.091*SL	0.27 + 0.095*SL
	t_F	0.96	0.66 + 0.151*SL	0.65 + 0.151*SL	0.65 + 0.152*SL
E to Y	t_{PLH}	0.32	0.23 + 0.043*SL	0.24 + 0.041*SL	0.24 + 0.041*SL
	t_{PHL}	0.63	0.49 + 0.074*SL	0.49 + 0.073*SL	0.49 + 0.073*SL
	t_R	0.52	0.35 + 0.084*SL	0.33 + 0.091*SL	0.29 + 0.095*SL
	t_F	0.96	0.66 + 0.149*SL	0.66 + 0.151*SL	0.65 + 0.152*SL
F to Y	t_{PLH}	0.33	0.25 + 0.043*SL	0.25 + 0.041*SL	0.25 + 0.041*SL
	t_{PHL}	0.62	0.47 + 0.074*SL	0.47 + 0.073*SL	0.48 + 0.073*SL
	t_R	0.54	0.37 + 0.085*SL	0.36 + 0.090*SL	0.32 + 0.095*SL
	t_F	0.96	0.66 + 0.152*SL	0.66 + 0.151*SL	0.65 + 0.152*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AO33D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.50	0.46 + 0.017*SL	0.47 + 0.013*SL	0.48 + 0.012*SL
	t_{PHL}	0.56	0.52 + 0.022*SL	0.52 + 0.019*SL	0.53 + 0.018*SL
	t_R	0.15	0.10 + 0.024*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
B to Y	t_{PLH}	0.53	0.49 + 0.017*SL	0.50 + 0.013*SL	0.51 + 0.012*SL
	t_{PHL}	0.56	0.51 + 0.022*SL	0.52 + 0.019*SL	0.53 + 0.018*SL
	t_R	0.15	0.11 + 0.024*SL	0.11 + 0.022*SL	0.08 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
C to Y	t_{PLH}	0.55	0.52 + 0.016*SL	0.52 + 0.013*SL	0.53 + 0.012*SL
	t_{PHL}	0.54	0.50 + 0.022*SL	0.50 + 0.019*SL	0.51 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D to Y	t_{PLH}	0.55	0.51 + 0.017*SL	0.52 + 0.013*SL	0.53 + 0.012*SL
	t_{PHL}	0.72	0.67 + 0.023*SL	0.68 + 0.019*SL	0.69 + 0.018*SL
	t_R	0.15	0.11 + 0.024*SL	0.11 + 0.022*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.10 + 0.031*SL	0.08 + 0.034*SL
E to Y	t_{PLH}	0.57	0.54 + 0.017*SL	0.55 + 0.013*SL	0.56 + 0.012*SL
	t_{PHL}	0.71	0.67 + 0.022*SL	0.67 + 0.019*SL	0.68 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.17	0.11 + 0.029*SL	0.11 + 0.030*SL	0.07 + 0.034*SL
F to Y	t_{PLH}	0.60	0.56 + 0.017*SL	0.57 + 0.013*SL	0.58 + 0.012*SL
	t_{PHL}	0.70	0.65 + 0.022*SL	0.66 + 0.019*SL	0.67 + 0.018*SL
	t_R	0.15	0.12 + 0.019*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.17	0.11 + 0.029*SL	0.11 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AO33

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.36	0.23 + 0.063*SL	0.23 + 0.063*SL	0.23 + 0.063*SL
	t_{PHL}	0.51	0.31 + 0.101*SL	0.32 + 0.100*SL	0.32 + 0.099*SL
	t_R	0.69	0.42 + 0.133*SL	0.41 + 0.137*SL	0.39 + 0.140*SL
	t_F	0.91	0.51 + 0.197*SL	0.50 + 0.201*SL	0.50 + 0.201*SL
B to Y	t_{PLH}	0.38	0.25 + 0.064*SL	0.25 + 0.064*SL	0.26 + 0.063*SL
	t_{PHL}	0.53	0.32 + 0.102*SL	0.33 + 0.100*SL	0.34 + 0.099*SL
	t_R	0.71	0.45 + 0.133*SL	0.43 + 0.137*SL	0.42 + 0.140*SL
	t_F	0.91	0.52 + 0.196*SL	0.51 + 0.201*SL	0.50 + 0.201*SL
C to Y	t_{PLH}	0.39	0.27 + 0.064*SL	0.27 + 0.063*SL	0.27 + 0.063*SL
	t_{PHL}	0.52	0.32 + 0.102*SL	0.32 + 0.101*SL	0.33 + 0.099*SL
	t_R	0.74	0.48 + 0.133*SL	0.47 + 0.137*SL	0.45 + 0.139*SL
	t_F	0.91	0.51 + 0.198*SL	0.51 + 0.201*SL	0.50 + 0.201*SL
D to Y	t_{PLH}	0.47	0.34 + 0.065*SL	0.34 + 0.064*SL	0.35 + 0.063*SL
	t_{PHL}	0.88	0.68 + 0.101*SL	0.68 + 0.100*SL	0.69 + 0.099*SL
	t_R	0.70	0.43 + 0.132*SL	0.42 + 0.137*SL	0.41 + 0.139*SL
	t_F	1.26	0.86 + 0.202*SL	0.86 + 0.201*SL	0.86 + 0.201*SL
E to Y	t_{PLH}	0.49	0.36 + 0.064*SL	0.37 + 0.064*SL	0.37 + 0.063*SL
	t_{PHL}	0.89	0.69 + 0.101*SL	0.69 + 0.100*SL	0.70 + 0.099*SL
	t_R	0.72	0.46 + 0.133*SL	0.44 + 0.137*SL	0.43 + 0.139*SL
	t_F	1.26	0.86 + 0.202*SL	0.86 + 0.201*SL	0.86 + 0.201*SL
F to Y	t_{PLH}	0.51	0.38 + 0.065*SL	0.39 + 0.064*SL	0.39 + 0.063*SL
	t_{PHL}	0.89	0.69 + 0.101*SL	0.69 + 0.100*SL	0.70 + 0.099*SL
	t_R	0.75	0.49 + 0.133*SL	0.47 + 0.137*SL	0.46 + 0.139*SL
	t_F	1.26	0.86 + 0.201*SL	0.86 + 0.201*SL	0.86 + 0.201*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AO33D2

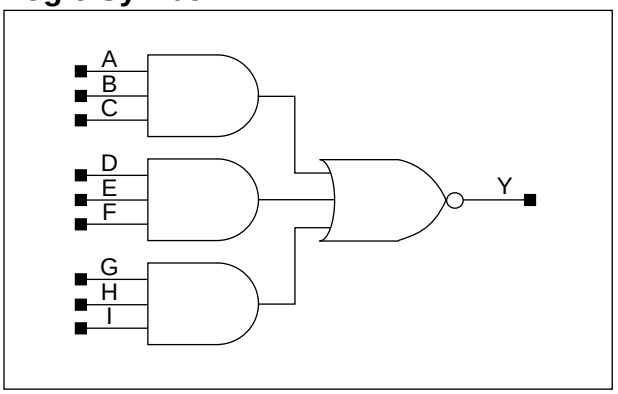
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.70	0.66 + 0.022*SL	0.67 + 0.019*SL	0.68 + 0.017*SL
	t_{PHL}	0.76	0.70 + 0.029*SL	0.72 + 0.024*SL	0.73 + 0.022*SL
	t_R	0.20	0.14 + 0.030*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.21	0.13 + 0.039*SL	0.14 + 0.037*SL	0.13 + 0.038*SL
B to Y	t_{PLH}	0.75	0.70 + 0.022*SL	0.71 + 0.019*SL	0.73 + 0.017*SL
	t_{PHL}	0.77	0.71 + 0.029*SL	0.73 + 0.024*SL	0.74 + 0.022*SL
	t_R	0.20	0.14 + 0.031*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.21	0.13 + 0.038*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
C to Y	t_{PLH}	0.78	0.74 + 0.022*SL	0.75 + 0.019*SL	0.76 + 0.017*SL
	t_{PHL}	0.77	0.71 + 0.029*SL	0.72 + 0.025*SL	0.74 + 0.022*SL
	t_R	0.20	0.14 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.21	0.13 + 0.038*SL	0.13 + 0.039*SL	0.14 + 0.038*SL
D to Y	t_{PLH}	0.82	0.78 + 0.022*SL	0.79 + 0.019*SL	0.80 + 0.017*SL
	t_{PHL}	0.98	0.92 + 0.029*SL	0.94 + 0.024*SL	0.95 + 0.022*SL
	t_R	0.20	0.14 + 0.030*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.21	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
E to Y	t_{PLH}	0.86	0.82 + 0.023*SL	0.83 + 0.019*SL	0.84 + 0.017*SL
	t_{PHL}	0.99	0.93 + 0.029*SL	0.94 + 0.024*SL	0.96 + 0.022*SL
	t_R	0.20	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.21	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
F to Y	t_{PLH}	0.90	0.86 + 0.022*SL	0.87 + 0.019*SL	0.88 + 0.017*SL
	t_{PHL}	0.99	0.93 + 0.029*SL	0.94 + 0.024*SL	0.96 + 0.022*SL
	t_R	0.20	0.14 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

AO333/AO333D2

Three 3-ANDs into 3-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Y
1	1	1	x	x	x	x	x	x	0
x	x	x	1	1	1	x	x	x	0
x	x	x	x	x	x	1	1	1	0
Other States									1

Cell Data

Input Load (SL)									Gate Count
STD80									
AO333									*AO333*
A	B	C	D	E	F	G	H	I	
0.5	0.5	0.5	0.9	0.9	0.9	0.7	0.7	0.8	3.3
AO333D2									*AO333D2*
A	B	C	D	E	F	G	H	I	
0.4	0.4	0.4	0.6	0.6	0.6	0.4	0.5	0.6	4.7
STDM80									
AO333									*AO333*
A	B	C	D	E	F	G	H	I	
1.1	1.0	1.0	1.0	1.0	1.0	0.9	0.8	0.9	3.3
AO333D2									*AO333D2*
A	B	C	D	E	F	G	H	I	
0.5	0.5	0.5	0.7	0.7	0.7	0.5	0.6	0.7	4.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AO333

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.24 + 0.055*SL	0.23 + 0.059*SL	0.23 + 0.060*SL
	t_{PHL}	0.43	0.29 + 0.074*SL	0.29 + 0.073*SL	0.29 + 0.073*SL
	t_R	0.82	0.56 + 0.129*SL	0.55 + 0.135*SL	0.52 + 0.138*SL
	t_F	0.80	0.51 + 0.143*SL	0.50 + 0.149*SL	0.47 + 0.152*SL
B to Y	t_{PLH}	0.37	0.25 + 0.056*SL	0.25 + 0.059*SL	0.24 + 0.060*SL
	t_{PHL}	0.43	0.28 + 0.075*SL	0.28 + 0.073*SL	0.28 + 0.073*SL
	t_R	0.86	0.59 + 0.130*SL	0.59 + 0.135*SL	0.55 + 0.138*SL
	t_F	0.80	0.51 + 0.143*SL	0.50 + 0.150*SL	0.47 + 0.152*SL
C to Y	t_{PLH}	0.38	0.27 + 0.056*SL	0.26 + 0.059*SL	0.26 + 0.060*SL
	t_{PHL}	0.41	0.26 + 0.075*SL	0.27 + 0.073*SL	0.27 + 0.073*SL
	t_R	0.89	0.64 + 0.127*SL	0.62 + 0.134*SL	0.58 + 0.138*SL
	t_F	0.79	0.51 + 0.143*SL	0.49 + 0.150*SL	0.47 + 0.152*SL
D to Y	t_{PLH}	0.47	0.34 + 0.061*SL	0.35 + 0.060*SL	0.35 + 0.060*SL
	t_{PHL}	0.61	0.46 + 0.075*SL	0.46 + 0.074*SL	0.47 + 0.073*SL
	t_R	0.85	0.59 + 0.131*SL	0.58 + 0.135*SL	0.55 + 0.138*SL
	t_F	1.08	0.79 + 0.145*SL	0.78 + 0.150*SL	0.75 + 0.152*SL
E to Y	t_{PLH}	0.49	0.37 + 0.060*SL	0.37 + 0.060*SL	0.37 + 0.060*SL
	t_{PHL}	0.60	0.45 + 0.076*SL	0.46 + 0.074*SL	0.47 + 0.073*SL
	t_R	0.88	0.62 + 0.130*SL	0.61 + 0.135*SL	0.58 + 0.138*SL
	t_F	1.08	0.79 + 0.145*SL	0.78 + 0.149*SL	0.75 + 0.152*SL
F to Y	t_{PLH}	0.50	0.38 + 0.061*SL	0.38 + 0.060*SL	0.39 + 0.060*SL
	t_{PHL}	0.59	0.44 + 0.076*SL	0.44 + 0.074*SL	0.45 + 0.073*SL
	t_R	0.91	0.65 + 0.130*SL	0.64 + 0.135*SL	0.61 + 0.138*SL
	t_F	1.08	0.79 + 0.145*SL	0.78 + 0.149*SL	0.75 + 0.152*SL
G to Y	t_{PLH}	0.54	0.41 + 0.062*SL	0.41 + 0.061*SL	0.42 + 0.060*SL
	t_{PHL}	0.75	0.59 + 0.079*SL	0.60 + 0.076*SL	0.63 + 0.073*SL
	t_R	0.85	0.59 + 0.130*SL	0.57 + 0.135*SL	0.55 + 0.138*SL
	t_F	1.37	1.08 + 0.145*SL	1.07 + 0.150*SL	1.05 + 0.152*SL
H to Y	t_{PLH}	0.56	0.43 + 0.062*SL	0.43 + 0.060*SL	0.44 + 0.060*SL
	t_{PHL}	0.74	0.58 + 0.080*SL	0.59 + 0.076*SL	0.62 + 0.073*SL
	t_R	0.87	0.61 + 0.131*SL	0.60 + 0.135*SL	0.58 + 0.138*SL
	t_F	1.37	1.08 + 0.148*SL	1.07 + 0.149*SL	1.05 + 0.152*SL
I to Y	t_{PLH}	0.57	0.45 + 0.062*SL	0.45 + 0.060*SL	0.46 + 0.060*SL
	t_{PHL}	0.73	0.57 + 0.080*SL	0.58 + 0.076*SL	0.61 + 0.073*SL
	t_R	0.91	0.64 + 0.131*SL	0.63 + 0.135*SL	0.61 + 0.138*SL
	t_F	1.37	1.08 + 0.149*SL	1.07 + 0.150*SL	1.05 + 0.152*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 AO333D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.66	0.63 + 0.017*SL	0.64 + 0.013*SL	0.65 + 0.012*SL
	t_{PHL}	0.62	0.58 + 0.022*SL	0.59 + 0.019*SL	0.59 + 0.018*SL
	t_R	0.18	0.14 + 0.019*SL	0.13 + 0.022*SL	0.09 + 0.026*SL
	t_F	0.17	0.12 + 0.027*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
B to Y	t_{PLH}	0.70	0.66 + 0.018*SL	0.67 + 0.013*SL	0.69 + 0.012*SL
	t_{PHL}	0.62	0.57 + 0.022*SL	0.58 + 0.019*SL	0.59 + 0.018*SL
	t_R	0.18	0.14 + 0.019*SL	0.14 + 0.022*SL	0.10 + 0.026*SL
	t_F	0.17	0.12 + 0.027*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
C to Y	t_{PLH}	0.73	0.69 + 0.018*SL	0.70 + 0.014*SL	0.72 + 0.012*SL
	t_{PHL}	0.60	0.56 + 0.022*SL	0.56 + 0.019*SL	0.57 + 0.018*SL
	t_R	0.18	0.14 + 0.019*SL	0.14 + 0.022*SL	0.10 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
D to Y	t_{PLH}	0.78	0.74 + 0.018*SL	0.75 + 0.013*SL	0.77 + 0.012*SL
	t_{PHL}	0.75	0.71 + 0.022*SL	0.72 + 0.019*SL	0.72 + 0.018*SL
	t_R	0.18	0.14 + 0.020*SL	0.13 + 0.022*SL	0.09 + 0.026*SL
	t_F	0.18	0.12 + 0.029*SL	0.12 + 0.030*SL	0.08 + 0.034*SL
E to Y	t_{PLH}	0.81	0.78 + 0.018*SL	0.79 + 0.013*SL	0.80 + 0.012*SL
	t_{PHL}	0.75	0.70 + 0.022*SL	0.71 + 0.019*SL	0.72 + 0.018*SL
	t_R	0.18	0.14 + 0.019*SL	0.14 + 0.022*SL	0.10 + 0.026*SL
	t_F	0.18	0.12 + 0.029*SL	0.12 + 0.030*SL	0.08 + 0.034*SL
F to Y	t_{PLH}	0.85	0.81 + 0.018*SL	0.82 + 0.014*SL	0.84 + 0.012*SL
	t_{PHL}	0.73	0.69 + 0.023*SL	0.70 + 0.019*SL	0.70 + 0.018*SL
	t_R	0.18	0.14 + 0.021*SL	0.14 + 0.022*SL	0.10 + 0.026*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.030*SL	0.08 + 0.034*SL
G to Y	t_{PLH}	0.85	0.81 + 0.018*SL	0.82 + 0.013*SL	0.84 + 0.012*SL
	t_{PHL}	0.85	0.80 + 0.023*SL	0.81 + 0.019*SL	0.82 + 0.018*SL
	t_R	0.18	0.14 + 0.019*SL	0.13 + 0.022*SL	0.09 + 0.026*SL
	t_F	0.19	0.12 + 0.031*SL	0.13 + 0.030*SL	0.09 + 0.034*SL
H to Y	t_{PLH}	0.88	0.85 + 0.018*SL	0.86 + 0.013*SL	0.87 + 0.012*SL
	t_{PHL}	0.84	0.80 + 0.023*SL	0.80 + 0.019*SL	0.81 + 0.018*SL
	t_R	0.18	0.14 + 0.018*SL	0.14 + 0.022*SL	0.10 + 0.026*SL
	t_F	0.19	0.13 + 0.030*SL	0.13 + 0.030*SL	0.09 + 0.034*SL
I to Y	t_{PLH}	0.92	0.88 + 0.018*SL	0.89 + 0.014*SL	0.91 + 0.012*SL
	t_{PHL}	0.83	0.78 + 0.023*SL	0.79 + 0.019*SL	0.80 + 0.018*SL
	t_R	0.18	0.14 + 0.019*SL	0.14 + 0.022*SL	0.10 + 0.026*SL
	t_F	0.18	0.13 + 0.027*SL	0.12 + 0.030*SL	0.09 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AO333

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.51	0.33 + 0.094*SL	0.32 + 0.094*SL	0.33 + 0.094*SL
	t_{PHL}	0.55	0.35 + 0.103*SL	0.35 + 0.101*SL	0.36 + 0.099*SL
	t_R	1.18	0.77 + 0.206*SL	0.76 + 0.209*SL	0.75 + 0.210*SL
	t_F	1.07	0.68 + 0.197*SL	0.66 + 0.201*SL	0.66 + 0.201*SL
B to Y	t_{PLH}	0.54	0.35 + 0.094*SL	0.35 + 0.094*SL	0.36 + 0.094*SL
	t_{PHL}	0.56	0.35 + 0.103*SL	0.36 + 0.102*SL	0.37 + 0.099*SL
	t_R	1.22	0.81 + 0.206*SL	0.80 + 0.209*SL	0.79 + 0.210*SL
	t_F	1.07	0.68 + 0.197*SL	0.67 + 0.201*SL	0.66 + 0.201*SL
C to Y	t_{PLH}	0.57	0.38 + 0.094*SL	0.38 + 0.094*SL	0.38 + 0.094*SL
	t_{PHL}	0.56	0.35 + 0.103*SL	0.35 + 0.102*SL	0.37 + 0.100*SL
	t_R	1.27	0.85 + 0.205*SL	0.84 + 0.209*SL	0.83 + 0.210*SL
	t_F	1.07	0.67 + 0.198*SL	0.67 + 0.201*SL	0.66 + 0.201*SL
D to Y	t_{PLH}	0.75	0.55 + 0.096*SL	0.56 + 0.095*SL	0.56 + 0.094*SL
	t_{PHL}	0.82	0.61 + 0.105*SL	0.61 + 0.102*SL	0.63 + 0.100*SL
	t_R	1.26	0.85 + 0.201*SL	0.85 + 0.204*SL	0.84 + 0.206*SL
	t_F	1.43	1.03 + 0.199*SL	1.03 + 0.200*SL	1.03 + 0.200*SL
E to Y	t_{PLH}	0.78	0.59 + 0.096*SL	0.59 + 0.094*SL	0.60 + 0.094*SL
	t_{PHL}	0.83	0.61 + 0.105*SL	0.63 + 0.102*SL	0.64 + 0.100*SL
	t_R	1.30	0.89 + 0.202*SL	0.89 + 0.204*SL	0.87 + 0.206*SL
	t_F	1.43	1.04 + 0.198*SL	1.03 + 0.200*SL	1.02 + 0.201*SL
F to Y	t_{PLH}	0.81	0.62 + 0.095*SL	0.62 + 0.095*SL	0.63 + 0.094*SL
	t_{PHL}	0.82	0.61 + 0.105*SL	0.62 + 0.102*SL	0.64 + 0.100*SL
	t_R	1.34	0.93 + 0.202*SL	0.93 + 0.204*SL	0.92 + 0.206*SL
	t_F	1.43	1.04 + 0.198*SL	1.03 + 0.200*SL	1.03 + 0.200*SL
G to Y	t_{PLH}	0.87	0.68 + 0.096*SL	0.68 + 0.095*SL	0.69 + 0.094*SL
	t_{PHL}	1.01	0.78 + 0.111*SL	0.80 + 0.106*SL	0.82 + 0.102*SL
	t_R	1.26	0.86 + 0.200*SL	0.85 + 0.204*SL	0.84 + 0.205*SL
	t_F	1.81	1.41 + 0.201*SL	1.41 + 0.200*SL	1.41 + 0.200*SL
H to Y	t_{PLH}	0.90	0.71 + 0.095*SL	0.72 + 0.094*SL	0.72 + 0.094*SL
	t_{PHL}	1.02	0.79 + 0.111*SL	0.81 + 0.106*SL	0.83 + 0.102*SL
	t_R	1.30	0.90 + 0.201*SL	0.89 + 0.204*SL	0.88 + 0.206*SL
	t_F	1.81	1.41 + 0.199*SL	1.41 + 0.200*SL	1.41 + 0.200*SL
I to Y	t_{PLH}	0.93	0.74 + 0.096*SL	0.75 + 0.094*SL	0.75 + 0.094*SL
	t_{PHL}	1.01	0.79 + 0.111*SL	0.81 + 0.106*SL	0.83 + 0.102*SL
	t_R	1.34	0.94 + 0.201*SL	0.93 + 0.204*SL	0.92 + 0.206*SL
	t_F	1.81	1.42 + 0.199*SL	1.42 + 0.199*SL	1.41 + 0.200*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

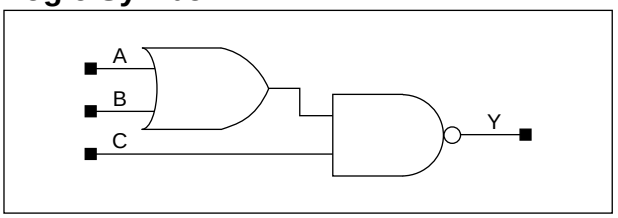
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 AO333D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.99	0.94 + 0.024*SL	0.95 + 0.019*SL	0.97 + 0.017*SL
	t_{PHL}	0.84	0.78 + 0.030*SL	0.80 + 0.025*SL	0.81 + 0.022*SL
	t_R	0.22	0.16 + 0.031*SL	0.16 + 0.032*SL	0.15 + 0.033*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
B to Y	t_{PLH}	1.05	1.00 + 0.024*SL	1.01 + 0.019*SL	1.03 + 0.017*SL
	t_{PHL}	0.85	0.79 + 0.030*SL	0.80 + 0.025*SL	0.82 + 0.022*SL
	t_R	0.23	0.17 + 0.031*SL	0.17 + 0.031*SL	0.16 + 0.032*SL
	t_F	0.22	0.14 + 0.039*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
C to Y	t_{PLH}	1.10	1.05 + 0.024*SL	1.07 + 0.019*SL	1.08 + 0.017*SL
	t_{PHL}	0.85	0.79 + 0.029*SL	0.80 + 0.025*SL	0.82 + 0.022*SL
	t_R	0.23	0.17 + 0.029*SL	0.16 + 0.031*SL	0.16 + 0.033*SL
	t_F	0.22	0.14 + 0.038*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
D to Y	t_{PLH}	1.23	1.18 + 0.024*SL	1.20 + 0.019*SL	1.21 + 0.017*SL
	t_{PHL}	1.02	0.97 + 0.030*SL	0.98 + 0.025*SL	1.00 + 0.022*SL
	t_R	0.22	0.16 + 0.031*SL	0.16 + 0.031*SL	0.15 + 0.033*SL
	t_F	0.22	0.15 + 0.039*SL	0.15 + 0.037*SL	0.15 + 0.037*SL
E to Y	t_{PLH}	1.29	1.24 + 0.024*SL	1.26 + 0.019*SL	1.27 + 0.017*SL
	t_{PHL}	1.03	0.97 + 0.030*SL	0.99 + 0.025*SL	1.01 + 0.022*SL
	t_R	0.23	0.17 + 0.029*SL	0.16 + 0.031*SL	0.15 + 0.033*SL
	t_F	0.22	0.15 + 0.039*SL	0.15 + 0.037*SL	0.15 + 0.037*SL
F to Y	t_{PLH}	1.35	1.30 + 0.024*SL	1.32 + 0.019*SL	1.33 + 0.017*SL
	t_{PHL}	1.03	0.97 + 0.030*SL	0.99 + 0.025*SL	1.01 + 0.022*SL
	t_R	0.23	0.16 + 0.032*SL	0.17 + 0.031*SL	0.16 + 0.033*SL
	t_F	0.22	0.15 + 0.039*SL	0.15 + 0.037*SL	0.15 + 0.038*SL
G to Y	t_{PLH}	1.36	1.31 + 0.024*SL	1.33 + 0.019*SL	1.34 + 0.017*SL
	t_{PHL}	1.15	1.08 + 0.030*SL	1.10 + 0.025*SL	1.12 + 0.023*SL
	t_R	0.22	0.16 + 0.030*SL	0.16 + 0.031*SL	0.15 + 0.033*SL
	t_F	0.23	0.15 + 0.038*SL	0.16 + 0.037*SL	0.15 + 0.037*SL
H to Y	t_{PLH}	1.42	1.38 + 0.023*SL	1.39 + 0.019*SL	1.40 + 0.017*SL
	t_{PHL}	1.15	1.09 + 0.030*SL	1.11 + 0.025*SL	1.13 + 0.023*SL
	t_R	0.23	0.16 + 0.032*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
	t_F	0.23	0.15 + 0.039*SL	0.16 + 0.037*SL	0.16 + 0.037*SL
I to Y	t_{PLH}	1.48	1.43 + 0.024*SL	1.45 + 0.019*SL	1.46 + 0.017*SL
	t_{PHL}	1.15	1.09 + 0.030*SL	1.11 + 0.025*SL	1.13 + 0.023*SL
	t_R	0.23	0.17 + 0.031*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
	t_F	0.23	0.15 + 0.038*SL	0.15 + 0.037*SL	0.15 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	Y
1	x	1	0
x	1	1	0
0	0	x	1
x	x	0	1

Cell Data

Input Load (SL)						Gate Count	
STD80							
OA21			*OA21D2*			*OA21*	*OA21D2*
A	B	C	A	B	C		
0.8	0.4	0.9	1.6	0.9	1.9	1.3	2.3
STDM80							
OA21			*OA21D2*			*OA21*	*OA21D2*
A	B	C	A	B	C		
1.1	1.0	1.0	2.0	2.1	2.1	1.3	2.3

OA21/OA21D2

2-OR into 2-NAND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 OA21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.13 + 0.041*SL
	t_{PHL}	0.32	0.21 + 0.053*SL	0.21 + 0.054*SL	0.20 + 0.055*SL
	t_R	0.39	0.23 + 0.080*SL	0.21 + 0.089*SL	0.15 + 0.095*SL
	t_F	0.48	0.29 + 0.095*SL	0.27 + 0.105*SL	0.21 + 0.111*SL
B to Y	t_{PLH}	0.22	0.12 + 0.050*SL	0.14 + 0.041*SL	0.13 + 0.041*SL
	t_{PHL}	0.27	0.16 + 0.057*SL	0.16 + 0.054*SL	0.15 + 0.055*SL
	t_R	0.40	0.25 + 0.076*SL	0.23 + 0.087*SL	0.16 + 0.095*SL
	t_F	0.39	0.20 + 0.095*SL	0.18 + 0.105*SL	0.13 + 0.111*SL
C to Y	t_{PLH}	0.18	0.11 + 0.032*SL	0.13 + 0.025*SL	0.14 + 0.024*SL
	t_{PHL}	0.31	0.21 + 0.054*SL	0.20 + 0.055*SL	0.20 + 0.055*SL
	t_R	0.36	0.29 + 0.034*SL	0.27 + 0.044*SL	0.19 + 0.052*SL
	t_F	0.46	0.25 + 0.102*SL	0.24 + 0.107*SL	0.21 + 0.111*SL

STD80 OA21D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.17	0.12 + 0.025*SL	0.12 + 0.022*SL	0.13 + 0.021*SL
	t_{PHL}	0.26	0.20 + 0.028*SL	0.21 + 0.026*SL	0.20 + 0.027*SL
	t_R	0.31	0.24 + 0.035*SL	0.23 + 0.042*SL	0.18 + 0.047*SL
	t_F	0.38	0.29 + 0.045*SL	0.28 + 0.049*SL	0.23 + 0.054*SL
B to Y	t_{PLH}	0.17	0.11 + 0.029*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
	t_{PHL}	0.21	0.15 + 0.030*SL	0.15 + 0.027*SL	0.15 + 0.027*SL
	t_R	0.33	0.26 + 0.034*SL	0.25 + 0.041*SL	0.18 + 0.047*SL
	t_F	0.30	0.21 + 0.044*SL	0.20 + 0.049*SL	0.14 + 0.054*SL
C to Y	t_{PLH}	0.15	0.11 + 0.018*SL	0.12 + 0.014*SL	0.14 + 0.012*SL
	t_{PHL}	0.25	0.19 + 0.028*SL	0.20 + 0.026*SL	0.19 + 0.027*SL
	t_R	0.32	0.29 + 0.016*SL	0.28 + 0.020*SL	0.22 + 0.025*SL
	t_F	0.35	0.25 + 0.049*SL	0.25 + 0.051*SL	0.22 + 0.054*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 OA21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.19 + 0.065*SL	0.19 + 0.063*SL	0.19 + 0.063*SL
	t_{PHL}	0.40	0.26 + 0.073*SL	0.26 + 0.072*SL	0.26 + 0.071*SL
	t_R	0.52	0.25 + 0.131*SL	0.24 + 0.136*SL	0.22 + 0.138*SL
	t_F	0.58	0.31 + 0.135*SL	0.29 + 0.140*SL	0.27 + 0.142*SL
B to Y	t_{PLH}	0.29	0.17 + 0.064*SL	0.17 + 0.063*SL	0.17 + 0.063*SL
	t_{PHL}	0.34	0.19 + 0.072*SL	0.19 + 0.072*SL	0.20 + 0.071*SL
	t_R	0.52	0.26 + 0.129*SL	0.25 + 0.135*SL	0.22 + 0.138*SL
	t_F	0.48	0.21 + 0.134*SL	0.19 + 0.140*SL	0.17 + 0.143*SL
C to Y	t_{PLH}	0.23	0.16 + 0.036*SL	0.17 + 0.033*SL	0.16 + 0.033*SL
	t_{PHL}	0.41	0.27 + 0.074*SL	0.27 + 0.073*SL	0.27 + 0.072*SL
	t_R	0.33	0.21 + 0.061*SL	0.20 + 0.067*SL	0.17 + 0.070*SL
	t_F	0.57	0.29 + 0.139*SL	0.29 + 0.141*SL	0.28 + 0.142*SL

STDM80 OA21D2

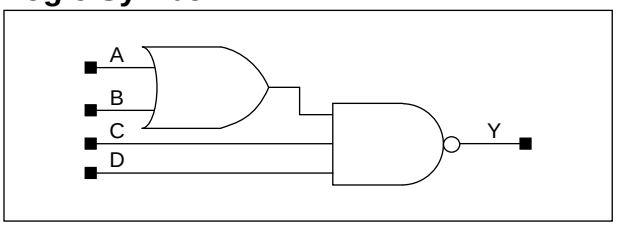
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.18 + 0.034*SL	0.19 + 0.032*SL	0.19 + 0.032*SL
	t_{PHL}	0.32	0.25 + 0.036*SL	0.25 + 0.035*SL	0.25 + 0.035*SL
	t_R	0.39	0.26 + 0.064*SL	0.25 + 0.066*SL	0.24 + 0.068*SL
	t_F	0.43	0.31 + 0.064*SL	0.30 + 0.066*SL	0.29 + 0.068*SL
B to Y	t_{PLH}	0.23	0.16 + 0.035*SL	0.17 + 0.031*SL	0.17 + 0.031*SL
	t_{PHL}	0.25	0.18 + 0.036*SL	0.19 + 0.035*SL	0.19 + 0.035*SL
	t_R	0.39	0.27 + 0.060*SL	0.26 + 0.065*SL	0.24 + 0.067*SL
	t_F	0.33	0.20 + 0.064*SL	0.20 + 0.066*SL	0.19 + 0.068*SL
C to Y	t_{PLH}	0.19	0.15 + 0.021*SL	0.16 + 0.017*SL	0.16 + 0.017*SL
	t_{PHL}	0.32	0.25 + 0.036*SL	0.25 + 0.035*SL	0.25 + 0.035*SL
	t_R	0.27	0.21 + 0.028*SL	0.21 + 0.031*SL	0.19 + 0.033*SL
	t_F	0.42	0.29 + 0.066*SL	0.28 + 0.067*SL	0.28 + 0.068*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

OA211/OA211D2

2-OR into 3-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	x	1	1	0
x	1	1	1	0
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1

Cell Data

Input Load (SL)								Gate Count	
STD80									
OA211				*OA211D2*				*OA211*	*OA211D2*
A	B	C	D	A	B	C	D		
0.9	0.5	1.0	1.0	1.6	0.9	1.9	1.8	1.7	3.0
STDM80									
OA211				*OA211D2*				*OA211*	*OA211D2*
A	B	C	D	A	B	C	D		
1.1	1.0	1.0	1.0	2.0	2.2	2.1	2.2	1.7	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 OA211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.14 + 0.045*SL	0.15 + 0.041*SL	0.15 + 0.041*SL
	t_{PHL}	0.44	0.30 + 0.071*SL	0.29 + 0.072*SL	0.29 + 0.073*SL
	t_R	0.44	0.28 + 0.081*SL	0.26 + 0.089*SL	0.21 + 0.095*SL
	t_F	0.71	0.43 + 0.141*SL	0.41 + 0.149*SL	0.38 + 0.152*SL
B to Y	t_{PLH}	0.24	0.14 + 0.049*SL	0.16 + 0.041*SL	0.15 + 0.041*SL
	t_{PHL}	0.37	0.23 + 0.070*SL	0.23 + 0.072*SL	0.22 + 0.073*SL
	t_R	0.46	0.30 + 0.079*SL	0.28 + 0.088*SL	0.21 + 0.095*SL
	t_F	0.59	0.31 + 0.141*SL	0.29 + 0.149*SL	0.26 + 0.152*SL
C to Y	t_{PLH}	0.19	0.13 + 0.032*SL	0.14 + 0.025*SL	0.15 + 0.024*SL
	t_{PHL}	0.45	0.31 + 0.072*SL	0.31 + 0.073*SL	0.31 + 0.073*SL
	t_R	0.38	0.30 + 0.039*SL	0.29 + 0.044*SL	0.22 + 0.052*SL
	t_F	0.70	0.41 + 0.146*SL	0.40 + 0.150*SL	0.38 + 0.152*SL
D to Y	t_{PLH}	0.20	0.14 + 0.031*SL	0.15 + 0.025*SL	0.16 + 0.024*SL
	t_{PHL}	0.44	0.29 + 0.072*SL	0.29 + 0.073*SL	0.29 + 0.073*SL
	t_R	0.40	0.32 + 0.036*SL	0.31 + 0.044*SL	0.23 + 0.052*SL
	t_F	0.70	0.40 + 0.148*SL	0.40 + 0.150*SL	0.38 + 0.152*SL

STD80 OA211D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.14 + 0.024*SL	0.14 + 0.021*SL	0.15 + 0.021*SL
	t_{PHL}	0.36	0.29 + 0.034*SL	0.29 + 0.035*SL	0.28 + 0.036*SL
	t_R	0.36	0.28 + 0.039*SL	0.27 + 0.043*SL	0.23 + 0.047*SL
	t_F	0.56	0.42 + 0.069*SL	0.42 + 0.071*SL	0.38 + 0.075*SL
B to Y	t_{PLH}	0.19	0.13 + 0.027*SL	0.15 + 0.022*SL	0.16 + 0.021*SL
	t_{PHL}	0.30	0.23 + 0.034*SL	0.23 + 0.035*SL	0.22 + 0.036*SL
	t_R	0.38	0.30 + 0.038*SL	0.29 + 0.041*SL	0.24 + 0.047*SL
	t_F	0.44	0.31 + 0.068*SL	0.30 + 0.072*SL	0.27 + 0.075*SL
C to Y	t_{PLH}	0.16	0.12 + 0.018*SL	0.13 + 0.014*SL	0.15 + 0.012*SL
	t_{PHL}	0.37	0.30 + 0.036*SL	0.30 + 0.035*SL	0.30 + 0.036*SL
	t_R	0.34	0.31 + 0.018*SL	0.30 + 0.020*SL	0.25 + 0.026*SL
	t_F	0.54	0.40 + 0.072*SL	0.40 + 0.073*SL	0.38 + 0.075*SL
D to Y	t_{PLH}	0.17	0.13 + 0.017*SL	0.14 + 0.014*SL	0.16 + 0.012*SL
	t_{PHL}	0.36	0.29 + 0.035*SL	0.29 + 0.036*SL	0.28 + 0.036*SL
	t_R	0.36	0.32 + 0.018*SL	0.32 + 0.020*SL	0.27 + 0.025*SL
	t_F	0.54	0.39 + 0.072*SL	0.39 + 0.074*SL	0.38 + 0.075*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

OA211/OA211D2

2-OR into 3-NAND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STDM80 OA211

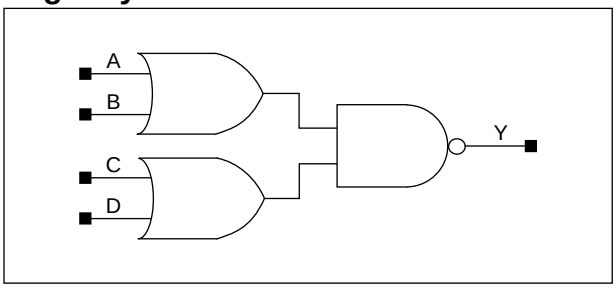
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.36	0.23 + 0.063*SL	0.23 + 0.063*SL	0.23 + 0.063*SL
	t_{PHL}	0.59	0.39 + 0.100*SL	0.39 + 0.099*SL	0.40 + 0.098*SL
	t_R	0.60	0.34 + 0.132*SL	0.33 + 0.136*SL	0.31 + 0.139*SL
	t_F	0.93	0.53 + 0.198*SL	0.53 + 0.201*SL	0.53 + 0.201*SL
B to Y	t_{PLH}	0.33	0.20 + 0.063*SL	0.20 + 0.063*SL	0.21 + 0.063*SL
	t_{PHL}	0.49	0.29 + 0.099*SL	0.29 + 0.099*SL	0.30 + 0.098*SL
	t_R	0.61	0.35 + 0.131*SL	0.33 + 0.136*SL	0.31 + 0.139*SL
	t_F	0.79	0.39 + 0.198*SL	0.38 + 0.201*SL	0.38 + 0.202*SL
C to Y	t_{PLH}	0.25	0.18 + 0.034*SL	0.18 + 0.033*SL	0.18 + 0.033*SL
	t_{PHL}	0.63	0.42 + 0.101*SL	0.43 + 0.100*SL	0.44 + 0.099*SL
	t_R	0.37	0.25 + 0.062*SL	0.23 + 0.068*SL	0.22 + 0.070*SL
	t_F	0.93	0.53 + 0.198*SL	0.53 + 0.201*SL	0.53 + 0.201*SL
D to Y	t_{PLH}	0.26	0.19 + 0.034*SL	0.19 + 0.033*SL	0.19 + 0.033*SL
	t_{PHL}	0.62	0.42 + 0.101*SL	0.43 + 0.100*SL	0.43 + 0.099*SL
	t_R	0.39	0.27 + 0.062*SL	0.25 + 0.067*SL	0.23 + 0.070*SL
	t_F	0.93	0.53 + 0.199*SL	0.53 + 0.201*SL	0.53 + 0.201*SL

STDM80 OA211D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.22 + 0.033*SL	0.23 + 0.032*SL	0.23 + 0.032*SL
	t_{PHL}	0.48	0.38 + 0.049*SL	0.38 + 0.048*SL	0.38 + 0.048*SL
	t_R	0.47	0.34 + 0.066*SL	0.34 + 0.067*SL	0.32 + 0.068*SL
	t_F	0.72	0.53 + 0.096*SL	0.52 + 0.098*SL	0.51 + 0.099*SL
B to Y	t_{PLH}	0.27	0.20 + 0.032*SL	0.20 + 0.032*SL	0.21 + 0.031*SL
	t_{PHL}	0.38	0.29 + 0.049*SL	0.29 + 0.048*SL	0.29 + 0.049*SL
	t_R	0.48	0.35 + 0.064*SL	0.34 + 0.066*SL	0.33 + 0.068*SL
	t_F	0.58	0.39 + 0.096*SL	0.38 + 0.098*SL	0.37 + 0.099*SL
C to Y	t_{PLH}	0.21	0.17 + 0.020*SL	0.18 + 0.017*SL	0.18 + 0.017*SL
	t_{PHL}	0.51	0.41 + 0.050*SL	0.41 + 0.049*SL	0.42 + 0.049*SL
	t_R	0.31	0.25 + 0.029*SL	0.24 + 0.033*SL	0.24 + 0.033*SL
	t_F	0.72	0.52 + 0.097*SL	0.52 + 0.098*SL	0.51 + 0.099*SL
D to Y	t_{PLH}	0.22	0.18 + 0.019*SL	0.19 + 0.017*SL	0.19 + 0.017*SL
	t_{PHL}	0.51	0.41 + 0.050*SL	0.41 + 0.049*SL	0.41 + 0.049*SL
	t_R	0.33	0.27 + 0.030*SL	0.26 + 0.032*SL	0.25 + 0.033*SL
	t_F	0.71	0.52 + 0.097*SL	0.52 + 0.098*SL	0.51 + 0.099*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	0	0	1
1	x	x	1	0
x	1	x	1	0
1	x	1	x	0
x	1	1	x	0

Cell Data

Input Load (SL)								**Gate Count**	
STD80									
OA22				*OA22D2*				*OA22*	*OA22D2*
A	B	C	D	A	B	C	D		
1.1	0.5	0.5	0.9	1.8	1.1	1.2	1.9	1.7	3.0
STDM80									
OA22				*OA22D2*				*OA22*	*OA22D2*
A	B	C	D	A	B	C	D		
1.1	1.0	1.0	1.0	2.0	2.1	2.2	2.2	1.7	3.0

OA22/OA22D2

Two 2-ORs into 2-NAND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 OA22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.14 + 0.045*SL	0.15 + 0.042*SL	0.15 + 0.041*SL
	t_{PHL}	0.37	0.27 + 0.054*SL	0.27 + 0.055*SL	0.26 + 0.055*SL
	t_R	0.49	0.33 + 0.078*SL	0.31 + 0.089*SL	0.25 + 0.095*SL
	t_F	0.55	0.35 + 0.102*SL	0.34 + 0.106*SL	0.30 + 0.111*SL
B to Y	t_{PLH}	0.24	0.14 + 0.048*SL	0.16 + 0.041*SL	0.16 + 0.041*SL
	t_{PHL}	0.33	0.22 + 0.055*SL	0.22 + 0.055*SL	0.21 + 0.055*SL
	t_R	0.50	0.35 + 0.076*SL	0.32 + 0.087*SL	0.25 + 0.095*SL
	t_F	0.46	0.26 + 0.102*SL	0.25 + 0.107*SL	0.21 + 0.111*SL
C to Y	t_{PLH}	0.27	0.18 + 0.044*SL	0.19 + 0.041*SL	0.18 + 0.041*SL
	t_{PHL}	0.32	0.21 + 0.056*SL	0.21 + 0.055*SL	0.22 + 0.055*SL
	t_R	0.55	0.40 + 0.076*SL	0.37 + 0.087*SL	0.30 + 0.095*SL
	t_F	0.45	0.25 + 0.104*SL	0.24 + 0.108*SL	0.21 + 0.111*SL
D to Y	t_{PLH}	0.26	0.18 + 0.043*SL	0.18 + 0.041*SL	0.18 + 0.041*SL
	t_{PHL}	0.37	0.26 + 0.055*SL	0.26 + 0.055*SL	0.26 + 0.055*SL
	t_R	0.53	0.37 + 0.081*SL	0.36 + 0.088*SL	0.30 + 0.095*SL
	t_F	0.54	0.34 + 0.103*SL	0.33 + 0.108*SL	0.30 + 0.111*SL

STD80 OA22D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.14 + 0.024*SL	0.15 + 0.021*SL	0.15 + 0.021*SL
	t_{PHL}	0.31	0.26 + 0.026*SL	0.26 + 0.026*SL	0.26 + 0.027*SL
	t_R	0.41	0.34 + 0.037*SL	0.32 + 0.042*SL	0.27 + 0.047*SL
	t_F	0.45	0.35 + 0.048*SL	0.35 + 0.051*SL	0.31 + 0.054*SL
B to Y	t_{PLH}	0.19	0.14 + 0.026*SL	0.15 + 0.022*SL	0.16 + 0.021*SL
	t_{PHL}	0.27	0.21 + 0.028*SL	0.22 + 0.027*SL	0.21 + 0.027*SL
	t_R	0.43	0.35 + 0.037*SL	0.34 + 0.041*SL	0.28 + 0.047*SL
	t_F	0.36	0.27 + 0.048*SL	0.26 + 0.051*SL	0.23 + 0.054*SL
C to Y	t_{PLH}	0.23	0.18 + 0.023*SL	0.19 + 0.021*SL	0.19 + 0.021*SL
	t_{PHL}	0.26	0.21 + 0.028*SL	0.21 + 0.027*SL	0.21 + 0.027*SL
	t_R	0.47	0.40 + 0.036*SL	0.39 + 0.041*SL	0.33 + 0.047*SL
	t_F	0.35	0.25 + 0.050*SL	0.25 + 0.052*SL	0.22 + 0.054*SL
D to Y	t_{PLH}	0.22	0.18 + 0.023*SL	0.18 + 0.021*SL	0.18 + 0.021*SL
	t_{PHL}	0.31	0.26 + 0.027*SL	0.26 + 0.027*SL	0.26 + 0.027*SL
	t_R	0.46	0.38 + 0.038*SL	0.37 + 0.042*SL	0.32 + 0.047*SL
	t_F	0.44	0.34 + 0.051*SL	0.34 + 0.051*SL	0.31 + 0.054*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 OA22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.33	0.20 + 0.065*SL	0.21 + 0.064*SL	0.21 + 0.064*SL
	t_{PHL}	0.48	0.33 + 0.073*SL	0.34 + 0.072*SL	0.34 + 0.072*SL
	t_R	0.66	0.40 + 0.130*SL	0.38 + 0.135*SL	0.36 + 0.138*SL
	t_F	0.67	0.40 + 0.137*SL	0.39 + 0.141*SL	0.38 + 0.142*SL
B to Y	t_{PLH}	0.31	0.18 + 0.064*SL	0.18 + 0.064*SL	0.18 + 0.064*SL
	t_{PHL}	0.41	0.26 + 0.074*SL	0.27 + 0.072*SL	0.27 + 0.072*SL
	t_R	0.66	0.41 + 0.128*SL	0.39 + 0.134*SL	0.36 + 0.138*SL
	t_F	0.57	0.30 + 0.137*SL	0.29 + 0.141*SL	0.27 + 0.143*SL
C to Y	t_{PLH}	0.36	0.23 + 0.065*SL	0.23 + 0.064*SL	0.23 + 0.064*SL
	t_{PHL}	0.43	0.29 + 0.075*SL	0.29 + 0.073*SL	0.30 + 0.072*SL
	t_R	0.73	0.47 + 0.128*SL	0.45 + 0.135*SL	0.42 + 0.138*SL
	t_F	0.57	0.29 + 0.139*SL	0.29 + 0.141*SL	0.28 + 0.142*SL
D to Y	t_{PLH}	0.38	0.25 + 0.066*SL	0.25 + 0.064*SL	0.26 + 0.064*SL
	t_{PHL}	0.50	0.35 + 0.074*SL	0.36 + 0.072*SL	0.36 + 0.072*SL
	t_R	0.72	0.46 + 0.130*SL	0.45 + 0.136*SL	0.43 + 0.138*SL
	t_F	0.67	0.39 + 0.140*SL	0.38 + 0.142*SL	0.38 + 0.142*SL

STDM80 OA22D2

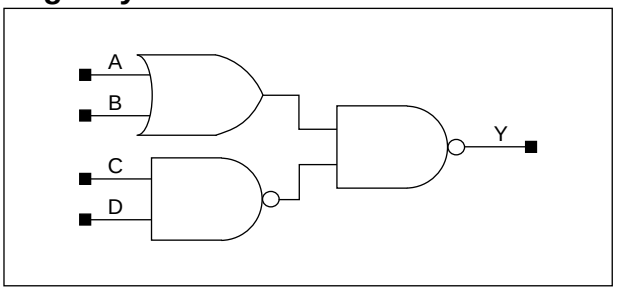
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.27	0.20 + 0.033*SL	0.21 + 0.032*SL	0.21 + 0.032*SL
	t_{PHL}	0.39	0.32 + 0.036*SL	0.32 + 0.035*SL	0.33 + 0.035*SL
	t_R	0.53	0.41 + 0.064*SL	0.40 + 0.066*SL	0.39 + 0.067*SL
	t_F	0.53	0.39 + 0.066*SL	0.39 + 0.068*SL	0.38 + 0.069*SL
B to Y	t_{PLH}	0.25	0.18 + 0.033*SL	0.18 + 0.032*SL	0.18 + 0.032*SL
	t_{PHL}	0.33	0.26 + 0.036*SL	0.26 + 0.036*SL	0.26 + 0.035*SL
	t_R	0.54	0.42 + 0.060*SL	0.41 + 0.065*SL	0.39 + 0.067*SL
	t_F	0.43	0.30 + 0.067*SL	0.29 + 0.067*SL	0.29 + 0.068*SL
C to Y	t_{PLH}	0.29	0.23 + 0.032*SL	0.23 + 0.032*SL	0.23 + 0.032*SL
	t_{PHL}	0.35	0.27 + 0.036*SL	0.27 + 0.036*SL	0.28 + 0.035*SL
	t_R	0.60	0.48 + 0.061*SL	0.47 + 0.065*SL	0.45 + 0.067*SL
	t_F	0.42	0.29 + 0.067*SL	0.29 + 0.068*SL	0.28 + 0.068*SL
D to Y	t_{PLH}	0.32	0.25 + 0.033*SL	0.25 + 0.033*SL	0.26 + 0.032*SL
	t_{PHL}	0.42	0.34 + 0.037*SL	0.35 + 0.036*SL	0.35 + 0.035*SL
	t_R	0.59	0.47 + 0.064*SL	0.46 + 0.066*SL	0.45 + 0.068*SL
	t_F	0.52	0.38 + 0.068*SL	0.38 + 0.068*SL	0.38 + 0.068*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

OA22A/OA22D2A

2-OR and 2-NAND into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	1	1	1
1	x	0	x	0
1	x	x	0	0
x	1	0	x	0
x	1	x	0	0

Cell Data

Input Load (SL)								Gate Count	
STD80									
OA22A				*OA22D2A*				*OA22A*	*OA22D2A*
A	B	C	D	A	B	C	D		
0.8	0.8	0.7	0.7	1.6	1.6	0.8	0.8	2.0	3.0
STDM80									
OA22A				*OA22D2A*				*OA22A*	*OA22D2A*
A	B	C	D	A	B	C	D		
1.1	1.0	0.7	0.7	2.1	2.0	0.8	0.8	2.0	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 OA22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.13 + 0.041*SL
	t_{PHL}	0.32	0.21 + 0.054*SL	0.21 + 0.054*SL	0.20 + 0.055*SL
	t_R	0.39	0.23 + 0.080*SL	0.21 + 0.089*SL	0.15 + 0.095*SL
	t_F	0.48	0.29 + 0.096*SL	0.27 + 0.105*SL	0.21 + 0.111*SL
B to Y	t_{PLH}	0.22	0.12 + 0.050*SL	0.14 + 0.041*SL	0.13 + 0.041*SL
	t_{PHL}	0.27	0.16 + 0.058*SL	0.16 + 0.054*SL	0.15 + 0.055*SL
	t_R	0.40	0.25 + 0.076*SL	0.23 + 0.087*SL	0.16 + 0.095*SL
	t_F	0.39	0.20 + 0.095*SL	0.18 + 0.105*SL	0.13 + 0.111*SL
C to Y	t_{PLH}	0.29	0.24 + 0.027*SL	0.24 + 0.025*SL	0.25 + 0.024*SL
	t_{PHL}	0.47	0.36 + 0.056*SL	0.36 + 0.056*SL	0.36 + 0.055*SL
	t_R	0.29	0.21 + 0.044*SL	0.20 + 0.048*SL	0.16 + 0.052*SL
	t_F	0.44	0.22 + 0.109*SL	0.22 + 0.110*SL	0.21 + 0.111*SL
D to Y	t_{PLH}	0.31	0.25 + 0.028*SL	0.26 + 0.025*SL	0.27 + 0.024*SL
	t_{PHL}	0.45	0.33 + 0.057*SL	0.34 + 0.056*SL	0.34 + 0.055*SL
	t_R	0.29	0.21 + 0.043*SL	0.20 + 0.048*SL	0.16 + 0.052*SL
	t_F	0.44	0.22 + 0.108*SL	0.22 + 0.110*SL	0.21 + 0.111*SL

STD80 OA22D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.17	0.11 + 0.028*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
	t_{PHL}	0.21	0.15 + 0.031*SL	0.16 + 0.027*SL	0.16 + 0.027*SL
	t_R	0.33	0.26 + 0.034*SL	0.25 + 0.041*SL	0.19 + 0.047*SL
	t_F	0.30	0.21 + 0.044*SL	0.20 + 0.049*SL	0.15 + 0.054*SL
B to Y	t_{PLH}	0.17	0.12 + 0.025*SL	0.12 + 0.022*SL	0.13 + 0.021*SL
	t_{PHL}	0.26	0.20 + 0.028*SL	0.21 + 0.026*SL	0.20 + 0.027*SL
	t_R	0.31	0.24 + 0.035*SL	0.23 + 0.042*SL	0.18 + 0.047*SL
	t_F	0.38	0.30 + 0.044*SL	0.29 + 0.049*SL	0.23 + 0.054*SL
C to Y	t_{PLH}	0.33	0.30 + 0.016*SL	0.30 + 0.014*SL	0.32 + 0.012*SL
	t_{PHL}	0.46	0.40 + 0.028*SL	0.40 + 0.027*SL	0.41 + 0.027*SL
	t_R	0.28	0.24 + 0.020*SL	0.24 + 0.022*SL	0.20 + 0.026*SL
	t_F	0.33	0.23 + 0.053*SL	0.23 + 0.053*SL	0.21 + 0.054*SL
D to Y	t_{PLH}	0.35	0.32 + 0.015*SL	0.32 + 0.014*SL	0.34 + 0.012*SL
	t_{PHL}	0.44	0.39 + 0.028*SL	0.39 + 0.027*SL	0.39 + 0.027*SL
	t_R	0.29	0.23 + 0.028*SL	0.25 + 0.021*SL	0.20 + 0.026*SL
	t_F	0.33	0.23 + 0.052*SL	0.22 + 0.053*SL	0.21 + 0.054*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

OA22A/OA22D2A

2-OR and 2-NAND into 2-NAND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 OA22A

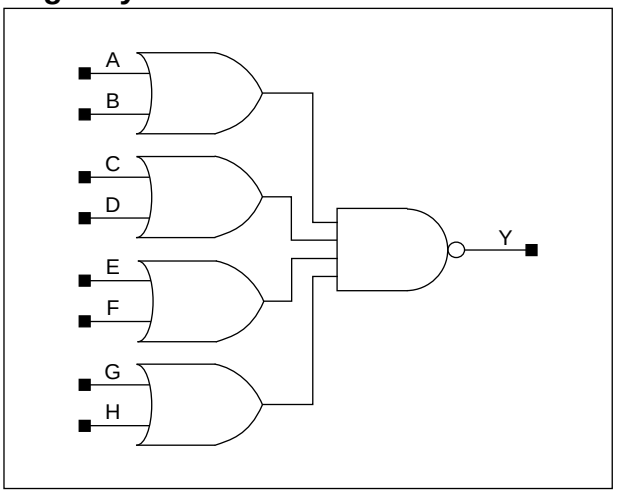
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.19 + 0.064*SL	0.19 + 0.063*SL	0.19 + 0.063*SL
	t_{PHL}	0.40	0.26 + 0.073*SL	0.26 + 0.072*SL	0.26 + 0.071*SL
	t_R	0.52	0.25 + 0.131*SL	0.24 + 0.136*SL	0.22 + 0.138*SL
	t_F	0.58	0.31 + 0.135*SL	0.29 + 0.140*SL	0.28 + 0.142*SL
B to Y	t_{PLH}	0.29	0.17 + 0.064*SL	0.17 + 0.063*SL	0.17 + 0.063*SL
	t_{PHL}	0.34	0.19 + 0.072*SL	0.19 + 0.072*SL	0.20 + 0.071*SL
	t_R	0.52	0.26 + 0.129*SL	0.25 + 0.135*SL	0.22 + 0.138*SL
	t_F	0.48	0.21 + 0.135*SL	0.19 + 0.140*SL	0.17 + 0.143*SL
C to Y	t_{PLH}	0.40	0.32 + 0.037*SL	0.33 + 0.034*SL	0.34 + 0.034*SL
	t_{PHL}	0.63	0.48 + 0.075*SL	0.48 + 0.073*SL	0.49 + 0.072*SL
	t_R	0.32	0.19 + 0.068*SL	0.18 + 0.070*SL	0.17 + 0.071*SL
	t_F	0.57	0.29 + 0.140*SL	0.28 + 0.142*SL	0.28 + 0.142*SL
D to Y	t_{PLH}	0.41	0.33 + 0.038*SL	0.34 + 0.035*SL	0.35 + 0.034*SL
	t_{PHL}	0.60	0.45 + 0.075*SL	0.46 + 0.073*SL	0.47 + 0.072*SL
	t_R	0.40	0.27 + 0.066*SL	0.26 + 0.069*SL	0.24 + 0.071*SL
	t_F	0.57	0.29 + 0.141*SL	0.28 + 0.142*SL	0.28 + 0.142*SL

STDM80 OA22D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.16 + 0.035*SL	0.17 + 0.032*SL	0.17 + 0.031*SL
	t_{PHL}	0.26	0.18 + 0.036*SL	0.19 + 0.035*SL	0.19 + 0.035*SL
	t_R	0.39	0.27 + 0.061*SL	0.26 + 0.065*SL	0.24 + 0.068*SL
	t_F	0.34	0.21 + 0.063*SL	0.20 + 0.066*SL	0.19 + 0.068*SL
B to Y	t_{PLH}	0.25	0.18 + 0.034*SL	0.19 + 0.032*SL	0.19 + 0.032*SL
	t_{PHL}	0.32	0.25 + 0.036*SL	0.25 + 0.035*SL	0.25 + 0.035*SL
	t_R	0.39	0.26 + 0.064*SL	0.25 + 0.066*SL	0.24 + 0.068*SL
	t_F	0.44	0.31 + 0.064*SL	0.30 + 0.066*SL	0.29 + 0.068*SL
C to Y	t_{PLH}	0.45	0.40 + 0.022*SL	0.41 + 0.019*SL	0.42 + 0.018*SL
	t_{PHL}	0.61	0.54 + 0.037*SL	0.54 + 0.036*SL	0.55 + 0.035*SL
	t_R	0.29	0.22 + 0.034*SL	0.22 + 0.034*SL	0.22 + 0.034*SL
	t_F	0.43	0.29 + 0.068*SL	0.29 + 0.067*SL	0.29 + 0.068*SL
D to Y	t_{PLH}	0.46	0.41 + 0.022*SL	0.42 + 0.019*SL	0.43 + 0.018*SL
	t_{PHL}	0.59	0.51 + 0.037*SL	0.52 + 0.036*SL	0.53 + 0.035*SL
	t_R	0.29	0.22 + 0.033*SL	0.22 + 0.034*SL	0.22 + 0.034*SL
	t_F	0.43	0.29 + 0.068*SL	0.29 + 0.068*SL	0.29 + 0.068*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	x	x	x	x	x	x	1
x	x	0	0	x	x	x	x	1
x	x	x	x	0	0	x	x	1
x	x	x	x	x	x	0	0	1
Other States								0

Cell Data

Input Load (SL)																Gate Count	
STD80																	
OA2222								*OA2222D2*								*OA2222*	*OA2222 D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
0.6	0.4	0.5	0.7	0.6	0.7	0.8	0.8	0.6	0.4	0.5	0.7	0.6	0.6	0.8	0.8	4.7	5.0
STDM80																	
OA2222								*OA2222D2*								*OA2222*	*OA2222 D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
0.7	0.7	0.8	0.8	0.7	0.7	0.8	0.8	0.7	0.7	0.8	0.8	0.7	0.7	0.8	0.8	4.7	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 OA2222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.50	0.45 + 0.026*SL	0.45 + 0.024*SL	0.45 + 0.024*SL
	t_{PHL}	0.59	0.50 + 0.043*SL	0.51 + 0.038*SL	0.52 + 0.037*SL
	t_R	0.19	0.11 + 0.042*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
B to Y	t_{PLH}	0.50	0.45 + 0.026*SL	0.46 + 0.024*SL	0.46 + 0.024*SL
	t_{PHL}	0.55	0.46 + 0.043*SL	0.47 + 0.038*SL	0.48 + 0.037*SL
	t_R	0.19	0.11 + 0.044*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.25	0.12 + 0.063*SL	0.11 + 0.067*SL	0.09 + 0.069*SL
C to Y	t_{PLH}	0.45	0.40 + 0.026*SL	0.40 + 0.024*SL	0.40 + 0.024*SL
	t_{PHL}	0.55	0.46 + 0.043*SL	0.47 + 0.038*SL	0.48 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.050*SL	0.07 + 0.052*SL
	t_F	0.25	0.12 + 0.064*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
D to Y	t_{PLH}	0.44	0.39 + 0.026*SL	0.40 + 0.024*SL	0.40 + 0.024*SL
	t_{PHL}	0.59	0.50 + 0.043*SL	0.51 + 0.038*SL	0.53 + 0.037*SL
	t_R	0.19	0.10 + 0.043*SL	0.09 + 0.050*SL	0.07 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
E to Y	t_{PLH}	0.53	0.48 + 0.027*SL	0.49 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.60	0.52 + 0.043*SL	0.53 + 0.038*SL	0.54 + 0.037*SL
	t_R	0.20	0.12 + 0.042*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.25	0.12 + 0.063*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
F to Y	t_{PLH}	0.54	0.49 + 0.026*SL	0.49 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.57	0.48 + 0.043*SL	0.49 + 0.038*SL	0.50 + 0.037*SL
	t_R	0.20	0.11 + 0.043*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
G to Y	t_{PLH}	0.48	0.43 + 0.027*SL	0.43 + 0.024*SL	0.43 + 0.024*SL
	t_{PHL}	0.57	0.48 + 0.043*SL	0.49 + 0.038*SL	0.50 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
H to Y	t_{PLH}	0.48	0.42 + 0.026*SL	0.43 + 0.024*SL	0.43 + 0.024*SL
	t_{PHL}	0.61	0.52 + 0.042*SL	0.53 + 0.038*SL	0.54 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 OA2222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.52	0.48 + 0.016*SL	0.49 + 0.013*SL	0.50 + 0.012*SL
	t_{PHL}	0.61	0.56 + 0.025*SL	0.57 + 0.021*SL	0.60 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.21	0.15 + 0.031*SL	0.15 + 0.031*SL	0.12 + 0.034*SL
B to Y	t_{PLH}	0.52	0.49 + 0.017*SL	0.50 + 0.013*SL	0.51 + 0.012*SL
	t_{PHL}	0.57	0.52 + 0.025*SL	0.53 + 0.021*SL	0.56 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.21	0.15 + 0.030*SL	0.15 + 0.031*SL	0.12 + 0.034*SL
C to Y	t_{PLH}	0.46	0.43 + 0.018*SL	0.44 + 0.013*SL	0.45 + 0.012*SL
	t_{PHL}	0.57	0.52 + 0.025*SL	0.53 + 0.021*SL	0.56 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.21	0.14 + 0.032*SL	0.14 + 0.031*SL	0.12 + 0.034*SL
D to Y	t_{PLH}	0.46	0.43 + 0.017*SL	0.43 + 0.013*SL	0.45 + 0.012*SL
	t_{PHL}	0.61	0.57 + 0.024*SL	0.57 + 0.021*SL	0.60 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.21	0.14 + 0.032*SL	0.15 + 0.031*SL	0.12 + 0.034*SL
E to Y	t_{PLH}	0.55	0.52 + 0.018*SL	0.53 + 0.013*SL	0.54 + 0.012*SL
	t_{PHL}	0.63	0.58 + 0.025*SL	0.59 + 0.021*SL	0.62 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.022*SL	0.08 + 0.026*SL
	t_F	0.21	0.15 + 0.032*SL	0.15 + 0.031*SL	0.12 + 0.034*SL
F to Y	t_{PLH}	0.56	0.52 + 0.017*SL	0.53 + 0.013*SL	0.54 + 0.012*SL
	t_{PHL}	0.60	0.55 + 0.025*SL	0.56 + 0.021*SL	0.58 + 0.018*SL
	t_R	0.16	0.12 + 0.019*SL	0.12 + 0.022*SL	0.08 + 0.026*SL
	t_F	0.21	0.15 + 0.029*SL	0.14 + 0.031*SL	0.12 + 0.034*SL
G to Y	t_{PLH}	0.50	0.46 + 0.017*SL	0.47 + 0.013*SL	0.48 + 0.012*SL
	t_{PHL}	0.60	0.55 + 0.025*SL	0.56 + 0.021*SL	0.58 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.022*SL	0.08 + 0.026*SL
	t_F	0.21	0.14 + 0.032*SL	0.15 + 0.031*SL	0.12 + 0.034*SL
H to Y	t_{PLH}	0.49	0.46 + 0.017*SL	0.47 + 0.013*SL	0.48 + 0.012*SL
	t_{PHL}	0.63	0.58 + 0.025*SL	0.59 + 0.021*SL	0.62 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.21	0.14 + 0.033*SL	0.15 + 0.031*SL	0.12 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 OA2222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.73	0.66 + 0.036*SL	0.67 + 0.034*SL	0.67 + 0.033*SL
	t_{PHL}	0.83	0.72 + 0.055*SL	0.74 + 0.048*SL	0.76 + 0.045*SL
	t_R	0.27	0.14 + 0.066*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.33	0.16 + 0.082*SL	0.17 + 0.080*SL	0.16 + 0.081*SL
B to Y	t_{PLH}	0.71	0.64 + 0.036*SL	0.64 + 0.034*SL	0.65 + 0.033*SL
	t_{PHL}	0.78	0.67 + 0.055*SL	0.69 + 0.048*SL	0.71 + 0.045*SL
	t_R	0.27	0.14 + 0.066*SL	0.12 + 0.069*SL	0.11 + 0.072*SL
	t_F	0.33	0.16 + 0.081*SL	0.17 + 0.080*SL	0.16 + 0.081*SL
C to Y	t_{PLH}	0.62	0.54 + 0.036*SL	0.55 + 0.034*SL	0.55 + 0.033*SL
	t_{PHL}	0.76	0.65 + 0.055*SL	0.67 + 0.048*SL	0.69 + 0.045*SL
	t_R	0.26	0.13 + 0.066*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.33	0.16 + 0.082*SL	0.17 + 0.080*SL	0.16 + 0.081*SL
D to Y	t_{PLH}	0.64	0.57 + 0.036*SL	0.57 + 0.034*SL	0.58 + 0.033*SL
	t_{PHL}	0.81	0.70 + 0.055*SL	0.72 + 0.048*SL	0.74 + 0.045*SL
	t_R	0.26	0.13 + 0.066*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.33	0.17 + 0.081*SL	0.17 + 0.080*SL	0.16 + 0.081*SL
E to Y	t_{PLH}	0.78	0.71 + 0.037*SL	0.72 + 0.034*SL	0.72 + 0.033*SL
	t_{PHL}	0.87	0.76 + 0.055*SL	0.78 + 0.048*SL	0.80 + 0.045*SL
	t_R	0.27	0.14 + 0.065*SL	0.13 + 0.069*SL	0.11 + 0.071*SL
	t_F	0.33	0.16 + 0.082*SL	0.17 + 0.080*SL	0.16 + 0.081*SL
F to Y	t_{PLH}	0.76	0.69 + 0.037*SL	0.70 + 0.034*SL	0.70 + 0.033*SL
	t_{PHL}	0.82	0.71 + 0.055*SL	0.73 + 0.048*SL	0.75 + 0.045*SL
	t_R	0.27	0.14 + 0.065*SL	0.13 + 0.069*SL	0.11 + 0.071*SL
	t_F	0.33	0.16 + 0.082*SL	0.17 + 0.080*SL	0.16 + 0.081*SL
G to Y	t_{PLH}	0.66	0.59 + 0.037*SL	0.60 + 0.034*SL	0.60 + 0.033*SL
	t_{PHL}	0.80	0.69 + 0.055*SL	0.71 + 0.048*SL	0.73 + 0.045*SL
	t_R	0.27	0.14 + 0.065*SL	0.13 + 0.069*SL	0.11 + 0.071*SL
	t_F	0.33	0.16 + 0.081*SL	0.17 + 0.080*SL	0.16 + 0.081*SL
H to Y	t_{PLH}	0.69	0.61 + 0.036*SL	0.62 + 0.034*SL	0.62 + 0.033*SL
	t_{PHL}	0.85	0.74 + 0.055*SL	0.76 + 0.048*SL	0.78 + 0.045*SL
	t_R	0.27	0.14 + 0.065*SL	0.13 + 0.069*SL	0.11 + 0.071*SL
	t_F	0.33	0.16 + 0.083*SL	0.17 + 0.079*SL	0.17 + 0.080*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 OA2222D2

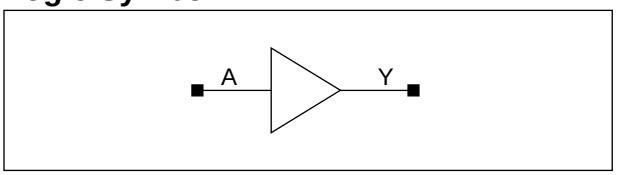
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.75	0.71 + 0.023*SL	0.72 + 0.019*SL	0.73 + 0.017*SL
	t_{PHL}	0.88	0.81 + 0.034*SL	0.83 + 0.028*SL	0.85 + 0.025*SL
	t_R	0.20	0.14 + 0.032*SL	0.14 + 0.032*SL	0.13 + 0.034*SL
	t_F	0.27	0.18 + 0.043*SL	0.19 + 0.039*SL	0.20 + 0.038*SL
B to Y	t_{PLH}	0.73	0.68 + 0.023*SL	0.70 + 0.019*SL	0.71 + 0.017*SL
	t_{PHL}	0.83	0.76 + 0.034*SL	0.78 + 0.028*SL	0.80 + 0.025*SL
	t_R	0.20	0.13 + 0.033*SL	0.14 + 0.032*SL	0.13 + 0.034*SL
	t_F	0.27	0.18 + 0.042*SL	0.19 + 0.039*SL	0.20 + 0.038*SL
C to Y	t_{PLH}	0.63	0.59 + 0.022*SL	0.60 + 0.019*SL	0.61 + 0.017*SL
	t_{PHL}	0.81	0.74 + 0.034*SL	0.75 + 0.028*SL	0.78 + 0.025*SL
	t_R	0.20	0.14 + 0.031*SL	0.13 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.27	0.18 + 0.043*SL	0.19 + 0.040*SL	0.20 + 0.038*SL
D to Y	t_{PLH}	0.66	0.61 + 0.023*SL	0.62 + 0.019*SL	0.64 + 0.017*SL
	t_{PHL}	0.86	0.79 + 0.034*SL	0.81 + 0.028*SL	0.83 + 0.025*SL
	t_R	0.20	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.27	0.18 + 0.042*SL	0.19 + 0.040*SL	0.20 + 0.038*SL
E to Y	t_{PLH}	0.80	0.76 + 0.023*SL	0.77 + 0.019*SL	0.78 + 0.017*SL
	t_{PHL}	0.92	0.85 + 0.034*SL	0.87 + 0.028*SL	0.89 + 0.025*SL
	t_R	0.21	0.15 + 0.031*SL	0.14 + 0.032*SL	0.13 + 0.033*SL
	t_F	0.27	0.18 + 0.043*SL	0.19 + 0.039*SL	0.20 + 0.038*SL
F to Y	t_{PLH}	0.78	0.73 + 0.023*SL	0.75 + 0.019*SL	0.76 + 0.017*SL
	t_{PHL}	0.87	0.81 + 0.034*SL	0.82 + 0.028*SL	0.85 + 0.025*SL
	t_R	0.21	0.14 + 0.031*SL	0.14 + 0.032*SL	0.13 + 0.033*SL
	t_F	0.27	0.18 + 0.043*SL	0.19 + 0.039*SL	0.20 + 0.038*SL
G to Y	t_{PLH}	0.68	0.64 + 0.023*SL	0.65 + 0.019*SL	0.66 + 0.017*SL
	t_{PHL}	0.85	0.78 + 0.034*SL	0.80 + 0.028*SL	0.82 + 0.025*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.032*SL	0.13 + 0.034*SL
	t_F	0.27	0.18 + 0.042*SL	0.19 + 0.039*SL	0.20 + 0.038*SL
H to Y	t_{PLH}	0.71	0.66 + 0.023*SL	0.67 + 0.019*SL	0.68 + 0.017*SL
	t_{PHL}	0.90	0.83 + 0.033*SL	0.85 + 0.028*SL	0.87 + 0.025*SL
	t_R	0.20	0.14 + 0.031*SL	0.14 + 0.033*SL	0.13 + 0.033*SL
	t_F	0.27	0.18 + 0.043*SL	0.20 + 0.039*SL	0.20 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

DL(1/2/3/4/5/10)D2/DL(1/2/3/4/5/10)D4

(1/2/3/4/5/10)ns Delay Cell with 2X/4X Drive

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)											
STD80											
DL1D2	*DL1D4*	*DL2D2*	*DL2D4*	*DL3D2*	*DL3D4*	*DL4D2*	*DL4D4*	*DL5D2*	*DL5D4*	*DL10D2*	*DL10D4*
A	A	A	A	A	A	A	A	A	A	A	A
0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.7	0.6	0.6	0.6
STDM80											
DL1D2	*DL1D4*	*DL2D2*	*DL2D4*	*DL3D2*	*DL3D4*	*DL4D2*	*DL4D4*	*DL5D2*	*DL5D4*	*DL10D2*	*DL10D4*
A	A	A	A	A	A	A	A	A	A	A	A
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
Gate Count											
STD80/STDM80											
DL1D2	*DL1D4*	*DL2D2*	*DL2D4*	*DL3D2*	*DL3D4*	*DL4D2*	*DL4D4*	*DL5D2*	*DL5D4*	*DL10D2*	*DL10D4*
3.7	4.3	4.3	5.0	4.7	5.3	5.3	6.0	5.7	6.3	7.3	8.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 DL1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.87	0.84 + 0.016*SL	0.85 + 0.013*SL	0.86 + 0.012*SL
	t_{PHL}	0.98	0.94 + 0.022*SL	0.94 + 0.019*SL	0.95 + 0.018*SL
	t_R	0.14	0.10 + 0.019*SL	0.09 + 0.024*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.029*SL	0.09 + 0.031*SL	0.07 + 0.034*SL

STD80 DL1D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.93	0.91 + 0.010*SL	0.92 + 0.008*SL	0.94 + 0.006*SL
	t_{PHL}	1.06	1.03 + 0.013*SL	1.04 + 0.011*SL	1.06 + 0.009*SL
	t_R	0.16	0.14 + 0.009*SL	0.14 + 0.010*SL	0.12 + 0.013*SL
	t_F	0.18	0.15 + 0.015*SL	0.15 + 0.015*SL	0.13 + 0.016*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 DL2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.48	1.45 + 0.017*SL	1.46 + 0.013*SL	1.46 + 0.012*SL
	t_{PHL}	1.84	1.80 + 0.023*SL	1.81 + 0.019*SL	1.81 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.18	0.11 + 0.031*SL	0.11 + 0.030*SL	0.08 + 0.034*SL

STD80 DL2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.55	1.53 + 0.011*SL	1.53 + 0.008*SL	1.55 + 0.006*SL
	t_{PHL}	1.93	1.90 + 0.013*SL	1.91 + 0.011*SL	1.93 + 0.009*SL
	t_R	0.17	0.16 + 0.008*SL	0.15 + 0.011*SL	0.13 + 0.012*SL
	t_F	0.19	0.17 + 0.013*SL	0.16 + 0.015*SL	0.15 + 0.016*SL

STD80 DL3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	2.07	2.04 + 0.018*SL	2.05 + 0.013*SL	2.06 + 0.012*SL
	t_{PHL}	2.67	2.63 + 0.023*SL	2.63 + 0.019*SL	2.64 + 0.018*SL
	t_R	0.17	0.12 + 0.021*SL	0.12 + 0.022*SL	0.09 + 0.026*SL
	t_F	0.20	0.14 + 0.029*SL	0.14 + 0.030*SL	0.10 + 0.034*SL

STD80 DL3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	2.14	2.12 + 0.012*SL	2.13 + 0.008*SL	2.15 + 0.006*SL
	t_{PHL}	2.76	2.74 + 0.013*SL	2.74 + 0.011*SL	2.76 + 0.009*SL
	t_R	0.19	0.17 + 0.009*SL	0.17 + 0.010*SL	0.14 + 0.012*SL
	t_F	0.21	0.18 + 0.015*SL	0.18 + 0.014*SL	0.16 + 0.016*SL

STD80 DL4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	2.60	2.56 + 0.018*SL	2.57 + 0.013*SL	2.59 + 0.012*SL
	t_{PHL}	3.57	3.52 + 0.023*SL	3.53 + 0.019*SL	3.55 + 0.018*SL
	t_R	0.17	0.14 + 0.019*SL	0.13 + 0.022*SL	0.09 + 0.026*SL
	t_F	0.22	0.16 + 0.029*SL	0.16 + 0.029*SL	0.12 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 DL4D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	2.67	2.65 + 0.012*SL	2.66 + 0.009*SL	2.68 + 0.006*SL
	t_{PHL}	3.68	3.65 + 0.014*SL	3.65 + 0.011*SL	3.68 + 0.009*SL
	t_R	0.20	0.18 + 0.009*SL	0.18 + 0.010*SL	0.16 + 0.012*SL
	t_F	0.23	0.20 + 0.016*SL	0.21 + 0.014*SL	0.19 + 0.016*SL

STD80 DL5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	3.20	3.16 + 0.019*SL	3.17 + 0.014*SL	3.19 + 0.012*SL
	t_{PHL}	4.78	4.73 + 0.025*SL	4.75 + 0.020*SL	4.76 + 0.018*SL
	t_R	0.19	0.15 + 0.019*SL	0.14 + 0.022*SL	0.10 + 0.026*SL
	t_F	0.25	0.20 + 0.027*SL	0.19 + 0.029*SL	0.15 + 0.033*SL

STD80 DL5D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	3.28	3.26 + 0.012*SL	3.26 + 0.009*SL	3.29 + 0.006*SL
	t_{PHL}	4.91	4.88 + 0.014*SL	4.88 + 0.011*SL	4.91 + 0.009*SL
	t_R	0.21	0.20 + 0.008*SL	0.19 + 0.010*SL	0.17 + 0.012*SL
	t_F	0.27	0.24 + 0.016*SL	0.24 + 0.014*SL	0.22 + 0.016*SL

STD80 DL10D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	5.98	5.94 + 0.022*SL	5.95 + 0.015*SL	5.98 + 0.012*SL
	t_{PHL}	10.71	10.65 + 0.030*SL	10.66 + 0.023*SL	10.71 + 0.018*SL
	t_R	0.24	0.20 + 0.019*SL	0.20 + 0.021*SL	0.15 + 0.025*SL
	t_F	0.39	0.32 + 0.033*SL	0.33 + 0.029*SL	0.30 + 0.032*SL

STD80 DL10D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	6.09	6.06 + 0.013*SL	6.07 + 0.010*SL	6.11 + 0.006*SL
	t_{PHL}	10.89	10.86 + 0.018*SL	10.87 + 0.013*SL	10.91 + 0.009*SL
	t_R	0.28	0.26 + 0.009*SL	0.26 + 0.009*SL	0.23 + 0.012*SL
	t_F	0.42	0.39 + 0.015*SL	0.39 + 0.014*SL	0.39 + 0.015*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 DL1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.29	1.24 + 0.021*SL	1.25 + 0.018*SL	1.26 + 0.017*SL
	t_{PHL}	1.50	1.44 + 0.029*SL	1.45 + 0.024*SL	1.47 + 0.022*SL
	t_R	0.18	0.12 + 0.032*SL	0.11 + 0.033*SL	0.11 + 0.035*SL
	t_F	0.20	0.12 + 0.039*SL	0.13 + 0.038*SL	0.12 + 0.038*SL

STDM80 DL1D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.36	1.33 + 0.014*SL	1.34 + 0.011*SL	1.35 + 0.010*SL
	t_{PHL}	1.61	1.57 + 0.017*SL	1.58 + 0.015*SL	1.59 + 0.013*SL
	t_R	0.19	0.15 + 0.017*SL	0.15 + 0.016*SL	0.15 + 0.017*SL
	t_F	0.21	0.17 + 0.020*SL	0.17 + 0.020*SL	0.18 + 0.019*SL

STDM80 DL2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	2.23	2.19 + 0.022*SL	2.20 + 0.019*SL	2.21 + 0.017*SL
	t_{PHL}	3.04	2.98 + 0.029*SL	2.99 + 0.025*SL	3.01 + 0.022*SL
	t_R	0.20	0.13 + 0.031*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.22	0.14 + 0.039*SL	0.15 + 0.037*SL	0.14 + 0.038*SL

STDM80 DL2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	2.32	2.29 + 0.015*SL	2.30 + 0.012*SL	2.31 + 0.010*SL
	t_{PHL}	3.16	3.13 + 0.018*SL	3.14 + 0.015*SL	3.15 + 0.014*SL
	t_R	0.20	0.18 + 0.012*SL	0.17 + 0.016*SL	0.17 + 0.016*SL
	t_F	0.24	0.19 + 0.022*SL	0.20 + 0.019*SL	0.20 + 0.019*SL

STDM80 DL3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	3.21	3.17 + 0.023*SL	3.18 + 0.019*SL	3.19 + 0.017*SL
	t_{PHL}	4.51	4.45 + 0.030*SL	4.46 + 0.025*SL	4.48 + 0.023*SL
	t_R	0.21	0.15 + 0.029*SL	0.14 + 0.032*SL	0.13 + 0.034*SL
	t_F	0.24	0.16 + 0.039*SL	0.17 + 0.036*SL	0.17 + 0.037*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 DL3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	3.31	3.28 + 0.014*SL	3.29 + 0.012*SL	3.30 + 0.010*SL
	t_{PHL}	4.65	4.61 + 0.018*SL	4.62 + 0.016*SL	4.63 + 0.014*SL
	t_R	0.22	0.19 + 0.015*SL	0.19 + 0.015*SL	0.18 + 0.016*SL
	t_F	0.25	0.21 + 0.020*SL	0.21 + 0.020*SL	0.23 + 0.018*SL

STDM80 DL4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	4.04	4.00 + 0.023*SL	4.01 + 0.019*SL	4.02 + 0.017*SL
	t_{PHL}	6.16	6.09 + 0.031*SL	6.11 + 0.026*SL	6.13 + 0.023*SL
	t_R	0.22	0.16 + 0.031*SL	0.15 + 0.032*SL	0.14 + 0.033*SL
	t_F	0.26	0.18 + 0.040*SL	0.19 + 0.036*SL	0.19 + 0.036*SL

STDM80 DL4D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	4.14	4.12 + 0.015*SL	4.12 + 0.012*SL	4.14 + 0.010*SL
	t_{PHL}	6.31	6.27 + 0.019*SL	6.28 + 0.016*SL	6.30 + 0.014*SL
	t_R	0.23	0.20 + 0.015*SL	0.20 + 0.015*SL	0.20 + 0.016*SL
	t_F	0.28	0.24 + 0.021*SL	0.24 + 0.020*SL	0.25 + 0.018*SL

STDM80 DL5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	4.95	4.91 + 0.024*SL	4.92 + 0.020*SL	4.94 + 0.017*SL
	t_{PHL}	8.44	8.38 + 0.033*SL	8.39 + 0.027*SL	8.42 + 0.023*SL
	t_R	0.23	0.17 + 0.031*SL	0.16 + 0.031*SL	0.16 + 0.032*SL
	t_F	0.29	0.21 + 0.040*SL	0.23 + 0.036*SL	0.23 + 0.036*SL

STDM80 DL5D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	5.06	5.03 + 0.015*SL	5.04 + 0.012*SL	5.05 + 0.011*SL
	t_{PHL}	8.61	8.58 + 0.019*SL	8.59 + 0.016*SL	8.60 + 0.014*SL
	t_R	0.24	0.21 + 0.013*SL	0.21 + 0.016*SL	0.21 + 0.015*SL
	t_F	0.31	0.27 + 0.020*SL	0.27 + 0.019*SL	0.28 + 0.018*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 DL10D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	9.35	9.29 + 0.027*SL	9.31 + 0.021*SL	9.33 + 0.018*SL
	t_{PHL}	19.69	19.61 + 0.038*SL	19.63 + 0.031*SL	19.66 + 0.027*SL
	t_R	0.27	0.21 + 0.030*SL	0.21 + 0.031*SL	0.20 + 0.031*SL
	t_F	0.42	0.34 + 0.042*SL	0.35 + 0.038*SL	0.36 + 0.036*SL

STDM80 DL10D4

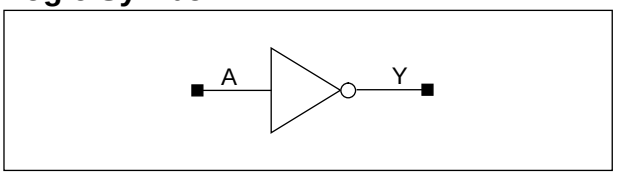
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	9.48	9.45 + 0.017*SL	9.46 + 0.014*SL	9.48 + 0.011*SL
	t_{PHL}	19.94	19.90 + 0.023*SL	19.91 + 0.019*SL	19.93 + 0.016*SL
	t_R	0.29	0.26 + 0.015*SL	0.26 + 0.015*SL	0.26 + 0.016*SL
	t_F	0.45	0.41 + 0.021*SL	0.41 + 0.020*SL	0.42 + 0.019*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

IV/IVD2/IVD3/IVD4/IVD6/IVD8

Inverter with 1X/2X/3X/4X/6X/8X Drive

Logic Symbol



Truth Table

A	Y
0	1
1	0

Cell Data

Input Load (SL)						Gate Count					
STD80											
IV	*IVD2*	*IVD3*	*IVD4*	*IVD6*	*IVD8*	*IV*	*IVD2*	*IVD3*	*IVD4*	*IVD6*	*IVD8*
A	A	A	A	A	A						
1.0	1.9	2.8	3.7	5.6	7.5	0.7	1.0	1.3	1.7	2.3	3.0
STDM80											
IV	*IVD2*	*IVD3*	*IVD4*	*IVD6*	*IVD8*	*IV*	*IVD2*	*IVD3*	*IVD4*	*IVD6*	*IVD8*
A	A	A	A	A	A						
1.0	2.1	3.0	4.0	6.0	8.0	0.7	1.0	1.3	1.7	2.3	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 IV

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.14	0.07 + 0.037*SL	0.10 + 0.026*SL	0.11 + 0.024*SL
	t_{PHL}	0.20	0.11 + 0.044*SL	0.13 + 0.036*SL	0.12 + 0.037*SL
	t_R	0.27	0.18 + 0.043*SL	0.18 + 0.044*SL	0.11 + 0.052*SL
	t_F	0.28	0.16 + 0.063*SL	0.16 + 0.061*SL	0.08 + 0.069*SL

STD80 IVD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.10	0.05 + 0.024*SL	0.07 + 0.016*SL	0.11 + 0.012*SL
	t_{PHL}	0.14	0.08 + 0.026*SL	0.10 + 0.020*SL	0.11 + 0.018*SL
	t_R	0.21	0.16 + 0.024*SL	0.17 + 0.021*SL	0.13 + 0.026*SL
	t_F	0.21	0.14 + 0.032*SL	0.15 + 0.028*SL	0.10 + 0.034*SL

STD80 IVD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.09	0.06 + 0.017*SL	0.07 + 0.012*SL	0.11 + 0.008*SL
	t_{PHL}	0.12	0.09 + 0.018*SL	0.10 + 0.014*SL	0.12 + 0.012*SL
	t_R	0.20	0.17 + 0.016*SL	0.17 + 0.015*SL	0.15 + 0.017*SL
	t_F	0.19	0.14 + 0.023*SL	0.15 + 0.019*SL	0.12 + 0.022*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 IVD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.08	0.05 + 0.014*SL	0.06 + 0.010*SL	0.10 + 0.006*SL
	t_{PHL}	0.11	0.08 + 0.014*SL	0.09 + 0.011*SL	0.11 + 0.009*SL
	t_R	0.19	0.16 + 0.011*SL	0.16 + 0.011*SL	0.15 + 0.012*SL
	t_F	0.17	0.14 + 0.018*SL	0.15 + 0.014*SL	0.13 + 0.016*SL

STD80 IVD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.07	0.05 + 0.010*SL	0.05 + 0.007*SL	0.09 + 0.004*SL
	t_{PHL}	0.10	0.08 + 0.011*SL	0.08 + 0.008*SL	0.11 + 0.006*SL
	t_R	0.18	0.16 + 0.008*SL	0.16 + 0.008*SL	0.16 + 0.008*SL
	t_F	0.16	0.14 + 0.012*SL	0.14 + 0.010*SL	0.14 + 0.010*SL

STD80 IVD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.06	0.05 + 0.008*SL	0.05 + 0.006*SL	0.08 + 0.003*SL
	t_{PHL}	0.09	0.08 + 0.008*SL	0.08 + 0.007*SL	0.10 + 0.004*SL
	t_R	0.17	0.16 + 0.008*SL	0.16 + 0.006*SL	0.17 + 0.006*SL
	t_F	0.16	0.14 + 0.009*SL	0.14 + 0.008*SL	0.14 + 0.008*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 IV

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.11 + 0.041*SL	0.13 + 0.033*SL	0.13 + 0.033*SL
	t_{PHL}	0.23	0.13 + 0.048*SL	0.15 + 0.044*SL	0.14 + 0.044*SL
	t_R	0.29	0.17 + 0.060*SL	0.16 + 0.066*SL	0.13 + 0.069*SL
	t_F	0.30	0.16 + 0.067*SL	0.13 + 0.078*SL	0.10 + 0.082*SL

STDM80 IVD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.13	0.08 + 0.026*SL	0.10 + 0.020*SL	0.12 + 0.017*SL
	t_{PHL}	0.15	0.09 + 0.030*SL	0.11 + 0.023*SL	0.13 + 0.021*SL
	t_R	0.21	0.15 + 0.030*SL	0.15 + 0.030*SL	0.13 + 0.033*SL
	t_F	0.20	0.12 + 0.037*SL	0.13 + 0.035*SL	0.11 + 0.038*SL

STDM80 IVD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.12	0.09 + 0.018*SL	0.10 + 0.015*SL	0.12 + 0.012*SL
	t_{PHL}	0.14	0.10 + 0.021*SL	0.11 + 0.017*SL	0.13 + 0.014*SL
	t_R	0.20	0.16 + 0.021*SL	0.16 + 0.019*SL	0.15 + 0.021*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.022*SL	0.13 + 0.024*SL

STDM80 IVD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.11	0.08 + 0.015*SL	0.09 + 0.012*SL	0.10 + 0.010*SL
	t_{PHL}	0.12	0.09 + 0.016*SL	0.10 + 0.014*SL	0.11 + 0.012*SL
	t_R	0.18	0.14 + 0.018*SL	0.15 + 0.015*SL	0.16 + 0.014*SL
	t_F	0.16	0.11 + 0.023*SL	0.14 + 0.016*SL	0.12 + 0.018*SL

STDM80 IVD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.10	0.08 + 0.011*SL	0.08 + 0.009*SL	0.09 + 0.008*SL
	t_{PHL}	0.11	0.09 + 0.012*SL	0.09 + 0.010*SL	0.10 + 0.009*SL
	t_R	0.17	0.15 + 0.011*SL	0.15 + 0.010*SL	0.15 + 0.010*SL
	t_F	0.15	0.11 + 0.016*SL	0.13 + 0.012*SL	0.14 + 0.011*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 IVD8

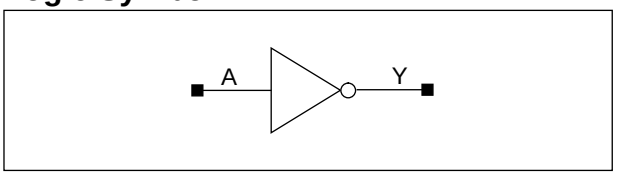
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.09	0.07 + 0.009*SL	0.08 + 0.007*SL	0.09 + 0.006*SL
	t_{PHL}	0.10	0.09 + 0.009*SL	0.09 + 0.008*SL	0.10 + 0.007*SL
	t_R	0.16	0.14 + 0.009*SL	0.15 + 0.008*SL	0.16 + 0.007*SL
	t_F	0.14	0.11 + 0.013*SL	0.12 + 0.010*SL	0.13 + 0.008*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

IVA/IVD2A/IVD3A/IVD4A

Inverter with (2X/4X/6X/8X) P-Transistor, (1X/2X/3X/4X) N-Transistor

Logic Symbol



Truth Table

A	Y
0	1
1	0

Cell Data

Input Load (SL)				Gate Count			
STD80							
IVA	*IVD2A*	*IVD3A*	*IVD4A*	*IVA*	*IVD2A*	*IVD3A*	*IVD4A*
A	A	A	A				
0.9	1.9	2.8	3.7	0.7	1.0	1.3	1.7
STDM80							
IVA	*IVD2A*	*IVD3A*	*IVD4A*	*IVA*	*IVD2A*	*IVD3A*	*IVD4A*
A	A	A	A				
1.0	2.0	3.0	4.0	0.7	1.0	1.3	1.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 IVA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.14	0.07 + 0.037*SL	0.10 + 0.026*SL	0.11 + 0.024*SL
	t_{PHL}	0.20	0.11 + 0.044*SL	0.13 + 0.036*SL	0.12 + 0.037*SL
	t_R	0.27	0.18 + 0.043*SL	0.18 + 0.044*SL	0.11 + 0.052*SL
	t_F	0.28	0.16 + 0.063*SL	0.16 + 0.061*SL	0.08 + 0.069*SL

STD80 IVD2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.10	0.05 + 0.024*SL	0.07 + 0.016*SL	0.11 + 0.012*SL
	t_{PHL}	0.14	0.08 + 0.026*SL	0.10 + 0.020*SL	0.11 + 0.018*SL
	t_R	0.21	0.16 + 0.024*SL	0.17 + 0.021*SL	0.13 + 0.026*SL
	t_F	0.21	0.14 + 0.032*SL	0.15 + 0.028*SL	0.10 + 0.034*SL

STD80 IVD3A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.09	0.06 + 0.017*SL	0.07 + 0.012*SL	0.11 + 0.008*SL
	t_{PHL}	0.12	0.09 + 0.018*SL	0.10 + 0.014*SL	0.12 + 0.012*SL
	t_R	0.20	0.17 + 0.016*SL	0.17 + 0.015*SL	0.15 + 0.017*SL
	t_F	0.19	0.14 + 0.023*SL	0.15 + 0.019*SL	0.12 + 0.022*SL

STD80 IVD4A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.08	0.05 + 0.014*SL	0.06 + 0.010*SL	0.10 + 0.006*SL
	t_{PHL}	0.11	0.08 + 0.014*SL	0.09 + 0.011*SL	0.11 + 0.009*SL
	t_R	0.19	0.16 + 0.011*SL	0.16 + 0.011*SL	0.15 + 0.012*SL
	t_F	0.17	0.14 + 0.018*SL	0.15 + 0.014*SL	0.13 + 0.016*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

IVA/IVD2A/IVD3A/IVD4A

Inverter with (2X/4X/6X/8X) P-Transistor, (1X/2X/3X/4X) N-Transistor

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 IVA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.11 + 0.041*SL	0.13 + 0.033*SL	0.13 + 0.033*SL
	t_{PHL}	0.23	0.13 + 0.048*SL	0.15 + 0.044*SL	0.14 + 0.044*SL
	t_R	0.29	0.17 + 0.060*SL	0.16 + 0.066*SL	0.13 + 0.069*SL
	t_F	0.30	0.16 + 0.067*SL	0.13 + 0.078*SL	0.10 + 0.082*SL

STDM80 IVD2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.13	0.08 + 0.026*SL	0.10 + 0.020*SL	0.12 + 0.017*SL
	t_{PHL}	0.15	0.09 + 0.030*SL	0.11 + 0.023*SL	0.13 + 0.021*SL
	t_R	0.21	0.15 + 0.030*SL	0.15 + 0.030*SL	0.13 + 0.033*SL
	t_F	0.20	0.12 + 0.037*SL	0.13 + 0.035*SL	0.11 + 0.038*SL

STD5M80 IVD3A

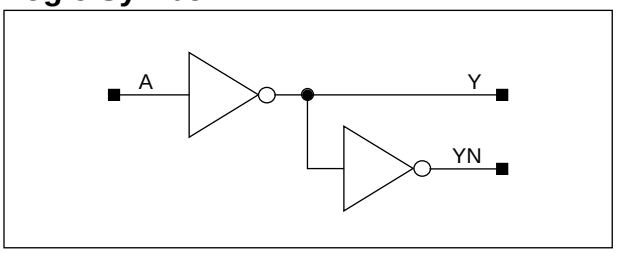
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.12	0.09 + 0.018*SL	0.10 + 0.015*SL	0.12 + 0.012*SL
	t_{PHL}	0.14	0.10 + 0.021*SL	0.11 + 0.017*SL	0.13 + 0.014*SL
	t_R	0.20	0.16 + 0.021*SL	0.16 + 0.019*SL	0.15 + 0.021*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.022*SL	0.13 + 0.024*SL

STDM80 IVD4A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.11	0.08 + 0.015*SL	0.09 + 0.012*SL	0.10 + 0.010*SL
	t_{PHL}	0.12	0.09 + 0.016*SL	0.10 + 0.014*SL	0.11 + 0.012*SL
	t_R	0.18	0.14 + 0.018*SL	0.15 + 0.015*SL	0.16 + 0.014*SL
	t_F	0.16	0.11 + 0.023*SL	0.14 + 0.016*SL	0.12 + 0.018*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	Y	YN
1	0	1
0	1	0

Cell Data

Input Load (SL)					Gate Count				
STD80									
IVCD11	*IVCD13*	*IVCD22*	*IVCD26*	*IVCD44*	*IVCD11*	*IVCD13*	*IVCD22*	*IVCD26*	*IVCD44*
A	A	A	A	A					
1.0	0.9	1.9	1.9	3.8	1.0	1.7	1.7	3.0	3.0
STDM80									
IVCD11	*IVCD13*	*IVCD22*	*IVCD26*	*IVCD44*	*IVCD11*	*IVCD13*	*IVCD22*	*IVCD26*	*IVCD44*
A	A	A	A	A					
1.0	1.0	2.0	2.0	4.0	1.0	1.7	1.7	3.0	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 IVCD11

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.18	0.11 + 0.032*SL	0.13 + 0.024*SL	0.14 + 0.024*SL
	t_{PHL}	0.23	0.15 + 0.040*SL	0.16 + 0.036*SL	0.15 + 0.037*SL
	t_R	0.31	0.23 + 0.037*SL	0.22 + 0.045*SL	0.15 + 0.052*SL
	t_F	0.34	0.23 + 0.053*SL	0.21 + 0.062*SL	0.15 + 0.069*SL
Y to YN	t_{PLH}	0.14	0.07 + 0.037*SL	0.10 + 0.026*SL	0.11 + 0.024*SL
	t_{PHL}	0.20	0.11 + 0.044*SL	0.13 + 0.036*SL	0.12 + 0.037*SL
	t_R	0.27	0.18 + 0.043*SL	0.18 + 0.044*SL	0.11 + 0.052*SL
	t_F	0.28	0.16 + 0.064*SL	0.16 + 0.061*SL	0.08 + 0.069*SL

STD80 IVCD13

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.18 + 0.027*SL	0.19 + 0.023*SL	0.18 + 0.024*SL
	t_{PHL}	0.29	0.22 + 0.034*SL	0.22 + 0.036*SL	0.21 + 0.037*SL
	t_R	0.42	0.33 + 0.045*SL	0.32 + 0.046*SL	0.27 + 0.052*SL
	t_F	0.49	0.37 + 0.059*SL	0.36 + 0.065*SL	0.31 + 0.069*SL
Y to YN	t_{PLH}	0.09	0.06 + 0.017*SL	0.07 + 0.012*SL	0.11 + 0.008*SL
	t_{PHL}	0.12	0.09 + 0.018*SL	0.10 + 0.014*SL	0.12 + 0.012*SL
	t_R	0.20	0.17 + 0.017*SL	0.17 + 0.014*SL	0.15 + 0.017*SL
	t_F	0.19	0.15 + 0.022*SL	0.15 + 0.019*SL	0.12 + 0.022*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 IVCD22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.14	0.10 + 0.018*SL	0.11 + 0.014*SL	0.13 + 0.012*SL
	t_{PHL}	0.17	0.13 + 0.022*SL	0.14 + 0.018*SL	0.14 + 0.018*SL
	t_R	0.26	0.23 + 0.018*SL	0.22 + 0.020*SL	0.17 + 0.026*SL
	t_F	0.28	0.23 + 0.025*SL	0.22 + 0.027*SL	0.16 + 0.034*SL
Y to YN	t_{PLH}	0.10	0.05 + 0.024*SL	0.07 + 0.016*SL	0.11 + 0.012*SL
	t_{PHL}	0.14	0.08 + 0.026*SL	0.10 + 0.020*SL	0.11 + 0.018*SL
	t_R	0.21	0.16 + 0.024*SL	0.17 + 0.021*SL	0.13 + 0.026*SL
	t_F	0.21	0.14 + 0.032*SL	0.15 + 0.028*SL	0.10 + 0.034*SL

STD80 IVCD26

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.17 + 0.013*SL	0.18 + 0.012*SL	0.18 + 0.012*SL
	t_{PHL}	0.24	0.20 + 0.018*SL	0.21 + 0.017*SL	0.20 + 0.018*SL
	t_R	0.36	0.31 + 0.023*SL	0.31 + 0.023*SL	0.29 + 0.026*SL
	t_F	0.41	0.35 + 0.030*SL	0.35 + 0.030*SL	0.31 + 0.034*SL
Y to YN	t_{PLH}	0.07	0.05 + 0.010*SL	0.05 + 0.007*SL	0.09 + 0.004*SL
	t_{PHL}	0.10	0.08 + 0.010*SL	0.08 + 0.008*SL	0.11 + 0.006*SL
	t_R	0.18	0.16 + 0.008*SL	0.16 + 0.008*SL	0.16 + 0.008*SL
	t_F	0.16	0.14 + 0.012*SL	0.14 + 0.010*SL	0.14 + 0.010*SL

STD80 IVCD44

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.12	0.10 + 0.009*SL	0.10 + 0.008*SL	0.13 + 0.006*SL
	t_{PHL}	0.15	0.13 + 0.011*SL	0.13 + 0.010*SL	0.14 + 0.009*SL
	t_R	0.24	0.22 + 0.010*SL	0.23 + 0.009*SL	0.19 + 0.012*SL
	t_F	0.25	0.22 + 0.013*SL	0.23 + 0.012*SL	0.19 + 0.016*SL
Y to YN	t_{PLH}	0.08	0.05 + 0.014*SL	0.06 + 0.010*SL	0.10 + 0.006*SL
	t_{PHL}	0.11	0.08 + 0.014*SL	0.09 + 0.011*SL	0.11 + 0.009*SL
	t_R	0.19	0.16 + 0.011*SL	0.16 + 0.011*SL	0.15 + 0.012*SL
	t_F	0.17	0.14 + 0.018*SL	0.15 + 0.014*SL	0.13 + 0.016*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 IVCD11

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.15 + 0.036*SL	0.16 + 0.033*SL	0.16 + 0.033*SL
	t_{PHL}	0.27	0.18 + 0.045*SL	0.18 + 0.044*SL	0.18 + 0.044*SL
	t_R	0.35	0.23 + 0.062*SL	0.21 + 0.067*SL	0.19 + 0.070*SL
	t_F	0.36	0.22 + 0.072*SL	0.20 + 0.079*SL	0.18 + 0.082*SL
Y to YN	t_{PLH}	0.19	0.11 + 0.041*SL	0.13 + 0.033*SL	0.13 + 0.033*SL
	t_{PHL}	0.23	0.13 + 0.048*SL	0.14 + 0.044*SL	0.14 + 0.044*SL
	t_R	0.29	0.17 + 0.061*SL	0.16 + 0.066*SL	0.13 + 0.069*SL
	t_F	0.30	0.16 + 0.067*SL	0.13 + 0.078*SL	0.11 + 0.082*SL

STDM80 IVCD13

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.23 + 0.033*SL	0.23 + 0.033*SL	0.23 + 0.033*SL
	t_{PHL}	0.33	0.25 + 0.044*SL	0.25 + 0.044*SL	0.24 + 0.044*SL
	t_R	0.51	0.37 + 0.067*SL	0.37 + 0.069*SL	0.36 + 0.070*SL
	t_F	0.56	0.40 + 0.078*SL	0.39 + 0.081*SL	0.38 + 0.082*SL
Y to YN	t_{PLH}	0.12	0.09 + 0.018*SL	0.10 + 0.015*SL	0.12 + 0.012*SL
	t_{PHL}	0.14	0.10 + 0.020*SL	0.11 + 0.017*SL	0.13 + 0.014*SL
	t_R	0.20	0.16 + 0.021*SL	0.16 + 0.019*SL	0.15 + 0.021*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.023*SL	0.13 + 0.023*SL

STDM80 IVCD22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.18	0.14 + 0.021*SL	0.15 + 0.018*SL	0.15 + 0.017*SL
	t_{PHL}	0.20	0.14 + 0.025*SL	0.16 + 0.022*SL	0.16 + 0.021*SL
	t_R	0.27	0.22 + 0.025*SL	0.20 + 0.032*SL	0.19 + 0.033*SL
	t_F	0.27	0.21 + 0.029*SL	0.19 + 0.036*SL	0.18 + 0.038*SL
Y to YN	t_{PLH}	0.13	0.08 + 0.026*SL	0.10 + 0.020*SL	0.12 + 0.017*SL
	t_{PHL}	0.15	0.09 + 0.030*SL	0.11 + 0.023*SL	0.13 + 0.021*SL
	t_R	0.21	0.15 + 0.030*SL	0.15 + 0.030*SL	0.13 + 0.033*SL
	t_F	0.20	0.12 + 0.038*SL	0.13 + 0.035*SL	0.11 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 IVCD26

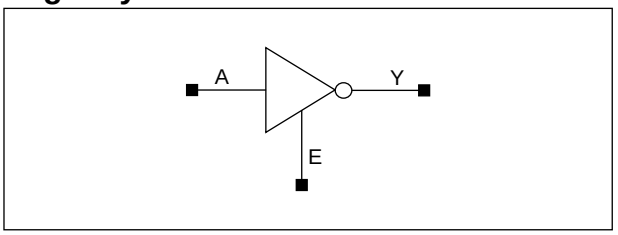
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.22 + 0.016*SL	0.22 + 0.016*SL	0.22 + 0.017*SL
	t_{PHL}	0.27	0.22 + 0.021*SL	0.22 + 0.021*SL	0.22 + 0.021*SL
	t_R	0.41	0.34 + 0.034*SL	0.35 + 0.034*SL	0.35 + 0.034*SL
	t_F	0.45	0.37 + 0.038*SL	0.37 + 0.038*SL	0.36 + 0.039*SL
Y to YN	t_{PLH}	0.10	0.08 + 0.011*SL	0.08 + 0.009*SL	0.09 + 0.008*SL
	t_{PHL}	0.11	0.09 + 0.012*SL	0.09 + 0.010*SL	0.10 + 0.009*SL
	t_R	0.17	0.15 + 0.011*SL	0.15 + 0.010*SL	0.15 + 0.010*SL
	t_F	0.15	0.11 + 0.016*SL	0.13 + 0.012*SL	0.14 + 0.011*SL

STDM80 IVCD44

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.16	0.13 + 0.011*SL	0.14 + 0.010*SL	0.15 + 0.009*SL
	t_{PHL}	0.17	0.14 + 0.014*SL	0.15 + 0.012*SL	0.15 + 0.011*SL
	t_R	0.25	0.23 + 0.009*SL	0.22 + 0.013*SL	0.20 + 0.016*SL
	t_F	0.24	0.21 + 0.015*SL	0.22 + 0.013*SL	0.19 + 0.018*SL
Y to YN	t_{PLH}	0.11	0.08 + 0.015*SL	0.09 + 0.012*SL	0.10 + 0.010*SL
	t_{PHL}	0.12	0.09 + 0.016*SL	0.10 + 0.014*SL	0.11 + 0.012*SL
	t_R	0.18	0.14 + 0.018*SL	0.15 + 0.015*SL	0.16 + 0.014*SL
	t_F	0.16	0.11 + 0.023*SL	0.14 + 0.016*SL	0.12 + 0.018*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	1
1	1	0

Cell Data

Input Load (SL)								Output Load (SL)				Gate Count			
STD80															
IVT		*IVTD2*		*IVTD4*		*IVTD8*		*IVT*	IVTD2	*IVTD4*	IVTD8	*IVT*	*IVTD2*	*IVTD4*	*IVTD8*
A	E	A	E	A	E	A	E	Y	Y	Y	Y				
0.7	1.1	0.7	1.4	0.7	2.2	0.7	3.7	0.9	1.7	4.8	9.7	2.3	3.0	4.3	7.0
STDM80															
IVT		*IVTD2*		*IVTD4*		*IVTD8*		*IVT*	IVTD2	*IVTD4*	IVTD8	*IVT*	*IVTD2*	*IVTD4*	*IVTD8*
A	E	A	E	A	E	A	E	Y	Y	Y	Y				
0.7	1.1	0.7	1.4	0.7	2.3	0.7	3.9	1.0	1.9	5.2	10.5	2.3	3.0	4.3	7.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 IVT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.39	0.35 + 0.019*SL	0.36 + 0.015*SL	0.39 + 0.012*SL
	t_{PHL}	0.42	0.34 + 0.039*SL	0.34 + 0.039*SL	0.35 + 0.039*SL
	t_R	0.18	0.13 + 0.023*SL	0.13 + 0.025*SL	0.10 + 0.027*SL
	t_F	0.26	0.11 + 0.074*SL	0.10 + 0.076*SL	0.09 + 0.078*SL
E to Y	t_{PLH}	0.26	0.22 + 0.020*SL	0.23 + 0.015*SL	0.26 + 0.012*SL
	t_{PHL}	0.17	0.05 + 0.057*SL	0.09 + 0.041*SL	0.11 + 0.039*SL
	t_R	0.19	0.15 + 0.021*SL	0.14 + 0.024*SL	0.11 + 0.027*SL
	t_F	0.31	0.17 + 0.070*SL	0.17 + 0.071*SL	0.11 + 0.078*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.36	0.36 + 0.000*SL	0.36 + 0.000*SL	0.36 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 IVTD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.46	0.43 + 0.013*SL	0.44 + 0.010*SL	0.47 + 0.006*SL
	t_{PHL}	0.47	0.43 + 0.020*SL	0.43 + 0.019*SL	0.43 + 0.019*SL
	t_R	0.21	0.18 + 0.013*SL	0.19 + 0.012*SL	0.17 + 0.013*SL
	t_F	0.21	0.14 + 0.035*SL	0.14 + 0.035*SL	0.11 + 0.039*SL
E to Y	t_{PLH}	0.33	0.30 + 0.013*SL	0.31 + 0.010*SL	0.34 + 0.006*SL
	t_{PHL}	0.10	0.04 + 0.034*SL	0.06 + 0.024*SL	0.10 + 0.019*SL
	t_R	0.22	0.19 + 0.013*SL	0.20 + 0.012*SL	0.18 + 0.013*SL
	t_F	0.24	0.16 + 0.040*SL	0.17 + 0.035*SL	0.13 + 0.039*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.51	0.51 + 0.001*SL	0.51 + 0.000*SL	0.51 + 0.000*SL

STD80 IVTD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.58	0.56 + 0.010*SL	0.57 + 0.008*SL	0.60 + 0.004*SL
	t_{PHL}	0.66	0.63 + 0.013*SL	0.64 + 0.011*SL	0.65 + 0.010*SL
	t_R	0.29	0.28 + 0.006*SL	0.28 + 0.007*SL	0.28 + 0.006*SL
	t_F	0.27	0.24 + 0.013*SL	0.23 + 0.016*SL	0.21 + 0.019*SL
E to Y	t_{PLH}	0.46	0.44 + 0.010*SL	0.44 + 0.008*SL	0.48 + 0.004*SL
	t_{PHL}	0.06	0.02 + 0.017*SL	0.03 + 0.013*SL	0.06 + 0.010*SL
	t_R	0.29	0.28 + 0.007*SL	0.28 + 0.007*SL	0.28 + 0.006*SL
	t_F	0.19	0.15 + 0.019*SL	0.15 + 0.018*SL	0.15 + 0.019*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.73	0.73 + 0.000*SL	0.73 + 0.000*SL	0.73 + 0.000*SL

STD80 IVTD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.87	0.86 + 0.006*SL	0.86 + 0.006*SL	0.88 + 0.003*SL
	t_{PHL}	1.04	1.03 + 0.007*SL	1.03 + 0.007*SL	1.05 + 0.005*SL
	t_R	0.51	0.51 + 0.001*SL	0.51 + 0.002*SL	0.50 + 0.003*SL
	t_F	0.45	0.44 + 0.005*SL	0.44 + 0.006*SL	0.42 + 0.008*SL
E to Y	t_{PLH}	0.75	0.74 + 0.006*SL	0.74 + 0.005*SL	0.76 + 0.003*SL
	t_{PHL}	0.04	0.02 + 0.009*SL	0.02 + 0.008*SL	0.05 + 0.005*SL
	t_R	0.51	0.51 + 0.001*SL	0.51 + 0.002*SL	0.50 + 0.003*SL
	t_F	0.18	0.16 + 0.008*SL	0.16 + 0.010*SL	0.16 + 0.009*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	1.26	1.26 + 0.001*SL	1.26 + 0.000*SL	1.26 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 IVT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.53	0.48 + 0.025*SL	0.49 + 0.021*SL	0.51 + 0.019*SL
	t_{PHL}	0.57	0.47 + 0.053*SL	0.47 + 0.051*SL	0.48 + 0.050*SL
	t_R	0.23	0.16 + 0.034*SL	0.16 + 0.035*SL	0.16 + 0.035*SL
	t_F	0.34	0.16 + 0.095*SL	0.15 + 0.097*SL	0.14 + 0.099*SL
E to Y	t_{PLH}	0.37	0.32 + 0.025*SL	0.33 + 0.021*SL	0.35 + 0.019*SL
	t_{PHL}	0.25	0.14 + 0.055*SL	0.15 + 0.051*SL	0.15 + 0.050*SL
	t_R	0.24	0.16 + 0.036*SL	0.17 + 0.034*SL	0.16 + 0.035*SL
	t_F	0.35	0.18 + 0.089*SL	0.16 + 0.095*SL	0.13 + 0.099*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.46	0.46 + 0.000*SL	0.46 + 0.000*SL	0.46 + 0.000*SL

STDM80 IVTD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.62	0.59 + 0.017*SL	0.60 + 0.014*SL	0.61 + 0.012*SL
	t_{PHL}	0.64	0.59 + 0.028*SL	0.59 + 0.027*SL	0.60 + 0.025*SL
	t_R	0.25	0.21 + 0.019*SL	0.22 + 0.018*SL	0.22 + 0.018*SL
	t_F	0.27	0.18 + 0.046*SL	0.18 + 0.046*SL	0.17 + 0.048*SL
E to Y	t_{PLH}	0.46	0.42 + 0.017*SL	0.43 + 0.014*SL	0.45 + 0.012*SL
	t_{PHL}	0.18	0.12 + 0.032*SL	0.13 + 0.026*SL	0.14 + 0.026*SL
	t_R	0.25	0.22 + 0.018*SL	0.22 + 0.018*SL	0.22 + 0.018*SL
	t_F	0.26	0.17 + 0.044*SL	0.17 + 0.046*SL	0.15 + 0.047*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.67	0.67 + 0.000*SL	0.67 + 0.000*SL	0.67 + 0.000*SL

STDM80 IVTD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.79	0.77 + 0.013*SL	0.77 + 0.011*SL	0.79 + 0.009*SL
	t_{PHL}	0.89	0.86 + 0.017*SL	0.86 + 0.016*SL	0.87 + 0.015*SL
	t_R	0.33	0.31 + 0.010*SL	0.31 + 0.010*SL	0.32 + 0.010*SL
	t_F	0.32	0.27 + 0.024*SL	0.28 + 0.023*SL	0.27 + 0.024*SL
E to Y	t_{PLH}	0.64	0.61 + 0.013*SL	0.62 + 0.011*SL	0.63 + 0.009*SL
	t_{PHL}	0.13	0.10 + 0.018*SL	0.10 + 0.015*SL	0.11 + 0.014*SL
	t_R	0.33	0.31 + 0.010*SL	0.31 + 0.010*SL	0.32 + 0.010*SL
	t_F	0.21	0.17 + 0.024*SL	0.16 + 0.025*SL	0.17 + 0.024*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.97	0.97 + 0.000*SL	0.97 + 0.000*SL	0.97 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

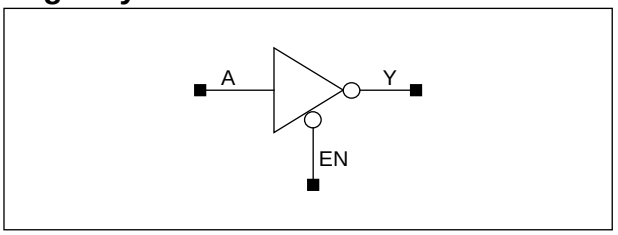
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 IVTD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.19	1.17 + 0.008*SL	1.17 + 0.008*SL	1.18 + 0.007*SL
	t_{PHL}	1.40	1.38 + 0.010*SL	1.38 + 0.009*SL	1.39 + 0.009*SL
	t_R	0.56	0.55 + 0.004*SL	0.55 + 0.005*SL	0.55 + 0.005*SL
	t_F	0.50	0.48 + 0.010*SL	0.48 + 0.011*SL	0.48 + 0.011*SL
E to Y	t_{PLH}	1.05	1.03 + 0.008*SL	1.03 + 0.008*SL	1.04 + 0.007*SL
	t_{PHL}	0.11	0.09 + 0.009*SL	0.10 + 0.009*SL	0.10 + 0.008*SL
	t_R	0.56	0.55 + 0.003*SL	0.54 + 0.005*SL	0.55 + 0.005*SL
	t_F	0.19	0.17 + 0.013*SL	0.17 + 0.012*SL	0.17 + 0.013*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	1.69	1.69 + 0.000*SL	1.69 + 0.000*SL	1.69 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	EN	Y
x	1	Hi-Z
0	0	1
1	0	0

Cell Data

Input Load (SL)								Output Load (SL)			
STD80											
IVTN		*IVTND2*		*IVTND4*		*IVTND8*		*IVTN*	*IVTND2*	*IVTND4*	*IVTND8*
A	EN	A	EN	A	EN	A	EN	Y	Y	Y	Y
0.8	0.7	0.8	0.7	0.8	0.7	0.8	0.7	1.3	2.4	4.8	9.8
STDM80											
IVTN		*IVTND2*		*IVTND4*		*IVTND8*		*IVTN*	*IVTND2*	*IVTND4*	*IVTND8*
A	EN	A	EN	A	EN	A	EN	Y	Y	Y	Y
0.8	0.7	0.8	0.7	0.8	0.7	0.8	0.7	1.4	2.6	5.2	10.6

STD80/STDM80			
Gate Count			
IVTN	*IVTND2*	*IVTND4*	*IVTND8*
2.7	3.3	4.7	7.3

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 IVTN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.38	0.34 + 0.020*SL	0.35 + 0.015*SL	0.38 + 0.012*SL
	t_{PHL}	0.44	0.36 + 0.040*SL	0.36 + 0.039*SL	0.36 + 0.039*SL
	t_R	0.17	0.12 + 0.023*SL	0.12 + 0.025*SL	0.09 + 0.027*SL
	t_F	0.27	0.12 + 0.072*SL	0.11 + 0.076*SL	0.10 + 0.078*SL
EN to Y	t_{PLH}	0.41	0.37 + 0.020*SL	0.38 + 0.015*SL	0.40 + 0.012*SL
	t_{PHL}	0.31	0.22 + 0.044*SL	0.23 + 0.040*SL	0.25 + 0.039*SL
	t_R	0.17	0.12 + 0.026*SL	0.12 + 0.024*SL	0.09 + 0.027*SL
	t_F	0.26	0.11 + 0.074*SL	0.11 + 0.077*SL	0.10 + 0.078*SL
	t_{PLZ}	0.16	0.16 + 0.000*SL	0.16 + 0.000*SL	0.17 + 0.000*SL
	t_{PHZ}	0.38	0.38 + 0.001*SL	0.38 + 0.000*SL	0.38 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 IVTND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.44	0.41 + 0.015*SL	0.42 + 0.011*SL	0.46 + 0.006*SL
	t_{PHL}	0.49	0.45 + 0.022*SL	0.45 + 0.020*SL	0.45 + 0.019*SL
	t_R	0.19	0.16 + 0.014*SL	0.17 + 0.012*SL	0.16 + 0.013*SL
	t_F	0.22	0.15 + 0.036*SL	0.15 + 0.036*SL	0.12 + 0.039*SL
EN to Y	t_{PLH}	0.49	0.46 + 0.015*SL	0.47 + 0.010*SL	0.50 + 0.006*SL
	t_{PHL}	0.28	0.23 + 0.023*SL	0.23 + 0.021*SL	0.25 + 0.019*SL
	t_R	0.19	0.17 + 0.011*SL	0.17 + 0.013*SL	0.16 + 0.013*SL
	t_F	0.18	0.11 + 0.036*SL	0.11 + 0.038*SL	0.10 + 0.039*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.53	0.53 + 0.001*SL	0.53 + 0.000*SL	0.54 + 0.000*SL

STD80 IVTND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.57	0.55 + 0.010*SL	0.56 + 0.008*SL	0.60 + 0.004*SL
	t_{PHL}	0.66	0.64 + 0.013*SL	0.64 + 0.011*SL	0.66 + 0.009*SL
	t_R	0.29	0.27 + 0.007*SL	0.28 + 0.006*SL	0.28 + 0.006*SL
	t_F	0.27	0.24 + 0.013*SL	0.24 + 0.016*SL	0.21 + 0.019*SL
EN to Y	t_{PLH}	0.67	0.65 + 0.009*SL	0.65 + 0.008*SL	0.69 + 0.004*SL
	t_{PHL}	0.28	0.25 + 0.014*SL	0.26 + 0.012*SL	0.28 + 0.010*SL
	t_R	0.29	0.28 + 0.006*SL	0.28 + 0.007*SL	0.28 + 0.006*SL
	t_F	0.16	0.12 + 0.018*SL	0.12 + 0.019*SL	0.12 + 0.019*SL
	t_{PLZ}	0.29	0.29 + 0.000*SL	0.29 + 0.000*SL	0.29 + 0.000*SL
	t_{PHZ}	0.84	0.84 + 0.001*SL	0.84 + 0.000*SL	0.84 + 0.000*SL

STD80 IVTND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.87	0.86 + 0.006*SL	0.86 + 0.005*SL	0.88 + 0.003*SL
	t_{PHL}	1.05	1.04 + 0.008*SL	1.04 + 0.007*SL	1.06 + 0.005*SL
	t_R	0.51	0.51 + 0.001*SL	0.51 + 0.002*SL	0.50 + 0.003*SL
	t_F	0.46	0.45 + 0.004*SL	0.45 + 0.006*SL	0.43 + 0.008*SL
EN to Y	t_{PLH}	1.06	1.05 + 0.006*SL	1.05 + 0.005*SL	1.07 + 0.003*SL
	t_{PHL}	0.32	0.30 + 0.008*SL	0.31 + 0.007*SL	0.33 + 0.005*SL
	t_R	0.52	0.52 + 0.001*SL	0.51 + 0.002*SL	0.50 + 0.003*SL
	t_F	0.17	0.15 + 0.011*SL	0.15 + 0.010*SL	0.15 + 0.010*SL
	t_{PLZ}	0.41	0.41 + 0.000*SL	0.41 + 0.000*SL	0.41 + 0.000*SL
	t_{PHZ}	1.47	1.47 + 0.000*SL	1.47 + 0.000*SL	1.47 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 IVTN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.52	0.46 + 0.027*SL	0.48 + 0.022*SL	0.50 + 0.019*SL
	t_{PHL}	0.60	0.49 + 0.054*SL	0.50 + 0.051*SL	0.51 + 0.050*SL
	t_R	0.22	0.15 + 0.036*SL	0.15 + 0.036*SL	0.15 + 0.036*SL
	t_F	0.36	0.17 + 0.095*SL	0.16 + 0.097*SL	0.15 + 0.099*SL
EN to Y	t_{PLH}	0.55	0.49 + 0.027*SL	0.51 + 0.022*SL	0.53 + 0.019*SL
	t_{PHL}	0.42	0.31 + 0.055*SL	0.32 + 0.052*SL	0.32 + 0.051*SL
	t_R	0.22	0.15 + 0.036*SL	0.15 + 0.035*SL	0.15 + 0.035*SL
	t_F	0.34	0.15 + 0.096*SL	0.14 + 0.099*SL	0.14 + 0.099*SL
	t_{PLZ}	0.25	0.25 + 0.000*SL	0.25 + 0.000*SL	0.25 + 0.000*SL
	t_{PHZ}	0.52	0.52 + 0.000*SL	0.52 + 0.000*SL	0.51 + 0.000*SL

STDM80 IVTND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.60	0.56 + 0.019*SL	0.57 + 0.015*SL	0.59 + 0.013*SL
	t_{PHL}	0.67	0.61 + 0.030*SL	0.62 + 0.027*SL	0.63 + 0.026*SL
	t_R	0.23	0.19 + 0.020*SL	0.20 + 0.018*SL	0.20 + 0.018*SL
	t_F	0.28	0.18 + 0.050*SL	0.19 + 0.047*SL	0.19 + 0.048*SL
EN to Y	t_{PLH}	0.66	0.62 + 0.019*SL	0.63 + 0.015*SL	0.65 + 0.012*SL
	t_{PHL}	0.37	0.31 + 0.030*SL	0.32 + 0.028*SL	0.33 + 0.026*SL
	t_R	0.24	0.19 + 0.020*SL	0.20 + 0.018*SL	0.20 + 0.018*SL
	t_F	0.24	0.14 + 0.049*SL	0.15 + 0.049*SL	0.14 + 0.049*SL
	t_{PLZ}	0.28	0.28 + 0.001*SL	0.28 + 0.000*SL	0.28 + 0.000*SL
	t_{PHZ}	0.72	0.72 + 0.000*SL	0.72 + 0.000*SL	0.72 + 0.000*SL

STDM80 IVTND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.78	0.76 + 0.013*SL	0.76 + 0.011*SL	0.78 + 0.009*SL
	t_{PHL}	0.90	0.87 + 0.017*SL	0.87 + 0.016*SL	0.88 + 0.015*SL
	t_R	0.33	0.31 + 0.010*SL	0.31 + 0.010*SL	0.32 + 0.009*SL
	t_F	0.33	0.28 + 0.023*SL	0.28 + 0.024*SL	0.28 + 0.023*SL
EN to Y	t_{PLH}	0.91	0.88 + 0.013*SL	0.89 + 0.011*SL	0.90 + 0.009*SL
	t_{PHL}	0.38	0.35 + 0.017*SL	0.35 + 0.016*SL	0.36 + 0.015*SL
	t_R	0.33	0.31 + 0.009*SL	0.31 + 0.010*SL	0.31 + 0.010*SL
	t_F	0.21	0.16 + 0.025*SL	0.16 + 0.026*SL	0.16 + 0.025*SL
	t_{PLZ}	0.34	0.34 + 0.000*SL	0.34 + 0.000*SL	0.34 + 0.000*SL
	t_{PHZ}	1.13	1.13 + 0.000*SL	1.13 + 0.000*SL	1.13 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

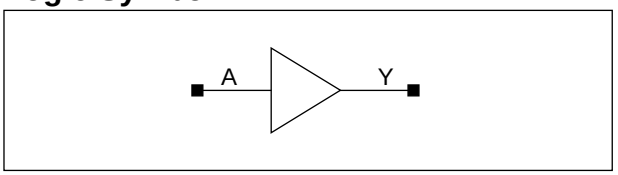
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 IVTND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.19	1.17 + 0.009*SL	1.17 + 0.008*SL	1.18 + 0.007*SL
	t_{PHL}	1.42	1.40 + 0.011*SL	1.40 + 0.009*SL	1.41 + 0.009*SL
	t_R	0.56	0.55 + 0.004*SL	0.55 + 0.005*SL	0.55 + 0.005*SL
	t_F	0.52	0.50 + 0.009*SL	0.49 + 0.011*SL	0.50 + 0.010*SL
EN to Y	t_{PLH}	1.46	1.44 + 0.009*SL	1.44 + 0.007*SL	1.45 + 0.007*SL
	t_{PHL}	0.45	0.43 + 0.010*SL	0.43 + 0.009*SL	0.43 + 0.009*SL
	t_R	0.57	0.56 + 0.004*SL	0.56 + 0.005*SL	0.55 + 0.005*SL
	t_F	0.22	0.19 + 0.014*SL	0.19 + 0.014*SL	0.20 + 0.014*SL
	t_{PLZ}	0.49	0.49 + 0.000*SL	0.49 + 0.000*SL	0.49 + 0.000*SL
	t_{PHZ}	1.98	1.98 + 0.000*SL	1.98 + 0.000*SL	1.98 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)						Gate Count					
STD80											
NID	*NID2*	*NID3*	*NID4*	*NID6*	*NID8*	*NID*	*NID2*	*NID3*	*NID4*	*NID6*	*NID8*
A	A	A	A	A	A						
0.7	0.6	0.7	1.3	1.3	1.3	1.0	1.3	1.7	2.3	3.0	3.7
STDM80											
NID	*NID2*	*NID3*	*NID4*	*NID6*	*NID8*	*NID*	*NID2*	*NID3*	*NID4*	*NID6*	*NID8*
A	A	A	A	A	A						
0.8	0.8	0.8	1.5	1.5	1.5	1.0	1.3	1.7	2.3	3.0	3.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NID

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.17 + 0.026*SL	0.17 + 0.024*SL	0.17 + 0.024*SL
	t_{PHL}	0.32	0.24 + 0.039*SL	0.24 + 0.037*SL	0.24 + 0.037*SL
	t_R	0.19	0.10 + 0.047*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.09 + 0.067*SL	0.06 + 0.069*SL

STD80 NID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.20 + 0.017*SL	0.21 + 0.013*SL	0.22 + 0.012*SL
	t_{PHL}	0.32	0.28 + 0.021*SL	0.28 + 0.019*SL	0.29 + 0.018*SL
	t_R	0.15	0.10 + 0.024*SL	0.11 + 0.022*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

STD80 NID3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.27	0.25 + 0.012*SL	0.25 + 0.009*SL	0.27 + 0.008*SL
	t_{PHL}	0.36	0.33 + 0.015*SL	0.34 + 0.013*SL	0.35 + 0.012*SL
	t_R	0.16	0.13 + 0.012*SL	0.13 + 0.015*SL	0.10 + 0.017*SL
	t_F	0.16	0.12 + 0.020*SL	0.12 + 0.020*SL	0.10 + 0.022*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NID4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.18 + 0.009*SL	0.19 + 0.007*SL	0.20 + 0.006*SL
	t_{PHL}	0.29	0.27 + 0.011*SL	0.27 + 0.010*SL	0.28 + 0.009*SL
	t_R	0.13	0.11 + 0.010*SL	0.10 + 0.011*SL	0.08 + 0.013*SL
	t_F	0.12	0.10 + 0.011*SL	0.09 + 0.015*SL	0.08 + 0.017*SL

STD80 NID6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.22 + 0.008*SL	0.23 + 0.005*SL	0.24 + 0.004*SL
	t_{PHL}	0.33	0.32 + 0.008*SL	0.32 + 0.007*SL	0.33 + 0.006*SL
	t_R	0.14	0.12 + 0.008*SL	0.13 + 0.007*SL	0.11 + 0.008*SL
	t_F	0.13	0.11 + 0.010*SL	0.11 + 0.010*SL	0.10 + 0.011*SL

STD80 NID8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.27	0.26 + 0.006*SL	0.26 + 0.004*SL	0.28 + 0.003*SL
	t_{PHL}	0.38	0.36 + 0.007*SL	0.37 + 0.006*SL	0.38 + 0.005*SL
	t_R	0.15	0.15 + 0.002*SL	0.14 + 0.005*SL	0.13 + 0.006*SL
	t_F	0.15	0.14 + 0.008*SL	0.14 + 0.007*SL	0.13 + 0.008*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NID

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.22 + 0.035*SL	0.22 + 0.034*SL	0.23 + 0.033*SL
	t_{PHL}	0.40	0.31 + 0.048*SL	0.31 + 0.045*SL	0.32 + 0.044*SL
	t_R	0.25	0.12 + 0.066*SL	0.11 + 0.071*SL	0.10 + 0.072*SL
	t_F	0.27	0.12 + 0.079*SL	0.11 + 0.082*SL	0.10 + 0.083*SL

STDM80 NID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.26 + 0.021*SL	0.27 + 0.018*SL	0.27 + 0.017*SL
	t_{PHL}	0.40	0.35 + 0.028*SL	0.36 + 0.024*SL	0.37 + 0.022*SL
	t_R	0.18	0.11 + 0.033*SL	0.11 + 0.033*SL	0.10 + 0.035*SL
	t_F	0.19	0.12 + 0.039*SL	0.12 + 0.039*SL	0.12 + 0.038*SL

STDM80 NID3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.34	0.30 + 0.016*SL	0.31 + 0.013*SL	0.32 + 0.012*SL
	t_{PHL}	0.46	0.42 + 0.021*SL	0.43 + 0.018*SL	0.44 + 0.016*SL
	t_R	0.18	0.14 + 0.023*SL	0.14 + 0.022*SL	0.14 + 0.022*SL
	t_F	0.20	0.15 + 0.027*SL	0.16 + 0.025*SL	0.16 + 0.024*SL

STDM80 NID4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.23 + 0.012*SL	0.24 + 0.010*SL	0.24 + 0.009*SL
	t_{PHL}	0.35	0.32 + 0.015*SL	0.33 + 0.013*SL	0.34 + 0.012*SL
	t_R	0.14	0.11 + 0.017*SL	0.11 + 0.016*SL	0.11 + 0.017*SL
	t_F	0.15	0.10 + 0.022*SL	0.11 + 0.019*SL	0.11 + 0.019*SL

STDM80 NID6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.27 + 0.009*SL	0.28 + 0.007*SL	0.28 + 0.007*SL
	t_{PHL}	0.41	0.39 + 0.011*SL	0.39 + 0.010*SL	0.40 + 0.009*SL
	t_R	0.15	0.13 + 0.008*SL	0.12 + 0.011*SL	0.12 + 0.011*SL
	t_F	0.16	0.13 + 0.013*SL	0.13 + 0.014*SL	0.14 + 0.013*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

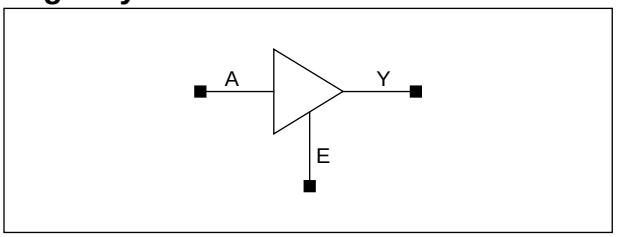
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NID8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.33	0.32 + 0.007*SL	0.32 + 0.006*SL	0.32 + 0.006*SL
	t_{PHL}	0.47	0.46 + 0.009*SL	0.46 + 0.008*SL	0.46 + 0.008*SL
	t_R	0.16	0.14 + 0.009*SL	0.15 + 0.008*SL	0.14 + 0.009*SL
	t_F	0.18	0.16 + 0.011*SL	0.16 + 0.011*SL	0.17 + 0.010*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	0
1	1	1

Cell Data

Input Load (SL)								Output Load (SL)				Gate Count			
STD80															
NIT		*NITD2*		*NITD4*		*NITD8*		*NIT*	*NITD2*	*NITD4*	*NITD8*	*NIT*	*NITD2*	*NITD4*	*NITD8*
A	E	A	E	A	E	A	E	Y	Y	Y	Y				
0.8	0.9	0.7	1.0	0.8	1.8	0.8	2.9	0.9	1.7	4.1	8.2	1.7	2.3	3.7	6.3
STDM80															
NIT		*NITD2*		*NITD4*		*NITD8*		*NIT*	*NITD2*	*NITD4*	*NITD8*	*NIT*	*NITD2*	*NITD4*	*NITD8*
A	E	A	E	A	E	A	E	Y	Y	Y	Y				
0.6	1.1	0.5	1.4	0.6	2.2	0.6	3.7	1.0	1.9	4.5	9.0	1.7	2.3	3.7	6.3

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NIT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.25 + 0.019*SL	0.26 + 0.015*SL	0.28 + 0.012*SL
	t_{PHL}	0.38	0.30 + 0.039*SL	0.30 + 0.038*SL	0.30 + 0.039*SL
	t_R	0.19	0.14 + 0.024*SL	0.14 + 0.023*SL	0.11 + 0.027*SL
	t_F	0.26	0.12 + 0.071*SL	0.11 + 0.076*SL	0.09 + 0.078*SL
E to Y	t_{PLH}	0.26	0.22 + 0.020*SL	0.23 + 0.015*SL	0.26 + 0.012*SL
	t_{PHL}	0.17	0.06 + 0.057*SL	0.09 + 0.041*SL	0.12 + 0.039*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.024*SL	0.11 + 0.027*SL
	t_F	0.31	0.17 + 0.070*SL	0.17 + 0.072*SL	0.11 + 0.078*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.36	0.36 + -0.002*SL	0.36 + 0.000*SL	0.36 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NITD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.33 + 0.013*SL	0.34 + 0.010*SL	0.37 + 0.006*SL
	t_{PHL}	0.43	0.40 + 0.019*SL	0.40 + 0.019*SL	0.39 + 0.019*SL
	t_R	0.22	0.19 + 0.012*SL	0.19 + 0.011*SL	0.18 + 0.013*SL
	t_F	0.21	0.15 + 0.032*SL	0.14 + 0.035*SL	0.11 + 0.039*SL
E to Y	t_{PLH}	0.33	0.30 + 0.013*SL	0.31 + 0.010*SL	0.35 + 0.006*SL
	t_{PHL}	0.10	0.04 + 0.034*SL	0.06 + 0.024*SL	0.10 + 0.019*SL
	t_R	0.22	0.19 + 0.014*SL	0.20 + 0.011*SL	0.19 + 0.013*SL
	t_F	0.24	0.15 + 0.041*SL	0.17 + 0.035*SL	0.13 + 0.039*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.52	0.52 + 0.001*SL	0.52 + 0.000*SL	0.52 + 0.000*SL

STD80 NITD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.48	0.47 + 0.009*SL	0.47 + 0.007*SL	0.50 + 0.004*SL
	t_{PHL}	0.61	0.58 + 0.012*SL	0.59 + 0.010*SL	0.59 + 0.009*SL
	t_R	0.30	0.29 + 0.005*SL	0.29 + 0.006*SL	0.29 + 0.006*SL
	t_F	0.27	0.24 + 0.013*SL	0.24 + 0.015*SL	0.20 + 0.019*SL
E to Y	t_{PLH}	0.47	0.45 + 0.009*SL	0.45 + 0.007*SL	0.49 + 0.004*SL
	t_{PHL}	0.06	0.02 + 0.018*SL	0.03 + 0.014*SL	0.07 + 0.010*SL
	t_R	0.30	0.29 + 0.004*SL	0.29 + 0.007*SL	0.29 + 0.006*SL
	t_F	0.20	0.15 + 0.022*SL	0.16 + 0.018*SL	0.15 + 0.019*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.40	0.40 + 0.000*SL	0.40 + 0.000*SL	0.40 + 0.000*SL

STD80 NITD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.77	0.76 + 0.006*SL	0.76 + 0.005*SL	0.78 + 0.003*SL
	t_{PHL}	0.98	0.96 + 0.008*SL	0.97 + 0.006*SL	0.98 + 0.005*SL
	t_R	0.53	0.53 + 0.000*SL	0.53 + 0.002*SL	0.51 + 0.003*SL
	t_F	0.46	0.45 + 0.003*SL	0.45 + 0.006*SL	0.42 + 0.008*SL
E to Y	t_{PLH}	0.76	0.75 + 0.006*SL	0.75 + 0.005*SL	0.77 + 0.003*SL
	t_{PHL}	0.04	0.02 + 0.009*SL	0.02 + 0.008*SL	0.05 + 0.005*SL
	t_R	0.53	0.53 + 0.001*SL	0.53 + 0.002*SL	0.51 + 0.003*SL
	t_F	0.18	0.15 + 0.013*SL	0.16 + 0.010*SL	0.16 + 0.009*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	1.34	1.34 + 0.000*SL	1.34 + 0.000*SL	1.34 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NIT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.38	0.33 + 0.025*SL	0.34 + 0.021*SL	0.36 + 0.019*SL
	t_{PHL}	0.49	0.39 + 0.053*SL	0.39 + 0.051*SL	0.40 + 0.050*SL
	t_R	0.23	0.16 + 0.037*SL	0.16 + 0.035*SL	0.16 + 0.035*SL
	t_F	0.34	0.15 + 0.095*SL	0.15 + 0.097*SL	0.14 + 0.099*SL
E to Y	t_{PLH}	0.37	0.31 + 0.026*SL	0.33 + 0.021*SL	0.34 + 0.019*SL
	t_{PHL}	0.25	0.14 + 0.055*SL	0.15 + 0.051*SL	0.15 + 0.051*SL
	t_R	0.23	0.16 + 0.035*SL	0.16 + 0.035*SL	0.16 + 0.035*SL
	t_F	0.35	0.18 + 0.089*SL	0.16 + 0.095*SL	0.13 + 0.099*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.46	0.46 + 0.000*SL	0.46 + 0.000*SL	0.46 + 0.000*SL

STDM80 NITD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.47	0.44 + 0.017*SL	0.45 + 0.014*SL	0.46 + 0.012*SL
	t_{PHL}	0.56	0.51 + 0.028*SL	0.51 + 0.027*SL	0.52 + 0.025*SL
	t_R	0.25	0.21 + 0.019*SL	0.22 + 0.018*SL	0.22 + 0.018*SL
	t_F	0.28	0.19 + 0.043*SL	0.18 + 0.047*SL	0.17 + 0.048*SL
E to Y	t_{PLH}	0.46	0.43 + 0.017*SL	0.44 + 0.014*SL	0.45 + 0.012*SL
	t_{PHL}	0.18	0.12 + 0.032*SL	0.13 + 0.026*SL	0.14 + 0.026*SL
	t_R	0.26	0.22 + 0.018*SL	0.22 + 0.018*SL	0.22 + 0.018*SL
	t_F	0.26	0.17 + 0.043*SL	0.17 + 0.045*SL	0.15 + 0.048*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.68	0.68 + 0.000*SL	0.68 + 0.000*SL	0.68 + 0.000*SL

STDM80 NITD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.65	0.63 + 0.012*SL	0.63 + 0.011*SL	0.64 + 0.009*SL
	t_{PHL}	0.80	0.76 + 0.016*SL	0.77 + 0.015*SL	0.77 + 0.014*SL
	t_R	0.34	0.32 + 0.010*SL	0.32 + 0.010*SL	0.32 + 0.010*SL
	t_F	0.32	0.28 + 0.022*SL	0.28 + 0.022*SL	0.27 + 0.023*SL
E to Y	t_{PLH}	0.65	0.62 + 0.012*SL	0.63 + 0.010*SL	0.64 + 0.009*SL
	t_{PHL}	0.14	0.10 + 0.018*SL	0.11 + 0.015*SL	0.12 + 0.013*SL
	t_R	0.34	0.32 + 0.010*SL	0.32 + 0.010*SL	0.32 + 0.010*SL
	t_F	0.22	0.17 + 0.023*SL	0.17 + 0.023*SL	0.16 + 0.024*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	1.03	1.03 + 0.000*SL	1.03 + 0.000*SL	1.03 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

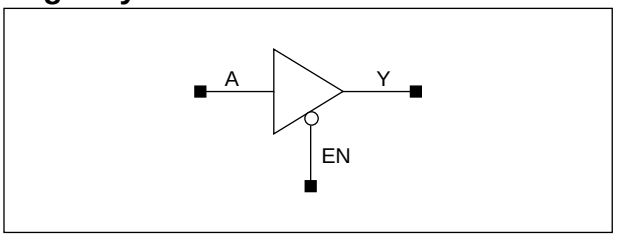
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NITD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.05	1.03 + 0.007*SL	1.03 + 0.007*SL	1.04 + 0.007*SL
	t_{PHL}	1.30	1.28 + 0.010*SL	1.28 + 0.009*SL	1.29 + 0.008*SL
	t_R	0.57	0.56 + 0.004*SL	0.56 + 0.005*SL	0.56 + 0.005*SL
	t_F	0.51	0.49 + 0.009*SL	0.49 + 0.009*SL	0.49 + 0.010*SL
E to Y	t_{PLH}	1.06	1.04 + 0.008*SL	1.05 + 0.007*SL	1.05 + 0.007*SL
	t_{PHL}	0.12	0.10 + 0.009*SL	0.10 + 0.009*SL	0.11 + 0.008*SL
	t_R	0.57	0.56 + 0.004*SL	0.55 + 0.005*SL	0.56 + 0.005*SL
	t_F	0.20	0.17 + 0.014*SL	0.18 + 0.011*SL	0.17 + 0.012*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	1.81	1.81 + 0.000*SL	1.81 + 0.000*SL	1.81 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

A	EN	Y
x	1	Hi-Z
0	0	0
1	0	1

Cell Data

Input Load (SL)								Output Load (SL)			
STD80											
NITN		*NITND2*		*NITND4*		*NITND8*		*NITN*	*NITND2*	*NITND4*	*NITND8*
A	EN	A	EN	A	EN	A	EN	Y	Y	Y	Y
0.6	0.7	0.6	0.7	0.6	0.8	0.5	0.8	1.3	2.0	4.1	8.2
STDM80											
NITN		*NITND2*		*NITND4*		*NITND8*		*NITN*	*NITND2*	*NITND4*	*NITND8*
A	EN	A	EN	A	EN	A	EN	Y	Y	Y	Y
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	1.4	2.2	4.5	9.0

STD80/STDM80			
Gate Count			
NITN	*NITND2*	*NITND4*	*NITND8*
2.3	2.7	4.0	6.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NITN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.24 + 0.021*SL	0.25 + 0.015*SL	0.28 + 0.012*SL
	t_{PHL}	0.39	0.31 + 0.039*SL	0.31 + 0.039*SL	0.31 + 0.039*SL
	t_R	0.18	0.13 + 0.023*SL	0.13 + 0.024*SL	0.10 + 0.027*SL
	t_F	0.27	0.12 + 0.072*SL	0.12 + 0.076*SL	0.10 + 0.078*SL
EN to Y	t_{PLH}	0.40	0.36 + 0.021*SL	0.37 + 0.015*SL	0.40 + 0.012*SL
	t_{PHL}	0.32	0.23 + 0.044*SL	0.24 + 0.040*SL	0.25 + 0.039*SL
	t_R	0.17	0.12 + 0.023*SL	0.12 + 0.025*SL	0.09 + 0.027*SL
	t_F	0.26	0.11 + 0.074*SL	0.11 + 0.076*SL	0.09 + 0.078*SL
	t_{PLZ}	0.21	0.21 + 0.001*SL	0.21 + 0.000*SL	0.21 + 0.000*SL
	t_{PHZ}	0.40	0.40 + 0.000*SL	0.40 + 0.000*SL	0.40 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 NITND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.31 + 0.016*SL	0.33 + 0.010*SL	0.36 + 0.006*SL
	t_{PHL}	0.43	0.39 + 0.020*SL	0.40 + 0.019*SL	0.40 + 0.019*SL
	t_R	0.21	0.18 + 0.012*SL	0.18 + 0.012*SL	0.17 + 0.013*SL
	t_F	0.21	0.14 + 0.036*SL	0.14 + 0.036*SL	0.12 + 0.039*SL
EN to Y	t_{PLH}	0.48	0.45 + 0.014*SL	0.46 + 0.010*SL	0.50 + 0.006*SL
	t_{PHL}	0.28	0.24 + 0.024*SL	0.24 + 0.021*SL	0.26 + 0.019*SL
	t_R	0.20	0.18 + 0.011*SL	0.18 + 0.012*SL	0.17 + 0.013*SL
	t_F	0.19	0.14 + 0.027*SL	0.11 + 0.037*SL	0.10 + 0.039*SL
	t_{PLZ}	0.23	0.23 + 0.000*SL	0.23 + 0.000*SL	0.23 + 0.000*SL
	t_{PHZ}	0.56	0.56 + 0.001*SL	0.56 + 0.000*SL	0.57 + 0.000*SL

STD80 NITND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.48	0.47 + 0.008*SL	0.47 + 0.007*SL	0.50 + 0.004*SL
	t_{PHL}	0.60	0.58 + 0.012*SL	0.58 + 0.010*SL	0.59 + 0.009*SL
	t_R	0.30	0.29 + 0.005*SL	0.29 + 0.006*SL	0.29 + 0.006*SL
	t_F	0.27	0.24 + 0.016*SL	0.24 + 0.015*SL	0.21 + 0.019*SL
EN to Y	t_{PLH}	0.66	0.64 + 0.009*SL	0.65 + 0.007*SL	0.68 + 0.004*SL
	t_{PHL}	0.29	0.26 + 0.014*SL	0.26 + 0.012*SL	0.28 + 0.010*SL
	t_R	0.30	0.29 + 0.005*SL	0.29 + 0.006*SL	0.29 + 0.006*SL
	t_F	0.16	0.12 + 0.020*SL	0.13 + 0.019*SL	0.12 + 0.019*SL
	t_{PLZ}	0.30	0.30 + 0.000*SL	0.30 + 0.000*SL	0.30 + 0.000*SL
	t_{PHZ}	0.88	0.88 + 0.000*SL	0.88 + 0.000*SL	0.88 + 0.000*SL

STD80 NITND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.77	0.76 + 0.005*SL	0.76 + 0.005*SL	0.78 + 0.003*SL
	t_{PHL}	0.98	0.97 + 0.007*SL	0.97 + 0.007*SL	0.98 + 0.005*SL
	t_R	0.53	0.53 + 0.001*SL	0.53 + 0.002*SL	0.51 + 0.003*SL
	t_F	0.46	0.45 + 0.004*SL	0.45 + 0.006*SL	0.43 + 0.008*SL
EN to Y	t_{PLH}	1.04	1.03 + 0.006*SL	1.03 + 0.005*SL	1.05 + 0.003*SL
	t_{PHL}	0.32	0.30 + 0.008*SL	0.31 + 0.008*SL	0.33 + 0.005*SL
	t_R	0.53	0.53 + 0.000*SL	0.53 + 0.002*SL	0.52 + 0.003*SL
	t_F	0.16	0.14 + 0.010*SL	0.14 + 0.010*SL	0.15 + 0.010*SL
	t_{PLZ}	0.42	0.42 + 0.001*SL	0.42 + 0.000*SL	0.42 + 0.000*SL
	t_{PHZ}	1.53	1.53 + 0.000*SL	1.53 + 0.000*SL	1.54 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NITN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.37	0.32 + 0.027*SL	0.33 + 0.022*SL	0.35 + 0.019*SL
	t_{PHL}	0.50	0.40 + 0.054*SL	0.41 + 0.051*SL	0.41 + 0.050*SL
	t_R	0.22	0.14 + 0.037*SL	0.15 + 0.035*SL	0.14 + 0.036*SL
	t_F	0.36	0.17 + 0.095*SL	0.16 + 0.097*SL	0.15 + 0.099*SL
EN to Y	t_{PLH}	0.54	0.49 + 0.027*SL	0.51 + 0.022*SL	0.53 + 0.019*SL
	t_{PHL}	0.42	0.31 + 0.055*SL	0.32 + 0.052*SL	0.33 + 0.051*SL
	t_R	0.22	0.14 + 0.036*SL	0.15 + 0.035*SL	0.14 + 0.036*SL
	t_F	0.34	0.15 + 0.097*SL	0.14 + 0.098*SL	0.14 + 0.099*SL
	t_{PLZ}	0.26	0.26 + 0.000*SL	0.26 + 0.000*SL	0.26 + 0.000*SL
	t_{PHZ}	0.55	0.55 + 0.000*SL	0.55 + 0.000*SL	0.55 + 0.000*SL

STDM80 NITND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.46	0.42 + 0.018*SL	0.43 + 0.014*SL	0.45 + 0.012*SL
	t_{PHL}	0.57	0.51 + 0.029*SL	0.51 + 0.027*SL	0.52 + 0.026*SL
	t_R	0.24	0.20 + 0.018*SL	0.21 + 0.018*SL	0.21 + 0.018*SL
	t_F	0.28	0.18 + 0.047*SL	0.18 + 0.048*SL	0.18 + 0.048*SL
EN to Y	t_{PLH}	0.66	0.62 + 0.018*SL	0.63 + 0.014*SL	0.65 + 0.012*SL
	t_{PHL}	0.38	0.32 + 0.030*SL	0.33 + 0.028*SL	0.34 + 0.026*SL
	t_R	0.24	0.21 + 0.019*SL	0.21 + 0.018*SL	0.21 + 0.018*SL
	t_F	0.24	0.15 + 0.049*SL	0.15 + 0.048*SL	0.14 + 0.049*SL
	t_{PLZ}	0.29	0.29 + 0.000*SL	0.29 + 0.000*SL	0.29 + 0.000*SL
	t_{PHZ}	0.76	0.76 + 0.000*SL	0.76 + 0.000*SL	0.76 + 0.000*SL

STDM80 NITND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.65	0.62 + 0.012*SL	0.63 + 0.010*SL	0.64 + 0.009*SL
	t_{PHL}	0.79	0.76 + 0.016*SL	0.77 + 0.015*SL	0.77 + 0.014*SL
	t_R	0.34	0.32 + 0.010*SL	0.32 + 0.010*SL	0.32 + 0.009*SL
	t_F	0.32	0.28 + 0.021*SL	0.27 + 0.023*SL	0.27 + 0.023*SL
EN to Y	t_{PLH}	0.90	0.88 + 0.012*SL	0.89 + 0.010*SL	0.90 + 0.009*SL
	t_{PHL}	0.39	0.35 + 0.017*SL	0.36 + 0.016*SL	0.37 + 0.014*SL
	t_R	0.34	0.32 + 0.010*SL	0.32 + 0.010*SL	0.32 + 0.010*SL
	t_F	0.21	0.16 + 0.025*SL	0.16 + 0.025*SL	0.17 + 0.024*SL
	t_{PLZ}	0.36	0.35 + 0.000*SL	0.35 + 0.000*SL	0.35 + 0.000*SL
	t_{PHZ}	1.19	1.19 + 0.000*SL	1.19 + 0.000*SL	1.19 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 NITND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.05	1.03 + 0.008*SL	1.04 + 0.007*SL	1.04 + 0.006*SL
	t_{PHL}	1.30	1.28 + 0.010*SL	1.28 + 0.009*SL	1.29 + 0.008*SL
	t_R	0.56	0.55 + 0.005*SL	0.55 + 0.005*SL	0.55 + 0.005*SL
	t_F	0.51	0.50 + 0.008*SL	0.49 + 0.009*SL	0.49 + 0.010*SL
EN to Y	t_{PLH}	1.43	1.42 + 0.007*SL	1.42 + 0.007*SL	1.43 + 0.006*SL
	t_{PHL}	0.45	0.43 + 0.011*SL	0.43 + 0.010*SL	0.44 + 0.009*SL
	t_R	0.57	0.56 + 0.004*SL	0.56 + 0.005*SL	0.56 + 0.005*SL
	t_F	0.22	0.19 + 0.014*SL	0.19 + 0.014*SL	0.20 + 0.013*SL
	t_{PLZ}	0.50	0.50 + 0.000*SL	0.50 + 0.000*SL	0.50 + 0.000*SL
	t_{PHZ}	2.07	2.07 + 0.001*SL	2.07 + 0.000*SL	2.07 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Cell List

Cell Name	Function Description
FD1	D Flip-Flop
FD1D2	D Flip-Flop with 2X Drive
FD1CS	D Flip-Flop with Scan Clock
FD1CSD2	D Flip-Flop with Scan Clock, 2X Drive
FD1S	D Flip-Flop with Scan
FD1SD2	D Flip-Flop with Scan, 2X Drive
FD1Q	D Flip-Flop with Q Output Only
FD1QD2	D Flip-Flop with Q Output Only, 2X Drive
FD1X2	2-Bit D Flip-Flop
FD1X4	4-Bit D Flip-Flop
YFD1	Fast D Flip-Flop
YFD1D2	Fast D Flip-Flop with 2X Drive
FD2	D Flip-Flop with Reset
FD2D2	D Flip-Flop with Reset, 2X Drive
FD2CS	D Flip-Flop with Reset, Scan Clock
FD2CSD2	D Flip-Flop with Reset, Scan Clock, 2X Drive
FD2S	D Flip-Flop with Reset, Scan
FD2SD2	D Flip-Flop with Reset, Scan, 2X Drive
FD2Q	D Flip-Flop with Reset, Q Output Only
FD2QD2	D Flip-Flop with Reset, Q Output Only, 2X Drive
FD2X2	2-Bit D Flip-Flop with Reset
FD2X4	4-Bit D Flip-Flop with Reset
YFD2	Fast D Flip-Flop with Reset
YFD2D2	Fast D Flip-Flop with Reset, 2X Drive
FD2T	D Flip-Flop with Reset, Tri-State Output
FD2TD2	D Flip-Flop with Reset, Tri-State Output, 2X Drive
FD2TCS	D Flip-Flop with Reset, Scan Clock, Tri-State Output
FD2TCSD2	D Flip-Flop with Reset, Scan Clock, Tri-State Output, 2X Drive
FD2TS	D Flip-Flop with Reset, Scan, Tri-State Output
FD2TSD2	D Flip-Flop with Reset, Scan, Tri-State Output, 2X Drive
FD3	D Flip-Flop with Set
FD3D2	D Flip-Flop with Set, 2X Drive
FD3CS	D Flip-Flop with Set, Scan Clock
FD3CSD2	D Flip-Flop with Set, Scan Clock, 2X Drive

Cell List (Continued)

Cell Name	Function Description
FD3S	D Flip-Flop with Set, Scan
FD3SD2	D Flip-Flop with Set, Scan, 2X Drive
FD3Q	D Flip-Flop with Set, Q Output Only
FD3QD2	D Flip-Flop with Set, Q Output Only, 2X Drive
FD3X2	2-Bit D Flip-Flop with Set
FD3X4	4-Bit D Flip-Flop with Set
YFD3	Fast D Flip-Flop with Set
YFD3D2	Fast D Flip-Flop with Set, 2X Drive
FD4	D Flip-Flop with Reset, Set
FD4D2	D Flip-Flop with Reset, Set, 2X Drive
FD4CS	D Flip-Flop with Reset, Set, Scan Clock
FD4CSD2	D Flip-Flop with Reset, Set, Scan Clock, 2X Drive
FD4S	D Flip-Flop with Reset, Set, Scan
FD4SD2	D Flip-Flop with Reset, Set, Scan, 2X Drive
FD4Q	D Flip-Flop with Reset, Set, Q Output Only
FD4QD2	D Flip-Flop with Reset, Set, Q Output Only, 2X Drive
FD4X2	2-Bit D Flip-Flop with Reset, Set
FD4X4	4-Bit D Flip-Flop with Reset, Set
YFD4	Fast D Flip-Flop with Reset, Set
YFD4D2	Fast D Flip-Flop with Reset, Set, 2X Drive
FD5	D Flip-Flop with Negative Edge Trigger
FD5D2	D Flip-Flop with Negative Edge Trigger, 2X Drive
FD5S	D Flip-Flop with Negative Edge Trigger, Scan
FD5SD2	D Flip-Flop with Negative Edge Trigger, Scan, 2X Drive
FD5X4	4-Bit Flip-Flop with Negative Edge Trigger
FD6	D Flip-Flop with Negative Edge Trigger, Reset
FD6D2	D Flip-Flop with Negative Edge Trigger, Reset, 2X Drive
FD6S	D Flip-Flop with Negative Edge Trigger, Reset, Scan
FD6SD2	D Flip-Flop with Negative Edge Trigger, Reset, Scan, 2X Drive
FD7	D Flip-Flop with Negative Edge Trigger, Set
FD7D2	D Flip-Flop with Negative Edge Trigger, Set, 2X Drive
FD7S	D Flip-Flop with Negative Edge Trigger, Set, Scan
FD7SD2	D Flip-Flop with Negative Edge Trigger, Set, Scan, 2X Drive
FD8	D Flip-Flop with Negative Edge Trigger, Reset, Set

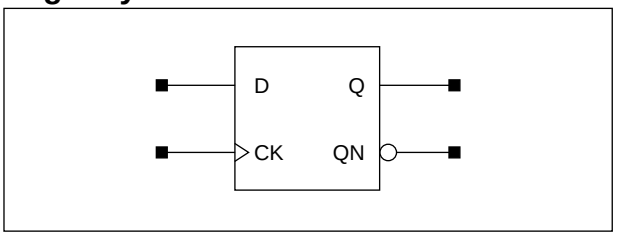
Cell List (Continued)

Cell Name	Function Description
FD8D2	D Flip-Flop with Negative Edge Trigger, Reset, Set, 2X Drive
FD8S	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan
FD8SD2	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 2X Drive
FDS2	D Flip-Flop with Synchronous Clear
FDS2D2	D Flip-Flop with Synchronous Clear, 2X Drive
FDS2CS	D Flip-Flop with Synchronous Clear, Scan Clock
FDS2CSD2	D Flip-Flop with Synchronous Clear, Scan Clock, 2X Drive
FDS2S	D Flip-Flop with Synchronous Clear, Scan
FDS2SD2	D Flip-Flop with Synchronous Clear, Scan, 2X Drive
FDS3	D Flip-Flop with Synchronous Set
FDS3D2	D Flip-Flop with Synchronous Set, 2X Drive
FG1	D Flip-Flop with CK Enable
FG1X4	4-Bit D Flip-Flop with CK Enable
FG2	D Flip-Flop with CK Enable, Reset
FG2X4	4-Bit D Flip-Flop with CK Enable, Reset
FJ1	JK Flip-Flop
FJ1D2	JK Flip-Flop with 2X Drive
FJ1S	JK Flip-Flop with Scan
FJ1SD2	JK Flip-Flop with Scan, 2X Drive
FJ2	JK Flip-Flop with Reset
FJ2D2	JK Flip-Flop with Reset, 2X Drive
FJ2S	JK Flip-Flop with Reset, Scan
FJ2SD2	JK Flip-Flop with Reset, Scan, 2X Drive
FJ4	JK Flip-Flop with Reset, Set
FJ4D2	JK Flip-Flop with Reset, Set, 2X Drive
FJ4S	JK Flip-Flop with Reset, Set, Scan
FJ4SD2	JK Flip-Flop with Reset, Set, Scan, 2X Drive
FT2	Toggle Flip-Flop with Reset
FT2D2	Toggle Flip-Flop with Reset, 2X Drive
FT3	Toggle Flip-Flop with Set
FT3D2	Toggle Flip-Flop with Set, 2X Drive

FD1/FD1D2

D Flip-Flop with 1X/2X Drive

Logic Symbol



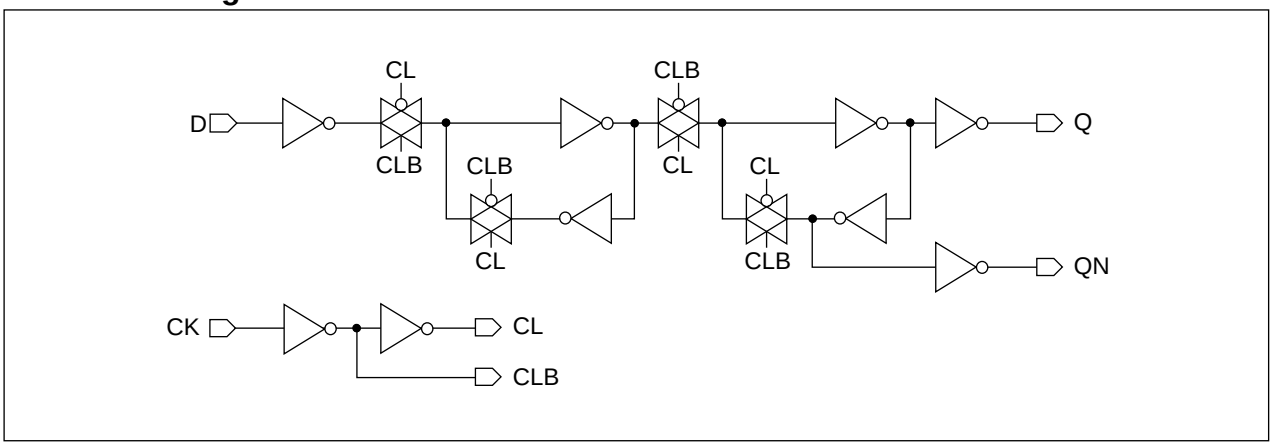
Truth Table

D	CK	Q (n+1)	QN (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
STD80					
FD1		*FD1D2*		*FD1*	*FD1D2*
D	CK	D	CK		
0.5	0.5	0.5	0.5	5.3	6.0
STDM80					
FD1		*FD1D2*		*FD1*	*FD1D2*
D	CK	D	CK		
0.6	0.6	0.6	0.6	5.3	6.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD1	FD1D2	FD1	FD1D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.87	0.87
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.46	0.46	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44, SL: Standard Load)

STD80 FD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.57	0.52 + 0.028*SL	0.52 + 0.024*SL	0.53 + 0.024*SL
	t_{PHL}	0.66	0.57 + 0.042*SL	0.58 + 0.038*SL	0.59 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.70	0.65 + 0.024*SL	0.65 + 0.024*SL	0.65 + 0.024*SL
	t_{PHL}	0.74	0.66 + 0.038*SL	0.67 + 0.037*SL	0.67 + 0.037*SL
	t_R	0.18	0.09 + 0.046*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.06 + 0.069*SL

STD80 FD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.54 + 0.018*SL	0.55 + 0.014*SL	0.57 + 0.012*SL
	t_{PHL}	0.65	0.60 + 0.023*SL	0.61 + 0.020*SL	0.62 + 0.018*SL
	t_R	0.16	0.12 + 0.023*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
CK to QN	t_{PLH}	0.76	0.73 + 0.013*SL	0.74 + 0.012*SL	0.74 + 0.012*SL
	t_{PHL}	0.80	0.76 + 0.018*SL	0.76 + 0.018*SL	0.76 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.033*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40, SL: Standard Load)

STDM80 FD1

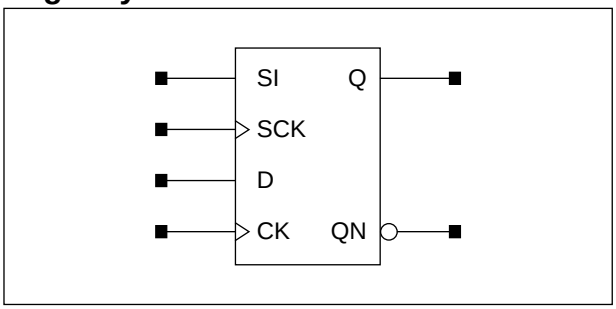
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.74 + 0.038*SL	0.75 + 0.035*SL	0.76 + 0.034*SL
	t_{PHL}	0.93	0.83 + 0.052*SL	0.84 + 0.046*SL	0.86 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
CK to QN	t_{PLH}	1.00	0.93 + 0.035*SL	0.93 + 0.033*SL	0.94 + 0.033*SL
	t_{PHL}	1.05	0.95 + 0.047*SL	0.96 + 0.045*SL	0.96 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL

STDM80 FD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.77 + 0.024*SL	0.79 + 0.020*SL	0.80 + 0.018*SL
	t_{PHL}	0.92	0.86 + 0.031*SL	0.87 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
CK to QN	t_{PLH}	1.09	1.05 + 0.019*SL	1.06 + 0.017*SL	1.06 + 0.017*SL
	t_{PHL}	1.12	1.07 + 0.026*SL	1.08 + 0.023*SL	1.09 + 0.022*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



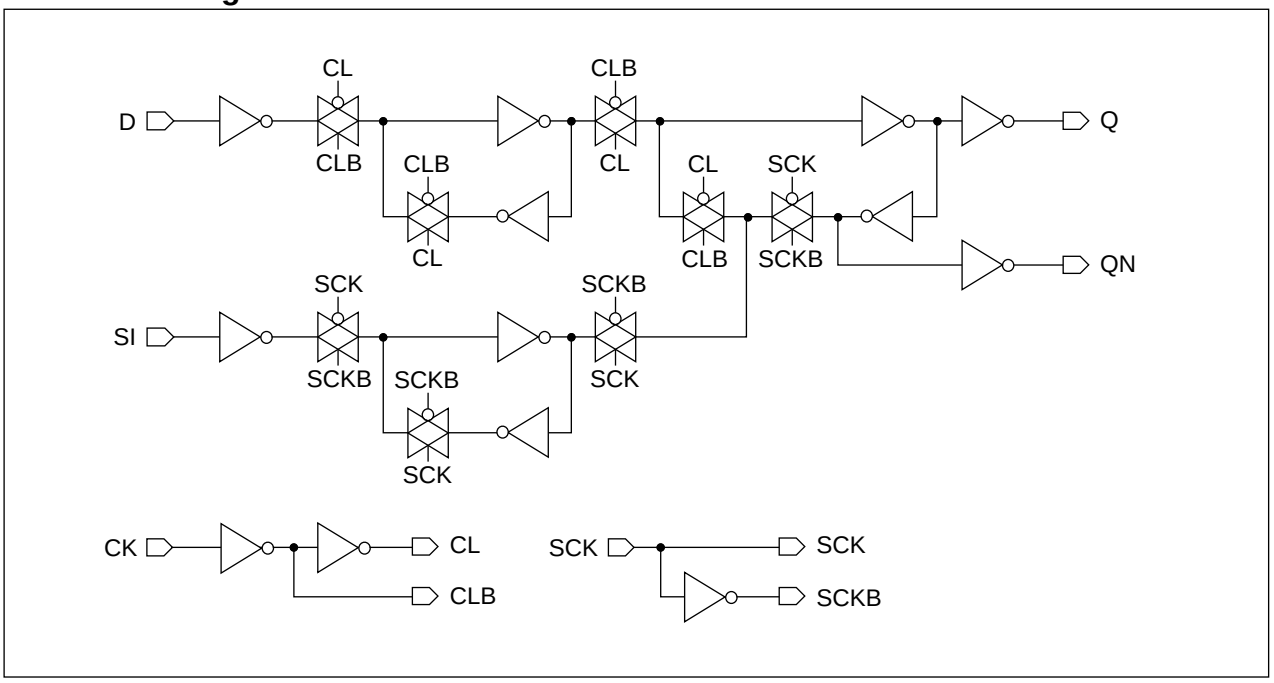
Truth Table

SI	SCK	D	CK	Q (n+1)	QN (n+1)
x	0	0	⎍	0	1
x	0	1	⎍	1	0
0	⎍	x	0	0	1
1	⎍	x	0	1	0

Cell Data

Input Load (SL)								Gate Count	
STD80									
FD1CS				*FD1CSD2*				*FD1CS*	*FD1CSD2*
SI	SCK	D	CK	SI	SCK	D	CK		
0.6	1.8	0.6	0.6	0.6	1.8	0.6	0.6	8.7	9.0
STDM80									
FD1CS				*FD1CSD2*				*FD1CS*	*FD1CSD2*
SI	SCK	D	CK	SI	SCK	D	CK		
0.6	2.0	0.6	0.6	0.6	2.0	0.6	0.6	8.7	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD1CS	FD1CSD2	FD1CS	FD1CSD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.87	0.87
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (SCK)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width High (SCK)	t_{PWH}	0.87	0.87	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.46	0.46	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.68	0.68	0.82	0.82
Input Hold Time (SI to SCK)	t_{HD}	0.33	0.33	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD1CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.52 + 0.028*SL	0.53 + 0.024*SL	0.54 + 0.024*SL
	t_{PHL}	0.65	0.57 + 0.041*SL	0.58 + 0.038*SL	0.59 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.10 + 0.066*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SCK to Q	t_{PLH}	0.65	0.59 + 0.029*SL	0.60 + 0.025*SL	0.61 + 0.024*SL
	t_{PHL}	0.59	0.50 + 0.042*SL	0.51 + 0.038*SL	0.52 + 0.037*SL
	t_R	0.23	0.14 + 0.044*SL	0.13 + 0.047*SL	0.09 + 0.052*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.75	0.69 + 0.029*SL	0.70 + 0.025*SL	0.71 + 0.024*SL
	t_{PHL}	0.82	0.73 + 0.041*SL	0.74 + 0.038*SL	0.75 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.11 + 0.067*SL	0.09 + 0.069*SL
SCK to QN	t_{PLH}	0.62	0.57 + 0.025*SL	0.57 + 0.023*SL	0.57 + 0.024*SL
	t_{PHL}	0.82	0.74 + 0.037*SL	0.74 + 0.037*SL	0.74 + 0.037*SL
	t_R	0.19	0.09 + 0.048*SL	0.09 + 0.050*SL	0.07 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.09 + 0.068*SL	0.07 + 0.069*SL

STD80 FD1CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.59	0.55 + 0.018*SL	0.56 + 0.014*SL	0.58 + 0.012*SL
	t_{PHL}	0.65	0.60 + 0.023*SL	0.61 + 0.020*SL	0.62 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SCK to Q	t_{PLH}	0.66	0.63 + 0.019*SL	0.64 + 0.014*SL	0.66 + 0.012*SL
	t_{PHL}	0.58	0.54 + 0.023*SL	0.55 + 0.020*SL	0.56 + 0.018*SL
	t_R	0.19	0.15 + 0.020*SL	0.15 + 0.022*SL	0.11 + 0.026*SL
	t_F	0.18	0.12 + 0.029*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
CK to QN	t_{PLH}	0.82	0.78 + 0.017*SL	0.79 + 0.014*SL	0.81 + 0.012*SL
	t_{PHL}	0.87	0.83 + 0.021*SL	0.83 + 0.019*SL	0.84 + 0.018*SL
	t_R	0.18	0.14 + 0.023*SL	0.14 + 0.022*SL	0.10 + 0.026*SL
	t_F	0.19	0.13 + 0.030*SL	0.12 + 0.031*SL	0.10 + 0.034*SL
SCK to QN	t_{PLH}	0.69	0.66 + 0.014*SL	0.67 + 0.012*SL	0.67 + 0.012*SL
	t_{PHL}	0.89	0.85 + 0.017*SL	0.85 + 0.017*SL	0.84 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

FD1CS/FD1CSD2

D Flip-Flop with Scan Clock, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD1CS

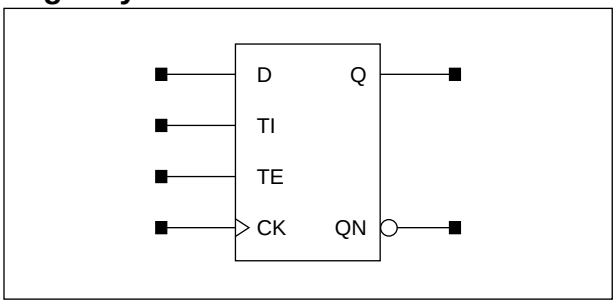
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.83	0.75 + 0.038*SL	0.76 + 0.035*SL	0.77 + 0.034*SL
	t_{PHL}	0.92	0.82 + 0.052*SL	0.84 + 0.047*SL	0.85 + 0.045*SL
	t_R	0.28	0.15 + 0.068*SL	0.14 + 0.070*SL	0.13 + 0.071*SL
	t_F	0.31	0.14 + 0.081*SL	0.14 + 0.081*SL	0.14 + 0.082*SL
SCK to Q	t_{PLH}	0.98	0.90 + 0.041*SL	0.91 + 0.036*SL	0.93 + 0.034*SL
	t_{PHL}	0.82	0.72 + 0.053*SL	0.74 + 0.046*SL	0.75 + 0.044*SL
	t_R	0.32	0.19 + 0.065*SL	0.18 + 0.067*SL	0.16 + 0.070*SL
	t_F	0.32	0.16 + 0.078*SL	0.16 + 0.079*SL	0.14 + 0.081*SL
CK to QN	t_{PLH}	1.07	0.99 + 0.042*SL	1.01 + 0.036*SL	1.02 + 0.033*SL
	t_{PHL}	1.16	1.05 + 0.053*SL	1.07 + 0.048*SL	1.09 + 0.046*SL
	t_R	0.30	0.17 + 0.069*SL	0.17 + 0.069*SL	0.15 + 0.070*SL
	t_F	0.32	0.15 + 0.084*SL	0.16 + 0.082*SL	0.16 + 0.082*SL
SCK to QN	t_{PLH}	0.89	0.82 + 0.034*SL	0.82 + 0.033*SL	0.82 + 0.033*SL
	t_{PHL}	1.21	1.11 + 0.046*SL	1.12 + 0.044*SL	1.12 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.12 + 0.071*SL	0.11 + 0.072*SL
	t_F	0.28	0.13 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.083*SL

STDM80 FD1CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.84	0.79 + 0.024*SL	0.80 + 0.020*SL	0.82 + 0.018*SL
	t_{PHL}	0.92	0.86 + 0.030*SL	0.87 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.21	0.15 + 0.032*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.039*SL
SCK to Q	t_{PLH}	1.00	0.95 + 0.026*SL	0.97 + 0.021*SL	0.99 + 0.018*SL
	t_{PHL}	0.82	0.76 + 0.031*SL	0.77 + 0.026*SL	0.79 + 0.023*SL
	t_R	0.25	0.18 + 0.032*SL	0.18 + 0.032*SL	0.18 + 0.033*SL
	t_F	0.22	0.14 + 0.041*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
CK to QN	t_{PLH}	1.16	1.11 + 0.023*SL	1.12 + 0.020*SL	1.13 + 0.018*SL
	t_{PHL}	1.23	1.17 + 0.029*SL	1.18 + 0.025*SL	1.19 + 0.023*SL
	t_R	0.23	0.16 + 0.037*SL	0.17 + 0.033*SL	0.17 + 0.033*SL
	t_F	0.23	0.15 + 0.041*SL	0.15 + 0.040*SL	0.16 + 0.039*SL
SCK to QN	t_{PLH}	0.98	0.95 + 0.018*SL	0.95 + 0.017*SL	0.95 + 0.017*SL
	t_{PHL}	1.31	1.26 + 0.024*SL	1.27 + 0.022*SL	1.27 + 0.021*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



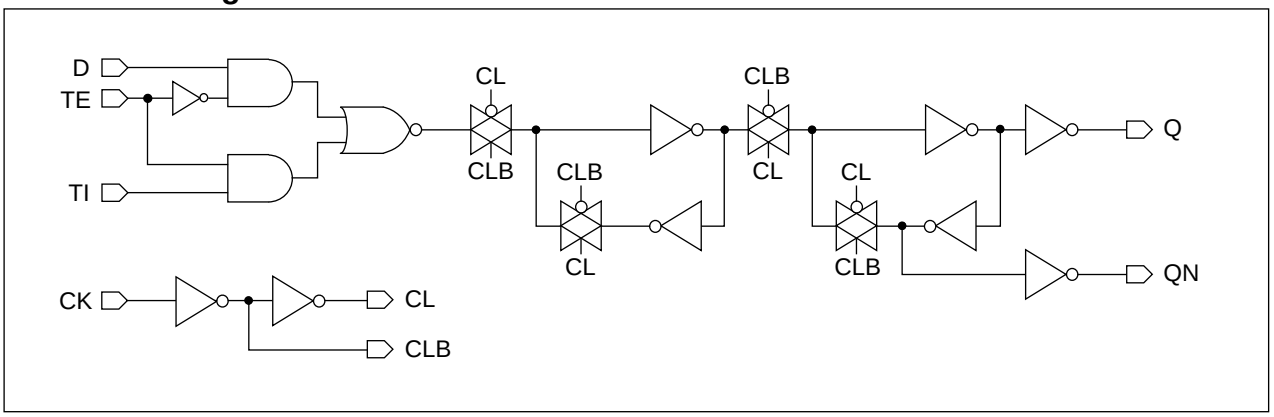
Truth Table

D	TI	TE	CK	Q (n+1)	QN (n+1)
0	x	0	↑	0	1
1	x	0	↑	1	0
x	0	1	↑	0	1
x	1	1	↑	1	0

Cell Data

Input Load (SL)								Gate Count	
STD80									
FD1S				*FD1SD2*				*FD1S*	*FD1SD2*
D	TI	TE	CK	D	TI	TE	CK		
0.3	0.5	0.9	0.5	0.3	0.5	0.9	0.5	7.0	7.7
STDM80									
FD1S				*FD1SD2*				*FD1S*	*FD1SD2*
D	TI	TE	CK	D	TI	TE	CK		
0.6	0.6	1.1	0.6	0.6	0.6	1.1	0.6	7.0	7.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD1S	FD1SD2	FD1S	FD1SD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.96	0.96
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.57	0.57	0.76	0.79
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.60	0.60	0.85	0.85
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.68	0.68	0.87	0.87
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33	0.33	0.33

FD1S/FD1SD2

D Flip-Flop with Scan, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.53 + 0.028*SL	0.53 + 0.024*SL	0.54 + 0.024*SL
	t_{PHL}	0.68	0.59 + 0.042*SL	0.60 + 0.038*SL	0.61 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.71	0.66 + 0.025*SL	0.67 + 0.024*SL	0.67 + 0.024*SL
	t_{PHL}	0.75	0.67 + 0.038*SL	0.68 + 0.037*SL	0.68 + 0.037*SL
	t_R	0.18	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL

STD80 FD1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.59	0.55 + 0.018*SL	0.56 + 0.013*SL	0.58 + 0.012*SL
	t_{PHL}	0.66	0.62 + 0.023*SL	0.63 + 0.020*SL	0.64 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
CK to QN	t_{PLH}	0.78	0.75 + 0.013*SL	0.75 + 0.012*SL	0.76 + 0.012*SL
	t_{PHL}	0.81	0.77 + 0.018*SL	0.77 + 0.018*SL	0.77 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.83	0.75 + 0.038*SL	0.77 + 0.035*SL	0.77 + 0.034*SL
	t_{PHL}	0.95	0.85 + 0.052*SL	0.86 + 0.046*SL	0.88 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
CK to QN	t_{PLH}	1.02	0.95 + 0.035*SL	0.96 + 0.033*SL	0.96 + 0.033*SL
	t_{PHL}	1.06	0.96 + 0.047*SL	0.97 + 0.045*SL	0.97 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL

STDM80 FD1SD2

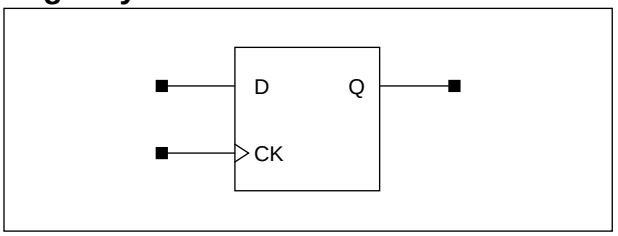
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.83	0.79 + 0.023*SL	0.80 + 0.020*SL	0.81 + 0.018*SL
	t_{PHL}	0.94	0.88 + 0.030*SL	0.89 + 0.026*SL	0.91 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.039*SL
CK to QN	t_{PLH}	1.11	1.07 + 0.018*SL	1.08 + 0.017*SL	1.08 + 0.017*SL
	t_{PHL}	1.13	1.08 + 0.025*SL	1.09 + 0.023*SL	1.10 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

FD1Q/FD1QD2

D Flip-Flop with Q Output Only, 1X/2X Drive

Logic Symbol



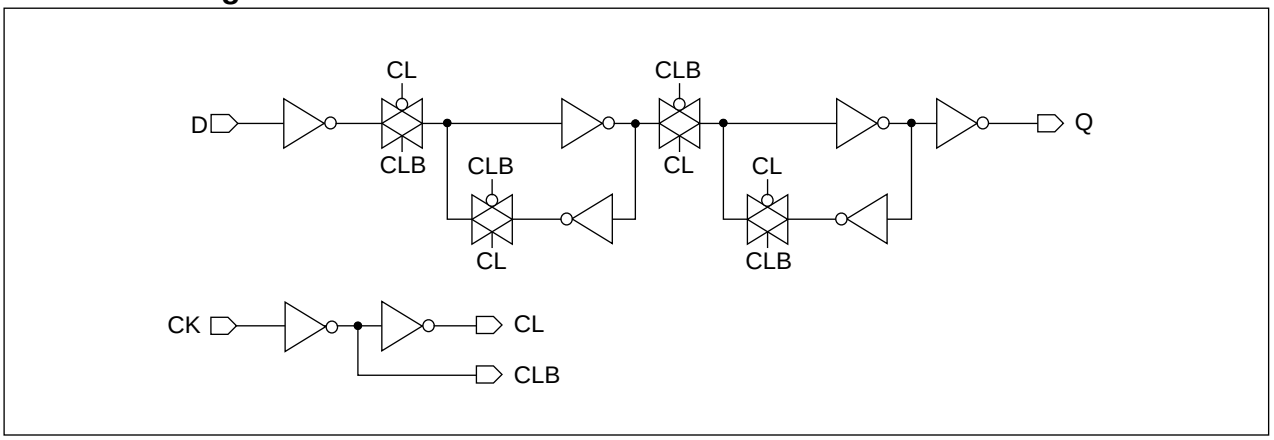
Truth Table

D	CK	Q (n+1)
0	↑	0
1	↑	1
x	↓	Q (n)

Cell Data

Input Load (SL)				Gate Count	
STD80/STDM80					
FD1Q		*FD1QD2*		*FD1Q*	*FD1QD2*
D	CK	D	CK		
0.6	0.6	0.6	0.6	5.0	5.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD1Q	FD1QD2	FD1Q	FD1QD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.87	0.87
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.46	0.00	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD1Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.57	0.51 + 0.028*SL	0.52 + 0.024*SL	0.52 + 0.024*SL
	t_{PHL}	0.65	0.57 + 0.040*SL	0.57 + 0.038*SL	0.58 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.10 + 0.063*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

STD80 FD1QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.57	0.54 + 0.018*SL	0.55 + 0.014*SL	0.56 + 0.012*SL
	t_{PHL}	0.64	0.59 + 0.023*SL	0.60 + 0.019*SL	0.61 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.17	0.10 + 0.034*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD1Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.74 + 0.038*SL	0.75 + 0.034*SL	0.76 + 0.033*SL
	t_{PHL}	0.91	0.81 + 0.051*SL	0.83 + 0.045*SL	0.83 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.30	0.14 + 0.078*SL	0.14 + 0.080*SL	0.12 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

STDM80 FD1QD2

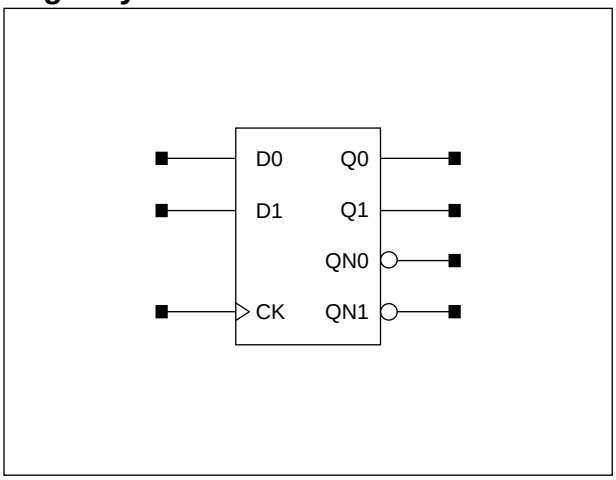
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.77 + 0.024*SL	0.78 + 0.020*SL	0.80 + 0.018*SL
	t_{PHL}	0.90	0.84 + 0.031*SL	0.86 + 0.025*SL	0.88 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.038*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

FD1X2

2-Bit D Flip-Flop

Logic Symbol



Truth Table

Dn	CK	Qn (n+1)	QNn (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Qn (n)	QNn (n)

Cell Data

Input Load (SL)		Gate Count
STD80		
Dn	CK	
0.5	0.5	9.7
STDM80		
Dn	CK	
0.6	0.6	9.7

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CK)	t_{PWL}	0.90	1.07
Pulse Width High (CK)	t_{PWH}	0.90	0.82
Input Setup Time (D0 to CK)	t_{SU}	0.36	0.46
Input Hold Time (D0 to CK)	t_{HD}	0.33	0.38
Input Setup Time (D1 to CK)	t_{SU}	0.36	0.46
Input Hold Time (D1 to CK)	t_{HD}	0.33	0.38

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD1X2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.65	0.59 + 0.028*SL	0.60 + 0.024*SL	0.61 + 0.024*SL
	t_{PHL}	0.81	0.72 + 0.042*SL	0.73 + 0.038*SL	0.74 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to Q1	t_{PLH}	0.65	0.59 + 0.028*SL	0.60 + 0.025*SL	0.61 + 0.024*SL
	t_{PHL}	0.81	0.73 + 0.041*SL	0.73 + 0.038*SL	0.74 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to QN0	t_{PLH}	0.85	0.80 + 0.025*SL	0.80 + 0.024*SL	0.80 + 0.024*SL
	t_{PHL}	0.82	0.74 + 0.037*SL	0.74 + 0.037*SL	0.74 + 0.037*SL
	t_R	0.19	0.09 + 0.047*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
CK to QN1	t_{PLH}	0.85	0.80 + 0.025*SL	0.80 + 0.024*SL	0.80 + 0.024*SL
	t_{PHL}	0.82	0.74 + 0.037*SL	0.74 + 0.037*SL	0.74 + 0.037*SL
	t_R	0.18	0.09 + 0.048*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.06 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD1X2

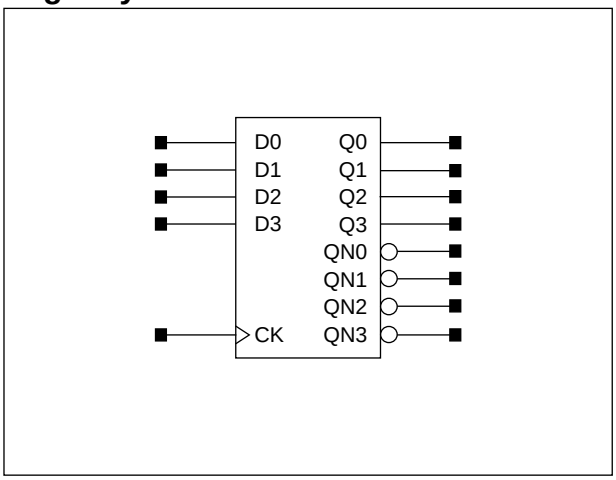
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.91	0.84 + 0.038*SL	0.85 + 0.035*SL	0.85 + 0.034*SL
	t_{PHL}	1.14	1.04 + 0.052*SL	1.05 + 0.046*SL	1.07 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
CK to Q1	t_{PLH}	0.91	0.83 + 0.038*SL	0.85 + 0.035*SL	0.85 + 0.034*SL
	t_{PHL}	1.14	1.04 + 0.052*SL	1.05 + 0.046*SL	1.06 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
CK to QN0	t_{PLH}	1.21	1.14 + 0.035*SL	1.15 + 0.033*SL	1.15 + 0.033*SL
	t_{PHL}	1.14	1.05 + 0.047*SL	1.05 + 0.044*SL	1.05 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.083*SL
CK to QN1	t_{PLH}	1.21	1.14 + 0.035*SL	1.14 + 0.033*SL	1.14 + 0.033*SL
	t_{PHL}	1.14	1.04 + 0.047*SL	1.05 + 0.045*SL	1.05 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.080*SL	0.12 + 0.080*SL	0.11 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

FD1X4

4-Bit D Flip-Flop

Logic Symbol



Truth Table

Dn	CK	Qn (n+1)	QNn (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Qn (n)	QNn (n)

Cell Data

Input Load (SL)		Gate Count
STD80		
Dn	CK	
0.5	0.5	18.3
STDM80		
Dn	CK	
0.6	0.6	18.3

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CK)	t_{PWL}	0.90	1.67
Pulse Width High (CK)	t_{PWH}	0.87	1.09
Input Setup Time (D0 to CK)	t_{SU}	0.33	0.36
Input Hold Time (D0 to CK)	t_{HD}	0.66	0.63
Input Setup Time (D1 to CK)	t_{SU}	0.33	0.36
Input Hold Time (D1 to CK)	t_{HD}	0.66	0.63
Input Setup Time (D2 to CK)	t_{SU}	0.33	0.36
Input Hold Time (D2 to CK)	t_{HD}	0.66	0.63
Input Setup Time (D3 to CK)	t_{SU}	0.33	0.36
Input Hold Time (D3 to CK)	t_{HD}	0.66	0.63

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.79	0.74 + 0.028*SL	0.74 + 0.024*SL	0.75 + 0.024*SL
	t_{PHL}	1.08	1.00 + 0.041*SL	1.01 + 0.038*SL	1.01 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to Q1	t_{PLH}	0.79	0.74 + 0.028*SL	0.74 + 0.024*SL	0.75 + 0.024*SL
	t_{PHL}	1.08	1.00 + 0.041*SL	1.01 + 0.038*SL	1.01 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to Q2	t_{PLH}	0.79	0.74 + 0.028*SL	0.74 + 0.024*SL	0.75 + 0.024*SL
	t_{PHL}	1.08	1.00 + 0.041*SL	1.01 + 0.038*SL	1.01 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to Q3	t_{PLH}	0.79	0.74 + 0.028*SL	0.74 + 0.024*SL	0.75 + 0.024*SL
	t_{PHL}	1.08	1.00 + 0.041*SL	1.01 + 0.038*SL	1.01 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to QN0	t_{PLH}	1.12	1.07 + 0.025*SL	1.07 + 0.024*SL	1.07 + 0.024*SL
	t_{PHL}	0.96	0.88 + 0.038*SL	0.88 + 0.037*SL	0.88 + 0.037*SL
	t_R	0.19	0.09 + 0.046*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
CK to QN1	t_{PLH}	1.12	1.07 + 0.025*SL	1.07 + 0.024*SL	1.07 + 0.024*SL
	t_{PHL}	0.96	0.88 + 0.037*SL	0.88 + 0.037*SL	0.88 + 0.037*SL
	t_R	0.19	0.10 + 0.043*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
CK to QN2	t_{PLH}	1.12	1.07 + 0.025*SL	1.07 + 0.024*SL	1.07 + 0.024*SL
	t_{PHL}	0.96	0.88 + 0.038*SL	0.88 + 0.037*SL	0.88 + 0.037*SL
	t_R	0.19	0.09 + 0.045*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
CK to QN3	t_{PLH}	1.12	1.07 + 0.025*SL	1.07 + 0.024*SL	1.07 + 0.024*SL
	t_{PHL}	0.96	0.88 + 0.038*SL	0.88 + 0.037*SL	0.88 + 0.037*SL
	t_R	0.18	0.09 + 0.045*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.068*SL	0.06 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

FD1X4

4-Bit D Flip-Flop

Switching Characteristics

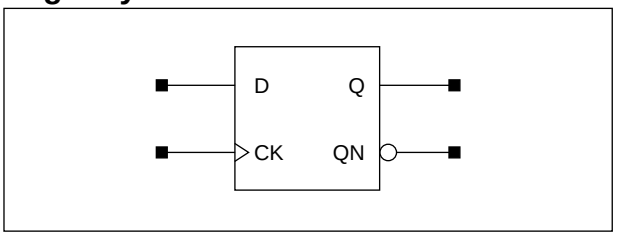
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.08	1.00 + 0.038*SL	1.01 + 0.035*SL	1.02 + 0.034*SL
	t_{PHL}	1.53	1.43 + 0.052*SL	1.45 + 0.046*SL	1.46 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.078*SL	0.14 + 0.080*SL	0.13 + 0.081*SL
CK to Q1	t_{PLH}	1.08	1.00 + 0.038*SL	1.01 + 0.035*SL	1.02 + 0.034*SL
	t_{PHL}	1.53	1.43 + 0.052*SL	1.44 + 0.046*SL	1.46 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.082*SL
CK to Q2	t_{PLH}	1.08	1.00 + 0.038*SL	1.01 + 0.035*SL	1.02 + 0.034*SL
	t_{PHL}	1.53	1.43 + 0.052*SL	1.45 + 0.046*SL	1.46 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.082*SL
CK to Q3	t_{PLH}	1.08	1.00 + 0.038*SL	1.01 + 0.035*SL	1.02 + 0.033*SL
	t_{PHL}	1.53	1.43 + 0.052*SL	1.44 + 0.046*SL	1.46 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.15 + 0.079*SL	0.14 + 0.080*SL	0.13 + 0.081*SL
CK to QN0	t_{PLH}	1.60	1.53 + 0.035*SL	1.54 + 0.033*SL	1.54 + 0.033*SL
	t_{PHL}	1.31	1.21 + 0.046*SL	1.22 + 0.045*SL	1.22 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
CK to QN1	t_{PLH}	1.60	1.53 + 0.035*SL	1.54 + 0.033*SL	1.54 + 0.033*SL
	t_{PHL}	1.31	1.21 + 0.047*SL	1.22 + 0.045*SL	1.22 + 0.044*SL
	t_R	0.26	0.13 + 0.066*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.13 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
CK to QN2	t_{PLH}	1.60	1.53 + 0.035*SL	1.54 + 0.033*SL	1.54 + 0.033*SL
	t_{PHL}	1.31	1.21 + 0.046*SL	1.22 + 0.045*SL	1.22 + 0.044*SL
	t_R	0.26	0.13 + 0.066*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
CK to QN3	t_{PLH}	1.60	1.53 + 0.035*SL	1.54 + 0.033*SL	1.53 + 0.033*SL
	t_{PHL}	1.30	1.21 + 0.047*SL	1.22 + 0.044*SL	1.22 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.10 + 0.083*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



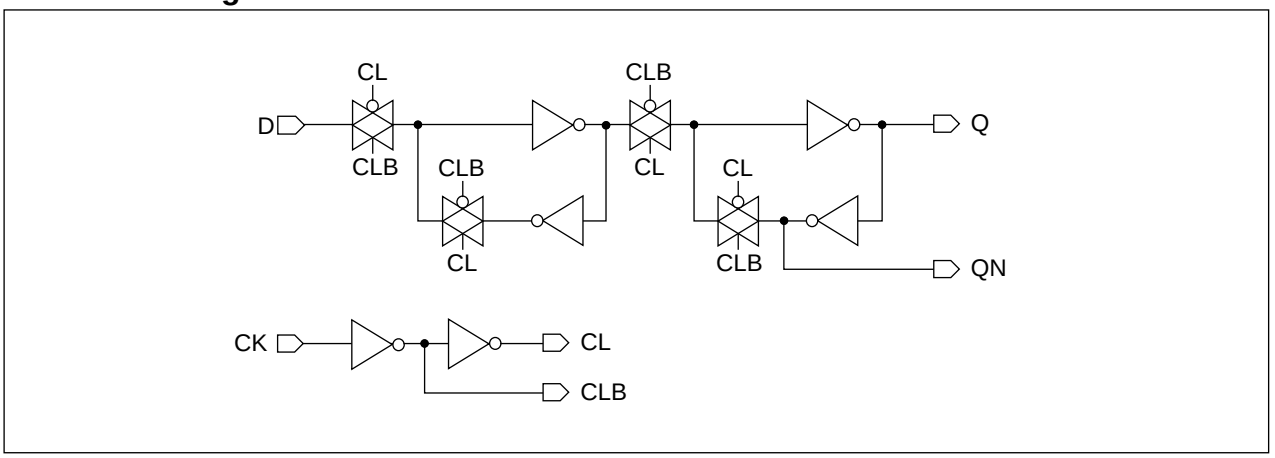
Truth Table

D	CK	Q (n+1)	QN (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
STD80					
YFD1		*YFD1D2*		*YFD1*	*YFD1D2*
D	CK	D	CK		
1.7	0.5	1.7	0.5	4.0	5.0
STDM80					
YFD1		*YFD1D2*		*YFD1*	*YFD1D2*
D	CK	D	CK		
2.0	0.6	2.0	0.6	4.0	5.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		YFD1	YFD1D2	YFD1	YFD1D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.87	0.96
Input Setup Time (D to CK)	t_{SU}	0.38	0.38	0.41	0.38
Input Hold Time (D to CK)	t_{HD}	0.46	0.46	0.49	0.49

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44, SL: Standard Load)

STD80 YFD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.48	0.43 + 0.027*SL	0.44 + 0.025*SL	0.44 + 0.024*SL
	t_{PHL}	0.58	0.49 + 0.043*SL	0.50 + 0.039*SL	0.52 + 0.037*SL
	t_R	0.26	0.17 + 0.044*SL	0.16 + 0.049*SL	0.13 + 0.052*SL
	t_F	0.35	0.23 + 0.061*SL	0.22 + 0.065*SL	0.18 + 0.069*SL
CK to QN	t_{PLH}	0.71	0.55 + 0.081*SL	0.56 + 0.077*SL	0.57 + 0.075*SL
	t_{PHL}	0.66	0.51 + 0.075*SL	0.51 + 0.072*SL	0.52 + 0.072*SL
	t_R	0.23	0.11 + 0.063*SL	0.10 + 0.064*SL	0.09 + 0.065*SL
	t_F	0.24	0.08 + 0.076*SL	0.08 + 0.076*SL	0.08 + 0.076*SL

STD80 YFD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.50	0.47 + 0.017*SL	0.48 + 0.014*SL	0.49 + 0.012*SL
	t_{PHL}	0.62	0.57 + 0.025*SL	0.58 + 0.022*SL	0.61 + 0.018*SL
	t_R	0.23	0.19 + 0.019*SL	0.18 + 0.023*SL	0.16 + 0.026*SL
	t_F	0.34	0.28 + 0.029*SL	0.28 + 0.030*SL	0.24 + 0.033*SL
CK to QN	t_{PLH}	0.71	0.62 + 0.045*SL	0.63 + 0.041*SL	0.66 + 0.037*SL
	t_{PHL}	0.62	0.54 + 0.039*SL	0.54 + 0.037*SL	0.56 + 0.036*SL
	t_R	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.10 + 0.032*SL
	t_F	0.15	0.08 + 0.038*SL	0.08 + 0.037*SL	0.07 + 0.038*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40, SL: Standard Load)

STDM80 YFD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.62 + 0.038*SL	0.63 + 0.035*SL	0.64 + 0.034*SL
	t_{PHL}	0.83	0.71 + 0.057*SL	0.73 + 0.050*SL	0.76 + 0.046*SL
	t_R	0.36	0.22 + 0.066*SL	0.22 + 0.069*SL	0.20 + 0.071*SL
	t_F	0.46	0.31 + 0.078*SL	0.30 + 0.079*SL	0.30 + 0.079*SL
CK to QN	t_{PLH}	1.02	0.80 + 0.112*SL	0.82 + 0.104*SL	0.85 + 0.101*SL
	t_{PHL}	0.93	0.73 + 0.100*SL	0.74 + 0.097*SL	0.74 + 0.096*SL
	t_R	0.32	0.15 + 0.085*SL	0.15 + 0.085*SL	0.14 + 0.086*SL
	t_F	0.30	0.12 + 0.094*SL	0.11 + 0.094*SL	0.11 + 0.095*SL

STDM80 YFD1D2

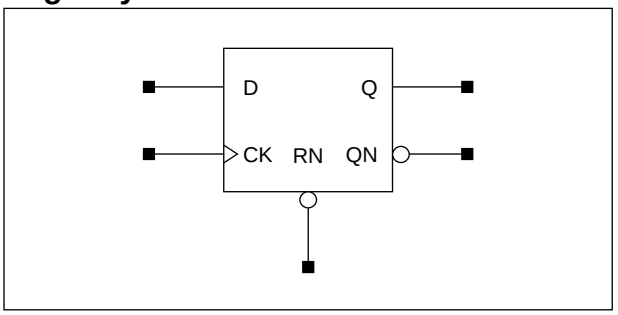
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.72	0.67 + 0.022*SL	0.68 + 0.020*SL	0.69 + 0.018*SL
	t_{PHL}	0.91	0.84 + 0.034*SL	0.85 + 0.031*SL	0.88 + 0.027*SL
	t_R	0.30	0.24 + 0.030*SL	0.23 + 0.033*SL	0.23 + 0.034*SL
	t_F	0.45	0.38 + 0.037*SL	0.38 + 0.038*SL	0.38 + 0.038*SL
CK to QN	t_{PLH}	1.05	0.92 + 0.063*SL	0.94 + 0.058*SL	0.97 + 0.054*SL
	t_{PHL}	0.87	0.76 + 0.054*SL	0.78 + 0.050*SL	0.79 + 0.049*SL
	t_R	0.22	0.14 + 0.041*SL	0.14 + 0.042*SL	0.14 + 0.042*SL
	t_F	0.19	0.10 + 0.045*SL	0.10 + 0.046*SL	0.10 + 0.046*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

FD2/FD2D2

D Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



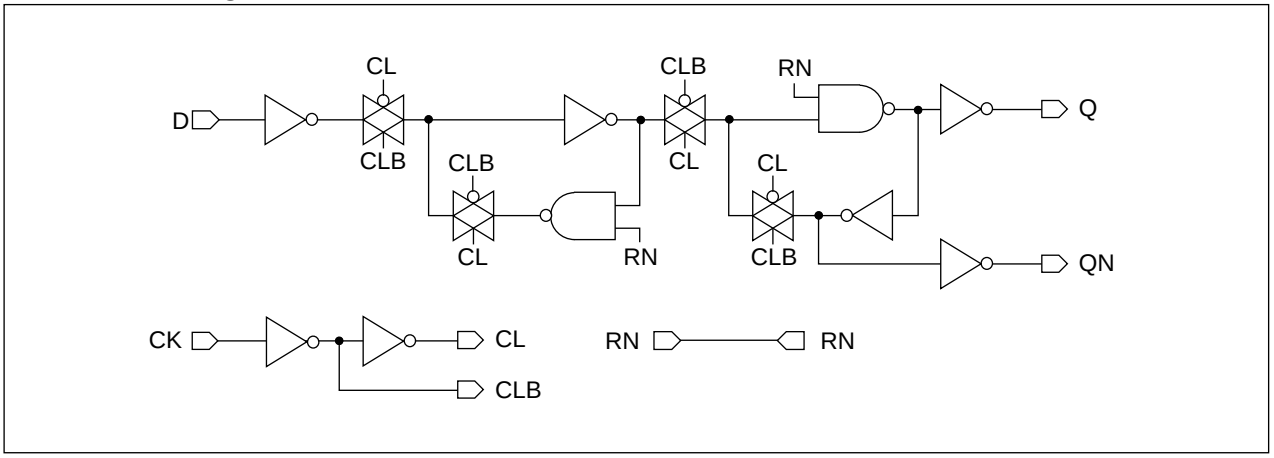
Truth Table

D	CK	RN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
STD80							
FD2			*FD2D2*			*FD2*	*FD2D2*
D	CK	RN	D	CK	RN		
0.5	0.5	0.7	0.5	0.5	0.7	6.3	7.0
STDM80							
FD2			*FD2D2*			*FD2*	*FD2D2*
D	CK	RN	D	CK	RN		
0.6	0.6	1.4	0.6	0.6	1.4	6.3	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD2	FD2D2	FD2	FD2D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.90	0.90
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.46	0.46	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66	0.76	0.76

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.57 + 0.032*SL	0.58 + 0.026*SL	0.60 + 0.024*SL
	t_{PHL}	0.68	0.60 + 0.042*SL	0.61 + 0.038*SL	0.62 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.72	0.67 + 0.026*SL	0.68 + 0.024*SL	0.68 + 0.024*SL
	t_{PHL}	0.81	0.73 + 0.037*SL	0.73 + 0.037*SL	0.73 + 0.037*SL
	t_R	0.18	0.09 + 0.045*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.40	0.35 + 0.025*SL	0.36 + 0.024*SL	0.36 + 0.023*SL
	t_R	0.18	0.09 + 0.045*SL	0.08 + 0.050*SL	0.06 + 0.052*SL

STD80 FD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.60 + 0.021*SL	0.61 + 0.016*SL	0.65 + 0.012*SL
	t_{PHL}	0.67	0.63 + 0.023*SL	0.63 + 0.020*SL	0.65 + 0.018*SL
	t_R	0.20	0.14 + 0.026*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.18	0.11 + 0.031*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
RN to Q	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.020*SL	0.33 + 0.018*SL
	t_F	0.18	0.11 + 0.033*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
CK to QN	t_{PLH}	0.79	0.76 + 0.014*SL	0.76 + 0.012*SL	0.77 + 0.012*SL
	t_{PHL}	0.89	0.85 + 0.017*SL	0.85 + 0.017*SL	0.84 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
RN to QN	t_{PLH}	0.47	0.44 + 0.015*SL	0.45 + 0.012*SL	0.45 + 0.012*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

FD2/FD2D2

D Flip-Flop with Reset, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD2

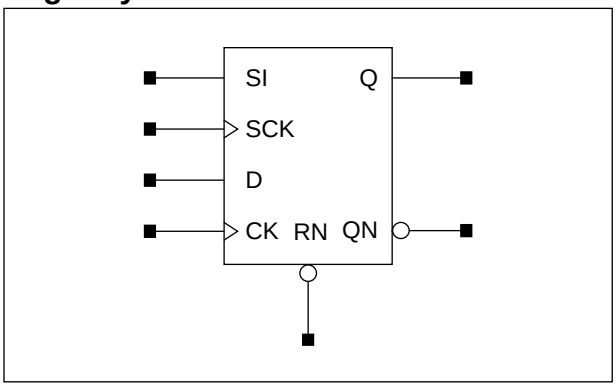
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.90	0.81 + 0.044*SL	0.83 + 0.037*SL	0.85 + 0.035*SL
	t_{PHL}	0.97	0.86 + 0.052*SL	0.88 + 0.046*SL	0.89 + 0.044*SL
	t_R	0.32	0.18 + 0.071*SL	0.18 + 0.068*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
RN to Q	t_{PHL}	0.47	0.37 + 0.052*SL	0.38 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
CK to QN	t_{PLH}	1.04	0.97 + 0.035*SL	0.98 + 0.033*SL	0.98 + 0.033*SL
	t_{PHL}	1.14	1.04 + 0.047*SL	1.05 + 0.044*SL	1.05 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
RN to QN	t_{PLH}	0.55	0.48 + 0.035*SL	0.48 + 0.033*SL	0.48 + 0.033*SL
	t_R	0.26	0.12 + 0.066*SL	0.11 + 0.070*SL	0.10 + 0.072*SL

STDM80 FD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.91	0.86 + 0.028*SL	0.87 + 0.023*SL	0.90 + 0.019*SL
	t_{PHL}	0.96	0.89 + 0.031*SL	0.91 + 0.026*SL	0.93 + 0.023*SL
	t_R	0.25	0.17 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.041*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
RN to Q	t_{PHL}	0.46	0.40 + 0.031*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_F	0.22	0.13 + 0.041*SL	0.14 + 0.039*SL	0.15 + 0.038*SL
CK to QN	t_{PLH}	1.13	1.09 + 0.019*SL	1.10 + 0.017*SL	1.10 + 0.017*SL
	t_{PHL}	1.25	1.20 + 0.024*SL	1.21 + 0.022*SL	1.21 + 0.021*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.037*SL	0.14 + 0.038*SL
RN to QN	t_{PLH}	0.63	0.60 + 0.019*SL	0.60 + 0.017*SL	0.61 + 0.017*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Logic Symbol



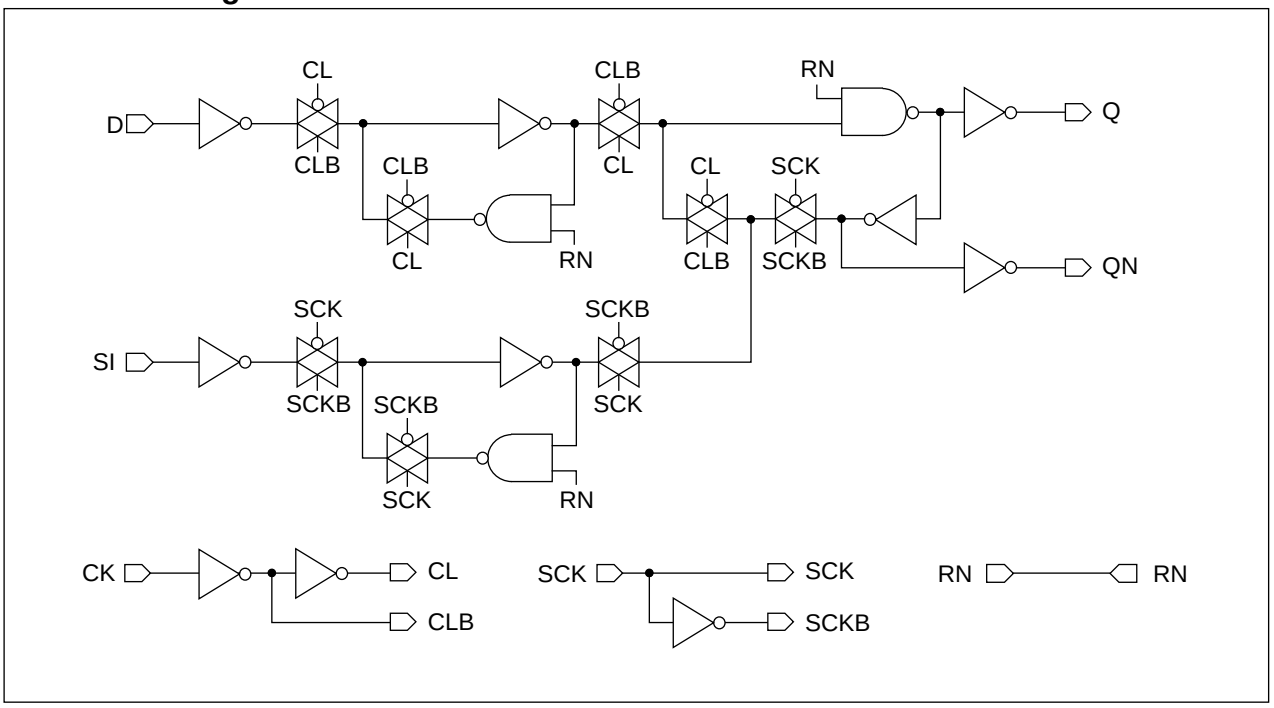
Truth Table

SI	SCK	D	CK	RN	Q (n+1)	QN (n+1)
x	0	0	↑	1	0	1
x	0	1	↑	1	1	0
0	↑	x	0	1	0	1
1	↑	x	0	1	1	0
x	x	x	x	0	0	1

Cell Data

Input Load (SL)										Gate Count	
STD80											
FD2CS					*FD2CSD2*					*FD2CS*	*FD2CSD2*
SI	SCK	D	CK	RN	SI	SCK	D	CK	RN		
0.6	1.8	0.6	0.6	1.8	0.6	1.8	0.6	0.6	1.8	10.3	10.7
STDM80											
FD2CS					*FD2CSD2*					*FD2CS*	*FD2CSD2*
SI	SCK	D	CK	RN	SI	SCK	D	CK	RN		
0.6	1.8	0.6	0.6	1.9	0.6	1.8	0.6	0.6	1.9	10.3	10.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD2CS	FD2CSD2	FD2CS	FD2CSD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.90	0.90
Pulse Width High (CK)	t_{PWH}	0.87	0.97	0.82	0.85
Pulse Width Low (SCK)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width High (SCK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.46	0.46	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.64	0.64	0.85	0.85
Input Hold Time (SI to SCK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN to CK)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66	0.76	0.76
Recovery Time (RN to SCK)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to SCK)	t_{HD}	0.49	0.49	0.55	0.49

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD2CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.65	0.59 + 0.031*SL	0.60 + 0.026*SL	0.62 + 0.024*SL
	t_{PHL}	0.66	0.58 + 0.041*SL	0.59 + 0.038*SL	0.60 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.13 + 0.049*SL	0.11 + 0.052*SL
	t_F	0.24	0.11 + 0.065*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SCK to Q	t_{PLH}	0.74	0.67 + 0.033*SL	0.68 + 0.026*SL	0.71 + 0.024*SL
	t_{PHL}	0.59	0.51 + 0.042*SL	0.52 + 0.038*SL	0.53 + 0.037*SL
	t_R	0.26	0.16 + 0.047*SL	0.16 + 0.047*SL	0.12 + 0.052*SL
	t_F	0.25	0.12 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PHL}	0.38	0.30 + 0.040*SL	0.31 + 0.038*SL	0.32 + 0.037*SL
	t_F	0.25	0.12 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.76	0.70 + 0.029*SL	0.71 + 0.025*SL	0.72 + 0.024*SL
	t_{PHL}	0.90	0.82 + 0.040*SL	0.83 + 0.038*SL	0.84 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.25	0.12 + 0.064*SL	0.12 + 0.067*SL	0.09 + 0.069*SL
SCK to QN	t_{PLH}	0.62	0.58 + 0.024*SL	0.58 + 0.023*SL	0.58 + 0.024*SL
	t_{PHL}	0.91	0.84 + 0.037*SL	0.84 + 0.037*SL	0.84 + 0.037*SL
	t_R	0.19	0.09 + 0.047*SL	0.09 + 0.050*SL	0.07 + 0.052*SL
	t_F	0.22	0.10 + 0.065*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.49	0.43 + 0.029*SL	0.44 + 0.025*SL	0.45 + 0.024*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.049*SL	0.09 + 0.052*SL

STD80 FD2CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.68	0.63 + 0.021*SL	0.65 + 0.016*SL	0.68 + 0.012*SL
	t_{PHL}	0.66	0.62 + 0.023*SL	0.62 + 0.020*SL	0.64 + 0.018*SL
	t_R	0.20	0.16 + 0.023*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SCK to Q	t_{PLH}	0.77	0.72 + 0.022*SL	0.74 + 0.016*SL	0.77 + 0.012*SL
	t_{PHL}	0.59	0.55 + 0.023*SL	0.55 + 0.020*SL	0.57 + 0.018*SL
	t_R	0.22	0.18 + 0.022*SL	0.18 + 0.023*SL	0.15 + 0.025*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
RN to Q	t_{PHL}	0.38	0.33 + 0.023*SL	0.34 + 0.020*SL	0.35 + 0.018*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
CK to QN	t_{PLH}	0.83	0.80 + 0.017*SL	0.80 + 0.014*SL	0.82 + 0.012*SL
	t_{PHL}	0.99	0.95 + 0.020*SL	0.96 + 0.018*SL	0.96 + 0.018*SL
	t_R	0.18	0.14 + 0.023*SL	0.14 + 0.022*SL	0.11 + 0.026*SL
	t_F	0.20	0.14 + 0.031*SL	0.14 + 0.031*SL	0.11 + 0.034*SL
SCK to QN	t_{PLH}	0.70	0.67 + 0.013*SL	0.68 + 0.012*SL	0.68 + 0.012*SL
	t_{PHL}	1.01	0.98 + 0.016*SL	0.98 + 0.017*SL	0.97 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.11 + 0.022*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
RN to QN	t_{PLH}	0.55	0.51 + 0.017*SL	0.52 + 0.014*SL	0.54 + 0.012*SL
	t_R	0.18	0.14 + 0.023*SL	0.14 + 0.023*SL	0.10 + 0.026*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD2CS

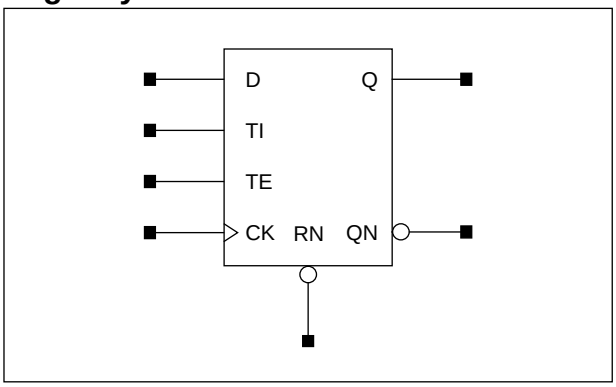
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.94	0.85 + 0.044*SL	0.87 + 0.037*SL	0.89 + 0.035*SL
	t_{PHL}	0.94	0.84 + 0.051*SL	0.85 + 0.047*SL	0.87 + 0.045*SL
	t_R	0.32	0.18 + 0.069*SL	0.18 + 0.069*SL	0.18 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.14 + 0.082*SL
SCK to Q	t_{PLH}	1.11	1.02 + 0.045*SL	1.04 + 0.038*SL	1.07 + 0.035*SL
	t_{PHL}	0.83	0.73 + 0.053*SL	0.75 + 0.047*SL	0.76 + 0.044*SL
	t_R	0.35	0.21 + 0.069*SL	0.22 + 0.067*SL	0.20 + 0.069*SL
	t_F	0.32	0.16 + 0.079*SL	0.16 + 0.079*SL	0.14 + 0.081*SL
RN to Q	t_{PHL}	0.50	0.39 + 0.052*SL	0.41 + 0.047*SL	0.42 + 0.045*SL
	t_F	0.31	0.15 + 0.081*SL	0.15 + 0.081*SL	0.14 + 0.081*SL
CK to QN	t_{PLH}	1.09	1.01 + 0.042*SL	1.02 + 0.036*SL	1.04 + 0.034*SL
	t_{PHL}	1.29	1.18 + 0.052*SL	1.20 + 0.048*SL	1.21 + 0.046*SL
	t_R	0.30	0.16 + 0.070*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.33	0.16 + 0.084*SL	0.17 + 0.082*SL	0.17 + 0.081*SL
SCK to QN	t_{PLH}	0.90	0.83 + 0.034*SL	0.83 + 0.033*SL	0.83 + 0.033*SL
	t_{PHL}	1.35	1.25 + 0.046*SL	1.26 + 0.044*SL	1.26 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.12 + 0.071*SL	0.11 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.13 + 0.081*SL	0.11 + 0.082*SL
RN to QN	t_{PLH}	0.65	0.56 + 0.042*SL	0.58 + 0.036*SL	0.60 + 0.033*SL
	t_R	0.30	0.16 + 0.070*SL	0.17 + 0.068*SL	0.16 + 0.070*SL

STDM80 FD2CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.97	0.92 + 0.028*SL	0.93 + 0.023*SL	0.96 + 0.020*SL
	t_{PHL}	0.94	0.88 + 0.031*SL	0.89 + 0.026*SL	0.91 + 0.023*SL
	t_R	0.26	0.19 + 0.035*SL	0.19 + 0.034*SL	0.19 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.039*SL
SCK to Q	t_{PLH}	1.16	1.10 + 0.029*SL	1.12 + 0.023*SL	1.14 + 0.020*SL
	t_{PHL}	0.84	0.77 + 0.031*SL	0.79 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.29	0.22 + 0.034*SL	0.22 + 0.034*SL	0.22 + 0.033*SL
	t_F	0.23	0.15 + 0.039*SL	0.15 + 0.039*SL	0.15 + 0.038*SL
RN to Q	t_{PHL}	0.49	0.42 + 0.031*SL	0.44 + 0.026*SL	0.46 + 0.023*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.039*SL	0.15 + 0.038*SL
CK to QN	t_{PLH}	1.18	1.13 + 0.023*SL	1.14 + 0.020*SL	1.16 + 0.018*SL
	t_{PHL}	1.41	1.36 + 0.027*SL	1.37 + 0.024*SL	1.37 + 0.023*SL
	t_R	0.23	0.16 + 0.035*SL	0.17 + 0.033*SL	0.17 + 0.033*SL
	t_F	0.24	0.16 + 0.042*SL	0.17 + 0.040*SL	0.18 + 0.038*SL
SCK to QN	t_{PLH}	1.00	0.96 + 0.018*SL	0.97 + 0.017*SL	0.97 + 0.017*SL
	t_{PHL}	1.49	1.45 + 0.022*SL	1.45 + 0.021*SL	1.45 + 0.021*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
RN to QN	t_{PLH}	0.73	0.69 + 0.023*SL	0.69 + 0.020*SL	0.71 + 0.018*SL
	t_R	0.23	0.16 + 0.037*SL	0.17 + 0.033*SL	0.17 + 0.033*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Logic Symbol



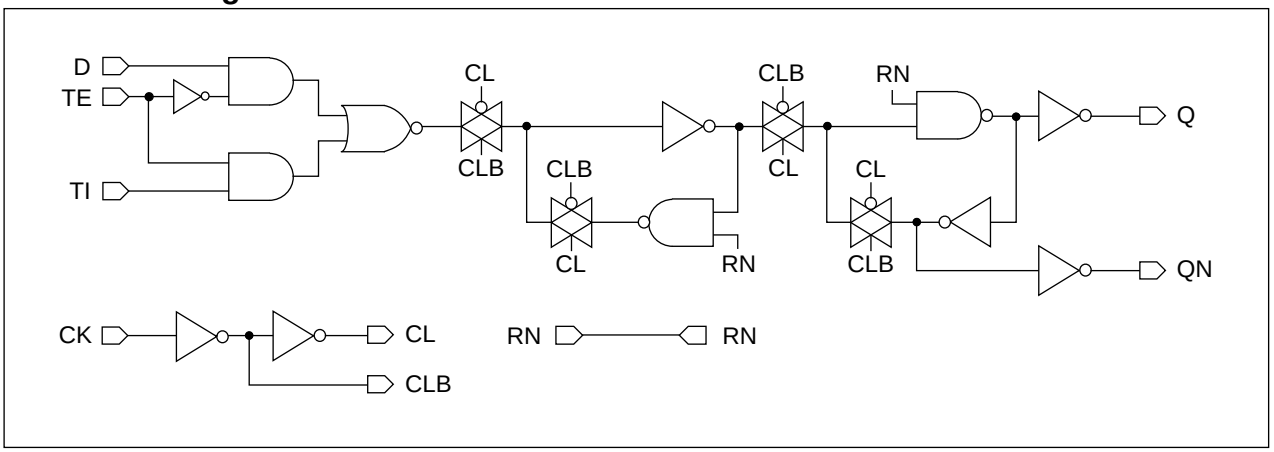
Truth Table

D	TI	TE	CK	RN	Q (n+1)	QN (n+1)
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	0	1

Cell Data

Input Load (SL)										Gate Count	
STD80											
FD2S					*FD2SD2*					*FD2S*	*FD2SD2*
D	TI	TE	CK	RN	D	TI	TE	CK	RN		
0.3	0.5	0.9	0.5	0.7	0.3	0.5	0.9	0.5	0.7	8.0	8.7
STDM80											
FD2S					*FD2SD2*					*FD2S*	*FD2SD2*
D	TI	TE	CK	RN	D	TI	TE	CK	RN		
0.6	0.6	1.1	0.6	1.4	0.6	0.6	1.1	0.6	1.4	8.0	8.7

Schematic Diagram



FD2S/FD2SD2

D Flip-Flop with Reset, Scan, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD2S	FD2SD2	FD2S	FD2SD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.96	0.96
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.60	0.60	0.79	0.79
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.63	0.63	0.85	0.85
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.68	0.68	0.90	0.90
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66	0.76	0.76

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.58 + 0.032*SL	0.59 + 0.026*SL	0.61 + 0.024*SL
	t_{PHL}	0.70	0.62 + 0.042*SL	0.63 + 0.038*SL	0.63 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.74	0.69 + 0.025*SL	0.70 + 0.024*SL	0.69 + 0.024*SL
	t_{PHL}	0.82	0.74 + 0.037*SL	0.74 + 0.037*SL	0.74 + 0.037*SL
	t_R	0.18	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.40	0.35 + 0.025*SL	0.36 + 0.024*SL	0.36 + 0.023*SL
	t_R	0.18	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL

STD80 FD2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.65	0.61 + 0.021*SL	0.62 + 0.015*SL	0.66 + 0.012*SL
	t_{PHL}	0.69	0.65 + 0.023*SL	0.65 + 0.020*SL	0.67 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
RN to Q	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.020*SL	0.33 + 0.018*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
CK to QN	t_{PLH}	0.81	0.78 + 0.014*SL	0.78 + 0.012*SL	0.79 + 0.012*SL
	t_{PHL}	0.90	0.86 + 0.018*SL	0.87 + 0.017*SL	0.86 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
RN to QN	t_{PLH}	0.47	0.44 + 0.015*SL	0.45 + 0.012*SL	0.45 + 0.012*SL
	t_R	0.15	0.11 + 0.022*SL	0.10 + 0.023*SL	0.07 + 0.026*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.91	0.83 + 0.044*SL	0.84 + 0.038*SL	0.87 + 0.035*SL
	t_{PHL}	0.99	0.89 + 0.052*SL	0.91 + 0.046*SL	0.92 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
RN to Q	t_{PHL}	0.47	0.37 + 0.052*SL	0.38 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
CK to QN	t_{PLH}	1.07	1.00 + 0.035*SL	1.00 + 0.033*SL	1.00 + 0.033*SL
	t_{PHL}	1.15	1.06 + 0.047*SL	1.07 + 0.044*SL	1.07 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
RN to QN	t_{PLH}	0.55	0.48 + 0.035*SL	0.48 + 0.033*SL	0.48 + 0.033*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL

STDM80 FD2SD2

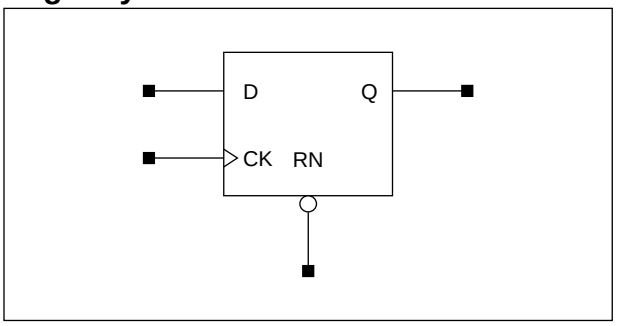
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.93	0.87 + 0.028*SL	0.89 + 0.023*SL	0.91 + 0.020*SL
	t_{PHL}	0.98	0.92 + 0.031*SL	0.93 + 0.026*SL	0.95 + 0.023*SL
	t_R	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.041*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
RN to Q	t_{PHL}	0.46	0.40 + 0.031*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_F	0.22	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
CK to QN	t_{PLH}	1.15	1.12 + 0.019*SL	1.12 + 0.017*SL	1.13 + 0.017*SL
	t_{PHL}	1.26	1.21 + 0.024*SL	1.22 + 0.022*SL	1.22 + 0.021*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.22	0.13 + 0.041*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
RN to QN	t_{PLH}	0.63	0.60 + 0.019*SL	0.60 + 0.017*SL	0.61 + 0.017*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

FD2Q/FD2QD2

D Flip-Flop with Reset, Q Output Only, 1X/2X Drive

Logic Symbol



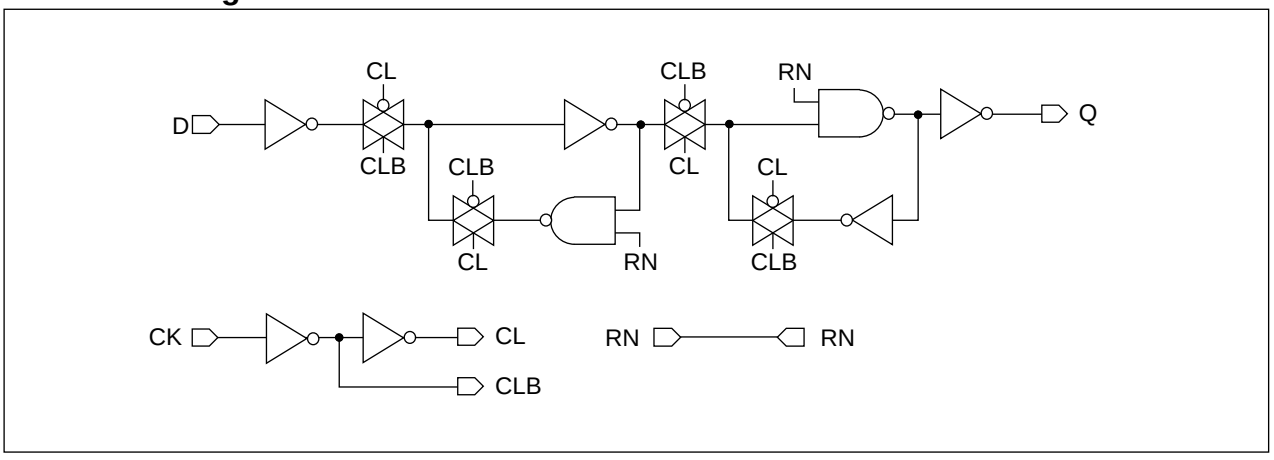
Truth Table

D	CK	RN	Q (n+1)
0	↑	1	0
1	↑	1	1
x	x	0	0
x	↓	x	Q (n)

Cell Data

Input Load (SL)						Gate Count	
STD80							
FD2Q			*FD2QD2*			*FD2Q*	*FD2QD2*
D	CK	RN	D	CK	RN		
0.6	0.6	1.1	0.6	0.6	1.1	6.0	6.3
STDM80							
FD2Q			*FD2QD2*			*FD2Q*	*FD2QD2*
D	CK	RN	D	CK	RN		
0.6	0.6	1.2	0.6	0.6	1.2	6.0	6.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD2Q	FD2QD2	FD2Q	FD2QD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.90	0.90
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.46	0.46	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66	0.76	0.76

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD2Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.62	0.56 + 0.031*SL	0.57 + 0.026*SL	0.59 + 0.024*SL
	t_{PHL}	0.67	0.59 + 0.041*SL	0.60 + 0.037*SL	0.60 + 0.037*SL
	t_R	0.22	0.13 + 0.048*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to Q	t_{PHL}	0.36	0.28 + 0.040*SL	0.28 + 0.037*SL	0.29 + 0.037*SL
	t_F	0.24	0.11 + 0.061*SL	0.10 + 0.066*SL	0.07 + 0.069*SL

STD80 FD2QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.60 + 0.020*SL	0.61 + 0.015*SL	0.64 + 0.012*SL
	t_{PHL}	0.66	0.62 + 0.023*SL	0.63 + 0.019*SL	0.64 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.024*SL	0.12 + 0.026*SL
	t_F	0.17	0.12 + 0.029*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
RN to Q	t_{PHL}	0.35	0.30 + 0.023*SL	0.31 + 0.019*SL	0.33 + 0.018*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD2Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.90	0.81 + 0.043*SL	0.83 + 0.037*SL	0.85 + 0.034*SL
	t_{PHL}	0.95	0.85 + 0.051*SL	0.86 + 0.046*SL	0.88 + 0.044*SL
	t_R	0.31	0.17 + 0.069*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.078*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
RN to Q	t_{PHL}	0.46	0.36 + 0.050*SL	0.37 + 0.046*SL	0.38 + 0.045*SL
	t_F	0.30	0.14 + 0.079*SL	0.13 + 0.081*SL	0.13 + 0.082*SL

STDM80 FD2QD2

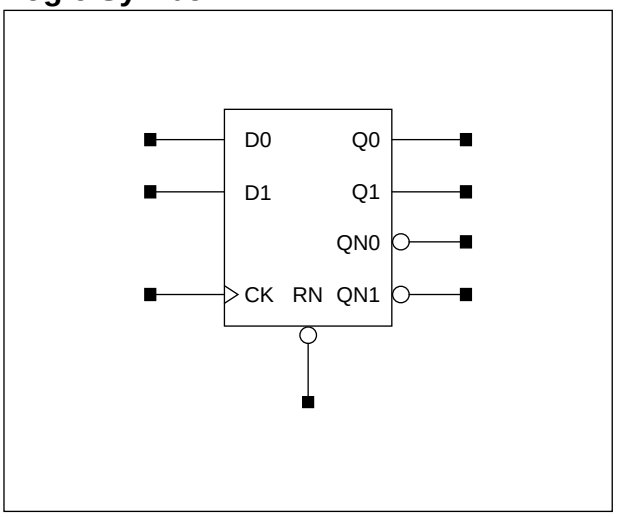
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.91	0.86 + 0.027*SL	0.87 + 0.023*SL	0.89 + 0.019*SL
	t_{PHL}	0.94	0.88 + 0.031*SL	0.90 + 0.026*SL	0.92 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.18 + 0.035*SL	0.19 + 0.034*SL
	t_F	0.22	0.14 + 0.039*SL	0.15 + 0.038*SL	0.14 + 0.038*SL
RN to Q	t_{PHL}	0.45	0.39 + 0.031*SL	0.40 + 0.026*SL	0.42 + 0.023*SL
	t_F	0.21	0.13 + 0.039*SL	0.14 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

FD2X2

2-Bit D Flip-Flop with Reset

Logic Symbol



Truth Table

Dn	CK	RN	Qn (n+1)	QNn (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
STD80			
Dn	CK	RN	
0.5	0.5	1.5	11.7
STDM80			
Dn	CK	RN	
0.6	0.6	2.4	11.7

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CK)	t_{PWL}	0.87	1.09
Pulse Width High (CK)	t_{PWH}	0.96	0.85
Pulse Width Low (RN)	t_{PWL}	0.87	0.82
Input Setup Time (D0 to CK)	t_{SU}	0.36	0.46
Input Hold Time (D0 to CK)	t_{HD}	0.41	0.41
Input Setup Time (D1 to CK)	t_{SU}	0.36	0.46
Input Hold Time (D1 to CK)	t_{HD}	0.41	0.41
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.76	0.87

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD2X2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.72	0.65 + 0.032*SL	0.66 + 0.026*SL	0.69 + 0.024*SL
	t_{PHL}	0.85	0.77 + 0.041*SL	0.78 + 0.038*SL	0.78 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q0	t_{PHL}	0.37	0.29 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to Q1	t_{PLH}	0.71	0.65 + 0.032*SL	0.66 + 0.026*SL	0.68 + 0.024*SL
	t_{PHL}	0.85	0.77 + 0.042*SL	0.78 + 0.038*SL	0.78 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q1	t_{PHL}	0.37	0.28 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to QN0	t_{PLH}	0.89	0.84 + 0.025*SL	0.85 + 0.023*SL	0.84 + 0.024*SL
	t_{PHL}	0.89	0.82 + 0.037*SL	0.82 + 0.037*SL	0.82 + 0.037*SL
	t_R	0.19	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN0	t_{PLH}	0.41	0.36 + 0.025*SL	0.36 + 0.024*SL	0.37 + 0.023*SL
	t_R	0.19	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
CK to QN1	t_{PLH}	0.89	0.84 + 0.025*SL	0.84 + 0.024*SL	0.84 + 0.024*SL
	t_{PHL}	0.89	0.82 + 0.037*SL	0.82 + 0.037*SL	0.81 + 0.037*SL
	t_R	0.18	0.09 + 0.045*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN1	t_{PLH}	0.41	0.35 + 0.026*SL	0.36 + 0.023*SL	0.36 + 0.023*SL
	t_R	0.18	0.09 + 0.047*SL	0.09 + 0.050*SL	0.06 + 0.052*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

FD2X2

2-Bit D Flip-Flop with Reset

Switching Characteristics

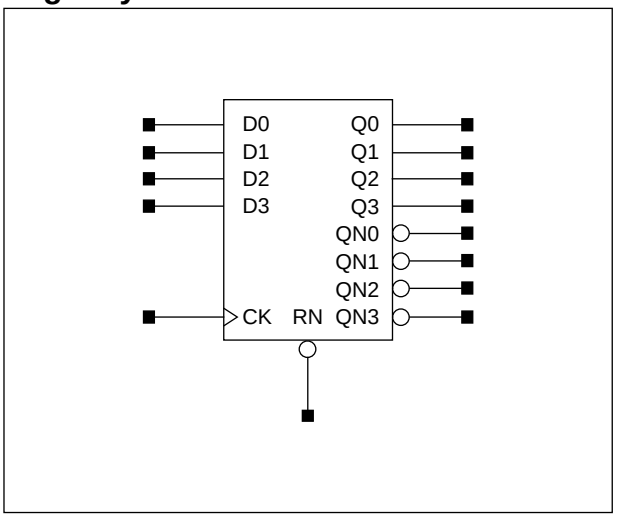
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD2X2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.00	0.92 + 0.044*SL	0.94 + 0.038*SL	0.96 + 0.035*SL
	t_{PHL}	1.20	1.10 + 0.052*SL	1.12 + 0.046*SL	1.13 + 0.044*SL
	t_R	0.32	0.18 + 0.071*SL	0.18 + 0.068*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to Q0	t_{PHL}	0.48	0.37 + 0.052*SL	0.39 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.14 + 0.081*SL
CK to Q1	t_{PLH}	1.00	0.91 + 0.044*SL	0.93 + 0.038*SL	0.95 + 0.035*SL
	t_{PHL}	1.20	1.10 + 0.052*SL	1.11 + 0.046*SL	1.13 + 0.045*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to Q1	t_{PHL}	0.47	0.37 + 0.052*SL	0.38 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
CK to QN0	t_{PLH}	1.28	1.21 + 0.035*SL	1.22 + 0.033*SL	1.22 + 0.033*SL
	t_{PHL}	1.25	1.15 + 0.046*SL	1.16 + 0.045*SL	1.16 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.14 + 0.076*SL	0.13 + 0.080*SL	0.11 + 0.082*SL
RN to QN0	t_{PLH}	0.56	0.48 + 0.035*SL	0.49 + 0.033*SL	0.49 + 0.033*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
CK to QN1	t_{PLH}	1.27	1.21 + 0.035*SL	1.21 + 0.033*SL	1.21 + 0.033*SL
	t_{PHL}	1.24	1.14 + 0.047*SL	1.15 + 0.045*SL	1.15 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.078*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
RN to QN1	t_{PLH}	0.55	0.48 + 0.035*SL	0.48 + 0.033*SL	0.48 + 0.033*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

Dn	CK	RN	Qn (n+1)	QNn (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
STD80			
Dn	CK	RN	
0.5	0.5	3.0	22.3
STDM80			
Dn	CK	RN	
0.6	0.6	5.1	22.3

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CK)	t_{PWL}	0.87	1.80
Pulse Width High (CK)	t_{PWH}	0.87	1.15
Pulse Width Low (RN)	t_{PWL}	0.87	0.82
Input Setup Time (D0 to CK)	t_{SU}	0.33	0.36
Input Hold Time (D0 to CK)	t_{HD}	0.63	0.68
Input Setup Time (D1 to CK)	t_{SU}	0.33	0.36
Input Hold Time (D1 to CK)	t_{HD}	0.63	0.68
Input Setup Time (D2 to CK)	t_{SU}	0.33	0.36
Input Hold Time (D2 to CK)	t_{HD}	0.63	0.68
Input Setup Time (D3 to CK)	t_{SU}	0.33	0.36
Input Hold Time (D3 to CK)	t_{HD}	0.63	0.68
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.93	1.04

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.87	0.81 + 0.032*SL	0.82 + 0.026*SL	0.84 + 0.024*SL
	t_{PHL}	1.15	1.07 + 0.041*SL	1.07 + 0.038*SL	1.08 + 0.037*SL
	t_R	0.23	0.14 + 0.048*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q0	t_{PHL}	0.37	0.29 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to Q1	t_{PLH}	0.87	0.81 + 0.032*SL	0.82 + 0.026*SL	0.84 + 0.024*SL
	t_{PHL}	1.15	1.07 + 0.041*SL	1.07 + 0.038*SL	1.08 + 0.037*SL
	t_R	0.23	0.14 + 0.048*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q1	t_{PHL}	0.37	0.29 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.067*SL	0.08 + 0.069*SL
CK to Q2	t_{PLH}	0.87	0.81 + 0.032*SL	0.82 + 0.026*SL	0.84 + 0.024*SL
	t_{PHL}	1.15	1.07 + 0.041*SL	1.07 + 0.038*SL	1.08 + 0.037*SL
	t_R	0.23	0.14 + 0.048*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q2	t_{PHL}	0.37	0.29 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to Q3	t_{PLH}	0.87	0.80 + 0.032*SL	0.81 + 0.026*SL	0.84 + 0.024*SL
	t_{PHL}	1.15	1.06 + 0.041*SL	1.07 + 0.038*SL	1.08 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q3	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to QN0	t_{PLH}	1.19	1.14 + 0.026*SL	1.14 + 0.023*SL	1.14 + 0.024*SL
	t_{PHL}	1.04	0.97 + 0.037*SL	0.97 + 0.037*SL	0.96 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN0	t_{PLH}	0.41	0.36 + 0.025*SL	0.36 + 0.024*SL	0.37 + 0.023*SL
	t_R	0.19	0.10 + 0.046*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
CK to QN1	t_{PLH}	1.19	1.14 + 0.026*SL	1.14 + 0.024*SL	1.14 + 0.024*SL
	t_{PHL}	1.04	0.97 + 0.037*SL	0.97 + 0.037*SL	0.97 + 0.037*SL
	t_R	0.19	0.09 + 0.046*SL	0.09 + 0.050*SL	0.07 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN1	t_{PLH}	0.41	0.36 + 0.024*SL	0.36 + 0.024*SL	0.37 + 0.023*SL
	t_R	0.19	0.10 + 0.046*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
CK to QN2	t_{PLH}	1.19	1.14 + 0.026*SL	1.14 + 0.023*SL	1.14 + 0.024*SL
	t_{PHL}	1.04	0.97 + 0.036*SL	0.97 + 0.037*SL	0.96 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD2X4

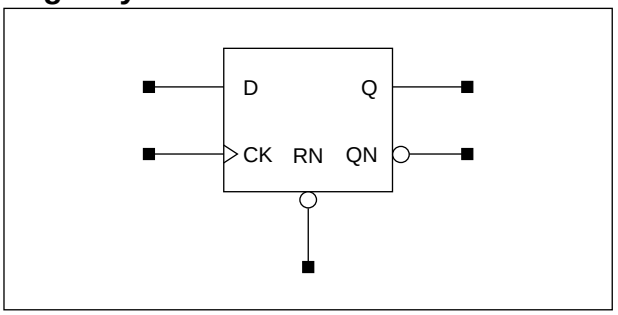
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.19	1.10 + 0.044*SL	1.12 + 0.038*SL	1.14 + 0.035*SL
	t_{PHL}	1.63	1.53 + 0.052*SL	1.55 + 0.046*SL	1.56 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.068*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q0	t_{PHL}	0.48	0.37 + 0.052*SL	0.39 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
CK to Q1	t_{PLH}	1.19	1.10 + 0.044*SL	1.12 + 0.038*SL	1.14 + 0.035*SL
	t_{PHL}	1.63	1.53 + 0.052*SL	1.54 + 0.047*SL	1.56 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q1	t_{PHL}	0.48	0.37 + 0.052*SL	0.39 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
CK to Q2	t_{PLH}	1.19	1.10 + 0.044*SL	1.12 + 0.038*SL	1.14 + 0.035*SL
	t_{PHL}	1.63	1.53 + 0.052*SL	1.55 + 0.046*SL	1.56 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.068*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q2	t_{PHL}	0.48	0.37 + 0.052*SL	0.39 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
CK to Q3	t_{PLH}	1.18	1.09 + 0.044*SL	1.11 + 0.038*SL	1.13 + 0.035*SL
	t_{PHL}	1.63	1.52 + 0.052*SL	1.54 + 0.046*SL	1.55 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.18 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to Q3	t_{PHL}	0.47	0.37 + 0.052*SL	0.38 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.14 + 0.081*SL
CK to QN0	t_{PLH}	1.71	1.64 + 0.035*SL	1.64 + 0.033*SL	1.64 + 0.033*SL
	t_{PHL}	1.42	1.33 + 0.047*SL	1.34 + 0.044*SL	1.34 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.13 + 0.080*SL	0.11 + 0.082*SL
RN to QN0	t_{PLH}	0.56	0.49 + 0.035*SL	0.49 + 0.033*SL	0.49 + 0.033*SL
	t_R	0.26	0.12 + 0.068*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
CK to QN1	t_{PLH}	1.71	1.64 + 0.035*SL	1.64 + 0.034*SL	1.64 + 0.033*SL
	t_{PHL}	1.42	1.33 + 0.047*SL	1.34 + 0.044*SL	1.34 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.29	0.13 + 0.078*SL	0.13 + 0.080*SL	0.11 + 0.082*SL
RN to QN1	t_{PLH}	0.56	0.49 + 0.035*SL	0.49 + 0.033*SL	0.49 + 0.033*SL
	t_R	0.26	0.13 + 0.066*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
CK to QN2	t_{PLH}	1.71	1.64 + 0.035*SL	1.64 + 0.033*SL	1.64 + 0.033*SL
	t_{PHL}	1.42	1.33 + 0.047*SL	1.34 + 0.044*SL	1.34 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.078*SL	0.13 + 0.080*SL	0.11 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

YFD2/YFD2D2

Fast D Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



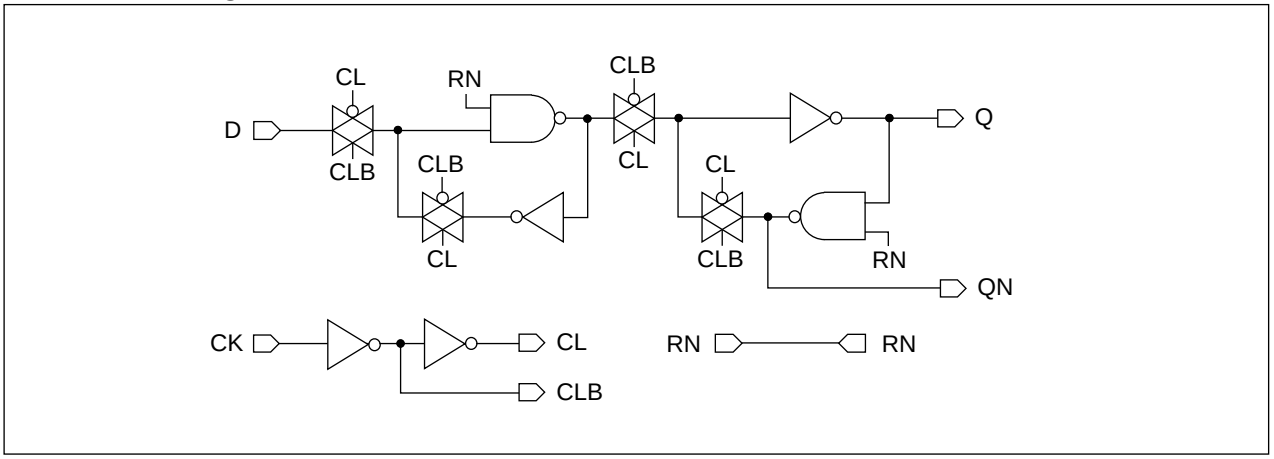
Truth Table

D	CK	RN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
STD80							
YFD2			*YFD2D2*			*YFD2*	*YFD2D2*
D	CK	RN	D	CK	RN		
1.7	0.5	1.2	1.7	0.5	2.2	5.3	6.3
STDM80							
YFD2			*YFD2D2*			*YFD2*	*YFD2D2*
D	CK	RN	D	CK	RN		
0.5	0.6	1.3	1.9	0.6	2.4	5.3	6.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		YFD2	YFD2D2	YFD2	YFD2D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.85	0.85
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.87	0.96
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	1.01	1.15
Input Setup Time (D to CK)	t_{SU}	0.38	0.38	0.46	0.44
Input Hold Time (D to CK)	t_{HD}	0.46	0.46	0.49	0.49
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.38	0.38	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 YFD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.53	0.47 + 0.030*SL	0.47 + 0.026*SL	0.50 + 0.024*SL
	t_{PHL}	0.59	0.50 + 0.044*SL	0.51 + 0.039*SL	0.53 + 0.037*SL
	t_R	0.29	0.20 + 0.047*SL	0.19 + 0.049*SL	0.16 + 0.052*SL
	t_F	0.35	0.22 + 0.064*SL	0.22 + 0.065*SL	0.19 + 0.069*SL
RN to Q	t_{PHL}	0.61	0.53 + 0.042*SL	0.54 + 0.038*SL	0.55 + 0.037*SL
	t_F	0.37	0.25 + 0.058*SL	0.24 + 0.063*SL	0.18 + 0.069*SL
CK to QN	t_{PLH}	0.75	0.58 + 0.083*SL	0.59 + 0.079*SL	0.61 + 0.077*SL
	t_{PHL}	0.71	0.56 + 0.074*SL	0.57 + 0.069*SL	0.60 + 0.067*SL
	t_R	0.28	0.15 + 0.065*SL	0.15 + 0.067*SL	0.14 + 0.067*SL
	t_F	0.29	0.13 + 0.081*SL	0.13 + 0.081*SL	0.13 + 0.082*SL
RN to QN	t_{PLH}	0.17	0.10 + 0.034*SL	0.12 + 0.025*SL	0.13 + 0.024*SL
	t_R	0.30	0.21 + 0.041*SL	0.20 + 0.045*SL	0.21 + 0.044*SL

STD80 YFD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.55	0.51 + 0.019*SL	0.52 + 0.016*SL	0.56 + 0.012*SL
	t_{PHL}	0.63	0.58 + 0.025*SL	0.59 + 0.022*SL	0.62 + 0.018*SL
	t_R	0.27	0.23 + 0.021*SL	0.22 + 0.024*SL	0.21 + 0.026*SL
	t_F	0.34	0.29 + 0.028*SL	0.28 + 0.030*SL	0.25 + 0.033*SL
RN to Q	t_{PHL}	0.65	0.60 + 0.023*SL	0.61 + 0.021*SL	0.63 + 0.018*SL
	t_F	0.34	0.28 + 0.028*SL	0.28 + 0.028*SL	0.23 + 0.033*SL
CK to QN	t_{PLH}	0.75	0.66 + 0.045*SL	0.66 + 0.041*SL	0.69 + 0.038*SL
	t_{PHL}	0.69	0.60 + 0.042*SL	0.61 + 0.038*SL	0.64 + 0.035*SL
	t_R	0.20	0.14 + 0.033*SL	0.14 + 0.032*SL	0.13 + 0.034*SL
	t_F	0.20	0.12 + 0.042*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN	t_{PLH}	0.14	0.10 + 0.019*SL	0.11 + 0.015*SL	0.14 + 0.012*SL
	t_R	0.26	0.21 + 0.023*SL	0.21 + 0.022*SL	0.21 + 0.022*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 YFD2

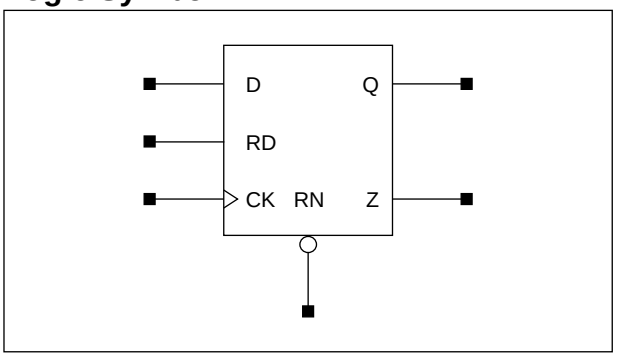
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.76	0.67 + 0.043*SL	0.69 + 0.038*SL	0.71 + 0.035*SL
	t_{PHL}	0.83	0.71 + 0.058*SL	0.74 + 0.051*SL	0.76 + 0.047*SL
	t_R	0.40	0.26 + 0.070*SL	0.26 + 0.069*SL	0.26 + 0.070*SL
	t_F	0.47	0.30 + 0.081*SL	0.31 + 0.080*SL	0.31 + 0.080*SL
RN to Q	t_{PHL}	0.86	0.75 + 0.056*SL	0.77 + 0.049*SL	0.80 + 0.045*SL
	t_F	0.49	0.35 + 0.071*SL	0.34 + 0.074*SL	0.32 + 0.078*SL
CK to QN	t_{PLH}	1.08	0.85 + 0.114*SL	0.87 + 0.107*SL	0.90 + 0.103*SL
	t_{PHL}	1.02	0.82 + 0.101*SL	0.83 + 0.096*SL	0.85 + 0.093*SL
	t_R	0.38	0.20 + 0.088*SL	0.21 + 0.088*SL	0.20 + 0.089*SL
	t_F	0.39	0.18 + 0.105*SL	0.18 + 0.105*SL	0.18 + 0.105*SL
RN to QN	t_{PLH}	0.22	0.15 + 0.038*SL	0.16 + 0.035*SL	0.16 + 0.035*SL
	t_R	0.34	0.21 + 0.065*SL	0.19 + 0.071*SL	0.19 + 0.070*SL

STDM80 YFD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.79	0.74 + 0.025*SL	0.75 + 0.023*SL	0.77 + 0.020*SL
	t_{PHL}	0.92	0.85 + 0.035*SL	0.86 + 0.031*SL	0.89 + 0.027*SL
	t_R	0.35	0.28 + 0.034*SL	0.28 + 0.035*SL	0.28 + 0.034*SL
	t_F	0.46	0.38 + 0.039*SL	0.38 + 0.039*SL	0.38 + 0.038*SL
RN to Q	t_{PHL}	0.92	0.85 + 0.033*SL	0.87 + 0.029*SL	0.89 + 0.026*SL
	t_F	0.46	0.39 + 0.036*SL	0.39 + 0.034*SL	0.39 + 0.035*SL
CK to QN	t_{PLH}	1.10	0.97 + 0.064*SL	0.99 + 0.059*SL	1.01 + 0.055*SL
	t_{PHL}	0.99	0.87 + 0.057*SL	0.88 + 0.053*SL	0.90 + 0.051*SL
	t_R	0.27	0.18 + 0.043*SL	0.18 + 0.043*SL	0.18 + 0.043*SL
	t_F	0.27	0.16 + 0.054*SL	0.16 + 0.053*SL	0.16 + 0.053*SL
RN to QN	t_{PLH}	0.18	0.14 + 0.022*SL	0.15 + 0.018*SL	0.16 + 0.017*SL
	t_R	0.27	0.21 + 0.029*SL	0.20 + 0.033*SL	0.18 + 0.035*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

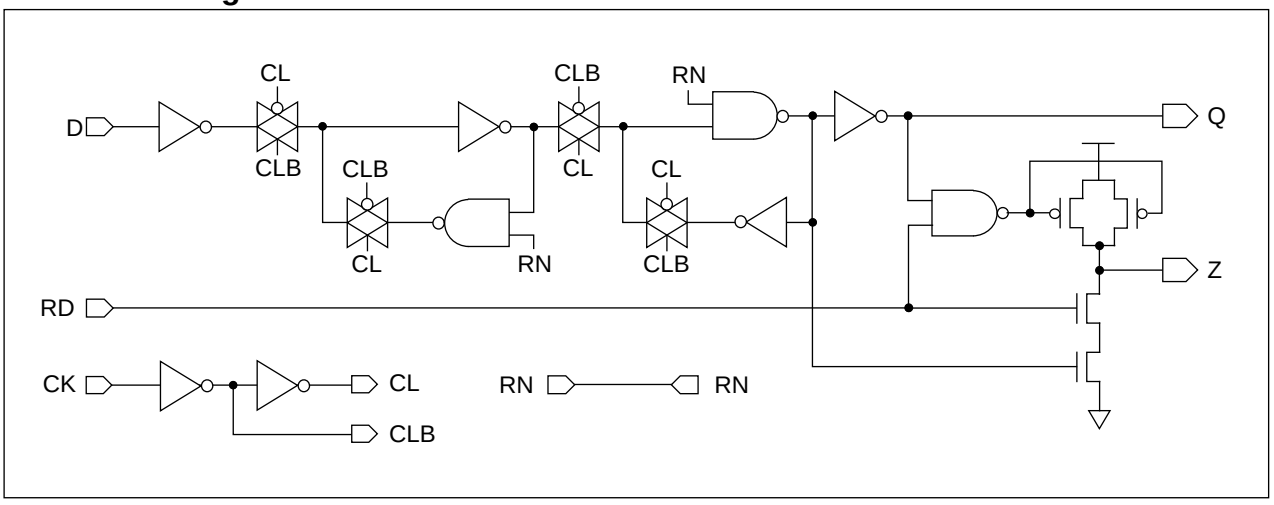
D	RD*	CK	RN	Q (n+1)	Z (n+1)
0	1	↑	1	0	0
1	1	↑	1	1	1
x	1	x	0	0	0
x	0	x	1	x	Hi-Z
x	1	↓	1	Q (n)	Z (n)

* RD is a tri-state enable pin.

Cell Data

Input Load (SL)								Output Load (SL)		Gate Count	
STD80											
FD2T				*FD2TD2*				*FD2T*	*FD2TD2*	*FD2T*	*FD2TD2*
D	RD	CK	RN	D	RD	CK	RN	Z	Z		
0.6	1.1	0.6	1.1	0.6	1.2	0.6	1.1	1.3	2.2	7.3	8.3
STDM80											
FD2T				*FD2TD2*				*FD2T*	*FD2TD2*	*FD2T*	*FD2TD2*
D	RD	CK	RN	D	RD	CK	RN	Z	Z		
0.6	0.9	0.6	1.2	0.6	1.3	0.6	1.2	1.4	2.5	7.3	8.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD2T	FD2TD2	FD2T	FD2TD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.90	0.90
Pulse Width High (CK)	t_{PWH}	0.79	0.79	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.85
Input Setup Time (D to CK)	t_{SU}	0.46	0.46	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66	0.76	0.76

FD2T/FD2TD2

D Flip-Flop with Reset, Tri-State Output, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD2T

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.68	0.62 + 0.032*SL	0.63 + 0.026*SL	0.66 + 0.024*SL
	t_{PHL}	0.73	0.65 + 0.040*SL	0.65 + 0.037*SL	0.66 + 0.037*SL
	t_R	0.28	0.18 + 0.048*SL	0.18 + 0.048*SL	0.15 + 0.052*SL
	t_F	0.29	0.16 + 0.063*SL	0.16 + 0.066*SL	0.12 + 0.069*SL
RN to Q	t_{PHL}	0.41	0.33 + 0.039*SL	0.33 + 0.038*SL	0.34 + 0.037*SL
	t_F	0.29	0.16 + 0.062*SL	0.15 + 0.066*SL	0.13 + 0.069*SL
CK to Z	t_{PLH}	0.89	0.78 + 0.057*SL	0.81 + 0.045*SL	0.88 + 0.038*SL
	t_{PHL}	1.01	0.85 + 0.081*SL	0.86 + 0.075*SL	0.92 + 0.070*SL
	t_R	0.15	0.09 + 0.029*SL	0.10 + 0.027*SL	0.09 + 0.028*SL
	t_F	0.43	0.18 + 0.128*SL	0.22 + 0.111*SL	0.31 + 0.101*SL
RN to Z	t_{PHL}	0.69	0.53 + 0.081*SL	0.55 + 0.075*SL	0.60 + 0.069*SL
	t_F	0.43	0.18 + 0.127*SL	0.22 + 0.110*SL	0.31 + 0.100*SL
RD to Z	t_{PLH}	0.25	0.20 + 0.025*SL	0.22 + 0.015*SL	0.25 + 0.012*SL
	t_{PHL}	0.14	0.04 + 0.050*SL	0.06 + 0.040*SL	0.07 + 0.039*SL
	t_R	0.16	0.11 + 0.023*SL	0.10 + 0.025*SL	0.09 + 0.027*SL
	t_F	0.32	0.18 + 0.068*SL	0.17 + 0.072*SL	0.11 + 0.078*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.31	0.30 + 0.002*SL	0.31 + 0.000*SL	0.31 + 0.000*SL

STD80 FD2TD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.71	0.67 + 0.021*SL	0.68 + 0.016*SL	0.72 + 0.012*SL
	t_{PHL}	0.72	0.68 + 0.023*SL	0.68 + 0.020*SL	0.70 + 0.018*SL
	t_R	0.24	0.19 + 0.023*SL	0.19 + 0.024*SL	0.17 + 0.025*SL
	t_F	0.22	0.16 + 0.029*SL	0.15 + 0.030*SL	0.12 + 0.034*SL
RN to Q	t_{PHL}	0.41	0.36 + 0.023*SL	0.37 + 0.019*SL	0.38 + 0.018*SL
	t_F	0.21	0.15 + 0.030*SL	0.15 + 0.030*SL	0.12 + 0.034*SL
CK to Z	t_{PLH}	0.95	0.88 + 0.037*SL	0.89 + 0.029*SL	0.98 + 0.020*SL
	t_{PHL}	1.03	0.94 + 0.044*SL	0.95 + 0.040*SL	0.99 + 0.036*SL
	t_R	0.16	0.12 + 0.017*SL	0.13 + 0.015*SL	0.14 + 0.014*SL
	t_F	0.33	0.21 + 0.057*SL	0.21 + 0.061*SL	0.30 + 0.051*SL
RN to Z	t_{PHL}	0.71	0.62 + 0.044*SL	0.63 + 0.039*SL	0.67 + 0.035*SL
	t_F	0.33	0.22 + 0.059*SL	0.21 + 0.060*SL	0.30 + 0.051*SL
RD to Z	t_{PLH}	0.28	0.24 + 0.016*SL	0.26 + 0.011*SL	0.30 + 0.006*SL
	t_{PHL}	0.09	0.03 + 0.031*SL	0.04 + 0.023*SL	0.08 + 0.019*SL
	t_R	0.17	0.14 + 0.016*SL	0.14 + 0.013*SL	0.15 + 0.013*SL
	t_F	0.26	0.18 + 0.037*SL	0.19 + 0.034*SL	0.15 + 0.038*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.42	0.42 + 0.001*SL	0.42 + 0.000*SL	0.42 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD2T

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.98	0.89 + 0.045*SL	0.91 + 0.037*SL	0.93 + 0.034*SL
	t_{PHL}	1.03	0.93 + 0.050*SL	0.94 + 0.046*SL	0.95 + 0.044*SL
	t_R	0.38	0.24 + 0.069*SL	0.24 + 0.067*SL	0.23 + 0.069*SL
	t_F	0.37	0.21 + 0.078*SL	0.21 + 0.079*SL	0.19 + 0.081*SL
RN to Q	t_{PHL}	0.53	0.43 + 0.050*SL	0.44 + 0.046*SL	0.45 + 0.045*SL
	t_F	0.36	0.20 + 0.080*SL	0.20 + 0.080*SL	0.19 + 0.081*SL
CK to Z	t_{PLH}	1.30	1.14 + 0.077*SL	1.18 + 0.064*SL	1.22 + 0.058*SL
	t_{PHL}	1.40	1.20 + 0.101*SL	1.22 + 0.094*SL	1.24 + 0.090*SL
	t_R	0.21	0.13 + 0.041*SL	0.14 + 0.036*SL	0.14 + 0.037*SL
	t_F	0.58	0.27 + 0.154*SL	0.31 + 0.139*SL	0.35 + 0.133*SL
RN to Z	t_{PHL}	0.90	0.70 + 0.101*SL	0.72 + 0.094*SL	0.75 + 0.090*SL
	t_F	0.58	0.27 + 0.154*SL	0.32 + 0.138*SL	0.36 + 0.133*SL
RD to Z	t_{PLH}	0.33	0.27 + 0.028*SL	0.29 + 0.021*SL	0.31 + 0.019*SL
	t_{PHL}	0.21	0.11 + 0.054*SL	0.12 + 0.050*SL	0.12 + 0.050*SL
	t_R	0.21	0.14 + 0.036*SL	0.14 + 0.036*SL	0.14 + 0.035*SL
	t_F	0.37	0.19 + 0.091*SL	0.17 + 0.095*SL	0.15 + 0.098*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.39	0.39 + 0.000*SL	0.39 + 0.000*SL	0.39 + 0.000*SL

STDM80 FD2TD2

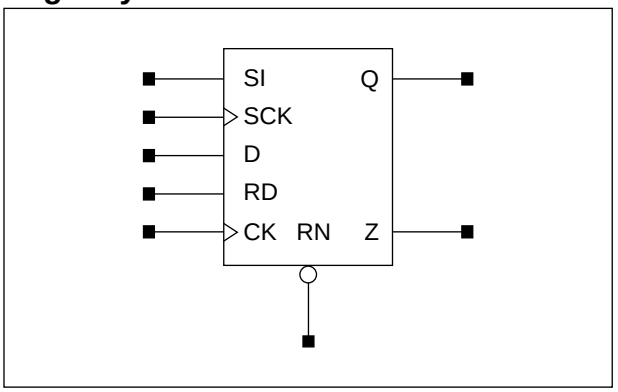
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.01	0.96 + 0.029*SL	0.97 + 0.024*SL	0.99 + 0.020*SL
	t_{PHL}	1.03	0.96 + 0.031*SL	0.98 + 0.026*SL	1.00 + 0.023*SL
	t_R	0.30	0.22 + 0.038*SL	0.23 + 0.035*SL	0.24 + 0.033*SL
	t_F	0.27	0.19 + 0.040*SL	0.20 + 0.038*SL	0.20 + 0.038*SL
RN to Q	t_{PHL}	0.53	0.47 + 0.032*SL	0.48 + 0.026*SL	0.51 + 0.023*SL
	t_F	0.26	0.19 + 0.039*SL	0.19 + 0.038*SL	0.19 + 0.037*SL
CK to Z	t_{PLH}	1.37	1.27 + 0.052*SL	1.30 + 0.042*SL	1.34 + 0.036*SL
	t_{PHL}	1.42	1.31 + 0.058*SL	1.33 + 0.052*SL	1.35 + 0.048*SL
	t_R	0.21	0.16 + 0.024*SL	0.17 + 0.020*SL	0.18 + 0.019*SL
	t_F	0.44	0.28 + 0.081*SL	0.28 + 0.080*SL	0.34 + 0.071*SL
RN to Z	t_{PHL}	0.93	0.81 + 0.058*SL	0.83 + 0.051*SL	0.85 + 0.048*SL
	t_F	0.44	0.27 + 0.083*SL	0.28 + 0.079*SL	0.34 + 0.071*SL
RD to Z	t_{PLH}	0.37	0.33 + 0.019*SL	0.35 + 0.015*SL	0.37 + 0.012*SL
	t_{PHL}	0.16	0.10 + 0.031*SL	0.12 + 0.026*SL	0.12 + 0.025*SL
	t_R	0.24	0.20 + 0.018*SL	0.20 + 0.018*SL	0.20 + 0.018*SL
	t_F	0.28	0.20 + 0.043*SL	0.19 + 0.045*SL	0.18 + 0.047*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.54	0.54 + 0.000*SL	0.54 + 0.000*SL	0.54 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

FD2TCS/FD2TCSD2

D Flip-Flop with Reset, Scan Clock, Tri-State Output, 1X/2X Drive

Logic Symbol



Truth Table

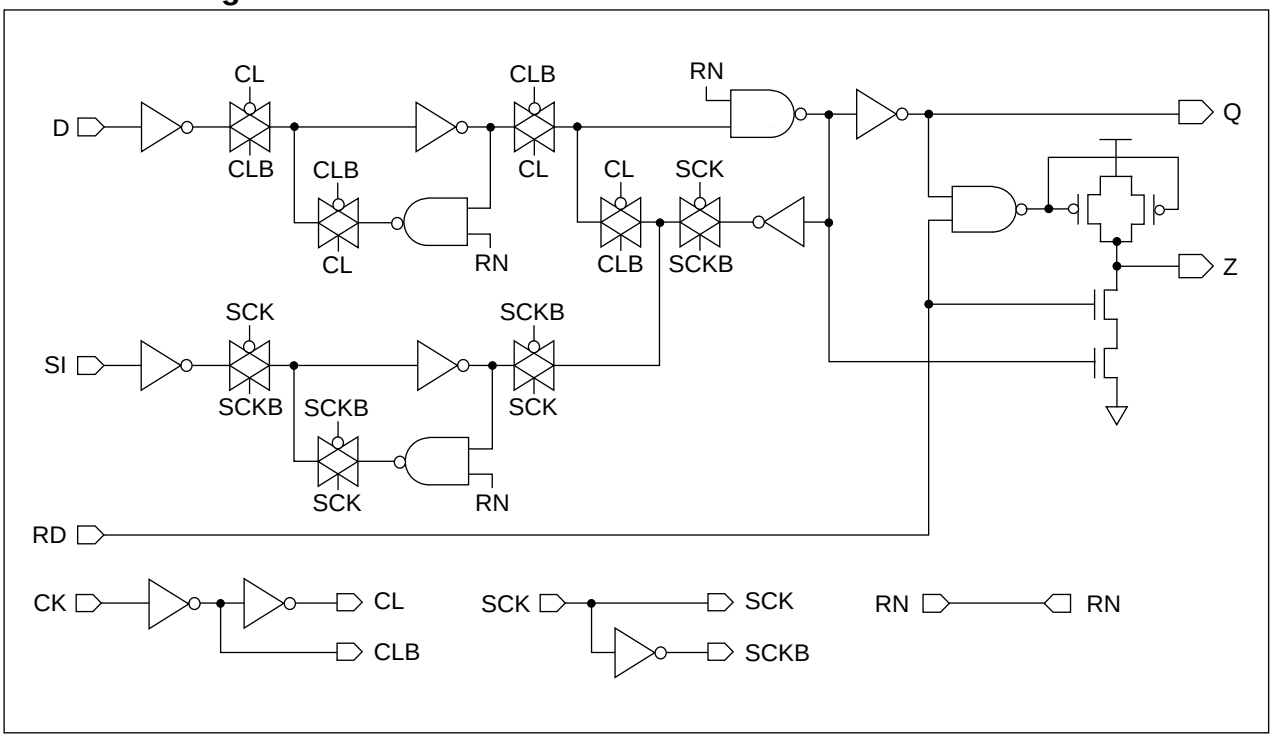
SI	SCK	D	RD	CK	RN	Q (n+1)	Z (n+1)
x	0	0	1	⎍	1	0	0
x	0	1	1	⎍	1	1	1
0	⎍	x	1	0	1	0	0
1	⎍	x	1	0	1	1	1
x	x	x	1	x	0	0	0
x	x	x	0	x	1	x	Hi-Z

* RD is a tri-state enable pin.

Cell Data

Input Load (SL)												Output Load (SL)		Gate Count	
STD80															
FD2TCS						*FD2TCSD2*						*FD2TCS*	*FD2TCS D2*	*FD2TCS*	*FD2TCS D2*
SI	SCK	D	RD	CK	RN	SI	SCK	D	RD	CK	RN	Z	Z		
0.6	2.0	0.6	1.1	0.6	1.7	0.6	2.0	0.6	1.5	0.6	1.9	1.3	2.4	11.3	12.0
STDM80															
FD2TCS						*FD2TCSD2*						*FD2TCS*	*FD2TCS D2*	*FD2TCS*	*FD2TCS D2*
SI	SCK	D	RD	CK	RN	SI	SCK	D	RD	CK	RN	Z	Z		
0.6	1.8	0.6	0.9	0.6	1.8	0.6	1.8	0.6	1.3	0.6	1.9	1.4	2.6	11.3	12.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD2TCS	FD2TCSD2	FD2TCS	FD2TCSD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.90	0.90
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.87
Pulse Width Low (SCK)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width High (SCK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.87
Input Setup Time (D to CK)	t_{SU}	0.46	0.46	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.68	0.68	0.85	0.85
Input Hold Time (SI to SCK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN to CK)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66	0.76	0.76
Recovery Time (RN to SCK)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to SCK)	t_{HD}	0.49	0.49	0.55	0.49

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD2TCS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.63 + 0.031*SL	0.64 + 0.026*SL	0.66 + 0.024*SL
	t_{PHL}	0.72	0.64 + 0.040*SL	0.64 + 0.038*SL	0.65 + 0.037*SL
	t_R	0.28	0.18 + 0.049*SL	0.18 + 0.049*SL	0.15 + 0.052*SL
	t_F	0.28	0.16 + 0.063*SL	0.15 + 0.067*SL	0.13 + 0.069*SL
SCK to Q	t_{PLH}	0.76	0.69 + 0.033*SL	0.71 + 0.026*SL	0.73 + 0.024*SL
	t_{PHL}	0.65	0.57 + 0.040*SL	0.58 + 0.037*SL	0.58 + 0.037*SL
	t_R	0.30	0.21 + 0.046*SL	0.20 + 0.047*SL	0.16 + 0.052*SL
	t_F	0.29	0.17 + 0.063*SL	0.16 + 0.066*SL	0.13 + 0.069*SL
RN to Q	t_{PHL}	0.41	0.33 + 0.040*SL	0.34 + 0.038*SL	0.34 + 0.037*SL
	t_F	0.29	0.16 + 0.065*SL	0.15 + 0.068*SL	0.14 + 0.069*SL
CK to Z	t_{PLH}	0.90	0.79 + 0.056*SL	0.81 + 0.045*SL	0.88 + 0.038*SL
	t_{PHL}	1.01	0.84 + 0.081*SL	0.86 + 0.076*SL	0.91 + 0.070*SL
	t_R	0.15	0.10 + 0.029*SL	0.10 + 0.027*SL	0.09 + 0.028*SL
	t_F	0.44	0.18 + 0.130*SL	0.22 + 0.110*SL	0.32 + 0.101*SL
SCK to Z	t_{PLH}	0.97	0.85 + 0.058*SL	0.88 + 0.045*SL	0.95 + 0.038*SL
	t_{PHL}	0.94	0.78 + 0.081*SL	0.79 + 0.075*SL	0.85 + 0.070*SL
	t_R	0.15	0.10 + 0.029*SL	0.10 + 0.027*SL	0.09 + 0.028*SL
	t_F	0.43	0.17 + 0.128*SL	0.21 + 0.111*SL	0.31 + 0.101*SL
RN to Z	t_{PHL}	0.69	0.53 + 0.081*SL	0.54 + 0.075*SL	0.60 + 0.070*SL
	t_F	0.44	0.18 + 0.129*SL	0.22 + 0.110*SL	0.31 + 0.101*SL
RD to Z	t_{PLH}	0.25	0.20 + 0.026*SL	0.22 + 0.015*SL	0.25 + 0.012*SL
	t_{PHL}	0.14	0.04 + 0.050*SL	0.06 + 0.040*SL	0.07 + 0.039*SL
	t_R	0.16	0.11 + 0.023*SL	0.10 + 0.025*SL	0.09 + 0.027*SL
	t_F	0.32	0.18 + 0.067*SL	0.17 + 0.072*SL	0.11 + 0.078*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.31	0.31 + 0.001*SL	0.31 + 0.000*SL	0.31 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

FD2TCS/FD2TCSD2

D Flip-Flop with Reset, Scan Clock, Tri-State Output, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD2TCSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.74	0.69 + 0.021*SL	0.71 + 0.016*SL	0.74 + 0.012*SL
	t_{PHL}	0.69	0.65 + 0.022*SL	0.65 + 0.020*SL	0.67 + 0.018*SL
	t_R	0.24	0.19 + 0.023*SL	0.19 + 0.024*SL	0.17 + 0.025*SL
	t_F	0.20	0.14 + 0.029*SL	0.14 + 0.031*SL	0.11 + 0.034*SL
SCK to Q	t_{PLH}	0.84	0.80 + 0.021*SL	0.81 + 0.017*SL	0.86 + 0.012*SL
	t_{PHL}	0.63	0.59 + 0.023*SL	0.60 + 0.020*SL	0.61 + 0.018*SL
	t_R	0.26	0.21 + 0.025*SL	0.22 + 0.023*SL	0.19 + 0.025*SL
	t_F	0.21	0.15 + 0.030*SL	0.15 + 0.030*SL	0.12 + 0.034*SL
RN to Q	t_{PHL}	0.42	0.38 + 0.023*SL	0.38 + 0.019*SL	0.40 + 0.018*SL
	t_F	0.21	0.15 + 0.030*SL	0.15 + 0.030*SL	0.12 + 0.034*SL
CK to Z	t_{PLH}	0.96	0.89 + 0.039*SL	0.91 + 0.029*SL	1.00 + 0.020*SL
	t_{PHL}	1.00	0.92 + 0.044*SL	0.92 + 0.040*SL	0.97 + 0.036*SL
	t_R	0.15	0.11 + 0.019*SL	0.12 + 0.015*SL	0.13 + 0.014*SL
	t_F	0.30	0.20 + 0.049*SL	0.18 + 0.061*SL	0.27 + 0.052*SL
SCK to Z	t_{PLH}	1.07	0.99 + 0.039*SL	1.01 + 0.029*SL	1.11 + 0.020*SL
	t_{PHL}	0.95	0.86 + 0.044*SL	0.87 + 0.040*SL	0.91 + 0.036*SL
	t_R	0.15	0.11 + 0.018*SL	0.12 + 0.015*SL	0.13 + 0.014*SL
	t_F	0.30	0.20 + 0.049*SL	0.18 + 0.061*SL	0.27 + 0.052*SL
RN to Z	t_{PHL}	0.72	0.63 + 0.044*SL	0.64 + 0.039*SL	0.68 + 0.035*SL
	t_F	0.31	0.20 + 0.051*SL	0.18 + 0.060*SL	0.27 + 0.052*SL
RD to Z	t_{PLH}	0.27	0.23 + 0.020*SL	0.25 + 0.012*SL	0.30 + 0.006*SL
	t_{PHL}	0.07	0.01 + 0.030*SL	0.03 + 0.023*SL	0.06 + 0.019*SL
	t_R	0.15	0.12 + 0.013*SL	0.12 + 0.014*SL	0.13 + 0.013*SL
	t_F	0.25	0.17 + 0.038*SL	0.18 + 0.034*SL	0.13 + 0.039*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.42	0.42 + 0.001*SL	0.42 + 0.000*SL	0.42 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD2TCS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.99	0.90 + 0.044*SL	0.92 + 0.038*SL	0.94 + 0.034*SL
	t_{PHL}	1.02	0.92 + 0.050*SL	0.93 + 0.046*SL	0.94 + 0.045*SL
	t_R	0.37	0.24 + 0.070*SL	0.24 + 0.068*SL	0.23 + 0.069*SL
	t_F	0.37	0.21 + 0.080*SL	0.21 + 0.079*SL	0.19 + 0.081*SL
SCK to Q	t_{PLH}	1.14	1.05 + 0.046*SL	1.07 + 0.038*SL	1.10 + 0.034*SL
	t_{PHL}	0.92	0.82 + 0.051*SL	0.83 + 0.046*SL	0.84 + 0.044*SL
	t_R	0.40	0.27 + 0.068*SL	0.27 + 0.066*SL	0.26 + 0.068*SL
	t_F	0.37	0.22 + 0.078*SL	0.22 + 0.079*SL	0.20 + 0.081*SL
RN to Q	t_{PHL}	0.53	0.43 + 0.050*SL	0.44 + 0.047*SL	0.45 + 0.045*SL
	t_F	0.36	0.20 + 0.080*SL	0.20 + 0.080*SL	0.19 + 0.081*SL
CK to Z	t_{PLH}	1.31	1.16 + 0.076*SL	1.19 + 0.064*SL	1.23 + 0.059*SL
	t_{PHL}	1.39	1.19 + 0.101*SL	1.21 + 0.094*SL	1.24 + 0.090*SL
	t_R	0.21	0.13 + 0.039*SL	0.13 + 0.037*SL	0.14 + 0.037*SL
	t_F	0.58	0.28 + 0.153*SL	0.32 + 0.138*SL	0.36 + 0.133*SL
SCK to Z	t_{PLH}	1.46	1.30 + 0.078*SL	1.34 + 0.065*SL	1.39 + 0.058*SL
	t_{PHL}	1.29	1.09 + 0.101*SL	1.11 + 0.094*SL	1.14 + 0.090*SL
	t_R	0.21	0.13 + 0.040*SL	0.14 + 0.037*SL	0.14 + 0.037*SL
	t_F	0.57	0.26 + 0.156*SL	0.31 + 0.139*SL	0.35 + 0.134*SL
RN to Z	t_{PHL}	0.90	0.70 + 0.102*SL	0.72 + 0.094*SL	0.75 + 0.090*SL
	t_F	0.59	0.28 + 0.153*SL	0.33 + 0.137*SL	0.37 + 0.132*SL
RD to Z	t_{PLH}	0.34	0.31 + 0.017*SL	0.24 + 0.040*SL	-2.59 + 0.441*SL
	t_{PHL}	0.20	0.13 + 0.034*SL	-0.06 + 0.098*SL	-8.16 + 1.249*SL
	t_R	0.19	0.14 + 0.024*SL	-0.00 + 0.070*SL	-6.17 + 0.946*SL
	t_F	0.34	0.23 + 0.053*SL	-0.17 + 0.186*SL	-16.54 + 2.513*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.39	0.39 + 0.001*SL	0.39 + 0.000*SL	0.39 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

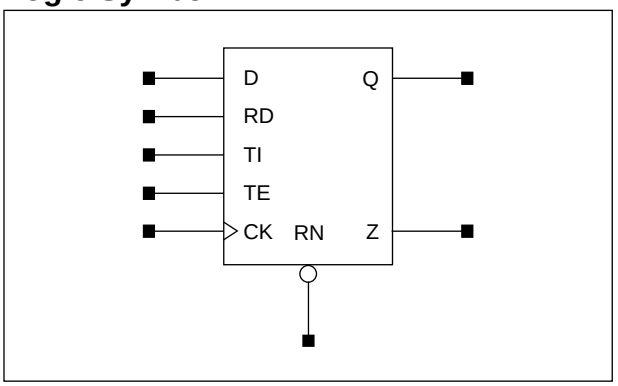
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD2TCSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.05	1.00 + 0.029*SL	1.01 + 0.024*SL	1.03 + 0.021*SL
	t_{PHL}	0.99	0.93 + 0.030*SL	0.94 + 0.026*SL	0.96 + 0.023*SL
	t_R	0.30	0.22 + 0.037*SL	0.23 + 0.035*SL	0.24 + 0.034*SL
	t_F	0.26	0.17 + 0.042*SL	0.18 + 0.039*SL	0.19 + 0.038*SL
SCK to Q	t_{PLH}	1.26	1.20 + 0.031*SL	1.22 + 0.025*SL	1.25 + 0.021*SL
	t_{PHL}	0.90	0.83 + 0.031*SL	0.85 + 0.026*SL	0.87 + 0.023*SL
	t_R	0.33	0.26 + 0.037*SL	0.27 + 0.034*SL	0.28 + 0.032*SL
	t_F	0.27	0.19 + 0.040*SL	0.19 + 0.038*SL	0.19 + 0.038*SL
RN to Q	t_{PHL}	0.54	0.48 + 0.031*SL	0.49 + 0.026*SL	0.51 + 0.023*SL
	t_F	0.26	0.18 + 0.041*SL	0.19 + 0.038*SL	0.19 + 0.037*SL
CK to Z	t_{PLH}	1.41	1.30 + 0.053*SL	1.33 + 0.043*SL	1.38 + 0.036*SL
	t_{PHL}	1.39	1.27 + 0.058*SL	1.29 + 0.052*SL	1.32 + 0.049*SL
	t_R	0.20	0.15 + 0.024*SL	0.17 + 0.020*SL	0.17 + 0.019*SL
	t_F	0.40	0.26 + 0.071*SL	0.23 + 0.082*SL	0.29 + 0.072*SL
SCK to Z	t_{PLH}	1.62	1.51 + 0.054*SL	1.54 + 0.043*SL	1.59 + 0.036*SL
	t_{PHL}	1.30	1.19 + 0.058*SL	1.20 + 0.052*SL	1.23 + 0.048*SL
	t_R	0.20	0.16 + 0.022*SL	0.16 + 0.020*SL	0.17 + 0.019*SL
	t_F	0.40	0.26 + 0.070*SL	0.22 + 0.081*SL	0.28 + 0.072*SL
RN to Z	t_{PHL}	0.94	0.82 + 0.057*SL	0.84 + 0.051*SL	0.87 + 0.048*SL
	t_F	0.40	0.26 + 0.070*SL	0.22 + 0.080*SL	0.28 + 0.072*SL
RD to Z	t_{PLH}	0.39	0.36 + 0.014*SL	0.32 + 0.027*SL	-1.07 + 0.225*SL
	t_{PHL}	0.14	0.10 + 0.019*SL	0.01 + 0.052*SL	-4.03 + 0.625*SL
	t_R	0.18	0.15 + 0.013*SL	0.08 + 0.039*SL	-2.90 + 0.462*SL
	t_F	0.26	0.20 + 0.027*SL	0.01 + 0.090*SL	-8.17 + 1.252*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.54	0.54 + 0.000*SL	0.55 + 0.000*SL	0.55 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

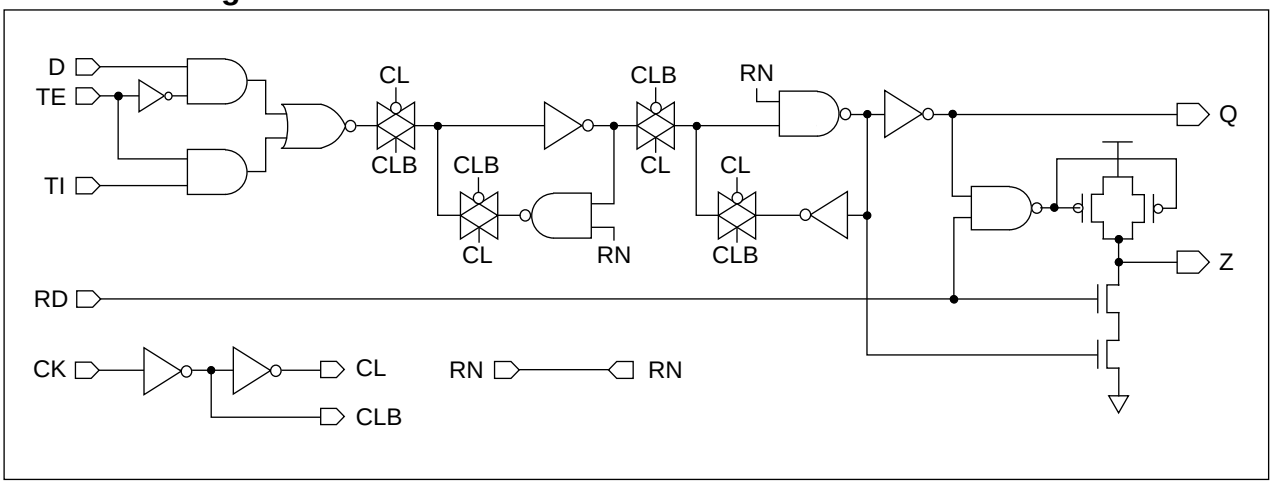
D	RD	TI	TE	CK	RN	Q (n+1)	Z (n+1)
0	1	x	0	↑	1	0	0
1	1	x	0	↑	1	1	1
x	1	0	1	↑	1	0	0
x	1	1	1	↑	1	1	1
x	1	x	x	x	0	0	0
x	0	x	x	x	1	x	Hi-Z
x	1	x	x	↓	1	Q (n)	Z (n)

* RD is a tri-state enable pin.

Cell Data

Input Load (SL)												Output Load (SL)		Gate Count	
STD80															
FD2TS						*FD2TSD2*						*FD2TS*	*FD2TSD2*	*FD2TS*	*FD2TSD2*
D	RD	TI	TE	CK	RN	D	RD	TI	TE	CK	RN	Z	Z		
0.4	1.1	0.6	1.1	0.6	1.4	0.4	1.2	0.6	1.1	0.6	1.4	1.3	2.2	9.0	10.0
STDM80															
FD2TS						*FD2TSD2*						*FD2TS*	*FD2TSD2*	*FD2TS*	*FD2TSD2*
D	RD	TI	TE	CK	RN	D	RD	TI	TE	CK	RN	Z	Z		
0.6	0.9	0.4	1.1	0.6	1.2	0.6	1.3	0.4	1.1	0.6	1.2	1.4	2.5	9.0	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD2TS	FD2TSD2	FD2TS	FD2TSD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.96	0.96
Pulse Width High (CK)	t_{PWH}	0.79	0.79	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.85
Input Setup Time (D to CK)	t_{SU}	0.60	0.60	0.79	0.79
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.63	0.63	0.85	0.85
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.33	0.33	0.90	0.90
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66	0.76	0.76

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD2TS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.63 + 0.033*SL	0.64 + 0.026*SL	0.67 + 0.024*SL
	t_{PHL}	0.75	0.67 + 0.040*SL	0.67 + 0.037*SL	0.67 + 0.037*SL
	t_R	0.28	0.18 + 0.047*SL	0.18 + 0.048*SL	0.15 + 0.052*SL
	t_F	0.29	0.16 + 0.062*SL	0.16 + 0.066*SL	0.12 + 0.069*SL
RN to Q	t_{PHL}	0.41	0.33 + 0.041*SL	0.33 + 0.037*SL	0.34 + 0.037*SL
	t_F	0.29	0.16 + 0.063*SL	0.16 + 0.066*SL	0.13 + 0.069*SL
CK to Z	t_{PLH}	0.91	0.79 + 0.057*SL	0.82 + 0.045*SL	0.89 + 0.038*SL
	t_{PHL}	1.03	0.87 + 0.081*SL	0.88 + 0.075*SL	0.94 + 0.070*SL
	t_R	0.15	0.09 + 0.029*SL	0.10 + 0.027*SL	0.09 + 0.028*SL
	t_F	0.44	0.18 + 0.128*SL	0.22 + 0.110*SL	0.31 + 0.101*SL
RN to Z	t_{PHL}	0.69	0.53 + 0.081*SL	0.55 + 0.075*SL	0.60 + 0.069*SL
	t_F	0.44	0.18 + 0.129*SL	0.22 + 0.109*SL	0.31 + 0.100*SL
RD to Z	t_{PLH}	0.25	0.20 + 0.025*SL	0.22 + 0.015*SL	0.25 + 0.012*SL
	t_{PHL}	0.14	0.04 + 0.050*SL	0.06 + 0.040*SL	0.07 + 0.039*SL
	t_R	0.16	0.11 + 0.022*SL	0.10 + 0.025*SL	0.09 + 0.027*SL
	t_F	0.32	0.18 + 0.069*SL	0.17 + 0.072*SL	0.11 + 0.078*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.31	0.31 + 0.001*SL	0.31 + 0.000*SL	0.31 + 0.000*SL

STD80 FD2TSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.72	0.68 + 0.021*SL	0.69 + 0.016*SL	0.73 + 0.012*SL
	t_{PHL}	0.74	0.70 + 0.023*SL	0.70 + 0.020*SL	0.72 + 0.018*SL
	t_R	0.24	0.19 + 0.026*SL	0.19 + 0.023*SL	0.17 + 0.025*SL
	t_F	0.22	0.16 + 0.030*SL	0.15 + 0.030*SL	0.12 + 0.034*SL
RN to Q	t_{PHL}	0.41	0.36 + 0.023*SL	0.37 + 0.019*SL	0.38 + 0.018*SL
	t_F	0.21	0.15 + 0.030*SL	0.15 + 0.030*SL	0.12 + 0.034*SL
CK to Z	t_{PLH}	0.96	0.89 + 0.037*SL	0.90 + 0.029*SL	0.99 + 0.020*SL
	t_{PHL}	1.05	0.96 + 0.044*SL	0.97 + 0.040*SL	1.01 + 0.036*SL
	t_R	0.16	0.12 + 0.017*SL	0.13 + 0.015*SL	0.14 + 0.014*SL
	t_F	0.33	0.22 + 0.056*SL	0.21 + 0.061*SL	0.30 + 0.051*SL
RN to Z	t_{PHL}	0.71	0.62 + 0.044*SL	0.63 + 0.040*SL	0.67 + 0.035*SL
	t_F	0.34	0.22 + 0.060*SL	0.22 + 0.060*SL	0.30 + 0.051*SL
RD to Z	t_{PLH}	0.28	0.24 + 0.016*SL	0.26 + 0.011*SL	0.30 + 0.006*SL
	t_{PHL}	0.09	0.03 + 0.031*SL	0.04 + 0.023*SL	0.08 + 0.019*SL
	t_R	0.17	0.14 + 0.015*SL	0.14 + 0.013*SL	0.15 + 0.013*SL
	t_F	0.26	0.18 + 0.039*SL	0.19 + 0.034*SL	0.15 + 0.038*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.42	0.42 + 0.001*SL	0.42 + 0.000*SL	0.42 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD2TS

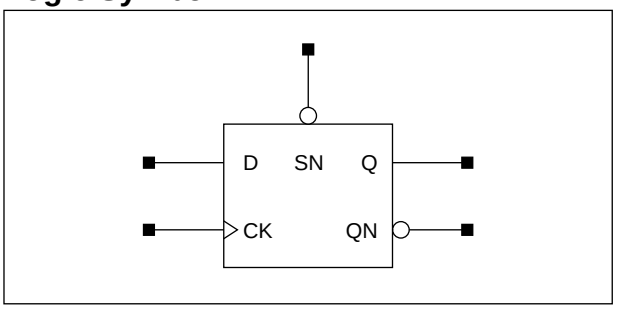
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.99	0.90 + 0.045*SL	0.92 + 0.038*SL	0.95 + 0.034*SL
	t_{PHL}	1.05	0.95 + 0.050*SL	0.96 + 0.046*SL	0.97 + 0.044*SL
	t_R	0.38	0.24 + 0.068*SL	0.24 + 0.067*SL	0.23 + 0.069*SL
	t_F	0.37	0.21 + 0.078*SL	0.21 + 0.079*SL	0.19 + 0.081*SL
RN to Q	t_{PHL}	0.53	0.43 + 0.050*SL	0.44 + 0.046*SL	0.45 + 0.045*SL
	t_F	0.36	0.20 + 0.080*SL	0.20 + 0.080*SL	0.19 + 0.081*SL
CK to Z	t_{PLH}	1.31	1.16 + 0.077*SL	1.19 + 0.064*SL	1.24 + 0.058*SL
	t_{PHL}	1.42	1.22 + 0.101*SL	1.24 + 0.094*SL	1.27 + 0.090*SL
	t_R	0.21	0.13 + 0.040*SL	0.14 + 0.037*SL	0.14 + 0.037*SL
	t_F	0.58	0.27 + 0.155*SL	0.32 + 0.139*SL	0.35 + 0.134*SL
RN to Z	t_{PHL}	0.90	0.70 + 0.101*SL	0.72 + 0.094*SL	0.75 + 0.090*SL
	t_F	0.58	0.28 + 0.153*SL	0.32 + 0.138*SL	0.36 + 0.133*SL
RD to Z	t_{PLH}	0.34	0.28 + 0.027*SL	0.30 + 0.022*SL	0.32 + 0.019*SL
	t_{PHL}	0.20	0.13 + 0.035*SL	-0.06 + 0.098*SL	-8.16 + 1.249*SL
	t_R	0.22	0.14 + 0.037*SL	0.15 + 0.035*SL	0.14 + 0.035*SL
	t_F	0.34	0.23 + 0.053*SL	-0.17 + 0.186*SL	-16.54 + 2.513*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.39	0.39 + 0.001*SL	0.39 + 0.000*SL	0.39 + 0.000*SL

STDM80 FD2TSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.03	0.97 + 0.028*SL	0.98 + 0.024*SL	1.01 + 0.020*SL
	t_{PHL}	1.05	0.99 + 0.031*SL	1.00 + 0.026*SL	1.02 + 0.023*SL
	t_R	0.30	0.22 + 0.038*SL	0.24 + 0.034*SL	0.24 + 0.033*SL
	t_F	0.27	0.19 + 0.040*SL	0.20 + 0.038*SL	0.20 + 0.038*SL
RN to Q	t_{PHL}	0.53	0.47 + 0.031*SL	0.48 + 0.026*SL	0.51 + 0.023*SL
	t_F	0.27	0.19 + 0.039*SL	0.19 + 0.038*SL	0.19 + 0.037*SL
CK to Z	t_{PLH}	1.38	1.28 + 0.051*SL	1.31 + 0.042*SL	1.35 + 0.036*SL
	t_{PHL}	1.45	1.33 + 0.058*SL	1.35 + 0.052*SL	1.37 + 0.049*SL
	t_R	0.21	0.16 + 0.023*SL	0.17 + 0.020*SL	0.18 + 0.019*SL
	t_F	0.44	0.27 + 0.082*SL	0.28 + 0.079*SL	0.34 + 0.071*SL
RN to Z	t_{PHL}	0.93	0.81 + 0.058*SL	0.83 + 0.052*SL	0.85 + 0.048*SL
	t_F	0.44	0.27 + 0.082*SL	0.28 + 0.079*SL	0.34 + 0.071*SL
RD to Z	t_{PLH}	0.37	0.35 + 0.012*SL	0.30 + 0.028*SL	-1.08 + 0.225*SL
	t_{PHL}	0.16	0.10 + 0.033*SL	0.12 + 0.027*SL	0.13 + 0.025*SL
	t_R	0.23	0.21 + 0.010*SL	0.14 + 0.034*SL	-2.85 + 0.458*SL
	t_F	0.30	0.21 + 0.043*SL	0.20 + 0.045*SL	0.19 + 0.046*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.54	0.54 + 0.000*SL	0.54 + 0.000*SL	0.54 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



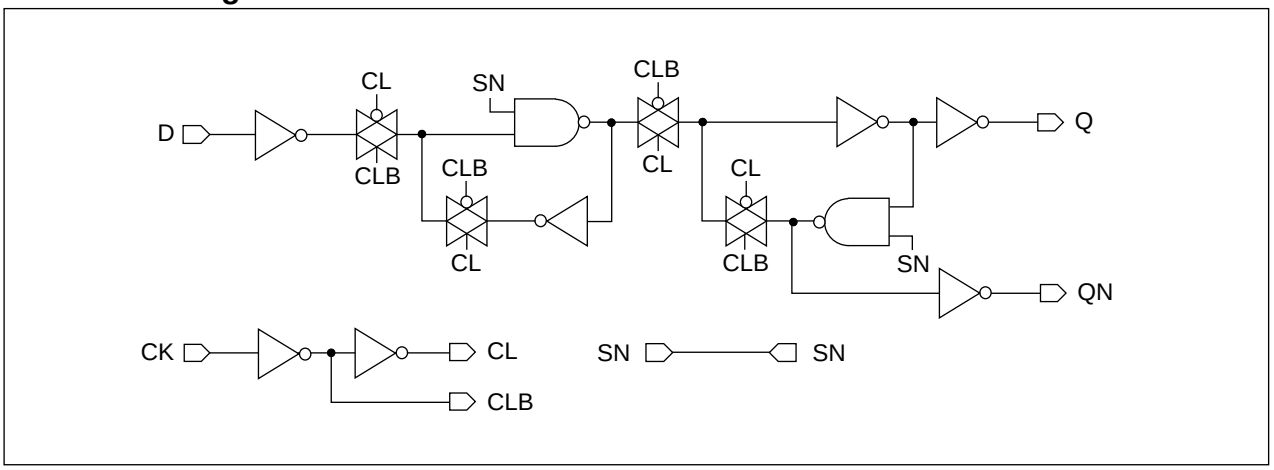
Truth Table

D	CK	SN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
STD80							
FD3			*FD3D2*			*FD3*	*FD3D2*
D	CK	SN	D	CK	SN		
0.5	0.5	0.7	0.5	0.5	0.7	6.7	7.3
STDM80							
FD3			*FD3D2*			*FD3*	*FD3D2*
D	CK	SN	D	CK	SN		
0.6	0.6	1.3	0.6	0.6	1.3	6.7	7.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD3	FD3D2	FD3	FD3D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.93	0.93
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.93	0.93
Input Setup Time (D to CK)	t_{SU}	0.49	0.49	0.60	0.60
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.38	0.38	0.44	0.44

FD3/FD3D2

D Flip-Flop with Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.52 + 0.028*SL	0.53 + 0.024*SL	0.53 + 0.024*SL
	t_{PHL}	0.70	0.62 + 0.041*SL	0.63 + 0.038*SL	0.63 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.065*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
SN to Q	t_{PLH}	0.61	0.55 + 0.029*SL	0.56 + 0.024*SL	0.56 + 0.024*SL
	t_R	0.21	0.12 + 0.043*SL	0.11 + 0.048*SL	0.07 + 0.052*SL
CK to QN	t_{PLH}	0.81	0.75 + 0.030*SL	0.76 + 0.025*SL	0.77 + 0.024*SL
	t_{PHL}	0.78	0.71 + 0.038*SL	0.71 + 0.037*SL	0.71 + 0.037*SL
	t_R	0.21	0.12 + 0.046*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.23	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
SN to QN	t_{PHL}	0.35	0.27 + 0.040*SL	0.27 + 0.038*SL	0.28 + 0.037*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

STD80 FD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.55 + 0.018*SL	0.56 + 0.014*SL	0.57 + 0.012*SL
	t_{PHL}	0.69	0.65 + 0.023*SL	0.65 + 0.020*SL	0.67 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.08 + 0.034*SL
SN to Q	t_{PLH}	0.61	0.58 + 0.018*SL	0.59 + 0.013*SL	0.60 + 0.012*SL
	t_R	0.17	0.12 + 0.021*SL	0.12 + 0.022*SL	0.09 + 0.026*SL
CK to QN	t_{PLH}	0.88	0.84 + 0.018*SL	0.85 + 0.014*SL	0.87 + 0.012*SL
	t_{PHL}	0.83	0.80 + 0.019*SL	0.80 + 0.018*SL	0.80 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to QN	t_{PHL}	0.35	0.30 + 0.023*SL	0.31 + 0.019*SL	0.32 + 0.018*SL
	t_F	0.17	0.11 + 0.029*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.75 + 0.038*SL	0.76 + 0.035*SL	0.76 + 0.034*SL
	t_{PHL}	0.99	0.89 + 0.051*SL	0.90 + 0.046*SL	0.91 + 0.045*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
SN to Q	t_{PLH}	0.87	0.79 + 0.038*SL	0.81 + 0.034*SL	0.81 + 0.033*SL
	t_R	0.29	0.16 + 0.064*SL	0.15 + 0.068*SL	0.13 + 0.071*SL
CK to QN	t_{PLH}	1.17	1.09 + 0.041*SL	1.10 + 0.036*SL	1.12 + 0.034*SL
	t_{PHL}	1.11	1.01 + 0.048*SL	1.02 + 0.045*SL	1.03 + 0.044*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.079*SL	0.14 + 0.080*SL	0.12 + 0.082*SL
SN to QN	t_{PHL}	0.45	0.35 + 0.050*SL	0.36 + 0.046*SL	0.37 + 0.045*SL
	t_F	0.29	0.13 + 0.081*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

STDM80 FD3D2

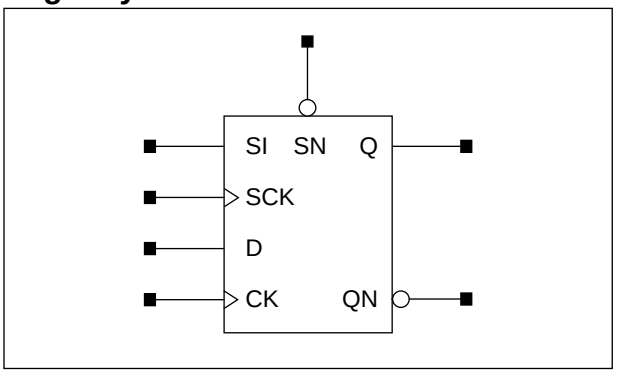
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.78 + 0.024*SL	0.79 + 0.020*SL	0.80 + 0.018*SL
	t_{PHL}	0.98	0.92 + 0.031*SL	0.93 + 0.026*SL	0.96 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.14 + 0.039*SL	0.15 + 0.038*SL
SN to Q	t_{PLH}	0.87	0.83 + 0.024*SL	0.84 + 0.020*SL	0.85 + 0.018*SL
	t_R	0.21	0.15 + 0.032*SL	0.15 + 0.033*SL	0.15 + 0.033*SL
CK to QN	t_{PLH}	1.27	1.22 + 0.024*SL	1.23 + 0.021*SL	1.24 + 0.019*SL
	t_{PHL}	1.18	1.13 + 0.027*SL	1.14 + 0.024*SL	1.15 + 0.022*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.041*SL	0.14 + 0.038*SL	0.14 + 0.038*SL
SN to QN	t_{PHL}	0.45	0.39 + 0.030*SL	0.40 + 0.025*SL	0.42 + 0.023*SL
	t_F	0.21	0.12 + 0.042*SL	0.13 + 0.038*SL	0.13 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

FD3CS/FD3CSD2

D Flip-Flop with Set, Scan Clock, 1X/2X Drive

Logic Symbol



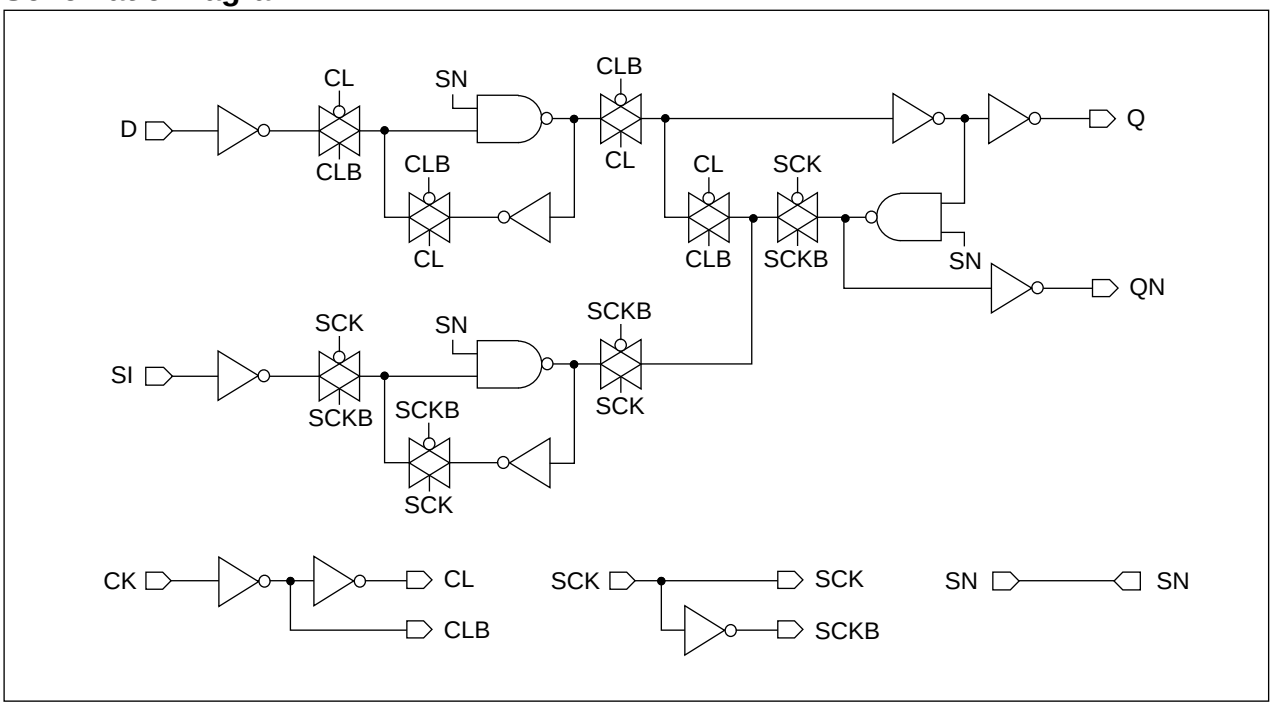
Truth Table

SI	SCK	D	CK	SN	Q (n+1)	QN (n+1)
x	0	0	↑	1	0	1
x	0	1	↑	1	1	0
0	↑	x	0	1	0	1
1	↑	x	0	1	1	0
x	x	x	x	0	1	0

Cell Data

Input Load (SL)										Gate Count	
STD80											
FD3CS					*FD3CSD2*					*FD3CS*	*FD3CSD2*
SI	SCK	D	CK	SN	SI	SCK	D	CK	SN		
0.6	1.8	0.6	0.6	1.7	0.6	1.8	0.6	0.6	1.7	10.7	11.0
STDM80											
FD3CS					*FD3CSD2*					*FD3CS*	*FD3CSD2*
SI	SCK	D	CK	SN	SI	SCK	D	CK	SN		
0.6	2.0	0.6	0.6	2.2	0.6	2.0	0.6	0.6	2.2	10.7	11.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD3CS	FD3CSD2	FD3CS	FD3CSD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.93	0.93
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (SCK)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width High (SCK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.90	0.90	0.93	0.93
Input Setup Time (D to CK)	t_{SU}	0.42	0.42	0.60	0.60
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.74	0.74	0.90	0.90
Input Hold Time (SI to SCK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (SN to CK)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.38	0.38	0.44	0.44
Recovery Time (SN to SCK)	t_{RC}	0.41	0.41	0.52	0.52
Input Hold Time (SN to SCK)	t_{HD}	0.33	0.33	0.33	0.33

FD3CS/FD3CSD2

D Flip-Flop with Set, Scan Clock, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD3CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.52 + 0.028*SL	0.53 + 0.024*SL	0.53 + 0.024*SL
	t_{PHL}	0.69	0.61 + 0.041*SL	0.61 + 0.038*SL	0.62 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.065*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SCK to Q	t_{PLH}	0.64	0.58 + 0.030*SL	0.59 + 0.025*SL	0.60 + 0.024*SL
	t_{PHL}	0.65	0.57 + 0.041*SL	0.58 + 0.038*SL	0.58 + 0.037*SL
	t_R	0.23	0.14 + 0.044*SL	0.13 + 0.047*SL	0.09 + 0.052*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
SN to Q	t_{PLH}	0.61	0.55 + 0.029*SL	0.56 + 0.024*SL	0.56 + 0.023*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
CK to QN	t_{PLH}	0.89	0.82 + 0.036*SL	0.83 + 0.027*SL	0.87 + 0.024*SL
	t_{PHL}	0.85	0.77 + 0.042*SL	0.78 + 0.038*SL	0.79 + 0.037*SL
	t_R	0.27	0.17 + 0.048*SL	0.17 + 0.048*SL	0.14 + 0.051*SL
	t_F	0.26	0.13 + 0.064*SL	0.13 + 0.066*SL	0.10 + 0.069*SL
SCK to QN	t_{PLH}	0.75	0.69 + 0.029*SL	0.70 + 0.025*SL	0.71 + 0.024*SL
	t_{PHL}	0.85	0.78 + 0.038*SL	0.78 + 0.037*SL	0.78 + 0.037*SL
	t_R	0.21	0.12 + 0.047*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.23	0.10 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to QN	t_{PHL}	0.42	0.33 + 0.043*SL	0.34 + 0.039*SL	0.36 + 0.037*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.066*SL	0.10 + 0.069*SL

STD80 FD3CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.55 + 0.018*SL	0.56 + 0.014*SL	0.58 + 0.012*SL
	t_{PHL}	0.69	0.64 + 0.023*SL	0.65 + 0.020*SL	0.66 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
SCK to Q	t_{PLH}	0.66	0.62 + 0.020*SL	0.64 + 0.014*SL	0.66 + 0.012*SL
	t_{PHL}	0.65	0.61 + 0.023*SL	0.62 + 0.020*SL	0.63 + 0.018*SL
	t_R	0.19	0.15 + 0.020*SL	0.15 + 0.022*SL	0.11 + 0.026*SL
	t_F	0.19	0.13 + 0.029*SL	0.13 + 0.030*SL	0.09 + 0.034*SL
SN to Q	t_{PLH}	0.62	0.58 + 0.018*SL	0.59 + 0.014*SL	0.61 + 0.012*SL
	t_R	0.17	0.13 + 0.018*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
CK to QN	t_{PLH}	0.95	0.91 + 0.022*SL	0.92 + 0.016*SL	0.97 + 0.012*SL
	t_{PHL}	0.91	0.86 + 0.023*SL	0.87 + 0.019*SL	0.88 + 0.018*SL
	t_R	0.24	0.19 + 0.025*SL	0.19 + 0.023*SL	0.17 + 0.025*SL
	t_F	0.20	0.14 + 0.032*SL	0.14 + 0.031*SL	0.12 + 0.034*SL
SCK to QN	t_{PLH}	0.83	0.80 + 0.017*SL	0.80 + 0.014*SL	0.83 + 0.012*SL
	t_{PHL}	0.92	0.89 + 0.018*SL	0.89 + 0.018*SL	0.88 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to QN	t_{PHL}	0.41	0.36 + 0.025*SL	0.37 + 0.020*SL	0.39 + 0.018*SL
	t_F	0.19	0.13 + 0.031*SL	0.13 + 0.031*SL	0.11 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD3CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.75 + 0.038*SL	0.76 + 0.034*SL	0.76 + 0.034*SL
	t_{PHL}	0.98	0.87 + 0.051*SL	0.89 + 0.046*SL	0.90 + 0.045*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.070*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.14 + 0.082*SL
SCK to Q	t_{PLH}	0.98	0.89 + 0.041*SL	0.91 + 0.035*SL	0.92 + 0.034*SL
	t_{PHL}	0.92	0.81 + 0.052*SL	0.83 + 0.047*SL	0.84 + 0.045*SL
	t_R	0.32	0.19 + 0.065*SL	0.18 + 0.067*SL	0.16 + 0.070*SL
	t_F	0.32	0.16 + 0.078*SL	0.16 + 0.079*SL	0.15 + 0.081*SL
SN to Q	t_{PLH}	0.87	0.79 + 0.039*SL	0.80 + 0.034*SL	0.81 + 0.033*SL
	t_R	0.28	0.16 + 0.064*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
CK to QN	t_{PLH}	1.28	1.18 + 0.051*SL	1.20 + 0.041*SL	1.24 + 0.036*SL
	t_{PHL}	1.22	1.11 + 0.055*SL	1.12 + 0.049*SL	1.15 + 0.046*SL
	t_R	0.37	0.22 + 0.074*SL	0.24 + 0.068*SL	0.24 + 0.068*SL
	t_F	0.34	0.17 + 0.084*SL	0.18 + 0.081*SL	0.18 + 0.081*SL
SCK to QN	t_{PLH}	1.09	1.01 + 0.040*SL	1.02 + 0.035*SL	1.03 + 0.034*SL
	t_{PHL}	1.27	1.17 + 0.048*SL	1.18 + 0.045*SL	1.19 + 0.044*SL
	t_R	0.30	0.16 + 0.069*SL	0.16 + 0.069*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.079*SL	0.14 + 0.080*SL	0.12 + 0.082*SL
SN to QN	t_{PHL}	0.55	0.43 + 0.056*SL	0.45 + 0.050*SL	0.48 + 0.046*SL
	t_F	0.33	0.16 + 0.086*SL	0.17 + 0.081*SL	0.18 + 0.081*SL

STDM80 FD3CSD2

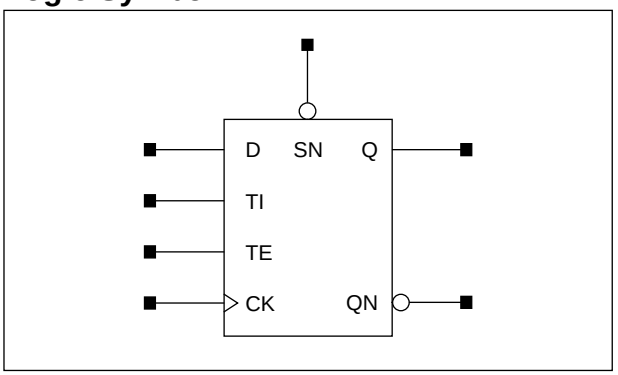
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.83	0.78 + 0.024*SL	0.80 + 0.020*SL	0.81 + 0.018*SL
	t_{PHL}	0.98	0.91 + 0.031*SL	0.93 + 0.026*SL	0.95 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.15 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.23	0.15 + 0.040*SL	0.15 + 0.037*SL	0.14 + 0.039*SL
SCK to Q	t_{PLH}	1.01	0.95 + 0.027*SL	0.97 + 0.021*SL	0.99 + 0.018*SL
	t_{PHL}	0.92	0.86 + 0.031*SL	0.88 + 0.026*SL	0.90 + 0.023*SL
	t_R	0.25	0.18 + 0.033*SL	0.19 + 0.031*SL	0.18 + 0.033*SL
	t_F	0.24	0.16 + 0.040*SL	0.17 + 0.038*SL	0.17 + 0.038*SL
SN to Q	t_{PLH}	0.88	0.83 + 0.024*SL	0.84 + 0.020*SL	0.86 + 0.018*SL
	t_R	0.22	0.15 + 0.032*SL	0.15 + 0.032*SL	0.15 + 0.033*SL
CK to QN	t_{PLH}	1.37	1.31 + 0.031*SL	1.33 + 0.024*SL	1.35 + 0.021*SL
	t_{PHL}	1.28	1.22 + 0.030*SL	1.24 + 0.026*SL	1.25 + 0.024*SL
	t_R	0.30	0.22 + 0.039*SL	0.24 + 0.035*SL	0.25 + 0.034*SL
	t_F	0.25	0.16 + 0.043*SL	0.17 + 0.040*SL	0.18 + 0.039*SL
SCK to QN	t_{PLH}	1.20	1.15 + 0.023*SL	1.16 + 0.021*SL	1.18 + 0.019*SL
	t_{PHL}	1.37	1.32 + 0.026*SL	1.33 + 0.023*SL	1.34 + 0.022*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.14 + 0.038*SL
SN to QN	t_{PHL}	0.53	0.47 + 0.033*SL	0.48 + 0.028*SL	0.50 + 0.025*SL
	t_F	0.24	0.15 + 0.043*SL	0.16 + 0.040*SL	0.17 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

FD3S/FD3SD2

D Flip-Flop with Set, Scan, 1X/2X Drive

Logic Symbol



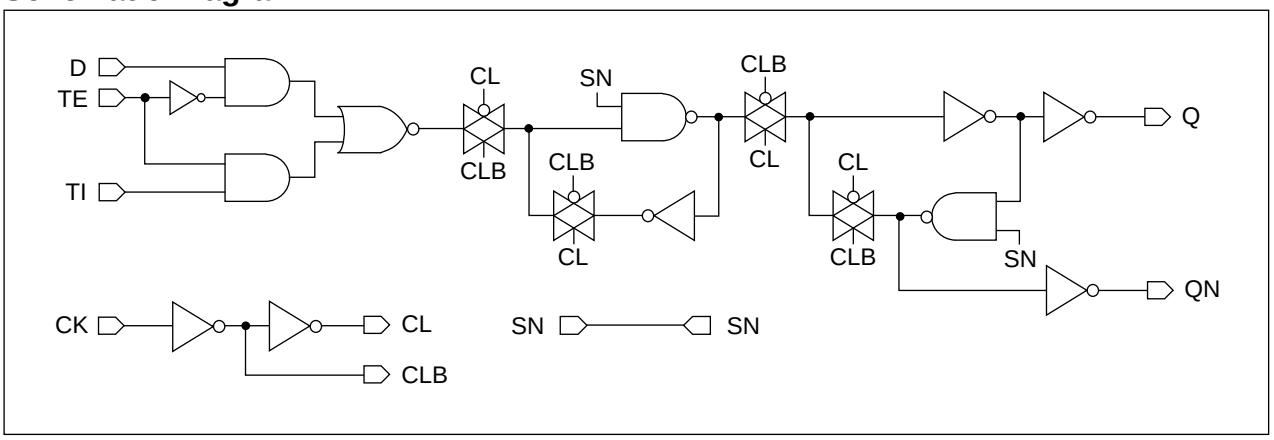
Truth Table

D	TI	TE	CK	SN	Q (n+1)	QN (n+1)
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	1	0
x	x	x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
STD80											
FD3S					*FD3SD2*					*FD3S*	*FD3SD2*
D	TI	TE	CK	SN	D	TI	TE	CK	SN		
0.3	0.5	0.9	0.5	0.7	0.3	0.5	0.9	0.5	0.7	8.3	9.0
STDM80											
FD3S					*FD3SD2*					*FD3S*	*FD3SD2*
D	TI	TE	CK	SN	D	TI	TE	CK	SN		
0.6	0.6	1.1	0.6	1.3	0.6	0.6	1.1	0.6	1.3	8.3	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD3S	FD3SD2	FD3S	FD3SD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.98	1.01
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.93	0.93
Input Setup Time (D to CK)	t_{SU}	0.63	0.63	0.85	0.85
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.66	0.66	0.90	0.90
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.71	0.71	0.98	0.98
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.38	0.38	0.49	0.49

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD3S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.59	0.53 + 0.028*SL	0.54 + 0.024*SL	0.55 + 0.024*SL
	t_{PHL}	0.72	0.64 + 0.041*SL	0.65 + 0.038*SL	0.65 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to Q	t_{PLH}	0.61	0.55 + 0.029*SL	0.56 + 0.024*SL	0.56 + 0.024*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.048*SL	0.07 + 0.052*SL
CK to QN	t_{PLH}	0.83	0.77 + 0.029*SL	0.78 + 0.025*SL	0.79 + 0.024*SL
	t_{PHL}	0.79	0.72 + 0.039*SL	0.72 + 0.037*SL	0.72 + 0.037*SL
	t_R	0.21	0.12 + 0.046*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
SN to QN	t_{PHL}	0.35	0.27 + 0.040*SL	0.27 + 0.038*SL	0.28 + 0.037*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

STD80 FD3SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.59	0.56 + 0.018*SL	0.57 + 0.014*SL	0.58 + 0.012*SL
	t_{PHL}	0.71	0.67 + 0.023*SL	0.67 + 0.020*SL	0.69 + 0.018*SL
	t_R	0.16	0.12 + 0.022*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
SN to Q	t_{PLH}	0.61	0.58 + 0.018*SL	0.59 + 0.013*SL	0.60 + 0.012*SL
	t_R	0.17	0.12 + 0.021*SL	0.12 + 0.022*SL	0.09 + 0.026*SL
CK to QN	t_{PLH}	0.90	0.86 + 0.018*SL	0.87 + 0.014*SL	0.89 + 0.012*SL
	t_{PHL}	0.85	0.81 + 0.020*SL	0.81 + 0.018*SL	0.81 + 0.018*SL
	t_R	0.19	0.14 + 0.025*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.033*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to QN	t_{PHL}	0.35	0.30 + 0.023*SL	0.31 + 0.019*SL	0.32 + 0.018*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

FD3S/FD3SD2

D Flip-Flop with Set, Scan, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD3S

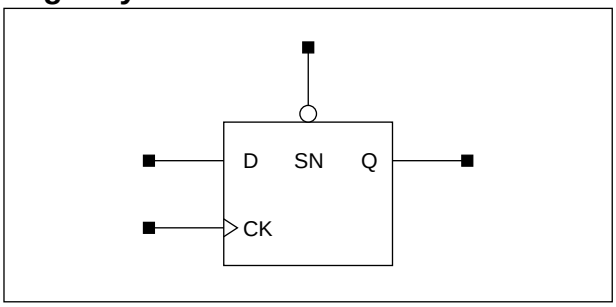
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.84	0.76 + 0.038*SL	0.77 + 0.034*SL	0.78 + 0.034*SL
	t_{PHL}	1.02	0.91 + 0.052*SL	0.93 + 0.046*SL	0.94 + 0.045*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
SN to Q	t_{PLH}	0.87	0.79 + 0.039*SL	0.81 + 0.034*SL	0.81 + 0.033*SL
	t_R	0.29	0.16 + 0.065*SL	0.15 + 0.068*SL	0.13 + 0.071*SL
CK to QN	t_{PLH}	1.19	1.11 + 0.041*SL	1.13 + 0.036*SL	1.14 + 0.034*SL
	t_{PHL}	1.12	1.03 + 0.048*SL	1.04 + 0.045*SL	1.04 + 0.044*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.079*SL	0.14 + 0.080*SL	0.12 + 0.082*SL
SN to QN	t_{PHL}	0.45	0.35 + 0.050*SL	0.36 + 0.046*SL	0.37 + 0.045*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

STDM80 FD3SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.84	0.79 + 0.024*SL	0.80 + 0.020*SL	0.82 + 0.018*SL
	t_{PHL}	1.01	0.94 + 0.031*SL	0.96 + 0.026*SL	0.98 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.14 + 0.039*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
SN to Q	t_{PLH}	0.87	0.83 + 0.024*SL	0.84 + 0.020*SL	0.85 + 0.018*SL
	t_R	0.22	0.15 + 0.033*SL	0.15 + 0.032*SL	0.14 + 0.033*SL
CK to QN	t_{PLH}	1.29	1.24 + 0.024*SL	1.25 + 0.021*SL	1.27 + 0.019*SL
	t_{PHL}	1.20	1.14 + 0.027*SL	1.15 + 0.024*SL	1.16 + 0.022*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.22	0.14 + 0.041*SL	0.14 + 0.038*SL	0.14 + 0.038*SL
SN to QN	t_{PHL}	0.45	0.39 + 0.030*SL	0.40 + 0.025*SL	0.42 + 0.023*SL
	t_F	0.21	0.12 + 0.042*SL	0.13 + 0.038*SL	0.13 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



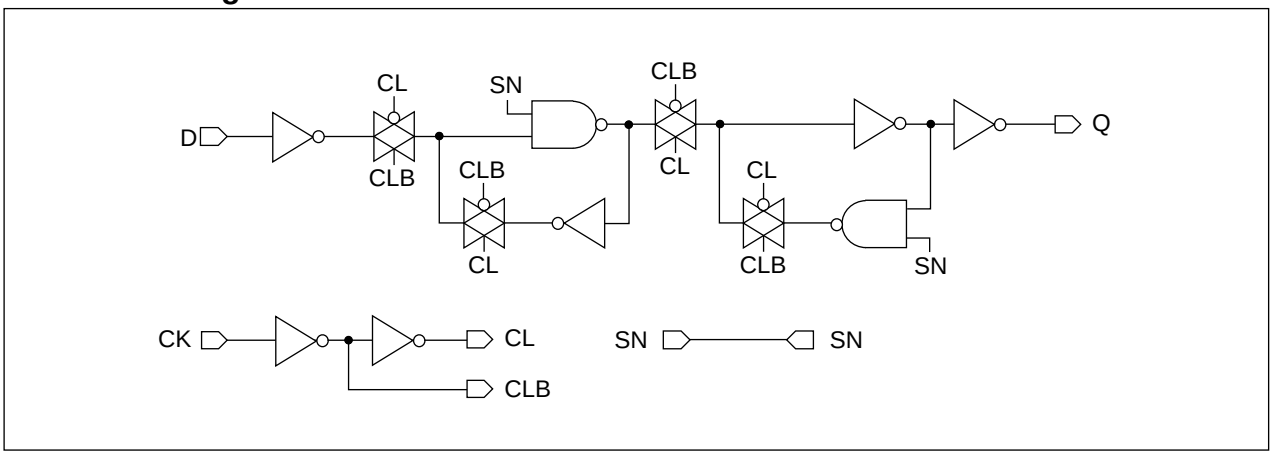
Truth Table

D	CK	SN	Q (n+1)
0	↑	1	0
1	↑	1	1
x	x	0	1
x	↓	x	Q (n)

Cell Data

Input Load (SL)						Gate Count	
STD80							
FD3Q			*FD3Q*			*FD3Q*	*FD3QD2*
D	CK	SN	D	CK	SN		
0.6	0.6	1.0	0.6	0.6	1.0	6.3	6.7
STDM80							
FD3Q			*FD3Q*			*FD3Q*	*FD3QD2*
D	CK	SN	D	CK	SN		
0.6	0.6	1.2	0.6	0.6	1.2	6.3	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD3Q	FD3QD2	FD3Q	FD3QD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.93	0.93
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.93	0.93
Input Setup Time (D to CK)	t_{SU}	0.49	0.49	0.60	0.60
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.38	0.38	0.44	0.44

FD3Q/FD3QD2

D Flip-Flop with Set, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD3Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.57	0.52 + 0.027*SL	0.52 + 0.024*SL	0.53 + 0.024*SL
	t_{PHL}	0.69	0.60 + 0.041*SL	0.61 + 0.038*SL	0.62 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
SN to Q	t_{PLH}	0.60	0.54 + 0.028*SL	0.55 + 0.024*SL	0.55 + 0.024*SL
	t_R	0.21	0.11 + 0.047*SL	0.11 + 0.048*SL	0.07 + 0.052*SL

STD80 FD3QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.54 + 0.018*SL	0.55 + 0.014*SL	0.57 + 0.012*SL
	t_{PHL}	0.68	0.63 + 0.023*SL	0.64 + 0.020*SL	0.65 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.17	0.11 + 0.029*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to Q	t_{PLH}	0.60	0.57 + 0.018*SL	0.58 + 0.013*SL	0.59 + 0.012*SL
	t_R	0.16	0.12 + 0.022*SL	0.12 + 0.022*SL	0.09 + 0.026*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD3Q

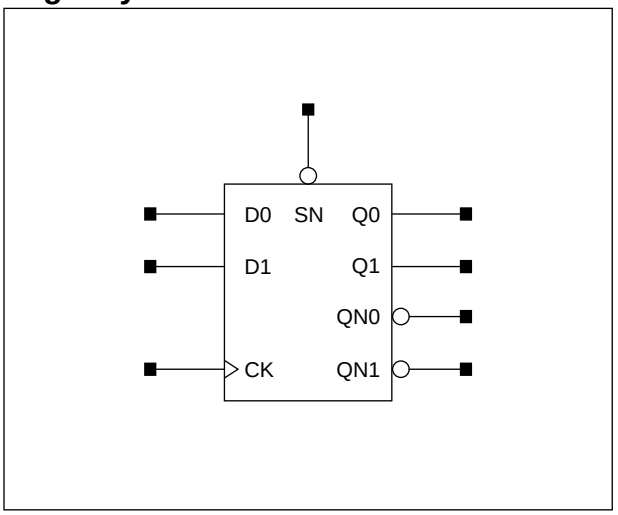
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.74 + 0.038*SL	0.75 + 0.034*SL	0.76 + 0.034*SL
	t_{PHL}	0.97	0.87 + 0.052*SL	0.88 + 0.046*SL	0.89 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.30	0.15 + 0.078*SL	0.14 + 0.079*SL	0.13 + 0.082*SL
SN to Q	t_{PLH}	0.86	0.78 + 0.038*SL	0.79 + 0.034*SL	0.80 + 0.033*SL
	t_R	0.28	0.15 + 0.064*SL	0.14 + 0.068*SL	0.12 + 0.071*SL

STDM80 FD3QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.78 + 0.023*SL	0.79 + 0.020*SL	0.80 + 0.018*SL
	t_{PHL}	0.96	0.90 + 0.031*SL	0.92 + 0.026*SL	0.94 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.033*SL
	t_F	0.22	0.14 + 0.039*SL	0.14 + 0.038*SL	0.14 + 0.038*SL
SN to Q	t_{PLH}	0.86	0.82 + 0.024*SL	0.83 + 0.019*SL	0.85 + 0.017*SL
	t_R	0.21	0.15 + 0.031*SL	0.15 + 0.033*SL	0.14 + 0.033*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

Dn	CK	SN	Qn (n+1)	QNn (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
STD80			
Dn	CK	SN	
0.5	0.5	1.5	12.3
STDM80			
Dn	CK	SN	
0.6	0.6	2.9	12.3

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CK)	t_{PWL}	0.90	0.98
Pulse Width High (CK)	t_{PWH}	0.87	0.79
Pulse Width Low (SN)	t_{PWL}	0.87	0.85
Input Setup Time (D0 to CK)	t_{SU}	0.38	0.46
Input Hold Time (D0 to CK)	t_{HD}	0.41	0.33
Input Setup Time (D1 to CK)	t_{SU}	0.38	0.45
Input Hold Time (D1 to CK)	t_{HD}	0.41	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.55	0.60

FD3X2

2-Bit D Flip-Flop with Set

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD3X2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.66	0.61 + 0.028*SL	0.62 + 0.024*SL	0.62 + 0.024*SL
	t_{PHL}	0.88	0.80 + 0.040*SL	0.80 + 0.038*SL	0.81 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
SN to Q0	t_{PLH}	0.61	0.55 + 0.028*SL	0.56 + 0.024*SL	0.56 + 0.024*SL
	t_R	0.21	0.12 + 0.042*SL	0.11 + 0.048*SL	0.07 + 0.052*SL
CK to Q1	t_{PLH}	0.66	0.61 + 0.028*SL	0.61 + 0.024*SL	0.62 + 0.024*SL
	t_{PHL}	0.87	0.79 + 0.041*SL	0.80 + 0.038*SL	0.81 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
SN to Q1	t_{PLH}	0.61	0.55 + 0.029*SL	0.56 + 0.024*SL	0.56 + 0.024*SL
	t_R	0.21	0.12 + 0.043*SL	0.11 + 0.048*SL	0.07 + 0.052*SL
CK to QN0	t_{PLH}	0.99	0.93 + 0.030*SL	0.94 + 0.025*SL	0.95 + 0.024*SL
	t_{PHL}	0.87	0.79 + 0.039*SL	0.80 + 0.037*SL	0.80 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.23	0.10 + 0.064*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
SN to QN0	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.038*SL	0.28 + 0.037*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
CK to QN1	t_{PLH}	0.98	0.92 + 0.029*SL	0.93 + 0.025*SL	0.94 + 0.024*SL
	t_{PHL}	0.87	0.79 + 0.038*SL	0.79 + 0.037*SL	0.79 + 0.037*SL
	t_R	0.21	0.12 + 0.046*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.23	0.10 + 0.065*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
SN to QN1	t_{PHL}	0.35	0.27 + 0.040*SL	0.27 + 0.038*SL	0.28 + 0.037*SL
	t_F	0.23	0.10 + 0.062*SL	0.09 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD3X2

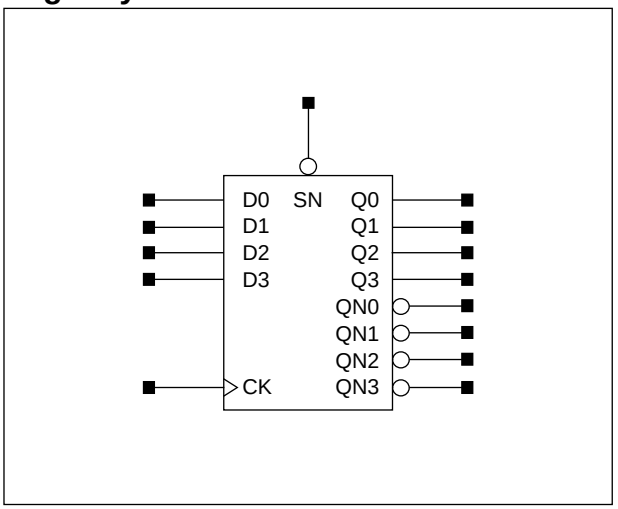
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.93	0.85 + 0.038*SL	0.87 + 0.034*SL	0.87 + 0.034*SL
	t_{PHL}	1.23	1.13 + 0.051*SL	1.15 + 0.046*SL	1.16 + 0.045*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
SN to Q0	t_{PLH}	0.87	0.79 + 0.039*SL	0.81 + 0.034*SL	0.81 + 0.033*SL
	t_R	0.29	0.16 + 0.064*SL	0.14 + 0.068*SL	0.13 + 0.071*SL
CK to Q1	t_{PLH}	0.93	0.85 + 0.038*SL	0.86 + 0.035*SL	0.87 + 0.034*SL
	t_{PHL}	1.23	1.13 + 0.051*SL	1.14 + 0.046*SL	1.15 + 0.045*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.078*SL	0.15 + 0.080*SL	0.13 + 0.082*SL
SN to Q1	t_{PLH}	0.87	0.79 + 0.039*SL	0.81 + 0.034*SL	0.81 + 0.033*SL
	t_R	0.29	0.16 + 0.064*SL	0.14 + 0.068*SL	0.13 + 0.071*SL
CK to QN0	t_{PLH}	1.42	1.34 + 0.040*SL	1.35 + 0.036*SL	1.36 + 0.034*SL
	t_{PHL}	1.22	1.12 + 0.048*SL	1.13 + 0.045*SL	1.14 + 0.044*SL
	t_R	0.30	0.17 + 0.066*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.081*SL
SN to QN0	t_{PHL}	0.46	0.36 + 0.050*SL	0.37 + 0.046*SL	0.38 + 0.045*SL
	t_F	0.29	0.13 + 0.081*SL	0.13 + 0.081*SL	0.12 + 0.082*SL
CK to QN1	t_{PLH}	1.41	1.33 + 0.041*SL	1.34 + 0.036*SL	1.36 + 0.034*SL
	t_{PHL}	1.21	1.12 + 0.048*SL	1.13 + 0.045*SL	1.13 + 0.044*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.069*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.079*SL	0.13 + 0.080*SL	0.12 + 0.082*SL
SN to QN1	t_{PHL}	0.45	0.35 + 0.050*SL	0.36 + 0.046*SL	0.37 + 0.045*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

FD3X4

4-Bit D Flip-Flop with Set

Logic Symbol



Truth Table

Dn	CK	SN	Qn (n+1)	QNn (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
STD80			
Dn	CK	SN	
0.5	0.5	3.0	23.7
STDM80			
Dn	CK	SN	
0.6	0.6	5.9	23.7

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CK)	t_{PWL}	0.90	1.80
Pulse Width High (CK)	t_{PWH}	0.87	1.20
Pulse Width Low (SN)	t_{PWL}	0.90	0.93
Input Setup Time (D0 to CK)	t_{SU}	0.33	0.41
Input Hold Time (D0 to CK)	t_{HD}	0.60	0.66
Input Setup Time (D1 to CK)	t_{SU}	0.33	0.41
Input Hold Time (D1 to CK)	t_{HD}	0.60	0.66
Input Setup Time (D2 to CK)	t_{SU}	0.33	0.41
Input Hold Time (D2 to CK)	t_{HD}	0.60	0.66
Input Setup Time (D3 to CK)	t_{SU}	0.33	0.41
Input Hold Time (D3 to CK)	t_{HD}	0.60	0.66
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.76	0.98

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD3X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.82	0.76 + 0.029*SL	0.77 + 0.024*SL	0.77 + 0.024*SL
	t_{PHL}	1.19	1.11 + 0.040*SL	1.11 + 0.038*SL	1.12 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
SN to Q0	t_{PLH}	0.61	0.55 + 0.028*SL	0.56 + 0.024*SL	0.56 + 0.024*SL
	t_R	0.21	0.12 + 0.043*SL	0.11 + 0.048*SL	0.07 + 0.052*SL
CK to Q1	t_{PLH}	0.82	0.76 + 0.029*SL	0.77 + 0.024*SL	0.77 + 0.024*SL
	t_{PHL}	1.19	1.11 + 0.040*SL	1.11 + 0.038*SL	1.12 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
SN to Q1	t_{PLH}	0.61	0.55 + 0.028*SL	0.56 + 0.024*SL	0.56 + 0.024*SL
	t_R	0.21	0.12 + 0.043*SL	0.11 + 0.048*SL	0.07 + 0.052*SL
CK to Q2	t_{PLH}	0.82	0.76 + 0.029*SL	0.77 + 0.024*SL	0.77 + 0.024*SL
	t_{PHL}	1.19	1.11 + 0.040*SL	1.11 + 0.038*SL	1.12 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
SN to Q2	t_{PLH}	0.61	0.55 + 0.028*SL	0.56 + 0.024*SL	0.56 + 0.024*SL
	t_R	0.21	0.12 + 0.043*SL	0.11 + 0.048*SL	0.07 + 0.052*SL
CK to Q3	t_{PLH}	0.81	0.76 + 0.028*SL	0.77 + 0.024*SL	0.77 + 0.024*SL
	t_{PHL}	1.19	1.10 + 0.041*SL	1.11 + 0.038*SL	1.12 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
SN to Q3	t_{PLH}	0.60	0.55 + 0.028*SL	0.56 + 0.024*SL	0.56 + 0.024*SL
	t_R	0.21	0.12 + 0.043*SL	0.11 + 0.048*SL	0.07 + 0.052*SL
CK to QN0	t_{PLH}	1.29	1.24 + 0.029*SL	1.24 + 0.025*SL	1.26 + 0.024*SL
	t_{PHL}	1.02	0.94 + 0.038*SL	0.94 + 0.037*SL	0.94 + 0.037*SL
	t_R	0.22	0.12 + 0.046*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.23	0.10 + 0.063*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
SN to QN0	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.038*SL	0.28 + 0.037*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
CK to QN1	t_{PLH}	1.29	1.23 + 0.030*SL	1.25 + 0.025*SL	1.26 + 0.024*SL
	t_{PHL}	1.02	0.94 + 0.038*SL	0.94 + 0.037*SL	0.94 + 0.037*SL
	t_R	0.22	0.12 + 0.046*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.23	0.10 + 0.063*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
SN to QN1	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.038*SL	0.28 + 0.037*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
CK to QN2	t_{PLH}	1.29	1.23 + 0.030*SL	1.25 + 0.025*SL	1.26 + 0.024*SL
	t_{PHL}	1.02	0.94 + 0.038*SL	0.94 + 0.037*SL	0.94 + 0.037*SL
	t_R	0.22	0.12 + 0.046*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.23	0.10 + 0.063*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

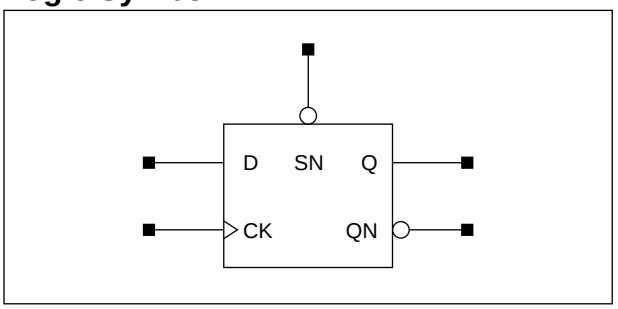
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD3X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.11	1.04 + 0.038*SL	1.05 + 0.035*SL	1.05 + 0.034*SL
	t_{PHL}	1.67	1.57 + 0.051*SL	1.58 + 0.046*SL	1.60 + 0.045*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.14 + 0.081*SL
SN to Q0	t_{PLH}	0.87	0.79 + 0.039*SL	0.80 + 0.034*SL	0.81 + 0.033*SL
	t_R	0.29	0.16 + 0.064*SL	0.15 + 0.068*SL	0.13 + 0.071*SL
CK to Q1	t_{PLH}	1.11	1.04 + 0.038*SL	1.05 + 0.035*SL	1.05 + 0.034*SL
	t_{PHL}	1.67	1.57 + 0.051*SL	1.58 + 0.046*SL	1.60 + 0.045*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.14 + 0.081*SL
SN to Q1	t_{PLH}	0.87	0.79 + 0.039*SL	0.80 + 0.034*SL	0.81 + 0.033*SL
	t_R	0.29	0.16 + 0.064*SL	0.15 + 0.068*SL	0.13 + 0.071*SL
CK to Q2	t_{PLH}	1.11	1.04 + 0.038*SL	1.05 + 0.035*SL	1.05 + 0.034*SL
	t_{PHL}	1.67	1.57 + 0.051*SL	1.58 + 0.046*SL	1.60 + 0.045*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.14 + 0.081*SL
SN to Q2	t_{PLH}	0.87	0.79 + 0.039*SL	0.80 + 0.034*SL	0.81 + 0.033*SL
	t_R	0.29	0.16 + 0.064*SL	0.15 + 0.068*SL	0.13 + 0.071*SL
CK to Q3	t_{PLH}	1.11	1.03 + 0.038*SL	1.04 + 0.034*SL	1.05 + 0.034*SL
	t_{PHL}	1.67	1.57 + 0.051*SL	1.58 + 0.046*SL	1.59 + 0.045*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.14 + 0.081*SL
SN to Q3	t_{PLH}	0.86	0.79 + 0.038*SL	0.80 + 0.034*SL	0.80 + 0.033*SL
	t_R	0.29	0.16 + 0.065*SL	0.15 + 0.068*SL	0.13 + 0.071*SL
CK to QN0	t_{PLH}	1.85	1.77 + 0.041*SL	1.79 + 0.036*SL	1.80 + 0.034*SL
	t_{PHL}	1.40	1.30 + 0.048*SL	1.31 + 0.045*SL	1.32 + 0.044*SL
	t_R	0.30	0.16 + 0.069*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.079*SL	0.14 + 0.080*SL	0.12 + 0.082*SL
SN to QN0	t_{PHL}	0.46	0.36 + 0.051*SL	0.37 + 0.046*SL	0.38 + 0.045*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.13 + 0.082*SL
CK to QN1	t_{PLH}	1.85	1.77 + 0.041*SL	1.79 + 0.036*SL	1.80 + 0.034*SL
	t_{PHL}	1.40	1.30 + 0.048*SL	1.31 + 0.045*SL	1.32 + 0.044*SL
	t_R	0.30	0.16 + 0.069*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.079*SL	0.12 + 0.082*SL
SN to QN1	t_{PHL}	0.46	0.36 + 0.051*SL	0.37 + 0.046*SL	0.38 + 0.045*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.13 + 0.082*SL
CK to QN2	t_{PLH}	1.85	1.77 + 0.041*SL	1.79 + 0.036*SL	1.80 + 0.034*SL
	t_{PHL}	1.40	1.30 + 0.048*SL	1.31 + 0.045*SL	1.32 + 0.044*SL
	t_R	0.30	0.16 + 0.069*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.079*SL	0.12 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



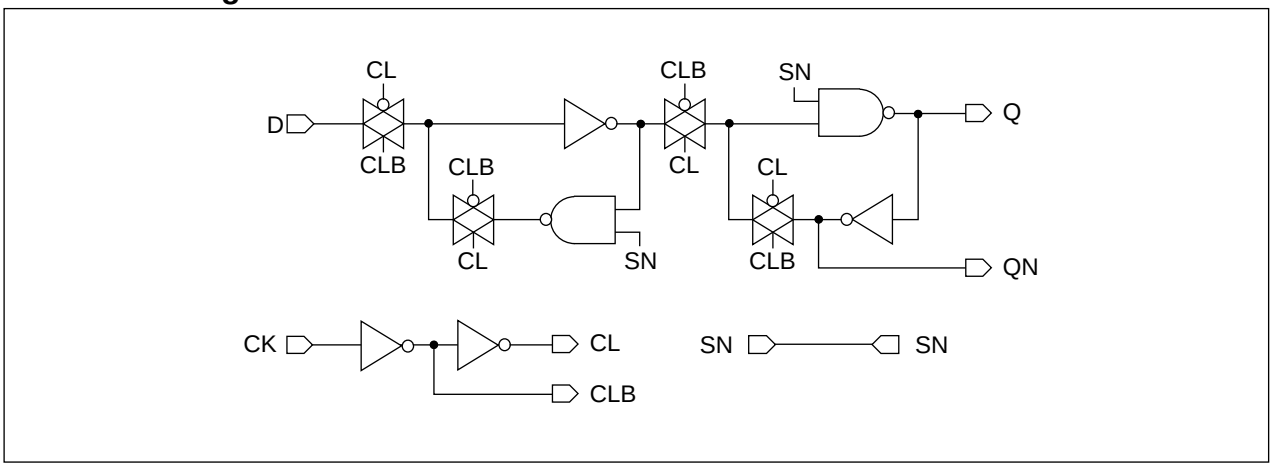
Truth Table

D	CK	SN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
STD80							
YFD3			*YFD3D2*			*YFD3*	*YFD3D2*
D	CK	SN	D	CK	SN		
1.8	0.5	1.2	1.8	0.5	2.4	5.0	6.3
STDM80							
YFD3			*YFD3D2*			*YFD3*	*YFD3D2*
D	CK	SN	D	CK	SN		
2.0	0.6	1.6	2.0	0.6	2.8	5.0	6.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		YFD3	YFD3D2	YFD3	YFD3D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.85	0.85
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.85	0.98
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.38	0.38	0.41	0.41
Input Hold Time (D to CK)	t_{HD}	0.46	0.49	0.49	0.49
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.66	0.60	0.71	0.71

YFD3/YFD3D2

Fast D Flip-Flop with Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 YFD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.52	0.47 + 0.027*SL	0.47 + 0.025*SL	0.48 + 0.025*SL
	t_{PHL}	0.58	0.50 + 0.040*SL	0.50 + 0.039*SL	0.50 + 0.039*SL
	t_R	0.29	0.20 + 0.046*SL	0.19 + 0.051*SL	0.16 + 0.054*SL
	t_F	0.39	0.25 + 0.068*SL	0.24 + 0.073*SL	0.20 + 0.078*SL
SN to Q	t_{PLH}	0.19	0.13 + 0.032*SL	0.14 + 0.025*SL	0.26 + 0.013*SL
	t_R	0.32	0.24 + 0.040*SL	0.26 + 0.031*SL	0.31 + 0.025*SL
CK to QN	t_{PLH}	0.71	0.55 + 0.081*SL	0.55 + 0.079*SL	0.56 + 0.078*SL
	t_{PHL}	0.70	0.55 + 0.076*SL	0.55 + 0.073*SL	0.56 + 0.073*SL
	t_R	0.24	0.11 + 0.065*SL	0.11 + 0.067*SL	0.10 + 0.068*SL
	t_F	0.24	0.09 + 0.075*SL	0.09 + 0.076*SL	0.09 + 0.077*SL
SN to QN	t_{PHL}	0.37	0.21 + 0.078*SL	0.23 + 0.068*SL	0.36 + 0.056*SL
	t_F	0.24	0.10 + 0.071*SL	0.10 + 0.071*SL	0.09 + 0.071*SL

STD80 YFD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.54	0.51 + 0.016*SL	0.51 + 0.014*SL	0.53 + 0.012*SL
	t_{PHL}	0.65	0.61 + 0.024*SL	0.61 + 0.022*SL	0.64 + 0.019*SL
	t_R	0.26	0.22 + 0.021*SL	0.21 + 0.024*SL	0.18 + 0.027*SL
	t_F	0.40	0.33 + 0.034*SL	0.33 + 0.034*SL	0.29 + 0.038*SL
SN to Q	t_{PLH}	0.17	0.14 + 0.016*SL	0.15 + 0.014*SL	0.20 + 0.008*SL
	t_R	0.30	0.27 + 0.016*SL	0.26 + 0.021*SL	0.35 + 0.012*SL
CK to QN	t_{PLH}	0.75	0.66 + 0.046*SL	0.67 + 0.042*SL	0.69 + 0.039*SL
	t_{PHL}	0.65	0.57 + 0.040*SL	0.58 + 0.038*SL	0.60 + 0.036*SL
	t_R	0.18	0.12 + 0.030*SL	0.11 + 0.033*SL	0.10 + 0.034*SL
	t_F	0.16	0.08 + 0.038*SL	0.08 + 0.037*SL	0.07 + 0.038*SL
SN to QN	t_{PHL}	0.29	0.21 + 0.040*SL	0.22 + 0.037*SL	0.30 + 0.028*SL
	t_F	0.16	0.09 + 0.037*SL	0.09 + 0.037*SL	0.10 + 0.035*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 YFD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.75	0.68 + 0.038*SL	0.68 + 0.036*SL	0.69 + 0.035*SL
	t_{PHL}	0.83	0.72 + 0.056*SL	0.73 + 0.052*SL	0.74 + 0.051*SL
	t_R	0.40	0.26 + 0.069*SL	0.26 + 0.072*SL	0.24 + 0.074*SL
	t_F	0.52	0.34 + 0.088*SL	0.32 + 0.094*SL	0.30 + 0.096*SL
SN to Q	t_{PLH}	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_R	0.37	0.24 + 0.067*SL	0.26 + 0.059*SL	0.42 + 0.036*SL
CK to QN	t_{PLH}	1.03	0.81 + 0.114*SL	0.82 + 0.110*SL	0.83 + 0.108*SL
	t_{PHL}	0.99	0.79 + 0.101*SL	0.79 + 0.099*SL	0.80 + 0.098*SL
	t_R	0.33	0.15 + 0.091*SL	0.15 + 0.090*SL	0.15 + 0.091*SL
	t_F	0.31	0.12 + 0.094*SL	0.12 + 0.095*SL	0.12 + 0.095*SL
SN to QN	t_{PHL}	0.48	0.28 + 0.099*SL	0.29 + 0.096*SL	0.36 + 0.085*SL
	t_F	0.30	0.12 + 0.094*SL	0.12 + 0.091*SL	0.18 + 0.083*SL

STDM80 YFD3D2

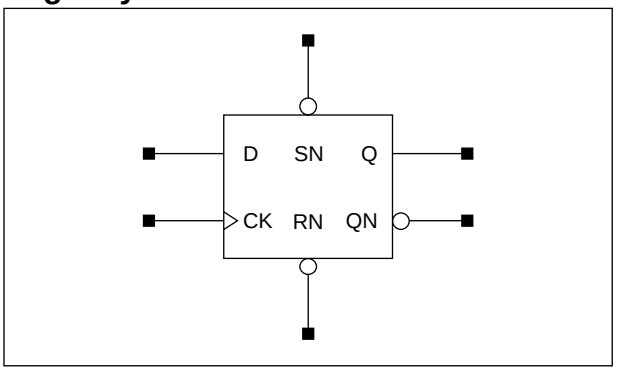
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.77	0.72 + 0.022*SL	0.73 + 0.020*SL	0.74 + 0.019*SL
	t_{PHL}	0.97	0.90 + 0.036*SL	0.91 + 0.032*SL	0.93 + 0.029*SL
	t_R	0.34	0.28 + 0.031*SL	0.27 + 0.034*SL	0.26 + 0.035*SL
	t_F	0.54	0.45 + 0.046*SL	0.45 + 0.046*SL	0.45 + 0.046*SL
SN to Q	t_{PLH}	0.22	0.18 + 0.019*SL	0.19 + 0.017*SL	0.18 + 0.017*SL
	t_R	0.33	0.27 + 0.028*SL	0.25 + 0.034*SL	0.25 + 0.034*SL
CK to QN	t_{PLH}	1.12	0.99 + 0.066*SL	1.00 + 0.062*SL	1.03 + 0.058*SL
	t_{PHL}	0.93	0.82 + 0.054*SL	0.83 + 0.051*SL	0.84 + 0.049*SL
	t_R	0.24	0.15 + 0.045*SL	0.15 + 0.045*SL	0.15 + 0.045*SL
	t_F	0.20	0.11 + 0.045*SL	0.11 + 0.047*SL	0.11 + 0.046*SL
SN to QN	t_{PHL}	0.37	0.27 + 0.050*SL	0.28 + 0.049*SL	0.28 + 0.048*SL
	t_F	0.19	0.10 + 0.047*SL	0.10 + 0.047*SL	0.11 + 0.046*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

FD4/FD4D2

D Flip-Flop with Reset, Set, 1X/2X Drive

Logic Symbol



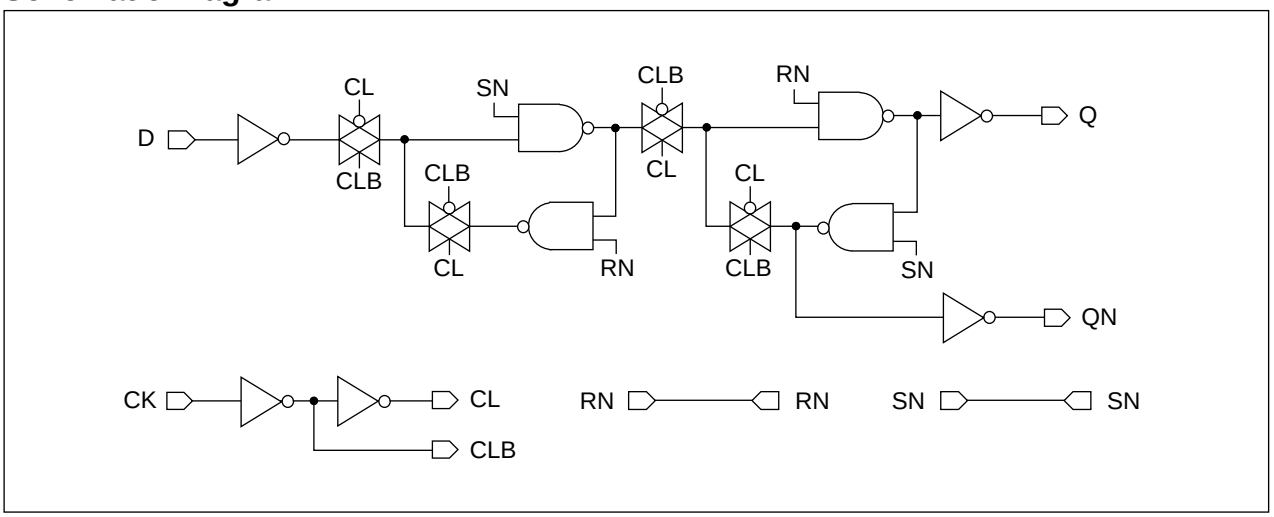
Truth Table

D	CK	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
STD80									
FD4				*FD4D2*				*FD4*	*FD4D2*
D	CK	RN	SN	D	CK	RN	SN		
0.5	0.5	1.1	0.7	0.6	0.6	1.2	1.1	7.7	8.3
STDM80									
FD4				*FD4D2*				*FD4*	*FD4D2*
D	CK	RN	SN	D	CK	RN	SN		
0.6	0.6	1.6	1.6	0.6	0.6	1.6	1.6	7.7	8.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD4	FD4D2	FD4	FD4D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.96	0.96
Pulse Width High (CK)	t_{PWH}	0.79	0.79	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.96	0.96
Input Setup Time (D to CK)	t_{SU}	0.52	0.52	0.63	0.63
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71	0.82	0.82
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.38	0.38	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.57 + 0.032*SL	0.59 + 0.026*SL	0.61 + 0.024*SL
	t_{PHL}	0.73	0.64 + 0.041*SL	0.65 + 0.038*SL	0.66 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PLH}	0.33	0.27 + 0.032*SL	0.28 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to Q	t_{PLH}	0.65	0.59 + 0.031*SL	0.60 + 0.026*SL	0.62 + 0.023*SL
	t_R	0.23	0.14 + 0.048*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
CK to QN	t_{PLH}	0.84	0.78 + 0.030*SL	0.79 + 0.025*SL	0.81 + 0.024*SL
	t_{PHL}	0.86	0.78 + 0.038*SL	0.79 + 0.037*SL	0.78 + 0.037*SL
	t_R	0.22	0.12 + 0.046*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.48	0.42 + 0.030*SL	0.43 + 0.025*SL	0.45 + 0.023*SL
	t_R	0.22	0.12 + 0.047*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
SN to QN	t_{PLH}	0.33	0.26 + 0.031*SL	0.28 + 0.025*SL	0.29 + 0.024*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

STD80 FD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.65	0.61 + 0.021*SL	0.62 + 0.015*SL	0.65 + 0.012*SL
	t_{PHL}	0.72	0.67 + 0.023*SL	0.68 + 0.020*SL	0.70 + 0.018*SL
	t_R	0.20	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.030*SL	0.09 + 0.034*SL
RN to Q	t_{PLH}	0.34	0.31 + 0.018*SL	0.31 + 0.015*SL	0.35 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.024*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to Q	t_{PLH}	0.67	0.63 + 0.021*SL	0.64 + 0.015*SL	0.67 + 0.012*SL
	t_R	0.20	0.15 + 0.023*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
CK to QN	t_{PLH}	0.91	0.87 + 0.018*SL	0.88 + 0.014*SL	0.91 + 0.012*SL
	t_{PHL}	0.94	0.90 + 0.019*SL	0.90 + 0.017*SL	0.90 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.19	0.12 + 0.032*SL	0.13 + 0.030*SL	0.09 + 0.034*SL
RN to QN	t_{PLH}	0.55	0.51 + 0.018*SL	0.52 + 0.014*SL	0.55 + 0.012*SL
	t_R	0.19	0.14 + 0.024*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.022*SL	0.31 + 0.015*SL	0.35 + 0.012*SL
	t_{PHL}	0.35	0.31 + 0.023*SL	0.31 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.91	0.82 + 0.043*SL	0.84 + 0.037*SL	0.86 + 0.035*SL
	t_{PHL}	1.03	0.92 + 0.052*SL	0.94 + 0.047*SL	0.95 + 0.045*SL
	t_R	0.31	0.18 + 0.069*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q	t_{PLH}	0.44	0.35 + 0.043*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.047*SL	0.39 + 0.045*SL
	t_R	0.30	0.17 + 0.068*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
SN to Q	t_{PLH}	0.94	0.85 + 0.044*SL	0.87 + 0.037*SL	0.89 + 0.034*SL
	t_R	0.32	0.18 + 0.067*SL	0.18 + 0.067*SL	0.17 + 0.069*SL
CK to QN	t_{PLH}	1.22	1.14 + 0.041*SL	1.15 + 0.036*SL	1.17 + 0.034*SL
	t_{PHL}	1.22	1.12 + 0.049*SL	1.14 + 0.045*SL	1.14 + 0.044*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.15 + 0.078*SL	0.14 + 0.079*SL	0.13 + 0.081*SL
RN to QN	t_{PLH}	0.67	0.58 + 0.042*SL	0.60 + 0.036*SL	0.62 + 0.034*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
SN to QN	t_{PLH}	0.44	0.35 + 0.042*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.46	0.36 + 0.051*SL	0.38 + 0.046*SL	0.38 + 0.045*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.069*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

STDM80 FD4D2

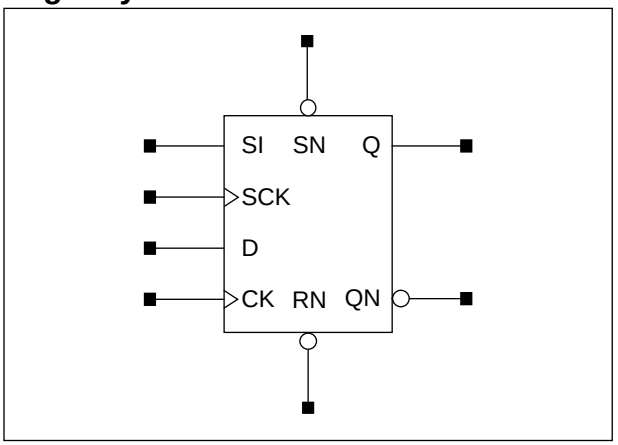
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.92	0.87 + 0.028*SL	0.88 + 0.023*SL	0.91 + 0.019*SL
	t_{PHL}	1.02	0.96 + 0.031*SL	0.98 + 0.026*SL	0.99 + 0.023*SL
	t_R	0.25	0.18 + 0.036*SL	0.18 + 0.034*SL	0.18 + 0.034*SL
	t_F	0.23	0.15 + 0.041*SL	0.16 + 0.038*SL	0.16 + 0.038*SL
RN to Q	t_{PLH}	0.45	0.39 + 0.027*SL	0.41 + 0.022*SL	0.43 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.21	0.13 + 0.042*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
SN to Q	t_{PLH}	0.95	0.90 + 0.028*SL	0.92 + 0.022*SL	0.94 + 0.019*SL
	t_R	0.25	0.18 + 0.035*SL	0.19 + 0.034*SL	0.19 + 0.033*SL
CK to QN	t_{PLH}	1.32	1.27 + 0.024*SL	1.28 + 0.021*SL	1.30 + 0.019*SL
	t_{PHL}	1.33	1.27 + 0.026*SL	1.28 + 0.023*SL	1.29 + 0.022*SL
	t_R	0.24	0.17 + 0.037*SL	0.17 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.23	0.15 + 0.040*SL	0.16 + 0.038*SL	0.16 + 0.037*SL
RN to QN	t_{PLH}	0.76	0.71 + 0.025*SL	0.72 + 0.021*SL	0.73 + 0.019*SL
	t_R	0.24	0.17 + 0.037*SL	0.18 + 0.034*SL	0.18 + 0.034*SL
SN to QN	t_{PLH}	0.45	0.40 + 0.027*SL	0.41 + 0.022*SL	0.43 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.16 + 0.037*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.21	0.12 + 0.042*SL	0.14 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

FD4CS/FD4CSD2

D Flip-Flop with Reset, Set, Scan Clock, 1X/2X Drive

Logic Symbol



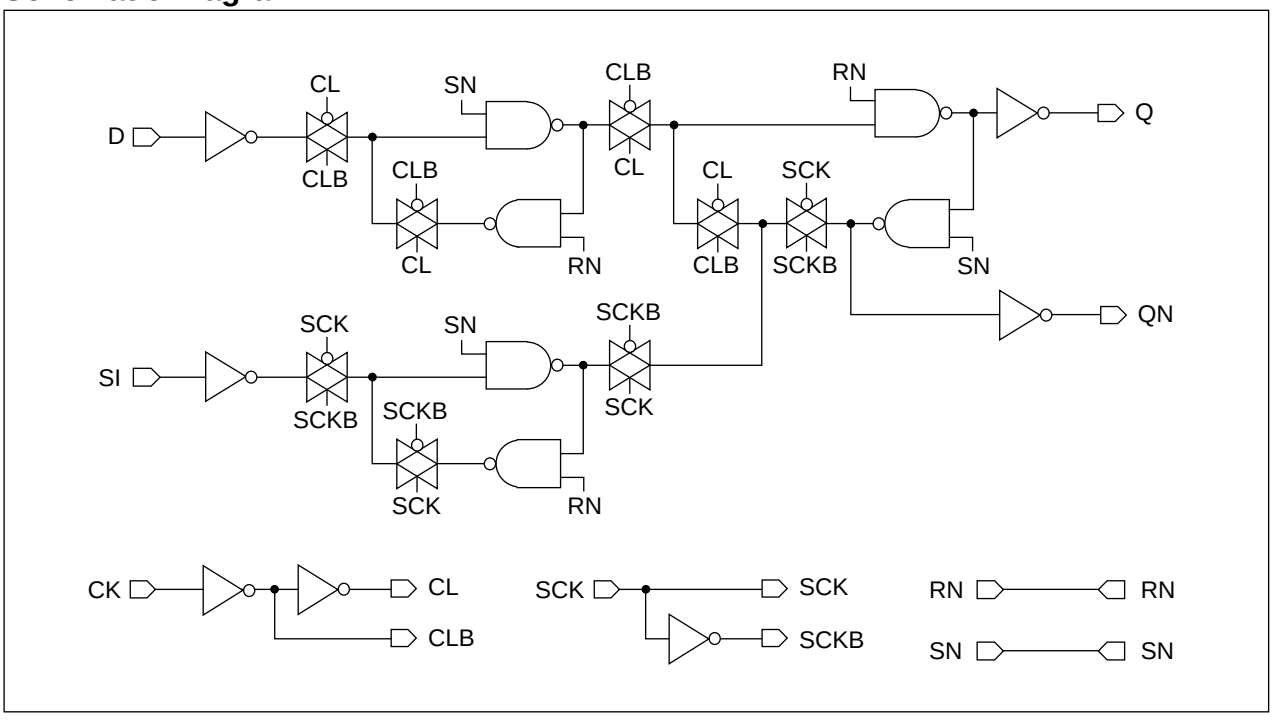
Truth Table

SI	SCK	D	CK	RN	SN	Q (n+1)	QN (n+1)
x	0	0	⎍	1	1	0	1
x	0	1	⎍	1	1	1	0
0	⎍	x	0	1	1	0	1
1	⎍	x	0	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0

Cell Data

Input Load (SL)												Gate Count	
STD80													
FD4CS						*FD4CSD2*						*FD4CS*	*FD4CSD2*
SI	SCK	D	CK	RN	SN	SI	SCK	D	CK	RN	SN		
0.6	2.1	0.6	0.6	1.8	1.8	0.6	2.1	0.6	0.6	1.9	1.8	12.3	12.7
STDM80													
FD4CS						*FD4CSD2*						*FD4CS*	*FD4CSD2*
SI	SCK	D	CK	RN	SN	SI	SCK	D	CK	RN	SN		
0.6	1.9	0.6	0.6	2.4	2.5	0.6	1.9	0.6	0.6	2.4	2.5	12.3	12.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD4CS	FD4CSD2	FD4CS	FD4CSD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.96	0.96
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (SCK)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width High (SCK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.96	0.96	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.98	1.01
Input Setup Time (D to CK)	t_{SU}	0.52	0.52	0.63	0.63
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.74	0.74	0.93	0.93
Input Hold Time (SI to SCK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN to CK)	t_{RC}	0.44	0.44	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71	0.82	0.82
Recovery Time (RN to SCK)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to SCK)	t_{HD}	0.55	0.55	0.60	0.60
Recovery Time (SN to CK)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.38	0.38	0.44	0.44
Recovery Time (SN to SCK)	t_{RC}	0.33	0.33	0.52	0.52
Input Hold Time (SN to SCK)	t_{HD}	0.33	0.33	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD4CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.65	0.59 + 0.031*SL	0.60 + 0.026*SL	0.62 + 0.024*SL
	t_{PHL}	0.70	0.62 + 0.041*SL	0.63 + 0.038*SL	0.64 + 0.037*SL
	t_R	0.23	0.14 + 0.046*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.065*SL	0.11 + 0.067*SL	0.08 + 0.069*SL
SCK to Q	t_{PLH}	0.74	0.67 + 0.033*SL	0.68 + 0.026*SL	0.71 + 0.024*SL
	t_{PHL}	0.65	0.57 + 0.042*SL	0.58 + 0.038*SL	0.59 + 0.037*SL
	t_R	0.26	0.16 + 0.046*SL	0.16 + 0.047*SL	0.12 + 0.052*SL
	t_F	0.25	0.13 + 0.062*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
SN to Q	t_{PLH}	0.68	0.62 + 0.033*SL	0.63 + 0.026*SL	0.65 + 0.024*SL
	t_R	0.23	0.14 + 0.044*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
RN to Q	t_{PLH}	0.31	0.25 + 0.031*SL	0.26 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.38	0.30 + 0.040*SL	0.31 + 0.038*SL	0.32 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.13 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.11 + 0.067*SL	0.09 + 0.069*SL
CK to QN	t_{PLH}	0.90	0.83 + 0.037*SL	0.85 + 0.027*SL	0.88 + 0.024*SL
	t_{PHL}	0.94	0.86 + 0.041*SL	0.87 + 0.038*SL	0.88 + 0.037*SL
	t_R	0.27	0.17 + 0.049*SL	0.17 + 0.048*SL	0.14 + 0.051*SL
	t_F	0.26	0.14 + 0.065*SL	0.13 + 0.066*SL	0.10 + 0.069*SL
SCK to QN	t_{PLH}	0.76	0.70 + 0.029*SL	0.71 + 0.025*SL	0.72 + 0.024*SL
	t_{PHL}	0.96	0.88 + 0.038*SL	0.88 + 0.037*SL	0.88 + 0.037*SL
	t_R	0.21	0.12 + 0.047*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.061*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
SN to QN	t_{PLH}	0.41	0.33 + 0.037*SL	0.36 + 0.027*SL	0.39 + 0.024*SL
	t_{PHL}	0.42	0.33 + 0.043*SL	0.34 + 0.039*SL	0.36 + 0.037*SL
	t_R	0.27	0.17 + 0.047*SL	0.17 + 0.047*SL	0.13 + 0.051*SL
	t_F	0.26	0.13 + 0.064*SL	0.12 + 0.066*SL	0.10 + 0.069*SL
RN to QN	t_{PLH}	0.49	0.43 + 0.029*SL	0.44 + 0.025*SL	0.45 + 0.023*SL
	t_R	0.21	0.12 + 0.047*SL	0.12 + 0.049*SL	0.09 + 0.052*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD4CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.67	0.63 + 0.021*SL	0.64 + 0.016*SL	0.67 + 0.012*SL
	t_{PHL}	0.70	0.65 + 0.023*SL	0.66 + 0.020*SL	0.68 + 0.018*SL
	t_R	0.20	0.15 + 0.023*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
SCK to Q	t_{PLH}	0.77	0.72 + 0.023*SL	0.73 + 0.016*SL	0.77 + 0.012*SL
	t_{PHL}	0.66	0.61 + 0.023*SL	0.62 + 0.020*SL	0.63 + 0.018*SL
	t_R	0.22	0.18 + 0.022*SL	0.18 + 0.023*SL	0.15 + 0.025*SL
	t_F	0.19	0.13 + 0.029*SL	0.13 + 0.030*SL	0.10 + 0.034*SL
SN to Q	t_{PLH}	0.70	0.66 + 0.021*SL	0.67 + 0.015*SL	0.71 + 0.012*SL
	t_R	0.20	0.15 + 0.025*SL	0.16 + 0.023*SL	0.13 + 0.026*SL
RN to Q	t_{PLH}	0.33	0.29 + 0.019*SL	0.30 + 0.016*SL	0.33 + 0.012*SL
	t_{PHL}	0.38	0.33 + 0.023*SL	0.34 + 0.020*SL	0.35 + 0.018*SL
	t_R	0.20	0.15 + 0.023*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
CK to QN	t_{PLH}	0.97	0.92 + 0.022*SL	0.93 + 0.017*SL	0.98 + 0.012*SL
	t_{PHL}	1.03	0.98 + 0.022*SL	0.99 + 0.018*SL	0.99 + 0.018*SL
	t_R	0.24	0.19 + 0.026*SL	0.19 + 0.023*SL	0.17 + 0.025*SL
	t_F	0.21	0.15 + 0.033*SL	0.15 + 0.031*SL	0.12 + 0.033*SL
SCK to QN	t_{PLH}	0.83	0.80 + 0.017*SL	0.81 + 0.014*SL	0.83 + 0.012*SL
	t_{PHL}	1.05	1.01 + 0.018*SL	1.02 + 0.017*SL	1.00 + 0.018*SL
	t_R	0.19	0.14 + 0.024*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.19	0.12 + 0.032*SL	0.13 + 0.030*SL	0.09 + 0.034*SL
SN to QN	t_{PLH}	0.42	0.37 + 0.023*SL	0.38 + 0.017*SL	0.43 + 0.012*SL
	t_{PHL}	0.41	0.36 + 0.025*SL	0.37 + 0.020*SL	0.39 + 0.018*SL
	t_R	0.23	0.18 + 0.025*SL	0.19 + 0.024*SL	0.17 + 0.025*SL
	t_F	0.20	0.13 + 0.034*SL	0.13 + 0.031*SL	0.11 + 0.034*SL
RN to QN	t_{PLH}	0.55	0.52 + 0.018*SL	0.53 + 0.014*SL	0.55 + 0.012*SL
	t_R	0.19	0.14 + 0.024*SL	0.14 + 0.023*SL	0.11 + 0.026*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD4CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.94	0.85 + 0.044*SL	0.87 + 0.037*SL	0.89 + 0.035*SL
	t_{PHL}	1.00	0.90 + 0.052*SL	0.91 + 0.046*SL	0.92 + 0.045*SL
	t_R	0.32	0.18 + 0.068*SL	0.18 + 0.070*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.14 + 0.082*SL
SCK to Q	t_{PLH}	1.11	1.02 + 0.045*SL	1.05 + 0.038*SL	1.07 + 0.035*SL
	t_{PHL}	0.93	0.82 + 0.053*SL	0.84 + 0.047*SL	0.86 + 0.045*SL
	t_R	0.35	0.22 + 0.067*SL	0.21 + 0.068*SL	0.21 + 0.069*SL
	t_F	0.33	0.17 + 0.080*SL	0.17 + 0.079*SL	0.15 + 0.081*SL
SN to Q	t_{PLH}	0.98	0.89 + 0.044*SL	0.92 + 0.037*SL	0.93 + 0.034*SL
	t_R	0.32	0.19 + 0.066*SL	0.18 + 0.068*SL	0.17 + 0.070*SL
RN to Q	t_{PLH}	0.43	0.35 + 0.043*SL	0.37 + 0.036*SL	0.38 + 0.034*SL
	t_{PHL}	0.49	0.39 + 0.051*SL	0.41 + 0.047*SL	0.41 + 0.045*SL
	t_R	0.31	0.17 + 0.068*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.31	0.14 + 0.082*SL	0.14 + 0.081*SL	0.14 + 0.082*SL
CK to QN	t_{PLH}	1.30	1.20 + 0.051*SL	1.23 + 0.041*SL	1.26 + 0.036*SL
	t_{PHL}	1.35	1.24 + 0.054*SL	1.26 + 0.048*SL	1.28 + 0.046*SL
	t_R	0.37	0.22 + 0.073*SL	0.24 + 0.068*SL	0.24 + 0.068*SL
	t_F	0.34	0.17 + 0.085*SL	0.18 + 0.081*SL	0.19 + 0.080*SL
SCK to QN	t_{PLH}	1.10	1.02 + 0.041*SL	1.04 + 0.035*SL	1.05 + 0.034*SL
	t_{PHL}	1.42	1.32 + 0.048*SL	1.33 + 0.045*SL	1.34 + 0.044*SL
	t_R	0.30	0.16 + 0.071*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.13 + 0.082*SL
SN to QN	t_{PLH}	0.54	0.44 + 0.051*SL	0.47 + 0.041*SL	0.50 + 0.036*SL
	t_{PHL}	0.55	0.44 + 0.056*SL	0.46 + 0.050*SL	0.48 + 0.046*SL
	t_R	0.37	0.22 + 0.073*SL	0.24 + 0.068*SL	0.23 + 0.068*SL
	t_F	0.33	0.16 + 0.085*SL	0.17 + 0.082*SL	0.18 + 0.081*SL
RN to QN	t_{PLH}	0.80	0.70 + 0.051*SL	0.73 + 0.041*SL	0.76 + 0.036*SL
	t_R	0.37	0.23 + 0.071*SL	0.24 + 0.068*SL	0.23 + 0.068*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD4CSD2

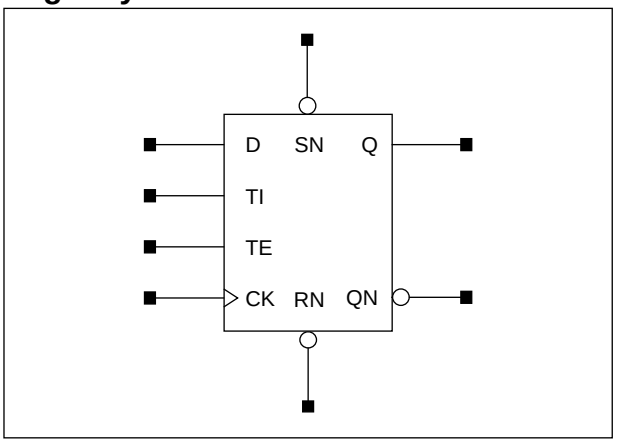
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.96	0.91 + 0.028*SL	0.92 + 0.023*SL	0.94 + 0.020*SL
	t_{PHL}	1.00	0.93 + 0.031*SL	0.95 + 0.026*SL	0.97 + 0.023*SL
	t_R	0.26	0.19 + 0.035*SL	0.19 + 0.034*SL	0.19 + 0.034*SL
	t_F	0.22	0.14 + 0.041*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
SCK to Q	t_{PLH}	1.16	1.10 + 0.029*SL	1.12 + 0.023*SL	1.14 + 0.020*SL
	t_{PHL}	0.93	0.87 + 0.032*SL	0.89 + 0.027*SL	0.91 + 0.023*SL
	t_R	0.29	0.22 + 0.034*SL	0.22 + 0.033*SL	0.22 + 0.034*SL
	t_F	0.24	0.16 + 0.040*SL	0.17 + 0.038*SL	0.17 + 0.038*SL
SN to Q	t_{PLH}	1.01	0.95 + 0.028*SL	0.97 + 0.023*SL	0.99 + 0.019*SL
	t_R	0.26	0.19 + 0.035*SL	0.19 + 0.034*SL	0.20 + 0.033*SL
RN to Q	t_{PLH}	0.45	0.40 + 0.028*SL	0.41 + 0.023*SL	0.43 + 0.019*SL
	t_{PHL}	0.49	0.42 + 0.031*SL	0.44 + 0.026*SL	0.46 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.039*SL	0.15 + 0.038*SL
CK to QN	t_{PLH}	1.39	1.33 + 0.031*SL	1.35 + 0.025*SL	1.37 + 0.021*SL
	t_{PHL}	1.46	1.40 + 0.029*SL	1.41 + 0.025*SL	1.43 + 0.023*SL
	t_R	0.30	0.22 + 0.039*SL	0.23 + 0.036*SL	0.25 + 0.034*SL
	t_F	0.26	0.17 + 0.043*SL	0.18 + 0.040*SL	0.19 + 0.039*SL
SCK to QN	t_{PLH}	1.21	1.16 + 0.024*SL	1.17 + 0.021*SL	1.19 + 0.019*SL
	t_{PHL}	1.56	1.51 + 0.024*SL	1.52 + 0.022*SL	1.52 + 0.021*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.23	0.15 + 0.043*SL	0.17 + 0.036*SL	0.16 + 0.037*SL
SN to QN	t_{PLH}	0.55	0.48 + 0.033*SL	0.50 + 0.026*SL	0.53 + 0.022*SL
	t_{PHL}	0.53	0.47 + 0.033*SL	0.48 + 0.028*SL	0.50 + 0.025*SL
	t_R	0.30	0.22 + 0.038*SL	0.23 + 0.036*SL	0.24 + 0.034*SL
	t_F	0.24	0.16 + 0.042*SL	0.16 + 0.040*SL	0.17 + 0.039*SL
RN to QN	t_{PLH}	0.88	0.82 + 0.030*SL	0.84 + 0.025*SL	0.86 + 0.021*SL
	t_R	0.30	0.22 + 0.039*SL	0.23 + 0.036*SL	0.24 + 0.034*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

FD4S/FD4SD2

D Flip-Flop with Reset, Set, Scan, 1X/2X Drive

Logic Symbol



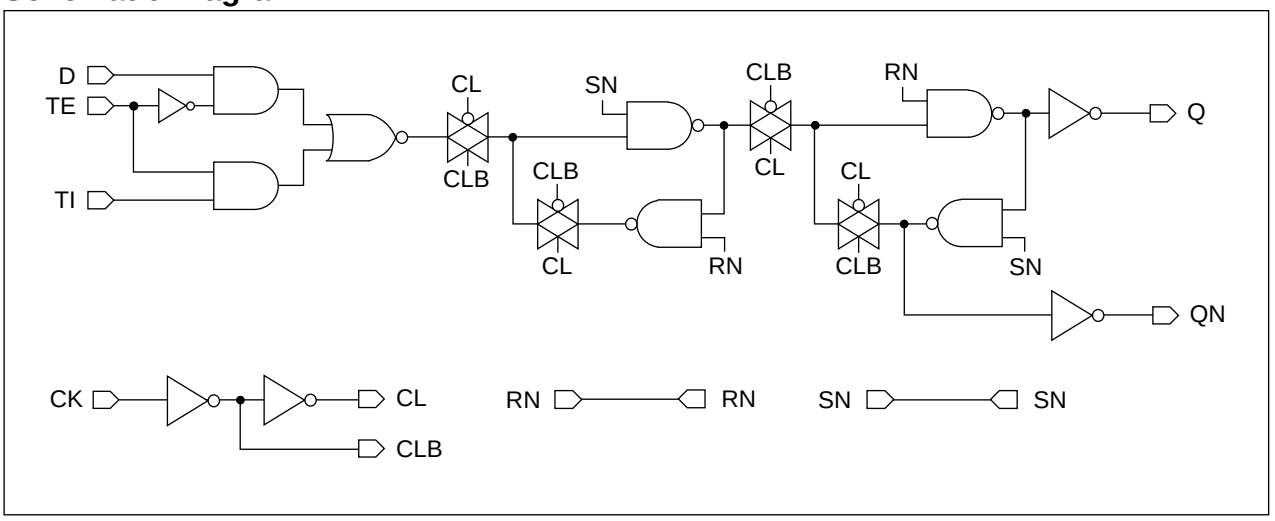
Truth Table

D	TI	TE	CK	RN	SN	Q (n+1)	QN (n+1)
0	x	0	⎍	1	1	0	1
1	x	0	⎍	1	1	1	0
x	0	1	⎍	1	1	0	1
x	1	1	⎍	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	x	x	⎎	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)												Gate Count	
STD80													
FD4S						*FD4SD2*						*FD4S*	*FD4SD2*
D	TI	TE	CK	RN	SN	D	TI	TE	CK	RN	SN		
0.3	0.5	1.0	0.5	0.9	0.7	0.3	0.5	0.9	0.5	0.9	0.7	9.3	10.0
STDM80													
FD4S						*FD4SD2*						*FD4S*	*FD4SD2*
D	TI	TE	CK	RN	SN	D	TI	TE	CK	RN	SN		
0.6	0.6	1.1	0.6	1.6	1.6	0.6	0.6	1.1	0.6	1.6	1.6	9.3	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD4S	FD4SD2	FD4S	FD4SD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	1.01	1.01
Pulse Width High (CK)	t_{PWH}	0.79	0.79	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.96	0.96
Input Setup Time (D to CK)	t_{SU}	0.63	0.63	0.85	0.85
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.66	0.66	0.93	0.93
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.71	0.71	1.01	1.01
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71	0.82	0.82
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.44	0.44	0.49	0.49

FD4S/FD4SD2

D Flip-Flop with Reset, Set, Scan, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD4S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.65	0.59 + 0.031*SL	0.60 + 0.026*SL	0.62 + 0.024*SL
	t_{PHL}	0.74	0.66 + 0.041*SL	0.67 + 0.038*SL	0.68 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PLH}	0.33	0.27 + 0.030*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to Q	t_{PLH}	0.66	0.59 + 0.031*SL	0.61 + 0.026*SL	0.62 + 0.024*SL
	t_R	0.23	0.14 + 0.049*SL	0.14 + 0.047*SL	0.10 + 0.052*SL
CK to QN	t_{PLH}	0.86	0.80 + 0.030*SL	0.81 + 0.025*SL	0.83 + 0.024*SL
	t_{PHL}	0.87	0.80 + 0.038*SL	0.80 + 0.037*SL	0.80 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.48	0.42 + 0.030*SL	0.43 + 0.025*SL	0.45 + 0.023*SL
	t_R	0.22	0.12 + 0.046*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
SN to QN	t_{PLH}	0.33	0.27 + 0.030*SL	0.28 + 0.025*SL	0.29 + 0.024*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.038*SL	0.28 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

STD80 FD4SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.66	0.62 + 0.021*SL	0.63 + 0.015*SL	0.67 + 0.012*SL
	t_{PHL}	0.74	0.69 + 0.023*SL	0.70 + 0.020*SL	0.72 + 0.018*SL
	t_R	0.20	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
RN to Q	t_{PLH}	0.35	0.30 + 0.022*SL	0.32 + 0.015*SL	0.35 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.020*SL	0.33 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to Q	t_{PLH}	0.67	0.63 + 0.021*SL	0.64 + 0.015*SL	0.67 + 0.012*SL
	t_R	0.20	0.15 + 0.023*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
CK to QN	t_{PLH}	0.93	0.89 + 0.018*SL	0.90 + 0.014*SL	0.93 + 0.012*SL
	t_{PHL}	0.95	0.91 + 0.018*SL	0.92 + 0.017*SL	0.91 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.19	0.12 + 0.031*SL	0.13 + 0.030*SL	0.09 + 0.034*SL
RN to QN	t_{PLH}	0.55	0.51 + 0.018*SL	0.52 + 0.014*SL	0.55 + 0.012*SL
	t_R	0.19	0.14 + 0.025*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.021*SL	0.32 + 0.015*SL	0.35 + 0.012*SL
	t_{PHL}	0.35	0.31 + 0.023*SL	0.31 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.19	0.14 + 0.022*SL	0.14 + 0.024*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD4S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.92	0.84 + 0.044*SL	0.86 + 0.037*SL	0.87 + 0.035*SL
	t_{PHL}	1.05	0.95 + 0.052*SL	0.97 + 0.046*SL	0.98 + 0.045*SL
	t_R	0.31	0.18 + 0.069*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q	t_{PLH}	0.44	0.35 + 0.043*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.047*SL	0.39 + 0.045*SL
	t_R	0.30	0.17 + 0.068*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
SN to Q	t_{PLH}	0.94	0.85 + 0.044*SL	0.87 + 0.037*SL	0.89 + 0.034*SL
	t_R	0.32	0.19 + 0.067*SL	0.18 + 0.068*SL	0.17 + 0.069*SL
CK to QN	t_{PLH}	1.24	1.16 + 0.042*SL	1.18 + 0.036*SL	1.20 + 0.034*SL
	t_{PHL}	1.24	1.14 + 0.048*SL	1.15 + 0.045*SL	1.16 + 0.044*SL
	t_R	0.30	0.16 + 0.069*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to QN	t_{PLH}	0.67	0.58 + 0.042*SL	0.60 + 0.036*SL	0.62 + 0.034*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
SN to QN	t_{PLH}	0.44	0.35 + 0.042*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.46	0.36 + 0.051*SL	0.38 + 0.046*SL	0.38 + 0.045*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.069*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

STDM80 FD4SD2

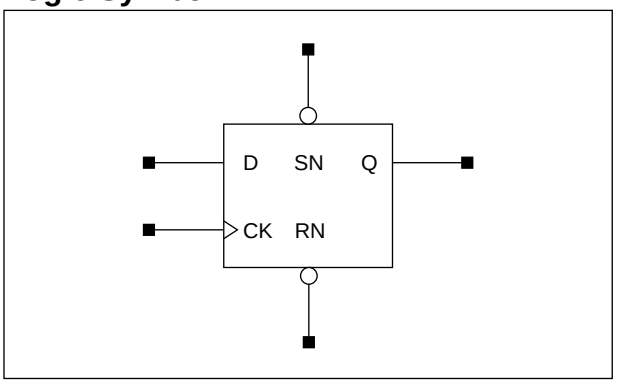
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.94	0.88 + 0.028*SL	0.90 + 0.023*SL	0.92 + 0.019*SL
	t_{PHL}	1.05	0.98 + 0.031*SL	1.00 + 0.026*SL	1.02 + 0.023*SL
	t_R	0.25	0.18 + 0.035*SL	0.18 + 0.034*SL	0.18 + 0.034*SL
	t_F	0.23	0.15 + 0.041*SL	0.16 + 0.037*SL	0.16 + 0.038*SL
RN to Q	t_{PLH}	0.45	0.39 + 0.027*SL	0.41 + 0.022*SL	0.43 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.21	0.13 + 0.042*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
SN to Q	t_{PLH}	0.96	0.90 + 0.028*SL	0.92 + 0.022*SL	0.94 + 0.019*SL
	t_R	0.25	0.18 + 0.037*SL	0.19 + 0.034*SL	0.19 + 0.033*SL
CK to QN	t_{PLH}	1.34	1.29 + 0.024*SL	1.30 + 0.021*SL	1.32 + 0.019*SL
	t_{PHL}	1.34	1.29 + 0.026*SL	1.30 + 0.023*SL	1.31 + 0.022*SL
	t_R	0.24	0.17 + 0.038*SL	0.18 + 0.034*SL	0.18 + 0.034*SL
	t_F	0.23	0.15 + 0.042*SL	0.16 + 0.037*SL	0.16 + 0.038*SL
RN to QN	t_{PLH}	0.76	0.71 + 0.025*SL	0.72 + 0.021*SL	0.74 + 0.019*SL
	t_R	0.24	0.17 + 0.036*SL	0.18 + 0.034*SL	0.18 + 0.034*SL
SN to QN	t_{PLH}	0.45	0.40 + 0.027*SL	0.41 + 0.022*SL	0.43 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.16 + 0.037*SL	0.17 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.13 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

FD4Q/FD4QD2

D Flip-Flop with Reset, Set, Q Output Only, 1X/2X Drive

Logic Symbol



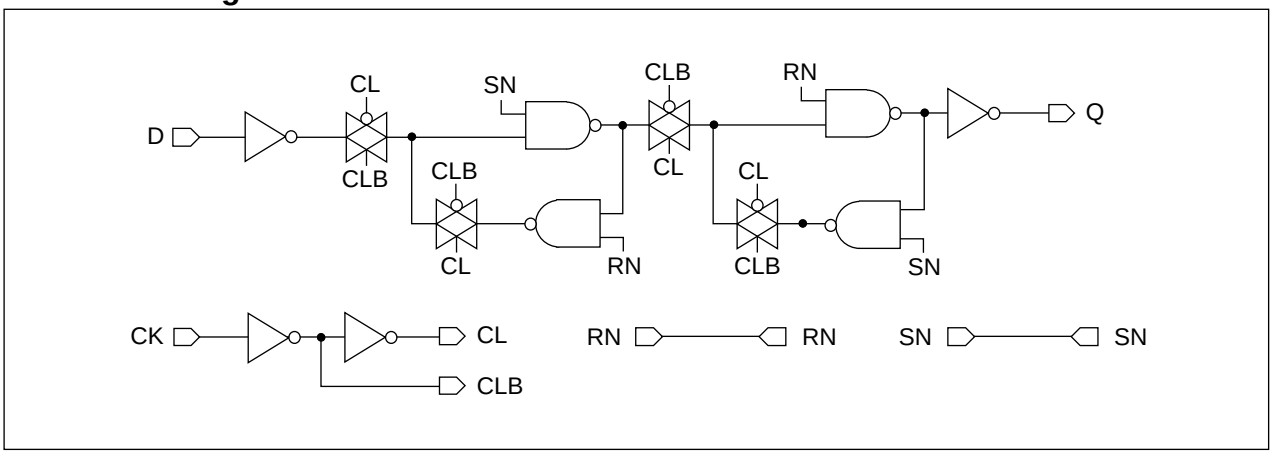
Truth Table

D	CK	RN	SN	Q (n+1)
0	↑	1	1	0
1	↑	1	1	1
x	x	1	0	1
x	x	0	1	0
x	x	0	0	0
x	↓	1	1	Q (n)

Cell Data

Input Load (SL)								Gate Count	
STD80									
FD4Q				*FD4QD2*				*FD4Q*	*FD4QD2*
D	CK	RN	SN	D	CK	RN	SN		
0.6	0.6	1.6	1.0	0.6	0.6	1.2	1.0	7.3	7.7
STDM80									
FD4Q				*FD4QD2*				*FD4Q*	*FD4QD2*
D	CK	RN	SN	D	CK	RN	SN		
0.6	0.6	1.6	1.4	0.6	0.6	1.6	1.4	7.3	7.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD4Q	FD4QD2	FD4Q	FD4QD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.96	0.96
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.96	0.96
Input Setup Time (D to CK)	t_{SU}	0.52	0.52	0.63	0.63
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71	0.82	0.82
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.38	0.38	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD4Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.56 + 0.032*SL	0.58 + 0.026*SL	0.59 + 0.024*SL
	t_{PHL}	0.71	0.63 + 0.041*SL	0.64 + 0.037*SL	0.64 + 0.037*SL
	t_R	0.22	0.13 + 0.047*SL	0.13 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PLH}	0.32	0.26 + 0.030*SL	0.27 + 0.025*SL	0.29 + 0.024*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.22	0.13 + 0.047*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to Q	t_{PLH}	0.65	0.58 + 0.032*SL	0.60 + 0.025*SL	0.61 + 0.024*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.048*SL	0.09 + 0.052*SL

STD80 FD4QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.60 + 0.020*SL	0.61 + 0.015*SL	0.64 + 0.012*SL
	t_{PHL}	0.71	0.66 + 0.023*SL	0.67 + 0.020*SL	0.68 + 0.018*SL
	t_R	0.19	0.14 + 0.024*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.18	0.12 + 0.029*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
RN to Q	t_{PLH}	0.34	0.30 + 0.018*SL	0.31 + 0.015*SL	0.34 + 0.012*SL
	t_{PHL}	0.35	0.30 + 0.023*SL	0.31 + 0.019*SL	0.32 + 0.018*SL
	t_R	0.19	0.14 + 0.022*SL	0.14 + 0.024*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to Q	t_{PLH}	0.66	0.62 + 0.021*SL	0.63 + 0.015*SL	0.66 + 0.012*SL
	t_R	0.19	0.14 + 0.025*SL	0.15 + 0.023*SL	0.12 + 0.026*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

FD4Q/FD4QD2

D Flip-Flop with Reset, Set, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD4Q

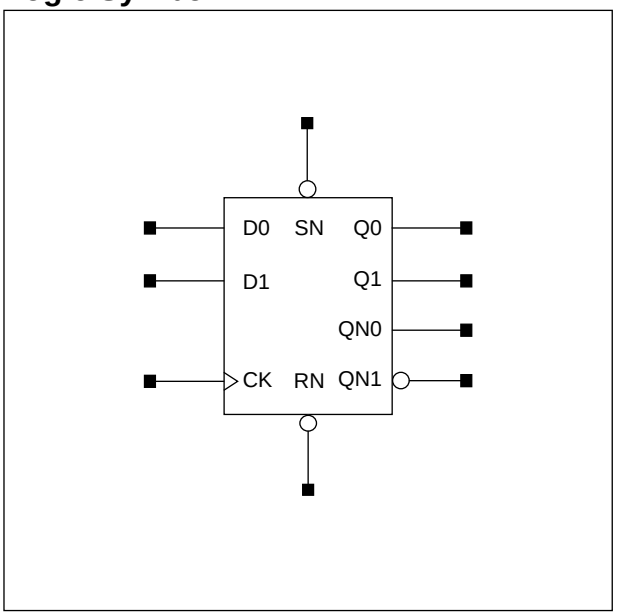
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.90	0.81 + 0.043*SL	0.83 + 0.037*SL	0.85 + 0.034*SL
	t_{PHL}	1.01	0.91 + 0.052*SL	0.92 + 0.046*SL	0.94 + 0.044*SL
	t_R	0.31	0.17 + 0.069*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.31	0.16 + 0.077*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to Q	t_{PLH}	0.43	0.34 + 0.042*SL	0.36 + 0.036*SL	0.38 + 0.034*SL
	t_{PHL}	0.46	0.36 + 0.051*SL	0.37 + 0.046*SL	0.38 + 0.045*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.069*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.081*SL	0.13 + 0.081*SL	0.13 + 0.082*SL
SN to Q	t_{PLH}	0.92	0.84 + 0.043*SL	0.86 + 0.036*SL	0.87 + 0.034*SL
	t_R	0.31	0.18 + 0.067*SL	0.18 + 0.068*SL	0.16 + 0.070*SL

STDM80 FD4QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.91	0.86 + 0.028*SL	0.87 + 0.022*SL	0.89 + 0.019*SL
	t_{PHL}	1.00	0.94 + 0.031*SL	0.96 + 0.026*SL	0.98 + 0.023*SL
	t_R	0.25	0.18 + 0.034*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.23	0.15 + 0.040*SL	0.15 + 0.038*SL	0.16 + 0.037*SL
RN to Q	t_{PLH}	0.44	0.38 + 0.027*SL	0.40 + 0.022*SL	0.42 + 0.019*SL
	t_{PHL}	0.45	0.39 + 0.030*SL	0.40 + 0.026*SL	0.42 + 0.023*SL
	t_R	0.23	0.16 + 0.037*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.21	0.13 + 0.042*SL	0.14 + 0.038*SL	0.14 + 0.038*SL
SN to Q	t_{PLH}	0.94	0.89 + 0.027*SL	0.90 + 0.022*SL	0.92 + 0.019*SL
	t_R	0.25	0.18 + 0.036*SL	0.19 + 0.033*SL	0.19 + 0.033*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

Dn	CK	RN	SN	Qn (n+1)	QNn (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↓	1	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count
STD80				
Dn	CK	RN	SN	
0.5	0.5	1.5	1.5	14.3
STDM80				
Dn	CK	RN	SN	
0.6	0.6	3.5	3.6	14.3

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CK)	t_{PWL}	0.90	1.09
Pulse Width High (CK)	t_{PWH}	0.85	0.85
Pulse Width Low (RN)	t_{PWL}	0.87	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.96
Input Setup Time (D0 to CK)	t_{SU}	0.41	0.57
Input Hold Time (D0 to CK)	t_{HD}	0.38	0.38
Input Setup Time (D1 to CK)	t_{SU}	0.41	0.57
Input Hold Time (D1 to CK)	t_{HD}	0.38	0.38
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.76	0.87
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.49	0.60

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD4X2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.71	0.65 + 0.031*SL	0.66 + 0.026*SL	0.68 + 0.024*SL
	t_{PHL}	0.88	0.79 + 0.041*SL	0.80 + 0.038*SL	0.81 + 0.037*SL
	t_R	0.23	0.14 + 0.046*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.065*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q0	t_{PLH}	0.34	0.27 + 0.033*SL	0.29 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.37	0.29 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.067*SL	0.08 + 0.069*SL
SN to Q0	t_{PLH}	0.66	0.59 + 0.032*SL	0.61 + 0.026*SL	0.63 + 0.023*SL
	t_R	0.23	0.14 + 0.046*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
CK to Q1	t_{PLH}	0.71	0.64 + 0.032*SL	0.65 + 0.026*SL	0.68 + 0.024*SL
	t_{PHL}	0.87	0.79 + 0.041*SL	0.80 + 0.038*SL	0.80 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q1	t_{PLH}	0.33	0.27 + 0.032*SL	0.28 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to Q1	t_{PLH}	0.65	0.59 + 0.032*SL	0.60 + 0.026*SL	0.62 + 0.023*SL
	t_R	0.23	0.14 + 0.045*SL	0.13 + 0.048*SL	0.10 + 0.052*SL
CK to QN0	t_{PLH}	1.00	0.94 + 0.030*SL	0.95 + 0.025*SL	0.96 + 0.024*SL
	t_{PHL}	0.93	0.86 + 0.038*SL	0.86 + 0.037*SL	0.86 + 0.037*SL
	t_R	0.22	0.13 + 0.047*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.061*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to QN0	t_{PLH}	0.49	0.43 + 0.030*SL	0.44 + 0.025*SL	0.46 + 0.023*SL
	t_R	0.22	0.12 + 0.047*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
SN to QN0	t_{PLH}	0.33	0.27 + 0.032*SL	0.28 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.28 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.065*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to QN1	t_{PLH}	0.99	0.93 + 0.030*SL	0.94 + 0.025*SL	0.95 + 0.024*SL
	t_{PHL}	0.93	0.85 + 0.037*SL	0.85 + 0.037*SL	0.85 + 0.037*SL
	t_R	0.22	0.12 + 0.048*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to QN1	t_{PLH}	0.48	0.42 + 0.030*SL	0.43 + 0.025*SL	0.45 + 0.023*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
SN to QN1	t_{PLH}	0.33	0.26 + 0.031*SL	0.28 + 0.025*SL	0.29 + 0.024*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.10 + 0.064*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD4X2

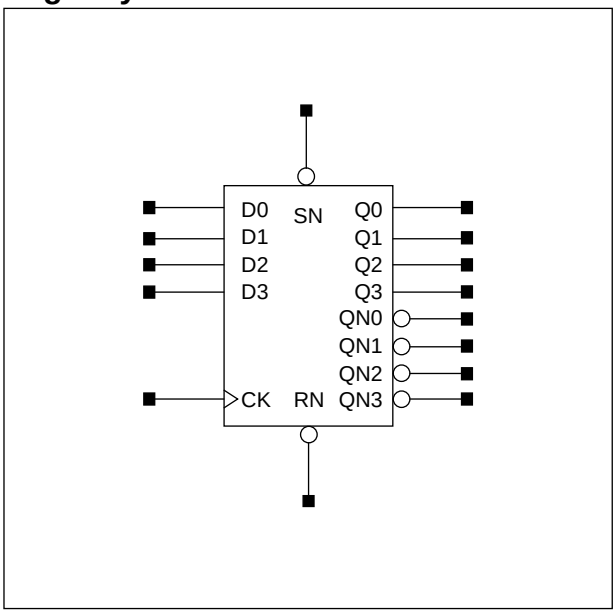
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.00	0.91 + 0.044*SL	0.93 + 0.037*SL	0.95 + 0.035*SL
	t_{PHL}	1.24	1.13 + 0.052*SL	1.15 + 0.046*SL	1.16 + 0.045*SL
	t_R	0.32	0.18 + 0.069*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q0	t_{PLH}	0.45	0.36 + 0.043*SL	0.38 + 0.036*SL	0.40 + 0.034*SL
	t_{PHL}	0.48	0.37 + 0.051*SL	0.39 + 0.046*SL	0.40 + 0.045*SL
	t_R	0.31	0.17 + 0.069*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
SN to Q0	t_{PLH}	0.94	0.85 + 0.044*SL	0.87 + 0.037*SL	0.89 + 0.034*SL
	t_R	0.32	0.19 + 0.068*SL	0.19 + 0.067*SL	0.17 + 0.069*SL
CK to Q1	t_{PLH}	0.99	0.91 + 0.044*SL	0.93 + 0.037*SL	0.94 + 0.035*SL
	t_{PHL}	1.23	1.13 + 0.052*SL	1.14 + 0.046*SL	1.16 + 0.045*SL
	t_R	0.31	0.18 + 0.069*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q1	t_{PLH}	0.44	0.35 + 0.043*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.047*SL	0.39 + 0.045*SL
	t_R	0.30	0.17 + 0.068*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
SN to Q1	t_{PLH}	0.93	0.85 + 0.044*SL	0.87 + 0.037*SL	0.89 + 0.034*SL
	t_R	0.32	0.19 + 0.067*SL	0.18 + 0.067*SL	0.17 + 0.069*SL
CK to QN0	t_{PLH}	1.43	1.35 + 0.042*SL	1.37 + 0.036*SL	1.38 + 0.034*SL
	t_{PHL}	1.31	1.22 + 0.049*SL	1.23 + 0.045*SL	1.23 + 0.044*SL
	t_R	0.30	0.17 + 0.068*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.31	0.15 + 0.078*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to QN0	t_{PLH}	0.68	0.60 + 0.042*SL	0.61 + 0.036*SL	0.63 + 0.034*SL
	t_R	0.30	0.17 + 0.068*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
SN to QN0	t_{PLH}	0.44	0.36 + 0.043*SL	0.38 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.046*SL	0.39 + 0.045*SL
	t_R	0.30	0.16 + 0.069*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.13 + 0.081*SL	0.13 + 0.082*SL
CK to QN1	t_{PLH}	1.42	1.34 + 0.042*SL	1.36 + 0.036*SL	1.37 + 0.034*SL
	t_{PHL}	1.30	1.21 + 0.048*SL	1.22 + 0.045*SL	1.22 + 0.044*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.15 + 0.079*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to QN1	t_{PLH}	0.67	0.58 + 0.042*SL	0.60 + 0.036*SL	0.62 + 0.034*SL
	t_R	0.30	0.16 + 0.069*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
SN to QN1	t_{PLH}	0.44	0.35 + 0.042*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.46	0.36 + 0.051*SL	0.38 + 0.046*SL	0.38 + 0.045*SL
	t_R	0.30	0.16 + 0.069*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

FD4X4

4-Bit D Flip-Flop with Reset, Set

Logic Symbol



Truth Table

Dn	CK	RN	SN	Qn (n+1)	QNn (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↓	1	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count
STD80				
Dn	CK	RN	SN	
0.5	0.5	4.6	4.6	27.7
STDM80				
Dn	CK	RN	SN	
0.6	0.6	7.1	7.5	27.7

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CK)	t_{PWL}	0.93	1.72
Pulse Width High (CK)	t_{PWH}	0.87	1.15
Pulse Width Low (RN)	t_{PWL}	0.93	0.82
Pulse Width Low (SN)	t_{PWL}	0.93	0.96
Input Setup Time (D0 to CK)	t_{SU}	0.33	0.44
Input Hold Time (D0 to CK)	t_{HD}	0.60	0.63
Input Setup Time (D1 to CK)	t_{SU}	0.33	0.44
Input Hold Time (D1 to CK)	t_{HD}	0.60	0.63
Input Setup Time (D2 to CK)	t_{SU}	0.33	0.44
Input Hold Time (D2 to CK)	t_{HD}	0.60	0.63
Input Setup Time (D3 to CK)	t_{SU}	0.33	0.44
Input Hold Time (D3 to CK)	t_{HD}	0.60	0.63
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.93	1.04
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.76	0.93

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD4X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.85	0.79 + 0.032*SL	0.80 + 0.026*SL	0.82 + 0.024*SL
	t_{PHL}	1.17	1.09 + 0.041*SL	1.10 + 0.038*SL	1.10 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.25	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q0	t_{PLH}	0.34	0.27 + 0.032*SL	0.29 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.37	0.29 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
SN to Q0	t_{PLH}	0.65	0.59 + 0.031*SL	0.60 + 0.026*SL	0.63 + 0.023*SL
	t_R	0.23	0.14 + 0.047*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
CK to Q1	t_{PLH}	0.85	0.79 + 0.032*SL	0.80 + 0.026*SL	0.82 + 0.024*SL
	t_{PHL}	1.17	1.09 + 0.041*SL	1.10 + 0.038*SL	1.10 + 0.037*SL
	t_R	0.23	0.14 + 0.046*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.25	0.12 + 0.060*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q1	t_{PLH}	0.34	0.27 + 0.032*SL	0.29 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.37	0.29 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
SN to Q1	t_{PLH}	0.65	0.59 + 0.032*SL	0.60 + 0.026*SL	0.63 + 0.023*SL
	t_R	0.23	0.14 + 0.047*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
CK to Q2	t_{PLH}	0.85	0.79 + 0.031*SL	0.80 + 0.026*SL	0.83 + 0.024*SL
	t_{PHL}	1.17	1.09 + 0.041*SL	1.10 + 0.038*SL	1.10 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.25	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q2	t_{PLH}	0.34	0.27 + 0.032*SL	0.29 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.37	0.29 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
SN to Q2	t_{PLH}	0.65	0.59 + 0.031*SL	0.60 + 0.026*SL	0.63 + 0.023*SL
	t_R	0.23	0.14 + 0.047*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
CK to Q3	t_{PLH}	0.85	0.79 + 0.031*SL	0.80 + 0.026*SL	0.82 + 0.024*SL
	t_{PHL}	1.17	1.09 + 0.041*SL	1.09 + 0.038*SL	1.10 + 0.037*SL
	t_R	0.23	0.14 + 0.046*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q3	t_{PLH}	0.33	0.27 + 0.032*SL	0.28 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.23	0.14 + 0.046*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.061*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to Q3	t_{PLH}	0.65	0.59 + 0.031*SL	0.60 + 0.026*SL	0.62 + 0.023*SL
	t_R	0.23	0.14 + 0.046*SL	0.13 + 0.048*SL	0.10 + 0.052*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD4X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN0	t_{PLH}	1.29	1.23 + 0.030*SL	1.24 + 0.025*SL	1.25 + 0.024*SL
	t_{PHL}	1.07	1.00 + 0.038*SL	1.00 + 0.037*SL	1.00 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.066*SL	0.07 + 0.069*SL
RN to QN0	t_{PLH}	0.49	0.43 + 0.030*SL	0.44 + 0.025*SL	0.46 + 0.023*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
SN to QN0	t_{PLH}	0.33	0.27 + 0.031*SL	0.28 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.28 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.065*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to QN1	t_{PLH}	1.29	1.23 + 0.030*SL	1.24 + 0.025*SL	1.25 + 0.024*SL
	t_{PHL}	1.07	1.00 + 0.038*SL	1.00 + 0.037*SL	1.00 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.12 + 0.060*SL	0.11 + 0.066*SL	0.07 + 0.069*SL
RN to QN1	t_{PLH}	0.49	0.43 + 0.030*SL	0.44 + 0.025*SL	0.46 + 0.023*SL
	t_R	0.22	0.12 + 0.047*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
SN to QN1	t_{PLH}	0.33	0.27 + 0.032*SL	0.28 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.28 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.065*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to QN2	t_{PLH}	1.29	1.23 + 0.030*SL	1.24 + 0.025*SL	1.25 + 0.024*SL
	t_{PHL}	1.07	1.00 + 0.037*SL	1.00 + 0.037*SL	1.00 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.061*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to QN2	t_{PLH}	0.49	0.43 + 0.030*SL	0.44 + 0.025*SL	0.46 + 0.023*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
SN to QN2	t_{PLH}	0.33	0.27 + 0.031*SL	0.28 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.28 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.065*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to QN3	t_{PLH}	1.28	1.22 + 0.030*SL	1.23 + 0.025*SL	1.24 + 0.024*SL
	t_{PHL}	1.07	0.99 + 0.038*SL	0.99 + 0.037*SL	0.99 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to QN3	t_{PLH}	0.48	0.42 + 0.030*SL	0.43 + 0.025*SL	0.45 + 0.023*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
SN to QN3	t_{PLH}	0.33	0.26 + 0.031*SL	0.28 + 0.025*SL	0.29 + 0.024*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD4X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.17	1.08 + 0.044*SL	1.10 + 0.037*SL	1.12 + 0.035*SL
	t_{PHL}	1.65	1.55 + 0.052*SL	1.56 + 0.047*SL	1.58 + 0.045*SL
	t_R	0.32	0.18 + 0.069*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.16 + 0.077*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q0	t_{PLH}	0.45	0.36 + 0.043*SL	0.38 + 0.036*SL	0.40 + 0.034*SL
	t_{PHL}	0.48	0.37 + 0.051*SL	0.39 + 0.046*SL	0.40 + 0.045*SL
	t_R	0.31	0.17 + 0.069*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.13 + 0.081*SL	0.13 + 0.082*SL
SN to Q0	t_{PLH}	0.93	0.84 + 0.044*SL	0.87 + 0.037*SL	0.89 + 0.034*SL
	t_R	0.32	0.19 + 0.067*SL	0.19 + 0.067*SL	0.17 + 0.069*SL
CK to Q1	t_{PLH}	1.17	1.08 + 0.044*SL	1.10 + 0.037*SL	1.12 + 0.035*SL
	t_{PHL}	1.65	1.55 + 0.052*SL	1.57 + 0.046*SL	1.58 + 0.045*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.32	0.16 + 0.078*SL	0.16 + 0.079*SL	0.14 + 0.081*SL
RN to Q1	t_{PLH}	0.45	0.36 + 0.043*SL	0.38 + 0.036*SL	0.40 + 0.034*SL
	t_{PHL}	0.48	0.37 + 0.051*SL	0.39 + 0.046*SL	0.40 + 0.045*SL
	t_R	0.31	0.17 + 0.070*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.13 + 0.081*SL	0.13 + 0.082*SL
SN to Q1	t_{PLH}	0.93	0.84 + 0.044*SL	0.87 + 0.037*SL	0.89 + 0.034*SL
	t_R	0.32	0.19 + 0.067*SL	0.19 + 0.067*SL	0.17 + 0.069*SL
CK to Q2	t_{PLH}	1.17	1.08 + 0.044*SL	1.10 + 0.037*SL	1.12 + 0.035*SL
	t_{PHL}	1.65	1.55 + 0.052*SL	1.57 + 0.046*SL	1.58 + 0.045*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.16 + 0.077*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q2	t_{PLH}	0.45	0.36 + 0.043*SL	0.38 + 0.036*SL	0.40 + 0.034*SL
	t_{PHL}	0.48	0.37 + 0.051*SL	0.39 + 0.046*SL	0.40 + 0.045*SL
	t_R	0.31	0.17 + 0.070*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.13 + 0.081*SL	0.13 + 0.082*SL
SN to Q2	t_{PLH}	0.93	0.84 + 0.044*SL	0.87 + 0.037*SL	0.89 + 0.034*SL
	t_R	0.32	0.19 + 0.067*SL	0.19 + 0.067*SL	0.17 + 0.069*SL
CK to Q3	t_{PLH}	1.17	1.08 + 0.043*SL	1.10 + 0.037*SL	1.12 + 0.035*SL
	t_{PHL}	1.65	1.54 + 0.052*SL	1.56 + 0.046*SL	1.57 + 0.045*SL
	t_R	0.32	0.18 + 0.069*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.16 + 0.078*SL	0.16 + 0.079*SL	0.14 + 0.081*SL
RN to Q3	t_{PLH}	0.44	0.35 + 0.043*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.047*SL	0.39 + 0.045*SL
	t_R	0.30	0.17 + 0.068*SL	0.16 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.082*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
SN to Q3	t_{PLH}	0.93	0.84 + 0.043*SL	0.86 + 0.037*SL	0.88 + 0.034*SL
	t_R	0.32	0.19 + 0.067*SL	0.18 + 0.067*SL	0.17 + 0.069*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

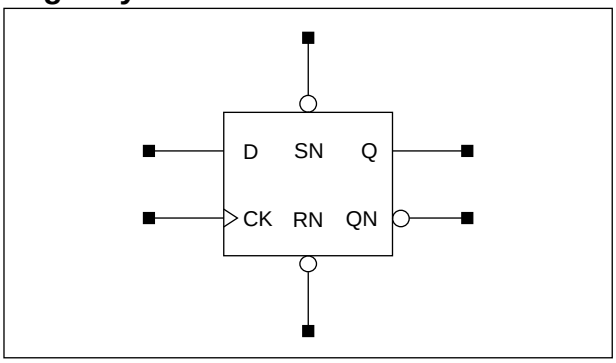
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD4X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN0	t_{PLH}	1.85	1.76 + 0.042*SL	1.78 + 0.036*SL	1.80 + 0.034*SL
	t_{PHL}	1.49	1.39 + 0.048*SL	1.40 + 0.045*SL	1.41 + 0.044*SL
	t_R	0.31	0.17 + 0.068*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.31	0.15 + 0.078*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to QN0	t_{PLH}	0.68	0.60 + 0.042*SL	0.61 + 0.036*SL	0.63 + 0.034*SL
	t_R	0.30	0.17 + 0.067*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
SN to QN0	t_{PLH}	0.44	0.36 + 0.042*SL	0.38 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.046*SL	0.39 + 0.045*SL
	t_R	0.30	0.16 + 0.069*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL
CK to QN1	t_{PLH}	1.85	1.76 + 0.042*SL	1.78 + 0.036*SL	1.80 + 0.034*SL
	t_{PHL}	1.49	1.39 + 0.048*SL	1.40 + 0.045*SL	1.41 + 0.044*SL
	t_R	0.31	0.17 + 0.069*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.31	0.15 + 0.078*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to QN1	t_{PLH}	0.68	0.60 + 0.042*SL	0.61 + 0.036*SL	0.63 + 0.034*SL
	t_R	0.30	0.17 + 0.068*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
SN to QN1	t_{PLH}	0.44	0.36 + 0.042*SL	0.38 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.046*SL	0.39 + 0.045*SL
	t_R	0.30	0.16 + 0.069*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL
CK to QN2	t_{PLH}	1.85	1.76 + 0.042*SL	1.78 + 0.036*SL	1.80 + 0.034*SL
	t_{PHL}	1.49	1.39 + 0.048*SL	1.40 + 0.045*SL	1.41 + 0.044*SL
	t_R	0.31	0.17 + 0.068*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.31	0.15 + 0.078*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to QN2	t_{PLH}	0.68	0.59 + 0.042*SL	0.61 + 0.036*SL	0.63 + 0.034*SL
	t_R	0.30	0.17 + 0.068*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
SN to QN2	t_{PLH}	0.44	0.36 + 0.042*SL	0.38 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.046*SL	0.39 + 0.045*SL
	t_R	0.30	0.16 + 0.069*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL
CK to QN3	t_{PLH}	1.84	1.75 + 0.042*SL	1.77 + 0.036*SL	1.79 + 0.034*SL
	t_{PHL}	1.48	1.38 + 0.048*SL	1.39 + 0.045*SL	1.40 + 0.044*SL
	t_R	0.30	0.17 + 0.068*SL	0.16 + 0.069*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to QN3	t_{PLH}	0.67	0.58 + 0.042*SL	0.60 + 0.036*SL	0.62 + 0.034*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
SN to QN3	t_{PLH}	0.44	0.35 + 0.042*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.46	0.36 + 0.051*SL	0.38 + 0.046*SL	0.38 + 0.045*SL
	t_R	0.30	0.16 + 0.069*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Logic Symbol



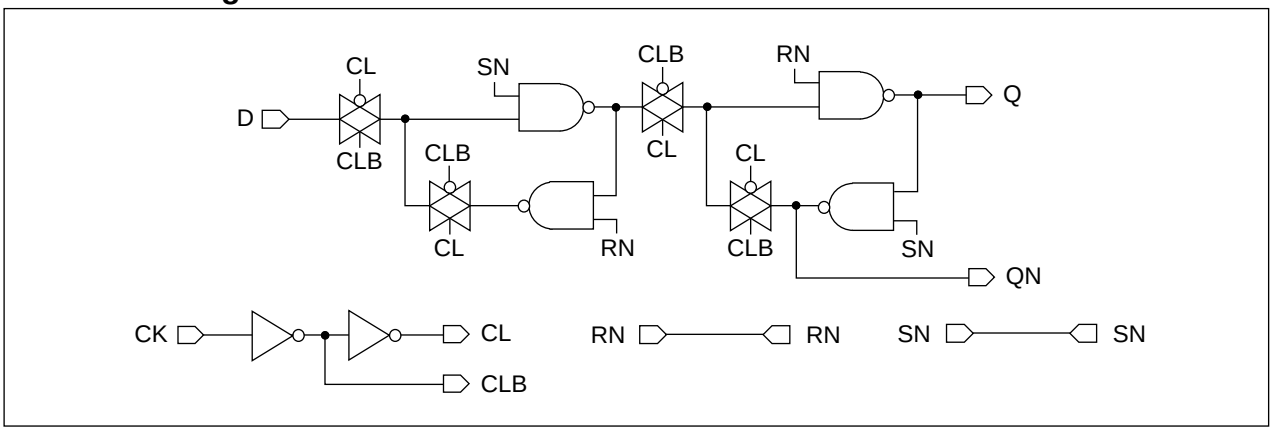
Truth Table

D	CK	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	1
x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
STD80									
YFD4				*YFD4D2*				*YFD4*	*YFD4D2*
D	CK	RN	SN	D	CK	RN	SN		
1.8	0.5	1.2	1.3	1.7	0.5	2.0	2.4	6.3	7.7
STDM80									
YFD4				*YFD4D2*				*YFD4*	*YFD4D2*
D	CK	RN	SN	D	CK	RN	SN		
2.0	0.6	1.7	2.0	2.0	0.6	2.8	3.1	6.3	7.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		YFD4	YFD4D2	YFD4	YFD4D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.87	0.87
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.85	1.01
Pulse Width Low (RN)	t_{PWL}	0.87	0.93	1.01	1.20
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.41	0.41	0.49	0.49
Input Hold Time (D to CK)	t_{HD}	0.46	0.49	0.49	0.49
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.38	0.38	0.44	0.44
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.66	0.66	0.76	0.71

YFD4/YFD4D2

Fast D Flip-Flop with Reset, Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 YFD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.57	0.51 + 0.030*SL	0.52 + 0.027*SL	0.54 + 0.025*SL
	t_{PHL}	0.58	0.50 + 0.041*SL	0.50 + 0.039*SL	0.51 + 0.039*SL
	t_R	0.33	0.23 + 0.050*SL	0.23 + 0.050*SL	0.20 + 0.054*SL
	t_F	0.39	0.25 + 0.069*SL	0.24 + 0.074*SL	0.20 + 0.078*SL
RN to Q	t_{PHL}	0.60	0.52 + 0.041*SL	0.52 + 0.039*SL	0.52 + 0.038*SL
	t_F	0.41	0.28 + 0.065*SL	0.26 + 0.072*SL	0.20 + 0.078*SL
SN to Q	t_{PLH}	0.19	0.13 + 0.031*SL	0.14 + 0.025*SL	0.26 + 0.013*SL
	t_{PHL}	0.24	0.16 + 0.041*SL	0.17 + 0.038*SL	0.16 + 0.038*SL
	t_R	0.33	0.24 + 0.041*SL	0.26 + 0.035*SL	0.35 + 0.025*SL
	t_F	0.39	0.26 + 0.065*SL	0.24 + 0.072*SL	0.19 + 0.078*SL
CK to QN	t_{PLH}	0.76	0.59 + 0.082*SL	0.60 + 0.080*SL	0.60 + 0.080*SL
	t_{PHL}	0.76	0.61 + 0.073*SL	0.62 + 0.070*SL	0.64 + 0.068*SL
	t_R	0.30	0.16 + 0.070*SL	0.16 + 0.069*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.082*SL	0.14 + 0.082*SL
RN to QN	t_{PLH}	0.17	0.11 + 0.034*SL	0.12 + 0.026*SL	0.14 + 0.024*SL
	t_{PHL}	0.22	0.14 + 0.042*SL	0.15 + 0.038*SL	0.14 + 0.038*SL
	t_R	0.30	0.21 + 0.043*SL	0.21 + 0.045*SL	0.21 + 0.045*SL
	t_F	0.35	0.22 + 0.065*SL	0.20 + 0.071*SL	0.14 + 0.078*SL
SN to QN	t_{PHL}	0.38	0.23 + 0.074*SL	0.25 + 0.067*SL	0.37 + 0.054*SL
	t_F	0.30	0.14 + 0.079*SL	0.14 + 0.080*SL	0.15 + 0.079*SL

STD80 YFD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.60	0.56 + 0.018*SL	0.56 + 0.016*SL	0.60 + 0.013*SL
	t_{PHL}	0.66	0.61 + 0.025*SL	0.62 + 0.022*SL	0.65 + 0.019*SL
	t_R	0.31	0.27 + 0.020*SL	0.26 + 0.025*SL	0.24 + 0.027*SL
	t_F	0.40	0.34 + 0.032*SL	0.33 + 0.035*SL	0.30 + 0.038*SL
RN to Q	t_{PHL}	0.68	0.63 + 0.023*SL	0.64 + 0.021*SL	0.66 + 0.019*SL
	t_F	0.40	0.34 + 0.032*SL	0.33 + 0.033*SL	0.29 + 0.038*SL
SN to Q	t_{PLH}	0.18	0.14 + 0.016*SL	0.15 + 0.013*SL	0.20 + 0.008*SL
	t_{PHL}	0.18	0.14 + 0.022*SL	0.14 + 0.020*SL	0.15 + 0.019*SL
	t_R	0.31	0.27 + 0.018*SL	0.26 + 0.022*SL	0.35 + 0.013*SL
	t_F	0.31	0.25 + 0.034*SL	0.24 + 0.036*SL	0.21 + 0.039*SL
CK to QN	t_{PLH}	0.79	0.70 + 0.046*SL	0.71 + 0.043*SL	0.73 + 0.040*SL
	t_{PHL}	0.73	0.65 + 0.041*SL	0.66 + 0.037*SL	0.69 + 0.034*SL
	t_R	0.23	0.16 + 0.033*SL	0.16 + 0.034*SL	0.15 + 0.035*SL
	t_F	0.20	0.13 + 0.038*SL	0.12 + 0.041*SL	0.12 + 0.041*SL
RN to QN	t_{PLH}	0.13	0.09 + 0.020*SL	0.10 + 0.015*SL	0.13 + 0.012*SL
	t_{PHL}	0.17	0.12 + 0.023*SL	0.13 + 0.020*SL	0.13 + 0.019*SL
	t_R	0.24	0.20 + 0.023*SL	0.20 + 0.022*SL	0.19 + 0.023*SL
	t_F	0.26	0.20 + 0.032*SL	0.19 + 0.034*SL	0.14 + 0.039*SL
SN to QN	t_{PHL}	0.31	0.23 + 0.038*SL	0.24 + 0.035*SL	0.30 + 0.028*SL
	t_F	0.20	0.12 + 0.038*SL	0.12 + 0.040*SL	0.13 + 0.039*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 YFD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.73 + 0.042*SL	0.74 + 0.038*SL	0.76 + 0.036*SL
	t_{PHL}	0.83	0.72 + 0.056*SL	0.73 + 0.052*SL	0.74 + 0.051*SL
	t_R	0.45	0.31 + 0.071*SL	0.30 + 0.072*SL	0.29 + 0.073*SL
	t_F	0.51	0.33 + 0.092*SL	0.32 + 0.094*SL	0.31 + 0.097*SL
RN to Q	t_{PHL}	0.85	0.73 + 0.057*SL	0.75 + 0.053*SL	0.76 + 0.050*SL
	t_F	0.55	0.38 + 0.086*SL	0.36 + 0.091*SL	0.33 + 0.095*SL
SN to Q	t_{PLH}	0.25	0.17 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.30	0.20 + 0.050*SL	0.20 + 0.050*SL	0.19 + 0.050*SL
	t_R	0.38	0.24 + 0.067*SL	0.24 + 0.066*SL	0.41 + 0.043*SL
	t_F	0.45	0.27 + 0.093*SL	0.26 + 0.096*SL	0.24 + 0.098*SL
CK to QN	t_{PLH}	1.09	0.86 + 0.115*SL	0.87 + 0.112*SL	0.88 + 0.111*SL
	t_{PHL}	1.09	0.88 + 0.101*SL	0.90 + 0.097*SL	0.91 + 0.095*SL
	t_R	0.40	0.22 + 0.093*SL	0.22 + 0.093*SL	0.21 + 0.094*SL
	t_F	0.40	0.20 + 0.103*SL	0.19 + 0.106*SL	0.19 + 0.105*SL
RN to QN	t_{PLH}	0.23	0.15 + 0.038*SL	0.16 + 0.035*SL	0.16 + 0.035*SL
	t_{PHL}	0.28	0.18 + 0.050*SL	0.18 + 0.049*SL	0.17 + 0.050*SL
	t_R	0.34	0.21 + 0.066*SL	0.19 + 0.071*SL	0.20 + 0.070*SL
	t_F	0.40	0.22 + 0.091*SL	0.21 + 0.095*SL	0.19 + 0.098*SL
SN to QN	t_{PHL}	0.51	0.32 + 0.095*SL	0.32 + 0.093*SL	0.35 + 0.090*SL
	t_F	0.39	0.18 + 0.104*SL	0.18 + 0.104*SL	0.21 + 0.101*SL

STDM80 YFD4D2

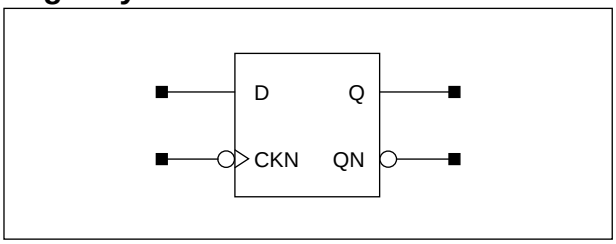
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.85	0.80 + 0.025*SL	0.81 + 0.023*SL	0.83 + 0.021*SL
	t_{PHL}	0.98	0.91 + 0.035*SL	0.92 + 0.032*SL	0.94 + 0.029*SL
	t_R	0.40	0.33 + 0.036*SL	0.33 + 0.036*SL	0.33 + 0.036*SL
	t_F	0.54	0.45 + 0.045*SL	0.45 + 0.047*SL	0.45 + 0.047*SL
RN to Q	t_{PHL}	0.98	0.91 + 0.034*SL	0.92 + 0.031*SL	0.94 + 0.028*SL
	t_F	0.55	0.46 + 0.045*SL	0.47 + 0.044*SL	0.47 + 0.044*SL
SN to Q	t_{PLH}	0.22	0.18 + 0.019*SL	0.19 + 0.017*SL	0.19 + 0.017*SL
	t_{PHL}	0.24	0.18 + 0.028*SL	0.18 + 0.027*SL	0.19 + 0.026*SL
	t_R	0.33	0.27 + 0.030*SL	0.26 + 0.034*SL	0.25 + 0.035*SL
	t_F	0.36	0.26 + 0.049*SL	0.26 + 0.050*SL	0.26 + 0.050*SL
CK to QN	t_{PLH}	1.18	1.05 + 0.066*SL	1.06 + 0.062*SL	1.08 + 0.059*SL
	t_{PHL}	1.04	0.93 + 0.055*SL	0.94 + 0.052*SL	0.96 + 0.050*SL
	t_R	0.30	0.21 + 0.045*SL	0.21 + 0.046*SL	0.21 + 0.046*SL
	t_F	0.27	0.16 + 0.053*SL	0.16 + 0.052*SL	0.16 + 0.052*SL
RN to QN	t_{PLH}	0.17	0.13 + 0.023*SL	0.14 + 0.019*SL	0.15 + 0.017*SL
	t_{PHL}	0.21	0.15 + 0.028*SL	0.16 + 0.025*SL	0.16 + 0.025*SL
	t_R	0.25	0.20 + 0.029*SL	0.19 + 0.033*SL	0.17 + 0.035*SL
	t_F	0.28	0.19 + 0.044*SL	0.19 + 0.046*SL	0.18 + 0.047*SL
SN to QN	t_{PHL}	0.41	0.31 + 0.049*SL	0.31 + 0.047*SL	0.32 + 0.047*SL
	t_F	0.26	0.15 + 0.053*SL	0.15 + 0.052*SL	0.15 + 0.053*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

FD5/FD5D2

D Flip-Flop with Negative Edge Trigger, 1X/2X Drive

Logic Symbol



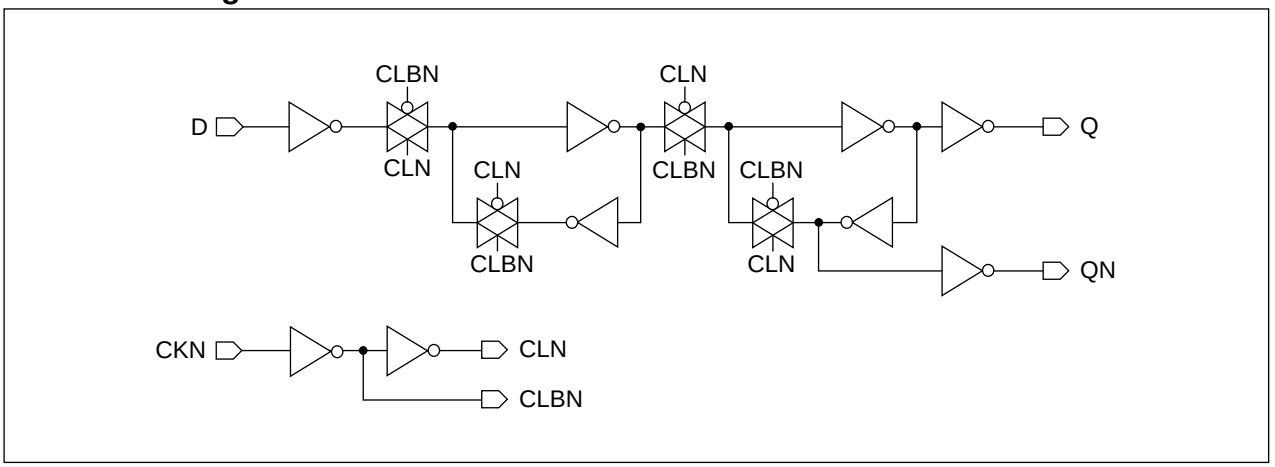
Truth Table

D	CKN	Q (n+1)	QN (n+1)
0	↓	0	1
1	↓	1	0
x	↑	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
STD80					
FD5		*FD5D2*		*FD5*	*FD5D2*
D	CKN	D	CKN		
0.5	0.5	0.5	0.5	5.3	6.0
STDM80					
FD5		*FD5D2*		*FD5*	*FD5D2*
D	CKN	D	CKN		
0.6	0.6	0.6	0.6	5.3	6.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD5	FD5D2	FD5	FD5D2
Pulse Width Low (CKN)	t_{PWL}	0.87	0.87	0.85	0.85
Pulse Width High (CKN)	t_{PWH}	0.79	0.79	0.79	0.79
Input Setup Time (D to CKN)	t_{SU}	0.41	0.41	0.41	0.41
Input Hold Time (D to CKN)	t_{HD}	0.44	0.44	0.55	0.55

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.73	0.68 + 0.028*SL	0.68 + 0.024*SL	0.69 + 0.024*SL
	t_{PHL}	0.68	0.60 + 0.041*SL	0.61 + 0.038*SL	0.62 + 0.037*SL
	t_R	0.20	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CKN to QN	t_{PLH}	0.72	0.67 + 0.025*SL	0.68 + 0.024*SL	0.67 + 0.024*SL
	t_{PHL}	0.90	0.82 + 0.038*SL	0.83 + 0.037*SL	0.82 + 0.037*SL
	t_R	0.18	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.06 + 0.069*SL

STD80 FD5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.74	0.70 + 0.018*SL	0.71 + 0.014*SL	0.73 + 0.012*SL
	t_{PHL}	0.67	0.63 + 0.023*SL	0.64 + 0.020*SL	0.65 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
CKN to QN	t_{PLH}	0.79	0.76 + 0.013*SL	0.76 + 0.012*SL	0.77 + 0.012*SL
	t_{PHL}	0.96	0.92 + 0.018*SL	0.92 + 0.018*SL	0.92 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

FD5/FD5D2

D Flip-Flop with Negative Edge Trigger, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD5

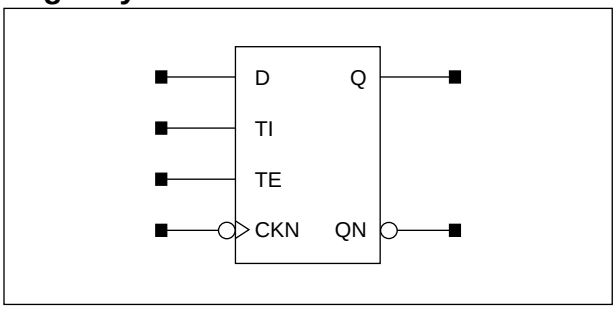
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.04	0.96 + 0.038*SL	0.97 + 0.035*SL	0.98 + 0.034*SL
	t_{PHL}	0.94	0.83 + 0.052*SL	0.85 + 0.046*SL	0.86 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
CKN to QN	t_{PLH}	1.01	0.94 + 0.035*SL	0.94 + 0.033*SL	0.94 + 0.033*SL
	t_{PHL}	1.27	1.17 + 0.047*SL	1.18 + 0.045*SL	1.18 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL

STDM80 FD5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.04	1.00 + 0.024*SL	1.01 + 0.020*SL	1.02 + 0.018*SL
	t_{PHL}	0.92	0.86 + 0.030*SL	0.88 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.13 + 0.042*SL	0.15 + 0.038*SL	0.14 + 0.039*SL
CKN to QN	t_{PLH}	1.10	1.06 + 0.019*SL	1.06 + 0.017*SL	1.07 + 0.017*SL
	t_{PHL}	1.34	1.29 + 0.026*SL	1.30 + 0.023*SL	1.31 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



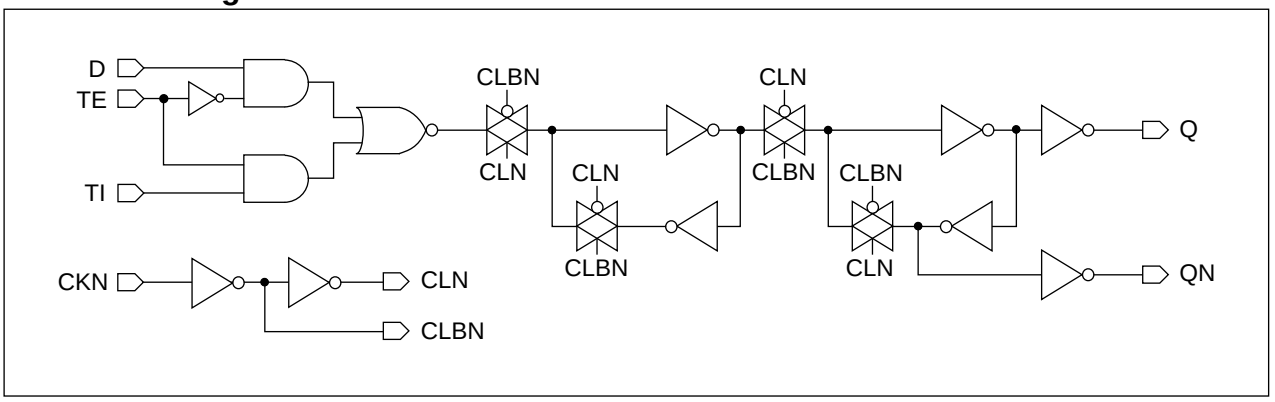
Truth Table

D	TI	TE	CKN	Q (n+1)	QN (n+1)
0	x	0	↓	0	1
1	x	0	↓	1	0
x	0	1	↓	0	1
x	1	1	↓	1	0
x	x	x	↑	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
STD80									
FD5S				*FD5SD2*				*FD5S*	*FD5SD2*
D	TI	TE	CKN	D	TI	TE	CKN		
0.3	0.5	0.9	0.5	0.3	0.5	0.9	0.5	7.0	7.7
STDM80									
FD5S				*FD5SD2*				*FD5S*	*FD5SD2*
D	TI	TE	CKN	D	TI	TE	CKN		
0.6	0.4	1.1	0.6	0.6	0.4	1.1	0.6	7.0	7.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD5S	FD5SD2	FD5S	FD5SD2
Pulse Width Low (CKN)	t_{PWL}	0.87	0.87	0.96	0.98
Pulse Width High (CKN)	t_{PWH}	0.79	0.79	0.82	0.82
Input Setup Time (D to CKN)	t_{SU}	0.52	0.52	0.71	0.71
Input Hold Time (D to CKN)	t_{HD}	0.38	0.38	0.41	0.41
Input Setup Time (TI to CKN)	t_{SU}	0.52	0.52	0.76	0.76
Input Hold Time (TI to CKN)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TE to CKN)	t_{SU}	0.55	0.71	0.74	0.74
Input Hold Time (TE to CKN)	t_{HD}	0.33	0.33	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD5S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.74	0.69 + 0.028*SL	0.69 + 0.024*SL	0.70 + 0.024*SL
	t_{PHL}	0.70	0.61 + 0.042*SL	0.62 + 0.038*SL	0.63 + 0.037*SL
	t_R	0.20	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CKN to QN	t_{PLH}	0.73	0.68 + 0.025*SL	0.69 + 0.024*SL	0.69 + 0.024*SL
	t_{PHL}	0.91	0.84 + 0.037*SL	0.84 + 0.037*SL	0.84 + 0.037*SL
	t_R	0.18	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL

STD80 FD5SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.75	0.71 + 0.018*SL	0.72 + 0.013*SL	0.74 + 0.012*SL
	t_{PHL}	0.69	0.64 + 0.023*SL	0.65 + 0.020*SL	0.66 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.029*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
CKN to QN	t_{PLH}	0.80	0.77 + 0.014*SL	0.78 + 0.012*SL	0.78 + 0.012*SL
	t_{PHL}	0.97	0.93 + 0.018*SL	0.93 + 0.018*SL	0.93 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD5S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.06	0.98 + 0.038*SL	0.99 + 0.035*SL	1.00 + 0.034*SL
	t_{PHL}	0.95	0.85 + 0.052*SL	0.87 + 0.046*SL	0.88 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
CKN to QN	t_{PLH}	1.02	0.96 + 0.035*SL	0.96 + 0.033*SL	0.96 + 0.033*SL
	t_{PHL}	1.29	1.19 + 0.047*SL	1.20 + 0.045*SL	1.20 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL

STDM80 FD5SD2

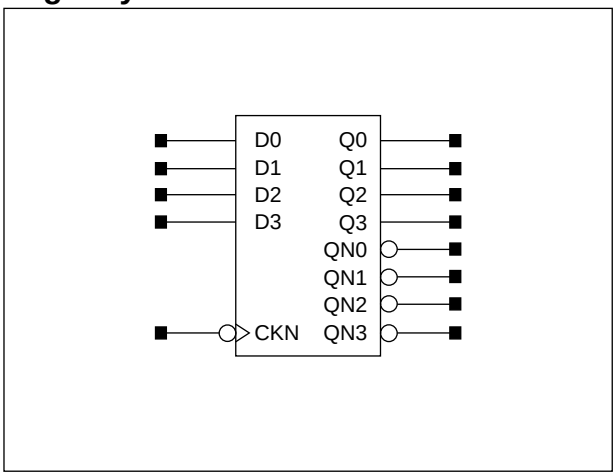
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.06	1.01 + 0.024*SL	1.03 + 0.020*SL	1.04 + 0.018*SL
	t_{PHL}	0.94	0.88 + 0.030*SL	0.90 + 0.026*SL	0.91 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
CKN to QN	t_{PLH}	1.11	1.08 + 0.018*SL	1.08 + 0.017*SL	1.09 + 0.017*SL
	t_{PHL}	1.36	1.31 + 0.025*SL	1.32 + 0.023*SL	1.33 + 0.022*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

FD5X4

4-Bit D Flip-Flop with Negative Edge Trigger

Logic Symbol



Truth Table

Dn	CKN	Qn (n+1)	QNn (n+1)
0	↓	0	1
1	↓	1	0
x	↑	Qn (n)	QNn (n)

Cell Data

Input Load (SL)		Gate Count
STD80		
Dn	CKN	
0.5	0.5	18.3
STDM80		
Dn	CKN	
0.6	0.6	18.3

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CKN)	t_{PWL}	0.90	1.50
Pulse Width High (CKN)	t_{PWH}	1.01	1.42
Input Setup Time (D0 to CKN)	t_{SU}	0.33	0.33
Input Hold Time (D0 to CKN)	t_{HD}	0.68	1.04
Input Setup Time (D1 to CKN)	t_{SU}	0.33	0.33
Input Hold Time (D1 to CKN)	t_{HD}	0.68	1.04
Input Setup Time (D2 to CKN)	t_{SU}	0.33	0.33
Input Hold Time (D2 to CKN)	t_{HD}	0.68	1.04
Input Setup Time (D3 to CKN)	t_{SU}	0.33	0.33
Input Hold Time (D3 to CKN)	t_{HD}	0.68	1.04

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q0	t_{PLH}	1.20	1.15 + 0.028*SL	1.15 + 0.024*SL	1.16 + 0.024*SL
	t_{PHL}	0.95	0.87 + 0.041*SL	0.88 + 0.038*SL	0.88 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CKN to Q1	t_{PLH}	1.20	1.15 + 0.028*SL	1.15 + 0.024*SL	1.16 + 0.024*SL
	t_{PHL}	0.95	0.87 + 0.041*SL	0.88 + 0.038*SL	0.88 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CKN to Q2	t_{PLH}	1.20	1.15 + 0.028*SL	1.15 + 0.024*SL	1.16 + 0.024*SL
	t_{PHL}	0.95	0.87 + 0.041*SL	0.88 + 0.038*SL	0.88 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CKN to Q3	t_{PLH}	1.20	1.15 + 0.028*SL	1.15 + 0.024*SL	1.16 + 0.024*SL
	t_{PHL}	0.95	0.87 + 0.042*SL	0.88 + 0.038*SL	0.88 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.12 + 0.061*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
CKN to QN0	t_{PLH}	0.96	0.91 + 0.025*SL	0.92 + 0.024*SL	0.92 + 0.024*SL
	t_{PHL}	1.37	1.30 + 0.038*SL	1.30 + 0.037*SL	1.30 + 0.037*SL
	t_R	0.19	0.10 + 0.045*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
CKN to QN1	t_{PLH}	0.96	0.91 + 0.025*SL	0.92 + 0.024*SL	0.92 + 0.024*SL
	t_{PHL}	1.37	1.30 + 0.038*SL	1.30 + 0.037*SL	1.30 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
CKN to QN2	t_{PLH}	0.96	0.91 + 0.025*SL	0.92 + 0.024*SL	0.92 + 0.024*SL
	t_{PHL}	1.37	1.30 + 0.038*SL	1.30 + 0.037*SL	1.30 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
CKN to QN3	t_{PLH}	0.96	0.91 + 0.025*SL	0.91 + 0.023*SL	0.91 + 0.024*SL
	t_{PHL}	1.37	1.30 + 0.038*SL	1.30 + 0.037*SL	1.30 + 0.037*SL
	t_R	0.18	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.06 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

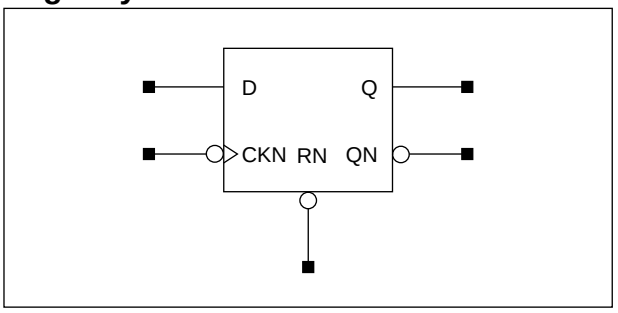
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q0	t_{PLH}	1.75	1.67 + 0.039*SL	1.68 + 0.035*SL	1.69 + 0.034*SL
	t_{PHL}	1.34	1.23 + 0.052*SL	1.25 + 0.046*SL	1.26 + 0.044*SL
	t_R	0.29	0.15 + 0.067*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
CKN to Q1	t_{PLH}	1.75	1.67 + 0.039*SL	1.68 + 0.035*SL	1.69 + 0.034*SL
	t_{PHL}	1.34	1.23 + 0.052*SL	1.25 + 0.046*SL	1.26 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
CKN to Q2	t_{PLH}	1.75	1.67 + 0.039*SL	1.68 + 0.035*SL	1.69 + 0.034*SL
	t_{PHL}	1.34	1.23 + 0.052*SL	1.25 + 0.046*SL	1.26 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
CKN to Q3	t_{PLH}	1.75	1.67 + 0.038*SL	1.68 + 0.035*SL	1.69 + 0.034*SL
	t_{PHL}	1.34	1.23 + 0.052*SL	1.25 + 0.046*SL	1.26 + 0.044*SL
	t_R	0.29	0.15 + 0.067*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
CKN to QN0	t_{PLH}	1.38	1.31 + 0.035*SL	1.32 + 0.033*SL	1.32 + 0.033*SL
	t_{PHL}	1.98	1.88 + 0.046*SL	1.89 + 0.045*SL	1.89 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.083*SL
CKN to QN1	t_{PLH}	1.38	1.31 + 0.035*SL	1.32 + 0.033*SL	1.32 + 0.033*SL
	t_{PHL}	1.98	1.88 + 0.046*SL	1.89 + 0.045*SL	1.89 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.083*SL
CKN to QN2	t_{PLH}	1.38	1.31 + 0.035*SL	1.32 + 0.033*SL	1.32 + 0.033*SL
	t_{PHL}	1.98	1.88 + 0.046*SL	1.89 + 0.045*SL	1.89 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.083*SL
CKN to QN3	t_{PLH}	1.38	1.31 + 0.035*SL	1.32 + 0.033*SL	1.31 + 0.033*SL
	t_{PHL}	1.97	1.88 + 0.047*SL	1.89 + 0.045*SL	1.89 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



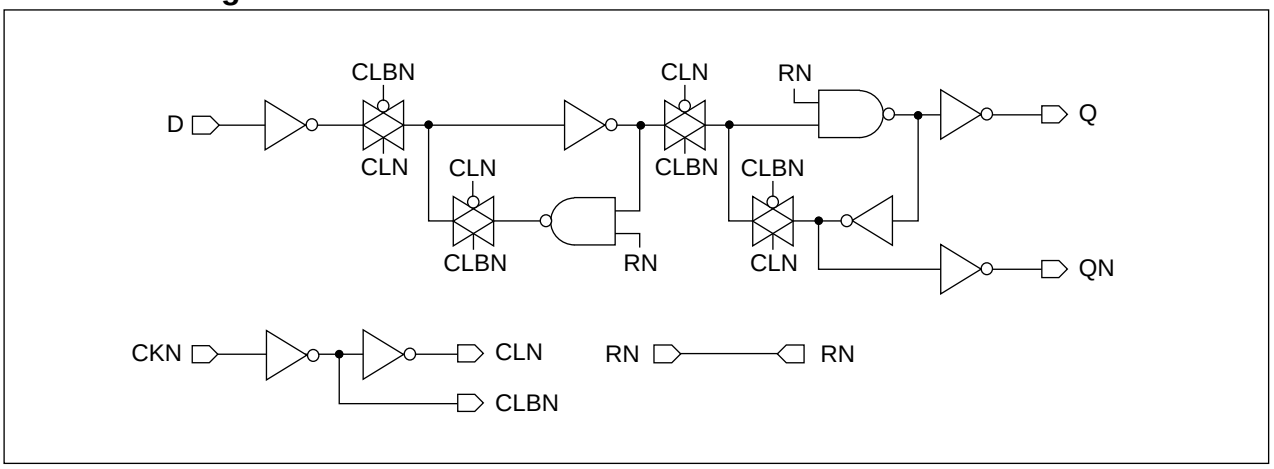
Truth Table

D	CKN	RN	Q (n+1)	QN (n+1)
0	↓	1	0	1
1	↓	1	1	0
x	x	0	0	1
x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
STD80							
FD6			*FD6D2*			*FD6*	*FD6D2*
D	CKN	RN	D	CKN	RN		
0.5	0.5	0.9	0.5	0.5	0.9	6.3	7.0
STDM80							
FD6			*FD6D2*			*FD6*	*FD6D2*
D	CKN	RN	D	CKN	RN		
0.6	0.6	1.2	0.6	0.6	1.2	6.3	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD6	FD6D2	FD6	FD6D2
Pulse Width Low (CKN)	t_{PWL}	0.87	0.87	0.96	0.98
Pulse Width High (CKN)	t_{PWH}	0.79	0.79	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Input Setup Time (D to CKN)	t_{SU}	0.49	0.49	0.52	0.52
Input Hold Time (D to CKN)	t_{HD}	0.52	0.52	0.52	0.52
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CKN)	t_{HD}	0.82	0.82	0.93	0.93

FD6/FD6D2

D Flip-Flop with Negative Edge Trigger, Reset, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.79	0.73 + 0.031*SL	0.74 + 0.026*SL	0.77 + 0.024*SL
	t_{PHL}	0.71	0.63 + 0.042*SL	0.64 + 0.038*SL	0.64 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PHL}	0.37	0.28 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CKN to QN	t_{PLH}	0.75	0.70 + 0.026*SL	0.70 + 0.024*SL	0.70 + 0.024*SL
	t_{PHL}	0.97	0.90 + 0.036*SL	0.90 + 0.037*SL	0.90 + 0.037*SL
	t_R	0.18	0.09 + 0.045*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.41	0.35 + 0.026*SL	0.36 + 0.023*SL	0.36 + 0.024*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.049*SL	0.06 + 0.052*SL

STD80 FD6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.81	0.77 + 0.021*SL	0.78 + 0.015*SL	0.81 + 0.012*SL
	t_{PHL}	0.70	0.65 + 0.023*SL	0.66 + 0.020*SL	0.68 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.18	0.12 + 0.030*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
RN to Q	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.020*SL	0.33 + 0.018*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
CKN to QN	t_{PLH}	0.82	0.79 + 0.014*SL	0.79 + 0.012*SL	0.80 + 0.012*SL
	t_{PHL}	1.05	1.02 + 0.017*SL	1.02 + 0.017*SL	1.01 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
RN to QN	t_{PLH}	0.47	0.44 + 0.014*SL	0.45 + 0.012*SL	0.45 + 0.012*SL
	t_R	0.15	0.11 + 0.019*SL	0.10 + 0.023*SL	0.07 + 0.026*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.14	1.05 + 0.044*SL	1.07 + 0.038*SL	1.09 + 0.035*SL
	t_{PHL}	0.98	0.87 + 0.052*SL	0.89 + 0.046*SL	0.90 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
RN to Q	t_{PHL}	0.47	0.37 + 0.052*SL	0.38 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.14 + 0.081*SL
CKN to QN	t_{PLH}	1.05	0.98 + 0.035*SL	0.99 + 0.033*SL	0.99 + 0.033*SL
	t_{PHL}	1.37	1.28 + 0.047*SL	1.29 + 0.044*SL	1.29 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.078*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
RN to QN	t_{PLH}	0.55	0.48 + 0.035*SL	0.48 + 0.033*SL	0.48 + 0.033*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL

STDM80 FD6D2

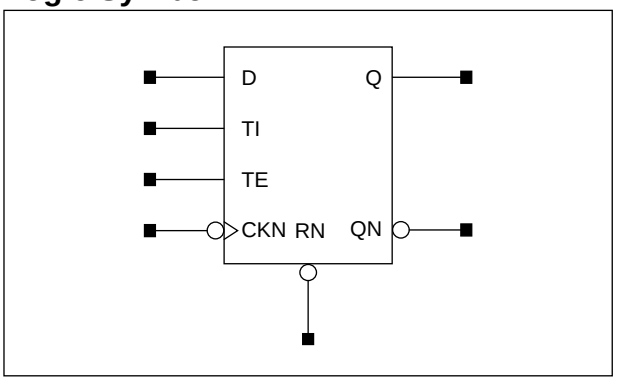
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.15	1.09 + 0.028*SL	1.11 + 0.023*SL	1.13 + 0.019*SL
	t_{PHL}	0.97	0.90 + 0.031*SL	0.92 + 0.026*SL	0.94 + 0.023*SL
	t_R	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
RN to Q	t_{PHL}	0.46	0.40 + 0.031*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_F	0.22	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
CKN to QN	t_{PLH}	1.14	1.10 + 0.019*SL	1.11 + 0.017*SL	1.11 + 0.017*SL
	t_{PHL}	1.48	1.44 + 0.024*SL	1.44 + 0.022*SL	1.45 + 0.021*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
RN to QN	t_{PLH}	0.63	0.60 + 0.019*SL	0.60 + 0.017*SL	0.61 + 0.017*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

FD6S/FD6SD2

D Flip-Flop with Negative Edge Trigger, Reset, Scan, 1X/2X Drive

Logic Symbol



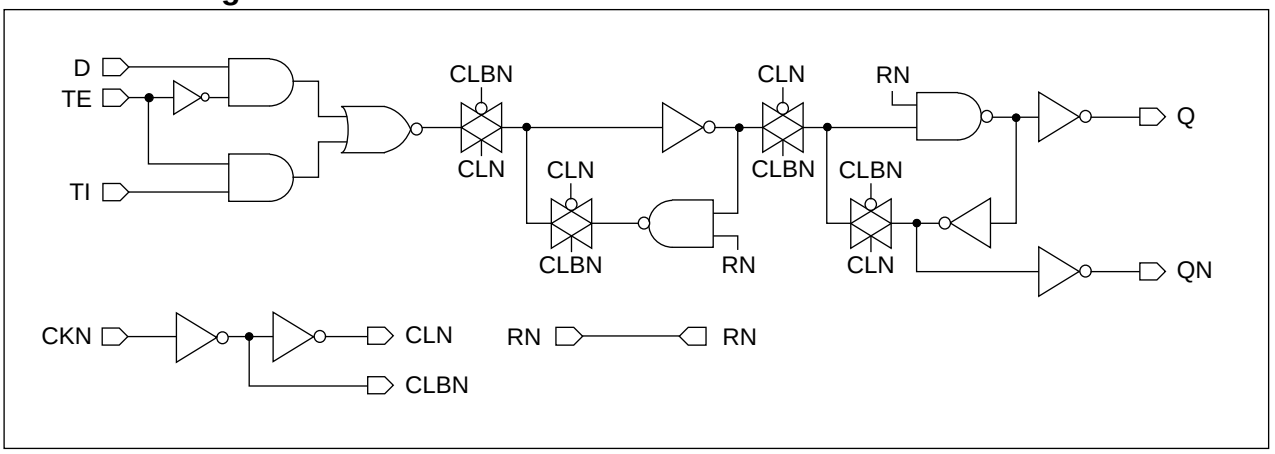
Truth Table

D	TI	TE	CKN	RN	Q (n+1)	QN (n+1)
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	0	1
x	x	x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
STD80											
FD6S					*FD6SD2*					*FD6S*	*FD6SD2*
D	TI	TE	CKN	RN	D	TI	TE	CKN	RN		
0.3	0.5	0.9	0.5	0.9	0.3	0.5	0.9	0.5	0.9	8.0	8.7
STDM80											
FD6S					*FD6SD2*					*FD6S*	*FD6SD2*
D	TI	TE	CKN	RN	D	TI	TE	CKN	RN		
0.6	0.4	1.1	0.6	1.2	0.6	0.4	1.1	0.6	1.2	8.0	8.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD6S	FD6SD2	FD6S	FD6SD2
Pulse Width Low (CKN)	t_{PWL}	0.87	0.87	0.98	1.01
Pulse Width High (CKN)	t_{PWH}	0.79	0.79	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Input Setup Time (D to CKN)	t_{SU}	0.71	0.71	0.74	0.74
Input Hold Time (D to CKN)	t_{HD}	0.44	0.44	0.41	0.41
Input Setup Time (TI to CKN)	t_{SU}	0.79	0.79	0.79	0.79
Input Hold Time (TI to CKN)	t_{HD}	0.36	0.36	0.33	0.33
Input Setup Time (TE to CKN)	t_{SU}	0.74	0.74	0.74	0.74
Input Hold Time (TE to CKN)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CKN)	t_{HD}	0.82	0.82	0.93	0.93

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD6S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.80	0.74 + 0.032*SL	0.75 + 0.026*SL	0.77 + 0.024*SL
	t_{PHL}	0.72	0.64 + 0.042*SL	0.65 + 0.038*SL	0.65 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PHL}	0.37	0.28 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CKN to QN	t_{PLH}	0.76	0.71 + 0.026*SL	0.72 + 0.024*SL	0.71 + 0.024*SL
	t_{PHL}	0.98	0.91 + 0.037*SL	0.91 + 0.037*SL	0.90 + 0.037*SL
	t_R	0.18	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.41	0.35 + 0.026*SL	0.36 + 0.023*SL	0.36 + 0.024*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.050*SL	0.06 + 0.052*SL

STD80 FD6SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.82	0.77 + 0.021*SL	0.79 + 0.015*SL	0.82 + 0.012*SL
	t_{PHL}	0.71	0.67 + 0.023*SL	0.67 + 0.020*SL	0.69 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.18	0.12 + 0.030*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
RN to Q	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.020*SL	0.33 + 0.018*SL
	t_F	0.18	0.11 + 0.033*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
CKN to QN	t_{PLH}	0.83	0.80 + 0.014*SL	0.80 + 0.012*SL	0.81 + 0.012*SL
	t_{PHL}	1.06	1.03 + 0.018*SL	1.03 + 0.017*SL	1.02 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
RN to QN	t_{PLH}	0.47	0.44 + 0.014*SL	0.45 + 0.012*SL	0.45 + 0.012*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD6S

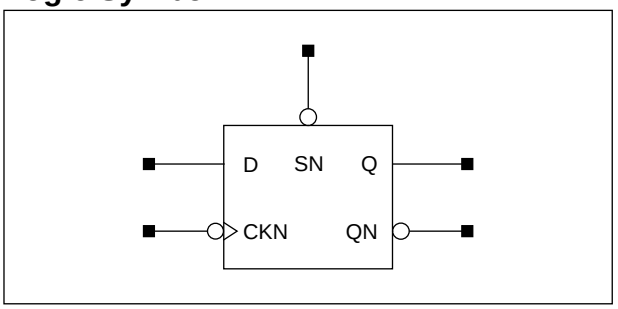
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.15	1.06 + 0.044*SL	1.08 + 0.038*SL	1.10 + 0.034*SL
	t_{PHL}	0.99	0.89 + 0.052*SL	0.91 + 0.046*SL	0.92 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
RN to Q	t_{PHL}	0.47	0.37 + 0.052*SL	0.38 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
CKN to QN	t_{PLH}	1.07	1.00 + 0.035*SL	1.00 + 0.033*SL	1.00 + 0.033*SL
	t_{PHL}	1.38	1.29 + 0.047*SL	1.30 + 0.045*SL	1.30 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.078*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
RN to QN	t_{PLH}	0.55	0.48 + 0.035*SL	0.48 + 0.033*SL	0.48 + 0.033*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL

STDM80 FD6SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.16	1.11 + 0.028*SL	1.12 + 0.023*SL	1.14 + 0.019*SL
	t_{PHL}	0.98	0.92 + 0.031*SL	0.94 + 0.026*SL	0.96 + 0.023*SL
	t_R	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
RN to Q	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_F	0.22	0.13 + 0.042*SL	0.14 + 0.039*SL	0.15 + 0.038*SL
CKN to QN	t_{PLH}	1.16	1.12 + 0.019*SL	1.12 + 0.017*SL	1.13 + 0.017*SL
	t_{PHL}	1.50	1.45 + 0.024*SL	1.45 + 0.022*SL	1.46 + 0.021*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.037*SL	0.14 + 0.038*SL
RN to QN	t_{PLH}	0.63	0.60 + 0.019*SL	0.60 + 0.017*SL	0.61 + 0.017*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



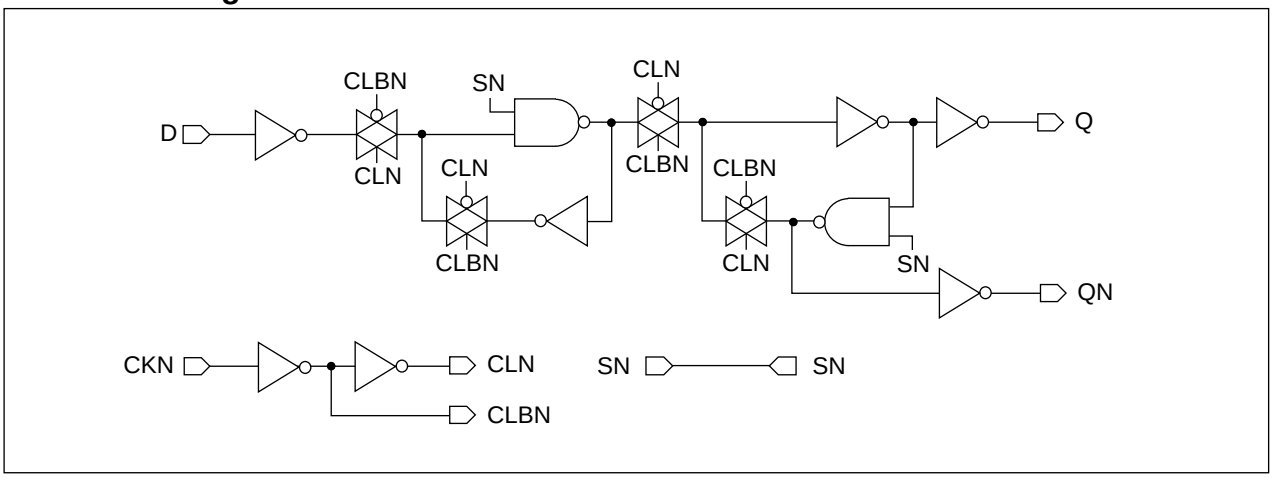
Truth Table

D	CKN	SN	Q (n+1)	QN (n+1)
0	↓	1	0	1
1	↓	1	1	0
x	x	0	1	0
x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
STD80							
FD7			*FD7D2*			*FD7*	*FD7D2*
D	CKN	SN	D	CKN	SN		
0.5	0.5	0.7	0.5	0.5	0.7	6.7	7.3
STDM80							
FD7			*FD7D2*			*FD7*	*FD7D2*
D	CKN	SN	D	CKN	SN		
0.6	0.6	1.1	0.6	0.6	1.1	6.7	7.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD7	FD7D2	FD7	FD7D2
Pulse Width Low (CKN)	t_{PWL}	0.87	0.87	0.96	0.96
Pulse Width High (CKN)	t_{PWH}	0.79	0.79	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.96	0.96
Input Setup Time (D to CKN)	t_{SU}	0.55	0.55	0.57	0.57
Input Hold Time (D to CKN)	t_{HD}	0.52	0.52	0.52	0.52
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CKN)	t_{HD}	0.49	0.49	0.55	0.55

FD7/FD7D2

D Flip-Flop with Negative Edge Trigger, Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.74	0.68 + 0.028*SL	0.69 + 0.024*SL	0.70 + 0.024*SL
	t_{PHL}	0.73	0.64 + 0.041*SL	0.65 + 0.038*SL	0.66 + 0.037*SL
	t_R	0.20	0.12 + 0.044*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to Q	t_{PLH}	0.61	0.55 + 0.029*SL	0.56 + 0.024*SL	0.56 + 0.024*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.048*SL	0.07 + 0.052*SL
CKN to QN	t_{PLH}	0.83	0.77 + 0.030*SL	0.78 + 0.025*SL	0.80 + 0.024*SL
	t_{PHL}	0.94	0.87 + 0.038*SL	0.87 + 0.037*SL	0.87 + 0.037*SL
	t_R	0.21	0.12 + 0.046*SL	0.12 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
SN to QN	t_{PHL}	0.35	0.27 + 0.040*SL	0.27 + 0.038*SL	0.28 + 0.037*SL
	t_F	0.23	0.10 + 0.064*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

STD80 FD7D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.75	0.71 + 0.018*SL	0.72 + 0.014*SL	0.74 + 0.012*SL
	t_{PHL}	0.72	0.67 + 0.023*SL	0.68 + 0.020*SL	0.69 + 0.018*SL
	t_R	0.16	0.12 + 0.022*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to Q	t_{PLH}	0.61	0.58 + 0.018*SL	0.59 + 0.013*SL	0.60 + 0.012*SL
	t_R	0.17	0.12 + 0.022*SL	0.12 + 0.022*SL	0.09 + 0.026*SL
CKN to QN	t_{PLH}	0.90	0.87 + 0.018*SL	0.88 + 0.014*SL	0.90 + 0.012*SL
	t_{PHL}	1.00	0.96 + 0.019*SL	0.96 + 0.018*SL	0.96 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.033*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to QN	t_{PHL}	0.35	0.30 + 0.023*SL	0.31 + 0.019*SL	0.32 + 0.018*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.06	0.98 + 0.038*SL	0.99 + 0.035*SL	1.00 + 0.034*SL
	t_{PHL}	1.00	0.90 + 0.051*SL	0.91 + 0.046*SL	0.92 + 0.045*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.082*SL
SN to Q	t_{PLH}	0.87	0.79 + 0.039*SL	0.81 + 0.034*SL	0.81 + 0.033*SL
	t_R	0.29	0.16 + 0.063*SL	0.15 + 0.068*SL	0.13 + 0.071*SL
CKN to QN	t_{PLH}	1.18	1.09 + 0.041*SL	1.11 + 0.036*SL	1.13 + 0.034*SL
	t_{PHL}	1.34	1.25 + 0.048*SL	1.26 + 0.045*SL	1.26 + 0.044*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.29	0.14 + 0.080*SL	0.13 + 0.080*SL	0.12 + 0.082*SL
SN to QN	t_{PHL}	0.45	0.35 + 0.051*SL	0.37 + 0.046*SL	0.37 + 0.045*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

STDM80 FD7D2

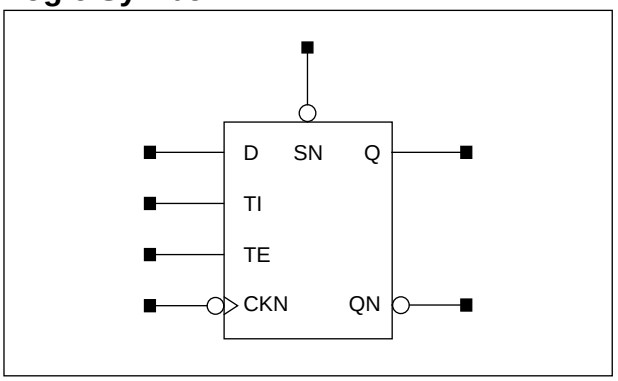
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.06	1.01 + 0.024*SL	1.03 + 0.020*SL	1.04 + 0.018*SL
	t_{PHL}	0.99	0.93 + 0.031*SL	0.94 + 0.026*SL	0.96 + 0.023*SL
	t_R	0.21	0.15 + 0.032*SL	0.15 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.14 + 0.038*SL
SN to Q	t_{PLH}	0.87	0.83 + 0.024*SL	0.84 + 0.020*SL	0.86 + 0.017*SL
	t_R	0.22	0.15 + 0.032*SL	0.15 + 0.032*SL	0.14 + 0.033*SL
CKN to QN	t_{PLH}	1.27	1.23 + 0.024*SL	1.24 + 0.021*SL	1.25 + 0.019*SL
	t_{PHL}	1.42	1.36 + 0.027*SL	1.37 + 0.024*SL	1.39 + 0.022*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.14 + 0.038*SL	0.14 + 0.038*SL
SN to QN	t_{PHL}	0.45	0.39 + 0.030*SL	0.40 + 0.025*SL	0.42 + 0.023*SL
	t_F	0.21	0.12 + 0.042*SL	0.13 + 0.039*SL	0.13 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

FD7S/FD7SD2

D Flip-Flop with Negative Edge Trigger, Set, Scan, 1X/2X Drive

Logic Symbol



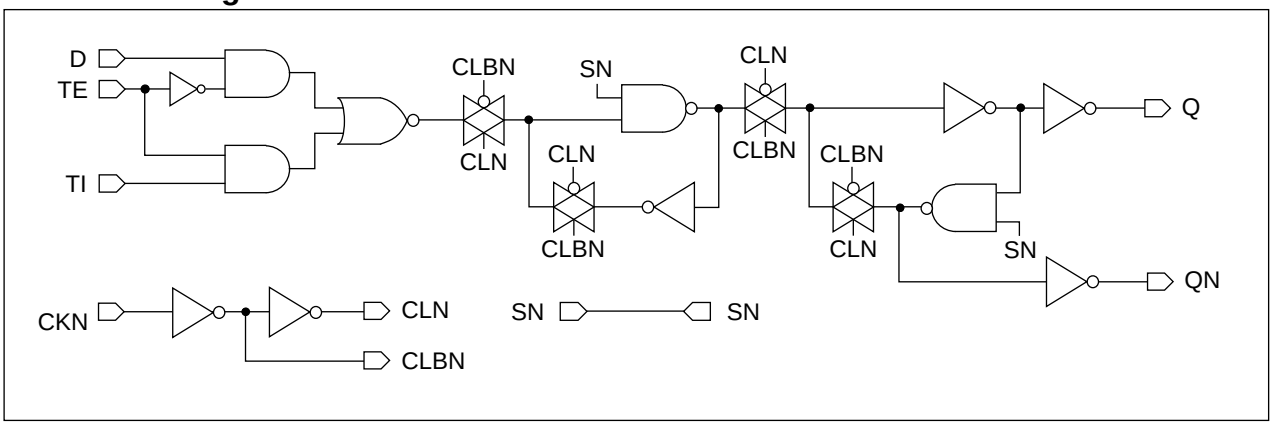
Truth Table

D	TI	TE	CKN	SN	Q (n+1)	QN (n+1)
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	1	0
x	x	x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
STD80											
FD7S					*FD7SD2*					*FD7S*	*FD7SD2*
D	TI	TE	CKN	SN	D	TI	TE	CKN	SN		
0.3	0.5	0.9	0.5	0.7	0.3	0.5	0.9	0.5	0.7	8.3	9.0
STDM80											
FD7S					*FD7SD2*					*FD7S*	*FD7SD2*
D	TI	TE	CKN	SN	D	TI	TE	CKN	SN		
0.6	0.4	1.1	0.6	1.1	0.6	0.4	1.1	0.6	1.1	8.3	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD7S	FD7SD2	FD7S	FD7SD2
Pulse Width Low (CKN)	t_{PWL}	0.87	0.87	0.96	0.98
Pulse Width High (CKN)	t_{PWH}	0.79	0.79	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.96	0.96
Input Setup Time (D to CKN)	t_{SU}	0.79	0.79	0.79	0.79
Input Hold Time (D to CKN)	t_{HD}	0.44	0.44	0.41	0.41
Input Setup Time (TI to CKN)	t_{SU}	0.85	0.85	0.85	0.85
Input Hold Time (TI to CKN)	t_{HD}	0.36	0.36	0.33	0.33
Input Setup Time (TE to CKN)	t_{SU}	0.79	0.79	0.82	0.82
Input Hold Time (TE to CKN)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CKN)	t_{HD}	0.55	0.55	0.60	0.60

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD7S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.75	0.69 + 0.028*SL	0.70 + 0.024*SL	0.71 + 0.024*SL
	t_{PHL}	0.74	0.65 + 0.041*SL	0.66 + 0.038*SL	0.67 + 0.037*SL
	t_R	0.20	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to Q	t_{PLH}	0.61	0.55 + 0.029*SL	0.56 + 0.024*SL	0.56 + 0.023*SL
	t_R	0.21	0.12 + 0.043*SL	0.11 + 0.048*SL	0.07 + 0.052*SL
CKN to QN	t_{PLH}	0.84	0.79 + 0.029*SL	0.80 + 0.025*SL	0.81 + 0.024*SL
	t_{PHL}	0.95	0.88 + 0.038*SL	0.88 + 0.037*SL	0.88 + 0.037*SL
	t_R	0.21	0.12 + 0.046*SL	0.12 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
SN to QN	t_{PHL}	0.35	0.27 + 0.040*SL	0.27 + 0.038*SL	0.28 + 0.037*SL
	t_F	0.23	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL

STD80 FD7SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.75	0.72 + 0.018*SL	0.73 + 0.014*SL	0.74 + 0.012*SL
	t_{PHL}	0.73	0.68 + 0.023*SL	0.69 + 0.020*SL	0.71 + 0.018*SL
	t_R	0.16	0.12 + 0.022*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
SN to Q	t_{PLH}	0.61	0.58 + 0.018*SL	0.59 + 0.013*SL	0.60 + 0.012*SL
	t_R	0.17	0.12 + 0.022*SL	0.12 + 0.022*SL	0.09 + 0.026*SL
CKN to QN	t_{PLH}	0.91	0.88 + 0.018*SL	0.89 + 0.014*SL	0.91 + 0.012*SL
	t_{PHL}	1.01	0.97 + 0.020*SL	0.97 + 0.018*SL	0.97 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to QN	t_{PHL}	0.35	0.30 + 0.023*SL	0.31 + 0.019*SL	0.32 + 0.018*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

FD7S/FD7SD2

D Flip-Flop with Negative Edge Trigger, Set, Scan, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD7S

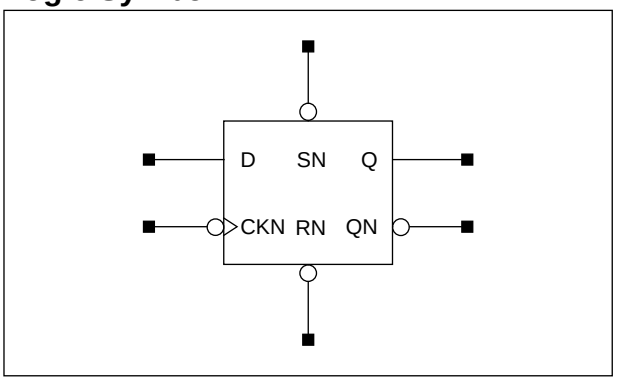
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.07	0.99 + 0.038*SL	1.01 + 0.035*SL	1.01 + 0.034*SL
	t_{PHL}	1.02	0.91 + 0.052*SL	0.93 + 0.046*SL	0.94 + 0.045*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.082*SL
SN to Q	t_{PLH}	0.87	0.79 + 0.039*SL	0.81 + 0.034*SL	0.81 + 0.033*SL
	t_R	0.29	0.16 + 0.064*SL	0.14 + 0.068*SL	0.13 + 0.071*SL
CKN to QN	t_{PLH}	1.19	1.11 + 0.041*SL	1.13 + 0.036*SL	1.14 + 0.034*SL
	t_{PHL}	1.36	1.26 + 0.048*SL	1.27 + 0.045*SL	1.28 + 0.044*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.12 + 0.082*SL
SN to QN	t_{PHL}	0.45	0.35 + 0.051*SL	0.37 + 0.046*SL	0.37 + 0.045*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

STDM80 FD7SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.08	1.03 + 0.024*SL	1.04 + 0.020*SL	1.06 + 0.018*SL
	t_{PHL}	1.01	0.94 + 0.031*SL	0.96 + 0.026*SL	0.98 + 0.023*SL
	t_R	0.21	0.15 + 0.031*SL	0.15 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.14 + 0.039*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
SN to Q	t_{PLH}	0.87	0.83 + 0.024*SL	0.84 + 0.020*SL	0.85 + 0.018*SL
	t_R	0.21	0.15 + 0.033*SL	0.15 + 0.032*SL	0.14 + 0.033*SL
CKN to QN	t_{PLH}	1.29	1.24 + 0.024*SL	1.25 + 0.021*SL	1.27 + 0.019*SL
	t_{PHL}	1.43	1.38 + 0.027*SL	1.39 + 0.024*SL	1.40 + 0.022*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.034*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.14 + 0.038*SL	0.14 + 0.038*SL
SN to QN	t_{PHL}	0.45	0.39 + 0.030*SL	0.40 + 0.025*SL	0.42 + 0.023*SL
	t_F	0.21	0.12 + 0.041*SL	0.13 + 0.039*SL	0.13 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



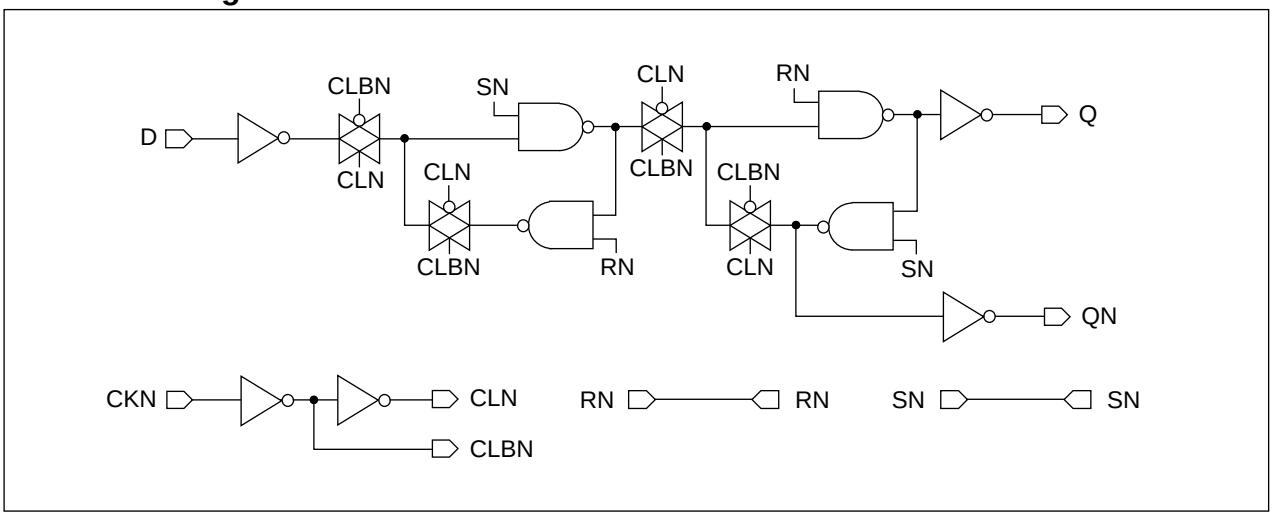
Truth Table

D	CKN	RN	SN	Q (n+1)	QN (n+1)
0	↓	1	1	0	1
1	↓	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↑	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
STD80									
FD8				*FD8D2*				*FD8*	*FD8D2*
D	CKN	RN	SN	D	CKN	RN	SN		
0.5	0.5	0.9	0.7	0.5	0.5	0.9	0.7	7.7	8.3
STDM80									
FD8				*FD8D2*				*FD8*	*FD8D2*
D	CKN	RN	SN	D	CKN	RN	SN		
0.6	0.6	1.6	1.6	0.6	0.6	1.6	1.6	7.7	8.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD8	FD8D2	FD8	FD8D2
Pulse Width Low (CKN)	t_{PWL}	0.87	0.87	0.93	0.98
Pulse Width High (CKN)	t_{PWH}	0.79	0.79	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.96	0.98
Input Setup Time (D to CKN)	t_{SU}	0.60	0.60	0.60	0.60
Input Hold Time (D to CKN)	t_{HD}	0.49	0.49	0.49	0.49
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CKN)	t_{HD}	0.82	0.82	0.93	0.93
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CKN)	t_{HD}	0.49	0.49	0.55	0.55

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.76	0.70 + 0.032*SL	0.71 + 0.026*SL	0.73 + 0.024*SL
	t_{PHL}	0.73	0.65 + 0.041*SL	0.66 + 0.038*SL	0.67 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PLH}	0.33	0.27 + 0.030*SL	0.28 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.23	0.14 + 0.045*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to Q	t_{PLH}	0.66	0.59 + 0.032*SL	0.61 + 0.025*SL	0.62 + 0.024*SL
	t_R	0.23	0.14 + 0.048*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
CKN to QN	t_{PLH}	0.85	0.79 + 0.030*SL	0.80 + 0.025*SL	0.82 + 0.024*SL
	t_{PHL}	0.99	0.91 + 0.038*SL	0.91 + 0.037*SL	0.91 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.48	0.42 + 0.030*SL	0.43 + 0.025*SL	0.45 + 0.024*SL
	t_R	0.22	0.12 + 0.047*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
SN to QN	t_{PLH}	0.33	0.26 + 0.031*SL	0.28 + 0.025*SL	0.29 + 0.024*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.038*SL	0.28 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

STD80 FD8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.78	0.74 + 0.021*SL	0.75 + 0.015*SL	0.78 + 0.012*SL
	t_{PHL}	0.73	0.68 + 0.023*SL	0.69 + 0.020*SL	0.70 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.18	0.12 + 0.029*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
RN to Q	t_{PLH}	0.34	0.31 + 0.019*SL	0.31 + 0.016*SL	0.35 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to Q	t_{PLH}	0.67	0.63 + 0.021*SL	0.64 + 0.015*SL	0.67 + 0.012*SL
	t_R	0.20	0.15 + 0.024*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
CKN to QN	t_{PLH}	0.92	0.89 + 0.018*SL	0.89 + 0.015*SL	0.92 + 0.012*SL
	t_{PHL}	1.07	1.03 + 0.019*SL	1.03 + 0.017*SL	1.03 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.024*SL	0.12 + 0.026*SL
	t_F	0.19	0.12 + 0.032*SL	0.13 + 0.030*SL	0.09 + 0.034*SL
RN to QN	t_{PLH}	0.55	0.51 + 0.018*SL	0.52 + 0.014*SL	0.55 + 0.012*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.020*SL	0.32 + 0.015*SL	0.35 + 0.012*SL
	t_{PHL}	0.35	0.31 + 0.023*SL	0.31 + 0.020*SL	0.33 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

FD8/FD8D2

D Flip-Flop with Negative Edge Trigger, Reset, Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD8

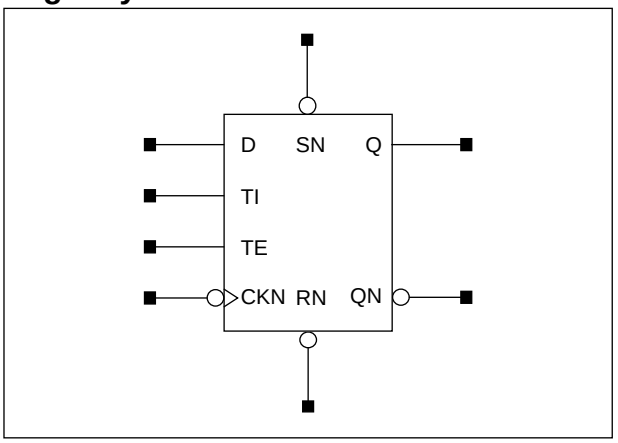
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.09	1.00 + 0.044*SL	1.02 + 0.037*SL	1.04 + 0.035*SL
	t_{PHL}	1.01	0.91 + 0.052*SL	0.92 + 0.047*SL	0.94 + 0.045*SL
	t_R	0.32	0.18 + 0.069*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q	t_{PLH}	0.44	0.35 + 0.043*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.046*SL	0.39 + 0.045*SL
	t_R	0.30	0.17 + 0.068*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
SN to Q	t_{PLH}	0.94	0.85 + 0.044*SL	0.87 + 0.037*SL	0.89 + 0.034*SL
	t_R	0.32	0.18 + 0.067*SL	0.18 + 0.068*SL	0.17 + 0.069*SL
CKN to QN	t_{PLH}	1.21	1.12 + 0.042*SL	1.14 + 0.036*SL	1.15 + 0.034*SL
	t_{PHL}	1.40	1.31 + 0.048*SL	1.32 + 0.045*SL	1.32 + 0.044*SL
	t_R	0.30	0.17 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.15 + 0.078*SL	0.14 + 0.079*SL	0.13 + 0.081*SL
RN to QN	t_{PLH}	0.67	0.59 + 0.042*SL	0.60 + 0.036*SL	0.62 + 0.033*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
SN to QN	t_{PLH}	0.44	0.35 + 0.042*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.46	0.36 + 0.051*SL	0.38 + 0.046*SL	0.38 + 0.045*SL
	t_R	0.30	0.16 + 0.069*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

STDM80 FD8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.11	1.05 + 0.028*SL	1.07 + 0.023*SL	1.09 + 0.019*SL
	t_{PHL}	1.00	0.94 + 0.032*SL	0.96 + 0.026*SL	0.98 + 0.023*SL
	t_R	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.23	0.15 + 0.040*SL	0.16 + 0.038*SL	0.16 + 0.038*SL
RN to Q	t_{PLH}	0.45	0.39 + 0.027*SL	0.41 + 0.022*SL	0.43 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.031*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.039*SL
SN to Q	t_{PLH}	0.96	0.90 + 0.028*SL	0.92 + 0.022*SL	0.94 + 0.019*SL
	t_R	0.25	0.18 + 0.034*SL	0.18 + 0.035*SL	0.19 + 0.033*SL
CKN to QN	t_{PLH}	1.30	1.25 + 0.025*SL	1.26 + 0.021*SL	1.28 + 0.019*SL
	t_{PHL}	1.51	1.46 + 0.026*SL	1.47 + 0.023*SL	1.48 + 0.022*SL
	t_R	0.24	0.17 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.033*SL
	t_F	0.23	0.15 + 0.041*SL	0.16 + 0.038*SL	0.16 + 0.037*SL
RN to QN	t_{PLH}	0.76	0.71 + 0.025*SL	0.72 + 0.021*SL	0.74 + 0.019*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.18 + 0.034*SL
SN to QN	t_{PLH}	0.45	0.40 + 0.027*SL	0.41 + 0.022*SL	0.43 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.13 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Logic Symbol



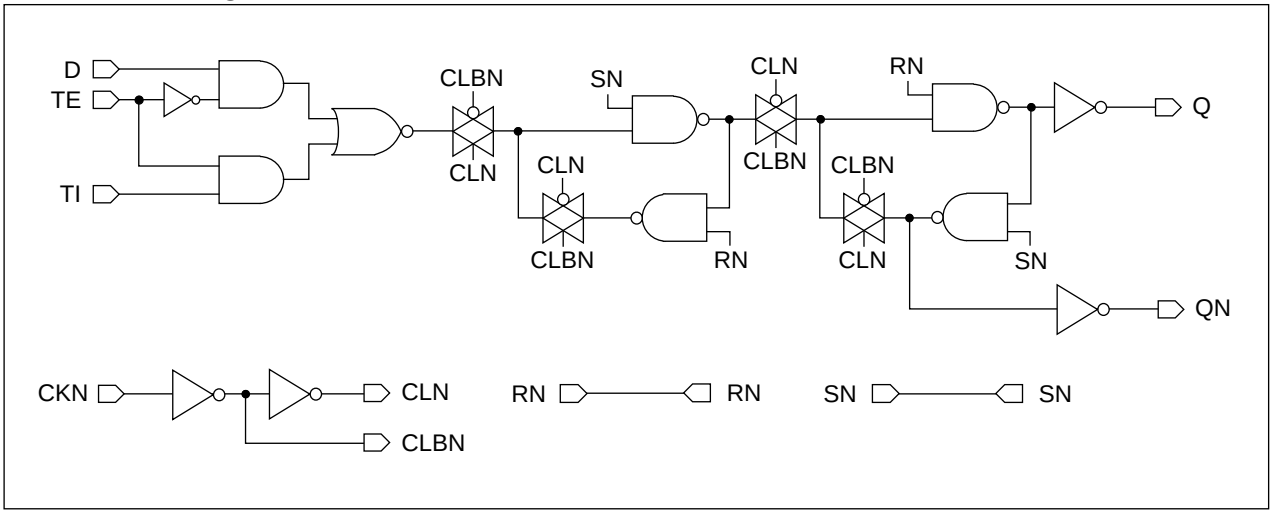
Truth Table

D	TI	TE	CKN	RN	SN	Q (n+1)	QN (n+1)
0	x	0	↓	1	1	0	1
1	x	0	↓	1	1	1	0
x	0	1	↓	1	1	0	1
x	1	1	↓	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	x	x	↑	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)												Gate Count	
STD80													
FD8S						*FD8SD2*						*FD8S*	*FD8SD2*
D	TI	TE	CKN	RN	SN	D	TI	TE	CKN	RN	SN		
0.3	0.5	0.9	0.5	0.7	0.7	0.3	0.5	0.9	0.5	0.7	0.7	9.3	10.0
STDM80													
FD8S						*FD8SD2*						*FD8S*	*FD8SD2*
D	TI	TE	CKN	RN	SN	D	TI	TE	CKN	RN	SN		
0.6	0.4	1.1	0.6	1.6	1.6	0.6	0.4	1.1	0.6	1.6	1.6	9.3	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FD8S	FD8SD2	FD8S	FD8SD2
Pulse Width Low (CKN)	t_{PWL}	0.87	0.87	0.96	0.98
Pulse Width High (CKN)	t_{PWH}	0.82	0.82	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.96	0.98
Input Setup Time (D to CKN)	t_{SU}	0.82	0.82	0.85	0.85
Input Hold Time (D to CKN)	t_{HD}	0.41	0.41	0.38	0.38
Input Setup Time (TI to CKN)	t_{SU}	0.87	0.87	0.90	0.90
Input Hold Time (TI to CKN)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TE to CKN)	t_{SU}	0.85	0.85	0.85	0.85
Input Hold Time (TE to CKN)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CKN)	t_{HD}	0.82	0.82	0.98	0.98
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CKN)	t_{HD}	0.49	0.49	0.55	0.55

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FD8S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.78	0.71 + 0.032*SL	0.72 + 0.026*SL	0.75 + 0.024*SL
	t_{PHL}	0.74	0.66 + 0.041*SL	0.67 + 0.038*SL	0.67 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PLH}	0.33	0.27 + 0.031*SL	0.28 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to Q	t_{PLH}	0.65	0.59 + 0.031*SL	0.60 + 0.026*SL	0.62 + 0.023*SL
	t_R	0.23	0.14 + 0.046*SL	0.13 + 0.048*SL	0.10 + 0.052*SL
CKN to QN	t_{PLH}	0.86	0.80 + 0.030*SL	0.81 + 0.025*SL	0.82 + 0.024*SL
	t_{PHL}	1.00	0.92 + 0.037*SL	0.92 + 0.037*SL	0.92 + 0.037*SL
	t_R	0.22	0.12 + 0.047*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.48	0.42 + 0.030*SL	0.43 + 0.025*SL	0.45 + 0.024*SL
	t_R	0.22	0.12 + 0.046*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
SN to QN	t_{PLH}	0.33	0.26 + 0.031*SL	0.28 + 0.025*SL	0.29 + 0.024*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.061*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

STD80 FD8SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.79	0.75 + 0.021*SL	0.76 + 0.015*SL	0.79 + 0.012*SL
	t_{PHL}	0.74	0.69 + 0.023*SL	0.70 + 0.020*SL	0.71 + 0.018*SL
	t_R	0.20	0.15 + 0.024*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
RN to Q	t_{PLH}	0.34	0.31 + 0.019*SL	0.31 + 0.016*SL	0.35 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to Q	t_{PLH}	0.67	0.63 + 0.021*SL	0.64 + 0.015*SL	0.67 + 0.012*SL
	t_R	0.20	0.15 + 0.025*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
CKN to QN	t_{PLH}	0.93	0.89 + 0.018*SL	0.90 + 0.014*SL	0.93 + 0.012*SL
	t_{PHL}	1.08	1.04 + 0.019*SL	1.04 + 0.017*SL	1.04 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.19	0.12 + 0.032*SL	0.13 + 0.030*SL	0.09 + 0.034*SL
RN to QN	t_{PLH}	0.55	0.51 + 0.018*SL	0.52 + 0.014*SL	0.55 + 0.012*SL
	t_R	0.19	0.15 + 0.022*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.020*SL	0.32 + 0.015*SL	0.35 + 0.012*SL
	t_{PHL}	0.35	0.31 + 0.023*SL	0.31 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

FD8S/FD8SD2

D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FD8S

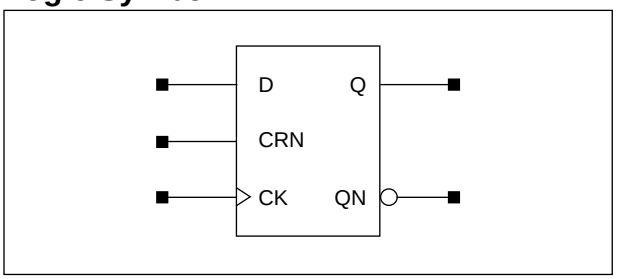
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.11	1.02 + 0.044*SL	1.04 + 0.037*SL	1.06 + 0.035*SL
	t_{PHL}	1.03	0.92 + 0.052*SL	0.94 + 0.046*SL	0.95 + 0.045*SL
	t_R	0.32	0.18 + 0.069*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q	t_{PLH}	0.44	0.35 + 0.043*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.047*SL	0.39 + 0.045*SL
	t_R	0.30	0.17 + 0.068*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
SN to Q	t_{PLH}	0.94	0.85 + 0.043*SL	0.87 + 0.037*SL	0.89 + 0.034*SL
	t_R	0.32	0.18 + 0.067*SL	0.18 + 0.067*SL	0.17 + 0.070*SL
CKN to QN	t_{PLH}	1.22	1.13 + 0.042*SL	1.15 + 0.036*SL	1.17 + 0.034*SL
	t_{PHL}	1.42	1.32 + 0.048*SL	1.33 + 0.045*SL	1.34 + 0.044*SL
	t_R	0.30	0.17 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.30	0.15 + 0.079*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to QN	t_{PLH}	0.67	0.59 + 0.042*SL	0.60 + 0.036*SL	0.62 + 0.034*SL
	t_R	0.30	0.17 + 0.067*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
SN to QN	t_{PLH}	0.44	0.35 + 0.043*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.46	0.36 + 0.051*SL	0.38 + 0.046*SL	0.38 + 0.045*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

STDM80 FD8SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.12	1.07 + 0.028*SL	1.08 + 0.023*SL	1.11 + 0.019*SL
	t_{PHL}	1.02	0.96 + 0.031*SL	0.97 + 0.026*SL	0.99 + 0.023*SL
	t_R	0.25	0.18 + 0.037*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.23	0.15 + 0.041*SL	0.16 + 0.037*SL	0.15 + 0.038*SL
RN to Q	t_{PLH}	0.45	0.39 + 0.027*SL	0.41 + 0.022*SL	0.43 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.16 + 0.037*SL	0.17 + 0.035*SL	0.18 + 0.033*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.038*SL	0.14 + 0.039*SL
SN to Q	t_{PLH}	0.95	0.90 + 0.028*SL	0.91 + 0.023*SL	0.94 + 0.019*SL
	t_R	0.25	0.18 + 0.035*SL	0.19 + 0.034*SL	0.19 + 0.033*SL
CKN to QN	t_{PLH}	1.32	1.26 + 0.025*SL	1.28 + 0.021*SL	1.29 + 0.019*SL
	t_{PHL}	1.53	1.47 + 0.027*SL	1.49 + 0.023*SL	1.50 + 0.021*SL
	t_R	0.24	0.17 + 0.037*SL	0.17 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.23	0.15 + 0.040*SL	0.16 + 0.038*SL	0.16 + 0.037*SL
RN to QN	t_{PLH}	0.76	0.71 + 0.025*SL	0.72 + 0.021*SL	0.73 + 0.019*SL
	t_R	0.24	0.17 + 0.037*SL	0.18 + 0.034*SL	0.18 + 0.034*SL
SN to QN	t_{PLH}	0.45	0.40 + 0.027*SL	0.41 + 0.022*SL	0.44 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.13 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Logic Symbol



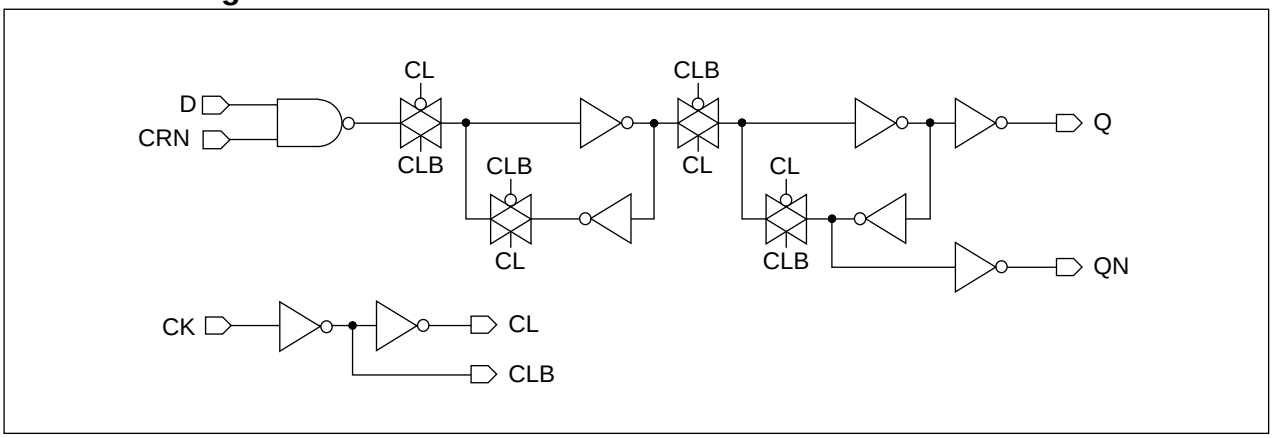
Truth Table

D	CRN	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	0	1
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
STD80							
FDS2			*FDS2D2*			*FDS2*	*FDS2D2*
D	CRN	CK	D	CRN	CK		
0.5	0.5	0.5	0.5	0.5	0.5	6.0	6.7
STDM80							
FDS2			*FDS2D2*			*FDS2*	*FDS2D2*
D	CRN	CK	D	CRN	CK		
0.4	0.5	0.6	0.4	0.5	0.6	6.0	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FDS2	FDS2D2	FDS2	FDS2D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.90	0.90
Pulse Width High (CK)	t_{PWH}	0.79	0.79	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.68	0.68	0.68	0.68
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (CRN to CK)	t_{SU}	0.68	0.68	0.68	0.68
Input Hold Time (CRN to CK)	t_{HD}	0.33	0.33	0.33	0.33

FDS2/FDS2D2

D Flip-Flop with Synchronous Clear, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FDS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.52 + 0.028*SL	0.53 + 0.024*SL	0.53 + 0.024*SL
	t_{PHL}	0.66	0.58 + 0.041*SL	0.59 + 0.038*SL	0.60 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.70	0.65 + 0.025*SL	0.66 + 0.024*SL	0.65 + 0.024*SL
	t_{PHL}	0.74	0.67 + 0.037*SL	0.67 + 0.037*SL	0.67 + 0.037*SL
	t_R	0.19	0.09 + 0.045*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL

STD80 FDS2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.54 + 0.018*SL	0.55 + 0.014*SL	0.57 + 0.012*SL
	t_{PHL}	0.65	0.61 + 0.023*SL	0.61 + 0.020*SL	0.63 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
CK to QN	t_{PLH}	0.77	0.74 + 0.013*SL	0.74 + 0.012*SL	0.75 + 0.012*SL
	t_{PHL}	0.80	0.76 + 0.018*SL	0.76 + 0.018*SL	0.76 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FDS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.75 + 0.038*SL	0.76 + 0.035*SL	0.77 + 0.034*SL
	t_{PHL}	0.94	0.84 + 0.052*SL	0.85 + 0.046*SL	0.86 + 0.045*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
CK to QN	t_{PLH}	1.01	0.94 + 0.034*SL	0.94 + 0.033*SL	0.94 + 0.033*SL
	t_{PHL}	1.05	0.96 + 0.047*SL	0.96 + 0.045*SL	0.97 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL

STDM80 FDS2D2

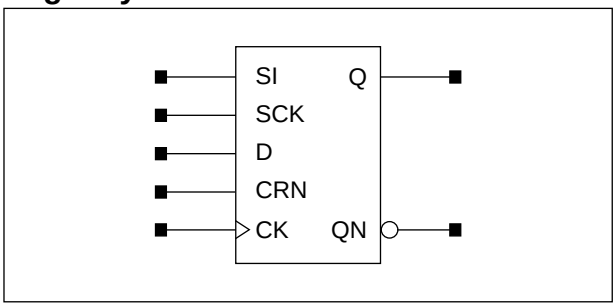
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.78 + 0.024*SL	0.79 + 0.020*SL	0.80 + 0.018*SL
	t_{PHL}	0.92	0.86 + 0.031*SL	0.88 + 0.026*SL	0.90 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
CK to QN	t_{PLH}	1.10	1.06 + 0.019*SL	1.06 + 0.017*SL	1.07 + 0.017*SL
	t_{PHL}	1.12	1.07 + 0.026*SL	1.08 + 0.023*SL	1.09 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

FDS2CS/FDS2CSD2

D Flip-Flop with Synchronous Clear, Scan Clock, 1X/2X Drive

Logic Symbol



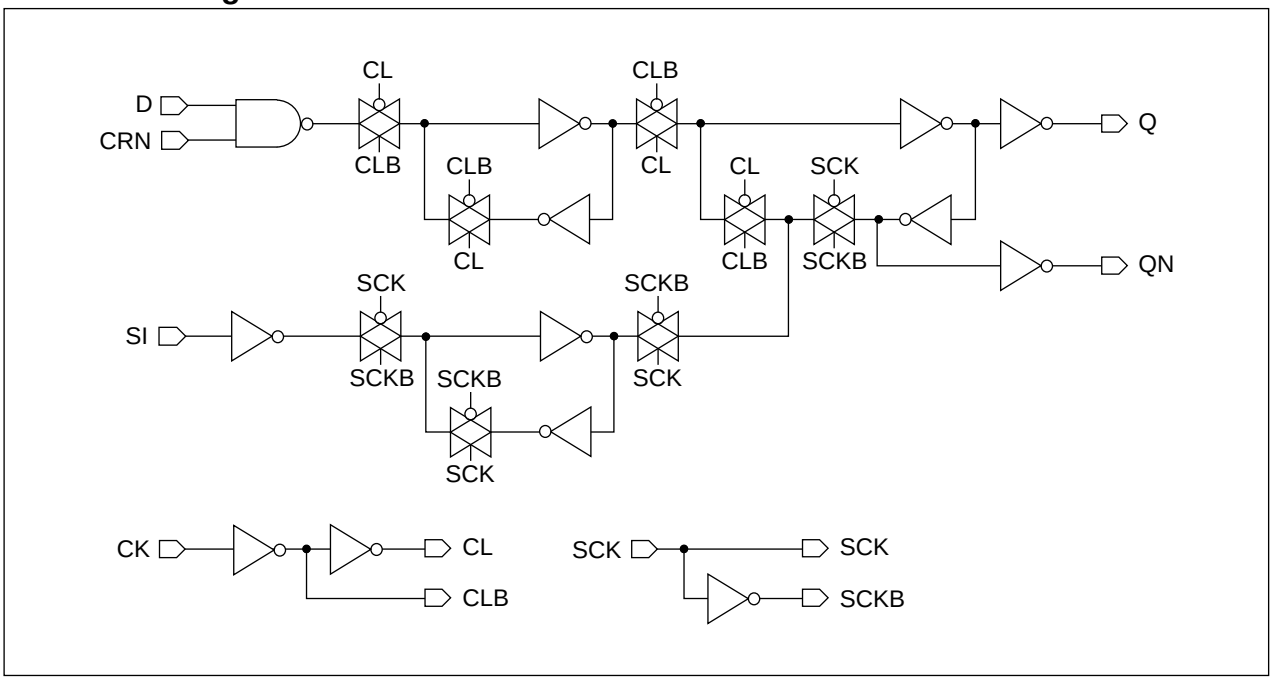
Truth Table

SI	SCK	D	CRN	CK	Q (n+1)	QN (n+1)
x	0	0	1	↑	0	1
x	0	1	1	↑	1	0
0	↑	x	1	0	0	1
1	↑	x	1	0	1	0
x	x	x	0	↑	0	1

Cell Data

Input Load (SL)										Gate Count	
STD80											
FDS2CS					*FDS2CSD2*					*FDS2CS*	*FDS2CSD2*
SI	SCK	D	CRN	CK	SI	SCK	D	CRN	CK		
0.7	1.8	0.7	0.6	0.6	0.6	1.8	0.7	0.6	0.6	9.3	9.7
STDM80											
FDS2CS					*FDS2CSD2*					*FDS2CS*	*FDS2CSD2*
SI	SCK	D	CRN	CK	SI	SCK	D	CRN	CK		
0.6	2.0	0.4	0.5	0.6	0.6	2.0	0.4	0.5	0.6	9.3	9.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FDS2CS	FDS2CSD2	FDS2CS	FDS2CSD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.87	0.87
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (SCK)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width High (SCK)	t_{PWH}	0.87	0.87	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.55	0.37	0.68	0.68
Input Hold Time (D to CK)	t_{HD}	0.36	0.36	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.68	0.68	0.82	0.82
Input Hold Time (SI to SCK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (CRN to CK)	t_{SU}	0.33	0.00	0.33	0.33
Input Hold Time (CRN to CK)	t_{HD}	0.33	0.00	0.33	0.33

FDS2CS/FDS2CSD2

D Flip-Flop with Synchronous Clear, Scan Clock, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FDS2CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.52 + 0.029*SL	0.53 + 0.024*SL	0.54 + 0.024*SL
	t_{PHL}	0.66	0.58 + 0.041*SL	0.58 + 0.038*SL	0.59 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.10 + 0.066*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SCK to Q	t_{PLH}	0.65	0.59 + 0.030*SL	0.60 + 0.025*SL	0.61 + 0.024*SL
	t_{PHL}	0.59	0.50 + 0.042*SL	0.51 + 0.038*SL	0.52 + 0.037*SL
	t_R	0.23	0.14 + 0.045*SL	0.13 + 0.047*SL	0.09 + 0.052*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.76	0.70 + 0.029*SL	0.71 + 0.025*SL	0.72 + 0.024*SL
	t_{PHL}	0.82	0.74 + 0.041*SL	0.74 + 0.038*SL	0.76 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.11 + 0.067*SL	0.09 + 0.069*SL
SCK to QN	t_{PLH}	0.62	0.57 + 0.025*SL	0.57 + 0.023*SL	0.57 + 0.024*SL
	t_{PHL}	0.82	0.74 + 0.037*SL	0.74 + 0.037*SL	0.74 + 0.037*SL
	t_R	0.19	0.09 + 0.048*SL	0.09 + 0.050*SL	0.07 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.09 + 0.068*SL	0.07 + 0.069*SL

STD80 FDS2CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.59	0.55 + 0.018*SL	0.56 + 0.014*SL	0.58 + 0.012*SL
	t_{PHL}	0.65	0.60 + 0.023*SL	0.61 + 0.020*SL	0.63 + 0.018*SL
	t_R	0.16	0.12 + 0.022*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SCK to Q	t_{PLH}	0.66	0.63 + 0.019*SL	0.64 + 0.014*SL	0.66 + 0.012*SL
	t_{PHL}	0.58	0.54 + 0.023*SL	0.55 + 0.020*SL	0.56 + 0.018*SL
	t_R	0.19	0.15 + 0.022*SL	0.15 + 0.022*SL	0.11 + 0.026*SL
	t_F	0.18	0.12 + 0.029*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
CK to QN	t_{PLH}	0.82	0.79 + 0.017*SL	0.79 + 0.014*SL	0.81 + 0.012*SL
	t_{PHL}	0.87	0.83 + 0.021*SL	0.83 + 0.019*SL	0.84 + 0.018*SL
	t_R	0.18	0.14 + 0.023*SL	0.14 + 0.022*SL	0.11 + 0.026*SL
	t_F	0.19	0.12 + 0.033*SL	0.13 + 0.031*SL	0.10 + 0.034*SL
SCK to QN	t_{PLH}	0.69	0.66 + 0.014*SL	0.67 + 0.012*SL	0.67 + 0.012*SL
	t_{PHL}	0.89	0.85 + 0.017*SL	0.85 + 0.017*SL	0.84 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FDS2CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.83	0.76 + 0.038*SL	0.77 + 0.035*SL	0.77 + 0.034*SL
	t_{PHL}	0.93	0.83 + 0.051*SL	0.84 + 0.047*SL	0.86 + 0.045*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.070*SL	0.13 + 0.071*SL
	t_F	0.31	0.14 + 0.081*SL	0.14 + 0.081*SL	0.14 + 0.082*SL
SCK to Q	t_{PLH}	0.98	0.90 + 0.041*SL	0.91 + 0.036*SL	0.93 + 0.034*SL
	t_{PHL}	0.82	0.72 + 0.053*SL	0.74 + 0.046*SL	0.75 + 0.044*SL
	t_R	0.32	0.19 + 0.065*SL	0.18 + 0.067*SL	0.16 + 0.070*SL
	t_F	0.32	0.16 + 0.078*SL	0.16 + 0.079*SL	0.14 + 0.081*SL
CK to QN	t_{PLH}	1.08	0.99 + 0.042*SL	1.01 + 0.036*SL	1.03 + 0.033*SL
	t_{PHL}	1.16	1.05 + 0.054*SL	1.07 + 0.048*SL	1.09 + 0.046*SL
	t_R	0.30	0.16 + 0.069*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.32	0.15 + 0.084*SL	0.16 + 0.082*SL	0.16 + 0.082*SL
SCK to QN	t_{PLH}	0.89	0.82 + 0.034*SL	0.82 + 0.033*SL	0.82 + 0.033*SL
	t_{PHL}	1.21	1.11 + 0.046*SL	1.12 + 0.044*SL	1.12 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.12 + 0.071*SL	0.11 + 0.072*SL
	t_F	0.28	0.13 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.083*SL

STDM80 FDS2CSD2

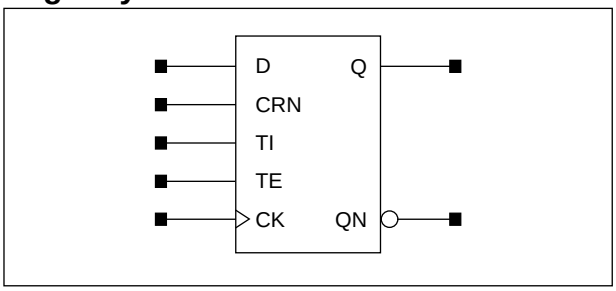
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.84	0.79 + 0.024*SL	0.81 + 0.020*SL	0.82 + 0.018*SL
	t_{PHL}	0.92	0.86 + 0.031*SL	0.88 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.15 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.13 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.039*SL
SCK to Q	t_{PLH}	1.00	0.95 + 0.026*SL	0.97 + 0.021*SL	0.99 + 0.018*SL
	t_{PHL}	0.82	0.76 + 0.031*SL	0.77 + 0.026*SL	0.79 + 0.023*SL
	t_R	0.25	0.18 + 0.033*SL	0.19 + 0.031*SL	0.18 + 0.033*SL
	t_F	0.22	0.14 + 0.041*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
CK to QN	t_{PLH}	1.16	1.12 + 0.023*SL	1.13 + 0.020*SL	1.14 + 0.018*SL
	t_{PHL}	1.23	1.17 + 0.029*SL	1.19 + 0.025*SL	1.20 + 0.023*SL
	t_R	0.23	0.16 + 0.037*SL	0.17 + 0.033*SL	0.17 + 0.033*SL
	t_F	0.23	0.15 + 0.042*SL	0.15 + 0.040*SL	0.16 + 0.039*SL
SCK to QN	t_{PLH}	0.98	0.95 + 0.018*SL	0.95 + 0.017*SL	0.95 + 0.017*SL
	t_{PHL}	1.31	1.26 + 0.024*SL	1.27 + 0.022*SL	1.27 + 0.021*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

FDS2S/FDS2SD2

D Flip-Flop with Synchronous Clear, Scan, 1X/2X Drive

Logic Symbol



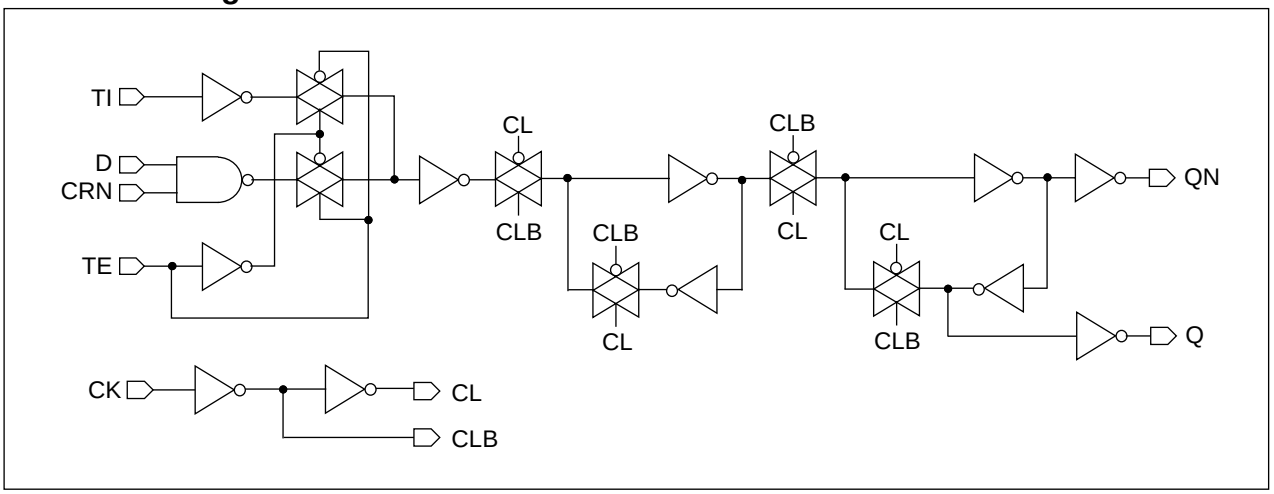
Truth Table

D	CRN	TI	TE	CK	Q (n+1)	QN (n+1)
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	0	x	0	↑	0	1
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0
x	x	x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
STD80											
FDS2S					*FDS2SD2*					*FDS2S*	*FDS2SD2*
D	CRN	TI	TE	CK	D	CRN	TI	TE	CK		
0.5	0.5	0.5	0.8	0.5	0.5	0.5	0.5	0.8	0.5	8.0	8.7
STDM80											
FDS2S					*FDS2SD2*					*FDS2S*	*FDS2SD2*
D	CRN	TI	TE	CK	D	CRN	TI	TE	CK		
0.5	0.4	0.6	1.1	0.6	0.5	0.4	0.6	1.1	0.6	8.0	8.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FDS2S	FDS2SD2	FDS2S	FDS2SD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79	0.77	0.77
Input Setup Time (D to CK)	t_{SU}	0.90	0.90	0.74	0.74
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (CRN to CK)	t_{SU}	0.90	0.90	0.74	0.74
Input Hold Time (CRN to CK)	t_{HD}	0.33	0.00	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.87	0.87	0.71	0.71
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.74	0.74	0.63	0.63
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FDS2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.65 + 0.025*SL	0.65 + 0.024*SL	0.65 + 0.024*SL
	t_{PHL}	0.74	0.67 + 0.038*SL	0.67 + 0.037*SL	0.67 + 0.037*SL
	t_R	0.18	0.09 + 0.046*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
CK to QN	t_{PLH}	0.57	0.52 + 0.028*SL	0.53 + 0.025*SL	0.53 + 0.024*SL
	t_{PHL}	0.66	0.58 + 0.041*SL	0.59 + 0.038*SL	0.59 + 0.037*SL
	t_R	0.20	0.11 + 0.046*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

STD80 FDS2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.76	0.73 + 0.014*SL	0.74 + 0.012*SL	0.74 + 0.012*SL
	t_{PHL}	0.80	0.76 + 0.019*SL	0.76 + 0.018*SL	0.76 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
CK to QN	t_{PLH}	0.58	0.54 + 0.018*SL	0.55 + 0.014*SL	0.57 + 0.012*SL
	t_{PHL}	0.65	0.60 + 0.023*SL	0.61 + 0.020*SL	0.63 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.029*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FDS2S

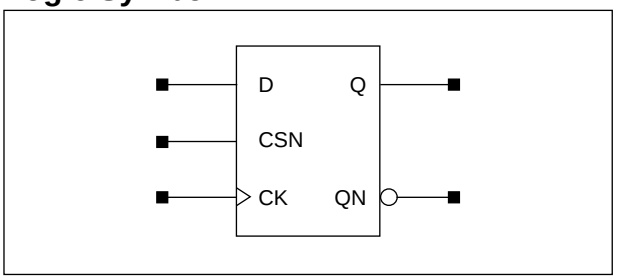
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.00	0.93 + 0.035*SL	0.94 + 0.033*SL	0.94 + 0.033*SL
	t_{PHL}	1.05	0.95 + 0.047*SL	0.96 + 0.044*SL	0.96 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
CK to QN	t_{PLH}	0.82	0.75 + 0.038*SL	0.76 + 0.035*SL	0.76 + 0.034*SL
	t_{PHL}	0.93	0.83 + 0.052*SL	0.85 + 0.046*SL	0.86 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

STDM80 FDS2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.09	1.05 + 0.019*SL	1.06 + 0.017*SL	1.06 + 0.017*SL
	t_{PHL}	1.12	1.07 + 0.025*SL	1.08 + 0.023*SL	1.09 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
CK to QN	t_{PLH}	0.82	0.78 + 0.024*SL	0.79 + 0.020*SL	0.80 + 0.018*SL
	t_{PHL}	0.92	0.86 + 0.030*SL	0.87 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.038*SL	0.14 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



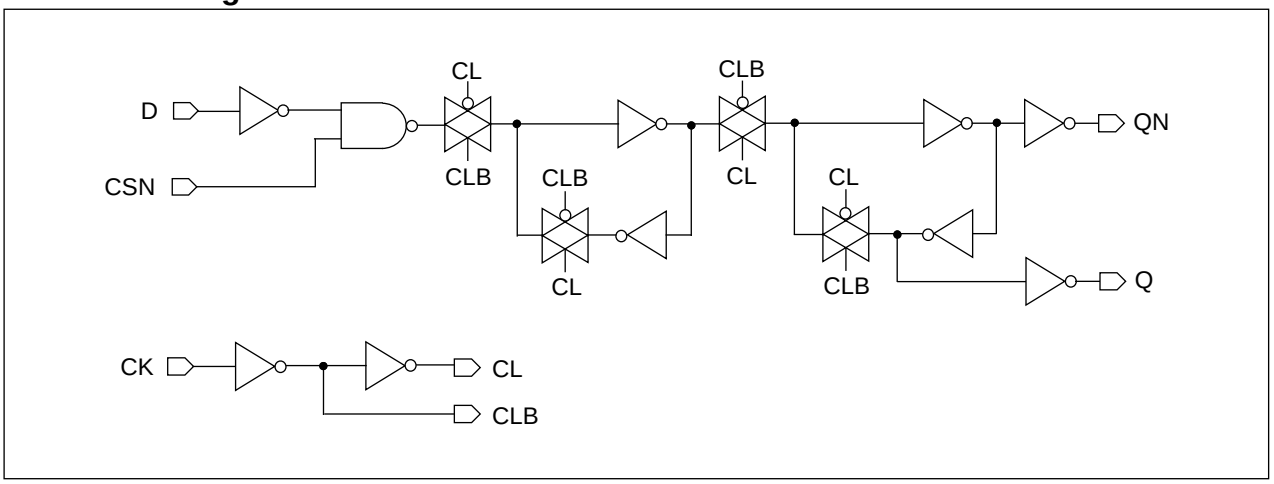
Truth Table

D	CSN	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	1	0
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
STD80							
FDS3			*FDS3D2*			*FDS3*	*FDS3D2*
D	CSN	CK	D	CSN	CK		
0.6	0.4	0.6	1.0	1.0	1.0	6.3	7.0
STDM80							
FDS3			*FDS3D2*			*FDS3*	*FDS3D2*
D	CSN	CK	D	CSN	CK		
0.6	0.7	0.6	0.6	0.7	0.6	6.3	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FDS2	FDS2D2	FDS2	FDS2D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.82	0.82
Pulse Width High (CK)	t_{PWH}	0.87	0.87	0.82	0.82
Input Setup Time (D to CK)	t_{SU}	0.33	0.33	0.33	0.33
Input Hold Time (D to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (CSN to CK)	t_{SU}	0.52	0.52	0.66	0.66
Input Hold Time (CSN to CK)	t_{HD}	0.33	0.33	0.33	0.33

FDS3/FDS3D2

D Flip-Flop with Synchronous Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FDS3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.71	0.66 + 0.025*SL	0.66 + 0.024*SL	0.66 + 0.024*SL
	t_{PHL}	0.75	0.67 + 0.038*SL	0.67 + 0.037*SL	0.67 + 0.037*SL
	t_R	0.18	0.09 + 0.045*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
CK to QN	t_{PLH}	0.58	0.52 + 0.029*SL	0.53 + 0.024*SL	0.54 + 0.024*SL
	t_{PHL}	0.67	0.59 + 0.041*SL	0.59 + 0.038*SL	0.60 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

STD80 FDS3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.77	0.74 + 0.013*SL	0.75 + 0.012*SL	0.75 + 0.012*SL
	t_{PHL}	0.80	0.76 + 0.018*SL	0.77 + 0.018*SL	0.76 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
CK to QN	t_{PLH}	0.58	0.55 + 0.018*SL	0.56 + 0.014*SL	0.57 + 0.012*SL
	t_{PHL}	0.66	0.61 + 0.023*SL	0.62 + 0.020*SL	0.63 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.029*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FDS3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.01	0.94 + 0.035*SL	0.95 + 0.033*SL	0.95 + 0.033*SL
	t_{PHL}	1.05	0.96 + 0.047*SL	0.97 + 0.044*SL	0.97 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
CK to QN	t_{PLH}	0.83	0.75 + 0.038*SL	0.76 + 0.035*SL	0.77 + 0.034*SL
	t_{PHL}	0.94	0.84 + 0.052*SL	0.86 + 0.046*SL	0.87 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

STDM80 FDS3D2

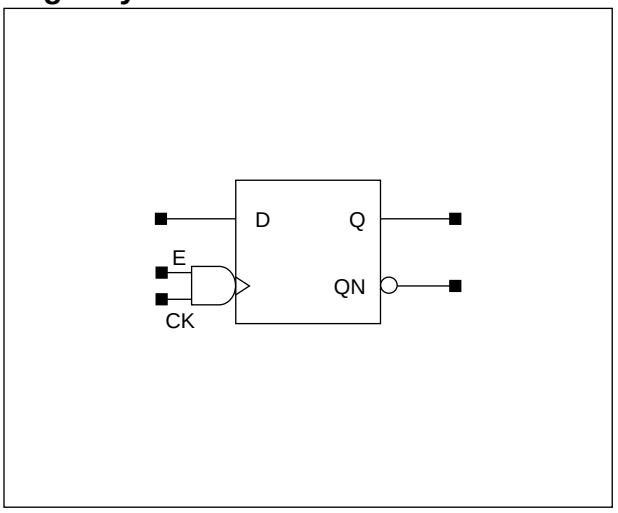
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.10	1.07 + 0.018*SL	1.07 + 0.017*SL	1.07 + 0.017*SL
	t_{PHL}	1.13	1.08 + 0.025*SL	1.08 + 0.023*SL	1.09 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.041*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
CK to QN	t_{PLH}	0.83	0.78 + 0.024*SL	0.79 + 0.020*SL	0.81 + 0.018*SL
	t_{PHL}	0.93	0.87 + 0.030*SL	0.88 + 0.026*SL	0.90 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.038*SL	0.14 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

FG1

D Flip-Flop with CK Enable

Logic Symbol



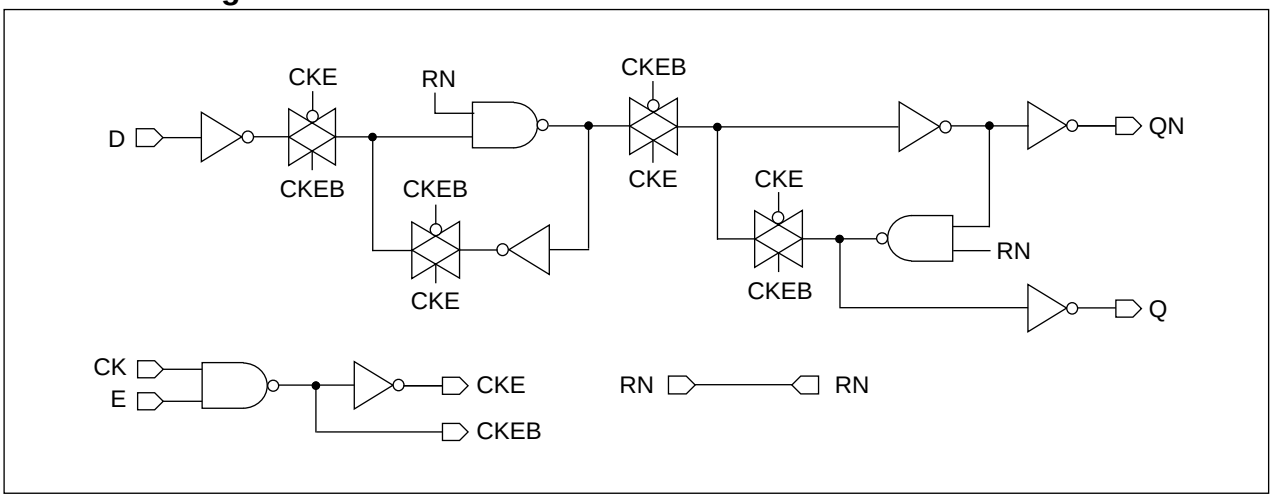
Truth Table

D	E	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	x	Q (n)	QN (n)
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)			Gate Count
STD80			
D	E	CK	
0.5	0.5	0.5	5.7
STDM80			
D	E	CK	
0.6	0.4	0.5	5.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CK)	t_{PWL}	0.87	0.90
Pulse Width High (CK)	t_{PWH}	0.82	0.82
Pulse Width Low (E)	t_{PWL}	0.87	0.85
Pulse Width High (E)	t_{PWH}	0.85	0.85
Input Setup Time (D to CK)	t_{SU}	0.44	0.46
Input Hold Time (D to CK)	t_{HD}	0.36	0.33
Input Setup Time (D to E)	t_{SU}	0.44	0.44
Input Hold Time (D to E)	t_{HD}	0.36	0.36

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FG1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.58 + 0.028*SL	0.59 + 0.024*SL	0.59 + 0.024*SL
	t_{PHL}	0.72	0.64 + 0.041*SL	0.64 + 0.038*SL	0.65 + 0.037*SL
	t_R	0.20	0.11 + 0.046*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
E to Q	t_{PLH}	0.66	0.60 + 0.028*SL	0.61 + 0.024*SL	0.61 + 0.024*SL
	t_{PHL}	0.74	0.66 + 0.041*SL	0.66 + 0.038*SL	0.67 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.76	0.71 + 0.025*SL	0.71 + 0.024*SL	0.71 + 0.024*SL
	t_{PHL}	0.80	0.73 + 0.037*SL	0.73 + 0.037*SL	0.73 + 0.037*SL
	t_R	0.18	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
E to QN	t_{PLH}	0.78	0.73 + 0.025*SL	0.73 + 0.024*SL	0.73 + 0.024*SL
	t_{PHL}	0.82	0.75 + 0.038*SL	0.75 + 0.037*SL	0.75 + 0.037*SL
	t_R	0.18	0.09 + 0.046*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FG1

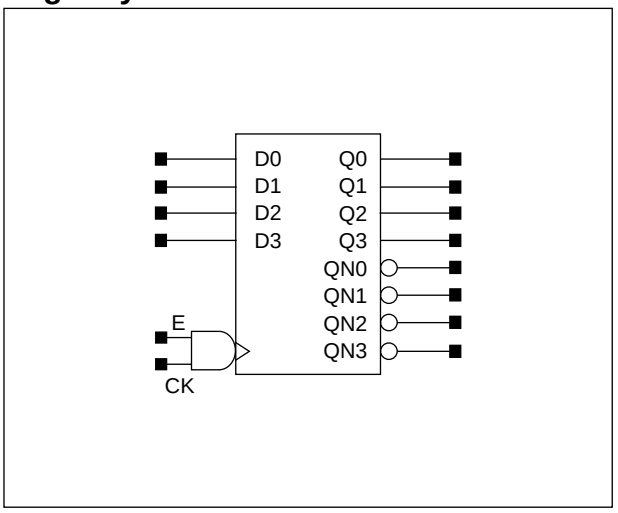
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.92	0.84 + 0.038*SL	0.86 + 0.035*SL	0.86 + 0.034*SL
	t_{PHL}	1.03	0.93 + 0.052*SL	0.94 + 0.046*SL	0.95 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
E to Q	t_{PLH}	0.93	0.86 + 0.038*SL	0.87 + 0.035*SL	0.88 + 0.034*SL
	t_{PHL}	1.04	0.94 + 0.052*SL	0.96 + 0.046*SL	0.97 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
CK to QN	t_{PLH}	1.10	1.03 + 0.035*SL	1.03 + 0.033*SL	1.03 + 0.033*SL
	t_{PHL}	1.15	1.05 + 0.046*SL	1.06 + 0.045*SL	1.06 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
E to QN	t_{PLH}	1.11	1.04 + 0.035*SL	1.04 + 0.034*SL	1.05 + 0.033*SL
	t_{PHL}	1.16	1.07 + 0.047*SL	1.07 + 0.045*SL	1.08 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

FG1X4

4-Bit D Flip-Flop with CK Enable

Logic Symbol



Truth Table

Dn	E	CK	Qn (n+1)	QNn (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	x	Qn (n)	QNn (n)
x	x	↓	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
STD80			
Dn	E	CK	
0.5	0.5	0.5	18.7
STDM80			
Dn	E	CK	
0.6	0.4	0.5	18.7

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CK)	t_{PWL}	0.87	1.86
Pulse Width High (CK)	t_{PWH}	0.87	1.37
Pulse Width Low (E)	t_{PWL}	0.87	1.83
Pulse Width High (E)	t_{PWH}	0.87	1.39
Input Setup Time (D0 to CK)	t_{SU}	0.33	0.33
Input Hold Time (D0 to CK)	t_{HD}	0.74	0.87
Input Setup Time (D0 to E)	t_{SU}	0.33	0.33
Input Hold Time (D0 to E)	t_{HD}	0.76	0.90
Input Setup Time (D1 to CK)	t_{SU}	0.33	0.33
Input Hold Time (D1 to CK)	t_{HD}	0.74	0.87
Input Setup Time (D1 to E)	t_{SU}	0.33	0.33
Input Hold Time (D1 to E)	t_{HD}	0.76	0.90
Input Setup Time (D2 to CK)	t_{SU}	0.33	0.33
Input Hold Time (D2 to CK)	t_{HD}	0.76	0.87
Input Setup Time (D2 to E)	t_{SU}	0.33	0.33
Input Hold Time (D2 to E)	t_{HD}	0.76	0.90
Input Setup Time (D3 to CK)	t_{SU}	0.33	0.33
Input Hold Time (D3 to CK)	t_{HD}	0.74	0.87
Input Setup Time (D3 to E)	t_{SU}	0.33	0.33
Input Hold Time (D3 to E)	t_{HD}	0.76	0.90

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FG1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.94	0.88 + 0.028*SL	0.89 + 0.024*SL	0.90 + 0.024*SL
	t_{PHL}	1.25	1.16 + 0.041*SL	1.17 + 0.038*SL	1.18 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
E to Q0	t_{PLH}	0.96	0.91 + 0.028*SL	0.91 + 0.024*SL	0.92 + 0.024*SL
	t_{PHL}	1.27	1.19 + 0.041*SL	1.19 + 0.038*SL	1.20 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to Q1	t_{PLH}	0.94	0.88 + 0.028*SL	0.89 + 0.025*SL	0.90 + 0.024*SL
	t_{PHL}	1.25	1.16 + 0.041*SL	1.17 + 0.038*SL	1.18 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
E to Q1	t_{PLH}	0.96	0.91 + 0.029*SL	0.91 + 0.024*SL	0.92 + 0.024*SL
	t_{PHL}	1.27	1.19 + 0.041*SL	1.19 + 0.038*SL	1.20 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to Q2	t_{PLH}	0.94	0.88 + 0.028*SL	0.89 + 0.024*SL	0.90 + 0.024*SL
	t_{PHL}	1.25	1.16 + 0.041*SL	1.17 + 0.038*SL	1.18 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
E to Q2	t_{PLH}	0.96	0.91 + 0.028*SL	0.91 + 0.024*SL	0.92 + 0.024*SL
	t_{PHL}	1.27	1.19 + 0.041*SL	1.19 + 0.038*SL	1.20 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
CK to Q3	t_{PLH}	0.94	0.88 + 0.028*SL	0.89 + 0.024*SL	0.90 + 0.024*SL
	t_{PHL}	1.24	1.16 + 0.041*SL	1.17 + 0.038*SL	1.18 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
E to Q3	t_{PLH}	0.96	0.91 + 0.028*SL	0.91 + 0.024*SL	0.92 + 0.024*SL
	t_{PHL}	1.27	1.19 + 0.041*SL	1.19 + 0.038*SL	1.20 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
CK to QN0	t_{PLH}	1.28	1.23 + 0.025*SL	1.24 + 0.024*SL	1.24 + 0.024*SL
	t_{PHL}	1.10	1.03 + 0.038*SL	1.03 + 0.037*SL	1.03 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
E to QN0	t_{PLH}	1.31	1.26 + 0.025*SL	1.26 + 0.024*SL	1.26 + 0.024*SL
	t_{PHL}	1.13	1.05 + 0.038*SL	1.05 + 0.037*SL	1.05 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

(Continued)

FG1X4

4-Bit D Flip-Flop with CK Enable

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FG1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN1	t_{PLH}	1.28	1.23 + 0.025*SL	1.24 + 0.023*SL	1.23 + 0.024*SL
	t_{PHL}	1.10	1.03 + 0.038*SL	1.03 + 0.037*SL	1.03 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
E to QN1	t_{PLH}	1.31	1.26 + 0.025*SL	1.26 + 0.024*SL	1.26 + 0.024*SL
	t_{PHL}	1.13	1.05 + 0.038*SL	1.05 + 0.037*SL	1.05 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
CK to QN2	t_{PLH}	1.28	1.23 + 0.025*SL	1.24 + 0.023*SL	1.23 + 0.024*SL
	t_{PHL}	1.10	1.03 + 0.038*SL	1.03 + 0.037*SL	1.03 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
E to QN2	t_{PLH}	1.31	1.26 + 0.025*SL	1.26 + 0.024*SL	1.26 + 0.024*SL
	t_{PHL}	1.13	1.05 + 0.038*SL	1.05 + 0.037*SL	1.05 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
CK to QN3	t_{PLH}	1.28	1.23 + 0.025*SL	1.23 + 0.024*SL	1.23 + 0.024*SL
	t_{PHL}	1.10	1.03 + 0.038*SL	1.03 + 0.037*SL	1.03 + 0.037*SL
	t_R	0.18	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
E to QN3	t_{PLH}	1.30	1.25 + 0.025*SL	1.26 + 0.023*SL	1.26 + 0.024*SL
	t_{PHL}	1.13	1.05 + 0.038*SL	1.05 + 0.037*SL	1.05 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.06 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FG1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.32	1.24 + 0.039*SL	1.25 + 0.035*SL	1.26 + 0.034*SL
	t_{PHL}	1.80	1.70 + 0.052*SL	1.71 + 0.046*SL	1.72 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.081*SL
E to Q0	t_{PLH}	1.33	1.26 + 0.038*SL	1.27 + 0.035*SL	1.27 + 0.034*SL
	t_{PHL}	1.81	1.71 + 0.052*SL	1.72 + 0.046*SL	1.74 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
CK to Q1	t_{PLH}	1.32	1.24 + 0.038*SL	1.25 + 0.035*SL	1.26 + 0.034*SL
	t_{PHL}	1.80	1.70 + 0.052*SL	1.71 + 0.046*SL	1.73 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.15 + 0.079*SL	0.14 + 0.080*SL	0.14 + 0.081*SL
E to Q1	t_{PLH}	1.33	1.26 + 0.038*SL	1.27 + 0.035*SL	1.27 + 0.034*SL
	t_{PHL}	1.81	1.71 + 0.052*SL	1.73 + 0.046*SL	1.74 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.15 + 0.079*SL	0.14 + 0.080*SL	0.14 + 0.081*SL
CK to Q2	t_{PLH}	1.32	1.24 + 0.038*SL	1.25 + 0.035*SL	1.26 + 0.034*SL
	t_{PHL}	1.80	1.70 + 0.052*SL	1.71 + 0.046*SL	1.72 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.081*SL
E to Q2	t_{PLH}	1.33	1.26 + 0.038*SL	1.27 + 0.035*SL	1.27 + 0.034*SL
	t_{PHL}	1.81	1.71 + 0.052*SL	1.72 + 0.046*SL	1.74 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.081*SL
CK to Q3	t_{PLH}	1.32	1.24 + 0.039*SL	1.25 + 0.035*SL	1.26 + 0.034*SL
	t_{PHL}	1.80	1.69 + 0.052*SL	1.71 + 0.046*SL	1.72 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.15 + 0.079*SL	0.14 + 0.080*SL	0.13 + 0.081*SL
E to Q3	t_{PLH}	1.33	1.25 + 0.039*SL	1.27 + 0.035*SL	1.27 + 0.034*SL
	t_{PHL}	1.81	1.71 + 0.052*SL	1.72 + 0.046*SL	1.74 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
CK to QN0	t_{PLH}	1.87	1.80 + 0.035*SL	1.81 + 0.033*SL	1.81 + 0.033*SL
	t_{PHL}	1.55	1.45 + 0.046*SL	1.46 + 0.045*SL	1.46 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
E to QN0	t_{PLH}	1.88	1.81 + 0.035*SL	1.82 + 0.033*SL	1.82 + 0.033*SL
	t_{PHL}	1.56	1.47 + 0.046*SL	1.47 + 0.045*SL	1.48 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

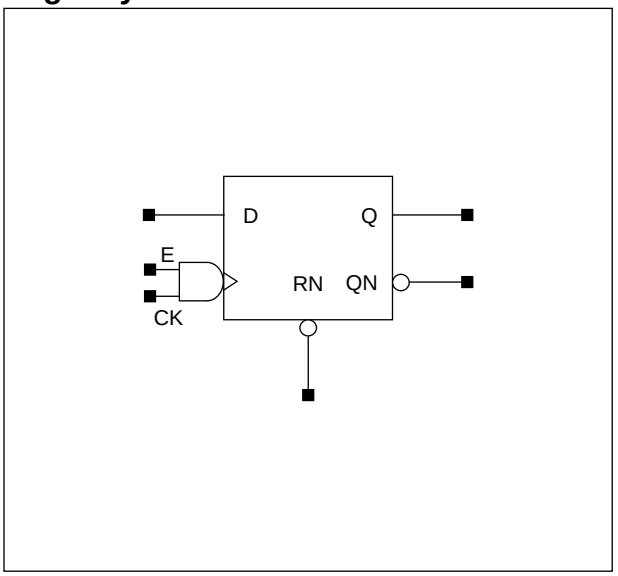
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FG1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN1	t_{PLH}	1.87	1.80 + 0.034*SL	1.80 + 0.034*SL	1.81 + 0.033*SL
	t_{PHL}	1.55	1.45 + 0.046*SL	1.46 + 0.045*SL	1.46 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.10 + 0.083*SL
E to QN1	t_{PLH}	1.88	1.81 + 0.035*SL	1.82 + 0.033*SL	1.82 + 0.033*SL
	t_{PHL}	1.56	1.47 + 0.046*SL	1.47 + 0.044*SL	1.47 + 0.044*SL
	t_R	0.26	0.13 + 0.066*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
CK to QN2	t_{PLH}	1.87	1.80 + 0.035*SL	1.81 + 0.033*SL	1.81 + 0.033*SL
	t_{PHL}	1.55	1.45 + 0.046*SL	1.46 + 0.045*SL	1.46 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
E to QN2	t_{PLH}	1.88	1.81 + 0.035*SL	1.82 + 0.033*SL	1.82 + 0.033*SL
	t_{PHL}	1.56	1.47 + 0.046*SL	1.47 + 0.045*SL	1.48 + 0.044*SL
	t_R	0.26	0.13 + 0.066*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
CK to QN3	t_{PLH}	1.87	1.80 + 0.035*SL	1.80 + 0.033*SL	1.80 + 0.033*SL
	t_{PHL}	1.54	1.45 + 0.046*SL	1.46 + 0.045*SL	1.46 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.10 + 0.083*SL
E to QN3	t_{PLH}	1.88	1.81 + 0.035*SL	1.81 + 0.033*SL	1.82 + 0.033*SL
	t_{PHL}	1.56	1.46 + 0.046*SL	1.47 + 0.045*SL	1.47 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.10 + 0.083*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



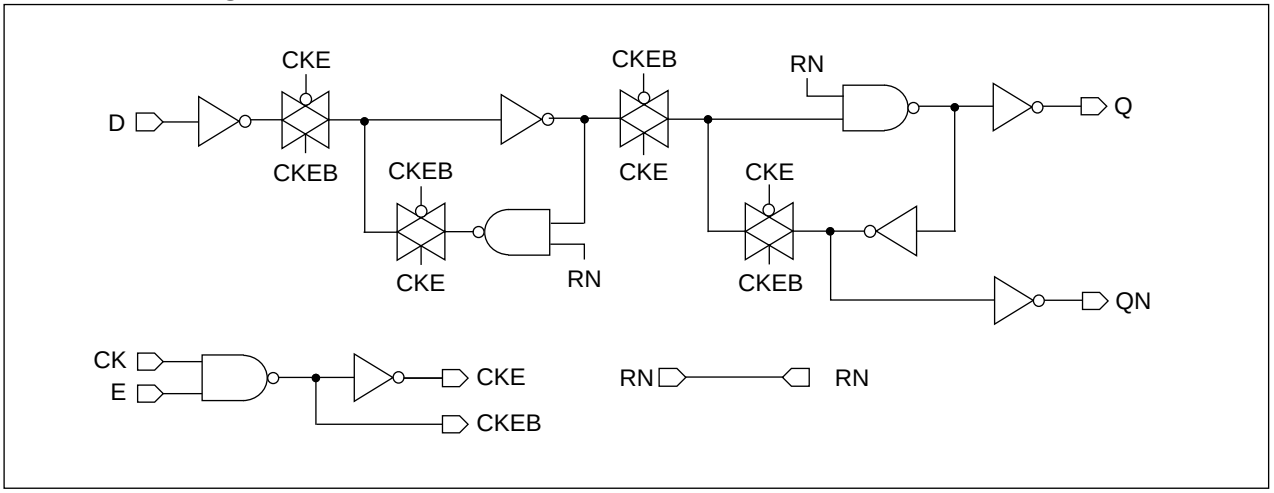
Truth Table

D	E	CK	RN	Q (n+1)	QN (n+1)
0	1	↑	1	0	1
1	1	↑	1	1	0
x	0	x	1	Q (n)	QN (n)
x	x	x	0	0	1
x	x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count
STD80				
D	E	CK	RN	
0.5	0.5	0.5	0.7	6.7
STDM80				
D	E	CK	RN	
0.6	0.4	0.5	1.2	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CK)	t_{PWL}	0.87	0.90
Pulse Width High (CK)	t_{PWH}	0.85	0.85
Pulse Width Low (E)	t_{PWL}	0.87	0.87
Pulse Width High (E)	t_{PWH}	0.85	0.87
Pulse Width Low (RN)	t_{PWL}	0.87	0.82
Input Setup Time (D to CK)	t_{SU}	0.44	0.46
Input Hold Time (D to CK)	t_{HD}	0.33	0.36
Input Setup Time (D to E)	t_{SU}	0.44	0.44
Input Hold Time (D to E)	t_{HD}	0.36	0.36
Recovery Time (RN to CK)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.87
Recovery Time (RN to E)	t_{RC}	0.33	0.33
Input Hold Time (RN to E)	t_{HD}	0.76	0.87

FG2

D Flip-Flop with CK Enable, Reset

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FG2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.63 + 0.031*SL	0.64 + 0.026*SL	0.66 + 0.024*SL
	t_{PHL}	0.74	0.66 + 0.042*SL	0.67 + 0.038*SL	0.68 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
E to Q	t_{PLH}	0.71	0.65 + 0.032*SL	0.66 + 0.026*SL	0.69 + 0.024*SL
	t_{PHL}	0.77	0.68 + 0.041*SL	0.69 + 0.038*SL	0.70 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.78	0.73 + 0.025*SL	0.74 + 0.024*SL	0.74 + 0.024*SL
	t_{PHL}	0.87	0.79 + 0.037*SL	0.79 + 0.037*SL	0.79 + 0.037*SL
	t_R	0.18	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
E to QN	t_{PLH}	0.81	0.76 + 0.025*SL	0.76 + 0.024*SL	0.76 + 0.024*SL
	t_{PHL}	0.89	0.82 + 0.037*SL	0.82 + 0.037*SL	0.82 + 0.037*SL
	t_R	0.18	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.40	0.35 + 0.025*SL	0.36 + 0.024*SL	0.36 + 0.023*SL
	t_R	0.18	0.09 + 0.047*SL	0.09 + 0.050*SL	0.06 + 0.052*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FG2

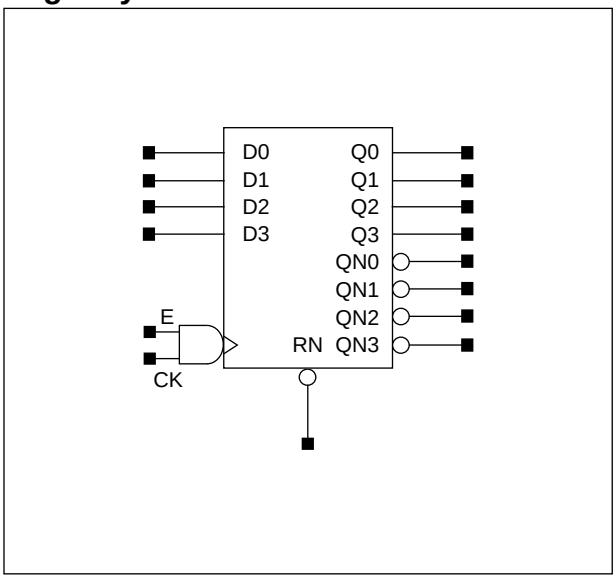
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.01	0.92 + 0.044*SL	0.94 + 0.038*SL	0.96 + 0.035*SL
	t_{PHL}	1.07	0.96 + 0.052*SL	0.98 + 0.046*SL	1.00 + 0.044*SL
	t_R	0.32	0.18 + 0.071*SL	0.18 + 0.068*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
E to Q	t_{PLH}	1.02	0.93 + 0.044*SL	0.95 + 0.037*SL	0.97 + 0.035*SL
	t_{PHL}	1.08	0.98 + 0.052*SL	1.00 + 0.046*SL	1.01 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.068*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
RN to Q	t_{PHL}	0.47	0.37 + 0.052*SL	0.38 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
CK to QN	t_{PLH}	1.14	1.07 + 0.035*SL	1.08 + 0.033*SL	1.08 + 0.033*SL
	t_{PHL}	1.24	1.15 + 0.046*SL	1.16 + 0.045*SL	1.16 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
E to QN	t_{PLH}	1.15	1.08 + 0.035*SL	1.09 + 0.033*SL	1.09 + 0.033*SL
	t_{PHL}	1.26	1.16 + 0.047*SL	1.17 + 0.045*SL	1.17 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.080*SL	0.11 + 0.082*SL
RN to QN	t_{PLH}	0.55	0.48 + 0.035*SL	0.48 + 0.033*SL	0.48 + 0.033*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

FG2X4

4-Bit D Flip-Flop with CK Enable, Reset

Logic Symbol



Truth Table

Dn	E	CK	RN	Qn (n+1)	QNn (n+1)
0	1	↑	1	0	1
1	1	↑	1	1	0
x	0	x	1	Qn (n)	QNn (n)
x	x	x	0	0	1
x	x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count
STD80				
Dn	E	CK	RN	
0.5	0.5	0.5	3.6	22.7
STDM80				
Dn	E	CK	RN	
0.6	0.4	0.5	5.1	22.7

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (CK)	t_{PWL}	0.93	2.00
Pulse Width High (CK)	t_{PWH}	0.87	1.45
Pulse Width Low (E)	t_{PWL}	0.90	1.97
Pulse Width High (E)	t_{PWH}	0.87	1.45
Pulse Width Low (RN)	t_{PWL}	0.87	0.82
Input Setup Time (D0 to CK)	t_{SU}	0.33	0.33
Input Hold Time (D0 to CK)	t_{HD}	0.79	0.93
Input Setup Time (D0 to E)	t_{SU}	0.33	0.33
Input Hold Time (D0 to E)	t_{HD}	0.82	0.96
Input Setup Time (D1 to CK)	t_{SU}	0.33	0.33
Input Hold Time (D1 to CK)	t_{HD}	0.79	0.93
Input Setup Time (D1 to E)	t_{SU}	0.33	0.33
Input Hold Time (D1 to E)	t_{HD}	0.82	0.93
Input Setup Time (D2 to CK)	t_{SU}	0.33	0.33
Input Hold Time (D2 to CK)	t_{HD}	0.79	0.93
Input Setup Time (D2 to E)	t_{SU}	0.33	0.33
Input Hold Time (D2 to E)	t_{HD}	0.82	0.93
Input Setup Time (D3 to CK)	t_{SU}	0.33	0.33
Input Hold Time (D3 to CK)	t_{HD}	0.79	0.93
Input Setup Time (D3 to E)	t_{SU}	0.33	0.33
Input Hold Time (D3 to E)	t_{HD}	0.82	0.93
Recovery Time (RN to CK)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	1.09	1.31
Recovery Time (RN to E)	t_{RC}	0.33	0.33
Input Hold Time (RN to E)	t_{HD}	1.09	1.31

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FG2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.03	0.96 + 0.032*SL	0.97 + 0.026*SL	1.00 + 0.024*SL
	t_{PHL}	1.32	1.24 + 0.041*SL	1.25 + 0.038*SL	1.25 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
E to Q0	t_{PLH}	1.05	0.99 + 0.032*SL	1.00 + 0.026*SL	1.02 + 0.024*SL
	t_{PHL}	1.35	1.27 + 0.041*SL	1.27 + 0.038*SL	1.28 + 0.037*SL
	t_R	0.23	0.14 + 0.048*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q0	t_{PHL}	0.37	0.29 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to Q1	t_{PLH}	1.03	0.96 + 0.032*SL	0.98 + 0.026*SL	1.00 + 0.024*SL
	t_{PHL}	1.32	1.24 + 0.041*SL	1.25 + 0.038*SL	1.25 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
E to Q1	t_{PLH}	1.05	0.99 + 0.032*SL	1.00 + 0.026*SL	1.02 + 0.024*SL
	t_{PHL}	1.35	1.27 + 0.041*SL	1.27 + 0.038*SL	1.28 + 0.037*SL
	t_R	0.23	0.14 + 0.048*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q1	t_{PHL}	0.37	0.29 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to Q2	t_{PLH}	1.03	0.96 + 0.032*SL	0.97 + 0.026*SL	1.00 + 0.024*SL
	t_{PHL}	1.32	1.24 + 0.041*SL	1.25 + 0.038*SL	1.25 + 0.037*SL
	t_R	0.23	0.14 + 0.045*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
E to Q2	t_{PLH}	1.05	0.99 + 0.032*SL	1.00 + 0.026*SL	1.02 + 0.024*SL
	t_{PHL}	1.35	1.27 + 0.041*SL	1.27 + 0.038*SL	1.28 + 0.037*SL
	t_R	0.23	0.14 + 0.048*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q2	t_{PHL}	0.37	0.29 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to Q3	t_{PLH}	1.02	0.96 + 0.032*SL	0.97 + 0.026*SL	1.00 + 0.024*SL
	t_{PHL}	1.32	1.24 + 0.041*SL	1.25 + 0.038*SL	1.25 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
E to Q3	t_{PLH}	1.05	0.98 + 0.032*SL	0.99 + 0.026*SL	1.02 + 0.024*SL
	t_{PHL}	1.34	1.26 + 0.041*SL	1.27 + 0.038*SL	1.28 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q3	t_{PHL}	0.37	0.28 + 0.041*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FG2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN0	t_{PLH}	1.36	1.31 + 0.025*SL	1.32 + 0.024*SL	1.32 + 0.024*SL
	t_{PHL}	1.20	1.12 + 0.037*SL	1.12 + 0.037*SL	1.12 + 0.037*SL
	t_R	0.19	0.09 + 0.047*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
E to QN0	t_{PLH}	1.39	1.34 + 0.025*SL	1.34 + 0.024*SL	1.34 + 0.024*SL
	t_{PHL}	1.22	1.15 + 0.037*SL	1.15 + 0.037*SL	1.14 + 0.037*SL
	t_R	0.19	0.09 + 0.046*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN0	t_{PLH}	0.41	0.36 + 0.025*SL	0.36 + 0.023*SL	0.36 + 0.023*SL
	t_R	0.19	0.09 + 0.047*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
CK to QN1	t_{PLH}	1.36	1.31 + 0.026*SL	1.32 + 0.023*SL	1.31 + 0.024*SL
	t_{PHL}	1.20	1.12 + 0.037*SL	1.12 + 0.037*SL	1.12 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
E to QN1	t_{PLH}	1.39	1.34 + 0.025*SL	1.34 + 0.024*SL	1.34 + 0.024*SL
	t_{PHL}	1.22	1.15 + 0.037*SL	1.15 + 0.037*SL	1.14 + 0.037*SL
	t_R	0.19	0.10 + 0.045*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN1	t_{PLH}	0.41	0.36 + 0.025*SL	0.36 + 0.024*SL	0.37 + 0.023*SL
	t_R	0.19	0.09 + 0.047*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
CK to QN2	t_{PLH}	1.36	1.31 + 0.026*SL	1.32 + 0.023*SL	1.31 + 0.024*SL
	t_{PHL}	1.20	1.12 + 0.037*SL	1.12 + 0.037*SL	1.12 + 0.037*SL
	t_R	0.19	0.10 + 0.045*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
E to QN2	t_{PLH}	1.39	1.34 + 0.025*SL	1.34 + 0.024*SL	1.34 + 0.024*SL
	t_{PHL}	1.22	1.15 + 0.037*SL	1.15 + 0.037*SL	1.14 + 0.037*SL
	t_R	0.19	0.09 + 0.046*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN2	t_{PLH}	0.41	0.36 + 0.025*SL	0.36 + 0.023*SL	0.36 + 0.023*SL
	t_R	0.19	0.09 + 0.047*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
CK to QN3	t_{PLH}	1.36	1.31 + 0.025*SL	1.31 + 0.024*SL	1.31 + 0.024*SL
	t_{PHL}	1.19	1.12 + 0.037*SL	1.12 + 0.037*SL	1.12 + 0.037*SL
	t_R	0.19	0.09 + 0.046*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
E to QN3	t_{PLH}	1.38	1.33 + 0.026*SL	1.34 + 0.023*SL	1.33 + 0.024*SL
	t_{PHL}	1.22	1.14 + 0.037*SL	1.14 + 0.037*SL	1.14 + 0.037*SL
	t_R	0.18	0.09 + 0.045*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN3	t_{PLH}	0.41	0.35 + 0.026*SL	0.36 + 0.023*SL	0.36 + 0.023*SL
	t_R	0.18	0.09 + 0.047*SL	0.09 + 0.049*SL	0.06 + 0.052*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FG2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.44	1.35 + 0.044*SL	1.37 + 0.038*SL	1.40 + 0.035*SL
	t_{PHL}	1.92	1.82 + 0.052*SL	1.83 + 0.046*SL	1.85 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.16 + 0.078*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
E to Q0	t_{PLH}	1.45	1.37 + 0.044*SL	1.38 + 0.038*SL	1.41 + 0.035*SL
	t_{PHL}	1.93	1.83 + 0.052*SL	1.84 + 0.046*SL	1.86 + 0.045*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.18 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q0	t_{PHL}	0.48	0.37 + 0.052*SL	0.39 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.080*SL	0.14 + 0.081*SL
CK to Q1	t_{PLH}	1.44	1.35 + 0.044*SL	1.37 + 0.038*SL	1.40 + 0.035*SL
	t_{PHL}	1.92	1.82 + 0.052*SL	1.83 + 0.046*SL	1.85 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.18 + 0.070*SL
	t_F	0.31	0.16 + 0.078*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
E to Q1	t_{PLH}	1.45	1.37 + 0.044*SL	1.38 + 0.038*SL	1.41 + 0.035*SL
	t_{PHL}	1.93	1.83 + 0.052*SL	1.84 + 0.046*SL	1.86 + 0.045*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.18 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q1	t_{PHL}	0.48	0.37 + 0.052*SL	0.39 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.14 + 0.081*SL
CK to Q2	t_{PLH}	1.44	1.35 + 0.044*SL	1.37 + 0.038*SL	1.40 + 0.035*SL
	t_{PHL}	1.92	1.82 + 0.052*SL	1.83 + 0.046*SL	1.85 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.31	0.16 + 0.078*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
E to Q2	t_{PLH}	1.45	1.37 + 0.044*SL	1.38 + 0.038*SL	1.41 + 0.035*SL
	t_{PHL}	1.93	1.83 + 0.052*SL	1.84 + 0.046*SL	1.86 + 0.045*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.18 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
RN to Q2	t_{PHL}	0.48	0.37 + 0.052*SL	0.39 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
CK to Q3	t_{PLH}	1.44	1.35 + 0.044*SL	1.37 + 0.038*SL	1.39 + 0.035*SL
	t_{PHL}	1.92	1.81 + 0.052*SL	1.83 + 0.046*SL	1.84 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.068*SL	0.18 + 0.070*SL
	t_F	0.31	0.15 + 0.078*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
E to Q3	t_{PLH}	1.45	1.36 + 0.044*SL	1.38 + 0.038*SL	1.40 + 0.034*SL
	t_{PHL}	1.93	1.82 + 0.052*SL	1.84 + 0.046*SL	1.85 + 0.044*SL
	t_R	0.32	0.18 + 0.071*SL	0.18 + 0.068*SL	0.17 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.14 + 0.081*SL
RN to Q3	t_{PHL}	0.47	0.37 + 0.052*SL	0.38 + 0.047*SL	0.40 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

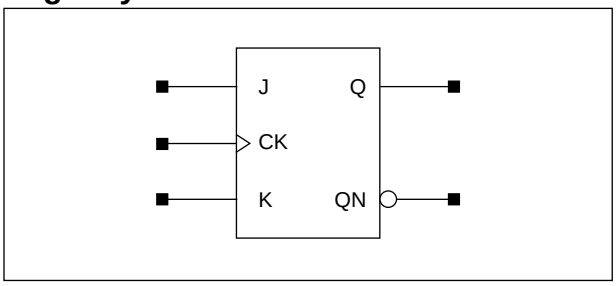
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FG2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN0	t_{PLH}	1.99	1.92 + 0.035*SL	1.93 + 0.033*SL	1.93 + 0.033*SL
	t_{PHL}	1.68	1.59 + 0.046*SL	1.59 + 0.045*SL	1.60 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.078*SL	0.13 + 0.080*SL	0.11 + 0.082*SL
E to QN0	t_{PLH}	2.01	1.94 + 0.035*SL	1.94 + 0.033*SL	1.94 + 0.033*SL
	t_{PHL}	1.69	1.60 + 0.047*SL	1.60 + 0.045*SL	1.61 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.13 + 0.080*SL	0.11 + 0.082*SL
RN to QN0	t_{PLH}	0.56	0.48 + 0.035*SL	0.49 + 0.033*SL	0.49 + 0.033*SL
	t_R	0.26	0.13 + 0.066*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
CK to QN1	t_{PLH}	1.99	1.92 + 0.035*SL	1.93 + 0.033*SL	1.93 + 0.033*SL
	t_{PHL}	1.68	1.58 + 0.047*SL	1.59 + 0.045*SL	1.60 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.078*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
E to QN1	t_{PLH}	2.01	1.94 + 0.035*SL	1.94 + 0.033*SL	1.94 + 0.033*SL
	t_{PHL}	1.69	1.60 + 0.047*SL	1.60 + 0.044*SL	1.61 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.078*SL	0.13 + 0.080*SL	0.11 + 0.082*SL
RN to QN1	t_{PLH}	0.56	0.48 + 0.035*SL	0.49 + 0.033*SL	0.49 + 0.033*SL
	t_R	0.26	0.13 + 0.066*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
CK to QN2	t_{PLH}	1.99	1.92 + 0.035*SL	1.93 + 0.033*SL	1.93 + 0.033*SL
	t_{PHL}	1.68	1.59 + 0.046*SL	1.59 + 0.045*SL	1.60 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.078*SL	0.13 + 0.080*SL	0.11 + 0.082*SL
E to QN2	t_{PLH}	2.01	1.94 + 0.035*SL	1.94 + 0.033*SL	1.94 + 0.033*SL
	t_{PHL}	1.69	1.60 + 0.047*SL	1.60 + 0.045*SL	1.61 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.13 + 0.080*SL	0.11 + 0.082*SL
RN to QN2	t_{PLH}	0.56	0.48 + 0.035*SL	0.49 + 0.033*SL	0.49 + 0.033*SL
	t_R	0.26	0.13 + 0.066*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
CK to QN3	t_{PLH}	1.99	1.92 + 0.035*SL	1.92 + 0.033*SL	1.92 + 0.033*SL
	t_{PHL}	1.67	1.58 + 0.046*SL	1.58 + 0.045*SL	1.59 + 0.044*SL
	t_R	0.26	0.13 + 0.066*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
E to QN3	t_{PLH}	2.00	1.93 + 0.035*SL	1.93 + 0.033*SL	1.94 + 0.033*SL
	t_{PHL}	1.68	1.59 + 0.047*SL	1.60 + 0.045*SL	1.60 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.078*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
RN to QN3	t_{PLH}	0.55	0.48 + 0.034*SL	0.48 + 0.034*SL	0.48 + 0.033*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Logic Symbol



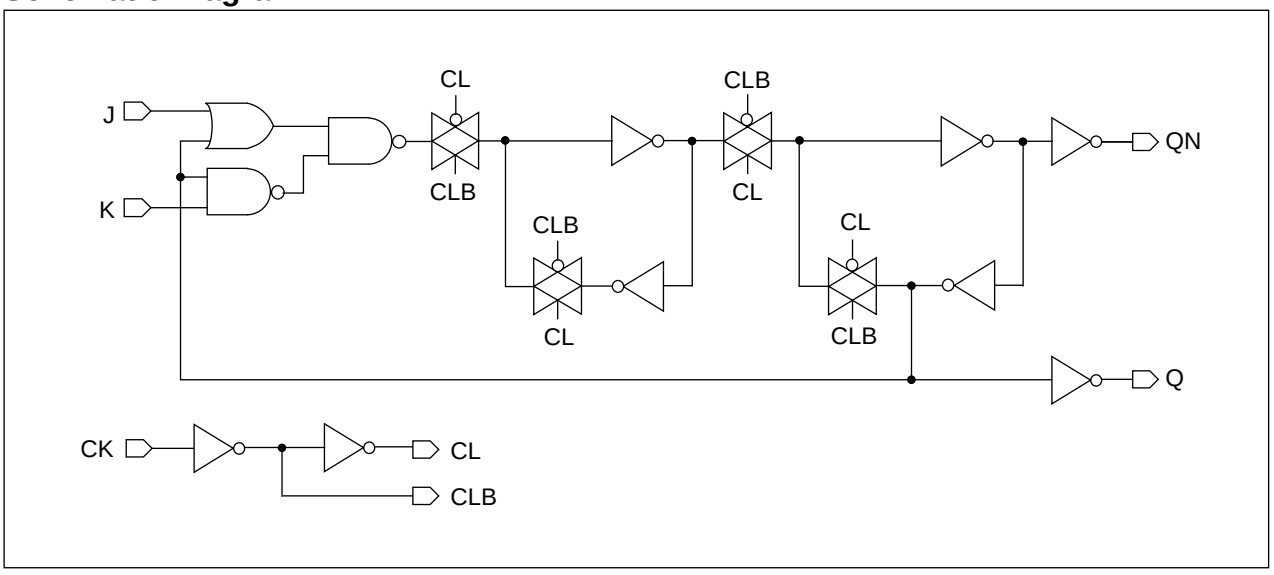
Truth Table

J	CK	K	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	0	1	0
0	↑	0	Q (n)	QN (n)
1	↑	1	QN (n)	Q (n)
x	↓	x	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
STD80							
FJ1			*FJ1D2*			*FJ1*	*FJ1D2*
J	CK	K	J	CK	K		
0.5	0.5	0.3	0.5	0.5	0.3	7.0	7.7
STDM80							
FJ1			*FJ1D2*			*FJ1*	*FJ1D2*
J	CK	K	J	CK	K		
0.4	0.6	0.6	0.4	0.6	0.6	7.0	7.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FJ1	FJ1D2	FJ1	FJ1D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.87	0.87
Pulse Width High (CK)	t_{PWH}	0.79	0.79	0.82	0.82
Input Setup Time (J to CK)	t_{SU}	0.79	0.82	0.82	0.82
Input Hold Time (J to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.79	0.82	0.82	0.82
Input Hold Time (K to CK)	t_{HD}	0.33	0.33	0.33	0.33

Switching Characteristics

(Typical process, 25 °C, 5 V, t_R/t_F = 0.44 ns, SL: Standard Load)

STD80 FJ1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.76	0.70 + 0.028*SL	0.71 + 0.024*SL	0.72 + 0.024*SL
	t_{PHL}	0.81	0.73 + 0.040*SL	0.74 + 0.037*SL	0.74 + 0.037*SL
	t_R	0.21	0.12 + 0.043*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.57	0.52 + 0.027*SL	0.52 + 0.024*SL	0.53 + 0.024*SL
	t_{PHL}	0.65	0.57 + 0.041*SL	0.58 + 0.038*SL	0.59 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

STD80 FJ1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.79 + 0.016*SL	0.79 + 0.013*SL	0.81 + 0.012*SL
	t_{PHL}	0.86	0.82 + 0.021*SL	0.83 + 0.019*SL	0.83 + 0.018*SL
	t_R	0.17	0.13 + 0.023*SL	0.13 + 0.023*SL	0.10 + 0.026*SL
	t_F	0.19	0.12 + 0.033*SL	0.13 + 0.031*SL	0.10 + 0.034*SL
CK to QN	t_{PLH}	0.58	0.54 + 0.018*SL	0.55 + 0.014*SL	0.57 + 0.012*SL
	t_{PHL}	0.64	0.60 + 0.023*SL	0.61 + 0.020*SL	0.62 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.10 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FJ1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.08	1.01 + 0.038*SL	1.02 + 0.034*SL	1.02 + 0.033*SL
	t_{PHL}	1.15	1.05 + 0.052*SL	1.07 + 0.046*SL	1.08 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.068*SL	0.13 + 0.071*SL
	t_F	0.32	0.16 + 0.080*SL	0.16 + 0.079*SL	0.15 + 0.081*SL
CK to QN	t_{PLH}	0.82	0.74 + 0.038*SL	0.75 + 0.034*SL	0.76 + 0.034*SL
	t_{PHL}	0.92	0.82 + 0.051*SL	0.83 + 0.047*SL	0.85 + 0.045*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.070*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

STDM80 FJ1D2

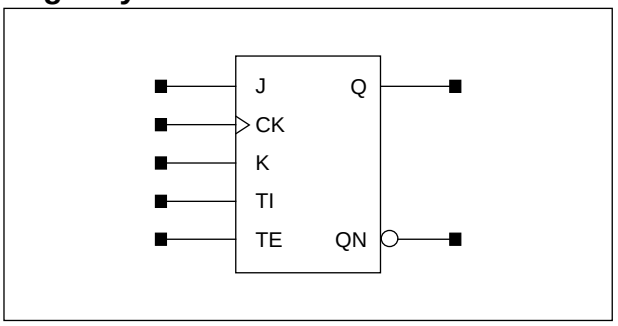
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.17	1.12 + 0.021*SL	1.13 + 0.019*SL	1.14 + 0.017*SL
	t_{PHL}	1.22	1.16 + 0.029*SL	1.17 + 0.025*SL	1.19 + 0.023*SL
	t_R	0.22	0.15 + 0.035*SL	0.15 + 0.033*SL	0.15 + 0.033*SL
	t_F	0.23	0.15 + 0.042*SL	0.16 + 0.040*SL	0.17 + 0.037*SL
CK to QN	t_{PLH}	0.82	0.77 + 0.024*SL	0.79 + 0.020*SL	0.80 + 0.018*SL
	t_{PHL}	0.91	0.85 + 0.030*SL	0.87 + 0.026*SL	0.88 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

FJ1S/FJ1SD2

JK Flip-Flop with Scan, 1X/2X Drive

Logic Symbol



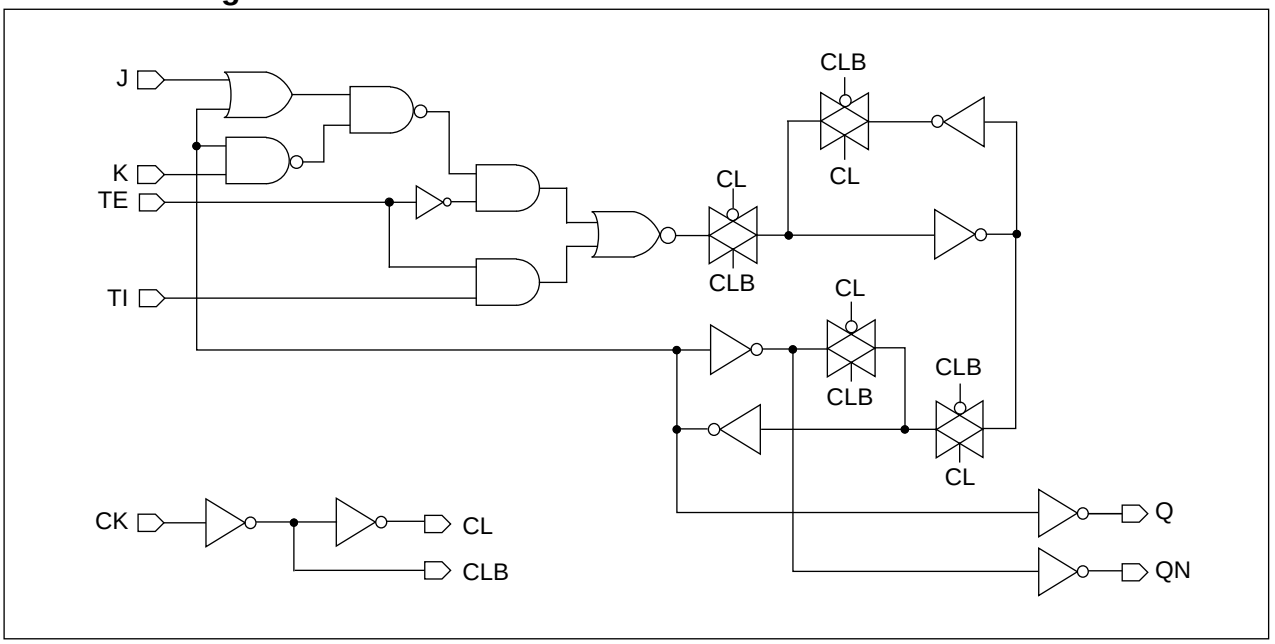
Truth Table

J	CK	K	TI	TE	Q (n+1)	QN (n+1)
0	↑	1	x	0	0	1
1	↑	0	x	0	1	0
0	↑	0	x	0	Q (n)	QN (n)
1	↑	1	x	0	QN (n)	Q (n)
x	↓	x	x	x	Q (n)	QN (n)
x	↑	x	0	1	0	1
x	↑	x	1	1	1	0

Cell Data

Input Load (SL)										Gate Count	
STD80											
FJ1S					*FJ1SD2*					*FJ1S*	*FJ1SD 2*
J	CK	K	TI	TE	J	CK	K	TI	TE		
0.3	0.5	0.3	0.5	0.9	0.3	0.5	0.3	0.5	0.9	9.3	10.0
STDM80											
FJ1S					*FJ1SD2*					*FJ1S*	*FJ1SD 2*
J	CK	K	TI	TE	J	CK	K	TI	TE		
0.6	0.6	0.5	0.4	1.1	0.6	0.6	0.5	0.4	1.1	9.3	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FJ1S	FJ1SD2	FJ1S	FJ1SD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.96	0.96
Pulse Width High (CK)	t_{PWH}	0.79	0.79	0.82	0.82
Input Setup Time (J to CK)	t_{SU}	0.82	0.82	1.20	1.20
Input Hold Time (J to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.82	0.82	1.20	1.20
Input Hold Time (K to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.66	0.66	0.93	0.93
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.63	0.63	0.82	0.82
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FJ1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.65	0.59 + 0.031*SL	0.60 + 0.026*SL	0.62 + 0.024*SL
	t_{PHL}	0.74	0.65 + 0.044*SL	0.66 + 0.039*SL	0.68 + 0.037*SL
	t_R	0.23	0.14 + 0.045*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.26	0.14 + 0.063*SL	0.13 + 0.065*SL	0.09 + 0.069*SL
CK to QN	t_{PLH}	0.77	0.72 + 0.025*SL	0.72 + 0.024*SL	0.72 + 0.024*SL
	t_{PHL}	0.82	0.75 + 0.037*SL	0.75 + 0.037*SL	0.75 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL

STD80 FJ1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.65	0.60 + 0.021*SL	0.62 + 0.015*SL	0.65 + 0.012*SL
	t_{PHL}	0.72	0.67 + 0.025*SL	0.68 + 0.021*SL	0.71 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.20	0.14 + 0.033*SL	0.14 + 0.031*SL	0.11 + 0.034*SL
CK to QN	t_{PLH}	0.84	0.81 + 0.014*SL	0.81 + 0.012*SL	0.82 + 0.012*SL
	t_{PHL}	0.88	0.84 + 0.019*SL	0.84 + 0.018*SL	0.84 + 0.018*SL
	t_R	0.16	0.11 + 0.024*SL	0.12 + 0.022*SL	0.08 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FJ1S

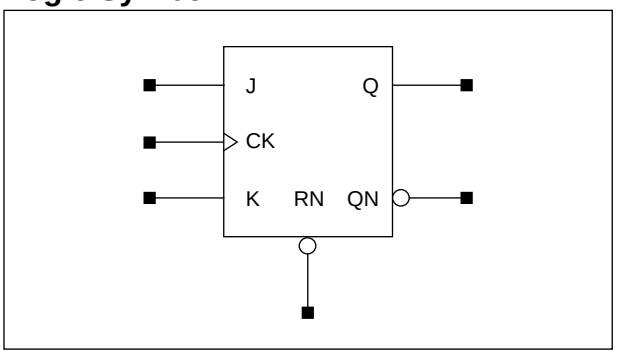
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.93	0.84 + 0.043*SL	0.86 + 0.036*SL	0.88 + 0.034*SL
	t_{PHL}	1.04	0.93 + 0.057*SL	0.95 + 0.049*SL	0.98 + 0.045*SL
	t_R	0.31	0.18 + 0.066*SL	0.18 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.34	0.18 + 0.081*SL	0.19 + 0.079*SL	0.18 + 0.080*SL
CK to QN	t_{PLH}	1.11	1.04 + 0.035*SL	1.04 + 0.033*SL	1.04 + 0.033*SL
	t_{PHL}	1.16	1.07 + 0.047*SL	1.07 + 0.045*SL	1.08 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.11 + 0.071*SL
	t_F	0.28	0.13 + 0.078*SL	0.12 + 0.080*SL	0.11 + 0.082*SL

STDM80 FJ1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.92	0.86 + 0.027*SL	0.88 + 0.022*SL	0.90 + 0.019*SL
	t_{PHL}	1.02	0.95 + 0.034*SL	0.97 + 0.028*SL	0.99 + 0.025*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.033*SL	0.17 + 0.034*SL
	t_F	0.25	0.16 + 0.043*SL	0.18 + 0.039*SL	0.18 + 0.038*SL
CK to QN	t_{PLH}	1.20	1.16 + 0.019*SL	1.16 + 0.018*SL	1.17 + 0.017*SL
	t_{PHL}	1.23	1.18 + 0.026*SL	1.19 + 0.023*SL	1.20 + 0.022*SL
	t_R	0.20	0.14 + 0.032*SL	0.14 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.13 + 0.038*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



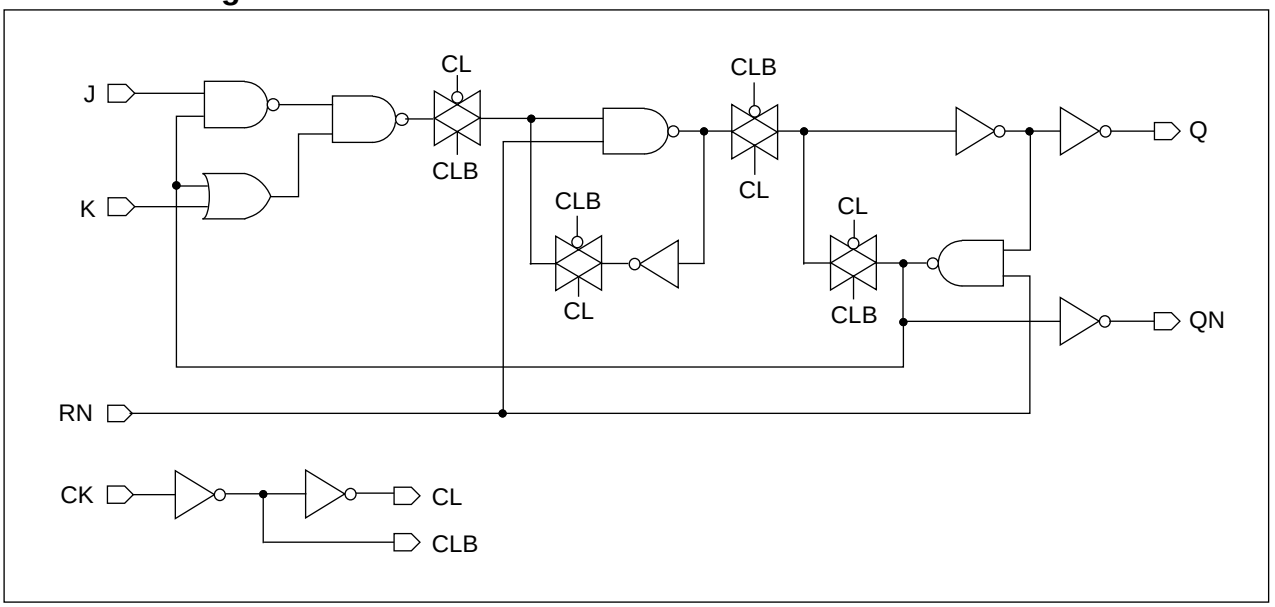
Truth Table

J	CK	K	RN	Q (n+1)	QN (n+1)
0	⎍	1	1	0	1
1	⎍	0	1	1	0
0	⎍	0	1	Q (n)	QN (n)
1	⎍	1	1	QN (n)	Q (n)
x	⎎	x	1	Q (n)	QN (n)
x	x	x	0	0	1

Cell Data

Input Load (SL)								Gate Count	
STD80									
FJ2				*FJ2D2*				*FJ2*	*FJ2D2*
J	CK	K	RN	J	CK	K	RN		
0.5	0.5	0.3	0.7	0.5	0.5	0.3	0.7	8.3	9.0
STDM80									
FJ2				*FJ2D2*				*FJ2*	*FJ2D2*
J	CK	K	RN	J	CK	K	RN		
0.6	0.6	0.5	1.1	0.6	0.6	0.5	1.1	8.3	9.0

Schematic Diagram



FJ2/FJ2D2

JK Flip-Flop with Reset, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FJ2	FJ2D2	FJ2	FJ2D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.96	0.96
Pulse Width High (CK)	t_{PWH}	0.79	0.79	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.87	0.90
Input Setup Time (J to CK)	t_{SU}	0.87	0.87	0.87	0.87
Input Hold Time (J to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.87	0.87	0.87	0.87
Input Hold Time (K to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.38	0.38	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FJ2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.90	0.83 + 0.034*SL	0.85 + 0.027*SL	0.88 + 0.024*SL
	t_{PHL}	0.86	0.78 + 0.041*SL	0.78 + 0.038*SL	0.79 + 0.037*SL
	t_R	0.25	0.16 + 0.047*SL	0.16 + 0.048*SL	0.12 + 0.051*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.065*SL	0.09 + 0.069*SL
RN to Q	t_{PHL}	0.43	0.35 + 0.042*SL	0.36 + 0.038*SL	0.36 + 0.037*SL
	t_F	0.25	0.13 + 0.062*SL	0.12 + 0.065*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.58	0.52 + 0.028*SL	0.53 + 0.024*SL	0.53 + 0.024*SL
	t_{PHL}	0.70	0.62 + 0.041*SL	0.63 + 0.038*SL	0.63 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
RN to QN	t_{PLH}	0.61	0.55 + 0.029*SL	0.56 + 0.024*SL	0.57 + 0.023*SL
	t_R	0.21	0.12 + 0.043*SL	0.11 + 0.048*SL	0.07 + 0.052*SL

STD80 FJ2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.96	0.92 + 0.022*SL	0.93 + 0.016*SL	0.97 + 0.012*SL
	t_{PHL}	0.91	0.86 + 0.023*SL	0.87 + 0.019*SL	0.88 + 0.018*SL
	t_R	0.22	0.17 + 0.025*SL	0.18 + 0.024*SL	0.16 + 0.025*SL
	t_F	0.20	0.14 + 0.031*SL	0.14 + 0.031*SL	0.11 + 0.034*SL
RN to Q	t_{PHL}	0.42	0.37 + 0.025*SL	0.38 + 0.020*SL	0.40 + 0.018*SL
	t_F	0.20	0.13 + 0.032*SL	0.14 + 0.030*SL	0.10 + 0.034*SL
CK to QN	t_{PLH}	0.58	0.55 + 0.018*SL	0.56 + 0.014*SL	0.57 + 0.012*SL
	t_{PHL}	0.69	0.65 + 0.023*SL	0.65 + 0.020*SL	0.67 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
RN to QN	t_{PLH}	0.61	0.58 + 0.018*SL	0.59 + 0.013*SL	0.60 + 0.012*SL
	t_R	0.17	0.13 + 0.019*SL	0.12 + 0.023*SL	0.09 + 0.026*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FJ2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.29	1.20 + 0.046*SL	1.22 + 0.039*SL	1.25 + 0.035*SL
	t_{PHL}	1.22	1.11 + 0.054*SL	1.13 + 0.047*SL	1.15 + 0.045*SL
	t_R	0.34	0.20 + 0.071*SL	0.21 + 0.068*SL	0.20 + 0.069*SL
	t_F	0.33	0.17 + 0.081*SL	0.18 + 0.078*SL	0.17 + 0.080*SL
RN to Q	t_{PHL}	0.57	0.46 + 0.056*SL	0.48 + 0.048*SL	0.50 + 0.045*SL
	t_F	0.33	0.17 + 0.080*SL	0.17 + 0.078*SL	0.16 + 0.080*SL
CK to QN	t_{PLH}	0.82	0.75 + 0.038*SL	0.76 + 0.034*SL	0.76 + 0.034*SL
	t_{PHL}	0.99	0.89 + 0.051*SL	0.90 + 0.046*SL	0.91 + 0.045*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.30	0.15 + 0.079*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
RN to QN	t_{PLH}	0.87	0.80 + 0.038*SL	0.81 + 0.034*SL	0.82 + 0.033*SL
	t_R	0.29	0.16 + 0.064*SL	0.15 + 0.068*SL	0.13 + 0.071*SL

STDM80 FJ2D2

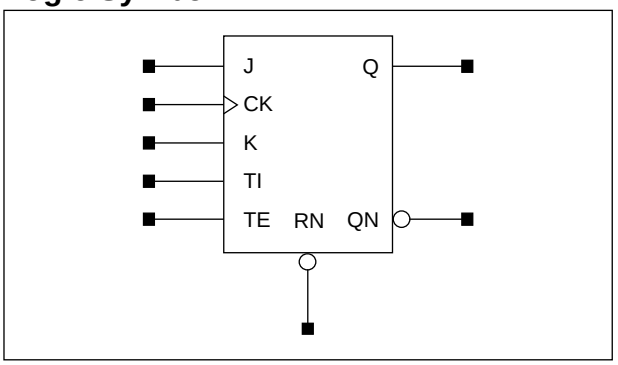
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.38	1.32 + 0.029*SL	1.34 + 0.023*SL	1.36 + 0.020*SL
	t_{PHL}	1.28	1.22 + 0.031*SL	1.23 + 0.026*SL	1.25 + 0.023*SL
	t_R	0.28	0.20 + 0.039*SL	0.21 + 0.035*SL	0.22 + 0.034*SL
	t_F	0.25	0.16 + 0.044*SL	0.18 + 0.039*SL	0.18 + 0.038*SL
RN to Q	t_{PHL}	0.55	0.48 + 0.034*SL	0.50 + 0.028*SL	0.53 + 0.024*SL
	t_F	0.25	0.16 + 0.042*SL	0.18 + 0.038*SL	0.18 + 0.037*SL
CK to QN	t_{PLH}	0.83	0.78 + 0.024*SL	0.79 + 0.020*SL	0.81 + 0.018*SL
	t_{PHL}	0.98	0.92 + 0.031*SL	0.93 + 0.026*SL	0.95 + 0.023*SL
	t_R	0.21	0.14 + 0.032*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.14 + 0.038*SL
RN to QN	t_{PLH}	0.88	0.83 + 0.024*SL	0.84 + 0.020*SL	0.86 + 0.018*SL
	t_R	0.22	0.16 + 0.030*SL	0.15 + 0.032*SL	0.14 + 0.033*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

FJ2S/FJ2SD2

JK Flip-Flop with Reset, Scan, 1X/2X Drive

Logic Symbol



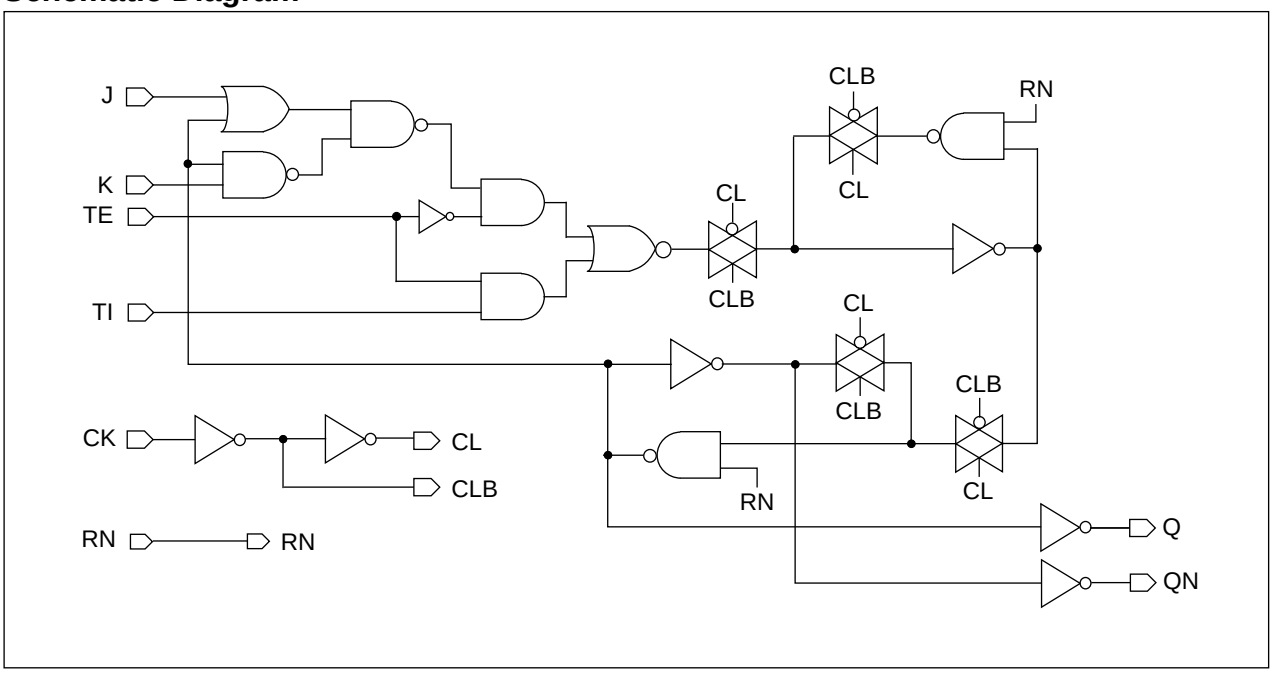
Truth Table

J	CK	K	TI	TE	RN	Q (n+1)	QN (n+1)
0	↑	1	x	0	1	0	1
1	↑	0	x	0	1	1	0
0	↑	0	x	0	1	Q (n)	QN (n)
1	↑	1	x	0	1	QN (n)	Q (n)
x	↓	x	x	0	1	Q (n)	QN (n)
x	x	x	x	x	0	0	1
x	↑	x	0	1	1	0	1
x	↑	x	1	1	1	1	0

Cell Data

Input Load (SL)												Gate Count	
STD80													
FJ2S						*FJ2SD2*						*FJ2S*	*FJ2S D2*
J	CK	K	TI	TE	RN	J	CK	K	TI	TE	RN		
0.5	0.5	0.5	0.5	0.9	0.7	0.5	0.5	0.5	0.5	0.9	0.7	10.3	11.0
STDM80													
FJ2S						*FJ2SD2*						*FJ2S*	*FJ2S D2*
J	CK	K	TI	TE	RN	J	CK	K	TI	TE	RN		
0.6	0.6	0.5	0.4	1.1	1.1	0.6	0.6	0.5	0.4	1.1	1.2	10.3	11.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FJ2S	FJ2SD2	FJ2S	FJ2SD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.98	0.98
Pulse Width High (CK)	t_{PWH}	0.79	0.85	0.82	0.85
Pulse Width High (RN)	t_{PWH}	0.87	0.87	0.90	0.90
Input Setup Time (J to CK)	t_{SU}	0.85	0.85	1.23	1.23
Input Hold Time (J to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.85	0.85	1.23	1.23
Input Hold Time (K to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.66	0.66	0.93	0.93
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.66	0.66	0.85	0.85
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66	0.76	0.76

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FJ2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.73	0.66 + 0.037*SL	0.68 + 0.028*SL	0.72 + 0.024*SL
	t_{PHL}	0.77	0.68 + 0.044*SL	0.69 + 0.039*SL	0.71 + 0.037*SL
	t_R	0.27	0.18 + 0.048*SL	0.18 + 0.048*SL	0.14 + 0.051*SL
	t_F	0.27	0.15 + 0.062*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
RN to Q	t_{PHL}	0.46	0.37 + 0.044*SL	0.38 + 0.038*SL	0.39 + 0.037*SL
	t_F	0.27	0.15 + 0.060*SL	0.14 + 0.064*SL	0.09 + 0.069*SL
CK to QN	t_{PLH}	0.80	0.75 + 0.025*SL	0.75 + 0.024*SL	0.75 + 0.024*SL
	t_{PHL}	0.92	0.85 + 0.037*SL	0.85 + 0.037*SL	0.85 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.23	0.10 + 0.062*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.49	0.44 + 0.025*SL	0.44 + 0.024*SL	0.44 + 0.024*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.049*SL	0.06 + 0.052*SL

STD80 FJ2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.017*SL	0.75 + 0.012*SL
	t_{PHL}	0.75	0.70 + 0.026*SL	0.71 + 0.021*SL	0.74 + 0.018*SL
	t_R	0.24	0.19 + 0.023*SL	0.19 + 0.024*SL	0.18 + 0.025*SL
	t_F	0.21	0.14 + 0.033*SL	0.15 + 0.031*SL	0.12 + 0.033*SL
RN to Q	t_{PHL}	0.44	0.39 + 0.025*SL	0.40 + 0.020*SL	0.42 + 0.018*SL
	t_F	0.20	0.14 + 0.030*SL	0.15 + 0.029*SL	0.11 + 0.034*SL
CK to QN	t_{PLH}	0.87	0.84 + 0.014*SL	0.84 + 0.013*SL	0.85 + 0.012*SL
	t_{PHL}	1.01	0.97 + 0.018*SL	0.97 + 0.017*SL	0.96 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.022*SL	0.08 + 0.026*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.030*SL	0.08 + 0.034*SL
RN to QN	t_{PLH}	0.55	0.53 + 0.013*SL	0.53 + 0.013*SL	0.54 + 0.012*SL
	t_R	0.16	0.11 + 0.022*SL	0.11 + 0.023*SL	0.08 + 0.026*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FJ2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.04	0.94 + 0.050*SL	0.97 + 0.041*SL	1.00 + 0.037*SL
	t_{PHL}	1.09	0.97 + 0.058*SL	1.00 + 0.049*SL	1.02 + 0.045*SL
	t_R	0.36	0.22 + 0.073*SL	0.23 + 0.069*SL	0.24 + 0.068*SL
	t_F	0.35	0.19 + 0.080*SL	0.19 + 0.078*SL	0.18 + 0.080*SL
RN to Q	t_{PHL}	0.60	0.49 + 0.058*SL	0.52 + 0.048*SL	0.54 + 0.045*SL
	t_F	0.34	0.18 + 0.080*SL	0.19 + 0.077*SL	0.18 + 0.079*SL
CK to QN	t_{PLH}	1.15	1.08 + 0.035*SL	1.09 + 0.033*SL	1.09 + 0.033*SL
	t_{PHL}	1.30	1.20 + 0.047*SL	1.21 + 0.045*SL	1.21 + 0.044*SL
	t_R	0.26	0.13 + 0.066*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.29	0.14 + 0.077*SL	0.13 + 0.080*SL	0.12 + 0.082*SL
RN to QN	t_{PLH}	0.67	0.60 + 0.035*SL	0.60 + 0.033*SL	0.61 + 0.033*SL
	t_R	0.26	0.13 + 0.066*SL	0.12 + 0.070*SL	0.11 + 0.072*SL

STDM80 FJ2SD2

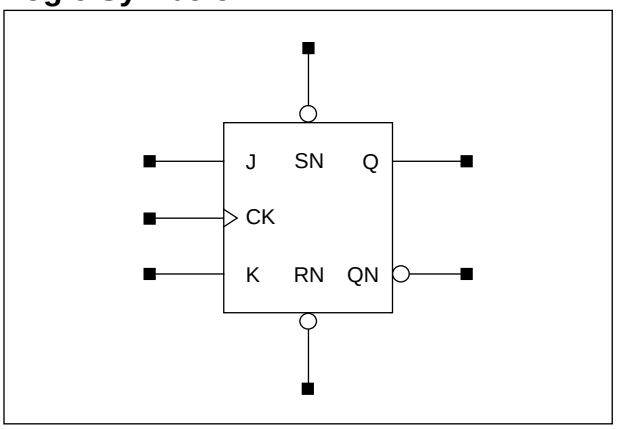
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.05	0.98 + 0.032*SL	1.00 + 0.025*SL	1.03 + 0.021*SL
	t_{PHL}	1.06	0.99 + 0.034*SL	1.01 + 0.029*SL	1.03 + 0.025*SL
	t_R	0.29	0.21 + 0.039*SL	0.22 + 0.036*SL	0.23 + 0.035*SL
	t_F	0.26	0.17 + 0.043*SL	0.18 + 0.040*SL	0.20 + 0.038*SL
RN to Q	t_{PHL}	0.58	0.51 + 0.035*SL	0.53 + 0.028*SL	0.56 + 0.024*SL
	t_F	0.26	0.18 + 0.041*SL	0.19 + 0.038*SL	0.20 + 0.036*SL
CK to QN	t_{PLH}	1.25	1.21 + 0.019*SL	1.21 + 0.018*SL	1.22 + 0.017*SL
	t_{PHL}	1.41	1.36 + 0.024*SL	1.36 + 0.022*SL	1.37 + 0.022*SL
	t_R	0.20	0.14 + 0.031*SL	0.14 + 0.032*SL	0.13 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.037*SL	0.15 + 0.038*SL
RN to QN	t_{PLH}	0.76	0.72 + 0.019*SL	0.72 + 0.018*SL	0.73 + 0.017*SL
	t_R	0.20	0.14 + 0.032*SL	0.14 + 0.032*SL	0.12 + 0.034*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

FJ4/FJ4D2

JK Flip-Flop with Reset, Set, 1X/2X Drive

Logic Symbol5



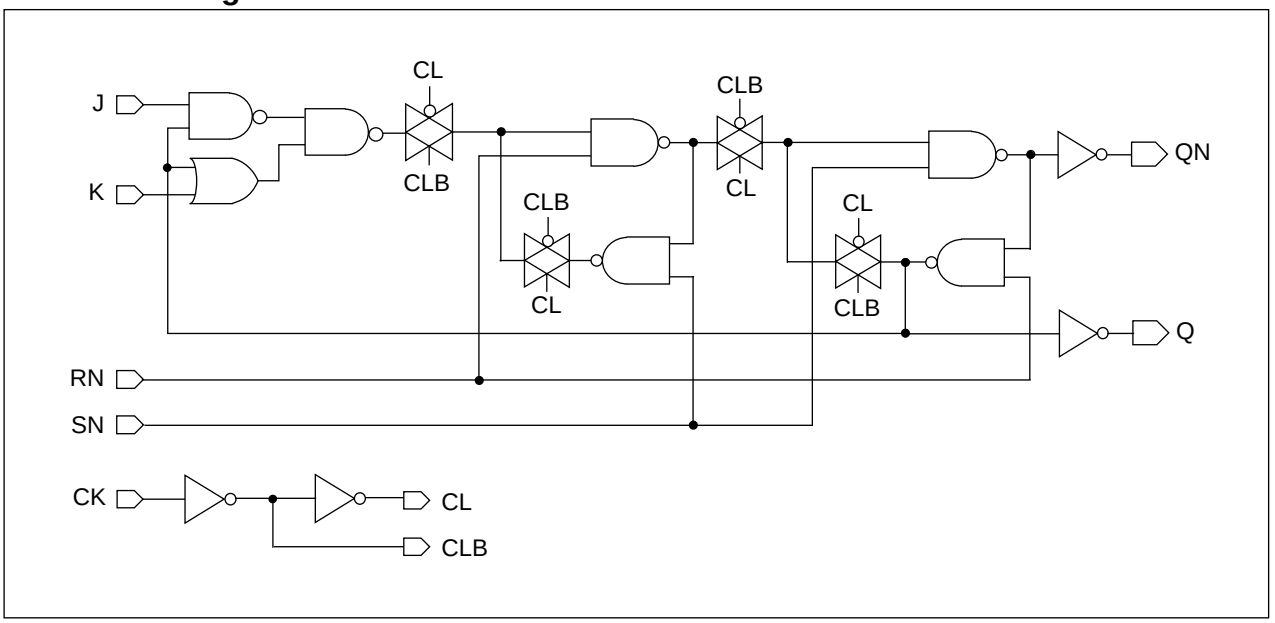
Truth Table

J	CK	K	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	1	0	1
1	↑	0	1	1	1	0
0	↑	0	1	1	Q (n)	QN (n)
1	↑	1	1	1	QN (n)	Q (n)
x	↓	x	1	1	Q (n)	QN (n)
x	x	x	0	1	0	1
x	x	x	1	0	1	0
x	x	x	0	0	0	0

Cell Data

Input Load (SL)										Gate Count	
STD80											
FJ4					*FJ4D2*					*FJ4*	*FJ4D2*
J	CK	K	RN	SN	J	CK	K	RN	SN		
0.3	0.5	0.3	0.7	0.7	0.3	0.5	0.3	0.7	0.7	9.3	10.0
STDM80											
FJ4					*FJ4D2*					*FJ4*	*FJ4D2*
J	CK	K	RN	SN	J	CK	K	RN	SN		
0.6	0.6	0.5	1.6	1.6	0.6	0.6	0.5	1.6	1.6	9.3	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FJ4	FJ4D2	FJ4	FJ4D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.98	0.98
Pulse Width High (CK)	t_{PWH}	0.79	0.85	0.82	0.85
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.87	0.90
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.85	0.93
Input Setup Time (J to CK)	t_{SU}	0.87	0.87	0.90	0.90
Input Hold Time (J to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.87	0.87	0.90	0.90
Input Hold Time (K to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.38	0.38	0.44	0.44
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.71	0.71	0.82	0.82

FJ4/FJ4D2

JK Flip-Flop with Reset, Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FJ4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.93	0.86 + 0.035*SL	0.88 + 0.027*SL	0.91 + 0.024*SL
	t_{PHL}	0.94	0.86 + 0.041*SL	0.87 + 0.037*SL	0.87 + 0.037*SL
	t_R	0.26	0.16 + 0.048*SL	0.16 + 0.048*SL	0.13 + 0.051*SL
	t_F	0.26	0.14 + 0.063*SL	0.13 + 0.065*SL	0.09 + 0.069*SL
RN to Q	t_{PLH}	0.42	0.35 + 0.035*SL	0.37 + 0.027*SL	0.40 + 0.024*SL
	t_{PHL}	0.44	0.35 + 0.043*SL	0.36 + 0.038*SL	0.37 + 0.037*SL
	t_R	0.26	0.16 + 0.048*SL	0.16 + 0.047*SL	0.12 + 0.051*SL
	t_F	0.26	0.13 + 0.063*SL	0.13 + 0.065*SL	0.08 + 0.069*SL
SN to Q	t_{PLH}	0.57	0.51 + 0.034*SL	0.52 + 0.027*SL	0.55 + 0.024*SL
	t_R	0.25	0.16 + 0.047*SL	0.16 + 0.047*SL	0.12 + 0.052*SL
CK to QN	t_{PLH}	0.64	0.58 + 0.032*SL	0.59 + 0.026*SL	0.61 + 0.024*SL
	t_{PHL}	0.73	0.64 + 0.041*SL	0.65 + 0.038*SL	0.66 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to QN	t_{PLH}	0.66	0.59 + 0.032*SL	0.61 + 0.026*SL	0.63 + 0.023*SL
	t_R	0.23	0.14 + 0.048*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
SN to QN	t_{PLH}	0.33	0.27 + 0.032*SL	0.28 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.12 + 0.060*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

STD80 FJ4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.00	0.95 + 0.022*SL	0.96 + 0.016*SL	1.01 + 0.012*SL
	t_{PHL}	1.02	0.97 + 0.023*SL	0.98 + 0.019*SL	0.98 + 0.018*SL
	t_R	0.23	0.18 + 0.025*SL	0.18 + 0.024*SL	0.17 + 0.025*SL
	t_F	0.21	0.15 + 0.031*SL	0.15 + 0.031*SL	0.12 + 0.033*SL
RN to Q	t_{PLH}	0.43	0.38 + 0.023*SL	0.39 + 0.017*SL	0.44 + 0.012*SL
	t_{PHL}	0.43	0.38 + 0.025*SL	0.39 + 0.020*SL	0.41 + 0.018*SL
	t_R	0.22	0.17 + 0.026*SL	0.18 + 0.024*SL	0.16 + 0.025*SL
	t_F	0.20	0.14 + 0.033*SL	0.14 + 0.030*SL	0.11 + 0.034*SL
SN to Q	t_{PLH}	0.64	0.59 + 0.022*SL	0.60 + 0.016*SL	0.65 + 0.012*SL
	t_R	0.22	0.18 + 0.024*SL	0.18 + 0.024*SL	0.16 + 0.025*SL
CK to QN	t_{PLH}	0.65	0.61 + 0.020*SL	0.62 + 0.015*SL	0.66 + 0.012*SL
	t_{PHL}	0.72	0.67 + 0.023*SL	0.68 + 0.020*SL	0.70 + 0.018*SL
	t_R	0.19	0.15 + 0.024*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.030*SL	0.09 + 0.034*SL
RN to QN	t_{PLH}	0.67	0.63 + 0.021*SL	0.64 + 0.015*SL	0.67 + 0.012*SL
	t_R	0.20	0.15 + 0.025*SL	0.16 + 0.023*SL	0.13 + 0.026*SL
SN to QN	t_{PLH}	0.35	0.30 + 0.022*SL	0.32 + 0.015*SL	0.35 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.020*SL	0.33 + 0.018*SL
	t_R	0.19	0.14 + 0.024*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FJ4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.35	1.25 + 0.047*SL	1.27 + 0.040*SL	1.30 + 0.035*SL
	t_{PHL}	1.34	1.24 + 0.053*SL	1.25 + 0.047*SL	1.27 + 0.045*SL
	t_R	0.35	0.20 + 0.071*SL	0.21 + 0.068*SL	0.21 + 0.069*SL
	t_F	0.34	0.18 + 0.081*SL	0.19 + 0.078*SL	0.18 + 0.080*SL
RN to Q	t_{PLH}	0.56	0.47 + 0.048*SL	0.49 + 0.039*SL	0.52 + 0.035*SL
	t_{PHL}	0.58	0.47 + 0.056*SL	0.49 + 0.048*SL	0.51 + 0.045*SL
	t_R	0.34	0.20 + 0.070*SL	0.21 + 0.067*SL	0.20 + 0.069*SL
	t_F	0.33	0.17 + 0.081*SL	0.18 + 0.078*SL	0.17 + 0.080*SL
SN to Q	t_{PLH}	0.80	0.70 + 0.047*SL	0.73 + 0.039*SL	0.75 + 0.035*SL
	t_R	0.34	0.21 + 0.069*SL	0.21 + 0.067*SL	0.20 + 0.069*SL
CK to QN	t_{PLH}	0.92	0.83 + 0.043*SL	0.85 + 0.037*SL	0.86 + 0.034*SL
	t_{PHL}	1.03	0.92 + 0.051*SL	0.94 + 0.046*SL	0.95 + 0.045*SL
	t_R	0.31	0.18 + 0.069*SL	0.18 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.14 + 0.081*SL
RN to QN	t_{PLH}	0.94	0.85 + 0.044*SL	0.88 + 0.037*SL	0.90 + 0.034*SL
	t_R	0.32	0.18 + 0.067*SL	0.18 + 0.067*SL	0.17 + 0.070*SL
SN to QN	t_{PLH}	0.44	0.35 + 0.043*SL	0.37 + 0.036*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.050*SL	0.38 + 0.046*SL	0.39 + 0.045*SL
	t_R	0.30	0.17 + 0.069*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.13 + 0.081*SL	0.13 + 0.082*SL

STDM80 FJ4D2

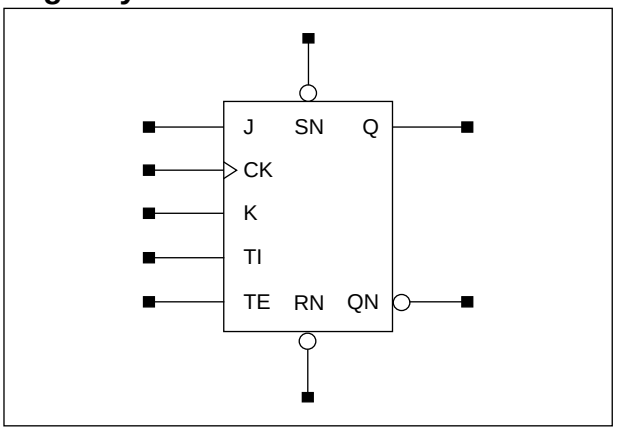
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.43	1.37 + 0.029*SL	1.39 + 0.024*SL	1.41 + 0.020*SL
	t_{PHL}	1.44	1.38 + 0.030*SL	1.39 + 0.026*SL	1.41 + 0.023*SL
	t_R	0.28	0.20 + 0.040*SL	0.22 + 0.035*SL	0.22 + 0.034*SL
	t_F	0.26	0.18 + 0.043*SL	0.19 + 0.039*SL	0.20 + 0.038*SL
RN to Q	t_{PLH}	0.57	0.51 + 0.031*SL	0.53 + 0.025*SL	0.55 + 0.021*SL
	t_{PHL}	0.56	0.49 + 0.034*SL	0.51 + 0.028*SL	0.54 + 0.024*SL
	t_R	0.28	0.20 + 0.039*SL	0.21 + 0.035*SL	0.22 + 0.034*SL
	t_F	0.25	0.17 + 0.041*SL	0.18 + 0.039*SL	0.18 + 0.037*SL
SN to Q	t_{PLH}	0.88	0.82 + 0.029*SL	0.84 + 0.023*SL	0.86 + 0.020*SL
	t_R	0.28	0.20 + 0.038*SL	0.21 + 0.036*SL	0.22 + 0.034*SL
CK to QN	t_{PLH}	0.93	0.87 + 0.028*SL	0.89 + 0.022*SL	0.91 + 0.019*SL
	t_{PHL}	1.02	0.96 + 0.031*SL	0.97 + 0.026*SL	0.99 + 0.023*SL
	t_R	0.25	0.18 + 0.035*SL	0.18 + 0.035*SL	0.19 + 0.034*SL
	t_F	0.23	0.15 + 0.040*SL	0.16 + 0.037*SL	0.15 + 0.038*SL
RN to QN	t_{PLH}	0.96	0.90 + 0.028*SL	0.92 + 0.023*SL	0.94 + 0.019*SL
	t_R	0.25	0.18 + 0.035*SL	0.19 + 0.034*SL	0.19 + 0.033*SL
SN to QN	t_{PLH}	0.45	0.39 + 0.027*SL	0.41 + 0.022*SL	0.43 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

FJ4S/FJ4SD2

JK Flip-Flop with Reset, Set, Scan, 1X/2X Drive

Logic Symbol



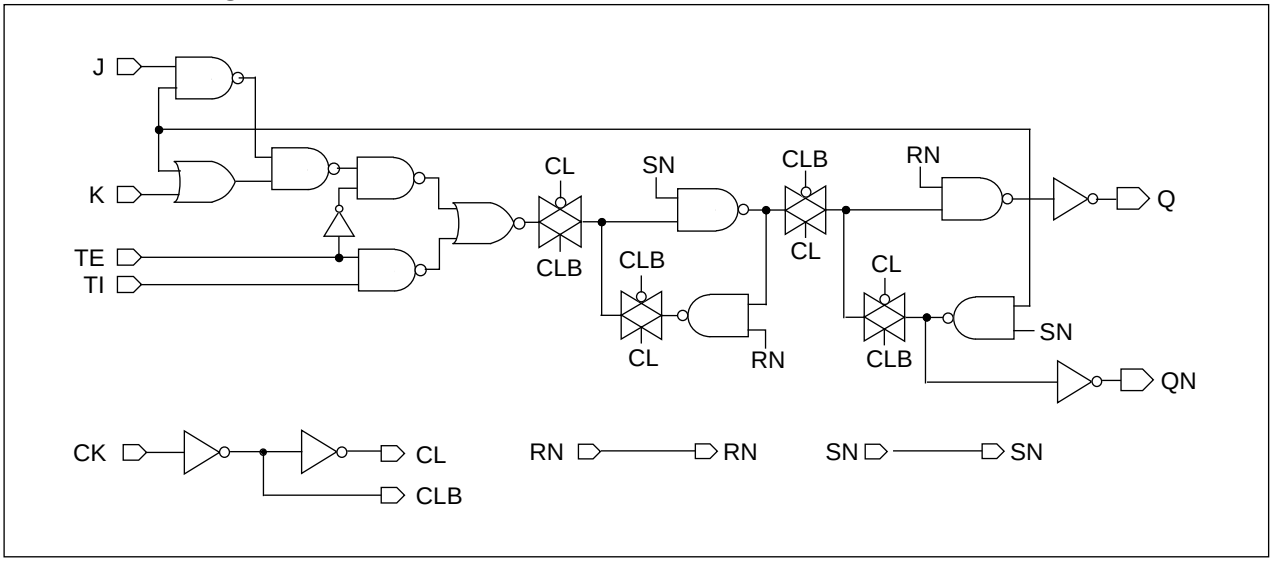
Truth Table

J	CK	K	TI	TE	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	x	0	1	1	0	1
1	↑	0	x	0	1	1	1	0
0	↑	0	x	0	1	1	Q (n)	QN (n)
1	↑	1	x	0	1	1	QN (n)	Q (n)
x	↓	x	x	0	1	1	Q (n)	QN (n)
x	x	x	x	x	0	1	0	1
x	x	x	x	x	1	0	1	0
x	x	x	x	x	0	0	0	0
x	↑	x	0	1	1	1	0	1
x	↑	x	1	1	1	1	1	0

Cell Data

Input Load (SL)														Gate Count	
STD80															
FJ4S							*FJ4SD2*							*FJ4S*	*FJ4S D2*
J	CK	K	TI	TE	RN	SN	J	CK	K	TI	TE	RN	SN		
0.3	0.5	0.3	0.4	0.9	0.7	0.9	0.3	0.5	0.3	0.4	0.9	0.7	0.9	11.7	12.3
STDM80															
FJ4S							*FJ4SD2*							*FJ4S*	*FJ4S D2*
J	CK	K	TI	TE	RN	SN	J	CK	K	TI	TE	RN	SN		
0.6	0.6	0.5	0.4	1.1	1.7	1.6	0.6	0.6	0.5	0.4	1.1	1.7	1.6	11.7	12.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FJ4S	FJ4SD2	FJ4S	FJ4SD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	1.04	1.04
Pulse Width High (CK)	t_{PWH}	0.82	0.85	0.82	0.87
Pulse Width High (RN)	t_{PWH}	0.87	0.87	0.90	0.93
Pulse Width High (SN)	t_{PWH}	0.87	0.87	0.98	0.98
Input Setup Time (J to CK)	t_{SU}	0.90	0.90	1.28	1.28
Input Hold Time (J to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.90	0.90	1.28	1.28
Input Hold Time (K to CK)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.33	0.33	0.98	0.98
Input Hold Time (TI to CK)	t_{HD}	0.71	0.71	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.68	0.68	0.93	0.93
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71	0.82	0.82
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.38	0.38	0.44	0.44

FJ4S/FJ4SD2

JK Flip-Flop with Reset, Set, Scan, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FJ4S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.74	0.67 + 0.037*SL	0.69 + 0.028*SL	0.73 + 0.024*SL
	t_{PHL}	0.82	0.73 + 0.044*SL	0.74 + 0.039*SL	0.76 + 0.037*SL
	t_R	0.27	0.18 + 0.048*SL	0.18 + 0.048*SL	0.15 + 0.051*SL
	t_F	0.27	0.15 + 0.063*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
RN to Q	t_{PLH}	0.43	0.36 + 0.036*SL	0.38 + 0.027*SL	0.42 + 0.024*SL
	t_{PHL}	0.46	0.37 + 0.043*SL	0.38 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.27	0.17 + 0.048*SL	0.17 + 0.047*SL	0.13 + 0.051*SL
	t_F	0.27	0.14 + 0.064*SL	0.14 + 0.064*SL	0.09 + 0.069*SL
SN to Q	t_{PLH}	0.76	0.69 + 0.037*SL	0.71 + 0.028*SL	0.75 + 0.024*SL
	t_R	0.27	0.18 + 0.044*SL	0.17 + 0.047*SL	0.13 + 0.051*SL
CK to QN	t_{PLH}	0.94	0.88 + 0.030*SL	0.89 + 0.025*SL	0.90 + 0.024*SL
	t_{PHL}	0.96	0.88 + 0.038*SL	0.88 + 0.037*SL	0.88 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.58	0.53 + 0.029*SL	0.53 + 0.025*SL	0.55 + 0.024*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
SN to QN	t_{PLH}	0.30	0.24 + 0.031*SL	0.25 + 0.025*SL	0.27 + 0.024*SL
	t_{PHL}	0.37	0.29 + 0.040*SL	0.29 + 0.037*SL	0.30 + 0.037*SL
	t_R	0.22	0.13 + 0.047*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

STD80 FJ4SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.75	0.70 + 0.024*SL	0.71 + 0.017*SL	0.77 + 0.012*SL
	t_{PHL}	0.80	0.75 + 0.027*SL	0.76 + 0.021*SL	0.79 + 0.018*SL
	t_R	0.24	0.19 + 0.025*SL	0.19 + 0.024*SL	0.18 + 0.025*SL
	t_F	0.22	0.15 + 0.033*SL	0.15 + 0.031*SL	0.13 + 0.033*SL
RN to Q	t_{PLH}	0.44	0.39 + 0.023*SL	0.40 + 0.017*SL	0.45 + 0.012*SL
	t_{PHL}	0.44	0.39 + 0.025*SL	0.40 + 0.020*SL	0.43 + 0.018*SL
	t_R	0.23	0.18 + 0.026*SL	0.18 + 0.024*SL	0.17 + 0.025*SL
	t_F	0.21	0.14 + 0.033*SL	0.15 + 0.030*SL	0.11 + 0.034*SL
SN to Q	t_{PLH}	0.77	0.72 + 0.024*SL	0.74 + 0.017*SL	0.79 + 0.012*SL
	t_R	0.24	0.18 + 0.026*SL	0.19 + 0.024*SL	0.17 + 0.025*SL
CK to QN	t_{PLH}	1.02	0.98 + 0.018*SL	0.99 + 0.014*SL	1.02 + 0.012*SL
	t_{PHL}	1.04	1.00 + 0.020*SL	1.00 + 0.017*SL	1.00 + 0.018*SL
	t_R	0.20	0.15 + 0.023*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.19	0.13 + 0.030*SL	0.13 + 0.030*SL	0.09 + 0.034*SL
RN to QN	t_{PLH}	0.66	0.62 + 0.018*SL	0.63 + 0.014*SL	0.65 + 0.012*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
SN to QN	t_{PLH}	0.32	0.28 + 0.019*SL	0.29 + 0.015*SL	0.32 + 0.012*SL
	t_{PHL}	0.37	0.32 + 0.023*SL	0.33 + 0.019*SL	0.34 + 0.018*SL
	t_R	0.19	0.14 + 0.022*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FJ4S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.06	0.96 + 0.050*SL	0.99 + 0.041*SL	1.02 + 0.037*SL
	t_{PHL}	1.16	1.04 + 0.057*SL	1.07 + 0.049*SL	1.09 + 0.046*SL
	t_R	0.37	0.22 + 0.072*SL	0.23 + 0.069*SL	0.24 + 0.068*SL
	t_F	0.35	0.19 + 0.081*SL	0.19 + 0.079*SL	0.19 + 0.080*SL
RN to Q	t_{PLH}	0.58	0.48 + 0.049*SL	0.51 + 0.040*SL	0.54 + 0.035*SL
	t_{PHL}	0.60	0.49 + 0.057*SL	0.52 + 0.049*SL	0.54 + 0.045*SL
	t_R	0.35	0.21 + 0.071*SL	0.22 + 0.067*SL	0.21 + 0.068*SL
	t_F	0.34	0.18 + 0.082*SL	0.19 + 0.079*SL	0.18 + 0.079*SL
SN to Q	t_{PLH}	1.09	0.99 + 0.049*SL	1.02 + 0.040*SL	1.05 + 0.035*SL
	t_R	0.36	0.22 + 0.070*SL	0.23 + 0.067*SL	0.22 + 0.068*SL
CK to QN	t_{PLH}	1.37	1.28 + 0.041*SL	1.30 + 0.036*SL	1.31 + 0.034*SL
	t_{PHL}	1.36	1.26 + 0.049*SL	1.27 + 0.045*SL	1.28 + 0.044*SL
	t_R	0.31	0.17 + 0.067*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.31	0.15 + 0.078*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
RN to QN	t_{PLH}	0.81	0.73 + 0.041*SL	0.75 + 0.036*SL	0.76 + 0.034*SL
	t_R	0.30	0.17 + 0.067*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
SN to QN	t_{PLH}	0.42	0.34 + 0.042*SL	0.35 + 0.036*SL	0.37 + 0.034*SL
	t_{PHL}	0.48	0.38 + 0.051*SL	0.39 + 0.046*SL	0.40 + 0.045*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.069*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.080*SL	0.13 + 0.081*SL	0.12 + 0.082*SL

STDM80 FJ4SD2

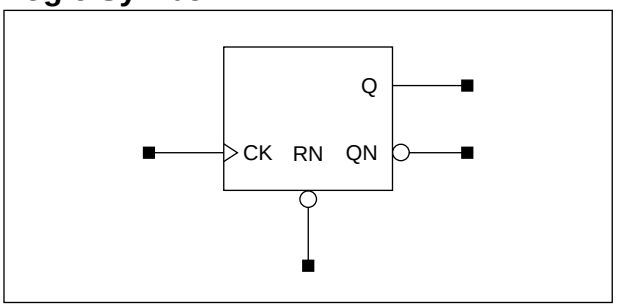
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.06	1.00 + 0.032*SL	1.02 + 0.025*SL	1.04 + 0.022*SL
	t_{PHL}	1.14	1.07 + 0.035*SL	1.09 + 0.028*SL	1.11 + 0.025*SL
	t_R	0.30	0.22 + 0.038*SL	0.23 + 0.036*SL	0.23 + 0.035*SL
	t_F	0.27	0.18 + 0.042*SL	0.19 + 0.039*SL	0.20 + 0.038*SL
RN to Q	t_{PLH}	0.58	0.51 + 0.031*SL	0.53 + 0.025*SL	0.56 + 0.021*SL
	t_{PHL}	0.58	0.51 + 0.035*SL	0.53 + 0.029*SL	0.56 + 0.024*SL
	t_R	0.28	0.21 + 0.037*SL	0.21 + 0.036*SL	0.22 + 0.034*SL
	t_F	0.26	0.17 + 0.042*SL	0.18 + 0.039*SL	0.19 + 0.037*SL
SN to Q	t_{PLH}	1.10	1.03 + 0.032*SL	1.06 + 0.025*SL	1.08 + 0.021*SL
	t_R	0.29	0.21 + 0.040*SL	0.23 + 0.035*SL	0.24 + 0.034*SL
CK to QN	t_{PLH}	1.48	1.43 + 0.024*SL	1.44 + 0.020*SL	1.45 + 0.019*SL
	t_{PHL}	1.46	1.41 + 0.026*SL	1.42 + 0.023*SL	1.43 + 0.022*SL
	t_R	0.25	0.18 + 0.036*SL	0.18 + 0.034*SL	0.19 + 0.034*SL
	t_F	0.24	0.15 + 0.041*SL	0.16 + 0.038*SL	0.16 + 0.037*SL
RN to QN	t_{PLH}	0.92	0.87 + 0.024*SL	0.88 + 0.020*SL	0.89 + 0.019*SL
	t_R	0.25	0.17 + 0.038*SL	0.18 + 0.034*SL	0.18 + 0.033*SL
SN to QN	t_{PLH}	0.44	0.38 + 0.027*SL	0.40 + 0.022*SL	0.42 + 0.019*SL
	t_{PHL}	0.47	0.41 + 0.031*SL	0.43 + 0.026*SL	0.45 + 0.023*SL
	t_R	0.24	0.16 + 0.037*SL	0.17 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

FT2/FT2D2

Toggle Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



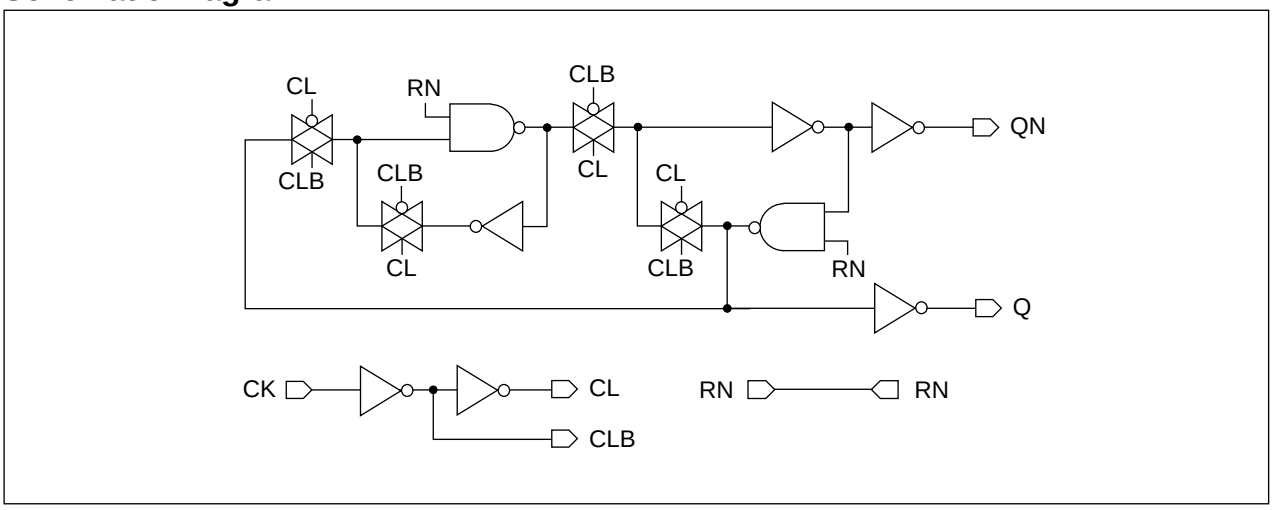
Truth Table

CK	RN	Q (n+1)	QN (n+1)
⎍	1	QN (n)	Q (n)
x	0	0	1

Cell Data

Input Load (SL)				Gate Count	
STD80					
FT2		*FT2D2*		*FT2*	*FT2D2*
CK	RN	CK	RN		
0.5	0.7	0.5	0.9	6.3	7.0
STDM80					
FT2		*FT2D2*		*FT2*	*FT2D2*
CK	RN	CK	RN		
0.6	1.3	0.6	1.3	6.3	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FT2	FT2D2	FT2	FT2D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.90	0.87
Pulse Width High (CK)	t_{PWH}	0.79	0.85	0.90	0.85
Pulse Width High (RN)	t_{PWH}	0.87	0.87	0.82	0.85
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.38	0.38	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FT2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.86	0.79 + 0.033*SL	0.81 + 0.026*SL	0.83 + 0.024*SL
	t_{PHL}	0.83	0.75 + 0.040*SL	0.75 + 0.037*SL	0.75 + 0.037*SL
	t_R	0.23	0.14 + 0.047*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.12 + 0.064*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PHL}	0.39	0.31 + 0.041*SL	0.31 + 0.038*SL	0.32 + 0.037*SL
	t_F	0.24	0.12 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
CK to QN	t_{PLH}	0.58	0.52 + 0.028*SL	0.53 + 0.024*SL	0.54 + 0.024*SL
	t_{PHL}	0.70	0.61 + 0.042*SL	0.62 + 0.038*SL	0.63 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.24	0.11 + 0.065*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
RN to QN	t_{PLH}	0.61	0.55 + 0.029*SL	0.56 + 0.024*SL	0.57 + 0.023*SL
	t_R	0.21	0.12 + 0.046*SL	0.11 + 0.048*SL	0.07 + 0.052*SL

STD80 FT2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.93	0.89 + 0.019*SL	0.90 + 0.015*SL	0.93 + 0.012*SL
	t_{PHL}	0.88	0.83 + 0.022*SL	0.84 + 0.019*SL	0.84 + 0.018*SL
	t_R	0.21	0.16 + 0.023*SL	0.16 + 0.023*SL	0.14 + 0.026*SL
	t_F	0.19	0.12 + 0.032*SL	0.13 + 0.031*SL	0.10 + 0.034*SL
RN to Q	t_{PHL}	0.38	0.34 + 0.023*SL	0.34 + 0.020*SL	0.36 + 0.018*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
CK to QN	t_{PLH}	0.58	0.55 + 0.018*SL	0.56 + 0.014*SL	0.57 + 0.012*SL
	t_{PHL}	0.69	0.64 + 0.023*SL	0.65 + 0.020*SL	0.67 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.030*SL	0.08 + 0.034*SL
RN to QN	t_{PLH}	0.61	0.58 + 0.018*SL	0.59 + 0.013*SL	0.60 + 0.012*SL
	t_R	0.17	0.13 + 0.020*SL	0.12 + 0.022*SL	0.09 + 0.026*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

FT2/FT2D2

Toggle Flip-Flop with Reset, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FT2

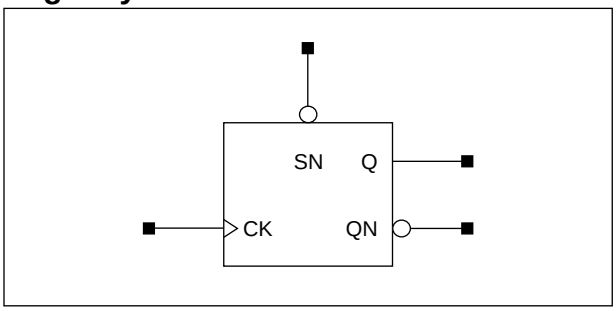
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.25	1.16 + 0.044*SL	1.18 + 0.037*SL	1.20 + 0.034*SL
	t_{PHL}	1.18	1.07 + 0.052*SL	1.09 + 0.046*SL	1.10 + 0.045*SL
	t_R	0.32	0.18 + 0.070*SL	0.19 + 0.068*SL	0.18 + 0.069*SL
	t_F	0.32	0.16 + 0.081*SL	0.16 + 0.079*SL	0.15 + 0.080*SL
RN to Q	t_{PHL}	0.51	0.41 + 0.054*SL	0.43 + 0.047*SL	0.44 + 0.045*SL
	t_F	0.31	0.15 + 0.082*SL	0.15 + 0.080*SL	0.15 + 0.081*SL
CK to QN	t_{PLH}	0.83	0.75 + 0.038*SL	0.76 + 0.034*SL	0.77 + 0.034*SL
	t_{PHL}	0.99	0.88 + 0.051*SL	0.90 + 0.046*SL	0.91 + 0.045*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.070*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.13 + 0.082*SL
RN to QN	t_{PLH}	0.87	0.79 + 0.038*SL	0.81 + 0.034*SL	0.81 + 0.033*SL
	t_R	0.29	0.16 + 0.064*SL	0.15 + 0.068*SL	0.13 + 0.071*SL

STDM80 FT2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.34	1.28 + 0.027*SL	1.30 + 0.022*SL	1.31 + 0.020*SL
	t_{PHL}	1.24	1.18 + 0.030*SL	1.20 + 0.025*SL	1.21 + 0.023*SL
	t_R	0.26	0.19 + 0.038*SL	0.20 + 0.034*SL	0.20 + 0.034*SL
	t_F	0.24	0.15 + 0.042*SL	0.16 + 0.039*SL	0.17 + 0.038*SL
RN to Q	t_{PHL}	0.50	0.44 + 0.032*SL	0.45 + 0.027*SL	0.48 + 0.024*SL
	t_F	0.23	0.14 + 0.043*SL	0.16 + 0.039*SL	0.16 + 0.038*SL
CK to QN	t_{PLH}	0.83	0.78 + 0.024*SL	0.79 + 0.020*SL	0.81 + 0.017*SL
	t_{PHL}	0.98	0.92 + 0.031*SL	0.93 + 0.026*SL	0.95 + 0.023*SL
	t_R	0.21	0.15 + 0.032*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.22	0.14 + 0.041*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
RN to QN	t_{PLH}	0.87	0.83 + 0.024*SL	0.84 + 0.020*SL	0.86 + 0.017*SL
	t_R	0.22	0.15 + 0.033*SL	0.15 + 0.032*SL	0.14 + 0.033*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



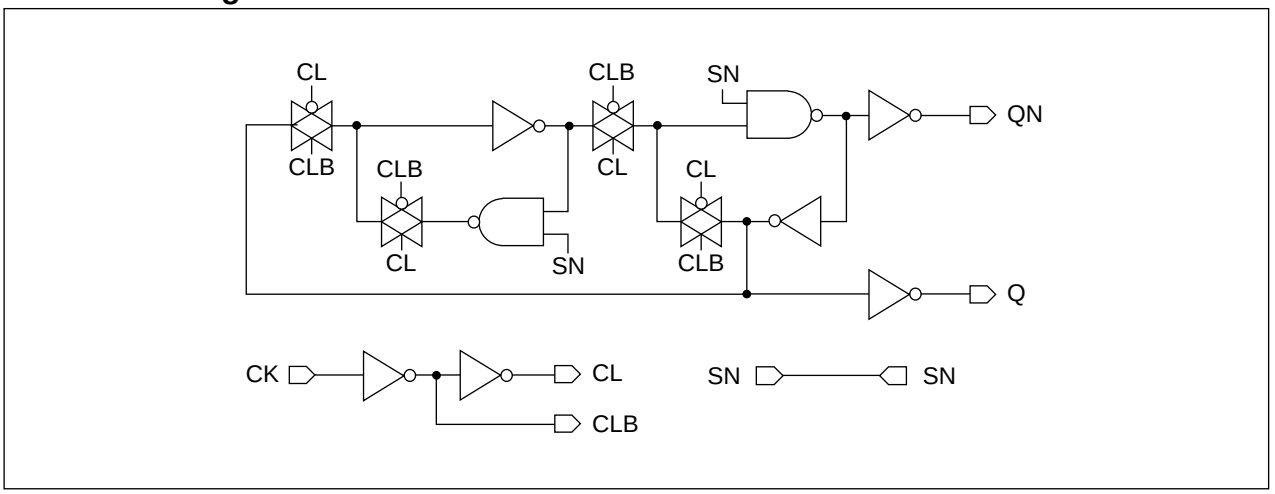
Truth Table

CK	SN	Q (n+1)	QN (n+1)
⎍	1	QN (n)	Q (n)
x	0	1	0

Cell Data

Input Load (SL)				Gate Count	
STD80					
FT3		*FT3D2*		*FT3*	*FT3D2*
CK	SN	CK	SN		
0.5	0.7	0.5	0.7	6.0	6.7
STDM80					
FT3		*FT3D2*		*FT3*	*FT3D2*
CK	SN	CK	SN		
0.6	1.4	0.6	1.4	6.0	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		FT3	FT3D2	FT3	FT3D2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87	0.87	0.85
Pulse Width High (CK)	t_{PWH}	0.82	0.87	0.93	0.90
Pulse Width High (SN)	t_{PWH}	0.87	0.87	0.82	0.87
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.66	0.66	0.76	0.76

FT3/FT3D2

Toggle Flip-Flop with Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FT3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.76	0.71 + 0.026*SL	0.71 + 0.024*SL	0.71 + 0.024*SL
	t_{PHL}	0.85	0.77 + 0.038*SL	0.78 + 0.037*SL	0.78 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
SN to Q	t_{PLH}	0.45	0.39 + 0.026*SL	0.40 + 0.024*SL	0.40 + 0.023*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
CK to QN	t_{PLH}	0.63	0.57 + 0.032*SL	0.58 + 0.026*SL	0.60 + 0.024*SL
	t_{PHL}	0.68	0.60 + 0.041*SL	0.60 + 0.038*SL	0.61 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to QN	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.30 + 0.037*SL
	t_F	0.24	0.11 + 0.065*SL	0.11 + 0.066*SL	0.08 + 0.069*SL

STD80 FT3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.79 + 0.015*SL	0.80 + 0.013*SL	0.81 + 0.012*SL
	t_{PHL}	0.93	0.89 + 0.018*SL	0.89 + 0.018*SL	0.89 + 0.018*SL
	t_R	0.16	0.12 + 0.023*SL	0.12 + 0.022*SL	0.08 + 0.026*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
SN to Q	t_{PLH}	0.51	0.48 + 0.015*SL	0.48 + 0.013*SL	0.49 + 0.012*SL
	t_R	0.16	0.12 + 0.023*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
CK to QN	t_{PLH}	0.64	0.60 + 0.021*SL	0.61 + 0.015*SL	0.65 + 0.012*SL
	t_{PHL}	0.67	0.62 + 0.023*SL	0.63 + 0.020*SL	0.65 + 0.018*SL
	t_R	0.20	0.15 + 0.023*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.18	0.11 + 0.031*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
SN to QN	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.020*SL	0.33 + 0.018*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FT3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.09	1.02 + 0.037*SL	1.03 + 0.034*SL	1.03 + 0.033*SL
	t_{PHL}	1.21	1.11 + 0.049*SL	1.12 + 0.045*SL	1.13 + 0.044*SL
	t_R	0.27	0.14 + 0.066*SL	0.13 + 0.069*SL	0.11 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
SN to Q	t_{PLH}	0.60	0.53 + 0.037*SL	0.54 + 0.034*SL	0.54 + 0.033*SL
	t_R	0.27	0.14 + 0.066*SL	0.13 + 0.069*SL	0.11 + 0.071*SL
CK to QN	t_{PLH}	0.90	0.82 + 0.043*SL	0.83 + 0.037*SL	0.85 + 0.035*SL
	t_{PHL}	0.96	0.86 + 0.051*SL	0.87 + 0.047*SL	0.89 + 0.045*SL
	t_R	0.31	0.18 + 0.069*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
SN to QN	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.047*SL	0.39 + 0.045*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.081*SL	0.13 + 0.082*SL

STDM80 FT3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.18	1.14 + 0.020*SL	1.15 + 0.018*SL	1.15 + 0.017*SL
	t_{PHL}	1.31	1.26 + 0.027*SL	1.27 + 0.023*SL	1.28 + 0.022*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.23	0.15 + 0.042*SL	0.16 + 0.038*SL	0.16 + 0.038*SL
SN to Q	t_{PLH}	0.69	0.65 + 0.020*SL	0.66 + 0.018*SL	0.66 + 0.017*SL
	t_R	0.21	0.14 + 0.034*SL	0.14 + 0.033*SL	0.14 + 0.033*SL
CK to QN	t_{PLH}	0.92	0.86 + 0.028*SL	0.88 + 0.022*SL	0.90 + 0.019*SL
	t_{PHL}	0.95	0.89 + 0.031*SL	0.90 + 0.026*SL	0.92 + 0.023*SL
	t_R	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.22	0.15 + 0.038*SL	0.15 + 0.038*SL	0.14 + 0.038*SL
SN to QN	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_F	0.21	0.13 + 0.042*SL	0.14 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

LATCHES

Cell List

Cell Name	Function Description
LD1	D Latch with Active High
LD1D2	D Latch with Active High, 2X Drive
LD1S	D Latch with Active High, Scan
LD1SD2	D Latch with Active High, Scan, 2X Drive
LD1Q	D Latch with Active High, Q Output Only
LD1QD2	D Latch with Active High, Q Output Only, 2X Drive
LD1X4	4-Bit D Latch with Active High
LD1X4D2	4-Bit D Latch with Active High, 2X Drive
YLD1	Fast D Latch with Active High
YLD1D2	Fast D Latch with Active High, 2X Drive
LD1A	D Latch with Active High, Tri-State Output
LD1B	D Latch with Active High, Tri-State Output, Separate WR, WRN
LD2	D Latch with Active High, Reset
LD2D2	D Latch with Active High, Reset, 2X Drive
LD2Q	D Latch with Active High, Reset, Q Output Only
LD2QD2	D Latch with Active High, Reset, Q Output Only, 2X Drive
YLD2	Fast D Latch with Active High, Reset
YLD2D2	Fast D Latch with Active High, Reset, 2X Drive
LD3	D Latch with Active High, Set
LD3D2	D Latch with Active High, Set, 2X Drive
LD4	D Latch with Active High, Reset, Set
LD4D2	D Latch with Active High, Reset, Set, 2X Drive
LD5	D Latch with Active Low
LD5D2	D Latch with Active Low, 2X Drive
LD5S	D Latch with Active Low, Scan
LD5SD2	D Latch with Active Low, Scan, 2X Drive
LD5X4	4-Bit D Latch with Active Low
LD5X4D2	4-Bit D Latch with Active Low, 2X Drive
LD6	D Latch with Active Low, Reset
LD6D2	D Latch with Active Low, Reset, 2X Drive
LD7	D Latch with Active Low, Set
LD7D2	D Latch with Active Low, Set, 2X Drive
LD8	D Latch with Active Low, Reset, Set
LD8D2	D Latch with Active Low, Reset, Set, 2X Drive

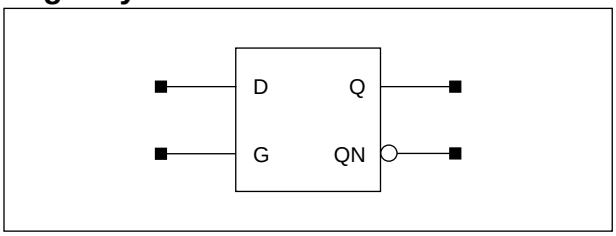
Cell List (Continued)

Cell Name	Function Description
LDS2	D Latch with Active High, Synchronous Clear
LDS6	D Latch with Active Low, Synchronous Clear
LS0	SR Latch
LS0D2	SR Latch with 2X Drive
LS1	SR Latch with Separate Inputs
LS2	SR Latch with Common Inputs

LD1/LD1D2

D Latch with Active High, 1X/2X Drive

Logic Symbol



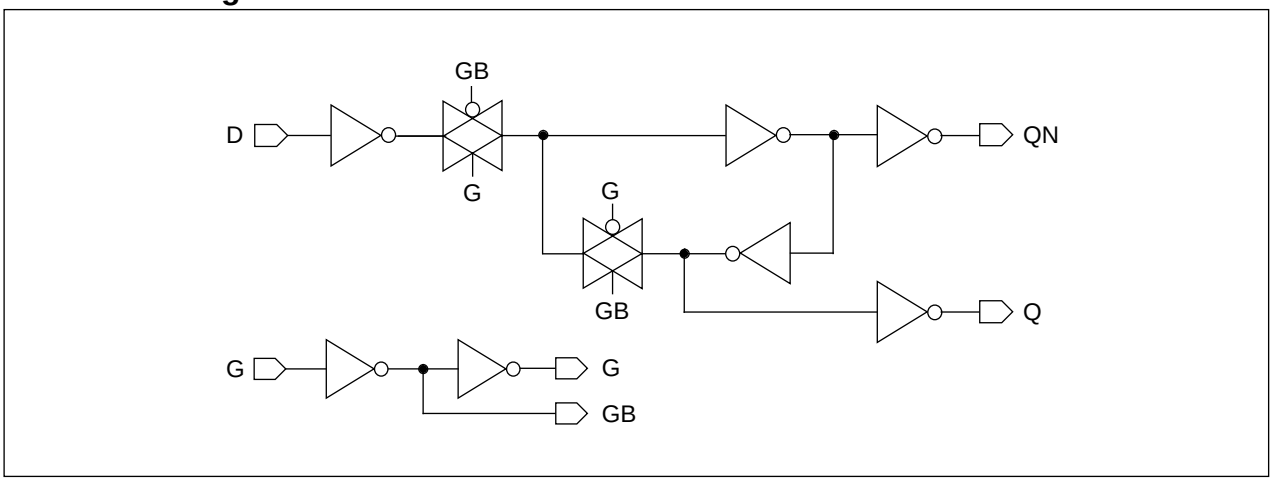
Truth Table

D	G	Q (n+1)	QN (n+1)
0	1	0	1
1	1	1	0
x	0	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
STD80					
LD1		*LD1D2*		*LD1*	*LD1D2*
D	G	D	G		
0.5	0.5	0.5	0.5	4.0	4.7
STDM80					
LD1		*LD1D2*		*LD1*	*LD1D2*
D	G	D	G		
0.6	0.6	0.6	0.6	4.0	4.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD1	LD1D2	LD1	LD1D2
Pulse Width High (G)	t_{PWH}	0.79	0.79	0.82	0.82
Input Setup Time (D to G)	t_{SU}	0.66	0.71	0.66	0.71
Input Hold Time (D to G)	t_{HD}	0.33	0.33	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.51	0.46 + 0.025*SL	0.46 + 0.024*SL	0.46 + 0.024*SL
	t_{PHL}	0.70	0.62 + 0.038*SL	0.62 + 0.037*SL	0.62 + 0.037*SL
	t_R	0.18	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
G to Q	t_{PLH}	0.62	0.57 + 0.025*SL	0.57 + 0.024*SL	0.57 + 0.024*SL
	t_{PHL}	0.69	0.62 + 0.038*SL	0.62 + 0.037*SL	0.62 + 0.037*SL
	t_R	0.18	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
D to QN	t_{PLH}	0.53	0.47 + 0.028*SL	0.48 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.47	0.39 + 0.041*SL	0.40 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
G to QN	t_{PLH}	0.53	0.47 + 0.028*SL	0.48 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.58	0.50 + 0.042*SL	0.51 + 0.038*SL	0.52 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

STD80 LD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.57	0.54 + 0.014*SL	0.55 + 0.012*SL	0.55 + 0.012*SL
	t_{PHL}	0.75	0.72 + 0.018*SL	0.72 + 0.018*SL	0.71 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
G to Q	t_{PLH}	0.69	0.66 + 0.013*SL	0.66 + 0.012*SL	0.67 + 0.012*SL
	t_{PHL}	0.75	0.71 + 0.018*SL	0.71 + 0.018*SL	0.71 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D to QN	t_{PLH}	0.53	0.50 + 0.018*SL	0.51 + 0.014*SL	0.52 + 0.012*SL
	t_{PHL}	0.46	0.41 + 0.023*SL	0.42 + 0.020*SL	0.44 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
G to QN	t_{PLH}	0.53	0.50 + 0.018*SL	0.51 + 0.014*SL	0.52 + 0.012*SL
	t_{PHL}	0.57	0.53 + 0.023*SL	0.53 + 0.020*SL	0.55 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.10 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

LD1/LD1D2

D Latch with Active High, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD1

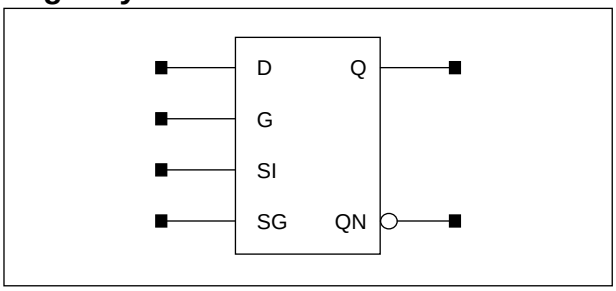
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.72	0.65 + 0.035*SL	0.65 + 0.033*SL	0.66 + 0.033*SL
	t_{PHL}	0.96	0.87 + 0.046*SL	0.87 + 0.045*SL	0.88 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
G to Q	t_{PLH}	0.90	0.83 + 0.035*SL	0.84 + 0.033*SL	0.84 + 0.033*SL
	t_{PHL}	1.00	0.91 + 0.047*SL	0.92 + 0.045*SL	0.92 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D to QN	t_{PLH}	0.74	0.66 + 0.038*SL	0.67 + 0.035*SL	0.68 + 0.034*SL
	t_{PHL}	0.65	0.55 + 0.052*SL	0.56 + 0.046*SL	0.58 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
G to QN	t_{PLH}	0.78	0.70 + 0.038*SL	0.71 + 0.035*SL	0.72 + 0.034*SL
	t_{PHL}	0.83	0.73 + 0.052*SL	0.74 + 0.046*SL	0.76 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

STDM80 LD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.81	0.77 + 0.018*SL	0.77 + 0.017*SL	0.78 + 0.017*SL
	t_{PHL}	1.04	0.99 + 0.026*SL	0.99 + 0.023*SL	1.00 + 0.022*SL
	t_R	0.19	0.13 + 0.033*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
G to Q	t_{PLH}	0.99	0.95 + 0.019*SL	0.96 + 0.017*SL	0.96 + 0.017*SL
	t_{PHL}	1.08	1.03 + 0.026*SL	1.04 + 0.023*SL	1.05 + 0.022*SL
	t_R	0.19	0.13 + 0.030*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D to QN	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.020*SL	0.72 + 0.018*SL
	t_{PHL}	0.64	0.58 + 0.030*SL	0.59 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.15 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
G to QN	t_{PLH}	0.78	0.73 + 0.024*SL	0.74 + 0.020*SL	0.76 + 0.018*SL
	t_{PHL}	0.82	0.76 + 0.031*SL	0.77 + 0.026*SL	0.79 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.14 + 0.038*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Logic Symbol



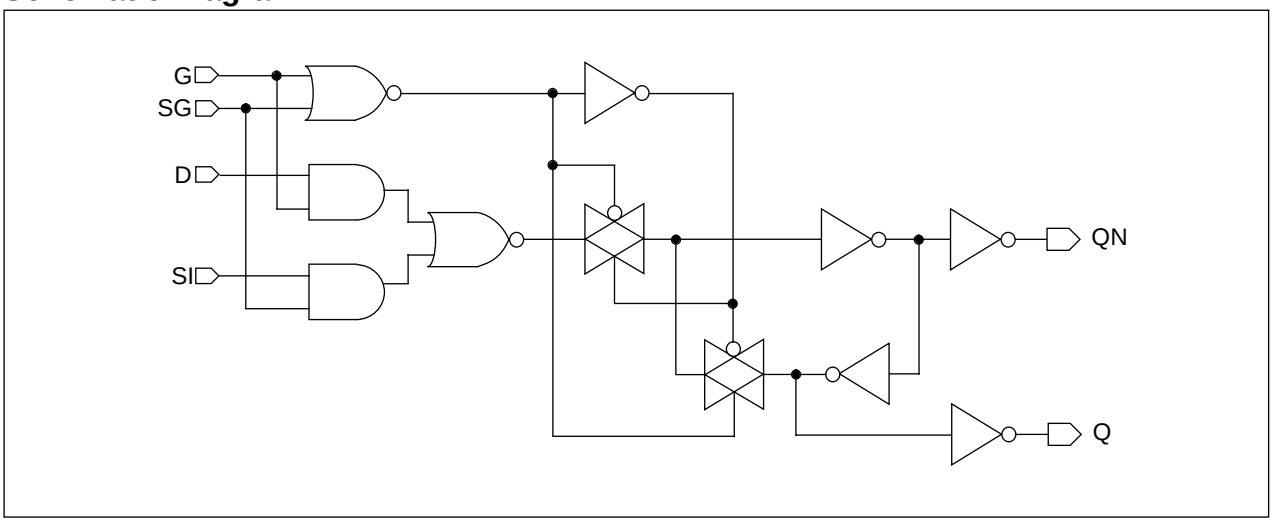
Truth Table

D	G	SI	SG	Q (n+1)	QN (n+1)
x	0	x	0	Q (n)	QN (n)
x	x	1	1	1	0
x	0	0	1	0	1
1	1	x	x	1	0
0	1	x	0	0	1
0	1	0	1	0	1

Cell Data

Input Load (SL)								Gate Count	
STD80									
LD1S				*LD1SD2*				*LD1S*	*LD1SD2*
D	G	SI	SG	D	G	SI	SG		
0.3	0.6	0.4	0.9	0.3	0.6	0.4	0.9	5.7	6.3
STDM80									
LD1S				*LD1SD2*				*LD1S*	*LD1SD2*
D	G	SI	SG	D	G	SI	SG		
0.4	1.3	0.4	1.1	0.4	1.3	0.4	1.1	5.7	6.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD1S	LD1SD2	LD1S	LD1SD2
Pulse Width High (G)	t_{PWH}	0.87	0.96	0.90	0.96
Pulse Width High (SG)	t_{PWH}	0.90	0.96	0.93	0.96
Input Setup Time (D to G)	t_{SU}	0.76	0.63	0.76	0.82
Input Hold Time (D to G)	t_{HD}	0.37	0.33	0.33	0.33
Input Setup Time (SI to SG)	t_{SU}	0.74	0.63	0.74	0.82
Input Hold Time (SI to SG)	t_{HD}	0.37	0.33	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.62	0.57 + 0.025*SL	0.57 + 0.024*SL	0.57 + 0.024*SL
	t_{PHL}	0.79	0.72 + 0.037*SL	0.72 + 0.037*SL	0.72 + 0.037*SL
	t_R	0.18	0.09 + 0.045*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
SI to Q	t_{PLH}	0.68	0.63 + 0.025*SL	0.63 + 0.024*SL	0.63 + 0.024*SL
	t_{PHL}	0.85	0.78 + 0.037*SL	0.78 + 0.037*SL	0.77 + 0.037*SL
	t_R	0.18	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
G to Q	t_{PLH}	0.69	0.64 + 0.025*SL	0.64 + 0.024*SL	0.64 + 0.024*SL
	t_{PHL}	0.73	0.66 + 0.037*SL	0.66 + 0.037*SL	0.66 + 0.037*SL
	t_R	0.18	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
SG to Q	t_{PLH}	0.73	0.68 + 0.025*SL	0.68 + 0.024*SL	0.68 + 0.024*SL
	t_{PHL}	0.74	0.67 + 0.038*SL	0.67 + 0.037*SL	0.67 + 0.037*SL
	t_R	0.18	0.09 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
D to QN	t_{PLH}	0.62	0.56 + 0.029*SL	0.57 + 0.024*SL	0.58 + 0.024*SL
	t_{PHL}	0.58	0.50 + 0.041*SL	0.51 + 0.038*SL	0.51 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
SI to QN	t_{PLH}	0.68	0.62 + 0.029*SL	0.63 + 0.024*SL	0.64 + 0.024*SL
	t_{PHL}	0.64	0.56 + 0.041*SL	0.57 + 0.038*SL	0.58 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
G to QN	t_{PLH}	0.56	0.51 + 0.028*SL	0.51 + 0.025*SL	0.52 + 0.024*SL
	t_{PHL}	0.65	0.57 + 0.042*SL	0.58 + 0.038*SL	0.59 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SG to QN	t_{PLH}	0.58	0.52 + 0.028*SL	0.53 + 0.025*SL	0.53 + 0.024*SL
	t_{PHL}	0.69	0.61 + 0.042*SL	0.62 + 0.038*SL	0.62 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.69	0.66 + 0.013*SL	0.66 + 0.012*SL	0.67 + 0.012*SL
	t_{PHL}	0.85	0.82 + 0.018*SL	0.82 + 0.018*SL	0.81 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.033*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
SI to Q	t_{PLH}	0.75	0.72 + 0.013*SL	0.72 + 0.012*SL	0.73 + 0.012*SL
	t_{PHL}	0.91	0.88 + 0.018*SL	0.88 + 0.018*SL	0.87 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.034*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
G to Q	t_{PLH}	0.76	0.73 + 0.013*SL	0.73 + 0.012*SL	0.74 + 0.012*SL
	t_{PHL}	0.79	0.75 + 0.018*SL	0.75 + 0.018*SL	0.75 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
SG to Q	t_{PLH}	0.80	0.77 + 0.013*SL	0.77 + 0.012*SL	0.78 + 0.012*SL
	t_{PHL}	0.80	0.77 + 0.018*SL	0.77 + 0.018*SL	0.76 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D to QN	t_{PLH}	0.63	0.59 + 0.018*SL	0.60 + 0.014*SL	0.62 + 0.012*SL
	t_{PHL}	0.57	0.53 + 0.023*SL	0.53 + 0.020*SL	0.55 + 0.018*SL
	t_R	0.17	0.13 + 0.021*SL	0.13 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.12 + 0.029*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SI to QN	t_{PLH}	0.69	0.65 + 0.018*SL	0.66 + 0.014*SL	0.68 + 0.012*SL
	t_{PHL}	0.64	0.59 + 0.023*SL	0.60 + 0.020*SL	0.61 + 0.018*SL
	t_R	0.18	0.13 + 0.022*SL	0.13 + 0.022*SL	0.10 + 0.026*SL
	t_F	0.18	0.12 + 0.030*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
G to QN	t_{PLH}	0.57	0.53 + 0.018*SL	0.54 + 0.014*SL	0.56 + 0.012*SL
	t_{PHL}	0.65	0.60 + 0.023*SL	0.61 + 0.020*SL	0.62 + 0.018*SL
	t_R	0.17	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SG to QN	t_{PLH}	0.58	0.55 + 0.018*SL	0.56 + 0.014*SL	0.57 + 0.012*SL
	t_{PHL}	0.68	0.64 + 0.023*SL	0.64 + 0.020*SL	0.66 + 0.018*SL
	t_R	0.17	0.12 + 0.022*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.09 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.88	0.81 + 0.035*SL	0.81 + 0.033*SL	0.81 + 0.033*SL
	t_{PHL}	1.15	1.06 + 0.046*SL	1.06 + 0.045*SL	1.07 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
SI to Q	t_{PLH}	0.96	0.89 + 0.035*SL	0.89 + 0.033*SL	0.89 + 0.033*SL
	t_{PHL}	1.26	1.16 + 0.046*SL	1.17 + 0.045*SL	1.17 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
G to Q	t_{PLH}	1.00	0.93 + 0.035*SL	0.93 + 0.033*SL	0.93 + 0.033*SL
	t_{PHL}	1.06	0.96 + 0.046*SL	0.97 + 0.045*SL	0.97 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
SG to Q	t_{PLH}	1.04	0.97 + 0.034*SL	0.97 + 0.033*SL	0.97 + 0.033*SL
	t_{PHL}	1.06	0.96 + 0.047*SL	0.97 + 0.045*SL	0.98 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D to QN	t_{PLH}	0.92	0.84 + 0.040*SL	0.86 + 0.035*SL	0.87 + 0.034*SL
	t_{PHL}	0.81	0.70 + 0.052*SL	0.72 + 0.046*SL	0.73 + 0.044*SL
	t_R	0.30	0.17 + 0.065*SL	0.16 + 0.068*SL	0.14 + 0.070*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.13 + 0.082*SL
SI to QN	t_{PLH}	1.03	0.95 + 0.040*SL	0.96 + 0.035*SL	0.97 + 0.033*SL
	t_{PHL}	0.89	0.78 + 0.052*SL	0.80 + 0.047*SL	0.81 + 0.044*SL
	t_R	0.30	0.17 + 0.065*SL	0.16 + 0.068*SL	0.14 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
G to QN	t_{PLH}	0.83	0.75 + 0.039*SL	0.76 + 0.035*SL	0.77 + 0.034*SL
	t_{PHL}	0.93	0.83 + 0.052*SL	0.84 + 0.046*SL	0.86 + 0.044*SL
	t_R	0.29	0.15 + 0.067*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.078*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
SG to QN	t_{PLH}	0.83	0.75 + 0.039*SL	0.77 + 0.035*SL	0.78 + 0.034*SL
	t_{PHL}	0.97	0.87 + 0.052*SL	0.88 + 0.046*SL	0.90 + 0.044*SL
	t_R	0.29	0.15 + 0.066*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.14 + 0.081*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD1SD2

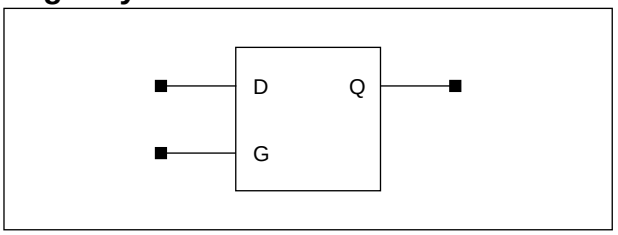
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.97	0.93 + 0.018*SL	0.94 + 0.017*SL	0.94 + 0.017*SL
	t_{PHL}	1.24	1.19 + 0.025*SL	1.20 + 0.023*SL	1.20 + 0.021*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
SI to Q	t_{PLH}	1.05	1.01 + 0.018*SL	1.02 + 0.017*SL	1.02 + 0.017*SL
	t_{PHL}	1.35	1.30 + 0.025*SL	1.30 + 0.023*SL	1.31 + 0.021*SL
	t_R	0.19	0.13 + 0.033*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.21	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
G to Q	t_{PLH}	1.09	1.06 + 0.018*SL	1.06 + 0.017*SL	1.06 + 0.017*SL
	t_{PHL}	1.14	1.09 + 0.025*SL	1.09 + 0.023*SL	1.10 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
SG to Q	t_{PLH}	1.13	1.10 + 0.018*SL	1.10 + 0.017*SL	1.11 + 0.017*SL
	t_{PHL}	1.14	1.09 + 0.025*SL	1.10 + 0.023*SL	1.11 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D to QN	t_{PLH}	0.93	0.88 + 0.024*SL	0.90 + 0.020*SL	0.91 + 0.018*SL
	t_{PHL}	0.80	0.73 + 0.031*SL	0.75 + 0.026*SL	0.77 + 0.023*SL
	t_R	0.23	0.16 + 0.032*SL	0.16 + 0.033*SL	0.16 + 0.033*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
SI to QN	t_{PLH}	1.04	0.99 + 0.025*SL	1.00 + 0.020*SL	1.02 + 0.018*SL
	t_{PHL}	0.88	0.82 + 0.031*SL	0.83 + 0.026*SL	0.85 + 0.023*SL
	t_R	0.23	0.17 + 0.032*SL	0.17 + 0.032*SL	0.16 + 0.033*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
G to QN	t_{PLH}	0.83	0.78 + 0.024*SL	0.80 + 0.020*SL	0.81 + 0.018*SL
	t_{PHL}	0.92	0.86 + 0.031*SL	0.87 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.22	0.15 + 0.032*SL	0.15 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.14 + 0.041*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
SG to QN	t_{PLH}	0.84	0.79 + 0.024*SL	0.80 + 0.020*SL	0.82 + 0.018*SL
	t_{PHL}	0.96	0.90 + 0.031*SL	0.91 + 0.026*SL	0.93 + 0.023*SL
	t_R	0.22	0.15 + 0.033*SL	0.15 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

LD1Q/LD1QD2

D Latch with Active High, Q Output Only, 1X/2X Drive

Logic Symbol



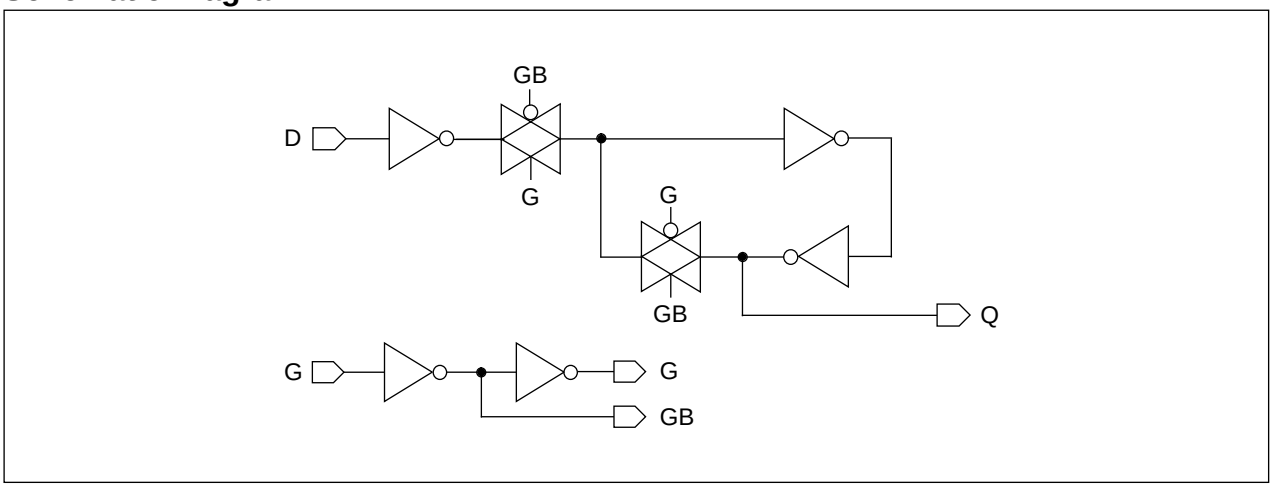
Truth Table

D	G	Q (n+1)
0	1	0
1	1	1
x	0	Q (n)

Cell Data

Input Load (SL)				Gate Count	
STD80					
LD1Q		*LD1QD2*		*LD1Q*	*LD1QD2*
D	G	D	G		
0.3	0.6	0.3	0.6	3.7	4.0
STDM80					
LD1Q		*LD1QD2*		*LD1Q*	*LD1QD2*
D	G	D	G		
0.9	0.9	0.9	0.9	3.7	4.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD1Q	LD1QD2	LD1Q	LD1QD2
Pulse Width High (G)	t_{PWH}	0.87	0.87	0.82	0.82
Input Setup Time (D to G)	t_{SU}	0.46	0.49	0.55	0.57
Input Hold Time (D to G)	t_{HD}	0.33	0.33	0.35	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD1Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.48	0.43 + 0.026*SL	0.43 + 0.024*SL	0.43 + 0.024*SL
	t_{PHL}	0.60	0.52 + 0.039*SL	0.53 + 0.037*SL	0.53 + 0.037*SL
	t_R	0.18	0.09 + 0.048*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
G to Q	t_{PLH}	0.59	0.54 + 0.025*SL	0.54 + 0.024*SL	0.54 + 0.024*SL
	t_{PHL}	0.60	0.52 + 0.039*SL	0.53 + 0.037*SL	0.53 + 0.037*SL
	t_R	0.18	0.09 + 0.046*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.068*SL	0.07 + 0.069*SL

STD80 LD1QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.49	0.45 + 0.016*SL	0.46 + 0.013*SL	0.47 + 0.012*SL
	t_{PHL}	0.60	0.55 + 0.022*SL	0.56 + 0.019*SL	0.57 + 0.018*SL
	t_R	0.14	0.10 + 0.024*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.15	0.09 + 0.029*SL	0.09 + 0.032*SL	0.07 + 0.034*SL
G to Q	t_{PLH}	0.60	0.57 + 0.017*SL	0.57 + 0.013*SL	0.58 + 0.012*SL
	t_{PHL}	0.60	0.55 + 0.022*SL	0.56 + 0.019*SL	0.57 + 0.018*SL
	t_R	0.14	0.10 + 0.023*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.15	0.09 + 0.030*SL	0.09 + 0.032*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

LD1Q/LD1QD2

D Latch with Active High, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD1Q

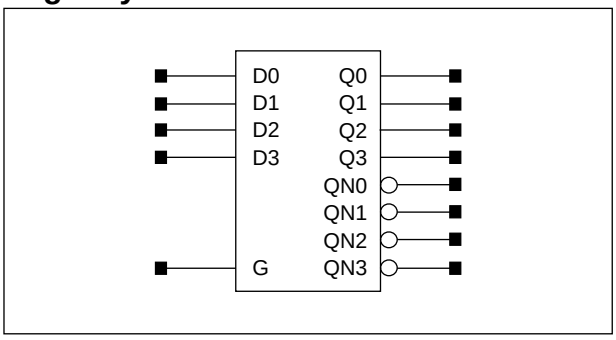
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.68	0.61 + 0.035*SL	0.61 + 0.033*SL	0.61 + 0.033*SL
	t_{PHL}	0.83	0.73 + 0.048*SL	0.74 + 0.045*SL	0.74 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.071*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.080*SL	0.11 + 0.081*SL	0.10 + 0.083*SL
G to Q	t_{PLH}	0.86	0.79 + 0.035*SL	0.80 + 0.034*SL	0.80 + 0.033*SL
	t_{PHL}	0.87	0.77 + 0.048*SL	0.78 + 0.045*SL	0.79 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.080*SL	0.11 + 0.081*SL	0.11 + 0.082*SL

STDM80 LD1QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.68	0.64 + 0.022*SL	0.65 + 0.019*SL	0.66 + 0.017*SL
	t_{PHL}	0.82	0.77 + 0.029*SL	0.78 + 0.024*SL	0.79 + 0.022*SL
	t_R	0.18	0.12 + 0.033*SL	0.12 + 0.034*SL	0.11 + 0.034*SL
	t_F	0.20	0.11 + 0.040*SL	0.12 + 0.038*SL	0.12 + 0.039*SL
G to Q	t_{PLH}	0.87	0.82 + 0.022*SL	0.83 + 0.018*SL	0.84 + 0.017*SL
	t_{PHL}	0.87	0.81 + 0.029*SL	0.82 + 0.025*SL	0.84 + 0.022*SL
	t_R	0.18	0.12 + 0.033*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.19	0.12 + 0.040*SL	0.12 + 0.038*SL	0.12 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

Dn	G	Qn (n+1)	QNn (n+1)
0	1	0	1
1	1	1	0
x	0	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count	
STD80					
LD1X4		*LD1X4D2*		*LD1X4*	*LD1X4D2*
Dn	G	Dn	G		
0.5	0.5	0.5	0.5	13.0	15.3
STDM80					
LD1X4		*LD1X4D2*		*LD1X4*	*LD1X4D2*
Dn	G	Dn	G		
0.6	0.6	0.6	0.6	13.0	15.3

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD1X4	LD1X4D2	LD1X4	LD1X4D2
Pulse Width High (G)	t_{PWH}	0.79	0.82	0.82	0.82
Input Setup Time (D0 to G)	t_{SU}	0.44	0.57	0.52	0.55
Input Hold Time (D0 to G)	t_{HD}	0.55	0.55	0.60	0.55
Input Setup Time (D1 to G)	t_{SU}	0.44	0.00	0.52	0.57
Input Hold Time (D1 to G)	t_{HD}	0.55	0.49	0.60	0.55
Input Setup Time (D2 to G)	t_{SU}	0.44	0.57	0.52	0.55
Input Hold Time (D2 to G)	t_{HD}	0.55	0.55	0.60	0.55
Input Setup Time (D3 to G)	t_{SU}	0.44	0.00	0.52	0.55
Input Hold Time (D3 to G)	t_{HD}	0.55	0.55	0.60	7.30

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.51	0.46 + 0.025*SL	0.46 + 0.024*SL	0.46 + 0.024*SL
	t_{PHL}	0.70	0.62 + 0.038*SL	0.62 + 0.037*SL	0.62 + 0.037*SL
	t_R	0.18	0.09 + 0.047*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
G to Q0	t_{PLH}	0.86	0.81 + 0.025*SL	0.81 + 0.024*SL	0.81 + 0.024*SL
	t_{PHL}	0.82	0.74 + 0.038*SL	0.75 + 0.037*SL	0.75 + 0.037*SL
	t_R	0.18	0.09 + 0.047*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
D1 to Q1	t_{PLH}	0.51	0.46 + 0.026*SL	0.46 + 0.023*SL	0.46 + 0.024*SL
	t_{PHL}	0.70	0.63 + 0.037*SL	0.63 + 0.037*SL	0.63 + 0.037*SL
	t_R	0.19	0.09 + 0.046*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
G to Q1	t_{PLH}	0.86	0.81 + 0.025*SL	0.81 + 0.024*SL	0.81 + 0.024*SL
	t_{PHL}	0.82	0.75 + 0.037*SL	0.75 + 0.037*SL	0.75 + 0.037*SL
	t_R	0.19	0.09 + 0.047*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
D2 to Q2	t_{PLH}	0.51	0.46 + 0.025*SL	0.46 + 0.024*SL	0.46 + 0.024*SL
	t_{PHL}	0.70	0.63 + 0.038*SL	0.63 + 0.037*SL	0.63 + 0.037*SL
	t_R	0.19	0.09 + 0.047*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
G to Q2	t_{PLH}	0.86	0.81 + 0.025*SL	0.81 + 0.024*SL	0.81 + 0.024*SL
	t_{PHL}	0.82	0.75 + 0.038*SL	0.75 + 0.037*SL	0.75 + 0.037*SL
	t_R	0.19	0.09 + 0.047*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
D3 to Q3	t_{PLH}	0.51	0.46 + 0.026*SL	0.46 + 0.024*SL	0.46 + 0.024*SL
	t_{PHL}	0.70	0.62 + 0.038*SL	0.62 + 0.037*SL	0.62 + 0.037*SL
	t_R	0.18	0.09 + 0.045*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
G to Q3	t_{PLH}	0.85	0.80 + 0.025*SL	0.81 + 0.024*SL	0.81 + 0.024*SL
	t_{PHL}	0.83	0.75 + 0.038*SL	0.75 + 0.037*SL	0.75 + 0.037*SL
	t_R	0.18	0.09 + 0.047*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
D0 to QN0	t_{PLH}	0.53	0.47 + 0.028*SL	0.48 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.47	0.39 + 0.042*SL	0.40 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
G to QN0	t_{PLH}	0.65	0.60 + 0.028*SL	0.60 + 0.024*SL	0.61 + 0.024*SL
	t_{PHL}	0.82	0.74 + 0.041*SL	0.74 + 0.038*SL	0.75 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.53	0.47 + 0.028*SL	0.48 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.47	0.39 + 0.041*SL	0.40 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
G to QN1	t_{PLH}	0.66	0.60 + 0.028*SL	0.61 + 0.024*SL	0.61 + 0.024*SL
	t_{PHL}	0.82	0.74 + 0.042*SL	0.74 + 0.038*SL	0.75 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
D2 to QN2	t_{PLH}	0.53	0.47 + 0.028*SL	0.48 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.47	0.39 + 0.042*SL	0.40 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
G to QN2	t_{PLH}	0.66	0.60 + 0.028*SL	0.61 + 0.024*SL	0.61 + 0.024*SL
	t_{PHL}	0.82	0.74 + 0.042*SL	0.74 + 0.038*SL	0.75 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
D3 to QN3	t_{PLH}	0.53	0.47 + 0.028*SL	0.48 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.47	0.39 + 0.042*SL	0.40 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
G to QN3	t_{PLH}	0.66	0.60 + 0.027*SL	0.61 + 0.024*SL	0.62 + 0.024*SL
	t_{PHL}	0.82	0.74 + 0.041*SL	0.74 + 0.038*SL	0.75 + 0.037*SL
	t_R	0.20	0.11 + 0.047*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD1X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.57	0.54 + 0.014*SL	0.55 + 0.012*SL	0.55 + 0.012*SL
	t_{PHL}	0.75	0.71 + 0.019*SL	0.72 + 0.018*SL	0.71 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
G to Q0	t_{PLH}	0.93	0.90 + 0.013*SL	0.90 + 0.012*SL	0.91 + 0.012*SL
	t_{PHL}	0.88	0.84 + 0.019*SL	0.84 + 0.018*SL	0.84 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D1 to Q1	t_{PLH}	0.57	0.55 + 0.013*SL	0.55 + 0.012*SL	0.56 + 0.012*SL
	t_{PHL}	0.76	0.72 + 0.018*SL	0.72 + 0.018*SL	0.72 + 0.018*SL
	t_R	0.15	0.11 + 0.019*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.029*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
G to Q1	t_{PLH}	0.93	0.90 + 0.013*SL	0.91 + 0.012*SL	0.91 + 0.012*SL
	t_{PHL}	0.88	0.84 + 0.018*SL	0.85 + 0.018*SL	0.84 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D2 to Q2	t_{PLH}	0.57	0.55 + 0.014*SL	0.55 + 0.012*SL	0.56 + 0.012*SL
	t_{PHL}	0.76	0.72 + 0.019*SL	0.72 + 0.018*SL	0.72 + 0.018*SL
	t_R	0.15	0.11 + 0.019*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.029*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
G to Q2	t_{PLH}	0.93	0.90 + 0.014*SL	0.91 + 0.012*SL	0.91 + 0.012*SL
	t_{PHL}	0.88	0.84 + 0.019*SL	0.85 + 0.018*SL	0.84 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D3 to Q3	t_{PLH}	0.57	0.54 + 0.014*SL	0.55 + 0.012*SL	0.55 + 0.012*SL
	t_{PHL}	0.75	0.72 + 0.018*SL	0.72 + 0.018*SL	0.71 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
G to Q3	t_{PLH}	0.93	0.90 + 0.013*SL	0.90 + 0.012*SL	0.91 + 0.012*SL
	t_{PHL}	0.88	0.85 + 0.019*SL	0.85 + 0.018*SL	0.85 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D0 to QN0	t_{PLH}	0.54	0.50 + 0.018*SL	0.51 + 0.013*SL	0.52 + 0.012*SL
	t_{PHL}	0.46	0.41 + 0.023*SL	0.42 + 0.020*SL	0.44 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.033*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
G to QN0	t_{PLH}	0.66	0.63 + 0.018*SL	0.64 + 0.014*SL	0.65 + 0.012*SL
	t_{PHL}	0.82	0.77 + 0.023*SL	0.78 + 0.020*SL	0.79 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD1X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.54	0.50 + 0.018*SL	0.51 + 0.013*SL	0.52 + 0.012*SL
	t_{PHL}	0.46	0.41 + 0.023*SL	0.42 + 0.020*SL	0.44 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
G to QN1	t_{PLH}	0.66	0.63 + 0.018*SL	0.64 + 0.014*SL	0.65 + 0.012*SL
	t_{PHL}	0.82	0.77 + 0.023*SL	0.78 + 0.020*SL	0.79 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
D2 to QN2	t_{PLH}	0.54	0.50 + 0.018*SL	0.51 + 0.013*SL	0.52 + 0.012*SL
	t_{PHL}	0.46	0.41 + 0.023*SL	0.42 + 0.020*SL	0.44 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.033*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
G to QN2	t_{PLH}	0.66	0.63 + 0.018*SL	0.64 + 0.014*SL	0.65 + 0.012*SL
	t_{PHL}	0.82	0.77 + 0.023*SL	0.78 + 0.020*SL	0.79 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
D3 to QN3	t_{PLH}	0.54	0.50 + 0.018*SL	0.51 + 0.013*SL	0.52 + 0.012*SL
	t_{PHL}	0.46	0.41 + 0.023*SL	0.42 + 0.020*SL	0.44 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.033*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
G to QN3	t_{PLH}	0.67	0.63 + 0.018*SL	0.64 + 0.013*SL	0.66 + 0.012*SL
	t_{PHL}	0.81	0.77 + 0.023*SL	0.77 + 0.020*SL	0.79 + 0.018*SL
	t_R	0.16	0.12 + 0.022*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.72	0.65 + 0.035*SL	0.65 + 0.033*SL	0.65 + 0.033*SL
	t_{PHL}	0.96	0.87 + 0.047*SL	0.87 + 0.045*SL	0.88 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.10 + 0.083*SL
G to Q0	t_{PLH}	1.23	1.16 + 0.035*SL	1.16 + 0.033*SL	1.16 + 0.033*SL
	t_{PHL}	1.14	1.05 + 0.047*SL	1.06 + 0.045*SL	1.06 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D1 to Q1	t_{PLH}	0.72	0.65 + 0.035*SL	0.66 + 0.033*SL	0.66 + 0.033*SL
	t_{PHL}	0.97	0.87 + 0.047*SL	0.88 + 0.045*SL	0.88 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.28	0.13 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.083*SL
G to Q1	t_{PLH}	1.23	1.16 + 0.035*SL	1.17 + 0.033*SL	1.17 + 0.033*SL
	t_{PHL}	1.15	1.06 + 0.047*SL	1.06 + 0.045*SL	1.07 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.28	0.13 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D2 to Q2	t_{PLH}	0.72	0.65 + 0.035*SL	0.66 + 0.033*SL	0.66 + 0.033*SL
	t_{PHL}	0.97	0.87 + 0.046*SL	0.88 + 0.045*SL	0.88 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.28	0.13 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.083*SL
G to Q2	t_{PLH}	1.23	1.16 + 0.035*SL	1.17 + 0.033*SL	1.17 + 0.033*SL
	t_{PHL}	1.15	1.06 + 0.047*SL	1.06 + 0.045*SL	1.07 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.28	0.12 + 0.080*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D3 to Q3	t_{PLH}	0.72	0.65 + 0.035*SL	0.65 + 0.033*SL	0.65 + 0.033*SL
	t_{PHL}	0.96	0.87 + 0.047*SL	0.87 + 0.045*SL	0.88 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
G to Q3	t_{PLH}	1.22	1.16 + 0.035*SL	1.16 + 0.033*SL	1.16 + 0.033*SL
	t_{PHL}	1.15	1.06 + 0.046*SL	1.06 + 0.045*SL	1.07 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D0 to QN0	t_{PLH}	0.74	0.66 + 0.038*SL	0.67 + 0.035*SL	0.68 + 0.034*SL
	t_{PHL}	0.65	0.55 + 0.051*SL	0.56 + 0.046*SL	0.57 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
G to QN0	t_{PLH}	0.92	0.84 + 0.038*SL	0.85 + 0.035*SL	0.86 + 0.034*SL
	t_{PHL}	1.16	1.05 + 0.052*SL	1.07 + 0.046*SL	1.08 + 0.045*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

STDM80 LD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.74	0.66 + 0.038*SL	0.67 + 0.035*SL	0.68 + 0.034*SL
	t_{PHL}	0.65	0.54 + 0.052*SL	0.56 + 0.046*SL	0.57 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
G to QN1	t_{PLH}	0.92	0.85 + 0.038*SL	0.86 + 0.035*SL	0.86 + 0.034*SL
	t_{PHL}	1.16	1.05 + 0.052*SL	1.07 + 0.046*SL	1.08 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
D2 to QN2	t_{PLH}	0.74	0.66 + 0.038*SL	0.67 + 0.035*SL	0.68 + 0.034*SL
	t_{PHL}	0.65	0.55 + 0.052*SL	0.56 + 0.046*SL	0.57 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
G to QN2	t_{PLH}	0.92	0.84 + 0.038*SL	0.86 + 0.035*SL	0.86 + 0.034*SL
	t_{PHL}	1.16	1.05 + 0.052*SL	1.07 + 0.046*SL	1.08 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
D3 to QN3	t_{PLH}	0.74	0.66 + 0.038*SL	0.67 + 0.035*SL	0.68 + 0.034*SL
	t_{PHL}	0.65	0.55 + 0.052*SL	0.56 + 0.046*SL	0.57 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
G to QN3	t_{PLH}	0.93	0.85 + 0.038*SL	0.86 + 0.035*SL	0.87 + 0.034*SL
	t_{PHL}	1.15	1.05 + 0.052*SL	1.07 + 0.046*SL	1.08 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

STDM80 LD1X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.81	0.77 + 0.018*SL	0.77 + 0.017*SL	0.78 + 0.017*SL
	t_{PHL}	1.04	0.99 + 0.026*SL	1.00 + 0.023*SL	1.00 + 0.022*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
G to Q0	t_{PLH}	1.33	1.29 + 0.018*SL	1.29 + 0.017*SL	1.30 + 0.017*SL
	t_{PHL}	1.22	1.17 + 0.026*SL	1.18 + 0.023*SL	1.19 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D1 to Q1	t_{PLH}	0.81	0.77 + 0.018*SL	0.78 + 0.017*SL	0.78 + 0.017*SL
	t_{PHL}	1.04	0.99 + 0.026*SL	1.00 + 0.023*SL	1.01 + 0.022*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.041*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
G to Q1	t_{PLH}	1.33	1.29 + 0.019*SL	1.30 + 0.017*SL	1.30 + 0.017*SL
	t_{PHL}	1.23	1.18 + 0.026*SL	1.18 + 0.023*SL	1.19 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D2 to Q2	t_{PLH}	0.81	0.77 + 0.018*SL	0.78 + 0.017*SL	0.78 + 0.017*SL
	t_{PHL}	1.04	0.99 + 0.026*SL	1.00 + 0.023*SL	1.01 + 0.022*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
G to Q2	t_{PLH}	1.33	1.29 + 0.019*SL	1.30 + 0.017*SL	1.30 + 0.017*SL
	t_{PHL}	1.23	1.18 + 0.026*SL	1.18 + 0.023*SL	1.19 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D3 to Q3	t_{PLH}	0.81	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.017*SL
	t_{PHL}	1.04	0.99 + 0.026*SL	1.00 + 0.023*SL	1.00 + 0.022*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
G to Q3	t_{PLH}	1.32	1.29 + 0.018*SL	1.29 + 0.017*SL	1.29 + 0.017*SL
	t_{PHL}	1.23	1.18 + 0.025*SL	1.19 + 0.023*SL	1.20 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D0 to QN0	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.020*SL	0.72 + 0.018*SL
	t_{PHL}	0.64	0.57 + 0.030*SL	0.59 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
G to QN0	t_{PLH}	0.93	0.88 + 0.024*SL	0.89 + 0.019*SL	0.90 + 0.018*SL
	t_{PHL}	1.15	1.09 + 0.031*SL	1.11 + 0.026*SL	1.12 + 0.023*SL
	t_R	0.21	0.14 + 0.032*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.13 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

STDM80 LD1X4D2

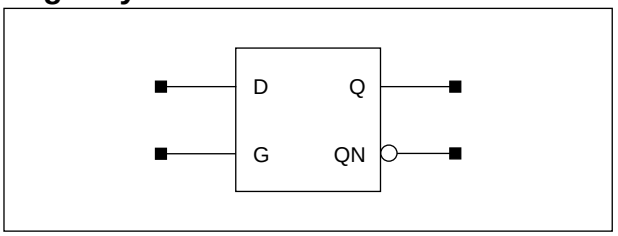
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.020*SL	0.72 + 0.018*SL
	t_{PHL}	0.64	0.57 + 0.030*SL	0.59 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
G to QN1	t_{PLH}	0.93	0.88 + 0.024*SL	0.89 + 0.020*SL	0.91 + 0.018*SL
	t_{PHL}	1.15	1.09 + 0.031*SL	1.11 + 0.026*SL	1.13 + 0.023*SL
	t_R	0.21	0.14 + 0.032*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
D2 to QN2	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.020*SL	0.72 + 0.018*SL
	t_{PHL}	0.64	0.57 + 0.030*SL	0.59 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
G to QN2	t_{PLH}	0.93	0.88 + 0.024*SL	0.89 + 0.019*SL	0.90 + 0.018*SL
	t_{PHL}	1.15	1.09 + 0.031*SL	1.11 + 0.026*SL	1.13 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.22	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
D3 to QN3	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.020*SL	0.72 + 0.018*SL
	t_{PHL}	0.63	0.57 + 0.030*SL	0.59 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
G to QN3	t_{PLH}	0.93	0.88 + 0.024*SL	0.90 + 0.020*SL	0.91 + 0.018*SL
	t_{PHL}	1.15	1.09 + 0.031*SL	1.11 + 0.026*SL	1.12 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.13 + 0.041*SL	0.14 + 0.038*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

YLD1/YLD1D2

Fast D Latch with Active High, 1X/2X Drive

Logic Symbol



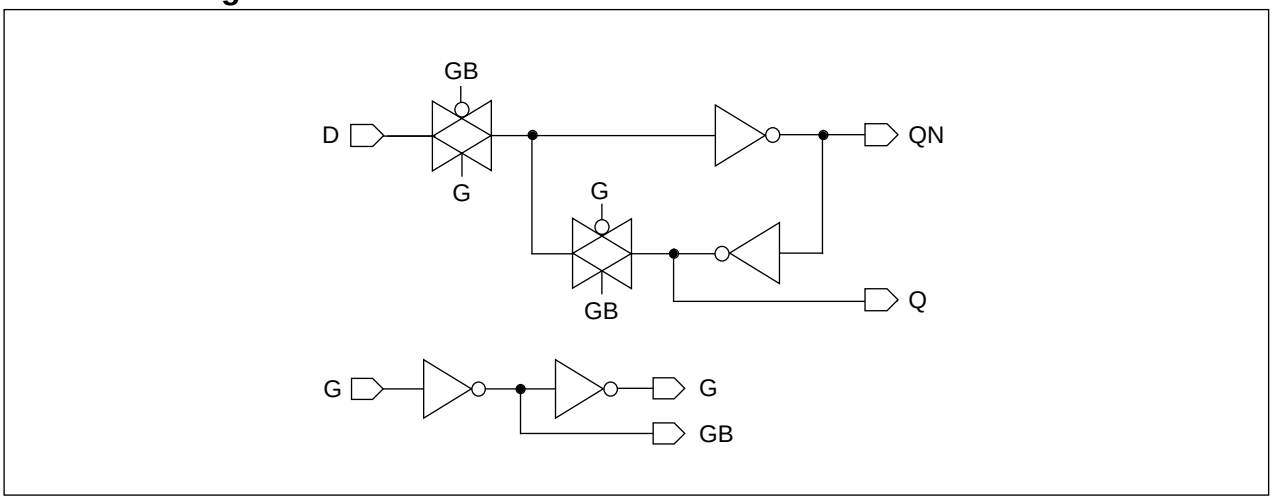
Truth Table

D	G	Q (n+1)	QN (n+1)
0	1	0	1
1	1	1	0
x	0	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
STD80					
YLD1		*YLD1D2*		*YLD1*	*YLD1D2*
D	G	D	G		
2.1	0.5	3.1	0.5	2.7	3.7
STDM80					
YLD1		*YLD1D2*		*YLD1*	*YLD1D2*
D	G	D	G		
2.4	0.6	3.5	0.6	2.7	3.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		YLD1	YLD1D2	YLD1	YLD1D2
Pulse Width High (G)	t_{PWH}	0.87	0.87	0.82	0.82
Input Setup Time (D to G)	t_{SU}	0.41	0.38	0.49	0.46
Input Hold Time (D to G)	t_{HD}	0.33	0.33	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 YLD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.42	0.26 + 0.080*SL	0.27 + 0.075*SL	0.27 + 0.075*SL
	t_{PHL}	0.40	0.25 + 0.076*SL	0.26 + 0.072*SL	0.26 + 0.072*SL
	t_R	0.23	0.10 + 0.064*SL	0.10 + 0.064*SL	0.09 + 0.065*SL
	t_F	0.24	0.09 + 0.072*SL	0.09 + 0.076*SL	0.08 + 0.076*SL
G to Q	t_{PLH}	0.57	0.42 + 0.078*SL	0.42 + 0.076*SL	0.42 + 0.075*SL
	t_{PHL}	0.54	0.40 + 0.073*SL	0.40 + 0.072*SL	0.40 + 0.072*SL
	t_R	0.22	0.10 + 0.064*SL	0.09 + 0.065*SL	0.09 + 0.065*SL
	t_F	0.23	0.08 + 0.075*SL	0.08 + 0.076*SL	0.08 + 0.076*SL
D to QN	t_{PLH}	0.23	0.17 + 0.030*SL	0.18 + 0.024*SL	0.18 + 0.024*SL
	t_{PHL}	0.29	0.22 + 0.039*SL	0.22 + 0.036*SL	0.22 + 0.037*SL
	t_R	0.30	0.22 + 0.039*SL	0.20 + 0.046*SL	0.14 + 0.052*SL
	t_F	0.36	0.26 + 0.050*SL	0.24 + 0.061*SL	0.16 + 0.069*SL
G to QN	t_{PLH}	0.37	0.32 + 0.024*SL	0.33 + 0.024*SL	0.33 + 0.024*SL
	t_{PHL}	0.45	0.37 + 0.039*SL	0.37 + 0.037*SL	0.37 + 0.037*SL
	t_R	0.23	0.14 + 0.046*SL	0.13 + 0.050*SL	0.11 + 0.052*SL
	t_F	0.30	0.17 + 0.062*SL	0.16 + 0.066*SL	0.14 + 0.069*SL

STD80 YLD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.36	0.27 + 0.043*SL	0.28 + 0.038*SL	0.29 + 0.037*SL
	t_{PHL}	0.34	0.26 + 0.039*SL	0.26 + 0.037*SL	0.27 + 0.035*SL
	t_R	0.16	0.10 + 0.030*SL	0.09 + 0.031*SL	0.08 + 0.033*SL
	t_F	0.15	0.08 + 0.034*SL	0.08 + 0.037*SL	0.07 + 0.038*SL
G to Q	t_{PLH}	0.53	0.45 + 0.040*SL	0.45 + 0.039*SL	0.46 + 0.037*SL
	t_{PHL}	0.49	0.40 + 0.042*SL	0.42 + 0.036*SL	0.42 + 0.036*SL
	t_R	0.15	0.09 + 0.029*SL	0.09 + 0.032*SL	0.08 + 0.033*SL
	t_F	0.15	0.08 + 0.034*SL	0.07 + 0.037*SL	0.07 + 0.038*SL
D to QN	t_{PLH}	0.22	0.19 + 0.017*SL	0.20 + 0.013*SL	0.21 + 0.012*SL
	t_{PHL}	0.27	0.23 + 0.022*SL	0.24 + 0.019*SL	0.25 + 0.018*SL
	t_R	0.25	0.21 + 0.018*SL	0.20 + 0.021*SL	0.16 + 0.026*SL
	t_F	0.31	0.26 + 0.023*SL	0.26 + 0.027*SL	0.20 + 0.033*SL
G to QN	t_{PLH}	0.38	0.34 + 0.018*SL	0.35 + 0.012*SL	0.36 + 0.012*SL
	t_{PHL}	0.45	0.40 + 0.021*SL	0.41 + 0.019*SL	0.42 + 0.018*SL
	t_R	0.19	0.16 + 0.017*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.25	0.19 + 0.029*SL	0.19 + 0.030*SL	0.15 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

YLD1/YLD1D2

Fast D Latch with Active High, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 YLD1

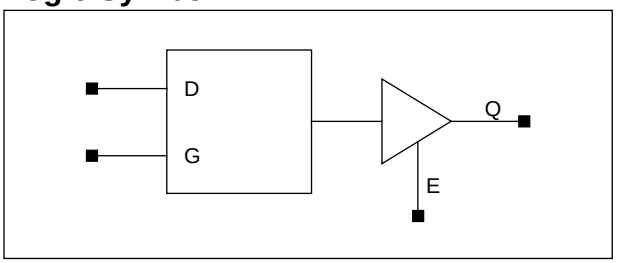
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.57	0.36 + 0.103*SL	0.38 + 0.100*SL	0.38 + 0.099*SL
	t_{PHL}	0.54	0.34 + 0.098*SL	0.35 + 0.096*SL	0.35 + 0.096*SL
	t_R	0.30	0.13 + 0.085*SL	0.13 + 0.086*SL	0.13 + 0.087*SL
	t_F	0.30	0.11 + 0.095*SL	0.11 + 0.094*SL	0.11 + 0.095*SL
G to Q	t_{PLH}	0.81	0.60 + 0.103*SL	0.61 + 0.100*SL	0.62 + 0.099*SL
	t_{PHL}	0.77	0.58 + 0.097*SL	0.58 + 0.096*SL	0.58 + 0.096*SL
	t_R	0.30	0.13 + 0.086*SL	0.13 + 0.087*SL	0.13 + 0.087*SL
	t_F	0.30	0.11 + 0.094*SL	0.11 + 0.095*SL	0.11 + 0.095*SL
D to QN	t_{PLH}	0.31	0.24 + 0.035*SL	0.25 + 0.033*SL	0.25 + 0.033*SL
	t_{PHL}	0.38	0.28 + 0.049*SL	0.30 + 0.045*SL	0.30 + 0.044*SL
	t_R	0.34	0.21 + 0.065*SL	0.19 + 0.069*SL	0.18 + 0.071*SL
	t_F	0.41	0.26 + 0.071*SL	0.24 + 0.077*SL	0.22 + 0.080*SL
G to QN	t_{PLH}	0.54	0.47 + 0.034*SL	0.48 + 0.034*SL	0.48 + 0.033*SL
	t_{PHL}	0.62	0.52 + 0.049*SL	0.53 + 0.045*SL	0.54 + 0.044*SL
	t_R	0.32	0.19 + 0.068*SL	0.18 + 0.070*SL	0.17 + 0.072*SL
	t_F	0.38	0.22 + 0.076*SL	0.21 + 0.080*SL	0.20 + 0.081*SL

STDM80 YLD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.50	0.38 + 0.056*SL	0.39 + 0.052*SL	0.41 + 0.050*SL
	t_{PHL}	0.46	0.36 + 0.050*SL	0.36 + 0.048*SL	0.37 + 0.047*SL
	t_R	0.20	0.12 + 0.041*SL	0.12 + 0.042*SL	0.11 + 0.043*SL
	t_F	0.19	0.10 + 0.045*SL	0.09 + 0.046*SL	0.09 + 0.046*SL
G to Q	t_{PLH}	0.77	0.66 + 0.056*SL	0.67 + 0.052*SL	0.68 + 0.050*SL
	t_{PHL}	0.69	0.59 + 0.050*SL	0.60 + 0.048*SL	0.61 + 0.047*SL
	t_R	0.20	0.12 + 0.042*SL	0.12 + 0.042*SL	0.11 + 0.043*SL
	t_F	0.19	0.09 + 0.046*SL	0.09 + 0.046*SL	0.09 + 0.046*SL
D to QN	t_{PLH}	0.31	0.27 + 0.019*SL	0.28 + 0.018*SL	0.28 + 0.017*SL
	t_{PHL}	0.37	0.31 + 0.029*SL	0.32 + 0.025*SL	0.33 + 0.023*SL
	t_R	0.26	0.20 + 0.029*SL	0.19 + 0.033*SL	0.18 + 0.034*SL
	t_F	0.34	0.28 + 0.032*SL	0.27 + 0.035*SL	0.25 + 0.037*SL
G to QN	t_{PLH}	0.55	0.51 + 0.019*SL	0.51 + 0.018*SL	0.52 + 0.017*SL
	t_{PHL}	0.64	0.58 + 0.029*SL	0.59 + 0.025*SL	0.61 + 0.023*SL
	t_R	0.25	0.19 + 0.030*SL	0.18 + 0.033*SL	0.18 + 0.034*SL
	t_F	0.32	0.25 + 0.033*SL	0.24 + 0.037*SL	0.24 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Logic Symbol



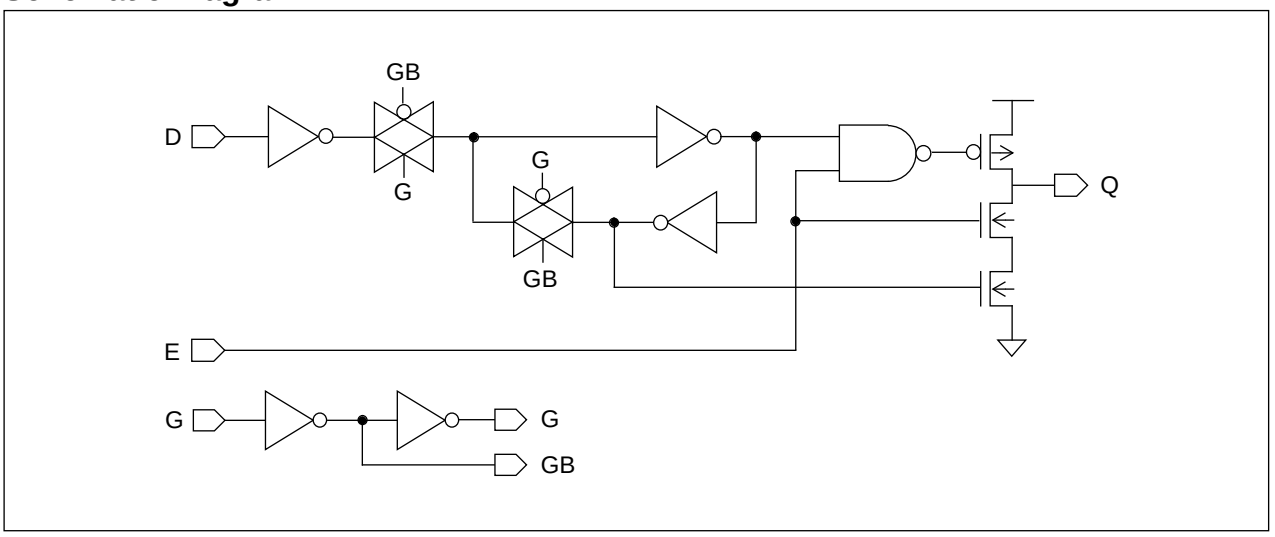
Truth Table

D	G	E	Q (n+1)
x	x	0	Hi-Z
0	1	1	0
1	1	1	1
x	0	1	Q (n)

Cell Data

Input Load (SL)			Output Load (SL)	Gate Count
STD80				
D	G	E	Q	
0.6	0.6	0.9	0.9	4.7
STDM80				
D	G	E	Q	
0.6	0.6	1.0	1.0	4.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width High (G)	t_{PWH}	0.79	0.82
Input Setup Time (D to G)	t_{SU}	0.57	0.57
Input Hold Time (D to G)	t_{HD}	0.33	0.33

LD1A

D Latch with Active High, Tri-State Output

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD1A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.56	0.52 + 0.021*SL	0.53 + 0.015*SL	0.56 + 0.012*SL
	t_{PHL}	0.66	0.58 + 0.037*SL	0.58 + 0.038*SL	0.58 + 0.039*SL
	t_R	0.16	0.11 + 0.029*SL	0.12 + 0.025*SL	0.10 + 0.027*SL
	t_F	0.26	0.11 + 0.071*SL	0.10 + 0.076*SL	0.09 + 0.078*SL
G to Q	t_{PLH}	0.67	0.63 + 0.021*SL	0.64 + 0.015*SL	0.67 + 0.012*SL
	t_{PHL}	0.66	0.59 + 0.036*SL	0.58 + 0.038*SL	0.58 + 0.039*SL
	t_R	0.16	0.11 + 0.028*SL	0.11 + 0.025*SL	0.10 + 0.027*SL
	t_F	0.26	0.12 + 0.070*SL	0.10 + 0.076*SL	0.09 + 0.078*SL
E to Q	t_{PLH}	0.22	0.18 + 0.023*SL	0.19 + 0.016*SL	0.22 + 0.012*SL
	t_{PHL}	0.15	0.03 + 0.058*SL	0.07 + 0.040*SL	0.09 + 0.039*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.024*SL	0.11 + 0.027*SL
	t_F	0.34	0.19 + 0.070*SL	0.20 + 0.070*SL	0.12 + 0.078*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.33	0.33 + -0.001*SL	0.33 + 0.000*SL	0.33 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

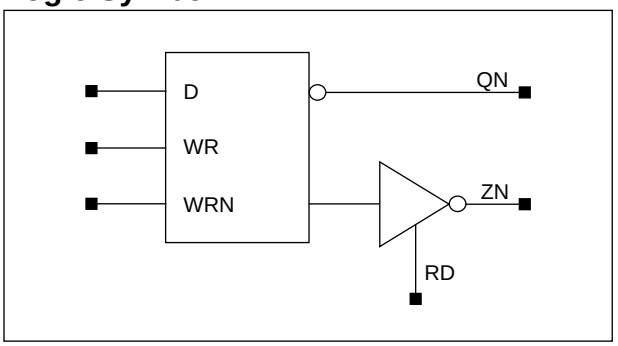
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD1A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.82	0.76 + 0.027*SL	0.78 + 0.021*SL	0.80 + 0.019*SL
	t_{PHL}	0.90	0.80 + 0.050*SL	0.80 + 0.049*SL	0.80 + 0.050*SL
	t_R	0.22	0.15 + 0.037*SL	0.16 + 0.035*SL	0.15 + 0.036*SL
	t_F	0.34	0.15 + 0.094*SL	0.13 + 0.098*SL	0.13 + 0.099*SL
G to Q	t_{PLH}	1.00	0.95 + 0.027*SL	0.96 + 0.021*SL	0.98 + 0.019*SL
	t_{PHL}	0.94	0.84 + 0.050*SL	0.85 + 0.049*SL	0.84 + 0.050*SL
	t_R	0.22	0.15 + 0.037*SL	0.16 + 0.035*SL	0.15 + 0.036*SL
	t_F	0.34	0.15 + 0.095*SL	0.14 + 0.098*SL	0.13 + 0.099*SL
E to Q	t_{PLH}	0.32	0.26 + 0.028*SL	0.28 + 0.021*SL	0.30 + 0.019*SL
	t_{PHL}	0.22	0.11 + 0.054*SL	0.13 + 0.049*SL	0.13 + 0.050*SL
	t_R	0.24	0.18 + 0.032*SL	0.17 + 0.034*SL	0.16 + 0.035*SL
	t_F	0.38	0.21 + 0.086*SL	0.19 + 0.093*SL	0.15 + 0.097*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.42	0.42 + 0.000*SL	0.42 + 0.000*SL	0.42 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Logic Symbol



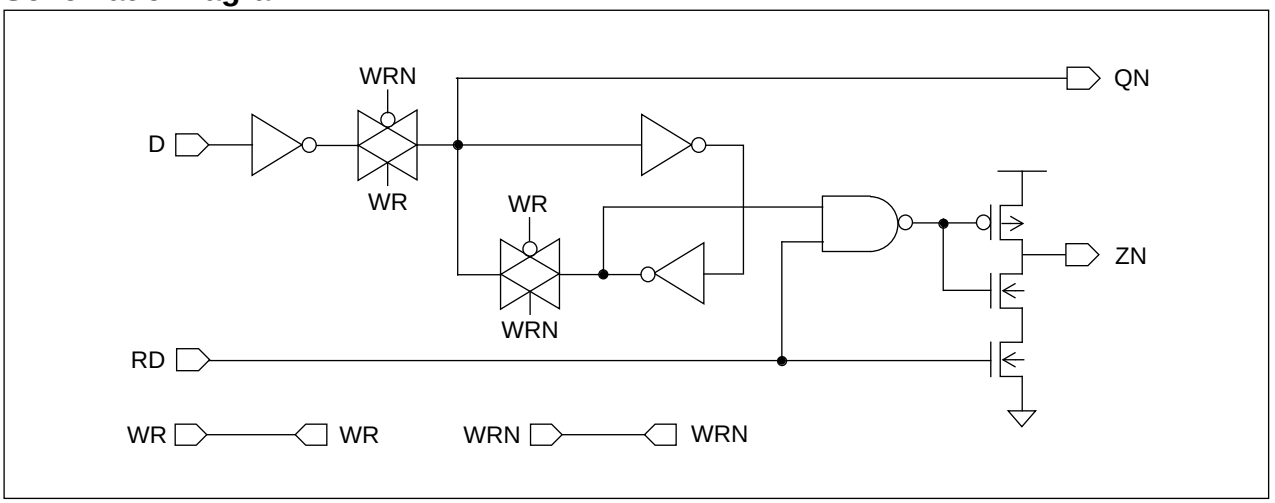
Truth Table

D	WR	WRN	RD	QN (n+1)	ZN (n+1)
0	1	0	0	1	Hi-Z
1	1	0	0	0	Hi-Z
0	1	0	1	1	1
1	1	0	1	0	0
x	0	1	0	QN (n)	Hi-Z
x	0	1	1	QN (n)	QN (n)

Cell Data

Input Load (SL)				Output Load (SL)	Gate Count
STD80					
D	WR	WRN	RD	ZN	
0.6	0.5	0.6	1.1	0.9	4.0
STDM80					
D	WR	WRN	RD	ZN	
0.6	0.6	0.6	1.1	1.0	4.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width High (WR)	t_{PWH}	0.87	1.18
Pulse Width Low (WRN)	t_{PWL}	0.87	1.18
Input Setup Time (D to WR)	t_{SU}	0.93	1.31
Input Hold Time (D to WR)	t_{HD}	0.33	0.33
Input Setup Time (D to WRN)	t_{SU}	0.93	1.31
Input Hold Time (D to WRN)	t_{HD}	0.52	0.33
Skew Time (WR to WRN)	t_{SK}	0.78	0.88
Skew Time (WRN to WR)	t_{SK}	0.78	0.88

LD1B

D Latch with Active High, Tri-State Output, Separate WR, WRN

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD1B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to QN	t_{PLH}	0.40	0.26 + 0.070*SL	0.26 + 0.070*SL	0.26 + 0.070*SL
	t_{PHL}	0.25	0.15 + 0.050*SL	0.16 + 0.046*SL	0.17 + 0.045*SL
	t_R	0.78	0.40 + 0.190*SL	0.38 + 0.199*SL	0.34 + 0.204*SL
	t_F	0.43	0.25 + 0.087*SL	0.23 + 0.096*SL	0.17 + 0.102*SL
WR to QN	t_{PLH}	0.30	0.19 + 0.055*SL	0.17 + 0.066*SL	0.13 + 0.070*SL
	t_{PHL}	0.21	0.11 + 0.049*SL	0.12 + 0.043*SL	0.11 + 0.045*SL
	t_R	0.78	0.41 + 0.182*SL	0.38 + 0.197*SL	0.32 + 0.204*SL
	t_F	0.44	0.28 + 0.082*SL	0.25 + 0.094*SL	0.17 + 0.102*SL
WRN to QN	t_{PLH}	0.30	0.19 + 0.055*SL	0.17 + 0.066*SL	0.13 + 0.070*SL
	t_{PHL}	0.21	0.11 + 0.049*SL	0.12 + 0.043*SL	0.11 + 0.045*SL
	t_R	0.78	0.41 + 0.182*SL	0.38 + 0.197*SL	0.32 + 0.204*SL
	t_F	0.44	0.28 + 0.082*SL	0.25 + 0.094*SL	0.17 + 0.102*SL
D to ZN	t_{PLH}	0.87	0.68 + 0.092*SL	0.71 + 0.081*SL	0.80 + 0.071*SL
	t_{PHL}	0.81	0.59 + 0.112*SL	0.61 + 0.104*SL	0.69 + 0.095*SL
	t_R	0.18	0.13 + 0.024*SL	0.13 + 0.025*SL	0.11 + 0.027*SL
	t_F	0.26	0.11 + 0.072*SL	0.10 + 0.076*SL	0.09 + 0.078*SL
WR to ZN	t_{PLH}	0.77	0.61 + 0.080*SL	0.61 + 0.076*SL	0.67 + 0.071*SL
	t_{PHL}	0.77	0.55 + 0.112*SL	0.57 + 0.101*SL	0.63 + 0.095*SL
	t_R	0.18	0.13 + 0.023*SL	0.13 + 0.025*SL	0.11 + 0.027*SL
	t_F	0.26	0.11 + 0.075*SL	0.10 + 0.076*SL	0.09 + 0.078*SL
WRN to ZN	t_{PLH}	0.77	0.61 + 0.080*SL	0.61 + 0.076*SL	0.67 + 0.071*SL
	t_{PHL}	0.77	0.55 + 0.112*SL	0.57 + 0.101*SL	0.63 + 0.095*SL
	t_R	0.18	0.13 + 0.023*SL	0.13 + 0.025*SL	0.11 + 0.027*SL
	t_F	0.26	0.11 + 0.075*SL	0.10 + 0.076*SL	0.09 + 0.078*SL
RD to ZN	t_{PLH}	0.26	0.22 + 0.020*SL	0.23 + 0.015*SL	0.26 + 0.012*SL
	t_{PHL}	0.15	0.03 + 0.057*SL	0.07 + 0.041*SL	0.09 + 0.039*SL
	t_R	0.19	0.15 + 0.021*SL	0.14 + 0.024*SL	0.11 + 0.027*SL
	t_F	0.33	0.19 + 0.070*SL	0.19 + 0.070*SL	0.12 + 0.078*SL
	t_{PLZ}	0.22	0.22 + 0.000*SL	0.22 + 0.000*SL	0.22 + 0.000*SL
	t_{PHZ}	0.36	0.36 + 0.001*SL	0.36 + 0.000*SL	0.36 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD1B

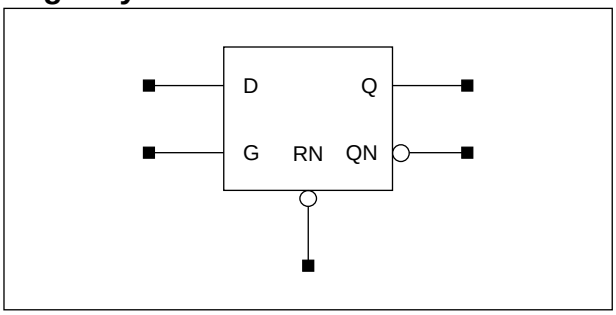
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to QN	t_{PLH}	0.56	0.34 + 0.110*SL	0.34 + 0.109*SL	0.35 + 0.108*SL
	t_{PHL}	0.33	0.21 + 0.061*SL	0.21 + 0.060*SL	0.21 + 0.060*SL
	t_R	1.22	0.58 + 0.318*SL	0.56 + 0.325*SL	0.55 + 0.327*SL
	t_F	0.51	0.26 + 0.124*SL	0.24 + 0.130*SL	0.22 + 0.133*SL
WR to QN	t_{PLH}	0.42	0.22 + 0.102*SL	0.20 + 0.106*SL	0.20 + 0.107*SL
	t_{PHL}	0.27	0.16 + 0.058*SL	0.15 + 0.059*SL	0.15 + 0.059*SL
	t_R	1.18	0.54 + 0.318*SL	0.51 + 0.327*SL	0.49 + 0.331*SL
	t_F	0.51	0.27 + 0.123*SL	0.25 + 0.129*SL	0.22 + 0.133*SL
WRN to QN	t_{PLH}	0.42	0.22 + 0.102*SL	0.20 + 0.106*SL	0.20 + 0.107*SL
	t_{PHL}	0.27	0.16 + 0.058*SL	0.15 + 0.059*SL	0.15 + 0.059*SL
	t_R	1.18	0.54 + 0.318*SL	0.51 + 0.327*SL	0.49 + 0.331*SL
	t_F	0.51	0.27 + 0.123*SL	0.25 + 0.129*SL	0.22 + 0.133*SL
D to ZN	t_{PLH}	1.26	0.99 + 0.139*SL	1.02 + 0.126*SL	1.08 + 0.118*SL
	t_{PHL}	1.13	0.84 + 0.144*SL	0.86 + 0.136*SL	0.89 + 0.133*SL
	t_R	0.23	0.16 + 0.036*SL	0.16 + 0.035*SL	0.16 + 0.035*SL
	t_F	0.34	0.15 + 0.095*SL	0.15 + 0.097*SL	0.14 + 0.099*SL
WR to ZN	t_{PLH}	1.13	0.86 + 0.130*SL	0.89 + 0.123*SL	0.93 + 0.117*SL
	t_{PHL}	1.07	0.79 + 0.141*SL	0.81 + 0.135*SL	0.83 + 0.132*SL
	t_R	0.23	0.16 + 0.036*SL	0.16 + 0.035*SL	0.16 + 0.035*SL
	t_F	0.34	0.15 + 0.096*SL	0.15 + 0.097*SL	0.14 + 0.099*SL
WRN to ZN	t_{PLH}	1.13	0.86 + 0.130*SL	0.89 + 0.123*SL	0.93 + 0.117*SL
	t_{PHL}	1.07	0.79 + 0.141*SL	0.81 + 0.135*SL	0.83 + 0.132*SL
	t_R	0.23	0.16 + 0.036*SL	0.16 + 0.035*SL	0.16 + 0.035*SL
	t_F	0.34	0.15 + 0.096*SL	0.15 + 0.097*SL	0.14 + 0.099*SL
RD to ZN	t_{PLH}	0.37	0.32 + 0.025*SL	0.33 + 0.021*SL	0.35 + 0.019*SL
	t_{PHL}	0.22	0.11 + 0.054*SL	0.13 + 0.049*SL	0.13 + 0.050*SL
	t_R	0.24	0.16 + 0.037*SL	0.17 + 0.034*SL	0.16 + 0.035*SL
	t_F	0.38	0.20 + 0.087*SL	0.19 + 0.093*SL	0.16 + 0.097*SL
	t_{PLZ}	0.19	0.19 + 0.000*SL	0.19 + 0.000*SL	0.19 + 0.000*SL
	t_{PHZ}	0.47	0.47 + 0.000*SL	0.46 + 0.000*SL	0.46 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

LD2/LD2D2

D Latch with Active High, Reset, 1X/2X Drive

Logic Symbol



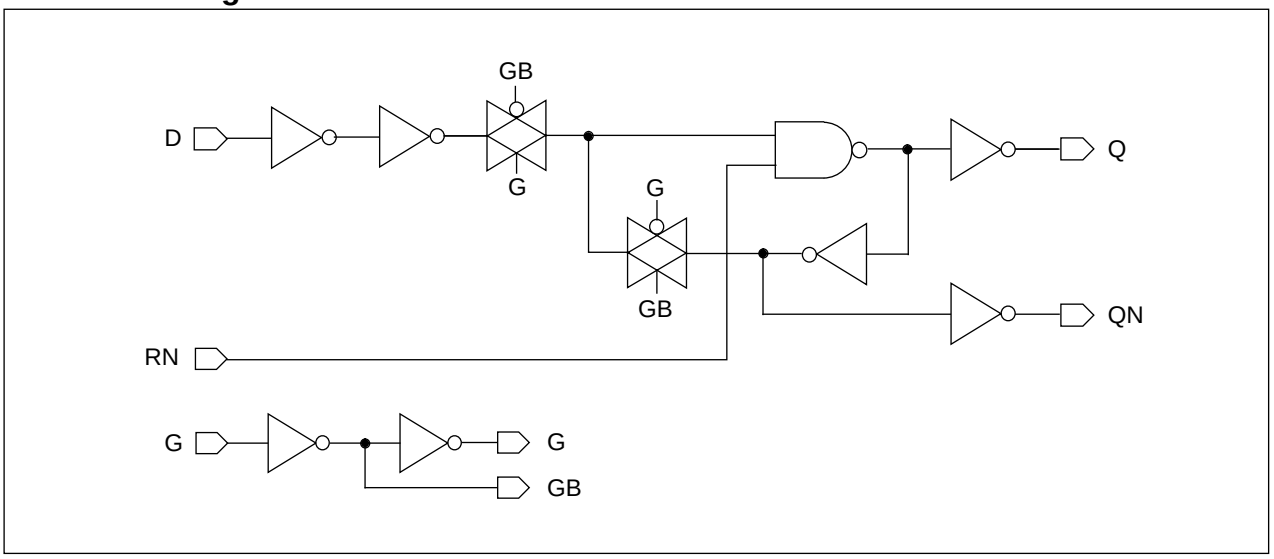
Truth Table

D	G	RN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
STD80							
LD2			*LD2D2*			*LD2*	*LD2D2*
D	G	RN	D	G	RN		
0.5	0.5	0.7	0.5	0.5	0.6	4.7	5.3
STDM80							
LD2			*LD2D2*			*LD2*	*LD2D2*
D	G	RN	D	G	RN		
0.6	0.6	0.8	0.6	0.6	0.8	4.7	5.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD2	LD2D2	LD2	LD2D2
Pulse Width High (G)	t_{PWH}	0.79	0.79	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Input Setup Time (D to G)	t_{SU}	0.55	0.76	0.71	0.76
Input Hold Time (D to G)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to G)	t_{HD}	0.38	0.33	0.44	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.57	0.51 + 0.032*SL	0.52 + 0.026*SL	0.54 + 0.024*SL
	t_{PHL}	0.64	0.56 + 0.041*SL	0.57 + 0.038*SL	0.58 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
G to Q	t_{PLH}	0.58	0.52 + 0.031*SL	0.53 + 0.026*SL	0.55 + 0.024*SL
	t_{PHL}	0.60	0.52 + 0.041*SL	0.53 + 0.038*SL	0.54 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.061*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PLH}	0.33	0.27 + 0.031*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.23	0.14 + 0.045*SL	0.13 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
D to QN	t_{PLH}	0.69	0.64 + 0.025*SL	0.64 + 0.024*SL	0.64 + 0.024*SL
	t_{PHL}	0.75	0.68 + 0.037*SL	0.68 + 0.037*SL	0.67 + 0.037*SL
	t_R	0.18	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
G to QN	t_{PLH}	0.65	0.60 + 0.025*SL	0.60 + 0.024*SL	0.60 + 0.024*SL
	t_{PHL}	0.76	0.68 + 0.037*SL	0.68 + 0.037*SL	0.68 + 0.037*SL
	t_R	0.19	0.10 + 0.045*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.47	0.41 + 0.030*SL	0.42 + 0.025*SL	0.43 + 0.024*SL
	t_{PHL}	0.51	0.43 + 0.037*SL	0.43 + 0.037*SL	0.43 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.22	0.10 + 0.060*SL	0.09 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.59	0.54 + 0.021*SL	0.56 + 0.015*SL	0.59 + 0.012*SL
	t_{PHL}	0.64	0.59 + 0.023*SL	0.60 + 0.020*SL	0.61 + 0.018*SL
	t_R	0.20	0.15 + 0.025*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.17	0.12 + 0.029*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
G to Q	t_{PLH}	0.60	0.55 + 0.021*SL	0.57 + 0.015*SL	0.60 + 0.012*SL
	t_{PHL}	0.60	0.55 + 0.023*SL	0.56 + 0.020*SL	0.57 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.18	0.11 + 0.031*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
RN to Q	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.015*SL	0.35 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
D to QN	t_{PLH}	0.75	0.72 + 0.014*SL	0.73 + 0.012*SL	0.73 + 0.012*SL
	t_{PHL}	0.83	0.80 + 0.017*SL	0.80 + 0.017*SL	0.79 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.033*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
G to QN	t_{PLH}	0.71	0.68 + 0.014*SL	0.69 + 0.012*SL	0.69 + 0.012*SL
	t_{PHL}	0.84	0.81 + 0.017*SL	0.81 + 0.017*SL	0.80 + 0.018*SL
	t_R	0.15	0.11 + 0.019*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
RN to QN	t_{PLH}	0.53	0.50 + 0.018*SL	0.51 + 0.014*SL	0.53 + 0.012*SL
	t_{PHL}	0.59	0.55 + 0.018*SL	0.55 + 0.017*SL	0.54 + 0.018*SL
	t_R	0.18	0.14 + 0.022*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.030*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.85	0.77 + 0.044*SL	0.79 + 0.038*SL	0.81 + 0.035*SL
	t_{PHL}	0.87	0.77 + 0.052*SL	0.79 + 0.046*SL	0.80 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
G to Q	t_{PLH}	0.86	0.77 + 0.044*SL	0.79 + 0.038*SL	0.81 + 0.034*SL
	t_{PHL}	0.86	0.76 + 0.052*SL	0.78 + 0.046*SL	0.79 + 0.044*SL
	t_R	0.31	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.081*SL
RN to Q	t_{PLH}	0.44	0.35 + 0.043*SL	0.37 + 0.037*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.047*SL	0.40 + 0.045*SL
	t_R	0.31	0.17 + 0.071*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
D to QN	t_{PLH}	0.95	0.88 + 0.035*SL	0.88 + 0.033*SL	0.88 + 0.033*SL
	t_{PHL}	1.09	1.00 + 0.047*SL	1.01 + 0.045*SL	1.01 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.078*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
G to QN	t_{PLH}	0.94	0.87 + 0.035*SL	0.87 + 0.033*SL	0.87 + 0.033*SL
	t_{PHL}	1.10	1.00 + 0.047*SL	1.01 + 0.044*SL	1.01 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
RN to QN	t_{PLH}	0.63	0.54 + 0.042*SL	0.56 + 0.036*SL	0.58 + 0.033*SL
	t_{PHL}	0.67	0.58 + 0.047*SL	0.59 + 0.045*SL	0.59 + 0.044*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

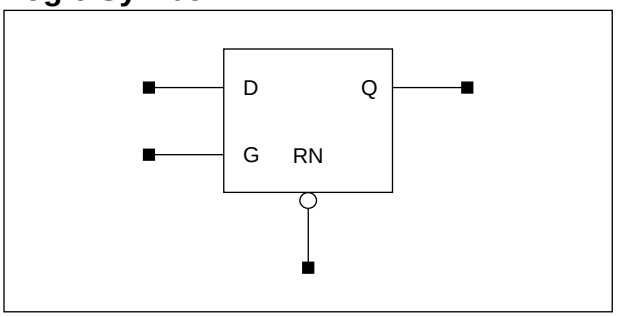
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.87	0.81 + 0.028*SL	0.83 + 0.022*SL	0.85 + 0.020*SL
	t_{PHL}	0.86	0.80 + 0.031*SL	0.81 + 0.026*SL	0.83 + 0.023*SL
	t_R	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
G to Q	t_{PLH}	0.87	0.82 + 0.028*SL	0.83 + 0.023*SL	0.85 + 0.019*SL
	t_{PHL}	0.85	0.79 + 0.031*SL	0.81 + 0.026*SL	0.83 + 0.023*SL
	t_R	0.25	0.17 + 0.038*SL	0.18 + 0.034*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
RN to Q	t_{PLH}	0.44	0.39 + 0.027*SL	0.40 + 0.022*SL	0.43 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.21	0.14 + 0.039*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
D to QN	t_{PLH}	1.04	1.00 + 0.019*SL	1.00 + 0.017*SL	1.01 + 0.017*SL
	t_{PHL}	1.20	1.15 + 0.024*SL	1.16 + 0.022*SL	1.16 + 0.021*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.22	0.13 + 0.041*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
G to QN	t_{PLH}	1.03	0.99 + 0.019*SL	0.99 + 0.017*SL	1.00 + 0.017*SL
	t_{PHL}	1.21	1.16 + 0.024*SL	1.16 + 0.022*SL	1.17 + 0.021*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.22	0.13 + 0.042*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
RN to QN	t_{PLH}	0.71	0.66 + 0.023*SL	0.67 + 0.020*SL	0.68 + 0.018*SL
	t_{PHL}	0.78	0.73 + 0.025*SL	0.73 + 0.022*SL	0.74 + 0.021*SL
	t_R	0.23	0.16 + 0.036*SL	0.17 + 0.033*SL	0.17 + 0.033*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.037*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



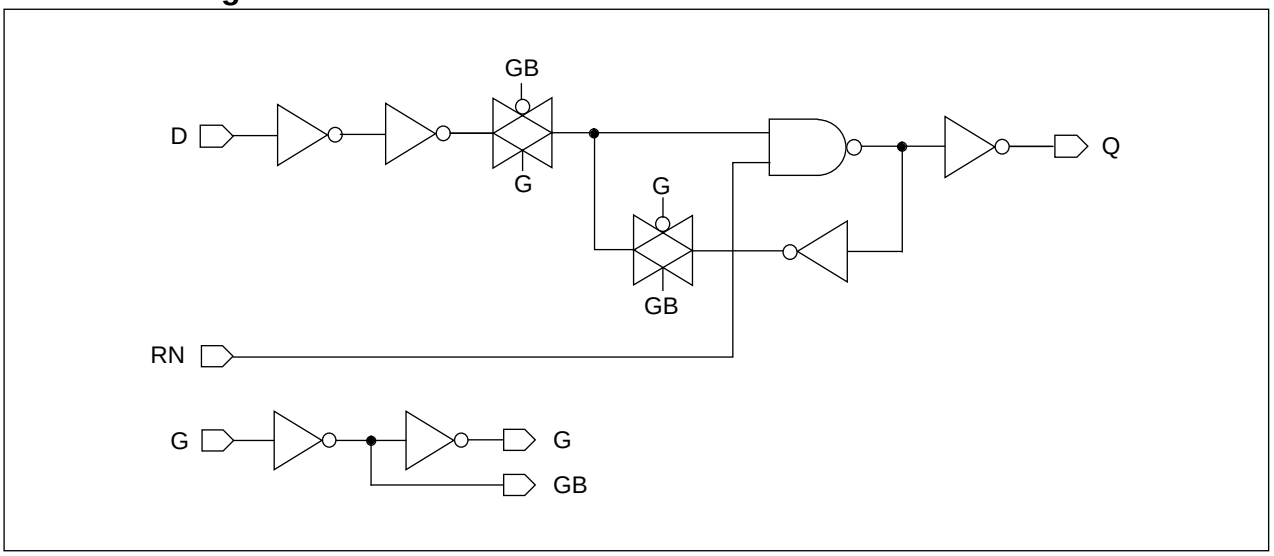
Truth Table

D	G	RN	Q (n+1)
0	1	1	0
1	1	1	1
x	0	1	Q (n)
x	x	0	0

Cell Data

Input Load (SL)						Gate Count	
STD80							
LD2Q			*LD2QD2*			*LD2Q*	*LD2QD2*
D	G	RN	D	G	RN		
0.6	0.6	0.5	0.6	0.6	0.8	4.3	4.7
STDM80							
LD2Q			*LD2QD2*			*LD2Q*	*LD2QD2*
D	G	RN	D	G	RN		
0.6	0.6	0.6	0.6	0.6	0.6	4.3	4.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD2Q	LD2QD2	LD2Q	LD2QD2
Pulse Width High (G)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Input Setup Time (D to G)	t_{SU}	0.55	0.57	0.71	0.74
Input Hold Time (D to G)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (RN to G)	t_{HD}	0.38	0.38	0.44	0.38

LD2Q/LD2QD2

D Latch with Active High, Reset, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD2Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.56	0.50 + 0.032*SL	0.51 + 0.026*SL	0.53 + 0.024*SL
	t_{PHL}	0.64	0.56 + 0.041*SL	0.56 + 0.037*SL	0.57 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
G to Q	t_{PLH}	0.57	0.51 + 0.031*SL	0.52 + 0.026*SL	0.54 + 0.024*SL
	t_{PHL}	0.60	0.52 + 0.040*SL	0.52 + 0.037*SL	0.53 + 0.037*SL
	t_R	0.22	0.13 + 0.047*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to Q	t_{PLH}	0.32	0.26 + 0.031*SL	0.27 + 0.026*SL	0.29 + 0.024*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.037*SL	0.28 + 0.037*SL
	t_R	0.23	0.13 + 0.046*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.066*SL	0.07 + 0.069*SL

STD80 LD2QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.58	0.54 + 0.021*SL	0.55 + 0.015*SL	0.58 + 0.012*SL
	t_{PHL}	0.63	0.58 + 0.023*SL	0.59 + 0.020*SL	0.61 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.024*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
G to Q	t_{PLH}	0.59	0.55 + 0.020*SL	0.56 + 0.016*SL	0.59 + 0.012*SL
	t_{PHL}	0.59	0.54 + 0.023*SL	0.55 + 0.020*SL	0.56 + 0.018*SL
	t_R	0.19	0.14 + 0.026*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.12 + 0.029*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
RN to Q	t_{PLH}	0.33	0.30 + 0.019*SL	0.30 + 0.016*SL	0.34 + 0.012*SL
	t_{PHL}	0.35	0.31 + 0.022*SL	0.31 + 0.019*SL	0.32 + 0.018*SL
	t_R	0.19	0.15 + 0.021*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.030*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD2Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.84	0.76 + 0.043*SL	0.78 + 0.037*SL	0.80 + 0.034*SL
	t_{PHL}	0.86	0.76 + 0.051*SL	0.78 + 0.046*SL	0.78 + 0.044*SL
	t_R	0.31	0.17 + 0.069*SL	0.18 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.078*SL	0.14 + 0.079*SL	0.13 + 0.082*SL
G to Q	t_{PLH}	0.85	0.76 + 0.043*SL	0.78 + 0.037*SL	0.80 + 0.034*SL
	t_{PHL}	0.85	0.75 + 0.051*SL	0.77 + 0.046*SL	0.78 + 0.044*SL
	t_R	0.31	0.17 + 0.069*SL	0.17 + 0.068*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.079*SL	0.14 + 0.079*SL	0.13 + 0.082*SL
RN to Q	t_{PLH}	0.43	0.34 + 0.042*SL	0.36 + 0.037*SL	0.38 + 0.034*SL
	t_{PHL}	0.46	0.36 + 0.051*SL	0.37 + 0.046*SL	0.38 + 0.044*SL
	t_R	0.30	0.16 + 0.070*SL	0.16 + 0.069*SL	0.15 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.079*SL	0.12 + 0.082*SL

STDM80 LD2QD2

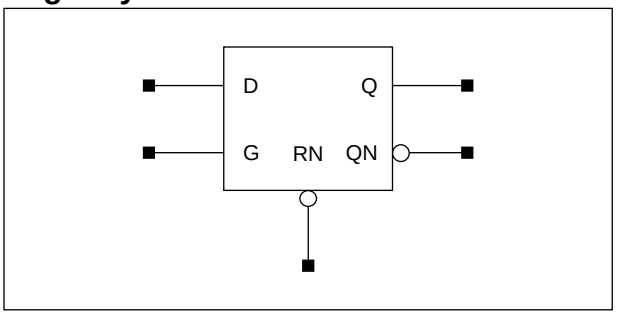
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.86	0.80 + 0.028*SL	0.82 + 0.023*SL	0.84 + 0.019*SL
	t_{PHL}	0.85	0.79 + 0.031*SL	0.81 + 0.026*SL	0.83 + 0.023*SL
	t_R	0.25	0.17 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.14 + 0.038*SL
G to Q	t_{PLH}	0.86	0.81 + 0.028*SL	0.82 + 0.022*SL	0.84 + 0.020*SL
	t_{PHL}	0.84	0.78 + 0.031*SL	0.80 + 0.026*SL	0.82 + 0.023*SL
	t_R	0.24	0.17 + 0.037*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.14 + 0.038*SL
RN to Q	t_{PLH}	0.44	0.38 + 0.027*SL	0.40 + 0.022*SL	0.42 + 0.019*SL
	t_{PHL}	0.45	0.39 + 0.030*SL	0.40 + 0.025*SL	0.42 + 0.023*SL
	t_R	0.24	0.16 + 0.037*SL	0.17 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.21	0.13 + 0.038*SL	0.14 + 0.038*SL	0.14 + 0.037*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 7, *Group3 : 7 < SL

YLD2/YLD2D2

Fast D Latch with Active High, Reset, 1X/2X Drive

Logic Symbol



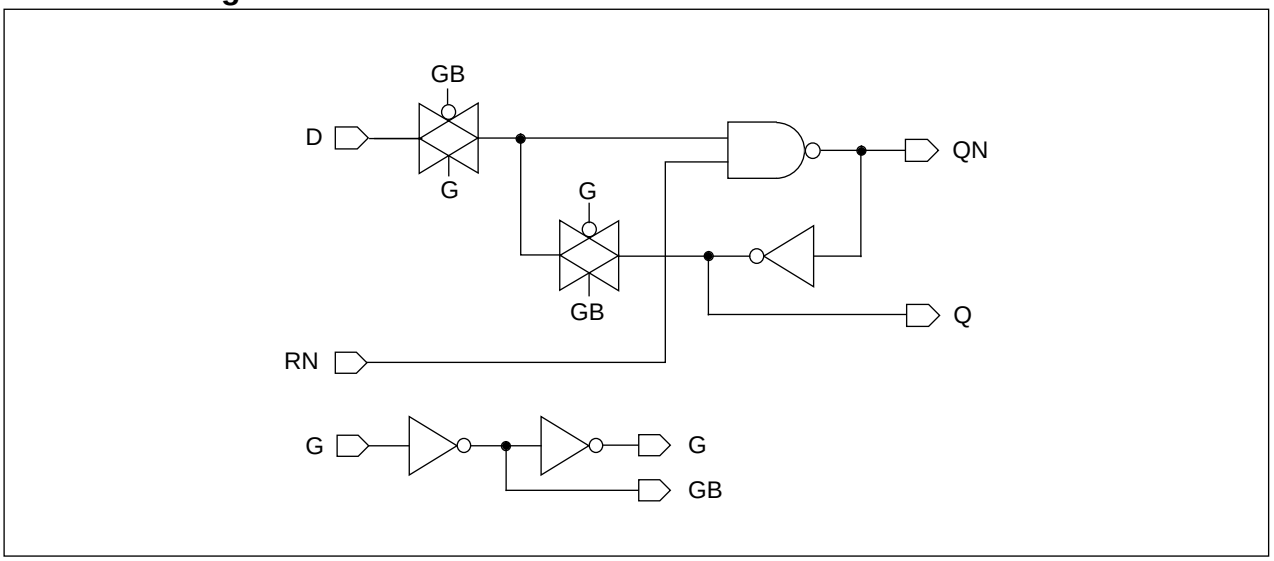
Truth Table

D	G	RN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
STD80							
YLD2			*YLD2D2*			*YLD2*	*YLD2D2*
D	G	RN	D	G	RN		
2.2	0.5	0.7	3.3	0.5	1.4	3.0	3.7
STDM80							
YLD2			*YLD2D2*			*YLD2*	*YLD2D2*
D	G	RN	D	G	RN		
2.5	0.6	0.8	3.6	0.6	1.6	3.0	3.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		YLD2	YLD2D2	YLD2	YLD2D2
Pulse Width High (G)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Input Setup Time (D to G)	t_{SU}	0.74	0.74	0.46	0.46
Input Hold Time (D to G)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.36	0.33	0.33	0.33
Input Hold Time (RN to G)	t_{HD}	0.38	0.44	0.33	0.49

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 YLD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.41	0.25 + 0.080*SL	0.26 + 0.077*SL	0.25 + 0.078*SL
	t_{PHL}	0.43	0.28 + 0.076*SL	0.29 + 0.073*SL	0.28 + 0.073*SL
	t_R	0.24	0.11 + 0.064*SL	0.11 + 0.067*SL	0.10 + 0.068*SL
	t_F	0.24	0.10 + 0.074*SL	0.09 + 0.076*SL	0.09 + 0.077*SL
G to Q	t_{PLH}	0.58	0.42 + 0.080*SL	0.43 + 0.079*SL	0.43 + 0.078*SL
	t_{PHL}	0.57	0.43 + 0.074*SL	0.43 + 0.073*SL	0.43 + 0.073*SL
	t_R	0.24	0.10 + 0.066*SL	0.10 + 0.068*SL	0.10 + 0.068*SL
	t_F	0.24	0.09 + 0.076*SL	0.09 + 0.077*SL	0.08 + 0.077*SL
RN to Q	t_{PLH}	0.37	0.21 + 0.078*SL	0.21 + 0.078*SL	0.21 + 0.078*SL
	t_{PHL}	0.42	0.25 + 0.083*SL	0.27 + 0.075*SL	0.29 + 0.073*SL
	t_R	0.24	0.11 + 0.064*SL	0.10 + 0.067*SL	0.10 + 0.068*SL
	t_F	0.38	0.24 + 0.070*SL	0.23 + 0.074*SL	0.22 + 0.076*SL
D to QN	t_{PLH}	0.26	0.20 + 0.027*SL	0.21 + 0.024*SL	0.20 + 0.025*SL
	t_{PHL}	0.28	0.20 + 0.039*SL	0.20 + 0.038*SL	0.19 + 0.038*SL
	t_R	0.33	0.25 + 0.040*SL	0.23 + 0.048*SL	0.17 + 0.054*SL
	t_F	0.41	0.28 + 0.063*SL	0.27 + 0.070*SL	0.19 + 0.078*SL
G to QN	t_{PLH}	0.40	0.35 + 0.025*SL	0.35 + 0.025*SL	0.35 + 0.025*SL
	t_{PHL}	0.45	0.37 + 0.040*SL	0.37 + 0.039*SL	0.37 + 0.039*SL
	t_R	0.26	0.17 + 0.047*SL	0.16 + 0.052*SL	0.14 + 0.054*SL
	t_F	0.35	0.21 + 0.071*SL	0.20 + 0.075*SL	0.17 + 0.078*SL
RN to QN	t_{PLH}	0.19	0.13 + 0.032*SL	0.14 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.24	0.16 + 0.040*SL	0.16 + 0.038*SL	0.16 + 0.038*SL
	t_R	0.32	0.24 + 0.040*SL	0.23 + 0.047*SL	0.17 + 0.053*SL
	t_F	0.40	0.27 + 0.067*SL	0.26 + 0.070*SL	0.19 + 0.078*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 YLD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.38	0.27 + 0.055*SL	0.27 + 0.052*SL	0.27 + 0.052*SL
	t_{PHL}	0.41	0.30 + 0.059*SL	0.30 + 0.056*SL	0.31 + 0.055*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.056*SL	0.09 + 0.058*SL
	t_F	0.23	0.09 + 0.069*SL	0.09 + 0.071*SL	0.08 + 0.071*SL
G to Q	t_{PLH}	0.56	0.45 + 0.054*SL	0.46 + 0.053*SL	0.46 + 0.052*SL
	t_{PHL}	0.56	0.45 + 0.057*SL	0.45 + 0.056*SL	0.45 + 0.055*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.057*SL	0.09 + 0.058*SL
	t_F	0.22	0.08 + 0.070*SL	0.08 + 0.071*SL	0.08 + 0.071*SL
RN to Q	t_{PLH}	0.29	0.18 + 0.057*SL	0.19 + 0.052*SL	0.19 + 0.052*SL
	t_{PHL}	0.37	0.23 + 0.070*SL	0.25 + 0.061*SL	0.30 + 0.055*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.057*SL	0.09 + 0.058*SL
	t_F	0.46	0.33 + 0.065*SL	0.32 + 0.069*SL	0.30 + 0.071*SL
D to QN	t_{PLH}	0.25	0.22 + 0.015*SL	0.22 + 0.013*SL	0.23 + 0.012*SL
	t_{PHL}	0.26	0.21 + 0.022*SL	0.22 + 0.019*SL	0.22 + 0.019*SL
	t_R	0.26	0.23 + 0.018*SL	0.22 + 0.022*SL	0.17 + 0.027*SL
	t_F	0.31	0.25 + 0.026*SL	0.24 + 0.032*SL	0.18 + 0.038*SL
G to QN	t_{PLH}	0.40	0.37 + 0.015*SL	0.37 + 0.013*SL	0.38 + 0.012*SL
	t_{PHL}	0.44	0.40 + 0.021*SL	0.40 + 0.020*SL	0.41 + 0.019*SL
	t_R	0.21	0.17 + 0.021*SL	0.16 + 0.024*SL	0.13 + 0.027*SL
	t_F	0.25	0.18 + 0.032*SL	0.17 + 0.036*SL	0.14 + 0.039*SL
RN to QN	t_{PLH}	0.14	0.10 + 0.020*SL	0.11 + 0.015*SL	0.14 + 0.012*SL
	t_{PHL}	0.18	0.13 + 0.023*SL	0.14 + 0.020*SL	0.14 + 0.019*SL
	t_R	0.26	0.21 + 0.022*SL	0.21 + 0.022*SL	0.16 + 0.027*SL
	t_F	0.28	0.23 + 0.029*SL	0.22 + 0.033*SL	0.16 + 0.039*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 YLD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.59	0.37 + 0.110*SL	0.37 + 0.109*SL	0.38 + 0.108*SL
	t_{PHL}	0.58	0.39 + 0.099*SL	0.39 + 0.098*SL	0.39 + 0.098*SL
	t_R	0.33	0.15 + 0.090*SL	0.14 + 0.091*SL	0.14 + 0.092*SL
	t_F	0.31	0.12 + 0.095*SL	0.12 + 0.095*SL	0.12 + 0.095*SL
G to Q	t_{PLH}	0.84	0.62 + 0.110*SL	0.62 + 0.109*SL	0.63 + 0.108*SL
	t_{PHL}	0.82	0.62 + 0.099*SL	0.62 + 0.099*SL	0.62 + 0.098*SL
	t_R	0.32	0.14 + 0.091*SL	0.14 + 0.092*SL	0.14 + 0.091*SL
	t_F	0.31	0.12 + 0.095*SL	0.12 + 0.095*SL	0.11 + 0.096*SL
RN to Q	t_{PLH}	0.49	0.27 + 0.109*SL	0.27 + 0.108*SL	0.28 + 0.108*SL
	t_{PHL}	0.53	0.32 + 0.105*SL	0.33 + 0.101*SL	0.34 + 0.100*SL
	t_R	0.32	0.14 + 0.091*SL	0.14 + 0.092*SL	0.14 + 0.092*SL
	t_F	0.49	0.31 + 0.089*SL	0.30 + 0.093*SL	0.29 + 0.094*SL
D to QN	t_{PLH}	0.35	0.28 + 0.035*SL	0.28 + 0.035*SL	0.28 + 0.035*SL
	t_{PHL}	0.38	0.28 + 0.052*SL	0.29 + 0.050*SL	0.29 + 0.050*SL
	t_R	0.38	0.24 + 0.068*SL	0.23 + 0.073*SL	0.21 + 0.075*SL
	t_F	0.48	0.31 + 0.085*SL	0.29 + 0.094*SL	0.26 + 0.097*SL
G to QN	t_{PLH}	0.58	0.51 + 0.035*SL	0.51 + 0.035*SL	0.51 + 0.035*SL
	t_{PHL}	0.63	0.53 + 0.052*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_R	0.37	0.23 + 0.070*SL	0.22 + 0.074*SL	0.20 + 0.075*SL
	t_F	0.46	0.28 + 0.090*SL	0.26 + 0.096*SL	0.24 + 0.098*SL
RN to QN	t_{PLH}	0.24	0.17 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.29	0.19 + 0.050*SL	0.19 + 0.050*SL	0.19 + 0.050*SL
	t_R	0.37	0.24 + 0.066*SL	0.22 + 0.071*SL	0.21 + 0.073*SL
	t_F	0.46	0.28 + 0.088*SL	0.26 + 0.094*SL	0.24 + 0.098*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

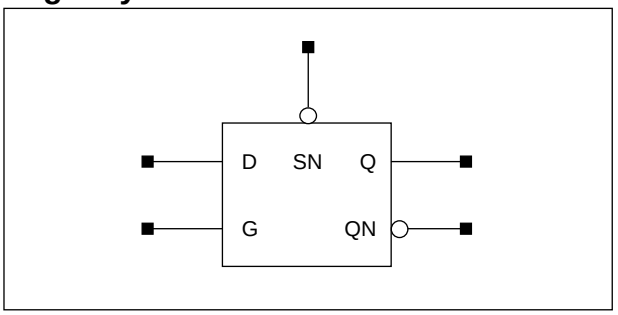
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 YLD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.55	0.39 + 0.077*SL	0.40 + 0.074*SL	0.41 + 0.073*SL
	t_{PHL}	0.56	0.41 + 0.075*SL	0.41 + 0.072*SL	0.42 + 0.072*SL
	t_R	0.29	0.13 + 0.079*SL	0.13 + 0.079*SL	0.13 + 0.079*SL
	t_F	0.29	0.11 + 0.086*SL	0.11 + 0.087*SL	0.11 + 0.087*SL
G to Q	t_{PLH}	0.83	0.67 + 0.077*SL	0.68 + 0.074*SL	0.69 + 0.073*SL
	t_{PHL}	0.79	0.64 + 0.075*SL	0.65 + 0.072*SL	0.66 + 0.072*SL
	t_R	0.29	0.13 + 0.079*SL	0.13 + 0.079*SL	0.13 + 0.079*SL
	t_F	0.29	0.11 + 0.087*SL	0.11 + 0.087*SL	0.11 + 0.087*SL
RN to Q	t_{PLH}	0.39	0.24 + 0.075*SL	0.24 + 0.073*SL	0.25 + 0.072*SL
	t_{PHL}	0.45	0.29 + 0.083*SL	0.31 + 0.077*SL	0.32 + 0.075*SL
	t_R	0.29	0.13 + 0.078*SL	0.12 + 0.080*SL	0.12 + 0.080*SL
	t_F	0.58	0.43 + 0.079*SL	0.41 + 0.083*SL	0.40 + 0.085*SL
D to QN	t_{PLH}	0.34	0.30 + 0.019*SL	0.31 + 0.018*SL	0.31 + 0.017*SL
	t_{PHL}	0.36	0.31 + 0.029*SL	0.31 + 0.027*SL	0.32 + 0.025*SL
	t_R	0.28	0.22 + 0.032*SL	0.21 + 0.034*SL	0.20 + 0.036*SL
	t_F	0.35	0.27 + 0.041*SL	0.26 + 0.044*SL	0.24 + 0.047*SL
G to QN	t_{PLH}	0.58	0.54 + 0.020*SL	0.54 + 0.018*SL	0.55 + 0.018*SL
	t_{PHL}	0.65	0.59 + 0.029*SL	0.59 + 0.027*SL	0.60 + 0.026*SL
	t_R	0.27	0.21 + 0.033*SL	0.20 + 0.035*SL	0.19 + 0.036*SL
	t_F	0.33	0.24 + 0.043*SL	0.23 + 0.046*SL	0.22 + 0.048*SL
RN to QN	t_{PLH}	0.18	0.14 + 0.022*SL	0.15 + 0.018*SL	0.16 + 0.017*SL
	t_{PHL}	0.21	0.16 + 0.028*SL	0.17 + 0.025*SL	0.17 + 0.025*SL
	t_R	0.27	0.21 + 0.030*SL	0.20 + 0.033*SL	0.18 + 0.035*SL
	t_F	0.30	0.22 + 0.041*SL	0.21 + 0.046*SL	0.20 + 0.047*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



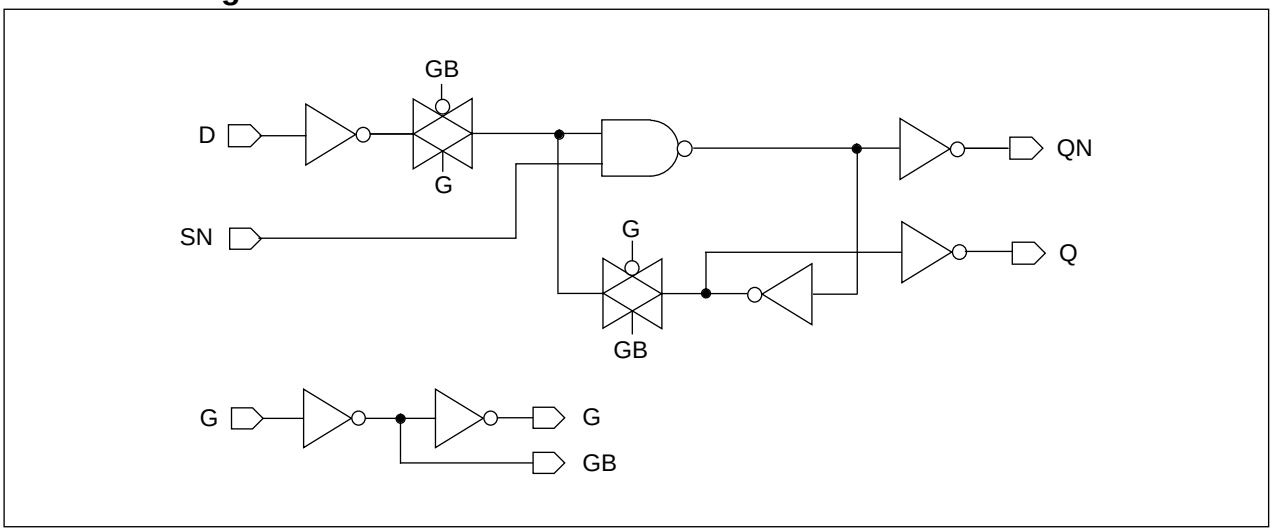
Truth Table

D	G	SN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	1	0

Cell Data

Input Load (SL)						Gate Count	
STD80							
LD3			*LD3D2*			*LD3*	*LD3D2*
D	G	SN	D	G	SN		
0.6	0.6	0.8	0.6	0.6	0.5	4.3	5.0
STDM80							
LD3			*LD3D2*			*LD3*	*LD3D2*
D	G	SN	D	G	SN		
0.6	0.6	0.6	0.6	0.6	0.6	4.3	5.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD3	LD3D2	LD3	LD3D2
Pulse Width High (G)	t_{PWH}	0.87	0.87	0.82	0.82
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.82	0.85
Input Setup Time (D to G)	t_{SU}	0.57	0.63	0.68	0.74
Input Hold Time (D to G)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to G)	t_{HD}	0.38	0.33	0.38	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.53	0.48 + 0.025*SL	0.48 + 0.024*SL	0.48 + 0.024*SL
	t_{PHL}	0.76	0.68 + 0.037*SL	0.68 + 0.037*SL	0.68 + 0.037*SL
	t_R	0.19	0.10 + 0.045*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
G to Q	t_{PLH}	0.64	0.59 + 0.025*SL	0.59 + 0.024*SL	0.59 + 0.024*SL
	t_{PHL}	0.75	0.68 + 0.037*SL	0.68 + 0.037*SL	0.68 + 0.037*SL
	t_R	0.19	0.09 + 0.048*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
SN to Q	t_{PLH}	0.47	0.41 + 0.030*SL	0.42 + 0.025*SL	0.43 + 0.024*SL
	t_{PHL}	0.51	0.43 + 0.037*SL	0.43 + 0.037*SL	0.43 + 0.037*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.22	0.10 + 0.060*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
D to QN	t_{PLH}	0.58	0.52 + 0.031*SL	0.53 + 0.026*SL	0.55 + 0.024*SL
	t_{PHL}	0.49	0.40 + 0.042*SL	0.41 + 0.038*SL	0.42 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
G to QN	t_{PLH}	0.58	0.51 + 0.032*SL	0.53 + 0.026*SL	0.55 + 0.024*SL
	t_{PHL}	0.60	0.52 + 0.042*SL	0.53 + 0.038*SL	0.53 + 0.037*SL
	t_R	0.23	0.13 + 0.049*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
SN to QN	t_{PLH}	0.33	0.27 + 0.031*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.23	0.14 + 0.045*SL	0.13 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.061*SL	0.10 + 0.066*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.59	0.56 + 0.014*SL	0.57 + 0.012*SL	0.57 + 0.012*SL
	t_{PHL}	0.84	0.80 + 0.018*SL	0.80 + 0.017*SL	0.79 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
G to Q	t_{PLH}	0.71	0.68 + 0.014*SL	0.68 + 0.012*SL	0.69 + 0.012*SL
	t_{PHL}	0.84	0.80 + 0.018*SL	0.80 + 0.017*SL	0.79 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
SN to Q	t_{PLH}	0.53	0.50 + 0.018*SL	0.51 + 0.014*SL	0.53 + 0.012*SL
	t_{PHL}	0.59	0.55 + 0.018*SL	0.55 + 0.017*SL	0.54 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
D to QN	t_{PLH}	0.59	0.55 + 0.021*SL	0.56 + 0.015*SL	0.59 + 0.012*SL
	t_{PHL}	0.48	0.43 + 0.023*SL	0.44 + 0.020*SL	0.46 + 0.018*SL
	t_R	0.20	0.15 + 0.025*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
G to QN	t_{PLH}	0.59	0.55 + 0.021*SL	0.56 + 0.015*SL	0.59 + 0.012*SL
	t_{PHL}	0.59	0.54 + 0.023*SL	0.55 + 0.020*SL	0.57 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.18	0.12 + 0.030*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.015*SL	0.35 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.75	0.68 + 0.035*SL	0.69 + 0.033*SL	0.69 + 0.033*SL
	t_{PHL}	1.04	0.95 + 0.047*SL	0.96 + 0.045*SL	0.96 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.14 + 0.076*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
G to Q	t_{PLH}	0.93	0.86 + 0.035*SL	0.87 + 0.033*SL	0.87 + 0.033*SL
	t_{PHL}	1.09	1.00 + 0.047*SL	1.00 + 0.045*SL	1.01 + 0.044*SL
	t_R	0.26	0.13 + 0.066*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
SN to Q	t_{PLH}	0.63	0.54 + 0.042*SL	0.56 + 0.036*SL	0.58 + 0.033*SL
	t_{PHL}	0.67	0.58 + 0.047*SL	0.59 + 0.045*SL	0.59 + 0.044*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
D to QN	t_{PLH}	0.81	0.72 + 0.044*SL	0.74 + 0.038*SL	0.76 + 0.035*SL
	t_{PHL}	0.68	0.57 + 0.052*SL	0.59 + 0.046*SL	0.60 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.068*SL	0.17 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.082*SL
G to QN	t_{PLH}	0.85	0.77 + 0.043*SL	0.78 + 0.038*SL	0.81 + 0.035*SL
	t_{PHL}	0.86	0.76 + 0.052*SL	0.77 + 0.046*SL	0.79 + 0.044*SL
	t_R	0.31	0.17 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.30	0.15 + 0.079*SL	0.14 + 0.080*SL	0.13 + 0.081*SL
SN to QN	t_{PLH}	0.44	0.35 + 0.043*SL	0.37 + 0.037*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.047*SL	0.40 + 0.045*SL
	t_R	0.31	0.17 + 0.071*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD3D2

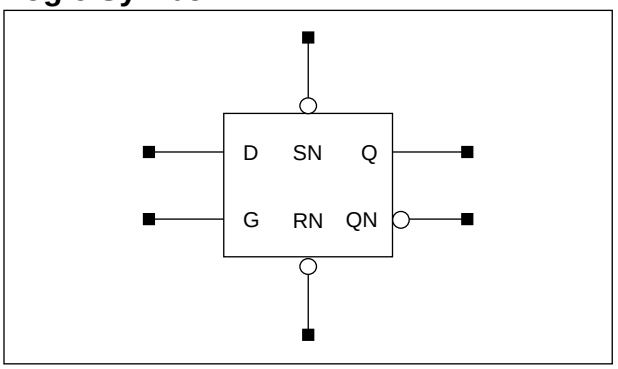
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.84	0.80 + 0.019*SL	0.81 + 0.017*SL	0.81 + 0.017*SL
	t_{PHL}	1.16	1.11 + 0.024*SL	1.11 + 0.022*SL	1.12 + 0.021*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.22	0.14 + 0.039*SL	0.14 + 0.038*SL	0.14 + 0.038*SL
G to Q	t_{PLH}	1.02	0.99 + 0.018*SL	0.99 + 0.018*SL	0.99 + 0.017*SL
	t_{PHL}	1.20	1.15 + 0.024*SL	1.16 + 0.022*SL	1.16 + 0.021*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.22	0.14 + 0.039*SL	0.14 + 0.037*SL	0.14 + 0.038*SL
SN to Q	t_{PLH}	0.71	0.66 + 0.023*SL	0.67 + 0.020*SL	0.68 + 0.018*SL
	t_{PHL}	0.78	0.73 + 0.025*SL	0.73 + 0.022*SL	0.74 + 0.021*SL
	t_R	0.23	0.16 + 0.036*SL	0.17 + 0.033*SL	0.17 + 0.033*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.037*SL	0.14 + 0.038*SL
D to QN	t_{PLH}	0.82	0.76 + 0.028*SL	0.78 + 0.023*SL	0.80 + 0.019*SL
	t_{PHL}	0.67	0.60 + 0.031*SL	0.62 + 0.026*SL	0.64 + 0.023*SL
	t_R	0.25	0.18 + 0.035*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.14 + 0.039*SL	0.15 + 0.038*SL
G to QN	t_{PLH}	0.87	0.81 + 0.028*SL	0.83 + 0.023*SL	0.85 + 0.019*SL
	t_{PHL}	0.85	0.79 + 0.031*SL	0.80 + 0.026*SL	0.82 + 0.023*SL
	t_R	0.25	0.18 + 0.036*SL	0.18 + 0.034*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.041*SL	0.14 + 0.039*SL	0.15 + 0.038*SL
SN to QN	t_{PLH}	0.44	0.39 + 0.027*SL	0.40 + 0.022*SL	0.43 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.21	0.13 + 0.042*SL	0.14 + 0.038*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

LD4/LD4D2

D Latch with Active High, Reset, Set, 1X/2X Drive

Logic Symbol



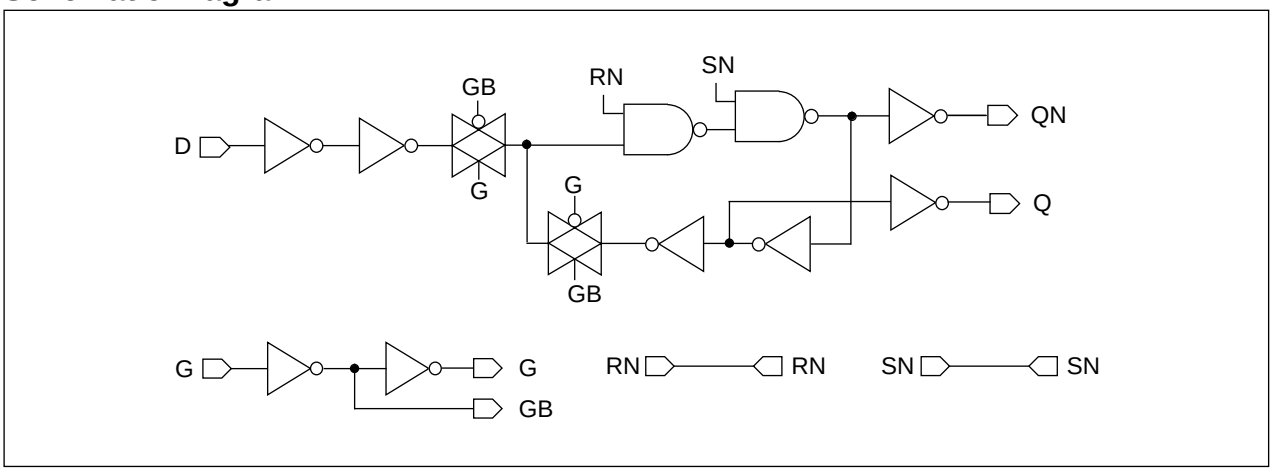
Truth Table

D	G	RN	SN	Q (n+1)	QN (n+1)
0	1	1	1	0	1
1	1	1	1	1	0
x	0	1	1	Q (n)	QN (n)
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0

Cell Data

Input Load (SL)								Gate Count	
STD80									
LD4				*LD4D2*				*LD4*	*LD4D2*
D	G	SN	RN	D	G	SN	RN		
0.6	0.6	0.8	0.6	0.6	0.6	0.8	0.4	6.0	6.7
STDM80									
LD4				*LD4D2*				*LD4*	*LD4D2*
D	G	SN	RN	D	G	SN	RN		
0.6	0.6	0.8	0.6	0.6	0.6	0.8	0.6	6.0	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD4	LD4D2	LD4	LD4D2
Pulse Width High (G)	t_{PWH}	0.87	0.87	0.82	0.85
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.90	1.01
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.82	0.87
Input Setup Time (D to G)	t_{SU}	0.63	0.71	0.74	0.87
Input Hold Time (D to G)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33	0.33	0.36
Input Hold Time (RN to G)	t_{HD}	0.38	0.33	0.38	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33	0.33	0.33
Input Hold Time (SN to G)	t_{HD}	0.44	0.33	0.49	0.38

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.74	0.69 + 0.028*SL	0.69 + 0.024*SL	0.70 + 0.024*SL
	t_{PHL}	0.96	0.89 + 0.038*SL	0.89 + 0.037*SL	0.89 + 0.037*SL
	t_R	0.19	0.11 + 0.043*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
G to Q	t_{PLH}	0.75	0.70 + 0.028*SL	0.70 + 0.024*SL	0.71 + 0.024*SL
	t_{PHL}	0.92	0.84 + 0.039*SL	0.85 + 0.037*SL	0.85 + 0.037*SL
	t_R	0.19	0.11 + 0.044*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.060*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
SN to Q	t_{PLH}	0.45	0.39 + 0.028*SL	0.40 + 0.024*SL	0.40 + 0.024*SL
	t_{PHL}	0.52	0.44 + 0.038*SL	0.44 + 0.037*SL	0.44 + 0.037*SL
	t_R	0.19	0.11 + 0.044*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to Q	t_{PLH}	0.50	0.45 + 0.028*SL	0.45 + 0.024*SL	0.46 + 0.024*SL
	t_{PHL}	0.68	0.61 + 0.039*SL	0.61 + 0.037*SL	0.61 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
D to QN	t_{PLH}	0.75	0.69 + 0.031*SL	0.70 + 0.026*SL	0.72 + 0.024*SL
	t_{PHL}	0.67	0.59 + 0.040*SL	0.60 + 0.038*SL	0.60 + 0.037*SL
	t_R	0.22	0.13 + 0.047*SL	0.12 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.23	0.10 + 0.066*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
G to QN	t_{PLH}	0.71	0.65 + 0.030*SL	0.66 + 0.026*SL	0.68 + 0.024*SL
	t_{PHL}	0.68	0.60 + 0.040*SL	0.61 + 0.038*SL	0.61 + 0.037*SL
	t_R	0.22	0.12 + 0.048*SL	0.12 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
SN to QN	t_{PLH}	0.31	0.25 + 0.030*SL	0.26 + 0.026*SL	0.28 + 0.024*SL
	t_{PHL}	0.38	0.30 + 0.039*SL	0.30 + 0.038*SL	0.31 + 0.037*SL
	t_R	0.23	0.13 + 0.046*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.067*SL	0.08 + 0.069*SL
RN to QN	t_{PLH}	0.48	0.41 + 0.031*SL	0.43 + 0.026*SL	0.45 + 0.024*SL
	t_{PHL}	0.43	0.35 + 0.040*SL	0.36 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.22	0.13 + 0.047*SL	0.12 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.81	0.78 + 0.014*SL	0.78 + 0.013*SL	0.79 + 0.012*SL
	t_{PHL}	1.04	1.00 + 0.019*SL	1.01 + 0.017*SL	1.00 + 0.018*SL
	t_R	0.16	0.11 + 0.023*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.030*SL	0.09 + 0.034*SL
G to Q	t_{PLH}	0.82	0.79 + 0.015*SL	0.79 + 0.013*SL	0.80 + 0.012*SL
	t_{PHL}	1.00	0.97 + 0.019*SL	0.97 + 0.017*SL	0.96 + 0.018*SL
	t_R	0.16	0.11 + 0.023*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.030*SL	0.09 + 0.034*SL
SN to Q	t_{PLH}	0.51	0.48 + 0.015*SL	0.49 + 0.013*SL	0.50 + 0.012*SL
	t_{PHL}	0.60	0.56 + 0.019*SL	0.56 + 0.017*SL	0.56 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.030*SL	0.09 + 0.034*SL
RN to Q	t_{PLH}	0.57	0.54 + 0.015*SL	0.54 + 0.013*SL	0.55 + 0.012*SL
	t_{PHL}	0.77	0.73 + 0.019*SL	0.73 + 0.017*SL	0.73 + 0.018*SL
	t_R	0.16	0.12 + 0.022*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
D to QN	t_{PLH}	0.77	0.72 + 0.021*SL	0.74 + 0.015*SL	0.77 + 0.012*SL
	t_{PHL}	0.67	0.62 + 0.023*SL	0.63 + 0.020*SL	0.64 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.024*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
G to QN	t_{PLH}	0.73	0.68 + 0.021*SL	0.70 + 0.015*SL	0.73 + 0.012*SL
	t_{PHL}	0.68	0.63 + 0.023*SL	0.64 + 0.020*SL	0.65 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.029*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SN to QN	t_{PLH}	0.32	0.28 + 0.020*SL	0.29 + 0.015*SL	0.32 + 0.012*SL
	t_{PHL}	0.37	0.33 + 0.023*SL	0.33 + 0.020*SL	0.35 + 0.018*SL
	t_R	0.19	0.15 + 0.022*SL	0.14 + 0.024*SL	0.12 + 0.026*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
RN to QN	t_{PLH}	0.49	0.45 + 0.021*SL	0.46 + 0.015*SL	0.49 + 0.012*SL
	t_{PHL}	0.43	0.38 + 0.023*SL	0.39 + 0.020*SL	0.40 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.024*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	1.10	1.03 + 0.037*SL	1.04 + 0.034*SL	1.04 + 0.033*SL
	t_{PHL}	1.33	1.24 + 0.049*SL	1.25 + 0.045*SL	1.25 + 0.044*SL
	t_R	0.27	0.13 + 0.067*SL	0.13 + 0.069*SL	0.11 + 0.071*SL
	t_F	0.30	0.15 + 0.077*SL	0.14 + 0.079*SL	0.13 + 0.081*SL
G to Q	t_{PLH}	1.10	1.03 + 0.037*SL	1.04 + 0.034*SL	1.04 + 0.033*SL
	t_{PHL}	1.32	1.23 + 0.049*SL	1.24 + 0.045*SL	1.25 + 0.044*SL
	t_R	0.27	0.13 + 0.067*SL	0.13 + 0.069*SL	0.11 + 0.071*SL
	t_F	0.30	0.15 + 0.078*SL	0.14 + 0.079*SL	0.13 + 0.081*SL
SN to Q	t_{PLH}	0.60	0.53 + 0.037*SL	0.54 + 0.034*SL	0.54 + 0.034*SL
	t_{PHL}	0.71	0.61 + 0.049*SL	0.62 + 0.045*SL	0.63 + 0.044*SL
	t_R	0.27	0.13 + 0.067*SL	0.12 + 0.070*SL	0.11 + 0.071*SL
	t_F	0.30	0.15 + 0.078*SL	0.14 + 0.079*SL	0.13 + 0.081*SL
RN to Q	t_{PLH}	0.71	0.63 + 0.037*SL	0.64 + 0.034*SL	0.65 + 0.033*SL
	t_{PHL}	0.93	0.83 + 0.049*SL	0.84 + 0.046*SL	0.85 + 0.044*SL
	t_R	0.27	0.13 + 0.067*SL	0.13 + 0.069*SL	0.11 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.079*SL	0.13 + 0.081*SL
D to QN	t_{PLH}	1.05	0.96 + 0.042*SL	0.98 + 0.037*SL	0.99 + 0.035*SL
	t_{PHL}	0.99	0.89 + 0.051*SL	0.90 + 0.046*SL	0.91 + 0.044*SL
	t_R	0.30	0.17 + 0.069*SL	0.17 + 0.070*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
G to QN	t_{PLH}	1.04	0.95 + 0.042*SL	0.97 + 0.037*SL	0.99 + 0.034*SL
	t_{PHL}	0.99	0.89 + 0.051*SL	0.90 + 0.046*SL	0.91 + 0.044*SL
	t_R	0.30	0.16 + 0.070*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
SN to QN	t_{PLH}	0.43	0.34 + 0.042*SL	0.36 + 0.037*SL	0.37 + 0.035*SL
	t_{PHL}	0.49	0.39 + 0.051*SL	0.40 + 0.046*SL	0.41 + 0.045*SL
	t_R	0.30	0.16 + 0.070*SL	0.16 + 0.070*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.082*SL	0.13 + 0.082*SL
RN to QN	t_{PLH}	0.65	0.56 + 0.042*SL	0.58 + 0.037*SL	0.59 + 0.034*SL
	t_{PHL}	0.60	0.50 + 0.051*SL	0.51 + 0.047*SL	0.52 + 0.044*SL
	t_R	0.30	0.16 + 0.070*SL	0.17 + 0.070*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

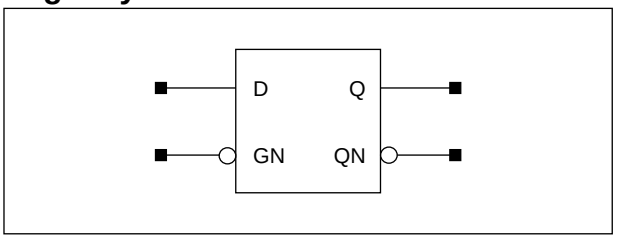
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	1.19	1.15 + 0.020*SL	1.16 + 0.018*SL	1.16 + 0.017*SL
	t_{PHL}	1.44	1.39 + 0.027*SL	1.40 + 0.023*SL	1.41 + 0.022*SL
	t_R	0.20	0.14 + 0.033*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.23	0.15 + 0.041*SL	0.16 + 0.037*SL	0.16 + 0.037*SL
G to Q	t_{PLH}	1.19	1.15 + 0.020*SL	1.16 + 0.018*SL	1.16 + 0.017*SL
	t_{PHL}	1.43	1.38 + 0.027*SL	1.39 + 0.023*SL	1.40 + 0.022*SL
	t_R	0.20	0.14 + 0.033*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.23	0.15 + 0.041*SL	0.16 + 0.037*SL	0.16 + 0.037*SL
SN to Q	t_{PLH}	0.69	0.65 + 0.020*SL	0.65 + 0.018*SL	0.66 + 0.017*SL
	t_{PHL}	0.82	0.76 + 0.027*SL	0.77 + 0.023*SL	0.78 + 0.022*SL
	t_R	0.20	0.14 + 0.033*SL	0.14 + 0.032*SL	0.13 + 0.034*SL
	t_F	0.23	0.15 + 0.041*SL	0.16 + 0.038*SL	0.16 + 0.037*SL
RN to Q	t_{PLH}	0.80	0.76 + 0.020*SL	0.77 + 0.018*SL	0.77 + 0.017*SL
	t_{PHL}	1.04	0.98 + 0.027*SL	0.99 + 0.023*SL	1.00 + 0.022*SL
	t_R	0.20	0.14 + 0.033*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.23	0.15 + 0.041*SL	0.15 + 0.039*SL	0.16 + 0.037*SL
D to QN	t_{PLH}	1.06	1.01 + 0.027*SL	1.03 + 0.022*SL	1.04 + 0.019*SL
	t_{PHL}	0.98	0.92 + 0.031*SL	0.94 + 0.026*SL	0.95 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_F	0.22	0.14 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
G to QN	t_{PLH}	1.06	1.00 + 0.027*SL	1.02 + 0.022*SL	1.03 + 0.019*SL
	t_{PHL}	0.98	0.92 + 0.031*SL	0.94 + 0.026*SL	0.95 + 0.023*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.039*SL
SN to QN	t_{PLH}	0.44	0.38 + 0.027*SL	0.40 + 0.022*SL	0.42 + 0.019*SL
	t_{PHL}	0.48	0.42 + 0.031*SL	0.43 + 0.026*SL	0.45 + 0.023*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_F	0.22	0.14 + 0.041*SL	0.15 + 0.038*SL	0.14 + 0.038*SL
RN to QN	t_{PLH}	0.66	0.61 + 0.027*SL	0.62 + 0.022*SL	0.64 + 0.019*SL
	t_{PHL}	0.59	0.53 + 0.031*SL	0.55 + 0.026*SL	0.56 + 0.023*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_F	0.22	0.14 + 0.039*SL	0.14 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Logic Symbol



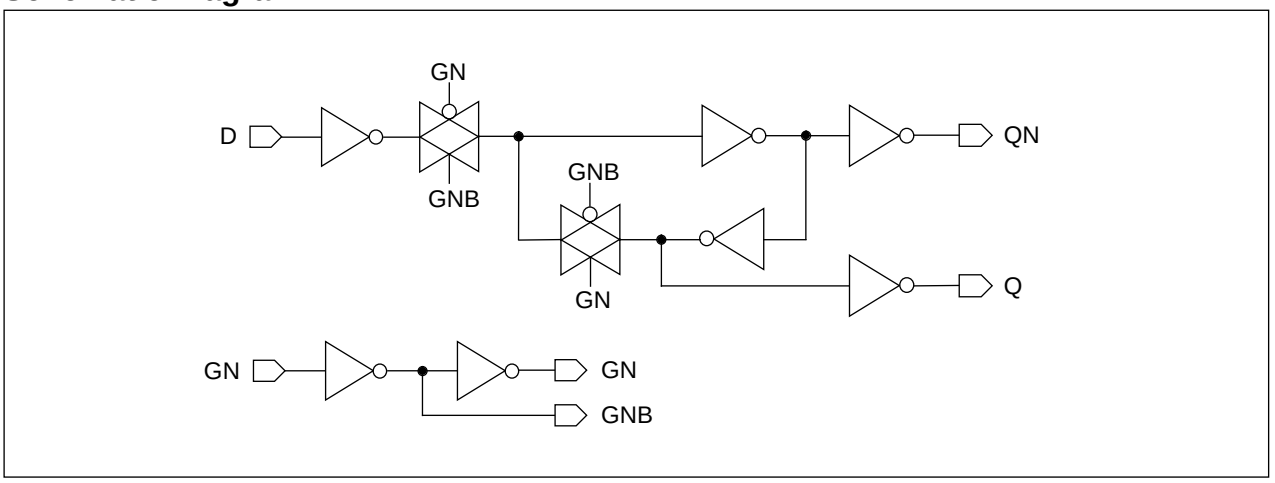
Truth Table

D	GN	Q (n+1)	QN (n+1)
0	0	0	1
1	0	1	0
x	1	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
STD80					
LD5		*LD5D2*		*LD5*	*LD5D2*
D	GN	D	GN		
0.5	0.5	0.6	0.6	4.0	4.7
STDM80					
LD5		*LD5D2*		*LD5*	*LD5D2*
D	GN	D	GN		
0.6	0.6	0.6	0.6	4.0	4.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD5	LD5D2	LD5	LD5D2
Pulse Width Low (GN)	t_{PWL}	0.87	0.87	0.85	0.90
Input Setup Time (D to GN)	t_{SU}	0.66	0.71	0.66	0.71
Input Hold Time (D to GN)	t_{HD}	0.33	0.33	0.33	0.33

LD5/LD5D2

D Latch with Active Low, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.51	0.46 + 0.025*SL	0.46 + 0.024*SL	0.46 + 0.024*SL
	t_{PHL}	0.70	0.62 + 0.038*SL	0.62 + 0.037*SL	0.62 + 0.037*SL
	t_R	0.19	0.09 + 0.045*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
GN to Q	t_{PLH}	0.67	0.62 + 0.026*SL	0.63 + 0.024*SL	0.63 + 0.024*SL
	t_{PHL}	0.81	0.74 + 0.038*SL	0.74 + 0.037*SL	0.74 + 0.037*SL
	t_R	0.18	0.09 + 0.047*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
D to QN	t_{PLH}	0.53	0.47 + 0.028*SL	0.48 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.47	0.39 + 0.041*SL	0.40 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
GN to QN	t_{PLH}	0.65	0.59 + 0.028*SL	0.60 + 0.024*SL	0.60 + 0.024*SL
	t_{PHL}	0.64	0.55 + 0.042*SL	0.56 + 0.038*SL	0.57 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

STD80 LD5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.57	0.55 + 0.013*SL	0.55 + 0.012*SL	0.55 + 0.012*SL
	t_{PHL}	0.75	0.72 + 0.018*SL	0.72 + 0.018*SL	0.71 + 0.018*SL
	t_R	0.15	0.11 + 0.019*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
GN to Q	t_{PLH}	0.74	0.71 + 0.014*SL	0.71 + 0.012*SL	0.72 + 0.012*SL
	t_{PHL}	0.87	0.83 + 0.018*SL	0.83 + 0.018*SL	0.83 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D to QN	t_{PLH}	0.53	0.50 + 0.018*SL	0.51 + 0.014*SL	0.52 + 0.012*SL
	t_{PHL}	0.46	0.41 + 0.023*SL	0.42 + 0.020*SL	0.44 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
GN to QN	t_{PLH}	0.65	0.62 + 0.018*SL	0.63 + 0.013*SL	0.64 + 0.012*SL
	t_{PHL}	0.62	0.58 + 0.023*SL	0.58 + 0.020*SL	0.60 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.029*SL	0.10 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.72	0.65 + 0.035*SL	0.65 + 0.033*SL	0.65 + 0.033*SL
	t_{PHL}	0.96	0.87 + 0.047*SL	0.88 + 0.044*SL	0.88 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
GN to Q	t_{PLH}	0.93	0.86 + 0.035*SL	0.87 + 0.033*SL	0.87 + 0.033*SL
	t_{PHL}	1.14	1.05 + 0.046*SL	1.06 + 0.045*SL	1.06 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D to QN	t_{PLH}	0.74	0.66 + 0.039*SL	0.67 + 0.035*SL	0.68 + 0.034*SL
	t_{PHL}	0.65	0.55 + 0.052*SL	0.56 + 0.046*SL	0.57 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
GN to QN	t_{PLH}	0.92	0.84 + 0.038*SL	0.85 + 0.035*SL	0.86 + 0.034*SL
	t_{PHL}	0.86	0.76 + 0.051*SL	0.77 + 0.046*SL	0.79 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

STDM80 LD5D2

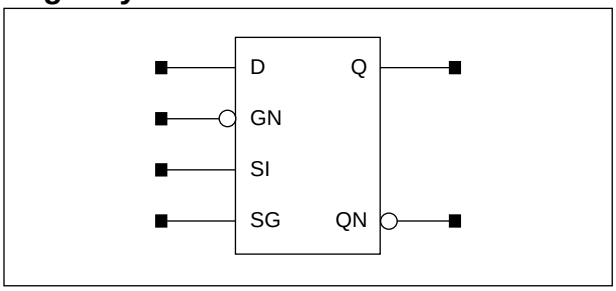
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.81	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.017*SL
	t_{PHL}	1.04	0.99 + 0.026*SL	1.00 + 0.023*SL	1.00 + 0.022*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
GN to Q	t_{PLH}	1.02	0.98 + 0.018*SL	0.99 + 0.017*SL	0.99 + 0.017*SL
	t_{PHL}	1.22	1.17 + 0.026*SL	1.18 + 0.023*SL	1.19 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D to QN	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.020*SL	0.72 + 0.018*SL
	t_{PHL}	0.64	0.57 + 0.030*SL	0.59 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
GN to QN	t_{PLH}	0.92	0.87 + 0.024*SL	0.88 + 0.020*SL	0.90 + 0.018*SL
	t_{PHL}	0.85	0.79 + 0.030*SL	0.80 + 0.026*SL	0.82 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

LD5S/LD5SD2

D Latch with Active Low, Scan, 1X/2X Drive

Logic Symbol



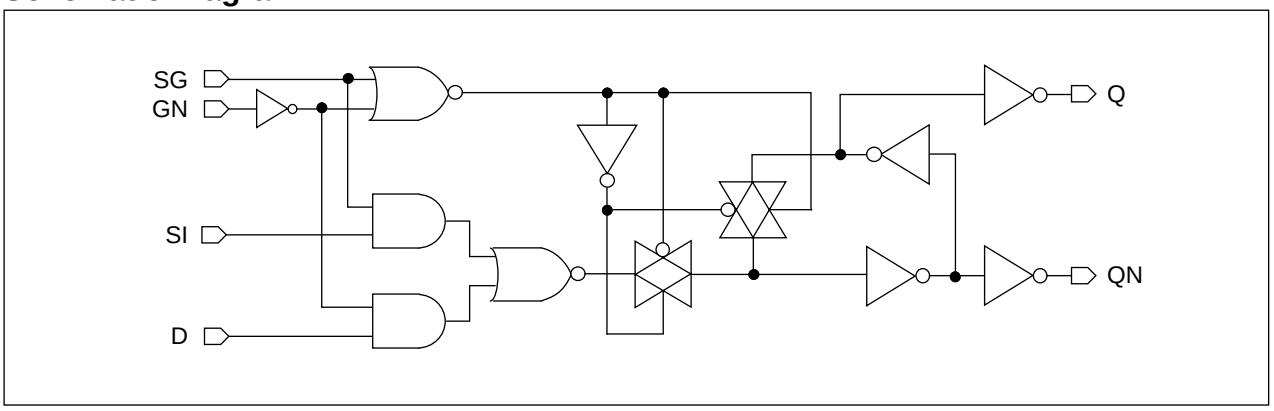
Truth Table

D	GN	SI	SG	Q (n+1)	QN (n+1)
x	1	x	0	Q (n)	QN (n)
x	x	1	1	1	0
x	1	0	1	0	1
1	0	x	x	1	0
0	0	x	0	0	1
0	0	0	1	0	1

Cell Data

Input Load (SL)								Gate Count	
STD80									
LD5S				*LD5SD2*				*LD5S*	*LD5SD2*
D	GN	SI	SG	D	GN	SI	SG		
0.3	0.5	0.5	1.0	0.3	0.5	0.5	1.0	6.0	6.7
STDM80									
LD5S				*LD5SD2*				*LD5S*	*LD5SD2*
D	GN	SI	SG	D	GN	SI	SG		
0.6	0.6	0.4	1.0	0.6	0.6	0.4	1.0	6.0	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD5S	LD5SD2	LD5S	LD5SD2
Pulse Width Low (GN)	t_{PWL}	0.90	0.90	1.04	1.09
Pulse Width High (SG)	t_{PWH}	0.87	0.96	0.93	0.96
Input Setup Time (D to GN)	t_{SU}	0.66	0.60	0.66	0.74
Input Hold Time (D to GN)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (SI to SG)	t_{SU}	0.60	0.63	0.74	0.82
Input Hold Time (SI to SG)	t_{HD}	0.33	0.33	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD5S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.62	0.57 + 0.025*SL	0.57 + 0.023*SL	0.57 + 0.024*SL
	t_{PHL}	0.79	0.72 + 0.037*SL	0.72 + 0.037*SL	0.72 + 0.037*SL
	t_R	0.18	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
SI to Q	t_{PLH}	0.68	0.63 + 0.025*SL	0.64 + 0.024*SL	0.63 + 0.024*SL
	t_{PHL}	0.85	0.78 + 0.037*SL	0.78 + 0.037*SL	0.78 + 0.037*SL
	t_R	0.18	0.09 + 0.047*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
GN to Q	t_{PLH}	0.91	0.86 + 0.025*SL	0.86 + 0.024*SL	0.86 + 0.024*SL
	t_{PHL}	0.95	0.87 + 0.038*SL	0.87 + 0.037*SL	0.87 + 0.037*SL
	t_R	0.19	0.09 + 0.047*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
SG to Q	t_{PLH}	0.73	0.68 + 0.025*SL	0.68 + 0.024*SL	0.68 + 0.024*SL
	t_{PHL}	0.75	0.67 + 0.038*SL	0.68 + 0.037*SL	0.67 + 0.037*SL
	t_R	0.18	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
D to QN	t_{PLH}	0.62	0.57 + 0.029*SL	0.58 + 0.024*SL	0.58 + 0.024*SL
	t_{PHL}	0.58	0.50 + 0.042*SL	0.51 + 0.038*SL	0.52 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
SI to QN	t_{PLH}	0.68	0.62 + 0.029*SL	0.63 + 0.024*SL	0.64 + 0.024*SL
	t_{PHL}	0.65	0.56 + 0.042*SL	0.57 + 0.038*SL	0.58 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.066*SL	0.08 + 0.069*SL
GN to QN	t_{PLH}	0.78	0.72 + 0.028*SL	0.73 + 0.024*SL	0.74 + 0.024*SL
	t_{PHL}	0.87	0.79 + 0.042*SL	0.80 + 0.038*SL	0.80 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
SG to QN	t_{PLH}	0.58	0.52 + 0.029*SL	0.53 + 0.024*SL	0.54 + 0.024*SL
	t_{PHL}	0.69	0.61 + 0.041*SL	0.62 + 0.038*SL	0.63 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD5SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.69	0.66 + 0.013*SL	0.66 + 0.012*SL	0.67 + 0.012*SL
	t_{PHL}	0.85	0.82 + 0.018*SL	0.82 + 0.018*SL	0.81 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.033*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
SI to Q	t_{PLH}	0.75	0.72 + 0.013*SL	0.73 + 0.012*SL	0.73 + 0.012*SL
	t_{PHL}	0.91	0.88 + 0.018*SL	0.88 + 0.017*SL	0.87 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
GN to Q	t_{PLH}	0.98	0.95 + 0.013*SL	0.95 + 0.012*SL	0.96 + 0.012*SL
	t_{PHL}	1.01	0.97 + 0.018*SL	0.97 + 0.018*SL	0.97 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
SG to Q	t_{PLH}	0.80	0.77 + 0.013*SL	0.78 + 0.012*SL	0.78 + 0.012*SL
	t_{PHL}	0.81	0.77 + 0.018*SL	0.77 + 0.018*SL	0.77 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D to QN	t_{PLH}	0.63	0.59 + 0.018*SL	0.60 + 0.014*SL	0.62 + 0.012*SL
	t_{PHL}	0.57	0.53 + 0.023*SL	0.54 + 0.020*SL	0.55 + 0.018*SL
	t_R	0.17	0.13 + 0.020*SL	0.13 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
SI to QN	t_{PLH}	0.69	0.65 + 0.019*SL	0.66 + 0.014*SL	0.68 + 0.012*SL
	t_{PHL}	0.64	0.59 + 0.023*SL	0.60 + 0.020*SL	0.61 + 0.018*SL
	t_R	0.18	0.14 + 0.019*SL	0.13 + 0.022*SL	0.10 + 0.026*SL
	t_F	0.18	0.11 + 0.031*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
GN to QN	t_{PLH}	0.79	0.75 + 0.018*SL	0.76 + 0.014*SL	0.78 + 0.012*SL
	t_{PHL}	0.86	0.82 + 0.023*SL	0.82 + 0.020*SL	0.84 + 0.018*SL
	t_R	0.17	0.12 + 0.022*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.12 + 0.029*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
SG to QN	t_{PLH}	0.59	0.55 + 0.018*SL	0.56 + 0.014*SL	0.58 + 0.012*SL
	t_{PHL}	0.69	0.64 + 0.023*SL	0.65 + 0.020*SL	0.66 + 0.018*SL
	t_R	0.17	0.12 + 0.022*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD5S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.88	0.81 + 0.035*SL	0.81 + 0.033*SL	0.81 + 0.033*SL
	t_{PHL}	1.16	1.06 + 0.046*SL	1.07 + 0.045*SL	1.07 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.10 + 0.083*SL
SI to Q	t_{PLH}	0.96	0.89 + 0.035*SL	0.89 + 0.033*SL	0.90 + 0.033*SL
	t_{PHL}	1.26	1.17 + 0.046*SL	1.18 + 0.044*SL	1.18 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
GN to Q	t_{PLH}	1.28	1.21 + 0.034*SL	1.21 + 0.033*SL	1.21 + 0.033*SL
	t_{PHL}	1.34	1.24 + 0.046*SL	1.25 + 0.045*SL	1.25 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
SG to Q	t_{PLH}	1.04	0.97 + 0.035*SL	0.98 + 0.033*SL	0.98 + 0.033*SL
	t_{PHL}	1.07	0.97 + 0.046*SL	0.98 + 0.045*SL	0.98 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.080*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
D to QN	t_{PLH}	0.93	0.85 + 0.040*SL	0.86 + 0.035*SL	0.87 + 0.034*SL
	t_{PHL}	0.81	0.71 + 0.052*SL	0.72 + 0.046*SL	0.74 + 0.044*SL
	t_R	0.30	0.17 + 0.064*SL	0.16 + 0.068*SL	0.14 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.079*SL	0.13 + 0.082*SL
SI to QN	t_{PLH}	1.03	0.95 + 0.040*SL	0.97 + 0.035*SL	0.98 + 0.034*SL
	t_{PHL}	0.89	0.79 + 0.052*SL	0.80 + 0.046*SL	0.82 + 0.044*SL
	t_R	0.30	0.17 + 0.066*SL	0.17 + 0.067*SL	0.14 + 0.070*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.079*SL	0.14 + 0.081*SL
GN to QN	t_{PLH}	1.11	1.03 + 0.039*SL	1.04 + 0.035*SL	1.05 + 0.034*SL
	t_{PHL}	1.21	1.10 + 0.052*SL	1.12 + 0.046*SL	1.13 + 0.045*SL
	t_R	0.29	0.15 + 0.066*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
SG to QN	t_{PLH}	0.84	0.76 + 0.039*SL	0.77 + 0.035*SL	0.78 + 0.034*SL
	t_{PHL}	0.97	0.87 + 0.052*SL	0.89 + 0.046*SL	0.90 + 0.044*SL
	t_R	0.29	0.15 + 0.067*SL	0.15 + 0.068*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.14 + 0.081*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

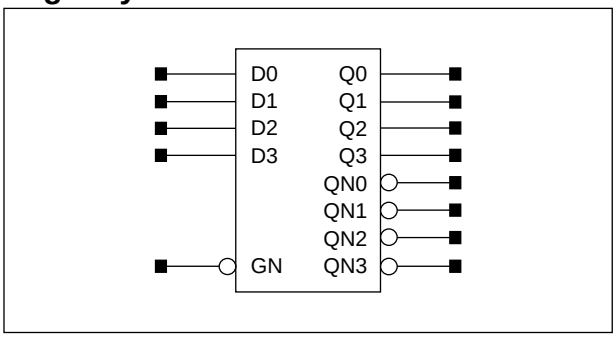
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD5SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.97	0.94 + 0.018*SL	0.94 + 0.017*SL	0.94 + 0.017*SL
	t_{PHL}	1.24	1.19 + 0.025*SL	1.20 + 0.023*SL	1.21 + 0.021*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
SI to Q	t_{PLH}	1.05	1.02 + 0.018*SL	1.02 + 0.017*SL	1.02 + 0.017*SL
	t_{PHL}	1.35	1.30 + 0.025*SL	1.31 + 0.022*SL	1.31 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.21	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
GN to Q	t_{PLH}	1.37	1.33 + 0.019*SL	1.34 + 0.017*SL	1.34 + 0.017*SL
	t_{PHL}	1.42	1.37 + 0.025*SL	1.38 + 0.023*SL	1.38 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
SG to Q	t_{PLH}	1.14	1.10 + 0.018*SL	1.10 + 0.017*SL	1.11 + 0.017*SL
	t_{PHL}	1.15	1.10 + 0.025*SL	1.10 + 0.023*SL	1.11 + 0.021*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D to QN	t_{PLH}	0.94	0.89 + 0.025*SL	0.90 + 0.020*SL	0.92 + 0.018*SL
	t_{PHL}	0.80	0.74 + 0.031*SL	0.75 + 0.026*SL	0.77 + 0.023*SL
	t_R	0.23	0.16 + 0.034*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
SI to QN	t_{PLH}	1.04	0.99 + 0.025*SL	1.01 + 0.020*SL	1.03 + 0.018*SL
	t_{PHL}	0.88	0.82 + 0.031*SL	0.83 + 0.026*SL	0.85 + 0.023*SL
	t_R	0.23	0.16 + 0.034*SL	0.17 + 0.032*SL	0.16 + 0.033*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
GN to QN	t_{PLH}	1.11	1.07 + 0.024*SL	1.08 + 0.020*SL	1.10 + 0.018*SL
	t_{PHL}	1.20	1.14 + 0.031*SL	1.15 + 0.026*SL	1.17 + 0.023*SL
	t_R	0.22	0.15 + 0.033*SL	0.15 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
SG to QN	t_{PLH}	0.84	0.79 + 0.024*SL	0.81 + 0.020*SL	0.82 + 0.018*SL
	t_{PHL}	0.96	0.90 + 0.031*SL	0.92 + 0.026*SL	0.94 + 0.023*SL
	t_R	0.22	0.15 + 0.032*SL	0.15 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.14 + 0.041*SL	0.15 + 0.038*SL	0.15 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

Dn	GN	Qn (n+1)	QNn (n+1)
0	0	0	1
1	0	1	0
x	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count	
STD80					
LD5X4		*LD5X4D2*		*LD5X4*	*LD5X4D2*
Dn	GN	Dn	GN		
0.5	0.5	0.5	0.5	13.0	15.3
STDM80					
LD5X4		*LD5X4D2*		*LD5X4*	*LD5X4D2*
Dn	GN	Dn	GN		
0.6	0.6	0.6	0.6	13.0	15.3

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD5X4	LD5X4D2	LD5X4	LD5X4D2
Pulse Width Low (GN)	t_{PWL}	0.90	0.87	1.09	1.15
Input Setup Time (D0 to GN)	t_{SU}	0.45	0.74	0.46	0.52
Input Hold Time (D0 to GN)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (D1 to GN)	t_{SU}	0.45	0.52	0.46	0.52
Input Hold Time (D1 to GN)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (D2 to GN)	t_{SU}	0.45	0.52	0.49	0.52
Input Hold Time (D2 to GN)	t_{HD}	0.33	0.33	0.33	0.33
Input Setup Time (D3 to GN)	t_{SU}	0.45	0.52	0.46	0.52
Input Hold Time (D3 to GN)	t_{HD}	0.33	0.33	0.33	0.36

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.51	0.46 + 0.025*SL	0.46 + 0.024*SL	0.46 + 0.024*SL
	t_{PHL}	0.70	0.62 + 0.038*SL	0.62 + 0.037*SL	0.62 + 0.037*SL
	t_R	0.18	0.09 + 0.047*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
GN to Q0	t_{PLH}	0.81	0.76 + 0.025*SL	0.76 + 0.024*SL	0.76 + 0.024*SL
	t_{PHL}	1.06	0.98 + 0.038*SL	0.98 + 0.037*SL	0.98 + 0.037*SL
	t_R	0.18	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
D1 to Q1	t_{PLH}	0.51	0.46 + 0.025*SL	0.46 + 0.024*SL	0.46 + 0.024*SL
	t_{PHL}	0.70	0.63 + 0.037*SL	0.63 + 0.037*SL	0.63 + 0.037*SL
	t_R	0.19	0.09 + 0.046*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
GN to Q1	t_{PLH}	0.81	0.76 + 0.025*SL	0.77 + 0.024*SL	0.77 + 0.024*SL
	t_{PHL}	1.06	0.98 + 0.038*SL	0.99 + 0.037*SL	0.99 + 0.037*SL
	t_R	0.19	0.09 + 0.046*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
D2 to Q2	t_{PLH}	0.51	0.46 + 0.025*SL	0.46 + 0.024*SL	0.46 + 0.024*SL
	t_{PHL}	0.70	0.63 + 0.038*SL	0.63 + 0.037*SL	0.63 + 0.037*SL
	t_R	0.19	0.10 + 0.043*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
GN to Q2	t_{PLH}	0.82	0.77 + 0.025*SL	0.77 + 0.024*SL	0.77 + 0.024*SL
	t_{PHL}	1.06	0.98 + 0.037*SL	0.98 + 0.037*SL	0.98 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
D3 to Q3	t_{PLH}	0.51	0.46 + 0.025*SL	0.46 + 0.024*SL	0.46 + 0.024*SL
	t_{PHL}	0.70	0.62 + 0.038*SL	0.62 + 0.037*SL	0.62 + 0.037*SL
	t_R	0.18	0.09 + 0.046*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
GN to Q3	t_{PLH}	0.81	0.76 + 0.025*SL	0.76 + 0.024*SL	0.76 + 0.024*SL
	t_{PHL}	1.06	0.98 + 0.038*SL	0.98 + 0.037*SL	0.98 + 0.037*SL
	t_R	0.18	0.09 + 0.046*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
D0 to QN0	t_{PLH}	0.53	0.47 + 0.028*SL	0.48 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.47	0.39 + 0.042*SL	0.40 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
GN to QN0	t_{PLH}	0.89	0.83 + 0.028*SL	0.84 + 0.024*SL	0.85 + 0.024*SL
	t_{PHL}	0.77	0.69 + 0.041*SL	0.70 + 0.038*SL	0.71 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.53	0.47 + 0.029*SL	0.48 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.47	0.39 + 0.041*SL	0.40 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
GN to QN1	t_{PLH}	0.89	0.83 + 0.028*SL	0.84 + 0.024*SL	0.85 + 0.024*SL
	t_{PHL}	0.78	0.69 + 0.042*SL	0.70 + 0.038*SL	0.71 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
D2 to QN2	t_{PLH}	0.53	0.47 + 0.028*SL	0.48 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.47	0.39 + 0.042*SL	0.40 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.061*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
GN to QN2	t_{PLH}	0.89	0.83 + 0.028*SL	0.84 + 0.024*SL	0.85 + 0.024*SL
	t_{PHL}	0.78	0.69 + 0.042*SL	0.70 + 0.038*SL	0.71 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
D3 to QN3	t_{PLH}	0.53	0.47 + 0.028*SL	0.48 + 0.024*SL	0.49 + 0.024*SL
	t_{PHL}	0.47	0.39 + 0.042*SL	0.40 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
GN to QN3	t_{PLH}	0.89	0.83 + 0.028*SL	0.84 + 0.024*SL	0.85 + 0.024*SL
	t_{PHL}	0.77	0.69 + 0.041*SL	0.70 + 0.038*SL	0.71 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD5X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.57	0.54 + 0.014*SL	0.55 + 0.012*SL	0.55 + 0.012*SL
	t_{PHL}	0.75	0.72 + 0.018*SL	0.72 + 0.018*SL	0.71 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
GN to Q0	t_{PLH}	0.88	0.85 + 0.013*SL	0.86 + 0.012*SL	0.86 + 0.012*SL
	t_{PHL}	1.12	1.08 + 0.018*SL	1.09 + 0.018*SL	1.08 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D1 to Q1	t_{PLH}	0.57	0.55 + 0.014*SL	0.55 + 0.012*SL	0.56 + 0.012*SL
	t_{PHL}	0.76	0.72 + 0.018*SL	0.72 + 0.018*SL	0.72 + 0.018*SL
	t_R	0.15	0.11 + 0.019*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.029*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
GN to Q1	t_{PLH}	0.88	0.86 + 0.013*SL	0.86 + 0.012*SL	0.86 + 0.012*SL
	t_{PHL}	1.12	1.09 + 0.018*SL	1.09 + 0.018*SL	1.08 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D2 to Q2	t_{PLH}	0.57	0.55 + 0.014*SL	0.55 + 0.012*SL	0.56 + 0.012*SL
	t_{PHL}	0.76	0.72 + 0.019*SL	0.72 + 0.018*SL	0.72 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
GN to Q2	t_{PLH}	0.89	0.86 + 0.013*SL	0.86 + 0.012*SL	0.87 + 0.012*SL
	t_{PHL}	1.12	1.08 + 0.018*SL	1.09 + 0.018*SL	1.08 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D3 to Q3	t_{PLH}	0.57	0.54 + 0.014*SL	0.55 + 0.012*SL	0.55 + 0.012*SL
	t_{PHL}	0.75	0.72 + 0.018*SL	0.72 + 0.018*SL	0.71 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
GN to Q3	t_{PLH}	0.88	0.85 + 0.013*SL	0.86 + 0.012*SL	0.86 + 0.012*SL
	t_{PHL}	1.12	1.08 + 0.018*SL	1.09 + 0.018*SL	1.08 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D0 to QN0	t_{PLH}	0.54	0.50 + 0.018*SL	0.51 + 0.013*SL	0.52 + 0.012*SL
	t_{PHL}	0.46	0.41 + 0.023*SL	0.42 + 0.020*SL	0.44 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.033*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
GN to QN0	t_{PLH}	0.90	0.87 + 0.018*SL	0.88 + 0.014*SL	0.89 + 0.012*SL
	t_{PHL}	0.77	0.72 + 0.023*SL	0.73 + 0.020*SL	0.74 + 0.018*SL
	t_R	0.16	0.12 + 0.022*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.10 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD5X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.54	0.50 + 0.018*SL	0.51 + 0.014*SL	0.53 + 0.012*SL
	t_{PHL}	0.46	0.41 + 0.023*SL	0.42 + 0.020*SL	0.44 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
GN to QN1	t_{PLH}	0.90	0.87 + 0.018*SL	0.88 + 0.013*SL	0.89 + 0.012*SL
	t_{PHL}	0.77	0.72 + 0.023*SL	0.73 + 0.020*SL	0.75 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.10 + 0.031*SL	0.08 + 0.034*SL
D2 to QN2	t_{PLH}	0.54	0.50 + 0.018*SL	0.51 + 0.013*SL	0.52 + 0.012*SL
	t_{PHL}	0.46	0.41 + 0.023*SL	0.42 + 0.020*SL	0.44 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.033*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
GN to QN2	t_{PLH}	0.90	0.86 + 0.018*SL	0.87 + 0.014*SL	0.89 + 0.012*SL
	t_{PHL}	0.77	0.73 + 0.023*SL	0.73 + 0.020*SL	0.75 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.11 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.10 + 0.031*SL	0.08 + 0.034*SL
D3 to QN3	t_{PLH}	0.54	0.50 + 0.018*SL	0.51 + 0.013*SL	0.52 + 0.012*SL
	t_{PHL}	0.46	0.41 + 0.023*SL	0.42 + 0.020*SL	0.44 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.033*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
GN to QN3	t_{PLH}	0.90	0.87 + 0.018*SL	0.88 + 0.014*SL	0.89 + 0.012*SL
	t_{PHL}	0.77	0.72 + 0.023*SL	0.73 + 0.020*SL	0.74 + 0.018*SL
	t_R	0.16	0.12 + 0.022*SL	0.12 + 0.023*SL	0.09 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.10 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.72	0.65 + 0.035*SL	0.65 + 0.033*SL	0.65 + 0.033*SL
	t_{PHL}	0.96	0.87 + 0.047*SL	0.88 + 0.044*SL	0.88 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
GN to Q0	t_{PLH}	1.15	1.08 + 0.034*SL	1.08 + 0.033*SL	1.08 + 0.033*SL
	t_{PHL}	1.51	1.41 + 0.047*SL	1.42 + 0.044*SL	1.42 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D1 to Q1	t_{PLH}	0.72	0.65 + 0.034*SL	0.66 + 0.033*SL	0.66 + 0.033*SL
	t_{PHL}	0.97	0.87 + 0.046*SL	0.88 + 0.045*SL	0.88 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.28	0.13 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
GN to Q1	t_{PLH}	1.15	1.08 + 0.034*SL	1.09 + 0.033*SL	1.09 + 0.033*SL
	t_{PHL}	1.51	1.42 + 0.047*SL	1.42 + 0.045*SL	1.43 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.28	0.13 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D2 to Q2	t_{PLH}	0.72	0.65 + 0.035*SL	0.66 + 0.033*SL	0.66 + 0.033*SL
	t_{PHL}	0.97	0.87 + 0.047*SL	0.88 + 0.044*SL	0.88 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.28	0.13 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.083*SL
GN to Q2	t_{PLH}	1.16	1.09 + 0.035*SL	1.09 + 0.033*SL	1.09 + 0.033*SL
	t_{PHL}	1.51	1.42 + 0.046*SL	1.42 + 0.045*SL	1.42 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.12 + 0.070*SL	0.11 + 0.072*SL
	t_F	0.28	0.13 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D3 to Q3	t_{PLH}	0.72	0.65 + 0.035*SL	0.65 + 0.033*SL	0.65 + 0.033*SL
	t_{PHL}	0.96	0.87 + 0.046*SL	0.87 + 0.045*SL	0.88 + 0.044*SL
	t_R	0.26	0.12 + 0.068*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.10 + 0.083*SL
GN to Q3	t_{PLH}	1.15	1.08 + 0.035*SL	1.08 + 0.033*SL	1.08 + 0.033*SL
	t_{PHL}	1.51	1.41 + 0.047*SL	1.42 + 0.045*SL	1.42 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D0 to QN0	t_{PLH}	0.74	0.66 + 0.038*SL	0.67 + 0.035*SL	0.68 + 0.034*SL
	t_{PHL}	0.65	0.55 + 0.052*SL	0.56 + 0.046*SL	0.57 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
GN to QN0	t_{PLH}	1.28	1.20 + 0.038*SL	1.21 + 0.035*SL	1.22 + 0.034*SL
	t_{PHL}	1.08	0.97 + 0.052*SL	0.99 + 0.046*SL	1.00 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.74	0.66 + 0.038*SL	0.67 + 0.035*SL	0.68 + 0.034*SL
	t_{PHL}	0.65	0.55 + 0.052*SL	0.56 + 0.046*SL	0.57 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
GN to QN1	t_{PLH}	1.28	1.20 + 0.039*SL	1.22 + 0.035*SL	1.22 + 0.034*SL
	t_{PHL}	1.08	0.98 + 0.052*SL	0.99 + 0.046*SL	1.01 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
D2 to QN2	t_{PLH}	0.74	0.66 + 0.038*SL	0.67 + 0.035*SL	0.68 + 0.034*SL
	t_{PHL}	0.65	0.55 + 0.052*SL	0.56 + 0.046*SL	0.57 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
GN to QN2	t_{PLH}	1.28	1.20 + 0.038*SL	1.21 + 0.035*SL	1.22 + 0.034*SL
	t_{PHL}	1.08	0.98 + 0.052*SL	1.00 + 0.046*SL	1.01 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
D3 to QN3	t_{PLH}	0.74	0.66 + 0.038*SL	0.67 + 0.035*SL	0.68 + 0.034*SL
	t_{PHL}	0.65	0.55 + 0.052*SL	0.56 + 0.046*SL	0.57 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
GN to QN3	t_{PLH}	1.28	1.20 + 0.039*SL	1.22 + 0.035*SL	1.22 + 0.034*SL
	t_{PHL}	1.08	0.97 + 0.052*SL	0.99 + 0.046*SL	1.00 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD5X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.81	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.017*SL
	t_{PHL}	1.04	0.99 + 0.026*SL	1.00 + 0.023*SL	1.01 + 0.021*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
GN to Q0	t_{PLH}	1.24	1.21 + 0.019*SL	1.21 + 0.017*SL	1.22 + 0.017*SL
	t_{PHL}	1.60	1.54 + 0.026*SL	1.55 + 0.023*SL	1.56 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D1 to Q1	t_{PLH}	0.81	0.77 + 0.019*SL	0.78 + 0.017*SL	0.78 + 0.017*SL
	t_{PHL}	1.04	0.99 + 0.026*SL	1.00 + 0.023*SL	1.01 + 0.022*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
GN to Q1	t_{PLH}	1.25	1.21 + 0.018*SL	1.21 + 0.017*SL	1.22 + 0.017*SL
	t_{PHL}	1.60	1.55 + 0.025*SL	1.55 + 0.023*SL	1.56 + 0.022*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D2 to Q2	t_{PLH}	0.81	0.77 + 0.018*SL	0.78 + 0.017*SL	0.78 + 0.017*SL
	t_{PHL}	1.04	0.99 + 0.026*SL	1.00 + 0.023*SL	1.01 + 0.022*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
GN to Q2	t_{PLH}	1.25	1.21 + 0.019*SL	1.22 + 0.017*SL	1.22 + 0.017*SL
	t_{PHL}	1.60	1.54 + 0.025*SL	1.55 + 0.023*SL	1.56 + 0.022*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D3 to Q3	t_{PLH}	0.81	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.017*SL
	t_{PHL}	1.04	0.99 + 0.026*SL	1.00 + 0.023*SL	1.00 + 0.022*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
GN to Q3	t_{PLH}	1.24	1.21 + 0.019*SL	1.21 + 0.017*SL	1.22 + 0.017*SL
	t_{PHL}	1.60	1.54 + 0.026*SL	1.55 + 0.023*SL	1.56 + 0.022*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.032*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D0 to QN0	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.020*SL	0.72 + 0.018*SL
	t_{PHL}	0.63	0.57 + 0.031*SL	0.59 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
GN to QN0	t_{PLH}	1.30	1.25 + 0.024*SL	1.26 + 0.020*SL	1.28 + 0.018*SL
	t_{PHL}	1.07	1.01 + 0.031*SL	1.03 + 0.026*SL	1.04 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD5X4D2

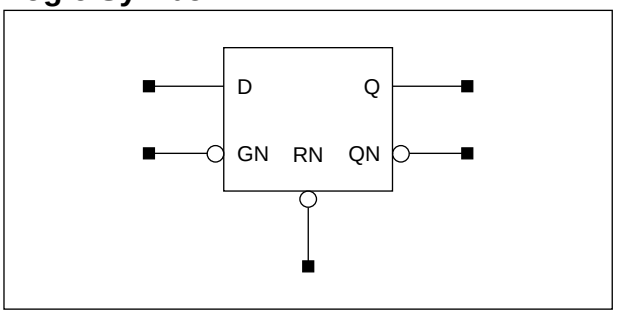
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.020*SL	0.72 + 0.018*SL
	t_{PHL}	0.64	0.57 + 0.030*SL	0.59 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.21	0.15 + 0.032*SL	0.15 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
GN to QN1	t_{PLH}	1.30	1.25 + 0.024*SL	1.26 + 0.020*SL	1.28 + 0.018*SL
	t_{PHL}	1.07	1.01 + 0.030*SL	1.03 + 0.026*SL	1.04 + 0.023*SL
	t_R	0.21	0.14 + 0.032*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
D2 to QN2	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.020*SL	0.72 + 0.018*SL
	t_{PHL}	0.64	0.57 + 0.030*SL	0.59 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.15 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
GN to QN2	t_{PLH}	1.29	1.24 + 0.024*SL	1.26 + 0.020*SL	1.27 + 0.018*SL
	t_{PHL}	1.08	1.02 + 0.030*SL	1.03 + 0.026*SL	1.05 + 0.023*SL
	t_R	0.21	0.15 + 0.032*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
D3 to QN3	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.020*SL	0.72 + 0.018*SL
	t_{PHL}	0.63	0.57 + 0.030*SL	0.59 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
GN to QN3	t_{PLH}	1.30	1.25 + 0.024*SL	1.26 + 0.020*SL	1.28 + 0.018*SL
	t_{PHL}	1.07	1.01 + 0.031*SL	1.03 + 0.026*SL	1.04 + 0.023*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.14 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

LD6/LD6D2

D Latch with Active Low, Reset, 1X/2X Drive

Logic Symbol



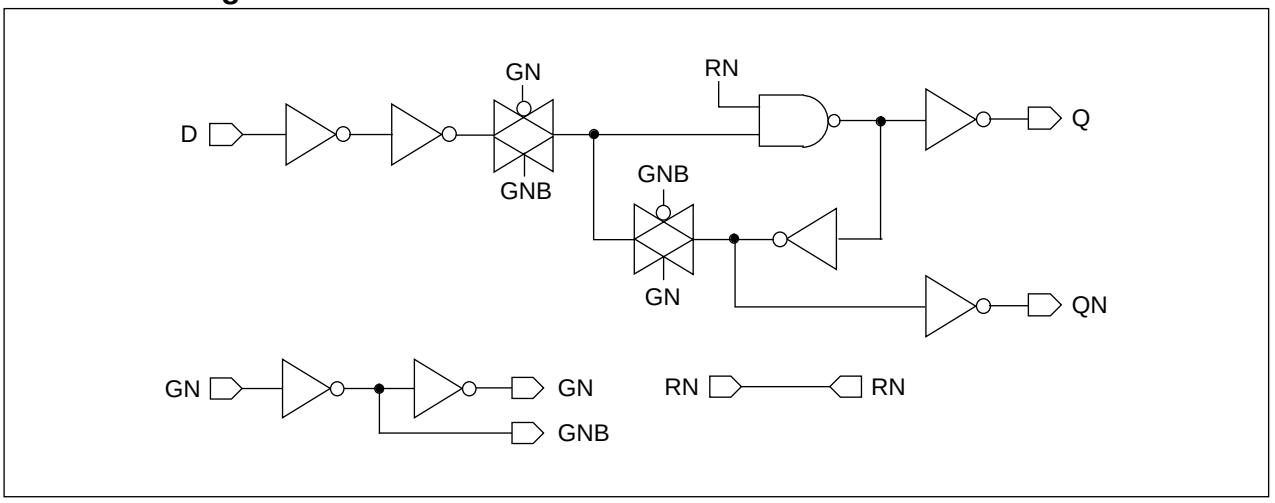
Truth Table

D	GN	RN	Q (n+1)	QN (n+1)
0	0	1	0	1
1	0	1	1	0
x	1	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
STD80							
LD6			*LD6D2*			*LD6*	*LD6D2*
D	GN	RN	D	GN	RN		
0.5	0.5	0.4	0.5	0.5	0.4	4.7	5.3
STDM80							
LD6			*LD6D2*			*LD6*	*LD6D2*
D	GN	RN	D	GN	RN		
0.6	0.6	0.8	0.6	0.6	0.8	4.7	5.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD6	LD6D2	LD6	LD6D2
Pulse Width Low (GN)	t_{PWL}	0.87	0.87	0.87	0.93
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.82	0.82
Input Setup Time (D to GN)	t_{SU}	0.74	0.76	0.74	0.79
Input Hold Time (D to GN)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.38	0.33	0.33
Input Hold Time (RN to GN)	t_{HD}	0.33	0.33	0.38	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.57	0.51 + 0.032*SL	0.52 + 0.026*SL	0.54 + 0.024*SL
	t_{PHL}	0.64	0.56 + 0.041*SL	0.57 + 0.038*SL	0.58 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
GN to Q	t_{PLH}	0.70	0.64 + 0.031*SL	0.65 + 0.026*SL	0.67 + 0.024*SL
	t_{PHL}	0.66	0.57 + 0.041*SL	0.58 + 0.038*SL	0.59 + 0.037*SL
	t_R	0.23	0.13 + 0.049*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
RN to Q	t_{PLH}	0.33	0.27 + 0.031*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.061*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
D to QN	t_{PLH}	0.68	0.63 + 0.025*SL	0.64 + 0.024*SL	0.64 + 0.024*SL
	t_{PHL}	0.75	0.67 + 0.037*SL	0.67 + 0.037*SL	0.67 + 0.037*SL
	t_R	0.19	0.09 + 0.046*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
GN to QN	t_{PLH}	0.70	0.65 + 0.026*SL	0.65 + 0.024*SL	0.65 + 0.024*SL
	t_{PHL}	0.88	0.80 + 0.036*SL	0.80 + 0.037*SL	0.80 + 0.037*SL
	t_R	0.19	0.09 + 0.046*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
RN to QN	t_{PLH}	0.47	0.41 + 0.030*SL	0.42 + 0.025*SL	0.43 + 0.024*SL
	t_{PHL}	0.51	0.43 + 0.037*SL	0.43 + 0.037*SL	0.43 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.58	0.54 + 0.021*SL	0.55 + 0.015*SL	0.59 + 0.012*SL
	t_{PHL}	0.63	0.59 + 0.023*SL	0.60 + 0.020*SL	0.61 + 0.018*SL
	t_R	0.20	0.15 + 0.025*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.18	0.11 + 0.031*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
GN to Q	t_{PLH}	0.71	0.67 + 0.021*SL	0.68 + 0.015*SL	0.72 + 0.012*SL
	t_{PHL}	0.65	0.60 + 0.023*SL	0.61 + 0.020*SL	0.62 + 0.018*SL
	t_R	0.20	0.15 + 0.024*SL	0.15 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
RN to Q	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.015*SL	0.35 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
D to QN	t_{PLH}	0.75	0.72 + 0.013*SL	0.73 + 0.012*SL	0.73 + 0.012*SL
	t_{PHL}	0.83	0.79 + 0.018*SL	0.80 + 0.017*SL	0.79 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
GN to QN	t_{PLH}	0.76	0.73 + 0.014*SL	0.74 + 0.012*SL	0.74 + 0.012*SL
	t_{PHL}	0.96	0.92 + 0.017*SL	0.92 + 0.017*SL	0.91 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.033*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
RN to QN	t_{PLH}	0.53	0.50 + 0.018*SL	0.51 + 0.014*SL	0.53 + 0.012*SL
	t_{PHL}	0.59	0.55 + 0.018*SL	0.55 + 0.017*SL	0.54 + 0.018*SL
	t_R	0.18	0.14 + 0.023*SL	0.14 + 0.022*SL	0.11 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.030*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.85	0.77 + 0.044*SL	0.79 + 0.038*SL	0.81 + 0.035*SL
	t_{PHL}	0.87	0.77 + 0.052*SL	0.79 + 0.046*SL	0.80 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
GN to Q	t_{PLH}	1.00	0.91 + 0.044*SL	0.93 + 0.037*SL	0.95 + 0.035*SL
	t_{PHL}	0.89	0.79 + 0.052*SL	0.81 + 0.046*SL	0.82 + 0.044*SL
	t_R	0.31	0.17 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.081*SL
RN to Q	t_{PLH}	0.44	0.35 + 0.043*SL	0.37 + 0.037*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.047*SL	0.40 + 0.045*SL
	t_R	0.31	0.17 + 0.071*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
D to QN	t_{PLH}	0.95	0.87 + 0.035*SL	0.88 + 0.033*SL	0.88 + 0.033*SL
	t_{PHL}	1.09	1.00 + 0.047*SL	1.01 + 0.045*SL	1.01 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
GN to QN	t_{PLH}	0.97	0.90 + 0.035*SL	0.90 + 0.033*SL	0.90 + 0.033*SL
	t_{PHL}	1.23	1.14 + 0.047*SL	1.15 + 0.044*SL	1.15 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
RN to QN	t_{PLH}	0.62	0.54 + 0.042*SL	0.56 + 0.036*SL	0.58 + 0.034*SL
	t_{PHL}	0.67	0.58 + 0.047*SL	0.59 + 0.045*SL	0.59 + 0.044*SL
	t_R	0.30	0.16 + 0.069*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

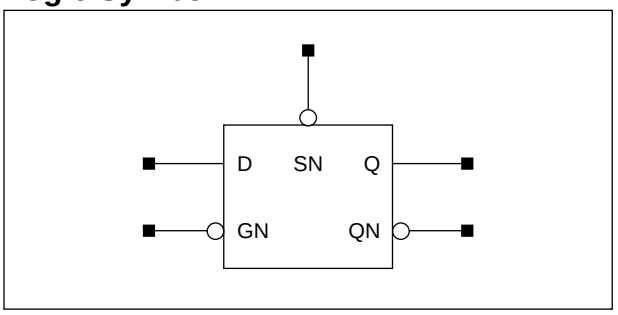
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.87	0.81 + 0.028*SL	0.83 + 0.022*SL	0.85 + 0.020*SL
	t_{PHL}	0.86	0.80 + 0.031*SL	0.81 + 0.026*SL	0.83 + 0.023*SL
	t_R	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.041*SL	0.15 + 0.038*SL	0.14 + 0.038*SL
GN to Q	t_{PLH}	1.01	0.95 + 0.028*SL	0.97 + 0.022*SL	0.99 + 0.020*SL
	t_{PHL}	0.88	0.82 + 0.031*SL	0.83 + 0.026*SL	0.85 + 0.023*SL
	t_R	0.25	0.18 + 0.036*SL	0.18 + 0.034*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
RN to Q	t_{PLH}	0.44	0.39 + 0.027*SL	0.40 + 0.022*SL	0.43 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.21	0.13 + 0.042*SL	0.14 + 0.038*SL	0.14 + 0.038*SL
D to QN	t_{PLH}	1.03	1.00 + 0.019*SL	1.00 + 0.017*SL	1.01 + 0.017*SL
	t_{PHL}	1.20	1.15 + 0.024*SL	1.16 + 0.022*SL	1.16 + 0.021*SL
	t_R	0.19	0.13 + 0.032*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.22	0.13 + 0.040*SL	0.14 + 0.037*SL	0.14 + 0.038*SL
GN to QN	t_{PLH}	1.06	1.02 + 0.019*SL	1.02 + 0.017*SL	1.03 + 0.017*SL
	t_{PHL}	1.34	1.30 + 0.024*SL	1.30 + 0.022*SL	1.31 + 0.021*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.037*SL	0.14 + 0.038*SL
RN to QN	t_{PLH}	0.71	0.66 + 0.023*SL	0.67 + 0.020*SL	0.68 + 0.018*SL
	t_{PHL}	0.78	0.73 + 0.025*SL	0.73 + 0.022*SL	0.74 + 0.021*SL
	t_R	0.23	0.16 + 0.036*SL	0.17 + 0.033*SL	0.16 + 0.034*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.037*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



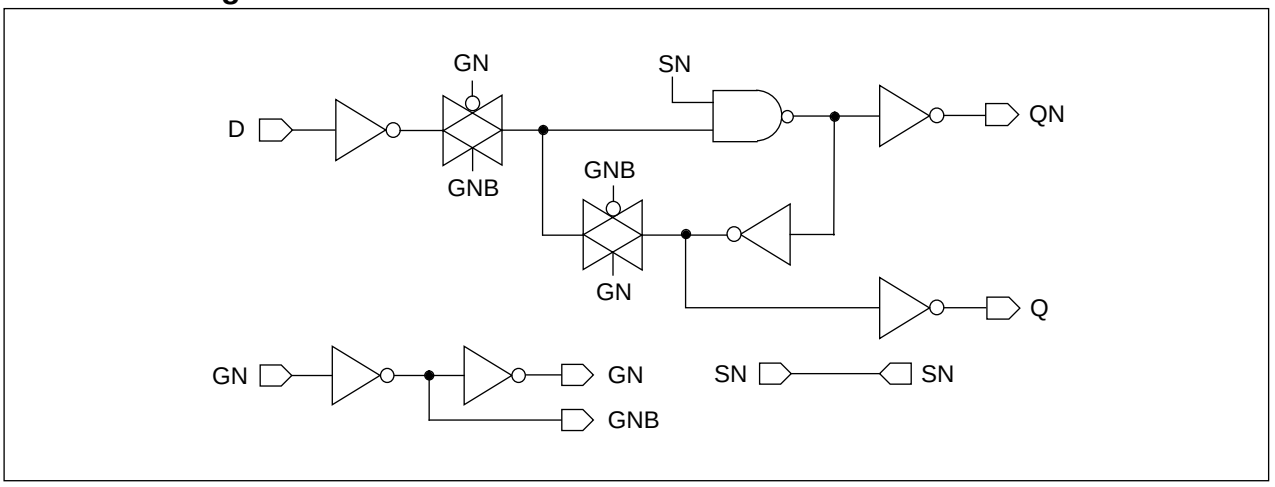
Truth Table

D	GN	SN	Q (n+1)	QN (n+1)
0	0	1	0	1
1	0	1	1	0
x	1	1	Q (n)	QN (n)
x	x	0	1	0

Cell Data

Input Load (SL)						Gate Count	
STD80							
LD7			*LD7D2*			*LD7*	*LD7D2*
D	GN	SN	D	GN	SN		
0.6	0.6	0.5	0.6	0.6	0.5	4.3	5.0
STDM80							
LD7			*LD7D2*			*LD7*	*LD7D2*
D	GN	SN	D	GN	SN		
0.6	0.6	0.8	0.6	0.6	0.8	4.3	5.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD7	LD7D2	LD7	LD7D2
Pulse Width Low (GN)	t_{PWL}	0.87	0.87	0.87	0.93
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.82	0.87
Input Setup Time (D to GN)	t_{SU}	0.60	0.66	0.66	0.74
Input Hold Time (D to GN)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.38	0.33	0.33
Input Hold Time (SN to GN)	t_{HD}	0.33	0.33	0.38	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.53	0.48 + 0.025*SL	0.48 + 0.024*SL	0.48 + 0.024*SL
	t_{PHL}	0.76	0.68 + 0.037*SL	0.68 + 0.037*SL	0.68 + 0.037*SL
	t_R	0.19	0.10 + 0.045*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
GN to Q	t_{PLH}	0.69	0.64 + 0.025*SL	0.65 + 0.024*SL	0.65 + 0.024*SL
	t_{PHL}	0.87	0.80 + 0.037*SL	0.80 + 0.037*SL	0.80 + 0.037*SL
	t_R	0.18	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
SN to Q	t_{PLH}	0.47	0.41 + 0.030*SL	0.42 + 0.025*SL	0.43 + 0.024*SL
	t_{PHL}	0.51	0.43 + 0.037*SL	0.43 + 0.037*SL	0.43 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
D to QN	t_{PLH}	0.58	0.52 + 0.031*SL	0.53 + 0.026*SL	0.55 + 0.024*SL
	t_{PHL}	0.49	0.41 + 0.041*SL	0.41 + 0.038*SL	0.42 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
GN to QN	t_{PLH}	0.70	0.63 + 0.032*SL	0.65 + 0.026*SL	0.67 + 0.024*SL
	t_{PHL}	0.65	0.57 + 0.041*SL	0.58 + 0.038*SL	0.59 + 0.037*SL
	t_R	0.23	0.13 + 0.047*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
SN to QN	t_{PLH}	0.33	0.27 + 0.031*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.040*SL	0.29 + 0.038*SL	0.29 + 0.037*SL
	t_R	0.23	0.13 + 0.048*SL	0.13 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.061*SL	0.10 + 0.066*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD7D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.59	0.56 + 0.014*SL	0.57 + 0.012*SL	0.57 + 0.012*SL
	t_{PHL}	0.84	0.80 + 0.018*SL	0.80 + 0.017*SL	0.79 + 0.018*SL
	t_R	0.15	0.11 + 0.022*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
GN to Q	t_{PLH}	0.76	0.73 + 0.014*SL	0.74 + 0.012*SL	0.74 + 0.012*SL
	t_{PHL}	0.95	0.92 + 0.017*SL	0.92 + 0.017*SL	0.91 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.11 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
SN to Q	t_{PLH}	0.53	0.50 + 0.018*SL	0.51 + 0.014*SL	0.53 + 0.012*SL
	t_{PHL}	0.59	0.55 + 0.018*SL	0.55 + 0.017*SL	0.54 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.030*SL	0.08 + 0.034*SL
D to QN	t_{PLH}	0.59	0.55 + 0.021*SL	0.56 + 0.015*SL	0.59 + 0.012*SL
	t_{PHL}	0.48	0.43 + 0.023*SL	0.44 + 0.020*SL	0.46 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
GN to QN	t_{PLH}	0.71	0.67 + 0.021*SL	0.68 + 0.015*SL	0.71 + 0.012*SL
	t_{PHL}	0.64	0.60 + 0.023*SL	0.60 + 0.020*SL	0.62 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.18	0.12 + 0.030*SL	0.11 + 0.031*SL	0.09 + 0.034*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.015*SL	0.35 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.75	0.68 + 0.035*SL	0.68 + 0.033*SL	0.69 + 0.033*SL
	t_{PHL}	1.05	0.95 + 0.047*SL	0.96 + 0.045*SL	0.96 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
GN to Q	t_{PLH}	0.96	0.89 + 0.035*SL	0.90 + 0.033*SL	0.90 + 0.033*SL
	t_{PHL}	1.23	1.14 + 0.046*SL	1.14 + 0.045*SL	1.14 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.29	0.14 + 0.076*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
SN to Q	t_{PLH}	0.62	0.54 + 0.042*SL	0.56 + 0.036*SL	0.58 + 0.034*SL
	t_{PHL}	0.67	0.58 + 0.047*SL	0.59 + 0.045*SL	0.59 + 0.044*SL
	t_R	0.30	0.16 + 0.069*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.29	0.13 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
D to QN	t_{PLH}	0.81	0.72 + 0.044*SL	0.74 + 0.038*SL	0.76 + 0.035*SL
	t_{PHL}	0.68	0.57 + 0.052*SL	0.59 + 0.046*SL	0.60 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
GN to QN	t_{PLH}	0.99	0.90 + 0.044*SL	0.92 + 0.037*SL	0.94 + 0.035*SL
	t_{PHL}	0.89	0.79 + 0.052*SL	0.80 + 0.046*SL	0.82 + 0.044*SL
	t_R	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.17 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.081*SL
SN to QN	t_{PLH}	0.44	0.35 + 0.043*SL	0.37 + 0.037*SL	0.39 + 0.034*SL
	t_{PHL}	0.47	0.37 + 0.051*SL	0.38 + 0.047*SL	0.40 + 0.045*SL
	t_R	0.31	0.17 + 0.071*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD7D2

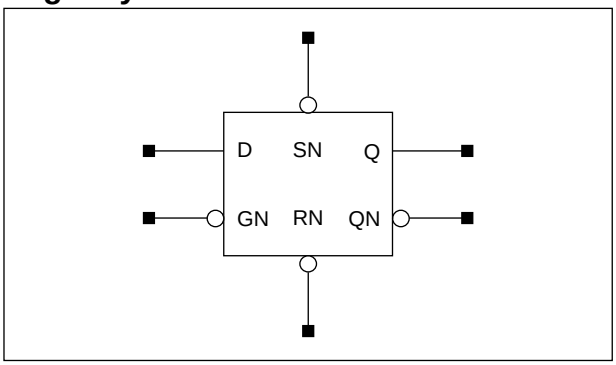
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.84	0.80 + 0.019*SL	0.81 + 0.017*SL	0.81 + 0.017*SL
	t_{PHL}	1.16	1.11 + 0.024*SL	1.11 + 0.022*SL	1.12 + 0.021*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.22	0.14 + 0.039*SL	0.14 + 0.037*SL	0.14 + 0.038*SL
GN to Q	t_{PLH}	1.05	1.01 + 0.019*SL	1.02 + 0.017*SL	1.02 + 0.017*SL
	t_{PHL}	1.34	1.29 + 0.024*SL	1.30 + 0.022*SL	1.30 + 0.021*SL
	t_R	0.19	0.13 + 0.031*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.22	0.13 + 0.041*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
SN to Q	t_{PLH}	0.71	0.66 + 0.023*SL	0.67 + 0.020*SL	0.69 + 0.018*SL
	t_{PHL}	0.78	0.73 + 0.025*SL	0.73 + 0.022*SL	0.74 + 0.021*SL
	t_R	0.23	0.16 + 0.036*SL	0.17 + 0.033*SL	0.17 + 0.033*SL
	t_F	0.21	0.13 + 0.040*SL	0.14 + 0.037*SL	0.14 + 0.038*SL
D to QN	t_{PLH}	0.82	0.77 + 0.028*SL	0.78 + 0.022*SL	0.80 + 0.020*SL
	t_{PHL}	0.66	0.60 + 0.031*SL	0.62 + 0.026*SL	0.64 + 0.023*SL
	t_R	0.25	0.17 + 0.037*SL	0.18 + 0.034*SL	0.18 + 0.035*SL
	t_F	0.22	0.14 + 0.039*SL	0.14 + 0.039*SL	0.15 + 0.038*SL
GN to QN	t_{PLH}	1.00	0.95 + 0.028*SL	0.96 + 0.023*SL	0.99 + 0.019*SL
	t_{PHL}	0.88	0.82 + 0.031*SL	0.83 + 0.026*SL	0.85 + 0.023*SL
	t_R	0.25	0.17 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.038*SL	0.15 + 0.038*SL
SN to QN	t_{PLH}	0.44	0.39 + 0.027*SL	0.40 + 0.022*SL	0.43 + 0.019*SL
	t_{PHL}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.21	0.13 + 0.042*SL	0.14 + 0.038*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

LD8/LD8D2

D Latch with Active Low, Reset, Set, 1X/2X Drive

Logic Symbol



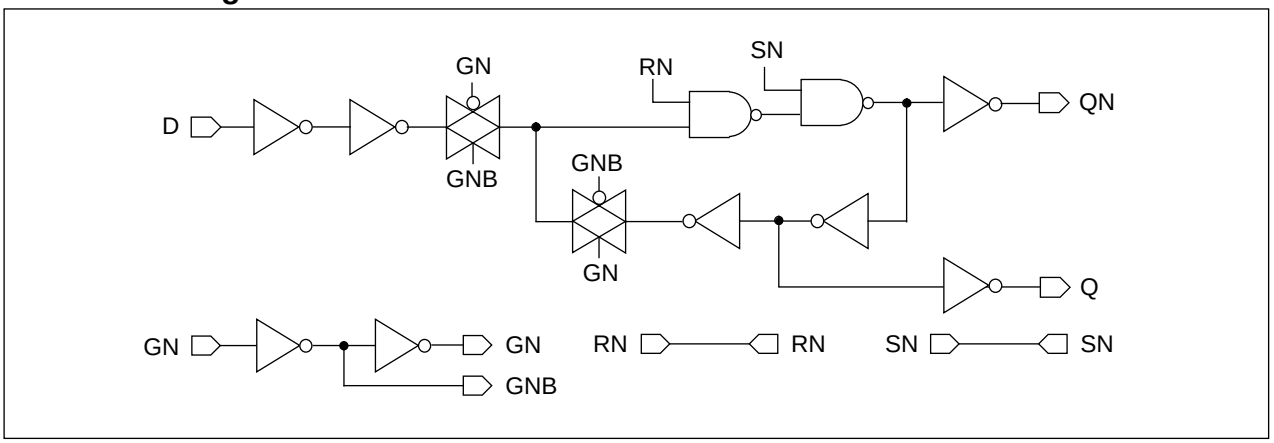
Truth Table

D	GN	RN	SN	Q (n+1)	QN (n+1)
0	0	1	1	0	1
1	0	1	1	1	0
x	1	1	1	Q (n)	QN (n)
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0

Cell Data

Input Load (SL)								Gate Count	
STD80									
LD8				*LD8D2*				*LD8*	*LD8D2*
D	GN	RN	SN	D	GN	RN	SN		
0.6	0.6	0.4	0.7	0.6	0.6	0.4	0.7	6.0	6.7
STDM80									
LD8				*LD8D2*				*LD8*	*LD8D2*
D	GN	RN	SN	D	GN	RN	SN		
0.6	0.6	0.4	0.8	0.6	0.6	0.4	0.8	6.0	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80		STDM80	
		LD8	LD8D2	LD8	LD8D2
Pulse Width Low (GN)	t_{PWL}	0.87	0.87	0.93	1.04
Pulse Width Low (RN)	t_{PWL}	0.87	0.87	0.90	1.01
Pulse Width Low (SN)	t_{PWL}	0.87	0.87	0.80	0.87
Input Setup Time (D to GN)	t_{SU}	0.00	0.00	0.90	1.01
Input Hold Time (D to GN)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.38	0.33	0.38
Input Hold Time (RN to GN)	t_{HD}	0.33	0.33	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.38	0.33	0.38
Input Hold Time (SN to GN)	t_{HD}	0.33	0.33	0.38	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.74	0.69 + 0.028*SL	0.69 + 0.024*SL	0.70 + 0.024*SL
	t_{PHL}	0.96	0.89 + 0.038*SL	0.89 + 0.037*SL	0.89 + 0.037*SL
	t_R	0.20	0.10 + 0.045*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
GN to Q	t_{PLH}	0.87	0.82 + 0.027*SL	0.82 + 0.024*SL	0.83 + 0.024*SL
	t_{PHL}	0.96	0.89 + 0.039*SL	0.89 + 0.037*SL	0.89 + 0.037*SL
	t_R	0.19	0.10 + 0.048*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.061*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
SN to Q	t_{PLH}	0.45	0.39 + 0.028*SL	0.40 + 0.024*SL	0.40 + 0.024*SL
	t_{PHL}	0.52	0.44 + 0.038*SL	0.44 + 0.037*SL	0.44 + 0.037*SL
	t_R	0.19	0.11 + 0.044*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
RN to Q	t_{PLH}	0.50	0.45 + 0.028*SL	0.46 + 0.024*SL	0.46 + 0.024*SL
	t_{PHL}	0.69	0.61 + 0.039*SL	0.61 + 0.037*SL	0.61 + 0.037*SL
	t_R	0.19	0.11 + 0.044*SL	0.09 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.066*SL	0.07 + 0.069*SL
D to QN	t_{PLH}	0.75	0.69 + 0.030*SL	0.70 + 0.026*SL	0.72 + 0.024*SL
	t_{PHL}	0.67	0.59 + 0.040*SL	0.60 + 0.038*SL	0.60 + 0.037*SL
	t_R	0.22	0.13 + 0.047*SL	0.12 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.23	0.10 + 0.066*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
GN to QN	t_{PLH}	0.75	0.69 + 0.031*SL	0.70 + 0.026*SL	0.72 + 0.024*SL
	t_{PHL}	0.80	0.72 + 0.040*SL	0.73 + 0.038*SL	0.73 + 0.037*SL
	t_R	0.22	0.13 + 0.048*SL	0.12 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
SN to QN	t_{PLH}	0.31	0.24 + 0.031*SL	0.26 + 0.026*SL	0.28 + 0.024*SL
	t_{PHL}	0.38	0.30 + 0.040*SL	0.30 + 0.038*SL	0.31 + 0.037*SL
	t_R	0.23	0.13 + 0.046*SL	0.13 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.067*SL	0.08 + 0.069*SL
RN to QN	t_{PLH}	0.48	0.42 + 0.031*SL	0.43 + 0.026*SL	0.45 + 0.024*SL
	t_{PHL}	0.43	0.35 + 0.040*SL	0.36 + 0.038*SL	0.37 + 0.037*SL
	t_R	0.22	0.13 + 0.047*SL	0.12 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.23	0.10 + 0.064*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LD8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.81	0.78 + 0.015*SL	0.78 + 0.013*SL	0.79 + 0.012*SL
	t_{PHL}	1.04	1.00 + 0.019*SL	1.01 + 0.017*SL	1.00 + 0.018*SL
	t_R	0.16	0.12 + 0.022*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.030*SL	0.09 + 0.034*SL
GN to Q	t_{PLH}	0.94	0.91 + 0.015*SL	0.91 + 0.013*SL	0.92 + 0.012*SL
	t_{PHL}	1.04	1.01 + 0.019*SL	1.01 + 0.017*SL	1.00 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.030*SL	0.09 + 0.034*SL
SN to Q	t_{PLH}	0.51	0.48 + 0.015*SL	0.49 + 0.013*SL	0.50 + 0.012*SL
	t_{PHL}	0.60	0.56 + 0.019*SL	0.56 + 0.017*SL	0.56 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.030*SL	0.09 + 0.034*SL
RN to Q	t_{PLH}	0.57	0.54 + 0.015*SL	0.54 + 0.013*SL	0.55 + 0.012*SL
	t_{PHL}	0.77	0.73 + 0.019*SL	0.73 + 0.017*SL	0.73 + 0.018*SL
	t_R	0.16	0.12 + 0.022*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.18	0.12 + 0.029*SL	0.12 + 0.030*SL	0.09 + 0.034*SL
D to QN	t_{PLH}	0.77	0.72 + 0.021*SL	0.74 + 0.015*SL	0.77 + 0.012*SL
	t_{PHL}	0.67	0.62 + 0.023*SL	0.63 + 0.020*SL	0.64 + 0.018*SL
	t_R	0.19	0.14 + 0.024*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL
GN to QN	t_{PLH}	0.77	0.73 + 0.020*SL	0.74 + 0.015*SL	0.77 + 0.012*SL
	t_{PHL}	0.79	0.75 + 0.023*SL	0.76 + 0.020*SL	0.77 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.030*SL	0.10 + 0.031*SL	0.08 + 0.034*SL
SN to QN	t_{PLH}	0.32	0.28 + 0.020*SL	0.29 + 0.015*SL	0.32 + 0.012*SL
	t_{PHL}	0.37	0.33 + 0.023*SL	0.33 + 0.020*SL	0.35 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.09 + 0.034*SL
RN to QN	t_{PLH}	0.49	0.45 + 0.021*SL	0.46 + 0.015*SL	0.49 + 0.012*SL
	t_{PHL}	0.43	0.38 + 0.023*SL	0.39 + 0.020*SL	0.40 + 0.018*SL
	t_R	0.19	0.15 + 0.022*SL	0.14 + 0.024*SL	0.12 + 0.026*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	1.10	1.03 + 0.037*SL	1.04 + 0.034*SL	1.04 + 0.033*SL
	t_{PHL}	1.33	1.24 + 0.049*SL	1.25 + 0.045*SL	1.25 + 0.044*SL
	t_R	0.27	0.13 + 0.067*SL	0.13 + 0.070*SL	0.11 + 0.071*SL
	t_F	0.30	0.15 + 0.078*SL	0.14 + 0.079*SL	0.13 + 0.081*SL
GN to Q	t_{PLH}	1.24	1.17 + 0.037*SL	1.18 + 0.034*SL	1.18 + 0.033*SL
	t_{PHL}	1.35	1.25 + 0.049*SL	1.26 + 0.045*SL	1.27 + 0.044*SL
	t_R	0.27	0.13 + 0.067*SL	0.13 + 0.070*SL	0.11 + 0.071*SL
	t_F	0.30	0.15 + 0.078*SL	0.14 + 0.079*SL	0.13 + 0.081*SL
SN to Q	t_{PLH}	0.60	0.52 + 0.037*SL	0.54 + 0.034*SL	0.54 + 0.034*SL
	t_{PHL}	0.71	0.61 + 0.049*SL	0.62 + 0.045*SL	0.63 + 0.044*SL
	t_R	0.27	0.13 + 0.067*SL	0.12 + 0.070*SL	0.11 + 0.071*SL
	t_F	0.30	0.15 + 0.078*SL	0.14 + 0.079*SL	0.13 + 0.081*SL
RN to Q	t_{PLH}	0.71	0.64 + 0.037*SL	0.65 + 0.034*SL	0.65 + 0.033*SL
	t_{PHL}	0.93	0.83 + 0.050*SL	0.84 + 0.046*SL	0.85 + 0.044*SL
	t_R	0.27	0.13 + 0.067*SL	0.13 + 0.070*SL	0.11 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.079*SL	0.13 + 0.081*SL
D to QN	t_{PLH}	1.05	0.96 + 0.043*SL	0.98 + 0.037*SL	0.99 + 0.035*SL
	t_{PHL}	0.99	0.89 + 0.051*SL	0.90 + 0.046*SL	0.92 + 0.044*SL
	t_R	0.30	0.16 + 0.070*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
GN to QN	t_{PLH}	1.06	0.98 + 0.042*SL	1.00 + 0.037*SL	1.01 + 0.034*SL
	t_{PHL}	1.13	1.03 + 0.051*SL	1.04 + 0.046*SL	1.06 + 0.044*SL
	t_R	0.31	0.17 + 0.069*SL	0.17 + 0.070*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL
SN to QN	t_{PLH}	0.43	0.34 + 0.042*SL	0.36 + 0.037*SL	0.37 + 0.034*SL
	t_{PHL}	0.49	0.39 + 0.051*SL	0.40 + 0.046*SL	0.41 + 0.045*SL
	t_R	0.30	0.16 + 0.070*SL	0.16 + 0.070*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.082*SL	0.13 + 0.082*SL
RN to QN	t_{PLH}	0.65	0.56 + 0.042*SL	0.58 + 0.037*SL	0.59 + 0.035*SL
	t_{PHL}	0.60	0.50 + 0.051*SL	0.51 + 0.046*SL	0.52 + 0.045*SL
	t_R	0.30	0.16 + 0.070*SL	0.17 + 0.070*SL	0.16 + 0.070*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.13 + 0.082*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

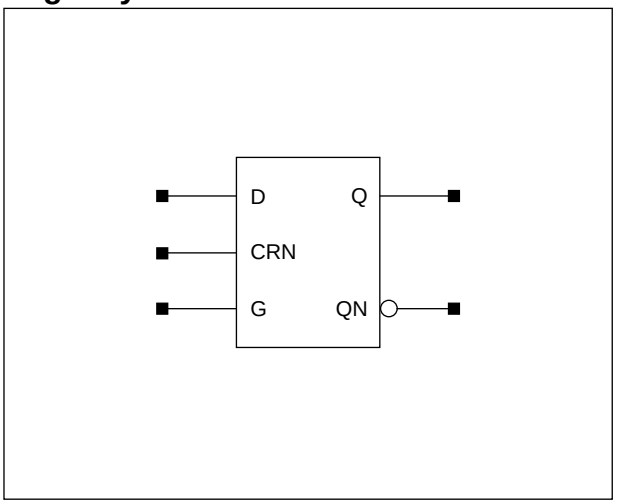
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LD8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	1.19	1.15 + 0.020*SL	1.16 + 0.018*SL	1.16 + 0.017*SL
	t_{PHL}	1.44	1.39 + 0.027*SL	1.40 + 0.023*SL	1.41 + 0.022*SL
	t_R	0.20	0.14 + 0.033*SL	0.14 + 0.032*SL	0.13 + 0.034*SL
	t_F	0.23	0.15 + 0.041*SL	0.16 + 0.037*SL	0.16 + 0.037*SL
GN to Q	t_{PLH}	1.33	1.29 + 0.020*SL	1.30 + 0.018*SL	1.30 + 0.017*SL
	t_{PHL}	1.46	1.40 + 0.027*SL	1.41 + 0.023*SL	1.42 + 0.022*SL
	t_R	0.20	0.14 + 0.033*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.23	0.15 + 0.042*SL	0.16 + 0.037*SL	0.16 + 0.037*SL
SN to Q	t_{PLH}	0.69	0.65 + 0.020*SL	0.65 + 0.018*SL	0.66 + 0.017*SL
	t_{PHL}	0.82	0.76 + 0.027*SL	0.77 + 0.023*SL	0.78 + 0.022*SL
	t_R	0.20	0.14 + 0.033*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_F	0.23	0.15 + 0.041*SL	0.16 + 0.038*SL	0.16 + 0.037*SL
RN to Q	t_{PLH}	0.80	0.76 + 0.020*SL	0.77 + 0.018*SL	0.77 + 0.017*SL
	t_{PHL}	1.04	0.98 + 0.027*SL	0.99 + 0.023*SL	1.00 + 0.022*SL
	t_R	0.20	0.14 + 0.033*SL	0.14 + 0.032*SL	0.13 + 0.034*SL
	t_F	0.23	0.15 + 0.041*SL	0.15 + 0.039*SL	0.16 + 0.037*SL
D to QN	t_{PLH}	1.06	1.01 + 0.027*SL	1.02 + 0.022*SL	1.04 + 0.019*SL
	t_{PHL}	0.98	0.92 + 0.031*SL	0.94 + 0.026*SL	0.95 + 0.023*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_F	0.22	0.14 + 0.040*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
GN to QN	t_{PLH}	1.08	1.02 + 0.027*SL	1.04 + 0.022*SL	1.06 + 0.019*SL
	t_{PHL}	1.12	1.06 + 0.030*SL	1.08 + 0.026*SL	1.10 + 0.023*SL
	t_R	0.24	0.17 + 0.037*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_F	0.22	0.14 + 0.039*SL	0.14 + 0.039*SL	0.14 + 0.038*SL
SN to QN	t_{PLH}	0.44	0.38 + 0.027*SL	0.40 + 0.022*SL	0.42 + 0.019*SL
	t_{PHL}	0.48	0.42 + 0.031*SL	0.43 + 0.026*SL	0.45 + 0.023*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_F	0.22	0.14 + 0.041*SL	0.15 + 0.038*SL	0.14 + 0.038*SL
RN to QN	t_{PLH}	0.66	0.61 + 0.027*SL	0.62 + 0.022*SL	0.64 + 0.019*SL
	t_{PHL}	0.59	0.53 + 0.031*SL	0.55 + 0.026*SL	0.56 + 0.023*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_F	0.22	0.13 + 0.041*SL	0.14 + 0.039*SL	0.14 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



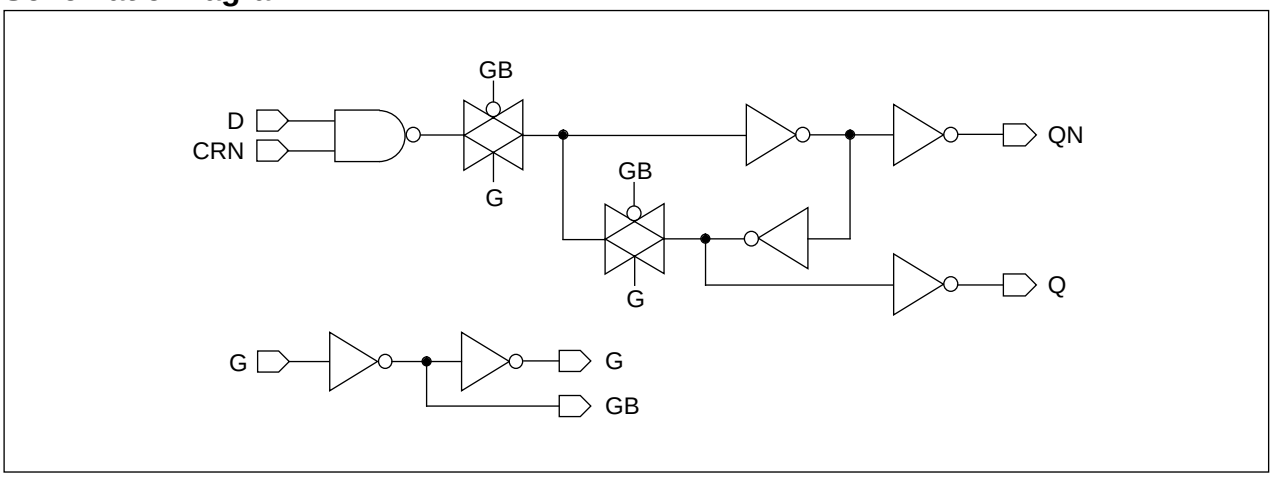
Truth Table

D	CRN	G	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	x	0	Q (n)	QN (n)
x	0	1	0	1

Cell Data

Input Load (SL)			Gate Count
STD80			
D	CRN	G	
0.5	0.5	0.5	4.3
STDM80			
D	CRN	G	
0.6	0.6	0.6	4.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width High (G)	t_{PWH}	0.79	0.82
Input Setup Time (D to G)	t_{SU}	0.55	0.55
Input Hold Time (D to G)	t_{HD}	0.33	0.33
Input Setup Time (CRN to G)	t_{SU}	0.55	0.55
Input Hold Time (CRN to G)	t_{HD}	0.33	0.33

LDS2

D Latch with Active High, Synchronous Clear

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LDS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.58	0.53 + 0.025*SL	0.53 + 0.024*SL	0.53 + 0.024*SL
	t_{PHL}	0.74	0.66 + 0.038*SL	0.66 + 0.037*SL	0.66 + 0.037*SL
	t_R	0.19	0.10 + 0.044*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
CRN to Q	t_{PLH}	0.60	0.55 + 0.025*SL	0.55 + 0.024*SL	0.55 + 0.024*SL
	t_{PHL}	0.71	0.64 + 0.038*SL	0.64 + 0.037*SL	0.64 + 0.037*SL
	t_R	0.18	0.09 + 0.047*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
G to Q	t_{PLH}	0.66	0.61 + 0.026*SL	0.61 + 0.023*SL	0.61 + 0.024*SL
	t_{PHL}	0.66	0.58 + 0.038*SL	0.59 + 0.037*SL	0.59 + 0.037*SL
	t_R	0.19	0.09 + 0.047*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
D to QN	t_{PLH}	0.57	0.51 + 0.028*SL	0.52 + 0.024*SL	0.53 + 0.024*SL
	t_{PHL}	0.54	0.46 + 0.042*SL	0.47 + 0.038*SL	0.47 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
CRN to QN	t_{PLH}	0.54	0.49 + 0.028*SL	0.49 + 0.024*SL	0.50 + 0.024*SL
	t_{PHL}	0.56	0.48 + 0.041*SL	0.49 + 0.038*SL	0.49 + 0.037*SL
	t_R	0.21	0.11 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
G to QN	t_{PLH}	0.49	0.44 + 0.027*SL	0.44 + 0.024*SL	0.45 + 0.024*SL
	t_{PHL}	0.62	0.54 + 0.041*SL	0.55 + 0.038*SL	0.55 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LDS2

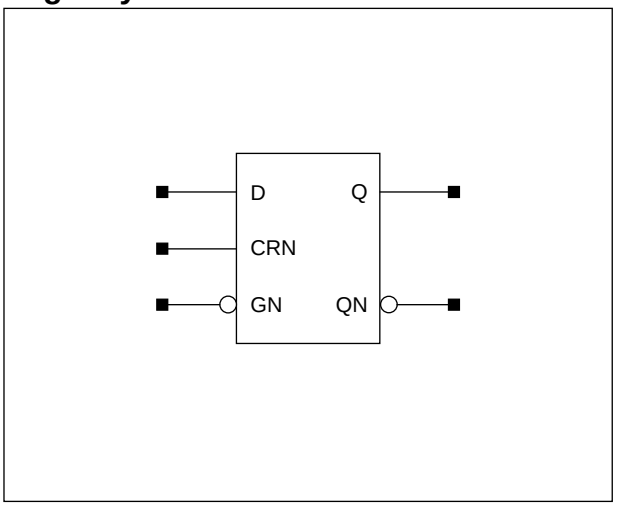
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.84	0.77 + 0.035*SL	0.77 + 0.033*SL	0.77 + 0.033*SL
	t_{PHL}	1.03	0.94 + 0.047*SL	0.94 + 0.044*SL	0.94 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.080*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
CRN to Q	t_{PLH}	0.85	0.78 + 0.035*SL	0.78 + 0.033*SL	0.78 + 0.033*SL
	t_{PHL}	0.99	0.90 + 0.047*SL	0.91 + 0.044*SL	0.91 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
G to Q	t_{PLH}	0.95	0.88 + 0.035*SL	0.89 + 0.033*SL	0.89 + 0.033*SL
	t_{PHL}	0.94	0.85 + 0.047*SL	0.86 + 0.044*SL	0.86 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D to QN	t_{PLH}	0.80	0.72 + 0.039*SL	0.74 + 0.035*SL	0.74 + 0.034*SL
	t_{PHL}	0.77	0.66 + 0.052*SL	0.68 + 0.046*SL	0.69 + 0.044*SL
	t_R	0.29	0.15 + 0.066*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
CRN to QN	t_{PLH}	0.77	0.69 + 0.038*SL	0.70 + 0.035*SL	0.71 + 0.034*SL
	t_{PHL}	0.78	0.67 + 0.052*SL	0.69 + 0.046*SL	0.70 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
G to QN	t_{PLH}	0.72	0.64 + 0.037*SL	0.65 + 0.035*SL	0.66 + 0.034*SL
	t_{PHL}	0.89	0.78 + 0.052*SL	0.80 + 0.046*SL	0.81 + 0.044*SL
	t_R	0.28	0.14 + 0.068*SL	0.13 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

LDS6

D Latch with Active Low, Synchronous Clear

Logic Symbol



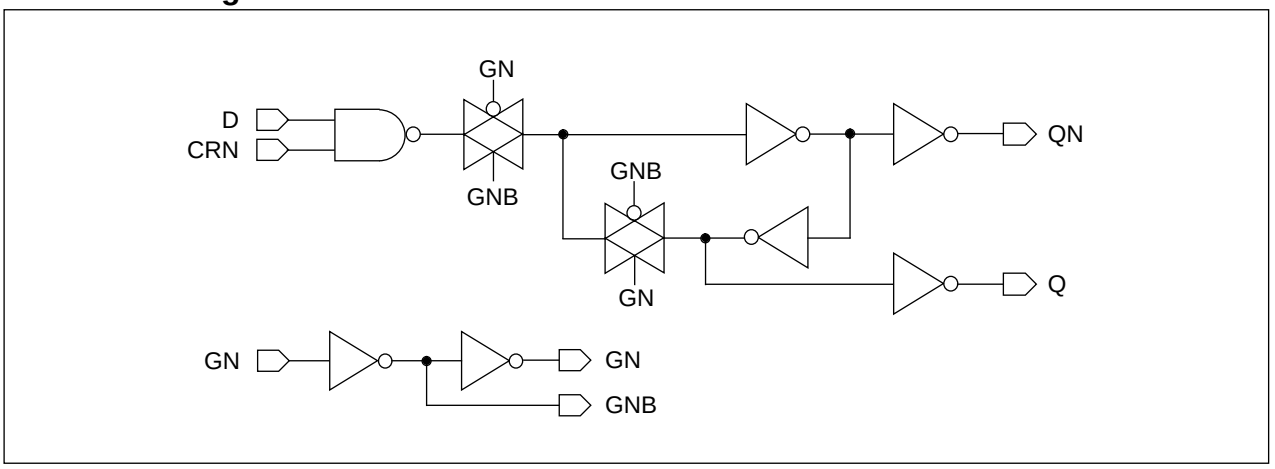
Truth Table

D	CRN	GN	Q (n+1)	QN (n+1)
0	1	0	0	1
1	1	0	1	0
x	x	1	Q (n)	QN (n)
x	0	0	0	1

Cell Data

Input Load (SL)			Gate Count
STD80			
D	CRN	GN	
0.5	0.5	0.5	4.3
STDM80			
D	CRN	GN	
0.6	0.6	0.6	4.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	STD80	STDM80
Pulse Width Low (GN)	t_{PWL}	0.87	0.85
Input Setup Time (D to GN)	t_{SU}	0.68	0.68
Input Hold Time (D to GN)	t_{HD}	0.33	0.33
Input Setup Time (CRN to GN)	t_{SU}	0.68	0.68
Input Hold Time (CRN to GN)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LDS6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.58	0.53 + 0.025*SL	0.53 + 0.024*SL	0.53 + 0.024*SL
	t_{PHL}	0.74	0.66 + 0.038*SL	0.66 + 0.037*SL	0.66 + 0.037*SL
	t_R	0.19	0.10 + 0.045*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
CRN to Q	t_{PLH}	0.60	0.55 + 0.025*SL	0.55 + 0.024*SL	0.55 + 0.024*SL
	t_{PHL}	0.71	0.64 + 0.038*SL	0.64 + 0.037*SL	0.64 + 0.037*SL
	t_R	0.18	0.09 + 0.047*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
GN to Q	t_{PLH}	0.70	0.65 + 0.025*SL	0.66 + 0.024*SL	0.66 + 0.024*SL
	t_{PHL}	0.78	0.70 + 0.038*SL	0.70 + 0.037*SL	0.70 + 0.037*SL
	t_R	0.18	0.10 + 0.044*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
D to QN	t_{PLH}	0.57	0.51 + 0.028*SL	0.52 + 0.024*SL	0.53 + 0.024*SL
	t_{PHL}	0.54	0.46 + 0.042*SL	0.47 + 0.038*SL	0.47 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.066*SL	0.08 + 0.069*SL
CRN to QN	t_{PLH}	0.54	0.49 + 0.028*SL	0.49 + 0.024*SL	0.50 + 0.024*SL
	t_{PHL}	0.56	0.48 + 0.041*SL	0.49 + 0.038*SL	0.49 + 0.037*SL
	t_R	0.21	0.11 + 0.045*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
GN to QN	t_{PLH}	0.61	0.56 + 0.028*SL	0.56 + 0.024*SL	0.57 + 0.024*SL
	t_{PHL}	0.67	0.58 + 0.042*SL	0.59 + 0.038*SL	0.60 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.067*SL	0.08 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

LDS6

D Latch with Active Low, Synchronous Clear

Switching Characteristics

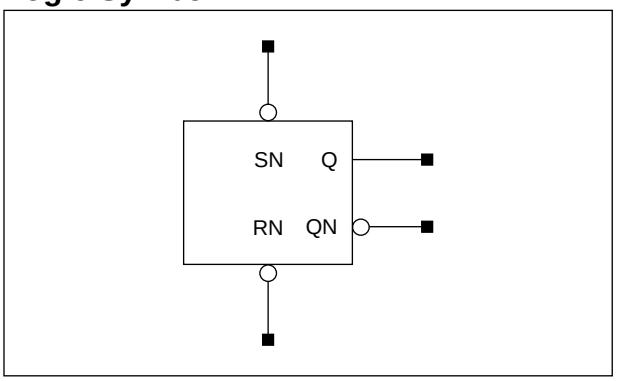
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LDS6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.84	0.77 + 0.035*SL	0.77 + 0.033*SL	0.77 + 0.033*SL
	t_{PHL}	1.03	0.94 + 0.047*SL	0.94 + 0.044*SL	0.95 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
CRN to Q	t_{PLH}	0.85	0.78 + 0.035*SL	0.78 + 0.033*SL	0.78 + 0.033*SL
	t_{PHL}	0.99	0.90 + 0.047*SL	0.91 + 0.044*SL	0.91 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.10 + 0.082*SL
GN to Q	t_{PLH}	0.98	0.91 + 0.035*SL	0.92 + 0.033*SL	0.92 + 0.033*SL
	t_{PHL}	1.08	0.99 + 0.047*SL	1.00 + 0.044*SL	1.00 + 0.044*SL
	t_R	0.26	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.082*SL
D to QN	t_{PLH}	0.80	0.73 + 0.038*SL	0.74 + 0.035*SL	0.75 + 0.034*SL
	t_{PHL}	0.77	0.66 + 0.052*SL	0.68 + 0.046*SL	0.69 + 0.044*SL
	t_R	0.29	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
CRN to QN	t_{PLH}	0.77	0.69 + 0.038*SL	0.70 + 0.035*SL	0.71 + 0.034*SL
	t_{PHL}	0.78	0.67 + 0.052*SL	0.69 + 0.046*SL	0.70 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.15 + 0.079*SL	0.15 + 0.080*SL	0.13 + 0.081*SL
GN to QN	t_{PLH}	0.86	0.78 + 0.038*SL	0.79 + 0.035*SL	0.80 + 0.034*SL
	t_{PHL}	0.91	0.81 + 0.052*SL	0.82 + 0.046*SL	0.84 + 0.044*SL
	t_R	0.28	0.14 + 0.068*SL	0.13 + 0.070*SL	0.12 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.13 + 0.081*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

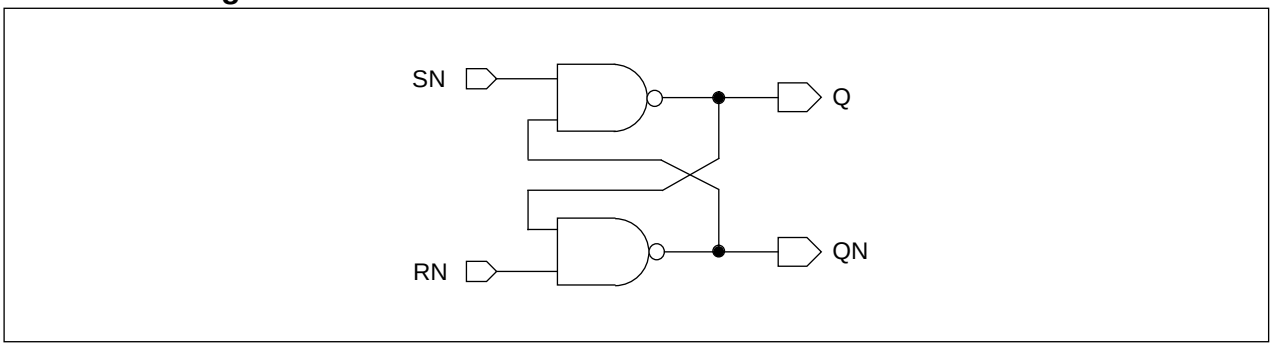
RN	SN	Q (n+1)	QN (n+1)
0	0	*	*
1	0	1	0
0	1	0	1
1	1	Q (n)	QN (n)

* Both Q and QN outputs will remain high during RN and SN are low. However, if RN and SN go high simultaneously, the output states are unpredictable.

Cell Data

Input Load (SL)				Gate Count	
STD80					
LS0		*LS0D2*		*LS0*	*LS0D2*
RN	SN	RN	SN		
0.7	0.7	1.6	1.6	1.7	3.0
STDM80					
LS0		*LS0D2*		*LS0*	*LS0D2*
RN	SN	RN	SN		
1.1	1.1	2.2	2.2	1.7	3.0

Schematic Diagram



LS0/LS0D2

SR Latch with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LS0

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.19	0.13 + 0.031*SL	0.15 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.25	0.16 + 0.041*SL	0.17 + 0.037*SL	0.16 + 0.038*SL
	t_R	0.32	0.25 + 0.039*SL	0.23 + 0.047*SL	0.16 + 0.054*SL
	t_F	0.39	0.26 + 0.066*SL	0.25 + 0.072*SL	0.19 + 0.078*SL
RN to Q	t_{PHL}	0.40	0.26 + 0.074*SL	0.27 + 0.068*SL	0.28 + 0.068*SL
	t_F	0.35	0.19 + 0.078*SL	0.18 + 0.081*SL	0.18 + 0.082*SL
SN to QN	t_{PHL}	0.40	0.26 + 0.074*SL	0.27 + 0.068*SL	0.28 + 0.068*SL
	t_F	0.35	0.19 + 0.078*SL	0.18 + 0.081*SL	0.18 + 0.082*SL
RN to QN	t_{PLH}	0.19	0.13 + 0.031*SL	0.15 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.25	0.17 + 0.040*SL	0.17 + 0.038*SL	0.16 + 0.038*SL
	t_R	0.32	0.24 + 0.041*SL	0.23 + 0.047*SL	0.16 + 0.054*SL
	t_F	0.39	0.26 + 0.066*SL	0.25 + 0.072*SL	0.19 + 0.078*SL

STD80 LS0D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.17	0.13 + 0.017*SL	0.14 + 0.014*SL	0.15 + 0.012*SL
	t_{PHL}	0.18	0.14 + 0.022*SL	0.15 + 0.019*SL	0.15 + 0.019*SL
	t_R	0.28	0.24 + 0.019*SL	0.24 + 0.022*SL	0.19 + 0.027*SL
	t_F	0.31	0.25 + 0.030*SL	0.24 + 0.034*SL	0.20 + 0.039*SL
RN to Q	t_{PHL}	0.34	0.26 + 0.039*SL	0.26 + 0.037*SL	0.27 + 0.035*SL
	t_F	0.25	0.17 + 0.040*SL	0.17 + 0.041*SL	0.16 + 0.042*SL
SN to QN	t_{PHL}	0.33	0.25 + 0.040*SL	0.26 + 0.037*SL	0.27 + 0.035*SL
	t_F	0.25	0.17 + 0.040*SL	0.17 + 0.041*SL	0.16 + 0.042*SL
RN to QN	t_{PLH}	0.17	0.13 + 0.017*SL	0.14 + 0.014*SL	0.15 + 0.012*SL
	t_{PHL}	0.18	0.14 + 0.022*SL	0.15 + 0.019*SL	0.15 + 0.019*SL
	t_R	0.28	0.24 + 0.019*SL	0.24 + 0.022*SL	0.19 + 0.027*SL
	t_F	0.31	0.24 + 0.031*SL	0.24 + 0.034*SL	0.19 + 0.039*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LS0

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.30	0.20 + 0.050*SL	0.20 + 0.050*SL	0.20 + 0.050*SL
	t_R	0.37	0.24 + 0.067*SL	0.23 + 0.071*SL	0.21 + 0.073*SL
	t_F	0.46	0.27 + 0.092*SL	0.26 + 0.095*SL	0.24 + 0.098*SL
RN to Q	t_{PHL}	0.54	0.35 + 0.096*SL	0.35 + 0.094*SL	0.35 + 0.094*SL
	t_F	0.45	0.24 + 0.104*SL	0.24 + 0.105*SL	0.23 + 0.105*SL
SN to QN	t_{PHL}	0.54	0.35 + 0.095*SL	0.35 + 0.094*SL	0.35 + 0.094*SL
	t_F	0.45	0.24 + 0.104*SL	0.24 + 0.105*SL	0.24 + 0.105*SL
RN to QN	t_{PLH}	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.30	0.20 + 0.050*SL	0.20 + 0.049*SL	0.20 + 0.050*SL
	t_R	0.37	0.24 + 0.067*SL	0.23 + 0.071*SL	0.21 + 0.073*SL
	t_F	0.46	0.27 + 0.091*SL	0.26 + 0.096*SL	0.24 + 0.098*SL

STDM80 LS0D2

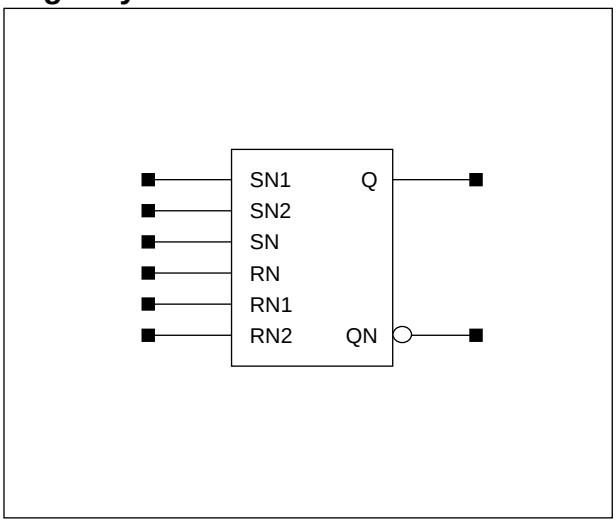
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.21	0.17 + 0.020*SL	0.18 + 0.017*SL	0.18 + 0.017*SL
	t_{PHL}	0.23	0.17 + 0.027*SL	0.18 + 0.025*SL	0.18 + 0.025*SL
	t_R	0.30	0.24 + 0.031*SL	0.23 + 0.034*SL	0.22 + 0.035*SL
	t_F	0.34	0.25 + 0.044*SL	0.25 + 0.047*SL	0.24 + 0.048*SL
RN to Q	t_{PHL}	0.44	0.34 + 0.051*SL	0.34 + 0.049*SL	0.35 + 0.049*SL
	t_F	0.32	0.22 + 0.053*SL	0.22 + 0.054*SL	0.22 + 0.053*SL
SN to QN	t_{PHL}	0.44	0.34 + 0.051*SL	0.34 + 0.049*SL	0.35 + 0.049*SL
	t_F	0.32	0.22 + 0.053*SL	0.22 + 0.053*SL	0.22 + 0.054*SL
RN to QN	t_{PLH}	0.21	0.17 + 0.020*SL	0.18 + 0.017*SL	0.18 + 0.017*SL
	t_{PHL}	0.23	0.18 + 0.026*SL	0.18 + 0.025*SL	0.18 + 0.025*SL
	t_R	0.30	0.24 + 0.032*SL	0.23 + 0.034*SL	0.22 + 0.035*SL
	t_F	0.34	0.25 + 0.044*SL	0.25 + 0.047*SL	0.24 + 0.048*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

LS1

SR Latch with Separate Inputs

Logic Symbol



Truth Table

RN	SN	RN*	SN*	Q (n+1)	QN (n+1)
0	0	x	x	*	*
x	0	0	x	*	*
x	x	0	0	*	*
0	x	x	0	*	*
1	0	1	x	1	0
0	1	x	1	0	1
1	x	1	0	1	0
x	1	0	1	0	1
1	1	1	1	Q (n)	QN (n)

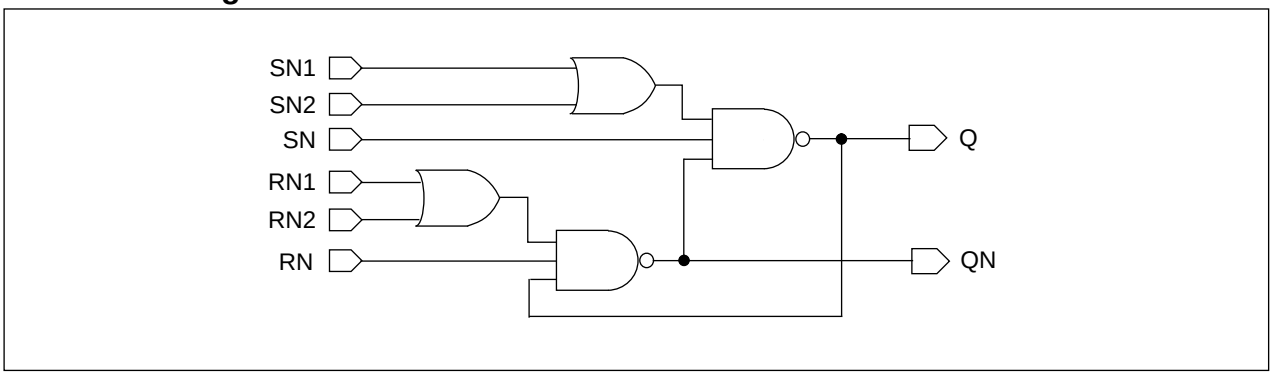
RN* = RN1 + RN2, SN* = SN1 + SN2

* Both Q and QN outputs will be unknown when RN (RN*) and SN (SN*) are low.

Cell Data

Input Load (SL)						Gate Count
STD80						
RN	RN1	RN2	SN	SN1	SN2	
0.8	0.8	0.8	0.8	0.8	0.8	3.0
STDM80						
RN	RN1	RN2	SN	SN1	SN2	
0.9	0.8	0.8	0.9	0.8	0.8	3.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LS1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN1 to Q	t_{PLH}	0.28	0.19 + 0.044*SL	0.20 + 0.041*SL	0.19 + 0.041*SL
	t_{PHL}	0.44	0.29 + 0.072*SL	0.29 + 0.072*SL	0.29 + 0.073*SL
	t_R	0.53	0.37 + 0.081*SL	0.35 + 0.089*SL	0.30 + 0.095*SL
	t_F	0.74	0.45 + 0.145*SL	0.44 + 0.150*SL	0.41 + 0.152*SL
SN2 to Q	t_{PLH}	0.27	0.19 + 0.044*SL	0.19 + 0.041*SL	0.19 + 0.041*SL
	t_{PHL}	0.50	0.36 + 0.071*SL	0.36 + 0.072*SL	0.35 + 0.073*SL
	t_R	0.52	0.36 + 0.083*SL	0.34 + 0.091*SL	0.30 + 0.095*SL
	t_F	0.85	0.57 + 0.143*SL	0.55 + 0.150*SL	0.53 + 0.152*SL
SN to Q	t_{PLH}	0.21	0.15 + 0.029*SL	0.16 + 0.024*SL	0.16 + 0.024*SL
	t_{PHL}	0.44	0.30 + 0.071*SL	0.29 + 0.072*SL	0.29 + 0.073*SL
	t_R	0.37	0.29 + 0.040*SL	0.28 + 0.045*SL	0.21 + 0.052*SL
	t_F	0.74	0.45 + 0.147*SL	0.44 + 0.150*SL	0.42 + 0.152*SL
RN1 to Q	t_{PHL}	0.73	0.48 + 0.123*SL	0.49 + 0.120*SL	0.48 + 0.121*SL
	t_F	0.75	0.43 + 0.156*SL	0.43 + 0.157*SL	0.43 + 0.158*SL
RN2 to Q	t_{PHL}	0.72	0.47 + 0.123*SL	0.48 + 0.120*SL	0.48 + 0.121*SL
	t_F	0.75	0.43 + 0.156*SL	0.43 + 0.157*SL	0.43 + 0.158*SL
RN to Q	t_{PHL}	0.64	0.42 + 0.106*SL	0.44 + 0.100*SL	0.45 + 0.099*SL
	t_F	0.73	0.42 + 0.154*SL	0.42 + 0.153*SL	0.42 + 0.154*SL
SN1 to QN	t_{PHL}	0.73	0.48 + 0.123*SL	0.49 + 0.120*SL	0.48 + 0.121*SL
	t_F	0.75	0.43 + 0.156*SL	0.43 + 0.157*SL	0.43 + 0.158*SL
SN2 to QN	t_{PHL}	0.72	0.47 + 0.123*SL	0.48 + 0.121*SL	0.48 + 0.121*SL
	t_F	0.75	0.43 + 0.156*SL	0.43 + 0.157*SL	0.43 + 0.158*SL
SN to QN	t_{PHL}	0.64	0.42 + 0.106*SL	0.44 + 0.100*SL	0.45 + 0.099*SL
	t_F	0.73	0.42 + 0.153*SL	0.42 + 0.153*SL	0.42 + 0.154*SL
RN1 to QN	t_{PLH}	0.28	0.19 + 0.044*SL	0.20 + 0.041*SL	0.19 + 0.041*SL
	t_{PHL}	0.44	0.29 + 0.072*SL	0.29 + 0.072*SL	0.29 + 0.073*SL
	t_R	0.53	0.37 + 0.081*SL	0.35 + 0.089*SL	0.30 + 0.095*SL
	t_F	0.74	0.45 + 0.145*SL	0.44 + 0.150*SL	0.41 + 0.152*SL
RN2 to QN	t_{PLH}	0.27	0.19 + 0.044*SL	0.19 + 0.041*SL	0.19 + 0.041*SL
	t_{PHL}	0.50	0.36 + 0.071*SL	0.36 + 0.072*SL	0.35 + 0.073*SL
	t_R	0.52	0.36 + 0.083*SL	0.34 + 0.091*SL	0.30 + 0.095*SL
	t_F	0.85	0.57 + 0.143*SL	0.55 + 0.150*SL	0.53 + 0.152*SL
RN to QN	t_{PLH}	0.21	0.15 + 0.029*SL	0.16 + 0.024*SL	0.16 + 0.024*SL
	t_{PHL}	0.44	0.29 + 0.072*SL	0.29 + 0.072*SL	0.29 + 0.073*SL
	t_R	0.37	0.29 + 0.040*SL	0.28 + 0.045*SL	0.21 + 0.052*SL
	t_F	0.74	0.45 + 0.146*SL	0.44 + 0.150*SL	0.42 + 0.152*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

LS1

SR Latch with Separate Inputs

Switching Characteristics

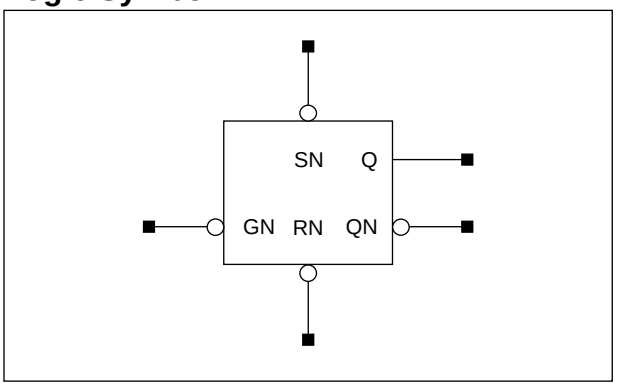
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LS1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN1 to Q	t_{PLH}	0.39	0.27 + 0.064*SL	0.27 + 0.063*SL	0.27 + 0.063*SL
	t_{PHL}	0.58	0.38 + 0.100*SL	0.38 + 0.099*SL	0.39 + 0.098*SL
	t_R	0.73	0.46 + 0.133*SL	0.45 + 0.136*SL	0.43 + 0.139*SL
	t_F	0.98	0.58 + 0.199*SL	0.58 + 0.202*SL	0.58 + 0.202*SL
SN2 to Q	t_{PLH}	0.42	0.29 + 0.064*SL	0.29 + 0.064*SL	0.29 + 0.063*SL
	t_{PHL}	0.67	0.47 + 0.099*SL	0.48 + 0.099*SL	0.48 + 0.098*SL
	t_R	0.73	0.46 + 0.134*SL	0.45 + 0.137*SL	0.44 + 0.139*SL
	t_F	1.12	0.73 + 0.199*SL	0.72 + 0.201*SL	0.72 + 0.201*SL
SN to Q	t_{PLH}	0.27	0.21 + 0.034*SL	0.21 + 0.033*SL	0.21 + 0.033*SL
	t_{PHL}	0.60	0.40 + 0.100*SL	0.40 + 0.099*SL	0.41 + 0.099*SL
	t_R	0.43	0.30 + 0.064*SL	0.29 + 0.068*SL	0.27 + 0.070*SL
	t_F	0.99	0.59 + 0.198*SL	0.58 + 0.201*SL	0.58 + 0.202*SL
RN1 to Q	t_{PHL}	1.03	0.69 + 0.173*SL	0.69 + 0.172*SL	0.69 + 0.172*SL
	t_F	1.02	0.60 + 0.208*SL	0.60 + 0.208*SL	0.60 + 0.208*SL
RN2 to Q	t_{PHL}	1.06	0.71 + 0.173*SL	0.71 + 0.172*SL	0.71 + 0.172*SL
	t_F	1.02	0.60 + 0.208*SL	0.60 + 0.208*SL	0.60 + 0.208*SL
RN to Q	t_{PHL}	0.90	0.62 + 0.139*SL	0.62 + 0.137*SL	0.63 + 0.137*SL
	t_F	0.99	0.59 + 0.203*SL	0.58 + 0.204*SL	0.59 + 0.204*SL
SN1 to QN	t_{PHL}	1.03	0.69 + 0.173*SL	0.69 + 0.172*SL	0.69 + 0.172*SL
	t_F	1.02	0.60 + 0.208*SL	0.60 + 0.208*SL	0.60 + 0.208*SL
SN2 to QN	t_{PHL}	1.06	0.71 + 0.173*SL	0.71 + 0.172*SL	0.71 + 0.172*SL
	t_F	1.02	0.60 + 0.208*SL	0.60 + 0.208*SL	0.60 + 0.208*SL
SN to QN	t_{PHL}	0.89	0.62 + 0.139*SL	0.62 + 0.137*SL	0.62 + 0.137*SL
	t_F	0.99	0.58 + 0.204*SL	0.58 + 0.204*SL	0.59 + 0.204*SL
RN1 to QN	t_{PLH}	0.39	0.27 + 0.064*SL	0.27 + 0.063*SL	0.27 + 0.063*SL
	t_{PHL}	0.58	0.38 + 0.100*SL	0.38 + 0.099*SL	0.39 + 0.098*SL
	t_R	0.73	0.46 + 0.133*SL	0.45 + 0.136*SL	0.43 + 0.139*SL
	t_F	0.98	0.58 + 0.199*SL	0.58 + 0.202*SL	0.58 + 0.202*SL
RN2 to QN	t_{PLH}	0.42	0.29 + 0.064*SL	0.29 + 0.063*SL	0.29 + 0.063*SL
	t_{PHL}	0.67	0.47 + 0.099*SL	0.48 + 0.099*SL	0.48 + 0.098*SL
	t_R	0.73	0.46 + 0.134*SL	0.45 + 0.137*SL	0.44 + 0.139*SL
	t_F	1.12	0.73 + 0.199*SL	0.72 + 0.201*SL	0.72 + 0.201*SL
RN to QN	t_{PLH}	0.27	0.21 + 0.034*SL	0.21 + 0.033*SL	0.21 + 0.033*SL
	t_{PHL}	0.60	0.40 + 0.100*SL	0.40 + 0.099*SL	0.41 + 0.099*SL
	t_R	0.43	0.30 + 0.065*SL	0.29 + 0.068*SL	0.27 + 0.070*SL
	t_F	0.99	0.59 + 0.198*SL	0.58 + 0.201*SL	0.58 + 0.202*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

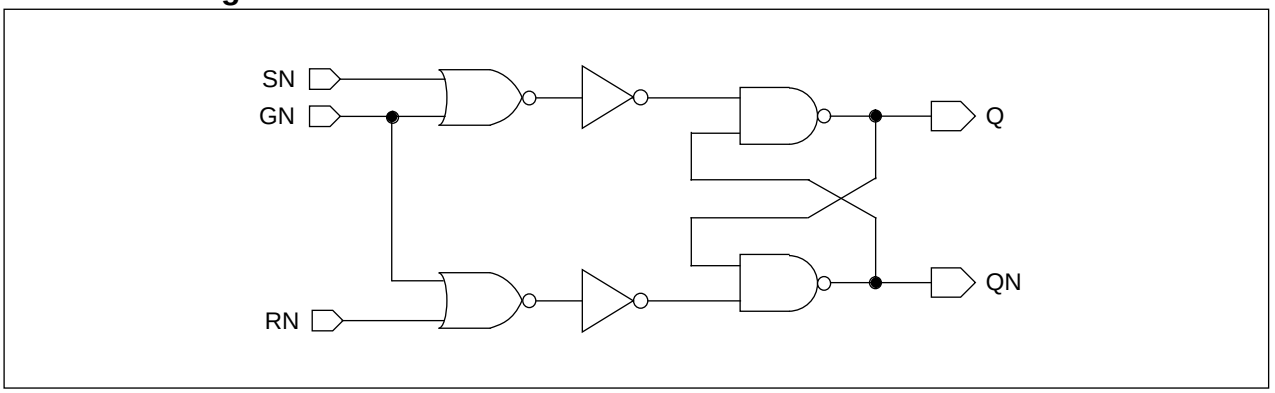
GN	RN	SN	Q (n+1)	QN (n+1)
1	x	x	Q (n)	QN (n)
0	1	1	Q (n)	QN (n)
0	0	1	0	1
0	1	0	1	0
0	0	0	*	*

* Both Q and QN outputs will be unknown when GN, RN, and SN are low.
However, if GN goes high, or RN and SN go high simultaneously, the output states are unpredictable.

Cell Data

Input Load (SL)			Gate Count
STD80			
GN	RN	SN	
1.2	0.4	0.4	4.3
STDM80			
GN	RN	SN	
1.4	0.6	0.6	4.3

Schematic Diagram



LS2

SR Latch with Common Inputs

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 LS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.48	0.43 + 0.025*SL	0.43 + 0.025*SL	0.43 + 0.025*SL
	t_{PHL}	0.41	0.33 + 0.039*SL	0.33 + 0.039*SL	0.34 + 0.039*SL
	t_R	0.25	0.15 + 0.049*SL	0.14 + 0.053*SL	0.13 + 0.054*SL
	t_F	0.35	0.20 + 0.074*SL	0.19 + 0.076*SL	0.18 + 0.078*SL
RN to Q	t_{PHL}	0.70	0.56 + 0.069*SL	0.56 + 0.068*SL	0.56 + 0.068*SL
	t_F	0.35	0.19 + 0.082*SL	0.19 + 0.082*SL	0.18 + 0.082*SL
GN to Q	t_{PLH}	0.48	0.42 + 0.026*SL	0.43 + 0.025*SL	0.43 + 0.025*SL
	t_{PHL}	0.70	0.56 + 0.070*SL	0.56 + 0.068*SL	0.56 + 0.068*SL
	t_R	0.25	0.16 + 0.047*SL	0.15 + 0.051*SL	0.14 + 0.052*SL
	t_F	0.35	0.19 + 0.081*SL	0.19 + 0.082*SL	0.18 + 0.082*SL
SN to QN	t_{PHL}	0.70	0.56 + 0.069*SL	0.56 + 0.068*SL	0.56 + 0.068*SL
	t_F	0.35	0.19 + 0.081*SL	0.19 + 0.082*SL	0.18 + 0.082*SL
RN to QN	t_{PLH}	0.48	0.43 + 0.025*SL	0.43 + 0.025*SL	0.43 + 0.025*SL
	t_{PHL}	0.41	0.33 + 0.040*SL	0.34 + 0.039*SL	0.34 + 0.039*SL
	t_R	0.25	0.15 + 0.049*SL	0.14 + 0.052*SL	0.13 + 0.054*SL
	t_F	0.35	0.20 + 0.074*SL	0.19 + 0.076*SL	0.18 + 0.078*SL
GN to QN	t_{PLH}	0.48	0.43 + 0.025*SL	0.43 + 0.025*SL	0.43 + 0.025*SL
	t_{PHL}	0.69	0.56 + 0.069*SL	0.56 + 0.068*SL	0.56 + 0.068*SL
	t_R	0.25	0.16 + 0.047*SL	0.15 + 0.051*SL	0.14 + 0.052*SL
	t_F	0.35	0.19 + 0.081*SL	0.19 + 0.082*SL	0.18 + 0.082*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 LS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.65	0.58 + 0.036*SL	0.59 + 0.035*SL	0.58 + 0.035*SL
	t_{PHL}	0.60	0.49 + 0.052*SL	0.50 + 0.050*SL	0.50 + 0.050*SL
	t_R	0.35	0.20 + 0.073*SL	0.20 + 0.074*SL	0.19 + 0.075*SL
	t_F	0.46	0.27 + 0.095*SL	0.27 + 0.097*SL	0.26 + 0.098*SL
RN to Q	t_{PHL}	0.96	0.77 + 0.095*SL	0.77 + 0.094*SL	0.77 + 0.094*SL
	t_F	0.46	0.25 + 0.105*SL	0.25 + 0.105*SL	0.25 + 0.105*SL
GN to Q	t_{PLH}	0.67	0.60 + 0.036*SL	0.60 + 0.035*SL	0.60 + 0.035*SL
	t_{PHL}	0.98	0.79 + 0.095*SL	0.79 + 0.094*SL	0.79 + 0.094*SL
	t_R	0.36	0.22 + 0.071*SL	0.21 + 0.073*SL	0.20 + 0.074*SL
	t_F	0.46	0.25 + 0.106*SL	0.25 + 0.105*SL	0.25 + 0.105*SL
SN to QN	t_{PHL}	0.96	0.76 + 0.095*SL	0.77 + 0.094*SL	0.77 + 0.094*SL
	t_F	0.46	0.25 + 0.105*SL	0.25 + 0.105*SL	0.25 + 0.105*SL
RN to QN	t_{PLH}	0.66	0.58 + 0.036*SL	0.59 + 0.035*SL	0.59 + 0.035*SL
	t_{PHL}	0.60	0.50 + 0.052*SL	0.50 + 0.050*SL	0.51 + 0.050*SL
	t_R	0.35	0.21 + 0.072*SL	0.20 + 0.074*SL	0.19 + 0.075*SL
	t_F	0.46	0.27 + 0.095*SL	0.27 + 0.097*SL	0.26 + 0.099*SL
GN to QN	t_{PLH}	0.67	0.60 + 0.036*SL	0.60 + 0.035*SL	0.61 + 0.035*SL
	t_{PHL}	0.97	0.78 + 0.095*SL	0.79 + 0.094*SL	0.79 + 0.094*SL
	t_R	0.36	0.22 + 0.071*SL	0.21 + 0.074*SL	0.21 + 0.074*SL
	t_F	0.46	0.25 + 0.106*SL	0.25 + 0.105*SL	0.25 + 0.105*SL

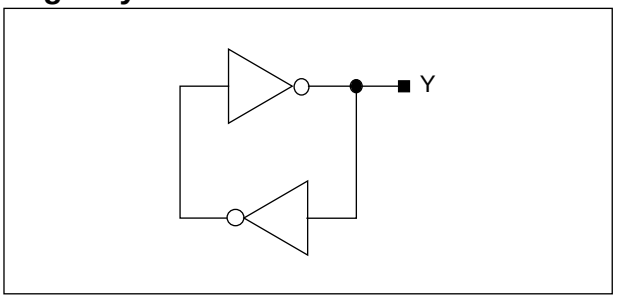
*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

BUS HOLDER

Cell List

Cell Name	Function Description
BUSHOLDER	Bus Holder

Logic Symbol



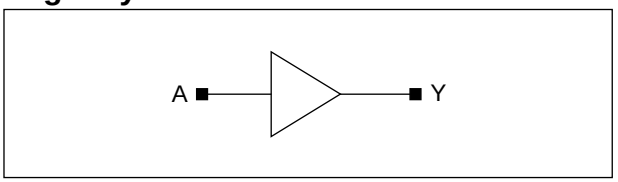
Cell Data

Input Load (SL)	Gate Count
STD80	
Y	
3.8	1.3
STDM80	
Y	
3.4	1.3

Cell List

Cell Name	Function Description
STD80	
CK2	Internal Clock Driver CMOS 2mA
CK4	Internal Clock Driver CMOS 4mA
CK8	Internal Clock Driver CMOS 8mA
CK12	Internal Clock Driver CMOS 12mA
STDM80	
CK2	Internal Clock Driver CMOS 2mA
CK4	Internal Clock Driver CMOS 4mA
CK6	Internal Clock Driver CMOS 6mA
CK8	Internal Clock Driver CMOS 8mA

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)				Gate Count			
STD80							
CK2	*CK4*	*CK8*	*CK12*	*CK2*	*CK4*	*CK8*	*CK12*
A	A	A	A				
3.1	3.1	5.5	5.5	1.0	1.0	1.0	1.0
STDM80							
CK2	*CK4*	*CK6*	*CK8*	*CK2*	*CK4*	*CK6*	*CK8*
A	A	A	A				
3.5	3.5	6.1	6.1	1.0	1.0	1.0	1.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

STD80 CK2

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.66	0.20 + 0.005*SL	0.20 + 0.005*SL	0.20 + 0.005*SL
	t_{PHL}	0.60	0.18 + 0.005*SL	0.18 + 0.005*SL	0.18 + 0.005*SL
	t_R	1.07	0.08 + 0.012*SL	0.07 + 0.012*SL	0.06 + 0.012*SL
	t_F	0.82	0.06 + 0.009*SL	0.06 + 0.009*SL	0.05 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

STD80 CK4

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.71	0.26 + 0.003*SL	0.26 + 0.003*SL	0.26 + 0.003*SL
	t_{PHL}	0.64	0.23 + 0.003*SL	0.24 + 0.002*SL	0.23 + 0.003*SL
	t_R	1.06	0.09 + 0.006*SL	0.08 + 0.006*SL	0.08 + 0.006*SL
	t_F	0.82	0.08 + 0.004*SL	0.07 + 0.005*SL	0.06 + 0.005*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

STD80 CK8

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.70	0.25 + 0.001*SL	0.25 + 0.001*SL	0.25 + 0.001*SL
	t_{PHL}	0.67	0.26 + 0.001*SL	0.26 + 0.001*SL	0.26 + 0.001*SL
	t_R	1.05	0.09 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.003*SL
	t_F	0.82	0.09 + 0.002*SL	0.08 + 0.002*SL	0.07 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

STD80 CK12

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.75	0.31 + 0.001*SL	0.31 + 0.001*SL	0.31 + 0.001*SL
	t_{PHL}	0.72	0.31 + 0.001*SL	0.32 + 0.001*SL	0.32 + 0.001*SL
	t_R	1.06	0.12 + 0.002*SL	0.10 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.83	0.11 + 0.001*SL	0.10 + 0.001*SL	0.09 + 0.002*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

STDM80 CK2

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.13	0.28 + 0.004*SL	0.28 + 0.004*SL	0.28 + 0.004*SL
	t_{PHL}	0.93	0.29 + 0.003*SL	0.29 + 0.003*SL	0.29 + 0.003*SL
	t_R	1.95	0.13 + 0.009*SL	0.10 + 0.010*SL	0.09 + 0.010*SL
	t_F	1.30	0.10 + 0.006*SL	0.09 + 0.006*SL	0.09 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

STDM80 CK4

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.23	0.39 + 0.002*SL	0.39 + 0.002*SL	0.39 + 0.002*SL
	t_{PHL}	1.03	0.39 + 0.002*SL	0.40 + 0.002*SL	0.40 + 0.002*SL
	t_R	1.95	0.17 + 0.005*SL	0.13 + 0.005*SL	0.13 + 0.005*SL
	t_F	1.31	0.16 + 0.003*SL	0.13 + 0.003*SL	0.10 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

STDM80 CK6

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.17	0.33 + 0.001*SL	0.33 + 0.001*SL	0.33 + 0.001*SL
	t_{PHL}	1.02	0.38 + 0.001*SL	0.38 + 0.001*SL	0.39 + 0.001*SL
	t_R	1.95	0.14 + 0.003*SL	0.12 + 0.003*SL	0.11 + 0.003*SL
	t_F	1.32	0.12 + 0.002*SL	0.13 + 0.002*SL	0.13 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

STDM80 CK8

Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.22	0.38 + 0.001*SL	0.38 + 0.001*SL	0.38 + 0.001*SL
	t_{PHL}	1.08	0.43 + 0.001*SL	0.44 + 0.001*SL	0.45 + 0.001*SL
	t_R	1.95	0.17 + 0.002*SL	0.14 + 0.002*SL	0.13 + 0.002*SL
	t_F	1.33	0.15 + 0.002*SL	0.16 + 0.002*SL	0.15 + 0.002*SL

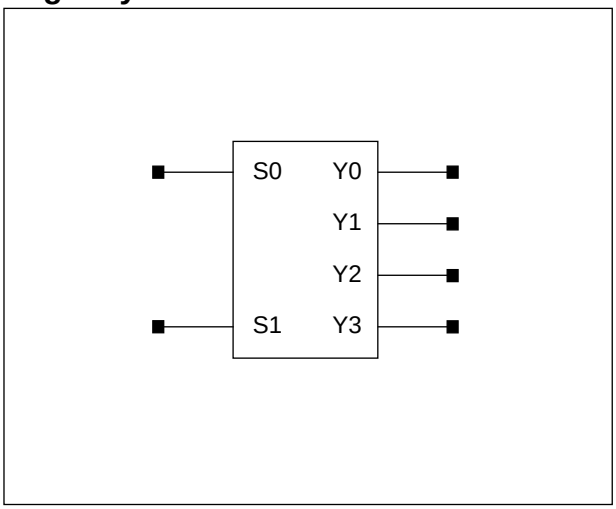
*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

DECODERS

Cell List

Cell Name	Function Description
DC4	2 > 4 Non-Inverting Decoder
DC4I	2 > 4 Inverting Decoder
DC8I	3 > 8 Inverting Decoder

Logic Symbol



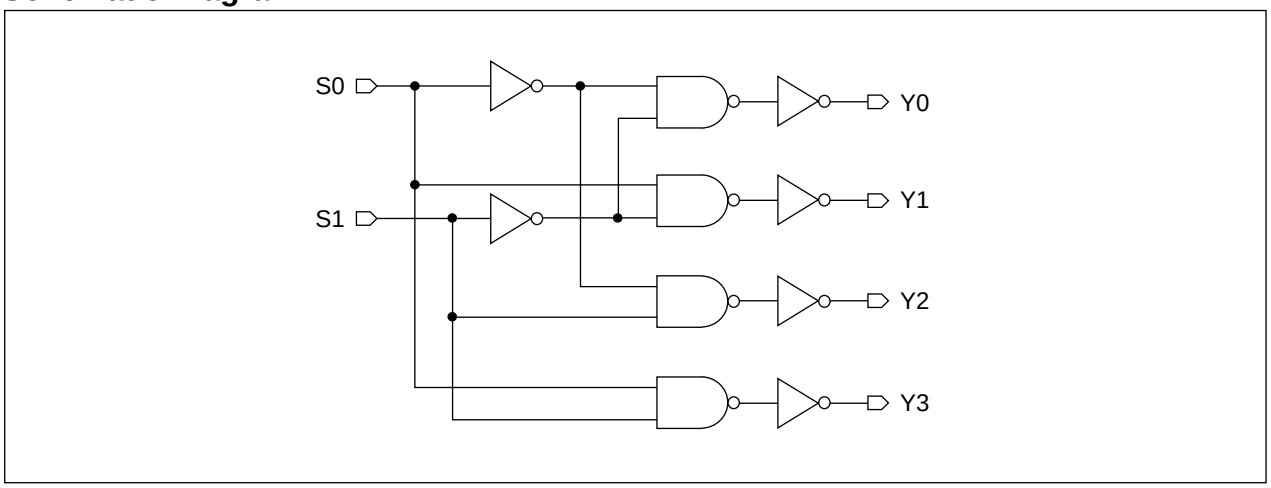
Truth Table

S1	S0	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Cell Data

Input Load (SL)		Gate Count
STD80		
S0	S1	
1.9	1.7	6.3
STDM80		
S0	S1	
2.4	2.2	6.3

Schematic Diagram



DC4

2 > 4 Non-Inverting Decoder

Switching Characteristics

(Typical process, 25℃, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 DC4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to Y0	t_{PLH}	0.44	0.38 + 0.029*SL	0.39 + 0.025*SL	0.40 + 0.024*SL
	t_{PHL}	0.45	0.37 + 0.039*SL	0.37 + 0.037*SL	0.37 + 0.037*SL
	t_R	0.20	0.11 + 0.047*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
S1 to Y0	t_{PLH}	0.43	0.37 + 0.029*SL	0.38 + 0.025*SL	0.39 + 0.024*SL
	t_{PHL}	0.41	0.33 + 0.040*SL	0.33 + 0.037*SL	0.34 + 0.037*SL
	t_R	0.20	0.10 + 0.047*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.08 + 0.068*SL	0.06 + 0.069*SL
S0 to Y1	t_{PLH}	0.26	0.20 + 0.029*SL	0.21 + 0.025*SL	0.22 + 0.024*SL
	t_{PHL}	0.34	0.26 + 0.039*SL	0.26 + 0.037*SL	0.26 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
S1 to Y1	t_{PLH}	0.43	0.37 + 0.029*SL	0.38 + 0.025*SL	0.39 + 0.024*SL
	t_{PHL}	0.41	0.33 + 0.039*SL	0.34 + 0.037*SL	0.34 + 0.037*SL
	t_R	0.20	0.11 + 0.047*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.22	0.09 + 0.066*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
S0 to Y2	t_{PLH}	0.44	0.38 + 0.029*SL	0.39 + 0.024*SL	0.40 + 0.024*SL
	t_{PHL}	0.45	0.37 + 0.039*SL	0.37 + 0.037*SL	0.38 + 0.037*SL
	t_R	0.20	0.10 + 0.048*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.22	0.09 + 0.062*SL	0.08 + 0.067*SL	0.06 + 0.069*SL
S1 to Y2	t_{PLH}	0.28	0.22 + 0.029*SL	0.23 + 0.024*SL	0.24 + 0.024*SL
	t_{PHL}	0.31	0.24 + 0.039*SL	0.24 + 0.037*SL	0.24 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
S0 to Y3	t_{PLH}	0.26	0.20 + 0.029*SL	0.21 + 0.025*SL	0.22 + 0.024*SL
	t_{PHL}	0.34	0.26 + 0.039*SL	0.27 + 0.037*SL	0.27 + 0.037*SL
	t_R	0.21	0.11 + 0.047*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
S1 to Y3	t_{PLH}	0.28	0.22 + 0.029*SL	0.23 + 0.024*SL	0.24 + 0.024*SL
	t_{PHL}	0.31	0.24 + 0.039*SL	0.24 + 0.037*SL	0.24 + 0.037*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.22	0.10 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25℃, 3.3V, tR/tF = 0.39ns, SL: Standard Load)

STDM80 DC4

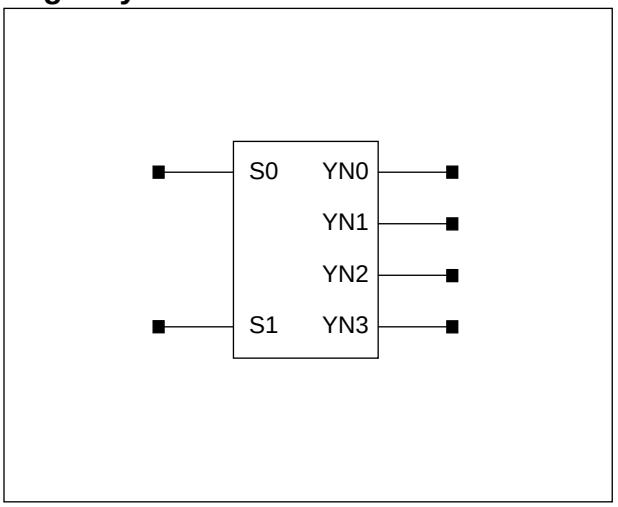
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to Y0	t_{PLH}	0.60	0.52 + 0.039*SL	0.53 + 0.035*SL	0.54 + 0.033*SL
	t_{PHL}	0.59	0.49 + 0.048*SL	0.50 + 0.045*SL	0.51 + 0.044*SL
	t_R	0.28	0.14 + 0.068*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.28	0.12 + 0.079*SL	0.11 + 0.081*SL	0.10 + 0.082*SL
S1 to Y0	t_{PLH}	0.58	0.50 + 0.039*SL	0.51 + 0.035*SL	0.52 + 0.033*SL
	t_{PHL}	0.54	0.44 + 0.048*SL	0.45 + 0.045*SL	0.46 + 0.044*SL
	t_R	0.28	0.14 + 0.068*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.27	0.11 + 0.080*SL	0.11 + 0.081*SL	0.10 + 0.083*SL
S0 to Y1	t_{PLH}	0.36	0.28 + 0.039*SL	0.29 + 0.035*SL	0.30 + 0.034*SL
	t_{PHL}	0.43	0.34 + 0.048*SL	0.35 + 0.045*SL	0.35 + 0.044*SL
	t_R	0.28	0.15 + 0.068*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.081*SL	0.11 + 0.083*SL
S1 to Y1	t_{PLH}	0.58	0.50 + 0.039*SL	0.51 + 0.035*SL	0.52 + 0.033*SL
	t_{PHL}	0.54	0.45 + 0.048*SL	0.45 + 0.045*SL	0.46 + 0.044*SL
	t_R	0.28	0.15 + 0.068*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.28	0.12 + 0.080*SL	0.11 + 0.081*SL	0.10 + 0.083*SL
S0 to Y2	t_{PLH}	0.60	0.52 + 0.040*SL	0.53 + 0.035*SL	0.54 + 0.034*SL
	t_{PHL}	0.59	0.49 + 0.048*SL	0.50 + 0.045*SL	0.51 + 0.044*SL
	t_R	0.28	0.14 + 0.067*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.28	0.12 + 0.078*SL	0.12 + 0.081*SL	0.10 + 0.083*SL
S1 to Y2	t_{PLH}	0.37	0.29 + 0.039*SL	0.30 + 0.035*SL	0.31 + 0.033*SL
	t_{PHL}	0.41	0.31 + 0.048*SL	0.32 + 0.045*SL	0.33 + 0.044*SL
	t_R	0.28	0.14 + 0.068*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.28	0.12 + 0.080*SL	0.11 + 0.081*SL	0.10 + 0.083*SL
S0 to Y3	t_{PLH}	0.36	0.28 + 0.040*SL	0.29 + 0.035*SL	0.30 + 0.034*SL
	t_{PHL}	0.43	0.34 + 0.049*SL	0.35 + 0.045*SL	0.35 + 0.044*SL
	t_R	0.28	0.15 + 0.067*SL	0.14 + 0.070*SL	0.13 + 0.071*SL
	t_F	0.28	0.12 + 0.080*SL	0.12 + 0.081*SL	0.10 + 0.083*SL
S1 to Y3	t_{PLH}	0.37	0.29 + 0.039*SL	0.30 + 0.035*SL	0.31 + 0.033*SL
	t_{PHL}	0.41	0.31 + 0.048*SL	0.32 + 0.045*SL	0.33 + 0.044*SL
	t_R	0.28	0.14 + 0.068*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.28	0.12 + 0.079*SL	0.11 + 0.081*SL	0.10 + 0.083*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

DC4I

2 > 4 Inverting Decoder

Logic Symbol



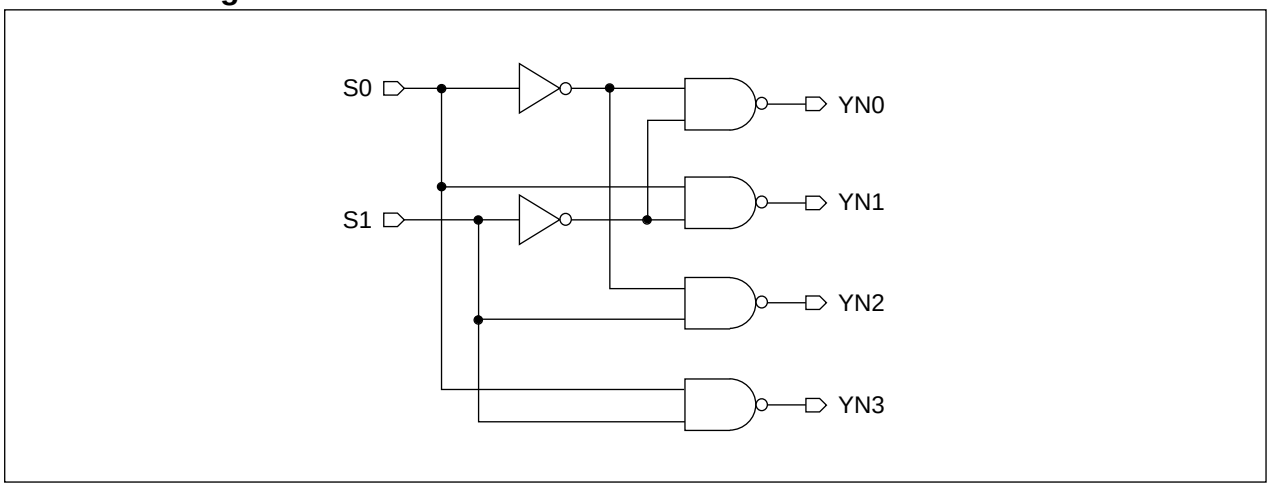
Truth Table

S1	S0	YN0	YN1	YN2	YN3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Cell Data

Input Load (SL)		Gate Count
STD80		
S0	S1	
2.3	2.5	4.3
STDM80		
S0	S1	
2.8	2.9	4.3

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 DC4I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	t_{PLH}	0.30	0.24 + 0.029*SL	0.25 + 0.025*SL	0.25 + 0.025*SL
	t_{PHL}	0.40	0.31 + 0.042*SL	0.32 + 0.039*SL	0.32 + 0.039*SL
	t_R	0.22	0.13 + 0.046*SL	0.12 + 0.051*SL	0.08 + 0.054*SL
	t_F	0.28	0.13 + 0.072*SL	0.13 + 0.075*SL	0.10 + 0.078*SL
S1 to YN0	t_{PLH}	0.31	0.25 + 0.028*SL	0.26 + 0.025*SL	0.26 + 0.025*SL
	t_{PHL}	0.38	0.30 + 0.039*SL	0.31 + 0.038*SL	0.30 + 0.039*SL
	t_R	0.24	0.15 + 0.044*SL	0.14 + 0.050*SL	0.10 + 0.054*SL
	t_F	0.27	0.13 + 0.070*SL	0.12 + 0.075*SL	0.09 + 0.078*SL
S0 to YN1	t_{PLH}	0.16	0.09 + 0.036*SL	0.11 + 0.026*SL	0.12 + 0.025*SL
	t_{PHL}	0.21	0.12 + 0.044*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
	t_R	0.28	0.19 + 0.043*SL	0.19 + 0.046*SL	0.11 + 0.054*SL
	t_F	0.32	0.20 + 0.062*SL	0.18 + 0.071*SL	0.11 + 0.078*SL
S1 to YN1	t_{PLH}	0.31	0.25 + 0.027*SL	0.26 + 0.025*SL	0.26 + 0.025*SL
	t_{PHL}	0.38	0.30 + 0.040*SL	0.31 + 0.038*SL	0.31 + 0.039*SL
	t_R	0.24	0.15 + 0.043*SL	0.14 + 0.050*SL	0.10 + 0.054*SL
	t_F	0.27	0.13 + 0.070*SL	0.12 + 0.075*SL	0.10 + 0.078*SL
S0 to YN2	t_{PLH}	0.30	0.24 + 0.029*SL	0.25 + 0.025*SL	0.25 + 0.025*SL
	t_{PHL}	0.40	0.31 + 0.041*SL	0.32 + 0.039*SL	0.32 + 0.039*SL
	t_R	0.22	0.13 + 0.043*SL	0.12 + 0.051*SL	0.08 + 0.054*SL
	t_F	0.28	0.14 + 0.071*SL	0.13 + 0.075*SL	0.10 + 0.078*SL
S1 to YN2	t_{PLH}	0.18	0.11 + 0.033*SL	0.13 + 0.025*SL	0.13 + 0.025*SL
	t_{PHL}	0.18	0.10 + 0.041*SL	0.11 + 0.038*SL	0.10 + 0.038*SL
	t_R	0.30	0.22 + 0.041*SL	0.21 + 0.046*SL	0.13 + 0.054*SL
	t_F	0.31	0.18 + 0.063*SL	0.16 + 0.071*SL	0.10 + 0.078*SL
S0 to YN3	t_{PLH}	0.16	0.09 + 0.036*SL	0.11 + 0.026*SL	0.12 + 0.025*SL
	t_{PHL}	0.21	0.12 + 0.044*SL	0.13 + 0.038*SL	0.12 + 0.038*SL
	t_R	0.28	0.19 + 0.044*SL	0.19 + 0.046*SL	0.11 + 0.054*SL
	t_F	0.32	0.19 + 0.063*SL	0.18 + 0.071*SL	0.11 + 0.078*SL
S1 to YN3	t_{PLH}	0.18	0.11 + 0.032*SL	0.13 + 0.025*SL	0.13 + 0.025*SL
	t_{PHL}	0.18	0.10 + 0.041*SL	0.11 + 0.038*SL	0.10 + 0.038*SL
	t_R	0.30	0.22 + 0.039*SL	0.21 + 0.046*SL	0.13 + 0.054*SL
	t_F	0.31	0.18 + 0.063*SL	0.16 + 0.072*SL	0.10 + 0.078*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

DC4I

2 > 4 Inverting Decoder

Switching Characteristics

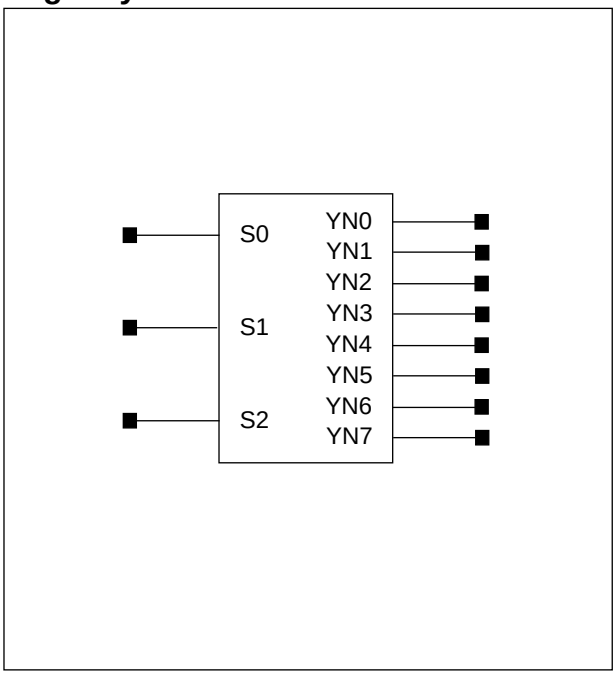
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 DC4I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	t_{PLH}	0.39	0.31 + 0.039*SL	0.32 + 0.036*SL	0.32 + 0.035*SL
	t_{PHL}	0.52	0.41 + 0.055*SL	0.42 + 0.051*SL	0.43 + 0.050*SL
	t_R	0.29	0.15 + 0.071*SL	0.14 + 0.073*SL	0.13 + 0.074*SL
	t_F	0.37	0.18 + 0.096*SL	0.18 + 0.095*SL	0.16 + 0.098*SL
S1 to YN0	t_{PLH}	0.40	0.32 + 0.038*SL	0.33 + 0.035*SL	0.33 + 0.035*SL
	t_{PHL}	0.50	0.39 + 0.053*SL	0.40 + 0.050*SL	0.41 + 0.050*SL
	t_R	0.31	0.17 + 0.070*SL	0.16 + 0.072*SL	0.15 + 0.074*SL
	t_F	0.35	0.17 + 0.094*SL	0.16 + 0.096*SL	0.15 + 0.098*SL
S0 to YN1	t_{PLH}	0.21	0.13 + 0.041*SL	0.15 + 0.034*SL	0.14 + 0.035*SL
	t_{PHL}	0.25	0.15 + 0.052*SL	0.15 + 0.049*SL	0.15 + 0.050*SL
	t_R	0.31	0.18 + 0.064*SL	0.16 + 0.070*SL	0.14 + 0.073*SL
	t_F	0.36	0.18 + 0.091*SL	0.17 + 0.094*SL	0.14 + 0.098*SL
S1 to YN1	t_{PLH}	0.40	0.32 + 0.038*SL	0.33 + 0.035*SL	0.33 + 0.035*SL
	t_{PHL}	0.50	0.39 + 0.054*SL	0.40 + 0.050*SL	0.41 + 0.050*SL
	t_R	0.31	0.17 + 0.070*SL	0.17 + 0.072*SL	0.15 + 0.075*SL
	t_F	0.35	0.16 + 0.095*SL	0.16 + 0.096*SL	0.15 + 0.098*SL
S0 to YN2	t_{PLH}	0.39	0.31 + 0.039*SL	0.32 + 0.036*SL	0.32 + 0.035*SL
	t_{PHL}	0.52	0.41 + 0.055*SL	0.42 + 0.051*SL	0.43 + 0.050*SL
	t_R	0.29	0.15 + 0.070*SL	0.14 + 0.073*SL	0.13 + 0.074*SL
	t_F	0.37	0.18 + 0.095*SL	0.18 + 0.096*SL	0.16 + 0.098*SL
S1 to YN2	t_{PLH}	0.22	0.15 + 0.038*SL	0.16 + 0.034*SL	0.16 + 0.035*SL
	t_{PHL}	0.24	0.13 + 0.053*SL	0.14 + 0.049*SL	0.14 + 0.049*SL
	t_R	0.33	0.21 + 0.062*SL	0.19 + 0.070*SL	0.16 + 0.073*SL
	t_F	0.35	0.17 + 0.091*SL	0.16 + 0.095*SL	0.14 + 0.098*SL
S0 to YN3	t_{PLH}	0.21	0.13 + 0.040*SL	0.14 + 0.035*SL	0.14 + 0.035*SL
	t_{PHL}	0.25	0.15 + 0.052*SL	0.15 + 0.049*SL	0.15 + 0.050*SL
	t_R	0.31	0.18 + 0.064*SL	0.16 + 0.070*SL	0.14 + 0.073*SL
	t_F	0.36	0.18 + 0.091*SL	0.17 + 0.095*SL	0.14 + 0.098*SL
S1 to YN3	t_{PLH}	0.22	0.15 + 0.038*SL	0.16 + 0.034*SL	0.16 + 0.035*SL
	t_{PHL}	0.24	0.13 + 0.052*SL	0.14 + 0.050*SL	0.14 + 0.050*SL
	t_R	0.33	0.21 + 0.063*SL	0.19 + 0.070*SL	0.16 + 0.073*SL
	t_F	0.35	0.16 + 0.093*SL	0.15 + 0.096*SL	0.14 + 0.098*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



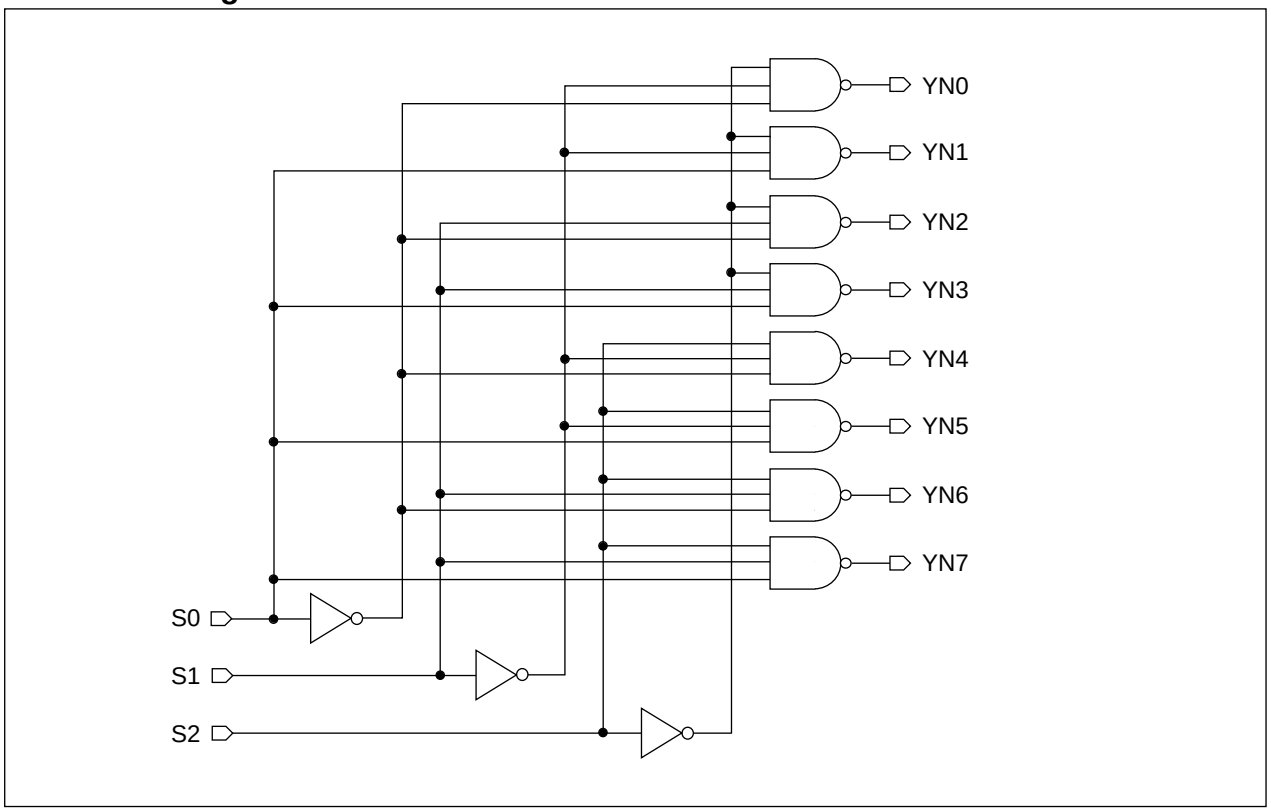
Truth Table

S0	S1	S2	YN 0	YN 1	YN 2	YN 3	YN 4	YN 5	YN 6	YN 7
0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
1	1	0	1	1	1	0	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Cell Data

Input Load (SL)			Gate Count
STD80			
S0	S1	S2	
5.2	4.8	5.2	11.0
STDM80			
S0	S1	S2	
4.9	4.9	5.2	11.0

Schematic Diagram



DC8I

3 > 8 Inverting Decoder

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	t_{PLH}	0.43	0.37 + 0.030*SL	0.38 + 0.026*SL	0.39 + 0.025*SL
	t_{PHL}	0.58	0.48 + 0.053*SL	0.48 + 0.051*SL	0.48 + 0.051*SL
	t_R	0.31	0.22 + 0.046*SL	0.21 + 0.049*SL	0.17 + 0.054*SL
	t_F	0.46	0.26 + 0.097*SL	0.25 + 0.104*SL	0.21 + 0.107*SL
S1 to YN0	t_{PLH}	0.40	0.34 + 0.031*SL	0.35 + 0.026*SL	0.37 + 0.025*SL
	t_{PHL}	0.58	0.47 + 0.053*SL	0.48 + 0.051*SL	0.48 + 0.051*SL
	t_R	0.29	0.19 + 0.045*SL	0.19 + 0.050*SL	0.14 + 0.054*SL
	t_F	0.46	0.26 + 0.102*SL	0.26 + 0.103*SL	0.21 + 0.107*SL
S2 to YN0	t_{PLH}	0.43	0.37 + 0.029*SL	0.38 + 0.026*SL	0.39 + 0.025*SL
	t_{PHL}	0.56	0.46 + 0.050*SL	0.46 + 0.050*SL	0.45 + 0.051*SL
	t_R	0.33	0.24 + 0.045*SL	0.23 + 0.048*SL	0.18 + 0.054*SL
	t_F	0.44	0.25 + 0.098*SL	0.24 + 0.104*SL	0.21 + 0.107*SL
S0 to YN1	t_{PLH}	0.19	0.13 + 0.032*SL	0.14 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.28	0.17 + 0.052*SL	0.18 + 0.050*SL	0.17 + 0.051*SL
	t_R	0.33	0.25 + 0.039*SL	0.24 + 0.047*SL	0.17 + 0.054*SL
	t_F	0.46	0.27 + 0.097*SL	0.26 + 0.102*SL	0.21 + 0.107*SL
S1 to YN1	t_{PLH}	0.40	0.34 + 0.031*SL	0.35 + 0.026*SL	0.37 + 0.025*SL
	t_{PHL}	0.58	0.47 + 0.054*SL	0.48 + 0.051*SL	0.48 + 0.051*SL
	t_R	0.28	0.19 + 0.046*SL	0.19 + 0.050*SL	0.14 + 0.054*SL
	t_F	0.46	0.26 + 0.101*SL	0.26 + 0.103*SL	0.22 + 0.107*SL
S2 to YN1	t_{PLH}	0.43	0.37 + 0.029*SL	0.38 + 0.026*SL	0.39 + 0.025*SL
	t_{PHL}	0.56	0.46 + 0.052*SL	0.46 + 0.050*SL	0.45 + 0.051*SL
	t_R	0.33	0.24 + 0.045*SL	0.23 + 0.049*SL	0.18 + 0.054*SL
	t_F	0.45	0.25 + 0.099*SL	0.24 + 0.104*SL	0.21 + 0.107*SL
S0 to YN2	t_{PLH}	0.44	0.38 + 0.030*SL	0.38 + 0.026*SL	0.40 + 0.025*SL
	t_{PHL}	0.58	0.48 + 0.053*SL	0.48 + 0.051*SL	0.48 + 0.051*SL
	t_R	0.31	0.22 + 0.045*SL	0.21 + 0.049*SL	0.16 + 0.054*SL
	t_F	0.45	0.26 + 0.097*SL	0.24 + 0.103*SL	0.20 + 0.107*SL
S1 to YN2	t_{PLH}	0.20	0.14 + 0.031*SL	0.15 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.26	0.15 + 0.051*SL	0.16 + 0.050*SL	0.15 + 0.051*SL
	t_R	0.35	0.27 + 0.040*SL	0.26 + 0.046*SL	0.18 + 0.054*SL
	t_F	0.44	0.25 + 0.097*SL	0.23 + 0.103*SL	0.20 + 0.107*SL
S2 to YN2	t_{PLH}	0.41	0.35 + 0.032*SL	0.36 + 0.026*SL	0.38 + 0.025*SL
	t_{PHL}	0.58	0.48 + 0.054*SL	0.48 + 0.051*SL	0.48 + 0.051*SL
	t_R	0.28	0.19 + 0.048*SL	0.19 + 0.049*SL	0.14 + 0.054*SL
	t_F	0.46	0.26 + 0.100*SL	0.25 + 0.103*SL	0.21 + 0.107*SL
S0 to YN3	t_{PLH}	0.19	0.12 + 0.033*SL	0.14 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.27	0.17 + 0.052*SL	0.17 + 0.050*SL	0.17 + 0.051*SL
	t_R	0.33	0.25 + 0.039*SL	0.23 + 0.047*SL	0.16 + 0.054*SL
	t_F	0.45	0.26 + 0.095*SL	0.24 + 0.102*SL	0.20 + 0.107*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S1 to YN3	t_{PLH}	0.20	0.14 + 0.031*SL	0.15 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.26	0.16 + 0.051*SL	0.16 + 0.050*SL	0.15 + 0.051*SL
	t_R	0.35	0.27 + 0.040*SL	0.26 + 0.046*SL	0.18 + 0.054*SL
	t_F	0.44	0.24 + 0.098*SL	0.23 + 0.104*SL	0.20 + 0.107*SL
S2 to YN3	t_{PLH}	0.41	0.34 + 0.034*SL	0.36 + 0.026*SL	0.38 + 0.025*SL
	t_{PHL}	0.58	0.48 + 0.054*SL	0.48 + 0.051*SL	0.48 + 0.051*SL
	t_R	0.29	0.19 + 0.048*SL	0.19 + 0.049*SL	0.14 + 0.054*SL
	t_F	0.46	0.26 + 0.100*SL	0.25 + 0.103*SL	0.21 + 0.107*SL
S0 to YN4	t_{PLH}	0.44	0.38 + 0.031*SL	0.39 + 0.026*SL	0.40 + 0.025*SL
	t_{PHL}	0.59	0.48 + 0.053*SL	0.48 + 0.051*SL	0.48 + 0.051*SL
	t_R	0.31	0.22 + 0.046*SL	0.21 + 0.049*SL	0.16 + 0.054*SL
	t_F	0.45	0.26 + 0.099*SL	0.25 + 0.103*SL	0.21 + 0.107*SL
S1 to YN4	t_{PLH}	0.40	0.34 + 0.032*SL	0.35 + 0.026*SL	0.36 + 0.025*SL
	t_{PHL}	0.58	0.47 + 0.053*SL	0.47 + 0.051*SL	0.47 + 0.051*SL
	t_R	0.28	0.19 + 0.046*SL	0.18 + 0.049*SL	0.14 + 0.054*SL
	t_F	0.45	0.25 + 0.099*SL	0.25 + 0.103*SL	0.21 + 0.107*SL
S2 to YN4	t_{PLH}	0.20	0.14 + 0.031*SL	0.15 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.26	0.16 + 0.052*SL	0.16 + 0.050*SL	0.15 + 0.051*SL
	t_R	0.35	0.27 + 0.039*SL	0.26 + 0.046*SL	0.18 + 0.054*SL
	t_F	0.44	0.25 + 0.097*SL	0.24 + 0.102*SL	0.19 + 0.107*SL
S0 to YN5	t_{PLH}	0.19	0.12 + 0.033*SL	0.14 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.27	0.17 + 0.052*SL	0.17 + 0.050*SL	0.17 + 0.051*SL
	t_R	0.33	0.25 + 0.040*SL	0.23 + 0.046*SL	0.16 + 0.054*SL
	t_F	0.45	0.26 + 0.095*SL	0.24 + 0.103*SL	0.20 + 0.107*SL
S1 to YN5	t_{PLH}	0.40	0.34 + 0.032*SL	0.35 + 0.026*SL	0.36 + 0.025*SL
	t_{PHL}	0.58	0.47 + 0.054*SL	0.48 + 0.051*SL	0.47 + 0.051*SL
	t_R	0.28	0.19 + 0.046*SL	0.18 + 0.049*SL	0.14 + 0.054*SL
	t_F	0.46	0.25 + 0.101*SL	0.25 + 0.103*SL	0.21 + 0.107*SL
S2 to YN5	t_{PLH}	0.20	0.14 + 0.030*SL	0.15 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.26	0.16 + 0.051*SL	0.16 + 0.050*SL	0.15 + 0.051*SL
	t_R	0.35	0.27 + 0.039*SL	0.26 + 0.046*SL	0.18 + 0.054*SL
	t_F	0.44	0.25 + 0.096*SL	0.23 + 0.103*SL	0.19 + 0.107*SL
S0 to YN6	t_{PLH}	0.45	0.38 + 0.031*SL	0.39 + 0.026*SL	0.41 + 0.025*SL
	t_{PHL}	0.59	0.49 + 0.052*SL	0.49 + 0.051*SL	0.49 + 0.051*SL
	t_R	0.31	0.22 + 0.047*SL	0.22 + 0.048*SL	0.16 + 0.054*SL
	t_F	0.45	0.26 + 0.096*SL	0.25 + 0.103*SL	0.21 + 0.107*SL
S1 to YN6	t_{PLH}	0.17	0.10 + 0.034*SL	0.12 + 0.026*SL	0.13 + 0.025*SL
	t_{PHL}	0.28	0.18 + 0.051*SL	0.18 + 0.050*SL	0.17 + 0.051*SL
	t_R	0.31	0.23 + 0.039*SL	0.21 + 0.047*SL	0.14 + 0.054*SL
	t_F	0.45	0.26 + 0.095*SL	0.24 + 0.102*SL	0.20 + 0.107*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

(Continued)

DC8I

3 > 8 Inverting Decoder

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S2 to YN6	t_{PLH}	0.20	0.14 + 0.031*SL	0.15 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.26	0.15 + 0.051*SL	0.16 + 0.050*SL	0.15 + 0.051*SL
	t_R	0.35	0.27 + 0.039*SL	0.26 + 0.046*SL	0.18 + 0.054*SL
	t_F	0.44	0.24 + 0.097*SL	0.23 + 0.103*SL	0.20 + 0.107*SL
S0 to YN7	t_{PLH}	0.19	0.13 + 0.032*SL	0.14 + 0.025*SL	0.14 + 0.025*SL
	t_{PHL}	0.27	0.17 + 0.050*SL	0.17 + 0.050*SL	0.16 + 0.051*SL
	t_R	0.33	0.25 + 0.040*SL	0.23 + 0.046*SL	0.16 + 0.054*SL
	t_F	0.44	0.25 + 0.095*SL	0.24 + 0.103*SL	0.20 + 0.107*SL
S1 to YN7	t_{PLH}	0.17	0.11 + 0.034*SL	0.12 + 0.026*SL	0.14 + 0.025*SL
	t_{PHL}	0.28	0.18 + 0.051*SL	0.18 + 0.050*SL	0.17 + 0.051*SL
	t_R	0.31	0.23 + 0.041*SL	0.21 + 0.046*SL	0.14 + 0.054*SL
	t_F	0.45	0.26 + 0.095*SL	0.25 + 0.102*SL	0.20 + 0.107*SL
S2 to YN7	t_{PLH}	0.20	0.14 + 0.031*SL	0.15 + 0.025*SL	0.15 + 0.025*SL
	t_{PHL}	0.26	0.16 + 0.051*SL	0.16 + 0.050*SL	0.15 + 0.051*SL
	t_R	0.35	0.27 + 0.039*SL	0.26 + 0.046*SL	0.18 + 0.054*SL
	t_F	0.44	0.25 + 0.094*SL	0.23 + 0.103*SL	0.20 + 0.107*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	t_{PLH}	0.56	0.48 + 0.041*SL	0.49 + 0.037*SL	0.50 + 0.035*SL
	t_{PHL}	0.80	0.65 + 0.073*SL	0.66 + 0.070*SL	0.67 + 0.068*SL
	t_R	0.41	0.27 + 0.069*SL	0.27 + 0.071*SL	0.25 + 0.073*SL
	t_F	0.62	0.35 + 0.134*SL	0.34 + 0.137*SL	0.33 + 0.139*SL
S1 to YN0	t_{PLH}	0.52	0.44 + 0.042*SL	0.45 + 0.037*SL	0.47 + 0.035*SL
	t_{PHL}	0.79	0.65 + 0.073*SL	0.66 + 0.069*SL	0.66 + 0.068*SL
	t_R	0.38	0.24 + 0.070*SL	0.24 + 0.071*SL	0.23 + 0.073*SL
	t_F	0.63	0.36 + 0.132*SL	0.36 + 0.135*SL	0.34 + 0.138*SL
S2 to YN0	t_{PLH}	0.55	0.47 + 0.040*SL	0.49 + 0.036*SL	0.49 + 0.035*SL
	t_{PHL}	0.76	0.62 + 0.071*SL	0.63 + 0.068*SL	0.63 + 0.068*SL
	t_R	0.43	0.30 + 0.068*SL	0.29 + 0.070*SL	0.27 + 0.073*SL
	t_F	0.60	0.34 + 0.134*SL	0.33 + 0.137*SL	0.31 + 0.139*SL
S0 to YN1	t_{PLH}	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.38	0.24 + 0.070*SL	0.24 + 0.069*SL	0.25 + 0.068*SL
	t_R	0.38	0.25 + 0.067*SL	0.24 + 0.071*SL	0.22 + 0.074*SL
	t_F	0.60	0.33 + 0.134*SL	0.32 + 0.137*SL	0.30 + 0.140*SL
S1 to YN1	t_{PLH}	0.52	0.44 + 0.042*SL	0.45 + 0.037*SL	0.47 + 0.035*SL
	t_{PHL}	0.79	0.65 + 0.073*SL	0.66 + 0.070*SL	0.67 + 0.068*SL
	t_R	0.38	0.24 + 0.070*SL	0.24 + 0.071*SL	0.22 + 0.073*SL
	t_F	0.63	0.37 + 0.133*SL	0.36 + 0.136*SL	0.34 + 0.138*SL
S2 to YN1	t_{PLH}	0.56	0.47 + 0.040*SL	0.49 + 0.036*SL	0.50 + 0.035*SL
	t_{PHL}	0.77	0.62 + 0.071*SL	0.63 + 0.069*SL	0.63 + 0.068*SL
	t_R	0.43	0.30 + 0.067*SL	0.29 + 0.071*SL	0.27 + 0.073*SL
	t_F	0.61	0.33 + 0.135*SL	0.33 + 0.138*SL	0.32 + 0.139*SL
S0 to YN2	t_{PLH}	0.56	0.48 + 0.042*SL	0.50 + 0.037*SL	0.51 + 0.035*SL
	t_{PHL}	0.80	0.65 + 0.073*SL	0.66 + 0.070*SL	0.67 + 0.068*SL
	t_R	0.40	0.27 + 0.068*SL	0.26 + 0.071*SL	0.25 + 0.073*SL
	t_F	0.61	0.34 + 0.133*SL	0.33 + 0.136*SL	0.32 + 0.138*SL
S1 to YN2	t_{PLH}	0.26	0.19 + 0.036*SL	0.19 + 0.035*SL	0.19 + 0.035*SL
	t_{PHL}	0.36	0.22 + 0.070*SL	0.23 + 0.069*SL	0.23 + 0.068*SL
	t_R	0.40	0.27 + 0.064*SL	0.25 + 0.070*SL	0.24 + 0.073*SL
	t_F	0.57	0.29 + 0.137*SL	0.29 + 0.139*SL	0.28 + 0.140*SL
S2 to YN2	t_{PLH}	0.53	0.44 + 0.042*SL	0.46 + 0.037*SL	0.47 + 0.035*SL
	t_{PHL}	0.79	0.64 + 0.074*SL	0.66 + 0.070*SL	0.67 + 0.068*SL
	t_R	0.38	0.24 + 0.069*SL	0.23 + 0.071*SL	0.22 + 0.073*SL
	t_F	0.62	0.35 + 0.134*SL	0.35 + 0.135*SL	0.33 + 0.138*SL
S0 to YN3	t_{PLH}	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.37	0.23 + 0.070*SL	0.23 + 0.069*SL	0.24 + 0.068*SL
	t_R	0.37	0.24 + 0.067*SL	0.23 + 0.071*SL	0.21 + 0.074*SL
	t_F	0.58	0.31 + 0.134*SL	0.30 + 0.138*SL	0.28 + 0.140*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

(Continued)

DC8I

3 > 8 Inverting Decoder

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S1 to YN3	t_{PLH}	0.26	0.19 + 0.035*SL	0.19 + 0.035*SL	0.19 + 0.035*SL
	t_{PHL}	0.36	0.22 + 0.070*SL	0.23 + 0.069*SL	0.23 + 0.068*SL
	t_R	0.40	0.28 + 0.064*SL	0.26 + 0.070*SL	0.23 + 0.073*SL
	t_F	0.57	0.29 + 0.137*SL	0.29 + 0.139*SL	0.28 + 0.140*SL
S2 to YN3	t_{PLH}	0.53	0.45 + 0.042*SL	0.46 + 0.037*SL	0.48 + 0.035*SL
	t_{PHL}	0.80	0.65 + 0.074*SL	0.66 + 0.070*SL	0.67 + 0.068*SL
	t_R	0.38	0.24 + 0.070*SL	0.24 + 0.071*SL	0.22 + 0.073*SL
	t_F	0.63	0.36 + 0.134*SL	0.35 + 0.135*SL	0.33 + 0.138*SL
S0 to YN4	t_{PLH}	0.57	0.48 + 0.042*SL	0.50 + 0.037*SL	0.51 + 0.035*SL
	t_{PHL}	0.80	0.65 + 0.074*SL	0.67 + 0.070*SL	0.68 + 0.068*SL
	t_R	0.41	0.27 + 0.069*SL	0.26 + 0.071*SL	0.25 + 0.073*SL
	t_F	0.61	0.35 + 0.133*SL	0.34 + 0.136*SL	0.33 + 0.138*SL
S1 to YN4	t_{PLH}	0.52	0.43 + 0.042*SL	0.45 + 0.037*SL	0.46 + 0.035*SL
	t_{PHL}	0.79	0.64 + 0.073*SL	0.65 + 0.069*SL	0.66 + 0.068*SL
	t_R	0.38	0.24 + 0.070*SL	0.23 + 0.071*SL	0.22 + 0.073*SL
	t_F	0.62	0.35 + 0.133*SL	0.35 + 0.136*SL	0.33 + 0.138*SL
S2 to YN4	t_{PLH}	0.26	0.19 + 0.035*SL	0.19 + 0.035*SL	0.19 + 0.035*SL
	t_{PHL}	0.37	0.23 + 0.070*SL	0.23 + 0.068*SL	0.24 + 0.067*SL
	t_R	0.40	0.27 + 0.065*SL	0.26 + 0.070*SL	0.24 + 0.073*SL
	t_F	0.57	0.30 + 0.133*SL	0.29 + 0.138*SL	0.27 + 0.140*SL
S0 to YN5	t_{PLH}	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.37	0.23 + 0.070*SL	0.23 + 0.068*SL	0.24 + 0.068*SL
	t_R	0.37	0.24 + 0.066*SL	0.23 + 0.071*SL	0.21 + 0.074*SL
	t_F	0.58	0.31 + 0.134*SL	0.30 + 0.138*SL	0.28 + 0.140*SL
S1 to YN5	t_{PLH}	0.52	0.43 + 0.042*SL	0.45 + 0.037*SL	0.46 + 0.035*SL
	t_{PHL}	0.79	0.64 + 0.073*SL	0.65 + 0.069*SL	0.66 + 0.068*SL
	t_R	0.38	0.24 + 0.069*SL	0.23 + 0.071*SL	0.22 + 0.073*SL
	t_F	0.62	0.35 + 0.133*SL	0.35 + 0.135*SL	0.33 + 0.138*SL
S2 to YN5	t_{PLH}	0.26	0.19 + 0.035*SL	0.19 + 0.035*SL	0.19 + 0.035*SL
	t_{PHL}	0.37	0.23 + 0.070*SL	0.23 + 0.068*SL	0.23 + 0.068*SL
	t_R	0.40	0.27 + 0.065*SL	0.26 + 0.070*SL	0.23 + 0.073*SL
	t_F	0.57	0.30 + 0.135*SL	0.29 + 0.138*SL	0.28 + 0.140*SL
S0 to YN6	t_{PLH}	0.58	0.49 + 0.042*SL	0.51 + 0.037*SL	0.52 + 0.035*SL
	t_{PHL}	0.81	0.66 + 0.073*SL	0.67 + 0.070*SL	0.68 + 0.069*SL
	t_R	0.41	0.28 + 0.067*SL	0.26 + 0.071*SL	0.25 + 0.073*SL
	t_F	0.62	0.35 + 0.132*SL	0.34 + 0.136*SL	0.32 + 0.138*SL
S1 to YN6	t_{PLH}	0.23	0.16 + 0.038*SL	0.16 + 0.035*SL	0.16 + 0.035*SL
	t_{PHL}	0.36	0.22 + 0.069*SL	0.22 + 0.068*SL	0.22 + 0.068*SL
	t_R	0.35	0.22 + 0.066*SL	0.21 + 0.071*SL	0.19 + 0.073*SL
	t_F	0.57	0.30 + 0.134*SL	0.29 + 0.138*SL	0.27 + 0.141*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S2 to YN6	t_{PLH}	0.26	0.19 + 0.035*SL	0.19 + 0.035*SL	0.19 + 0.035*SL
	t_{PHL}	0.36	0.22 + 0.070*SL	0.23 + 0.069*SL	0.23 + 0.069*SL
	t_R	0.40	0.27 + 0.065*SL	0.26 + 0.070*SL	0.23 + 0.073*SL
	t_F	0.57	0.29 + 0.138*SL	0.29 + 0.139*SL	0.28 + 0.140*SL
S0 to YN7	t_{PLH}	0.25	0.18 + 0.035*SL	0.18 + 0.035*SL	0.18 + 0.034*SL
	t_{PHL}	0.36	0.23 + 0.069*SL	0.23 + 0.068*SL	0.23 + 0.068*SL
	t_R	0.37	0.24 + 0.066*SL	0.23 + 0.070*SL	0.21 + 0.073*SL
	t_F	0.57	0.30 + 0.136*SL	0.29 + 0.139*SL	0.28 + 0.140*SL
S1 to YN7	t_{PLH}	0.23	0.16 + 0.038*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_{PHL}	0.36	0.22 + 0.068*SL	0.22 + 0.069*SL	0.23 + 0.068*SL
	t_R	0.35	0.22 + 0.066*SL	0.21 + 0.071*SL	0.19 + 0.073*SL
	t_F	0.57	0.31 + 0.134*SL	0.29 + 0.138*SL	0.28 + 0.141*SL
S2 to YN7	t_{PLH}	0.26	0.19 + 0.035*SL	0.19 + 0.035*SL	0.19 + 0.035*SL
	t_{PHL}	0.36	0.23 + 0.069*SL	0.23 + 0.069*SL	0.23 + 0.069*SL
	t_R	0.40	0.27 + 0.066*SL	0.26 + 0.070*SL	0.24 + 0.073*SL
	t_F	0.57	0.29 + 0.137*SL	0.29 + 0.139*SL	0.28 + 0.140*SL

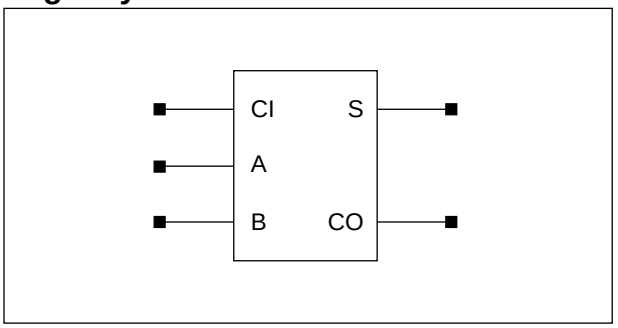
*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

ADDERS

Cell List

Cell Name	Function Description
FA	Full Adder
FAD2	Full Adder with 2X Drive
HA	Half Adder
HAD2	Half Adder with 2X Drive

Logic Symbol



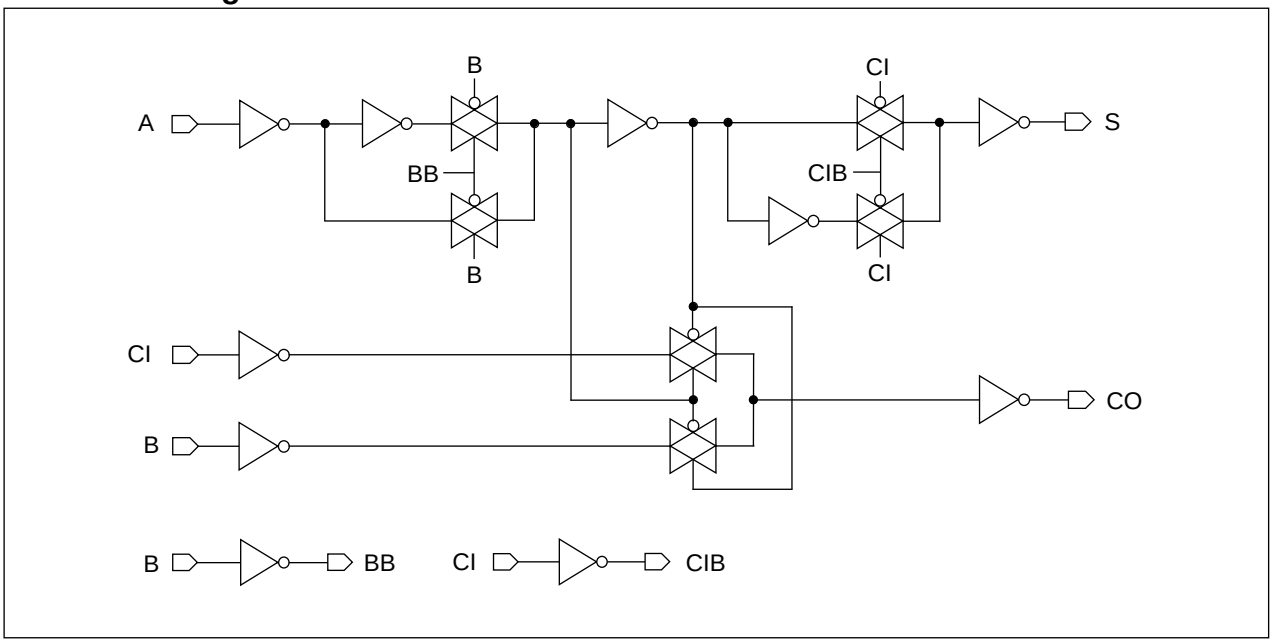
Truth Table

CI	A	B	S	CO
0	0	0	0	0
1	0	0	1	0
0	0	1	1	0
1	0	1	0	1
0	1	0	1	0
1	1	0	0	1
0	1	1	0	1
1	1	1	1	1

Cell Data

Input Load (SL)						Gate Count	
STD80							
FA			*FAD2*			*FA*	*FAD2*
CI	A	B	CI	A	B		
1.3	0.6	1.3	1.3	0.6	1.3	6.3	6.7
STDM80							
FA			*FAD2*			*FA*	*FAD2*
CI	A	B	CI	A	B		
1.5	0.7	1.6	1.5	0.7	1.6	6.3	6.7

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.84	0.78 + 0.030*SL	0.79 + 0.025*SL	0.80 + 0.024*SL
	t_{PHL}	0.90	0.81 + 0.044*SL	0.82 + 0.038*SL	0.84 + 0.037*SL
	t_R	0.21	0.12 + 0.045*SL	0.11 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.064*SL	0.13 + 0.066*SL	0.09 + 0.069*SL
B to S	t_{PLH}	0.75	0.68 + 0.035*SL	0.70 + 0.026*SL	0.73 + 0.024*SL
	t_{PHL}	0.87	0.79 + 0.044*SL	0.80 + 0.039*SL	0.81 + 0.037*SL
	t_R	0.26	0.17 + 0.044*SL	0.17 + 0.047*SL	0.12 + 0.052*SL
	t_F	0.26	0.13 + 0.064*SL	0.12 + 0.066*SL	0.09 + 0.069*SL
CI to S	t_{PLH}	0.43	0.37 + 0.032*SL	0.38 + 0.026*SL	0.40 + 0.024*SL
	t_{PHL}	0.50	0.42 + 0.044*SL	0.43 + 0.038*SL	0.44 + 0.037*SL
	t_R	0.24	0.15 + 0.044*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.27	0.14 + 0.060*SL	0.13 + 0.065*SL	0.10 + 0.069*SL
A to CO	t_{PLH}	0.72	0.65 + 0.032*SL	0.67 + 0.025*SL	0.68 + 0.024*SL
	t_{PHL}	0.86	0.77 + 0.044*SL	0.78 + 0.039*SL	0.80 + 0.037*SL
	t_R	0.25	0.16 + 0.044*SL	0.15 + 0.046*SL	0.10 + 0.052*SL
	t_F	0.28	0.16 + 0.064*SL	0.15 + 0.065*SL	0.12 + 0.069*SL
B to CO	t_{PLH}	0.59	0.53 + 0.032*SL	0.54 + 0.025*SL	0.56 + 0.024*SL
	t_{PHL}	0.66	0.57 + 0.044*SL	0.58 + 0.039*SL	0.60 + 0.037*SL
	t_R	0.25	0.17 + 0.042*SL	0.16 + 0.046*SL	0.10 + 0.052*SL
	t_F	0.26	0.12 + 0.066*SL	0.12 + 0.067*SL	0.10 + 0.069*SL
CI to CO	t_{PLH}	0.39	0.32 + 0.034*SL	0.34 + 0.025*SL	0.36 + 0.024*SL
	t_{PHL}	0.51	0.42 + 0.045*SL	0.43 + 0.039*SL	0.45 + 0.037*SL
	t_R	0.23	0.14 + 0.046*SL	0.14 + 0.048*SL	0.10 + 0.052*SL
	t_F	0.29	0.16 + 0.064*SL	0.16 + 0.065*SL	0.12 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 FAD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.85	0.81 + 0.021*SL	0.82 + 0.015*SL	0.85 + 0.012*SL
	t_{PHL}	0.91	0.85 + 0.026*SL	0.87 + 0.021*SL	0.89 + 0.018*SL
	t_R	0.18	0.13 + 0.023*SL	0.13 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.22	0.15 + 0.033*SL	0.15 + 0.031*SL	0.13 + 0.033*SL
B to S	t_{PLH}	0.78	0.73 + 0.023*SL	0.74 + 0.017*SL	0.79 + 0.012*SL
	t_{PHL}	0.89	0.84 + 0.026*SL	0.85 + 0.021*SL	0.88 + 0.018*SL
	t_R	0.23	0.19 + 0.022*SL	0.19 + 0.023*SL	0.16 + 0.025*SL
	t_F	0.21	0.14 + 0.033*SL	0.15 + 0.031*SL	0.13 + 0.034*SL
CI to S	t_{PLH}	0.45	0.41 + 0.022*SL	0.42 + 0.016*SL	0.46 + 0.012*SL
	t_{PHL}	0.52	0.46 + 0.027*SL	0.48 + 0.021*SL	0.51 + 0.018*SL
	t_R	0.22	0.17 + 0.023*SL	0.17 + 0.023*SL	0.14 + 0.026*SL
	t_F	0.23	0.16 + 0.032*SL	0.17 + 0.031*SL	0.14 + 0.033*SL
A to CO	t_{PLH}	0.74	0.70 + 0.023*SL	0.71 + 0.015*SL	0.75 + 0.012*SL
	t_{PHL}	0.87	0.81 + 0.027*SL	0.83 + 0.022*SL	0.86 + 0.018*SL
	t_R	0.23	0.19 + 0.021*SL	0.19 + 0.022*SL	0.15 + 0.025*SL
	t_F	0.24	0.18 + 0.032*SL	0.18 + 0.031*SL	0.16 + 0.033*SL
B to CO	t_{PLH}	0.62	0.57 + 0.023*SL	0.59 + 0.016*SL	0.62 + 0.012*SL
	t_{PHL}	0.68	0.63 + 0.026*SL	0.64 + 0.021*SL	0.67 + 0.018*SL
	t_R	0.23	0.19 + 0.022*SL	0.19 + 0.022*SL	0.15 + 0.025*SL
	t_F	0.21	0.15 + 0.032*SL	0.15 + 0.032*SL	0.13 + 0.033*SL
CI to CO	t_{PLH}	0.39	0.35 + 0.022*SL	0.36 + 0.015*SL	0.40 + 0.012*SL
	t_{PHL}	0.51	0.45 + 0.028*SL	0.46 + 0.022*SL	0.50 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.24	0.18 + 0.033*SL	0.18 + 0.031*SL	0.16 + 0.033*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	1.19	1.11 + 0.041*SL	1.12 + 0.035*SL	1.13 + 0.034*SL
	t_{PHL}	1.30	1.18 + 0.057*SL	1.21 + 0.048*SL	1.23 + 0.045*SL
	t_R	0.29	0.16 + 0.067*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.34	0.18 + 0.082*SL	0.19 + 0.079*SL	0.18 + 0.080*SL
B to S	t_{PLH}	1.06	0.97 + 0.044*SL	0.99 + 0.038*SL	1.01 + 0.035*SL
	t_{PHL}	1.22	1.11 + 0.057*SL	1.13 + 0.049*SL	1.16 + 0.045*SL
	t_R	0.34	0.20 + 0.067*SL	0.20 + 0.067*SL	0.19 + 0.069*SL
	t_F	0.34	0.18 + 0.081*SL	0.18 + 0.079*SL	0.17 + 0.080*SL
CI to S	t_{PLH}	0.60	0.51 + 0.042*SL	0.53 + 0.037*SL	0.54 + 0.034*SL
	t_{PHL}	0.65	0.54 + 0.057*SL	0.56 + 0.049*SL	0.59 + 0.045*SL
	t_R	0.32	0.19 + 0.067*SL	0.18 + 0.068*SL	0.17 + 0.070*SL
	t_F	0.35	0.19 + 0.081*SL	0.19 + 0.079*SL	0.19 + 0.080*SL
A to CO	t_{PLH}	1.01	0.93 + 0.042*SL	0.95 + 0.036*SL	0.96 + 0.034*SL
	t_{PHL}	1.21	1.10 + 0.058*SL	1.12 + 0.050*SL	1.15 + 0.046*SL
	t_R	0.33	0.20 + 0.064*SL	0.19 + 0.067*SL	0.17 + 0.069*SL
	t_F	0.37	0.20 + 0.083*SL	0.21 + 0.079*SL	0.21 + 0.080*SL
B to CO	t_{PLH}	0.85	0.77 + 0.042*SL	0.79 + 0.036*SL	0.80 + 0.034*SL
	t_{PHL}	0.92	0.81 + 0.057*SL	0.83 + 0.049*SL	0.85 + 0.046*SL
	t_R	0.33	0.20 + 0.064*SL	0.19 + 0.067*SL	0.17 + 0.069*SL
	t_F	0.34	0.17 + 0.084*SL	0.18 + 0.081*SL	0.18 + 0.081*SL
CI to CO	t_{PLH}	0.52	0.43 + 0.042*SL	0.45 + 0.037*SL	0.47 + 0.034*SL
	t_{PHL}	0.70	0.57 + 0.061*SL	0.61 + 0.051*SL	0.64 + 0.046*SL
	t_R	0.31	0.17 + 0.069*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_F	0.38	0.22 + 0.082*SL	0.23 + 0.078*SL	0.22 + 0.079*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 FAD2

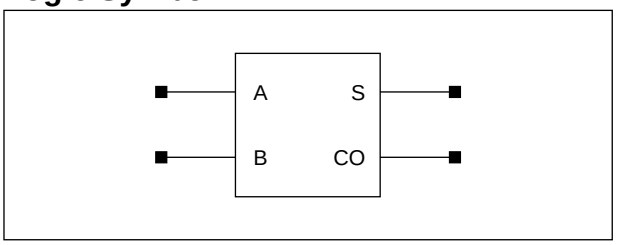
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	1.20	1.15 + 0.026*SL	1.16 + 0.021*SL	1.18 + 0.019*SL
	t_{PHL}	1.31	1.24 + 0.035*SL	1.26 + 0.029*SL	1.29 + 0.025*SL
	t_R	0.23	0.16 + 0.035*SL	0.16 + 0.034*SL	0.16 + 0.034*SL
	t_F	0.28	0.20 + 0.043*SL	0.21 + 0.040*SL	0.22 + 0.038*SL
B to S	t_{PLH}	1.09	1.03 + 0.029*SL	1.05 + 0.023*SL	1.07 + 0.020*SL
	t_{PHL}	1.24	1.17 + 0.036*SL	1.19 + 0.030*SL	1.22 + 0.025*SL
	t_R	0.28	0.21 + 0.034*SL	0.21 + 0.034*SL	0.21 + 0.033*SL
	t_F	0.28	0.19 + 0.042*SL	0.20 + 0.040*SL	0.21 + 0.038*SL
CI to S	t_{PLH}	0.63	0.57 + 0.028*SL	0.59 + 0.022*SL	0.61 + 0.019*SL
	t_{PHL}	0.67	0.59 + 0.036*SL	0.61 + 0.029*SL	0.64 + 0.025*SL
	t_R	0.27	0.20 + 0.035*SL	0.21 + 0.033*SL	0.20 + 0.033*SL
	t_F	0.29	0.21 + 0.044*SL	0.22 + 0.039*SL	0.23 + 0.038*SL
A to CO	t_{PLH}	1.05	1.00 + 0.028*SL	1.02 + 0.022*SL	1.04 + 0.019*SL
	t_{PHL}	1.23	1.15 + 0.036*SL	1.17 + 0.030*SL	1.20 + 0.026*SL
	t_R	0.28	0.21 + 0.033*SL	0.21 + 0.032*SL	0.21 + 0.032*SL
	t_F	0.31	0.22 + 0.045*SL	0.23 + 0.040*SL	0.24 + 0.038*SL
B to CO	t_{PLH}	0.89	0.84 + 0.028*SL	0.85 + 0.022*SL	0.87 + 0.019*SL
	t_{PHL}	0.96	0.89 + 0.035*SL	0.91 + 0.029*SL	0.93 + 0.026*SL
	t_R	0.28	0.21 + 0.033*SL	0.22 + 0.032*SL	0.21 + 0.032*SL
	t_F	0.27	0.19 + 0.043*SL	0.19 + 0.041*SL	0.20 + 0.039*SL
CI to CO	t_{PLH}	0.52	0.47 + 0.027*SL	0.48 + 0.022*SL	0.50 + 0.019*SL
	t_{PHL}	0.70	0.62 + 0.038*SL	0.64 + 0.031*SL	0.68 + 0.026*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.32	0.23 + 0.043*SL	0.24 + 0.040*SL	0.26 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

HA/HAD2

Half Adder with 1X/2X Drive

Logic Symbol



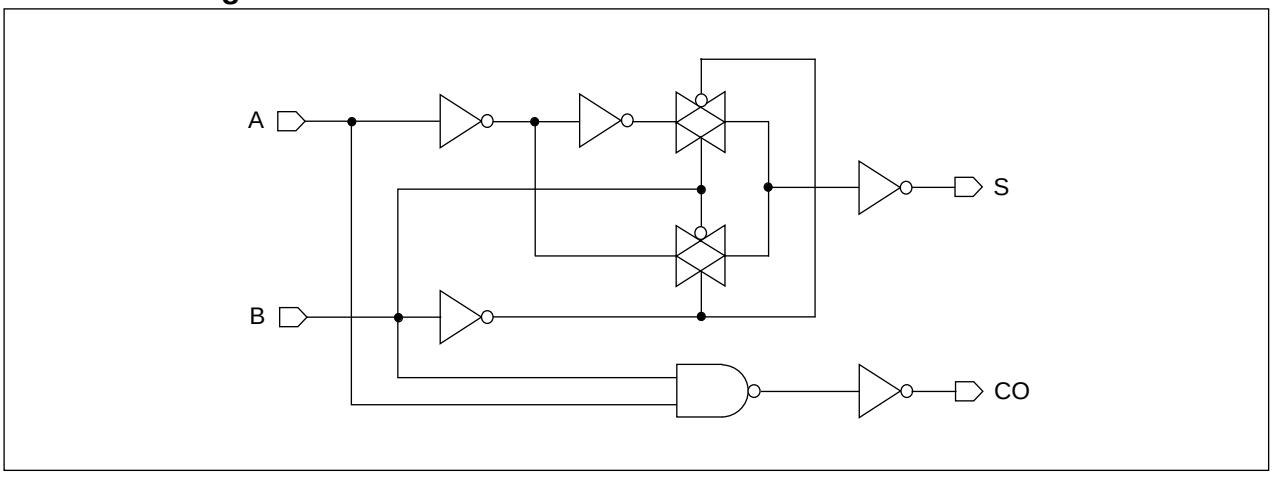
Truth Table

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Data

Input Load (SL)				Gate Count	
STD80					
HA		*HAD2*		*HA*	*HAD2*
A	B	A	B		
1.3	1.5	1.3	1.5	4.0	4.7
STDM80					
HA		*HAD2*		*HA*	*HAD2*
A	B	A	B		
1.5	2.3	1.5	2.3	4.0	4.7

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 HA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.47	0.41 + 0.031*SL	0.42 + 0.025*SL	0.43 + 0.024*SL
	t_{PHL}	0.51	0.42 + 0.044*SL	0.43 + 0.039*SL	0.45 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.14 + 0.065*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
B to S	t_{PLH}	0.34	0.28 + 0.030*SL	0.29 + 0.025*SL	0.31 + 0.024*SL
	t_{PHL}	0.40	0.31 + 0.044*SL	0.32 + 0.039*SL	0.34 + 0.037*SL
	t_R	0.21	0.11 + 0.048*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.12 + 0.066*SL	0.10 + 0.069*SL
A to CO	t_{PLH}	0.28	0.22 + 0.029*SL	0.23 + 0.025*SL	0.24 + 0.024*SL
	t_{PHL}	0.31	0.24 + 0.039*SL	0.24 + 0.037*SL	0.24 + 0.037*SL
	t_R	0.21	0.11 + 0.047*SL	0.11 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.22	0.09 + 0.065*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
B to CO	t_{PLH}	0.26	0.20 + 0.029*SL	0.21 + 0.025*SL	0.22 + 0.024*SL
	t_{PHL}	0.34	0.26 + 0.039*SL	0.26 + 0.037*SL	0.26 + 0.037*SL
	t_R	0.21	0.11 + 0.047*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.067*SL	0.07 + 0.069*SL

STD80 HAD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.47	0.43 + 0.020*SL	0.45 + 0.015*SL	0.48 + 0.012*SL
	t_{PHL}	0.51	0.46 + 0.027*SL	0.47 + 0.022*SL	0.50 + 0.018*SL
	t_R	0.18	0.14 + 0.023*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.22	0.15 + 0.034*SL	0.16 + 0.031*SL	0.13 + 0.033*SL
B to S	t_{PLH}	0.34	0.30 + 0.022*SL	0.31 + 0.015*SL	0.34 + 0.012*SL
	t_{PHL}	0.39	0.34 + 0.028*SL	0.35 + 0.022*SL	0.38 + 0.018*SL
	t_R	0.18	0.14 + 0.017*SL	0.13 + 0.024*SL	0.11 + 0.026*SL
	t_F	0.21	0.14 + 0.034*SL	0.15 + 0.032*SL	0.13 + 0.033*SL
A to CO	t_{PLH}	0.30	0.26 + 0.018*SL	0.27 + 0.014*SL	0.30 + 0.012*SL
	t_{PHL}	0.32	0.27 + 0.022*SL	0.28 + 0.019*SL	0.29 + 0.018*SL
	t_R	0.18	0.13 + 0.025*SL	0.13 + 0.023*SL	0.10 + 0.026*SL
	t_F	0.16	0.10 + 0.029*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
B to CO	t_{PLH}	0.28	0.24 + 0.018*SL	0.25 + 0.014*SL	0.27 + 0.012*SL
	t_{PHL}	0.34	0.29 + 0.023*SL	0.30 + 0.019*SL	0.31 + 0.018*SL
	t_R	0.18	0.13 + 0.022*SL	0.13 + 0.023*SL	0.10 + 0.026*SL
	t_F	0.16	0.11 + 0.027*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 HA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.64	0.55 + 0.042*SL	0.57 + 0.036*SL	0.59 + 0.034*SL
	t_{PHL}	0.72	0.61 + 0.058*SL	0.63 + 0.050*SL	0.66 + 0.046*SL
	t_R	0.29	0.16 + 0.068*SL	0.16 + 0.068*SL	0.14 + 0.070*SL
	t_F	0.35	0.19 + 0.083*SL	0.20 + 0.078*SL	0.19 + 0.080*SL
B to S	t_{PLH}	0.46	0.38 + 0.041*SL	0.40 + 0.036*SL	0.41 + 0.034*SL
	t_{PHL}	0.55	0.43 + 0.058*SL	0.45 + 0.049*SL	0.48 + 0.046*SL
	t_R	0.29	0.16 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.34	0.18 + 0.083*SL	0.19 + 0.080*SL	0.18 + 0.080*SL
A to CO	t_{PLH}	0.37	0.29 + 0.039*SL	0.30 + 0.035*SL	0.31 + 0.034*SL
	t_{PHL}	0.41	0.31 + 0.048*SL	0.32 + 0.045*SL	0.32 + 0.044*SL
	t_R	0.28	0.14 + 0.069*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.28	0.12 + 0.079*SL	0.11 + 0.081*SL	0.10 + 0.083*SL
B to CO	t_{PLH}	0.35	0.28 + 0.039*SL	0.29 + 0.035*SL	0.30 + 0.034*SL
	t_{PHL}	0.43	0.33 + 0.048*SL	0.34 + 0.045*SL	0.35 + 0.044*SL
	t_R	0.28	0.14 + 0.067*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.28	0.12 + 0.079*SL	0.11 + 0.081*SL	0.10 + 0.083*SL

STDM80 HAD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.64	0.59 + 0.027*SL	0.61 + 0.022*SL	0.63 + 0.019*SL
	t_{PHL}	0.73	0.66 + 0.036*SL	0.68 + 0.030*SL	0.70 + 0.026*SL
	t_R	0.23	0.16 + 0.035*SL	0.16 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.29	0.20 + 0.044*SL	0.21 + 0.040*SL	0.22 + 0.038*SL
B to S	t_{PLH}	0.46	0.41 + 0.026*SL	0.43 + 0.022*SL	0.45 + 0.019*SL
	t_{PHL}	0.54	0.47 + 0.036*SL	0.49 + 0.030*SL	0.52 + 0.026*SL
	t_R	0.23	0.16 + 0.037*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.28	0.19 + 0.044*SL	0.20 + 0.040*SL	0.21 + 0.039*SL
A to CO	t_{PLH}	0.39	0.34 + 0.025*SL	0.35 + 0.021*SL	0.37 + 0.018*SL
	t_{PHL}	0.41	0.35 + 0.029*SL	0.36 + 0.024*SL	0.38 + 0.022*SL
	t_R	0.22	0.14 + 0.037*SL	0.15 + 0.034*SL	0.15 + 0.034*SL
	t_F	0.19	0.11 + 0.039*SL	0.12 + 0.039*SL	0.12 + 0.039*SL
B to CO	t_{PLH}	0.38	0.33 + 0.025*SL	0.34 + 0.021*SL	0.36 + 0.018*SL
	t_{PHL}	0.43	0.37 + 0.029*SL	0.38 + 0.024*SL	0.40 + 0.022*SL
	t_R	0.22	0.15 + 0.035*SL	0.15 + 0.035*SL	0.15 + 0.034*SL
	t_F	0.20	0.12 + 0.039*SL	0.13 + 0.038*SL	0.12 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

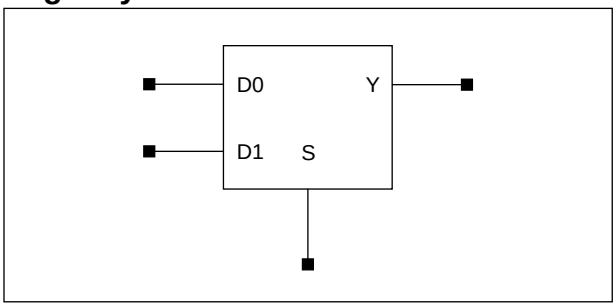
Cell List

Cell Name	Function Description
MX2	2 > 1 Non-Inverting Mux
MX2D3	2 > 1 Non-Inverting Mux with 3X Drive
MX2X4	4-Bit 2 > 1 Non-Inverting Mux
YMX2	Fast 2 > 1 Non-Inverting Mux
YMX2D2	Fast 2 > 1 Non-Inverting Mux with 2X Drive
MX2I	2 > 1 Inverting Mux
MX2ID2	2 > 1 Inverting Mux with 2X Drive
MX2IA	2 > 1 Inverting Mux with Separate S and SN Inputs
MX2ID2A	2 > 1 Inverting Mux with Separate S and SN Inputs, 2X Drive
MX2IX4	4-Bit 2 > 1 Inverting Mux
MX3I	3 > 1 Inverting Mux
MX3ID2	3 > 1 Inverting Mux with 2X Drive
MX4	4 > 1 Non-Inverting Mux
MX4D2	4 > 1 Non-Inverting Mux with 2X Drive
YMX4	Fast 4 > 1 Non-Inverting Mux
YMX4D2	Fast 4 > 1 Non-Inverting Mux with 2X Drive
MX5	5 > 1 Non-Inverting Mux
MX5D2	5 > 1 Non-Inverting Mux with 2X Drive
MX8	8 > 1 Non-Inverting Mux
MX8D2	8 > 1 Non-Inverting Mux with 2X Drive
YMX8	Fast 8 > 1 Non-Inverting Mux
YMX8D2	Fast 8 > 1 Non-Inverting Mux with 2X Drive

MX2/MX2D3

2 > 1 Non-Inverting MUX with 1X/3X Drive

Logic Symbol



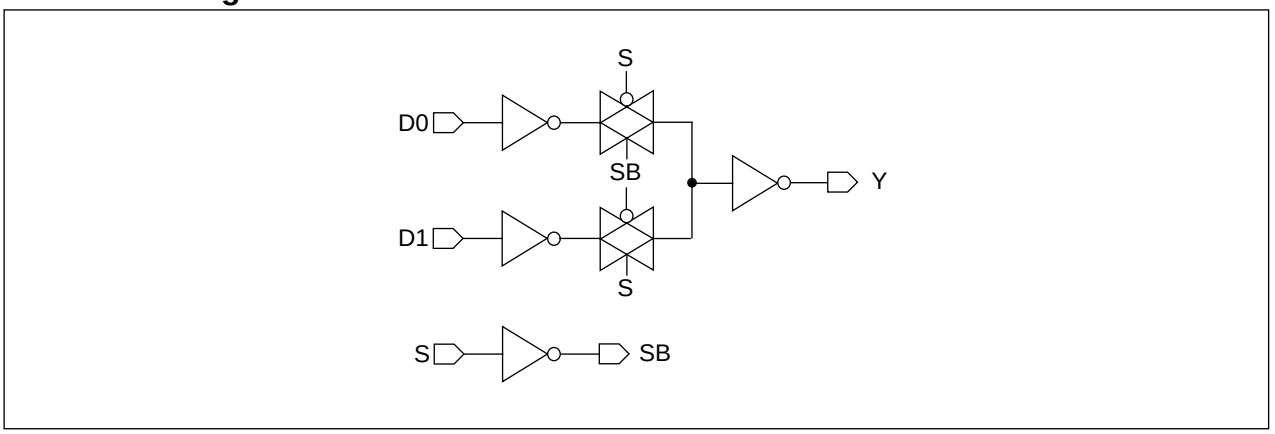
Truth Table

D0	D1	S	Y
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

Cell Data

Input Load (SL)						Gate Count	
STD80							
MX2			*MX2D3*			*MX2*	*MX2D3*
D0	D1	S	D0	D1	S		
0.7	0.7	1.0	0.6	0.6	1.0	2.7	3.3
STDM80							
MX2			*MX2D3*			*MX2*	*MX2D3*
D0	D1	S	D0	D1	S		
0.7	0.7	1.6	0.7	0.7	1.6	2.7	3.3

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.32	0.26 + 0.029*SL	0.27 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.42	0.34 + 0.043*SL	0.35 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.065*SL	0.09 + 0.069*SL
D1 to Y	t_{PLH}	0.32	0.26 + 0.030*SL	0.27 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.43	0.34 + 0.044*SL	0.35 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.066*SL	0.09 + 0.069*SL
S to Y	t_{PLH}	0.34	0.28 + 0.028*SL	0.29 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.40	0.31 + 0.044*SL	0.32 + 0.038*SL	0.33 + 0.037*SL
	t_R	0.21	0.11 + 0.047*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.25	0.12 + 0.065*SL	0.12 + 0.066*SL	0.09 + 0.069*SL

STD80 MX2D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.36	0.33 + 0.015*SL	0.34 + 0.011*SL	0.38 + 0.008*SL
	t_{PHL}	0.48	0.44 + 0.018*SL	0.45 + 0.016*SL	0.48 + 0.012*SL
	t_R	0.20	0.17 + 0.016*SL	0.17 + 0.016*SL	0.15 + 0.017*SL
	t_F	0.23	0.19 + 0.023*SL	0.19 + 0.021*SL	0.18 + 0.022*SL
D1 to Y	t_{PLH}	0.36	0.33 + 0.015*SL	0.34 + 0.011*SL	0.37 + 0.008*SL
	t_{PHL}	0.48	0.44 + 0.019*SL	0.45 + 0.016*SL	0.48 + 0.012*SL
	t_R	0.20	0.17 + 0.015*SL	0.17 + 0.015*SL	0.15 + 0.017*SL
	t_F	0.23	0.19 + 0.021*SL	0.19 + 0.021*SL	0.18 + 0.022*SL
S to Y	t_{PLH}	0.37	0.34 + 0.016*SL	0.35 + 0.011*SL	0.38 + 0.008*SL
	t_{PHL}	0.44	0.40 + 0.019*SL	0.41 + 0.016*SL	0.44 + 0.012*SL
	t_R	0.20	0.16 + 0.016*SL	0.16 + 0.016*SL	0.15 + 0.017*SL
	t_F	0.23	0.18 + 0.023*SL	0.18 + 0.021*SL	0.17 + 0.022*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX2

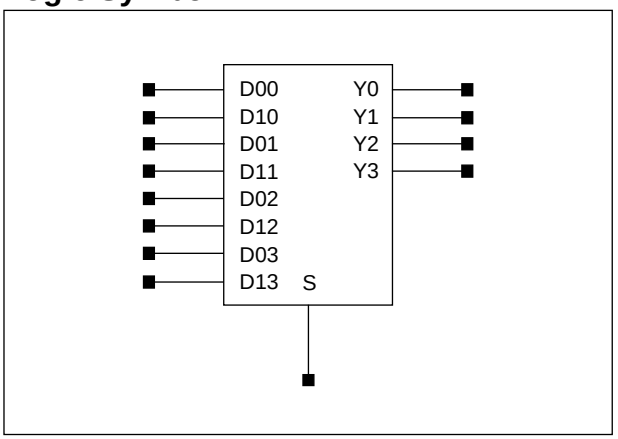
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.43	0.35 + 0.040*SL	0.36 + 0.035*SL	0.37 + 0.033*SL
	t_{PHL}	0.57	0.45 + 0.057*SL	0.48 + 0.049*SL	0.50 + 0.045*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.34	0.18 + 0.082*SL	0.18 + 0.079*SL	0.18 + 0.080*SL
D1 to Y	t_{PLH}	0.42	0.34 + 0.040*SL	0.36 + 0.035*SL	0.37 + 0.034*SL
	t_{PHL}	0.57	0.46 + 0.056*SL	0.48 + 0.049*SL	0.51 + 0.045*SL
	t_R	0.29	0.15 + 0.067*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.34	0.18 + 0.080*SL	0.18 + 0.079*SL	0.17 + 0.080*SL
S to Y	t_{PLH}	0.46	0.38 + 0.040*SL	0.40 + 0.035*SL	0.41 + 0.034*SL
	t_{PHL}	0.54	0.43 + 0.057*SL	0.45 + 0.048*SL	0.47 + 0.045*SL
	t_R	0.29	0.15 + 0.067*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.34	0.17 + 0.082*SL	0.18 + 0.079*SL	0.17 + 0.080*SL

STDM80 MX2D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.49	0.45 + 0.020*SL	0.46 + 0.016*SL	0.47 + 0.014*SL
	t_{PHL}	0.66	0.60 + 0.026*SL	0.62 + 0.022*SL	0.64 + 0.019*SL
	t_R	0.24	0.20 + 0.024*SL	0.20 + 0.023*SL	0.20 + 0.023*SL
	t_F	0.30	0.24 + 0.031*SL	0.25 + 0.027*SL	0.26 + 0.026*SL
D1 to Y	t_{PLH}	0.48	0.44 + 0.020*SL	0.45 + 0.016*SL	0.47 + 0.014*SL
	t_{PHL}	0.66	0.61 + 0.026*SL	0.62 + 0.022*SL	0.64 + 0.019*SL
	t_R	0.24	0.19 + 0.024*SL	0.20 + 0.023*SL	0.20 + 0.023*SL
	t_F	0.30	0.24 + 0.031*SL	0.25 + 0.028*SL	0.26 + 0.026*SL
S to Y	t_{PLH}	0.51	0.47 + 0.020*SL	0.48 + 0.016*SL	0.49 + 0.014*SL
	t_{PHL}	0.61	0.56 + 0.026*SL	0.57 + 0.022*SL	0.59 + 0.019*SL
	t_R	0.25	0.20 + 0.025*SL	0.20 + 0.023*SL	0.20 + 0.023*SL
	t_F	0.30	0.24 + 0.030*SL	0.24 + 0.028*SL	0.26 + 0.026*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

S	Y0	Y1	Y2	Y3
0	D00	D01	D02	D03
1	D10	D11	D12	D13

Cell Data

Input Load (SL)		Gate Count
STD80		
Dxy	S	
0.7	1.8	8.7
STDM80		
Dxy	S	
0.7	3.9	8.7

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to Y0	t_{PLH}	0.32	0.26 + 0.030*SL	0.27 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.42	0.34 + 0.044*SL	0.35 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.065*SL	0.09 + 0.069*SL
D10 to Y0	t_{PLH}	0.32	0.26 + 0.029*SL	0.27 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.43	0.34 + 0.043*SL	0.35 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.22	0.12 + 0.045*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.064*SL	0.13 + 0.066*SL	0.09 + 0.069*SL
S to Y0	t_{PLH}	0.43	0.37 + 0.031*SL	0.39 + 0.025*SL	0.40 + 0.024*SL
	t_{PHL}	0.49	0.41 + 0.044*SL	0.42 + 0.038*SL	0.43 + 0.037*SL
	t_R	0.23	0.15 + 0.042*SL	0.13 + 0.047*SL	0.09 + 0.052*SL
	t_F	0.26	0.14 + 0.064*SL	0.13 + 0.065*SL	0.09 + 0.069*SL
D01 to Y1	t_{PLH}	0.32	0.26 + 0.029*SL	0.27 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.43	0.34 + 0.043*SL	0.35 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.22	0.14 + 0.039*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.066*SL	0.10 + 0.069*SL
D11 to Y1	t_{PLH}	0.32	0.26 + 0.030*SL	0.27 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.43	0.34 + 0.043*SL	0.35 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.065*SL	0.10 + 0.069*SL
S to Y1	t_{PLH}	0.44	0.37 + 0.031*SL	0.39 + 0.025*SL	0.40 + 0.024*SL
	t_{PHL}	0.49	0.41 + 0.044*SL	0.42 + 0.038*SL	0.43 + 0.037*SL
	t_R	0.23	0.15 + 0.042*SL	0.14 + 0.047*SL	0.09 + 0.052*SL
	t_F	0.27	0.14 + 0.064*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
D02 to Y2	t_{PLH}	0.32	0.26 + 0.029*SL	0.27 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.43	0.34 + 0.043*SL	0.35 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.26	0.13 + 0.064*SL	0.13 + 0.066*SL	0.10 + 0.069*SL
D12 to Y2	t_{PLH}	0.32	0.26 + 0.029*SL	0.27 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.43	0.34 + 0.044*SL	0.35 + 0.038*SL	0.37 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.065*SL	0.10 + 0.069*SL
S to Y2	t_{PLH}	0.44	0.37 + 0.031*SL	0.39 + 0.025*SL	0.40 + 0.024*SL
	t_{PHL}	0.49	0.41 + 0.044*SL	0.42 + 0.038*SL	0.43 + 0.037*SL
	t_R	0.23	0.15 + 0.043*SL	0.14 + 0.047*SL	0.09 + 0.052*SL
	t_F	0.27	0.14 + 0.063*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
D03 to Y3	t_{PLH}	0.32	0.26 + 0.031*SL	0.27 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.42	0.34 + 0.043*SL	0.35 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.065*SL	0.09 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D13 to Y3	t_{PLH}	0.32	0.26 + 0.029*SL	0.27 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.43	0.34 + 0.043*SL	0.35 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.064*SL	0.13 + 0.066*SL	0.09 + 0.069*SL
S to Y3	t_{PLH}	0.43	0.37 + 0.031*SL	0.38 + 0.025*SL	0.40 + 0.024*SL
	t_{PHL}	0.49	0.41 + 0.043*SL	0.42 + 0.038*SL	0.43 + 0.037*SL
	t_R	0.23	0.15 + 0.042*SL	0.13 + 0.047*SL	0.09 + 0.052*SL
	t_F	0.26	0.14 + 0.064*SL	0.13 + 0.065*SL	0.09 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to Y0	t_{PLH}	0.43	0.35 + 0.040*SL	0.36 + 0.035*SL	0.37 + 0.033*SL
	t_{PHL}	0.57	0.45 + 0.057*SL	0.48 + 0.048*SL	0.50 + 0.045*SL
	t_R	0.29	0.15 + 0.067*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.34	0.18 + 0.081*SL	0.18 + 0.079*SL	0.17 + 0.080*SL
D10 to Y0	t_{PLH}	0.42	0.34 + 0.040*SL	0.36 + 0.035*SL	0.37 + 0.033*SL
	t_{PHL}	0.57	0.46 + 0.057*SL	0.48 + 0.048*SL	0.51 + 0.045*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.34	0.18 + 0.082*SL	0.18 + 0.079*SL	0.18 + 0.080*SL
S to Y0	t_{PLH}	0.60	0.52 + 0.042*SL	0.54 + 0.035*SL	0.55 + 0.034*SL
	t_{PHL}	0.65	0.53 + 0.056*SL	0.56 + 0.049*SL	0.58 + 0.045*SL
	t_R	0.31	0.18 + 0.065*SL	0.18 + 0.066*SL	0.15 + 0.070*SL
	t_F	0.35	0.18 + 0.081*SL	0.19 + 0.078*SL	0.18 + 0.080*SL
D01 to Y1	t_{PLH}	0.43	0.35 + 0.040*SL	0.36 + 0.035*SL	0.38 + 0.033*SL
	t_{PHL}	0.57	0.46 + 0.056*SL	0.48 + 0.049*SL	0.51 + 0.045*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.070*SL
	t_F	0.34	0.18 + 0.082*SL	0.19 + 0.079*SL	0.18 + 0.080*SL
D11 to Y1	t_{PLH}	0.43	0.35 + 0.040*SL	0.36 + 0.035*SL	0.37 + 0.033*SL
	t_{PHL}	0.58	0.46 + 0.057*SL	0.49 + 0.048*SL	0.51 + 0.045*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.34	0.18 + 0.081*SL	0.19 + 0.079*SL	0.18 + 0.080*SL
S to Y1	t_{PLH}	0.60	0.52 + 0.042*SL	0.54 + 0.035*SL	0.55 + 0.033*SL
	t_{PHL}	0.65	0.53 + 0.057*SL	0.56 + 0.049*SL	0.58 + 0.045*SL
	t_R	0.31	0.18 + 0.066*SL	0.18 + 0.067*SL	0.16 + 0.070*SL
	t_F	0.35	0.19 + 0.081*SL	0.20 + 0.078*SL	0.19 + 0.080*SL
D02 to Y2	t_{PLH}	0.43	0.35 + 0.040*SL	0.36 + 0.035*SL	0.38 + 0.033*SL
	t_{PHL}	0.57	0.46 + 0.056*SL	0.48 + 0.049*SL	0.51 + 0.045*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.34	0.18 + 0.082*SL	0.19 + 0.079*SL	0.18 + 0.080*SL
D12 to Y2	t_{PLH}	0.43	0.35 + 0.040*SL	0.36 + 0.035*SL	0.37 + 0.034*SL
	t_{PHL}	0.58	0.46 + 0.056*SL	0.49 + 0.049*SL	0.51 + 0.045*SL
	t_R	0.29	0.15 + 0.069*SL	0.15 + 0.068*SL	0.14 + 0.071*SL
	t_F	0.34	0.18 + 0.082*SL	0.19 + 0.079*SL	0.18 + 0.080*SL
S to Y2	t_{PLH}	0.60	0.52 + 0.041*SL	0.54 + 0.036*SL	0.55 + 0.033*SL
	t_{PHL}	0.65	0.53 + 0.057*SL	0.56 + 0.048*SL	0.58 + 0.045*SL
	t_R	0.31	0.18 + 0.065*SL	0.18 + 0.067*SL	0.16 + 0.070*SL
	t_F	0.35	0.19 + 0.081*SL	0.20 + 0.078*SL	0.19 + 0.080*SL
D03 to Y3	t_{PLH}	0.43	0.35 + 0.040*SL	0.36 + 0.035*SL	0.37 + 0.034*SL
	t_{PHL}	0.57	0.46 + 0.056*SL	0.48 + 0.049*SL	0.50 + 0.045*SL
	t_R	0.29	0.15 + 0.067*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.34	0.18 + 0.082*SL	0.19 + 0.079*SL	0.18 + 0.080*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX2X4

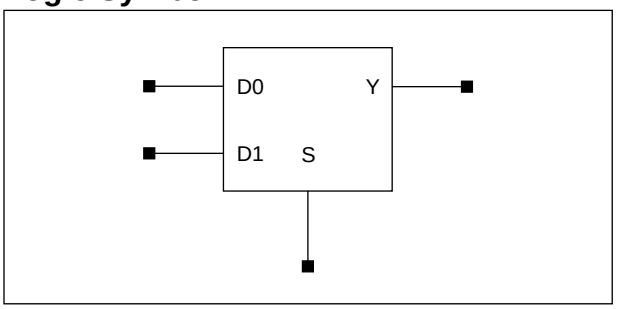
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D13 to Y3	t_{PLH}	0.42	0.34 + 0.040*SL	0.36 + 0.035*SL	0.37 + 0.033*SL
	t_{PHL}	0.57	0.46 + 0.057*SL	0.48 + 0.048*SL	0.51 + 0.045*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.34	0.18 + 0.082*SL	0.18 + 0.079*SL	0.18 + 0.080*SL
S to Y3	t_{PLH}	0.60	0.52 + 0.041*SL	0.54 + 0.035*SL	0.55 + 0.034*SL
	t_{PHL}	0.65	0.53 + 0.057*SL	0.56 + 0.049*SL	0.58 + 0.045*SL
	t_R	0.31	0.18 + 0.065*SL	0.18 + 0.067*SL	0.16 + 0.070*SL
	t_F	0.35	0.18 + 0.081*SL	0.19 + 0.078*SL	0.18 + 0.080*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

YMX2/YMX2D2

Fast 2 > 1 Non-Inverting MUX with 1X/2X Drive

Logic Symbol



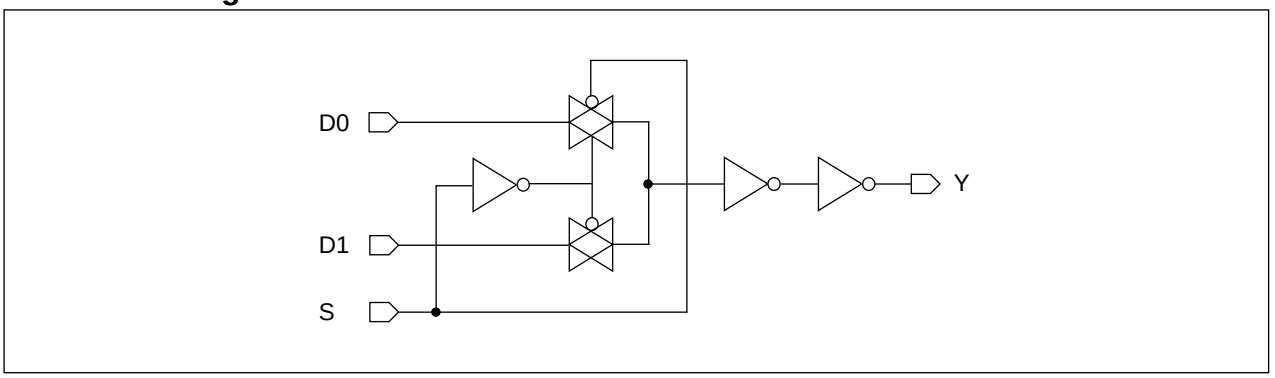
Truth Table

D0	D1	S	Y
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

Cell Data

Input Load (SL)						Gate Count	
STD80							
YMX2			*YMX2D2*			*YMX2*	*YMX2D2*
D0	D1	S	D0	D1	S		
2.2	2.2	1.2	2.2	2.2	0.9	2.7	3.0
STDM80							
YMX2			*YMX2D2*			*YMX2*	*YMX2D2*
D0	D1	S	D0	D1	S		
2.5	2.5	1.2	2.5	0.7	1.2	2.7	3.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 YMX2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.26	0.21 + 0.026*SL	0.22 + 0.024*SL	0.22 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.039*SL	0.28 + 0.037*SL	0.28 + 0.037*SL
	t_R	0.19	0.11 + 0.043*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.063*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
D1 to Y	t_{PLH}	0.26	0.21 + 0.026*SL	0.22 + 0.024*SL	0.22 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.039*SL	0.28 + 0.037*SL	0.28 + 0.037*SL
	t_R	0.19	0.11 + 0.042*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
S to Y	t_{PLH}	0.34	0.28 + 0.026*SL	0.29 + 0.024*SL	0.29 + 0.024*SL
	t_{PHL}	0.36	0.28 + 0.039*SL	0.29 + 0.037*SL	0.29 + 0.037*SL
	t_R	0.18	0.09 + 0.045*SL	0.08 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.21	0.08 + 0.066*SL	0.08 + 0.068*SL	0.06 + 0.069*SL

STD80 YMX2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.28	0.25 + 0.017*SL	0.25 + 0.013*SL	0.26 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.022*SL	0.32 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.15	0.11 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.09 + 0.032*SL	0.07 + 0.034*SL
D1 to Y	t_{PLH}	0.28	0.25 + 0.016*SL	0.25 + 0.013*SL	0.26 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.022*SL	0.32 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.09 + 0.031*SL	0.09 + 0.031*SL	0.07 + 0.034*SL
S to Y	t_{PLH}	0.34	0.31 + 0.018*SL	0.32 + 0.013*SL	0.33 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.022*SL	0.32 + 0.019*SL	0.33 + 0.018*SL
	t_R	0.14	0.11 + 0.014*SL	0.09 + 0.024*SL	0.07 + 0.026*SL
	t_F	0.15	0.09 + 0.032*SL	0.09 + 0.032*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 YMX2

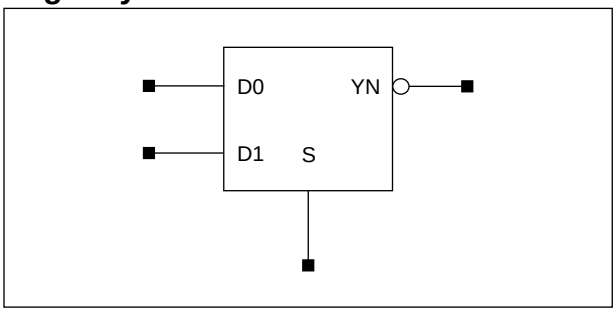
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.37	0.30 + 0.035*SL	0.31 + 0.033*SL	0.31 + 0.033*SL
	t_{PHL}	0.47	0.38 + 0.048*SL	0.38 + 0.045*SL	0.39 + 0.044*SL
	t_R	0.25	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.11 + 0.081*SL	0.10 + 0.083*SL
D1 to Y	t_{PLH}	0.37	0.30 + 0.035*SL	0.31 + 0.034*SL	0.31 + 0.033*SL
	t_{PHL}	0.47	0.37 + 0.048*SL	0.38 + 0.045*SL	0.38 + 0.044*SL
	t_R	0.25	0.12 + 0.067*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.080*SL	0.11 + 0.081*SL	0.10 + 0.083*SL
S to Y	t_{PLH}	0.49	0.42 + 0.035*SL	0.43 + 0.034*SL	0.43 + 0.033*SL
	t_{PHL}	0.60	0.51 + 0.048*SL	0.52 + 0.045*SL	0.52 + 0.044*SL
	t_R	0.25	0.12 + 0.067*SL	0.11 + 0.071*SL	0.10 + 0.072*SL
	t_F	0.27	0.11 + 0.080*SL	0.11 + 0.082*SL	0.10 + 0.083*SL

STDM80 YMX2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.38	0.34 + 0.021*SL	0.35 + 0.018*SL	0.36 + 0.017*SL
	t_{PHL}	0.47	0.41 + 0.028*SL	0.43 + 0.024*SL	0.44 + 0.022*SL
	t_R	0.18	0.12 + 0.032*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.20	0.12 + 0.037*SL	0.12 + 0.038*SL	0.12 + 0.039*SL
D1 to Y	t_{PLH}	0.38	0.34 + 0.022*SL	0.35 + 0.018*SL	0.36 + 0.017*SL
	t_{PHL}	0.47	0.41 + 0.029*SL	0.42 + 0.024*SL	0.44 + 0.022*SL
	t_R	0.18	0.12 + 0.031*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.20	0.12 + 0.038*SL	0.12 + 0.038*SL	0.12 + 0.038*SL
S to Y	t_{PLH}	0.50	0.45 + 0.022*SL	0.46 + 0.018*SL	0.47 + 0.017*SL
	t_{PHL}	0.60	0.55 + 0.028*SL	0.56 + 0.024*SL	0.57 + 0.022*SL
	t_R	0.18	0.11 + 0.033*SL	0.11 + 0.034*SL	0.10 + 0.035*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.039*SL	0.11 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



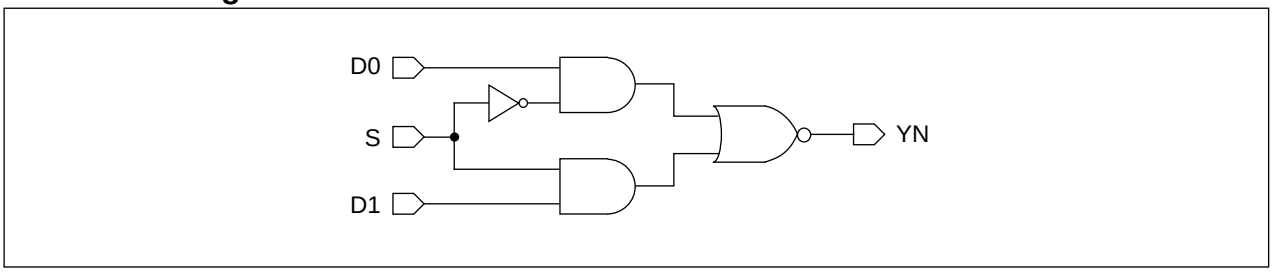
Truth Table

D0	D1	S	YN
0	x	0	1
1	x	0	0
x	0	1	1
x	1	1	0

Cell Data

Input Load (SL)						Gate Count	
STD80							
MX2I			*MX2ID2*			*MX2I*	*MX2ID2*
D0	D1	S	D0	D1	S		
0.5	0.9	1.5	0.7	0.6	1.0	2.3	3.7
STDM80							
MX2I			*MX2ID2*			*MX2I*	*MX2ID2*
D0	D1	S	D0	D1	S		
1.0	1.0	1.6	0.7	0.7	1.6	2.3	3.7

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX2I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.24	0.15 + 0.044*SL	0.16 + 0.040*SL	0.15 + 0.041*SL
	t_{PHL}	0.26	0.14 + 0.057*SL	0.15 + 0.055*SL	0.15 + 0.055*SL
	t_R	0.46	0.30 + 0.079*SL	0.28 + 0.088*SL	0.21 + 0.095*SL
	t_F	0.42	0.22 + 0.097*SL	0.20 + 0.106*SL	0.16 + 0.111*SL
D1 to YN	t_{PLH}	0.25	0.15 + 0.047*SL	0.17 + 0.042*SL	0.17 + 0.041*SL
	t_{PHL}	0.42	0.31 + 0.055*SL	0.31 + 0.055*SL	0.31 + 0.055*SL
	t_R	0.40	0.24 + 0.080*SL	0.22 + 0.090*SL	0.17 + 0.095*SL
	t_F	0.60	0.39 + 0.102*SL	0.38 + 0.107*SL	0.35 + 0.111*SL
S to YN	t_{PLH}	0.25	0.16 + 0.043*SL	0.17 + 0.041*SL	0.16 + 0.041*SL
	t_{PHL}	0.39	0.28 + 0.056*SL	0.28 + 0.055*SL	0.28 + 0.055*SL
	t_R	0.43	0.26 + 0.081*SL	0.24 + 0.091*SL	0.21 + 0.095*SL
	t_F	0.35	0.14 + 0.107*SL	0.13 + 0.109*SL	0.12 + 0.111*SL

STD80 MX2ID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.44	0.41 + 0.016*SL	0.42 + 0.013*SL	0.43 + 0.012*SL
	t_{PHL}	0.46	0.42 + 0.022*SL	0.42 + 0.019*SL	0.43 + 0.018*SL
	t_R	0.14	0.10 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.15	0.09 + 0.030*SL	0.09 + 0.032*SL	0.07 + 0.034*SL
D1 to YN	t_{PLH}	0.44	0.41 + 0.016*SL	0.42 + 0.013*SL	0.43 + 0.012*SL
	t_{PHL}	0.46	0.41 + 0.022*SL	0.42 + 0.019*SL	0.43 + 0.018*SL
	t_R	0.14	0.10 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.15	0.09 + 0.031*SL	0.09 + 0.032*SL	0.07 + 0.034*SL
S to YN	t_{PLH}	0.42	0.38 + 0.017*SL	0.39 + 0.013*SL	0.40 + 0.012*SL
	t_{PHL}	0.48	0.44 + 0.022*SL	0.45 + 0.019*SL	0.46 + 0.018*SL
	t_R	0.14	0.10 + 0.023*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.09 + 0.034*SL	0.09 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX2I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.32	0.20 + 0.062*SL	0.19 + 0.063*SL	0.19 + 0.063*SL
	t_{PHL}	0.33	0.19 + 0.074*SL	0.19 + 0.072*SL	0.20 + 0.072*SL
	t_R	0.59	0.33 + 0.131*SL	0.32 + 0.136*SL	0.29 + 0.139*SL
	t_F	0.52	0.24 + 0.137*SL	0.23 + 0.140*SL	0.22 + 0.142*SL
D1 to YN	t_{PLH}	0.38	0.25 + 0.066*SL	0.25 + 0.064*SL	0.26 + 0.063*SL
	t_{PHL}	0.54	0.39 + 0.075*SL	0.40 + 0.073*SL	0.40 + 0.072*SL
	t_R	0.55	0.29 + 0.130*SL	0.27 + 0.136*SL	0.25 + 0.139*SL
	t_F	0.74	0.46 + 0.140*SL	0.45 + 0.142*SL	0.45 + 0.142*SL
S to YN	t_{PLH}	0.38	0.25 + 0.064*SL	0.25 + 0.063*SL	0.26 + 0.063*SL
	t_{PHL}	0.51	0.36 + 0.074*SL	0.37 + 0.072*SL	0.37 + 0.071*SL
	t_R	0.59	0.32 + 0.134*SL	0.31 + 0.138*SL	0.30 + 0.139*SL
	t_F	0.47	0.19 + 0.138*SL	0.18 + 0.141*SL	0.18 + 0.142*SL

STDM80 MX2ID2

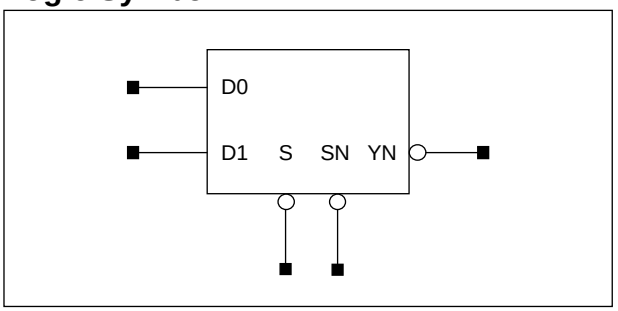
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.60	0.56 + 0.022*SL	0.57 + 0.018*SL	0.58 + 0.017*SL
	t_{PHL}	0.62	0.56 + 0.028*SL	0.58 + 0.024*SL	0.59 + 0.022*SL
	t_R	0.19	0.12 + 0.033*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.19	0.12 + 0.039*SL	0.12 + 0.038*SL	0.12 + 0.039*SL
D1 to YN	t_{PLH}	0.61	0.56 + 0.022*SL	0.57 + 0.018*SL	0.58 + 0.017*SL
	t_{PHL}	0.62	0.56 + 0.028*SL	0.57 + 0.024*SL	0.59 + 0.022*SL
	t_R	0.19	0.12 + 0.033*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.19	0.12 + 0.039*SL	0.12 + 0.038*SL	0.12 + 0.039*SL
S to YN	t_{PLH}	0.58	0.53 + 0.022*SL	0.54 + 0.018*SL	0.55 + 0.017*SL
	t_{PHL}	0.66	0.60 + 0.028*SL	0.61 + 0.024*SL	0.63 + 0.022*SL
	t_R	0.19	0.12 + 0.033*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.19	0.12 + 0.039*SL	0.12 + 0.038*SL	0.11 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

MX2IA/MX2ID2A

2 > 1 Inverting MUX with Separate S and SN Inputs, 1X/2X Drive

Logic Symbol



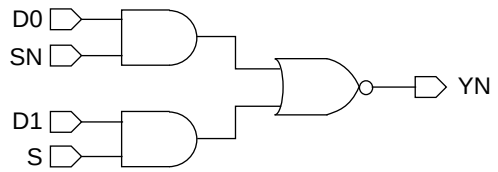
Truth Table

D0	D1	S	SN	YN
0	x	0	1	1
1	x	0	1	0
x	0	1	0	1
x	1	1	0	0

Cell Data

Input Load (SL)								Gate Count	
STD80									
MX2IA				*MX2ID2A*				*MX2IA*	*MX2ID2A*
D0	D1	S	SN	D0	D1	S	SN		
0.6	0.9	0.9	0.5	0.6	0.6	0.4	0.4	1.7	3.3
STDM80									
MX2IA				*MX2ID2A*				*MX2IA*	*MX2ID2A*
D0	D1	S	SN	D0	D1	S	SN		
0.8	0.9	0.8	0.9	0.7	0.7	0.8	0.6	1.7	3.3

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX2IA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.21	0.11 + 0.049*SL	0.13 + 0.041*SL	0.12 + 0.041*SL
	t_{PHL}	0.27	0.16 + 0.058*SL	0.16 + 0.054*SL	0.16 + 0.055*SL
	t_R	0.42	0.26 + 0.078*SL	0.24 + 0.088*SL	0.17 + 0.095*SL
	t_F	0.39	0.20 + 0.094*SL	0.17 + 0.105*SL	0.12 + 0.111*SL
D1 to YN	t_{PLH}	0.28	0.19 + 0.044*SL	0.20 + 0.041*SL	0.19 + 0.041*SL
	t_{PHL}	0.40	0.29 + 0.055*SL	0.29 + 0.055*SL	0.29 + 0.055*SL
	t_R	0.44	0.28 + 0.081*SL	0.26 + 0.090*SL	0.21 + 0.095*SL
	t_F	0.59	0.38 + 0.106*SL	0.38 + 0.108*SL	0.35 + 0.111*SL
S to YN	t_{PLH}	0.24	0.15 + 0.046*SL	0.16 + 0.041*SL	0.16 + 0.041*SL
	t_{PHL}	0.37	0.26 + 0.054*SL	0.26 + 0.055*SL	0.26 + 0.055*SL
	t_R	0.40	0.24 + 0.080*SL	0.22 + 0.089*SL	0.17 + 0.095*SL
	t_F	0.60	0.40 + 0.100*SL	0.38 + 0.106*SL	0.34 + 0.111*SL
SN to YN	t_{PLH}	0.24	0.15 + 0.046*SL	0.16 + 0.041*SL	0.16 + 0.041*SL
	t_{PHL}	0.37	0.26 + 0.054*SL	0.26 + 0.055*SL	0.26 + 0.055*SL
	t_R	0.40	0.24 + 0.080*SL	0.22 + 0.089*SL	0.17 + 0.095*SL
	t_F	0.60	0.40 + 0.100*SL	0.38 + 0.106*SL	0.34 + 0.111*SL

STD80 MX2ID2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.44	0.41 + 0.015*SL	0.42 + 0.013*SL	0.43 + 0.012*SL
	t_{PHL}	0.46	0.42 + 0.022*SL	0.42 + 0.019*SL	0.43 + 0.018*SL
	t_R	0.14	0.10 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.15	0.09 + 0.029*SL	0.09 + 0.032*SL	0.07 + 0.034*SL
D1 to YN	t_{PLH}	0.44	0.41 + 0.016*SL	0.42 + 0.013*SL	0.43 + 0.012*SL
	t_{PHL}	0.46	0.42 + 0.022*SL	0.42 + 0.019*SL	0.43 + 0.018*SL
	t_R	0.14	0.10 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.09 + 0.032*SL	0.09 + 0.031*SL	0.07 + 0.034*SL
S to YN	t_{PLH}	0.38	0.35 + 0.017*SL	0.36 + 0.013*SL	0.37 + 0.012*SL
	t_{PHL}	0.40	0.35 + 0.022*SL	0.36 + 0.019*SL	0.37 + 0.018*SL
	t_R	0.14	0.10 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.09 + 0.033*SL	0.09 + 0.031*SL	0.07 + 0.034*SL
SN to YN	t_{PLH}	0.38	0.35 + 0.017*SL	0.36 + 0.013*SL	0.37 + 0.012*SL
	t_{PHL}	0.40	0.35 + 0.022*SL	0.36 + 0.019*SL	0.37 + 0.018*SL
	t_R	0.14	0.10 + 0.020*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.16	0.09 + 0.033*SL	0.09 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX2IA

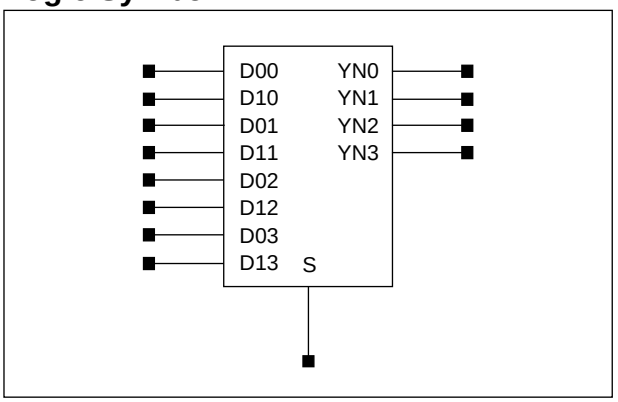
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.28	0.15 + 0.062*SL	0.15 + 0.063*SL	0.15 + 0.063*SL
	t_{PHL}	0.34	0.19 + 0.072*SL	0.19 + 0.072*SL	0.20 + 0.071*SL
	t_R	0.54	0.28 + 0.130*SL	0.26 + 0.135*SL	0.24 + 0.139*SL
	t_F	0.47	0.20 + 0.134*SL	0.19 + 0.140*SL	0.16 + 0.143*SL
D1 to YN	t_{PLH}	0.42	0.29 + 0.065*SL	0.30 + 0.063*SL	0.30 + 0.063*SL
	t_{PHL}	0.53	0.38 + 0.076*SL	0.39 + 0.073*SL	0.39 + 0.072*SL
	t_R	0.60	0.33 + 0.132*SL	0.32 + 0.137*SL	0.31 + 0.139*SL
	t_F	0.74	0.46 + 0.141*SL	0.45 + 0.142*SL	0.45 + 0.142*SL
S to YN	t_{PLH}	0.36	0.23 + 0.065*SL	0.24 + 0.063*SL	0.24 + 0.063*SL
	t_{PHL}	0.47	0.32 + 0.074*SL	0.33 + 0.073*SL	0.33 + 0.072*SL
	t_R	0.55	0.29 + 0.130*SL	0.27 + 0.136*SL	0.25 + 0.138*SL
	t_F	0.73	0.45 + 0.139*SL	0.44 + 0.142*SL	0.43 + 0.143*SL
SN to YN	t_{PLH}	0.36	0.23 + 0.065*SL	0.24 + 0.063*SL	0.24 + 0.063*SL
	t_{PHL}	0.47	0.32 + 0.074*SL	0.33 + 0.073*SL	0.33 + 0.072*SL
	t_R	0.55	0.29 + 0.130*SL	0.27 + 0.136*SL	0.25 + 0.138*SL
	t_F	0.73	0.45 + 0.139*SL	0.44 + 0.142*SL	0.43 + 0.143*SL

STDM80 MX2ID2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.61	0.56 + 0.022*SL	0.57 + 0.018*SL	0.58 + 0.017*SL
	t_{PHL}	0.62	0.56 + 0.028*SL	0.58 + 0.024*SL	0.59 + 0.022*SL
	t_R	0.19	0.12 + 0.032*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.19	0.12 + 0.039*SL	0.12 + 0.038*SL	0.12 + 0.039*SL
D1 to YN	t_{PLH}	0.61	0.56 + 0.022*SL	0.57 + 0.018*SL	0.58 + 0.017*SL
	t_{PHL}	0.62	0.56 + 0.028*SL	0.57 + 0.024*SL	0.59 + 0.022*SL
	t_R	0.19	0.12 + 0.032*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.19	0.12 + 0.039*SL	0.12 + 0.038*SL	0.12 + 0.039*SL
S to YN	t_{PLH}	0.52	0.47 + 0.022*SL	0.49 + 0.018*SL	0.50 + 0.017*SL
	t_{PHL}	0.54	0.49 + 0.028*SL	0.50 + 0.024*SL	0.51 + 0.022*SL
	t_R	0.19	0.12 + 0.032*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.20	0.11 + 0.041*SL	0.13 + 0.037*SL	0.12 + 0.039*SL
SN to YN	t_{PLH}	0.52	0.47 + 0.022*SL	0.49 + 0.018*SL	0.50 + 0.017*SL
	t_{PHL}	0.54	0.49 + 0.028*SL	0.50 + 0.024*SL	0.51 + 0.022*SL
	t_R	0.19	0.12 + 0.032*SL	0.12 + 0.033*SL	0.11 + 0.034*SL
	t_F	0.20	0.11 + 0.041*SL	0.13 + 0.037*SL	0.12 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



Truth Table

S	YN0	YN1	YN2	YN3
0	$\overline{D00}$	$\overline{D01}$	$\overline{D02}$	$\overline{D03}$
1	$\overline{D10}$	$\overline{D11}$	$\overline{D12}$	$\overline{D13}$

Cell Data

Input Load (SL)									Gate Count
STD80									
MX2IX4									*MX2IX4*
D00	D10	D01	D11	D02	D12	D03	D13	S	
0.9	0.8	0.9	0.8	0.9	0.8	0.9	0.8	3.5	7.3
STDM80									
MX2IX4									*MX2IX4*
D00	D10	D01	D11	D02	D12	D03	D13	S	
1.0	0.9	1.0	0.9	1.0	0.9	1.0	0.9	4.7	7.3

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX2IX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to YN0	t_{PLH}	0.19	0.11 + 0.039*SL	0.13 + 0.032*SL	0.13 + 0.032*SL
	t_{PHL}	0.25	0.14 + 0.056*SL	0.14 + 0.054*SL	0.13 + 0.055*SL
	t_R	0.36	0.25 + 0.056*SL	0.23 + 0.064*SL	0.15 + 0.072*SL
	t_F	0.38	0.19 + 0.097*SL	0.17 + 0.106*SL	0.13 + 0.111*SL
D10 to YN0	t_{PLH}	0.24	0.16 + 0.037*SL	0.18 + 0.032*SL	0.18 + 0.032*SL
	t_{PHL}	0.40	0.29 + 0.055*SL	0.29 + 0.055*SL	0.29 + 0.055*SL
	t_R	0.40	0.29 + 0.058*SL	0.27 + 0.066*SL	0.21 + 0.072*SL
	t_F	0.60	0.39 + 0.105*SL	0.38 + 0.108*SL	0.35 + 0.111*SL
S to YN0	t_{PLH}	0.42	0.33 + 0.044*SL	0.34 + 0.041*SL	0.34 + 0.041*SL
	t_{PHL}	0.55	0.43 + 0.059*SL	0.44 + 0.055*SL	0.44 + 0.055*SL
	t_R	0.42	0.24 + 0.086*SL	0.23 + 0.091*SL	0.19 + 0.095*SL
	t_F	0.39	0.19 + 0.102*SL	0.18 + 0.106*SL	0.14 + 0.110*SL
D01 to YN1	t_{PLH}	0.19	0.11 + 0.039*SL	0.13 + 0.032*SL	0.13 + 0.032*SL
	t_{PHL}	0.25	0.14 + 0.056*SL	0.14 + 0.054*SL	0.13 + 0.055*SL
	t_R	0.36	0.25 + 0.057*SL	0.23 + 0.063*SL	0.15 + 0.072*SL
	t_F	0.38	0.19 + 0.097*SL	0.17 + 0.106*SL	0.13 + 0.111*SL
D11 to YN1	t_{PLH}	0.24	0.16 + 0.037*SL	0.17 + 0.032*SL	0.18 + 0.032*SL
	t_{PHL}	0.40	0.29 + 0.056*SL	0.29 + 0.055*SL	0.29 + 0.055*SL
	t_R	0.40	0.29 + 0.060*SL	0.27 + 0.066*SL	0.21 + 0.072*SL
	t_F	0.60	0.39 + 0.105*SL	0.38 + 0.108*SL	0.35 + 0.111*SL
S to YN1	t_{PLH}	0.42	0.33 + 0.044*SL	0.34 + 0.041*SL	0.34 + 0.041*SL
	t_{PHL}	0.55	0.43 + 0.059*SL	0.44 + 0.055*SL	0.44 + 0.055*SL
	t_R	0.42	0.24 + 0.086*SL	0.23 + 0.091*SL	0.19 + 0.095*SL
	t_F	0.39	0.19 + 0.102*SL	0.18 + 0.106*SL	0.14 + 0.110*SL
D02 to YN2	t_{PLH}	0.19	0.11 + 0.039*SL	0.13 + 0.032*SL	0.13 + 0.032*SL
	t_{PHL}	0.25	0.14 + 0.056*SL	0.14 + 0.054*SL	0.13 + 0.055*SL
	t_R	0.36	0.25 + 0.057*SL	0.23 + 0.063*SL	0.15 + 0.072*SL
	t_F	0.38	0.19 + 0.097*SL	0.17 + 0.106*SL	0.13 + 0.111*SL
D12 to YN2	t_{PLH}	0.24	0.16 + 0.038*SL	0.18 + 0.032*SL	0.18 + 0.032*SL
	t_{PHL}	0.40	0.29 + 0.056*SL	0.29 + 0.055*SL	0.29 + 0.055*SL
	t_R	0.40	0.29 + 0.059*SL	0.27 + 0.066*SL	0.21 + 0.072*SL
	t_F	0.60	0.39 + 0.105*SL	0.38 + 0.108*SL	0.35 + 0.111*SL
S to YN2	t_{PLH}	0.42	0.33 + 0.044*SL	0.34 + 0.041*SL	0.34 + 0.041*SL
	t_{PHL}	0.55	0.43 + 0.059*SL	0.44 + 0.055*SL	0.44 + 0.055*SL
	t_R	0.42	0.24 + 0.086*SL	0.23 + 0.091*SL	0.19 + 0.095*SL
	t_F	0.39	0.19 + 0.102*SL	0.18 + 0.106*SL	0.14 + 0.110*SL
D03 to YN3	t_{PLH}	0.19	0.11 + 0.039*SL	0.13 + 0.032*SL	0.13 + 0.032*SL
	t_{PHL}	0.25	0.14 + 0.056*SL	0.14 + 0.054*SL	0.13 + 0.055*SL
	t_R	0.36	0.25 + 0.056*SL	0.23 + 0.064*SL	0.15 + 0.072*SL
	t_F	0.38	0.19 + 0.097*SL	0.17 + 0.106*SL	0.13 + 0.111*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX2IX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D13 to YN3	t_{PLH}	0.24	0.16 + 0.037*SL	0.18 + 0.032*SL	0.18 + 0.032*SL
	t_{PHL}	0.40	0.29 + 0.055*SL	0.29 + 0.055*SL	0.29 + 0.055*SL
	t_R	0.40	0.29 + 0.058*SL	0.27 + 0.066*SL	0.21 + 0.072*SL
	t_F	0.60	0.39 + 0.105*SL	0.38 + 0.108*SL	0.35 + 0.111*SL
S to YN3	t_{PLH}	0.42	0.33 + 0.044*SL	0.34 + 0.041*SL	0.34 + 0.041*SL
	t_{PHL}	0.55	0.43 + 0.059*SL	0.44 + 0.055*SL	0.44 + 0.055*SL
	t_R	0.42	0.24 + 0.086*SL	0.23 + 0.091*SL	0.19 + 0.095*SL
	t_F	0.39	0.19 + 0.102*SL	0.18 + 0.106*SL	0.14 + 0.110*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX2IX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to YN0	t_{PLH}	0.26	0.16 + 0.048*SL	0.16 + 0.047*SL	0.16 + 0.047*SL
	t_{PHL}	0.32	0.18 + 0.074*SL	0.18 + 0.072*SL	0.19 + 0.072*SL
	t_R	0.43	0.25 + 0.093*SL	0.23 + 0.099*SL	0.20 + 0.103*SL
	t_F	0.47	0.20 + 0.137*SL	0.19 + 0.141*SL	0.18 + 0.142*SL
D10 to YN0	t_{PLH}	0.35	0.25 + 0.050*SL	0.25 + 0.049*SL	0.26 + 0.048*SL
	t_{PHL}	0.53	0.38 + 0.076*SL	0.39 + 0.073*SL	0.39 + 0.072*SL
	t_R	0.52	0.32 + 0.097*SL	0.31 + 0.101*SL	0.29 + 0.104*SL
	t_F	0.74	0.46 + 0.140*SL	0.46 + 0.141*SL	0.45 + 0.142*SL
S to YN0	t_{PLH}	0.56	0.43 + 0.066*SL	0.44 + 0.063*SL	0.44 + 0.063*SL
	t_{PHL}	0.74	0.58 + 0.079*SL	0.60 + 0.072*SL	0.61 + 0.071*SL
	t_R	0.58	0.31 + 0.134*SL	0.31 + 0.136*SL	0.29 + 0.138*SL
	t_F	0.52	0.25 + 0.135*SL	0.25 + 0.137*SL	0.22 + 0.140*SL
D01 to YN1	t_{PLH}	0.26	0.16 + 0.048*SL	0.16 + 0.047*SL	0.16 + 0.047*SL
	t_{PHL}	0.32	0.18 + 0.074*SL	0.18 + 0.072*SL	0.19 + 0.072*SL
	t_R	0.43	0.25 + 0.093*SL	0.23 + 0.099*SL	0.20 + 0.103*SL
	t_F	0.47	0.20 + 0.137*SL	0.19 + 0.141*SL	0.18 + 0.142*SL
D11 to YN1	t_{PLH}	0.35	0.25 + 0.050*SL	0.25 + 0.048*SL	0.25 + 0.048*SL
	t_{PHL}	0.53	0.38 + 0.076*SL	0.39 + 0.073*SL	0.40 + 0.072*SL
	t_R	0.52	0.32 + 0.097*SL	0.31 + 0.101*SL	0.29 + 0.104*SL
	t_F	0.74	0.46 + 0.140*SL	0.46 + 0.141*SL	0.45 + 0.142*SL
S to YN1	t_{PLH}	0.56	0.43 + 0.066*SL	0.44 + 0.063*SL	0.44 + 0.063*SL
	t_{PHL}	0.74	0.58 + 0.078*SL	0.60 + 0.072*SL	0.61 + 0.071*SL
	t_R	0.58	0.31 + 0.134*SL	0.31 + 0.136*SL	0.29 + 0.138*SL
	t_F	0.52	0.25 + 0.135*SL	0.25 + 0.137*SL	0.22 + 0.140*SL
D02 to YN2	t_{PLH}	0.26	0.16 + 0.048*SL	0.16 + 0.047*SL	0.16 + 0.047*SL
	t_{PHL}	0.32	0.18 + 0.074*SL	0.18 + 0.072*SL	0.19 + 0.072*SL
	t_R	0.43	0.25 + 0.093*SL	0.23 + 0.099*SL	0.20 + 0.103*SL
	t_F	0.47	0.20 + 0.137*SL	0.19 + 0.141*SL	0.18 + 0.142*SL
D12 to YN2	t_{PLH}	0.35	0.25 + 0.050*SL	0.25 + 0.048*SL	0.25 + 0.048*SL
	t_{PHL}	0.53	0.38 + 0.076*SL	0.39 + 0.073*SL	0.40 + 0.072*SL
	t_R	0.52	0.32 + 0.097*SL	0.31 + 0.101*SL	0.29 + 0.104*SL
	t_F	0.74	0.46 + 0.140*SL	0.46 + 0.141*SL	0.45 + 0.142*SL
S to YN2	t_{PLH}	0.56	0.43 + 0.066*SL	0.44 + 0.063*SL	0.44 + 0.063*SL
	t_{PHL}	0.74	0.58 + 0.079*SL	0.60 + 0.072*SL	0.61 + 0.071*SL
	t_R	0.58	0.31 + 0.134*SL	0.31 + 0.136*SL	0.29 + 0.138*SL
	t_F	0.52	0.25 + 0.135*SL	0.25 + 0.137*SL	0.22 + 0.140*SL
D03 to YN3	t_{PLH}	0.26	0.16 + 0.048*SL	0.16 + 0.047*SL	0.16 + 0.047*SL
	t_{PHL}	0.32	0.18 + 0.074*SL	0.18 + 0.072*SL	0.19 + 0.072*SL
	t_R	0.43	0.25 + 0.093*SL	0.23 + 0.099*SL	0.20 + 0.103*SL
	t_F	0.47	0.20 + 0.137*SL	0.19 + 0.141*SL	0.18 + 0.142*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX2IX4

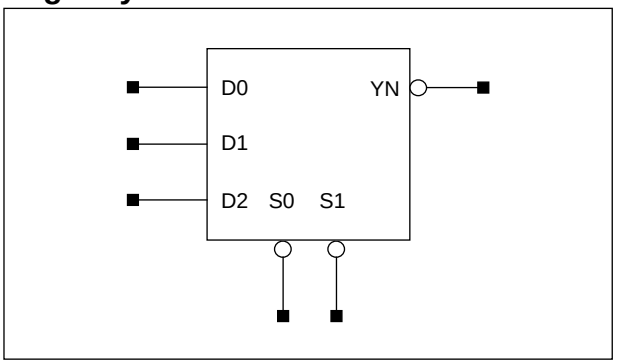
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D13 to YN3	t_{PLH}	0.35	0.25 + 0.050*SL	0.25 + 0.049*SL	0.26 + 0.048*SL
	t_{PHL}	0.53	0.38 + 0.076*SL	0.39 + 0.073*SL	0.39 + 0.072*SL
	t_R	0.52	0.32 + 0.097*SL	0.31 + 0.101*SL	0.29 + 0.104*SL
	t_F	0.74	0.46 + 0.140*SL	0.46 + 0.142*SL	0.45 + 0.142*SL
S to YN3	t_{PLH}	0.56	0.43 + 0.066*SL	0.44 + 0.063*SL	0.44 + 0.063*SL
	t_{PHL}	0.74	0.58 + 0.079*SL	0.60 + 0.072*SL	0.61 + 0.071*SL
	t_R	0.58	0.31 + 0.134*SL	0.31 + 0.136*SL	0.29 + 0.138*SL
	t_F	0.52	0.25 + 0.135*SL	0.25 + 0.137*SL	0.22 + 0.140*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

MX3I/MX3ID2

3 > 1 Inverting MUX with 1X/2X Drive

Logic Symbol



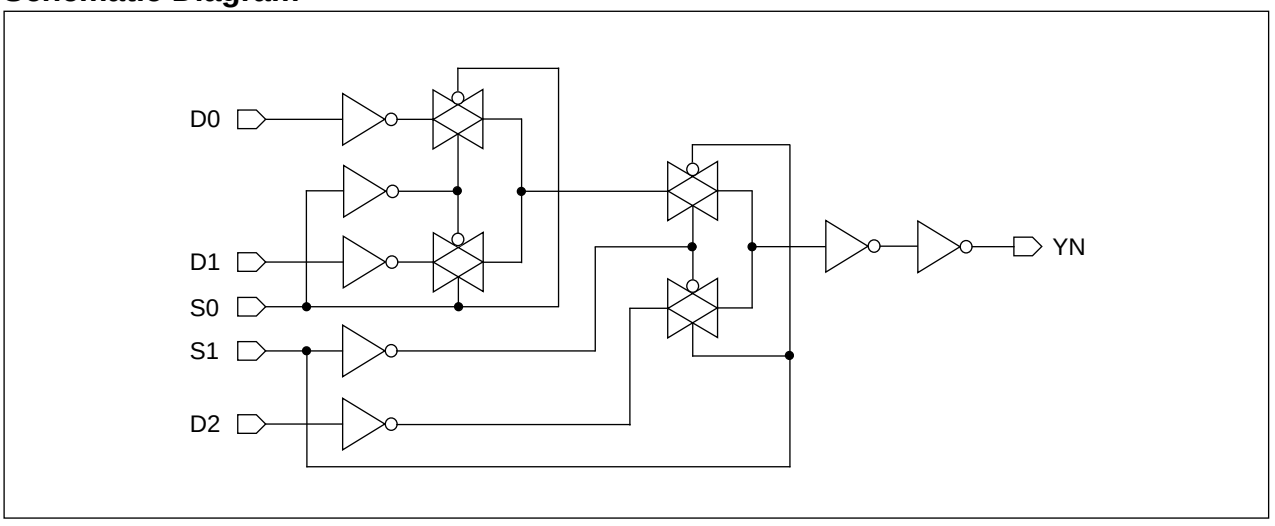
Truth Table

S0	S1	YN
0	0	$\overline{D0}$
1	0	$\overline{D1}$
x	1	$\overline{D2}$

Cell Data

Input Load (SL)										Gate Count	
STD80											
MX3I					*MX3ID2*					*MX3I*	*MX3ID2*
D0	D1	D2	S0	S1	D0	D1	D2	S0	S1		
0.7	0.6	0.6	1.0	1.0	0.7	0.6	0.7	1.0	1.0	5.3	5.7
STDM80											
MX3I					*MX3ID2*					*MX3I*	*MX3ID2*
D0	D1	D2	S0	S1	D0	D1	D2	S0	S1		
0.7	0.7	0.7	1.6	1.5	0.7	0.7	0.7	1.6	1.5	5.3	5.7

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX3I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.56	0.51 + 0.027*SL	0.52 + 0.024*SL	0.52 + 0.024*SL
	t_{PHL}	0.61	0.53 + 0.039*SL	0.54 + 0.037*SL	0.54 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.067*SL	0.07 + 0.069*SL
D1 to YN	t_{PLH}	0.57	0.51 + 0.026*SL	0.52 + 0.024*SL	0.52 + 0.024*SL
	t_{PHL}	0.61	0.53 + 0.039*SL	0.53 + 0.037*SL	0.54 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.22	0.09 + 0.064*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
D2 to YN	t_{PLH}	0.43	0.38 + 0.026*SL	0.38 + 0.024*SL	0.38 + 0.024*SL
	t_{PHL}	0.46	0.38 + 0.039*SL	0.38 + 0.037*SL	0.39 + 0.037*SL
	t_R	0.18	0.09 + 0.047*SL	0.09 + 0.050*SL	0.06 + 0.052*SL
	t_F	0.22	0.10 + 0.060*SL	0.08 + 0.068*SL	0.06 + 0.069*SL
S0 to YN	t_{PLH}	0.53	0.47 + 0.027*SL	0.48 + 0.024*SL	0.48 + 0.024*SL
	t_{PHL}	0.62	0.54 + 0.039*SL	0.54 + 0.037*SL	0.54 + 0.037*SL
	t_R	0.19	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.22	0.10 + 0.061*SL	0.08 + 0.067*SL	0.07 + 0.069*SL
S1 to YN	t_{PLH}	0.41	0.36 + 0.026*SL	0.36 + 0.024*SL	0.37 + 0.024*SL
	t_{PHL}	0.51	0.44 + 0.038*SL	0.44 + 0.037*SL	0.44 + 0.037*SL
	t_R	0.19	0.10 + 0.046*SL	0.09 + 0.049*SL	0.06 + 0.052*SL
	t_F	0.22	0.09 + 0.066*SL	0.09 + 0.067*SL	0.07 + 0.069*SL

STD80 MX3ID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.58	0.55 + 0.017*SL	0.56 + 0.013*SL	0.57 + 0.012*SL
	t_{PHL}	0.61	0.57 + 0.022*SL	0.58 + 0.019*SL	0.58 + 0.018*SL
	t_R	0.16	0.12 + 0.021*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D1 to YN	t_{PLH}	0.59	0.55 + 0.017*SL	0.56 + 0.013*SL	0.57 + 0.012*SL
	t_{PHL}	0.61	0.57 + 0.022*SL	0.57 + 0.019*SL	0.58 + 0.018*SL
	t_R	0.16	0.12 + 0.022*SL	0.12 + 0.022*SL	0.08 + 0.026*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
D2 to YN	t_{PLH}	0.44	0.41 + 0.016*SL	0.42 + 0.013*SL	0.43 + 0.012*SL
	t_{PHL}	0.46	0.41 + 0.022*SL	0.42 + 0.019*SL	0.43 + 0.018*SL
	t_R	0.14	0.10 + 0.021*SL	0.10 + 0.023*SL	0.07 + 0.026*SL
	t_F	0.15	0.10 + 0.029*SL	0.09 + 0.032*SL	0.07 + 0.034*SL
S0 to YN	t_{PLH}	0.55	0.51 + 0.017*SL	0.52 + 0.013*SL	0.53 + 0.012*SL
	t_{PHL}	0.62	0.58 + 0.022*SL	0.58 + 0.019*SL	0.59 + 0.018*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.022*SL	0.08 + 0.026*SL
	t_F	0.16	0.10 + 0.029*SL	0.10 + 0.031*SL	0.07 + 0.034*SL
S1 to YN	t_{PLH}	0.43	0.40 + 0.017*SL	0.40 + 0.013*SL	0.42 + 0.012*SL
	t_{PHL}	0.52	0.47 + 0.022*SL	0.48 + 0.019*SL	0.49 + 0.018*SL
	t_R	0.15	0.11 + 0.020*SL	0.11 + 0.023*SL	0.08 + 0.026*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.07 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX3I

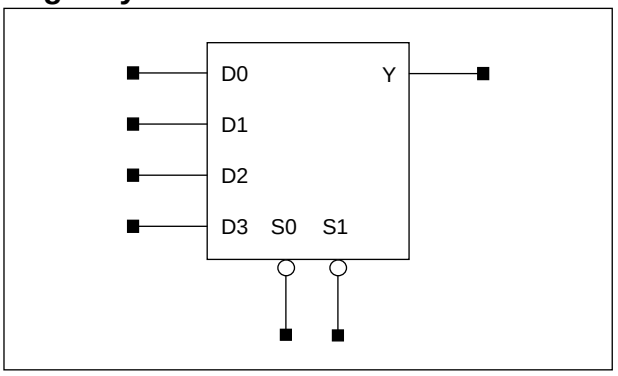
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.82	0.75 + 0.037*SL	0.76 + 0.034*SL	0.76 + 0.033*SL
	t_{PHL}	0.84	0.74 + 0.049*SL	0.75 + 0.045*SL	0.75 + 0.044*SL
	t_R	0.27	0.14 + 0.064*SL	0.13 + 0.069*SL	0.11 + 0.071*SL
	t_F	0.28	0.12 + 0.080*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
D1 to YN	t_{PLH}	0.83	0.75 + 0.037*SL	0.76 + 0.034*SL	0.77 + 0.033*SL
	t_{PHL}	0.83	0.73 + 0.049*SL	0.75 + 0.045*SL	0.75 + 0.044*SL
	t_R	0.27	0.15 + 0.063*SL	0.13 + 0.069*SL	0.11 + 0.071*SL
	t_F	0.28	0.12 + 0.081*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
D2 to YN	t_{PLH}	0.59	0.52 + 0.035*SL	0.53 + 0.034*SL	0.53 + 0.033*SL
	t_{PHL}	0.61	0.52 + 0.048*SL	0.53 + 0.045*SL	0.53 + 0.044*SL
	t_R	0.26	0.12 + 0.066*SL	0.11 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.080*SL	0.11 + 0.081*SL	0.10 + 0.083*SL
S0 to YN	t_{PLH}	0.78	0.71 + 0.037*SL	0.72 + 0.034*SL	0.72 + 0.033*SL
	t_{PHL}	0.86	0.76 + 0.049*SL	0.77 + 0.045*SL	0.78 + 0.044*SL
	t_R	0.27	0.14 + 0.064*SL	0.13 + 0.069*SL	0.11 + 0.071*SL
	t_F	0.28	0.12 + 0.080*SL	0.12 + 0.080*SL	0.11 + 0.082*SL
S1 to YN	t_{PLH}	0.57	0.49 + 0.036*SL	0.50 + 0.034*SL	0.50 + 0.033*SL
	t_{PHL}	0.69	0.60 + 0.048*SL	0.61 + 0.045*SL	0.61 + 0.044*SL
	t_R	0.26	0.13 + 0.067*SL	0.12 + 0.070*SL	0.10 + 0.072*SL
	t_F	0.28	0.12 + 0.079*SL	0.12 + 0.080*SL	0.11 + 0.082*SL

STDM80 MX3ID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.85	0.80 + 0.023*SL	0.82 + 0.019*SL	0.83 + 0.017*SL
	t_{PHL}	0.85	0.79 + 0.029*SL	0.80 + 0.024*SL	0.82 + 0.022*SL
	t_R	0.21	0.15 + 0.031*SL	0.15 + 0.032*SL	0.13 + 0.033*SL
	t_F	0.20	0.12 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D1 to YN	t_{PLH}	0.86	0.81 + 0.023*SL	0.82 + 0.019*SL	0.83 + 0.017*SL
	t_{PHL}	0.84	0.79 + 0.029*SL	0.80 + 0.024*SL	0.81 + 0.022*SL
	t_R	0.21	0.15 + 0.030*SL	0.15 + 0.032*SL	0.13 + 0.033*SL
	t_F	0.20	0.12 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
D2 to YN	t_{PLH}	0.61	0.56 + 0.022*SL	0.57 + 0.018*SL	0.59 + 0.017*SL
	t_{PHL}	0.62	0.56 + 0.029*SL	0.57 + 0.024*SL	0.59 + 0.022*SL
	t_R	0.19	0.12 + 0.032*SL	0.12 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.19	0.12 + 0.039*SL	0.12 + 0.038*SL	0.11 + 0.039*SL
S0 to YN	t_{PLH}	0.81	0.77 + 0.023*SL	0.78 + 0.019*SL	0.79 + 0.017*SL
	t_{PHL}	0.87	0.81 + 0.029*SL	0.83 + 0.024*SL	0.84 + 0.022*SL
	t_R	0.21	0.15 + 0.031*SL	0.14 + 0.032*SL	0.13 + 0.034*SL
	t_F	0.20	0.12 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
S1 to YN	t_{PLH}	0.59	0.54 + 0.023*SL	0.55 + 0.019*SL	0.56 + 0.017*SL
	t_{PHL}	0.71	0.65 + 0.029*SL	0.66 + 0.024*SL	0.68 + 0.022*SL
	t_R	0.20	0.14 + 0.030*SL	0.13 + 0.033*SL	0.12 + 0.034*SL
	t_F	0.20	0.12 + 0.039*SL	0.13 + 0.038*SL	0.12 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



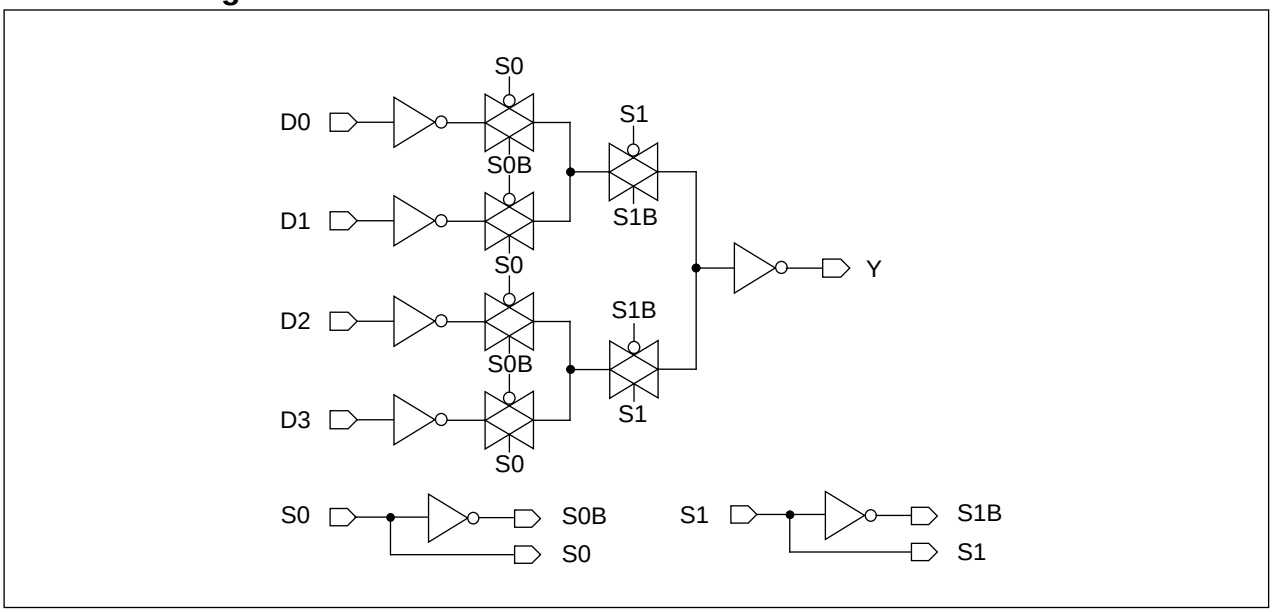
Truth Table

S0	S1	Y
0	0	D0
1	0	D1
0	1	D2
1	1	D3

Cell Data

Input Load (SL)												Gate Count	
STD80													
MX4						*MX4D2*						*MX4*	*MX4D2*
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1		
0.7	0.6	0.7	0.7	1.2	1.3	0.7	0.6	0.7	0.7	1.2	1.3	6.3	6.7
STDM80													
MX4						*MX4D2*						*MX4*	*MX4D2*
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1		
0.7	0.7	0.7	0.7	2.5	1.5	0.7	0.7	0.7	0.7	2.5	1.5	6.3	6.7

Schematic Diagram



Switching Characteristics

(Typical process, 25 °C, 5 V, t_R/t_F = 0.44 ns, SL: Standard Load)

STD80 MX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.46	0.39 + 0.036*SL	0.41 + 0.027*SL	0.44 + 0.024*SL
	t_{PHL}	0.59	0.48 + 0.050*SL	0.50 + 0.041*SL	0.55 + 0.037*SL
	t_R	0.27	0.17 + 0.048*SL	0.17 + 0.047*SL	0.13 + 0.051*SL
	t_F	0.34	0.20 + 0.066*SL	0.21 + 0.064*SL	0.17 + 0.069*SL
D1 to Y	t_{PLH}	0.46	0.38 + 0.037*SL	0.41 + 0.027*SL	0.44 + 0.024*SL
	t_{PHL}	0.59	0.49 + 0.050*SL	0.51 + 0.041*SL	0.55 + 0.037*SL
	t_R	0.27	0.18 + 0.045*SL	0.17 + 0.047*SL	0.13 + 0.051*SL
	t_F	0.34	0.20 + 0.066*SL	0.21 + 0.065*SL	0.17 + 0.068*SL
D2 to Y	t_{PLH}	0.46	0.38 + 0.036*SL	0.40 + 0.027*SL	0.44 + 0.024*SL
	t_{PHL}	0.59	0.48 + 0.050*SL	0.50 + 0.041*SL	0.55 + 0.037*SL
	t_R	0.27	0.17 + 0.046*SL	0.17 + 0.047*SL	0.13 + 0.051*SL
	t_F	0.33	0.20 + 0.065*SL	0.21 + 0.065*SL	0.17 + 0.069*SL
D3 to Y	t_{PLH}	0.45	0.38 + 0.036*SL	0.40 + 0.027*SL	0.44 + 0.024*SL
	t_{PHL}	0.59	0.49 + 0.050*SL	0.51 + 0.041*SL	0.55 + 0.037*SL
	t_R	0.27	0.17 + 0.047*SL	0.17 + 0.047*SL	0.13 + 0.051*SL
	t_F	0.34	0.21 + 0.065*SL	0.21 + 0.065*SL	0.17 + 0.069*SL
S0 to Y	t_{PLH}	0.50	0.42 + 0.037*SL	0.44 + 0.027*SL	0.48 + 0.024*SL
	t_{PHL}	0.57	0.47 + 0.050*SL	0.49 + 0.041*SL	0.54 + 0.037*SL
	t_R	0.27	0.17 + 0.046*SL	0.17 + 0.047*SL	0.13 + 0.051*SL
	t_F	0.33	0.20 + 0.065*SL	0.20 + 0.065*SL	0.17 + 0.069*SL
S1 to Y	t_{PLH}	0.36	0.29 + 0.034*SL	0.31 + 0.027*SL	0.34 + 0.024*SL
	t_{PHL}	0.44	0.34 + 0.050*SL	0.36 + 0.042*SL	0.40 + 0.037*SL
	t_R	0.24	0.14 + 0.048*SL	0.14 + 0.050*SL	0.12 + 0.052*SL
	t_F	0.30	0.17 + 0.069*SL	0.17 + 0.067*SL	0.15 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.47	0.42 + 0.025*SL	0.44 + 0.017*SL	0.49 + 0.012*SL
	t_{PHL}	0.59	0.53 + 0.031*SL	0.54 + 0.024*SL	0.60 + 0.018*SL
	t_R	0.24	0.19 + 0.026*SL	0.19 + 0.024*SL	0.18 + 0.025*SL
	t_F	0.30	0.22 + 0.038*SL	0.23 + 0.032*SL	0.22 + 0.033*SL
D1 to Y	t_{PLH}	0.47	0.42 + 0.024*SL	0.43 + 0.017*SL	0.49 + 0.012*SL
	t_{PHL}	0.59	0.53 + 0.032*SL	0.55 + 0.024*SL	0.60 + 0.018*SL
	t_R	0.24	0.19 + 0.026*SL	0.19 + 0.024*SL	0.17 + 0.025*SL
	t_F	0.30	0.22 + 0.037*SL	0.23 + 0.032*SL	0.22 + 0.033*SL
D2 to Y	t_{PLH}	0.46	0.42 + 0.024*SL	0.43 + 0.017*SL	0.48 + 0.012*SL
	t_{PHL}	0.59	0.53 + 0.032*SL	0.54 + 0.024*SL	0.60 + 0.018*SL
	t_R	0.24	0.18 + 0.027*SL	0.19 + 0.023*SL	0.17 + 0.025*SL
	t_F	0.30	0.22 + 0.039*SL	0.23 + 0.032*SL	0.22 + 0.033*SL
D3 to Y	t_{PLH}	0.46	0.41 + 0.024*SL	0.43 + 0.017*SL	0.48 + 0.012*SL
	t_{PHL}	0.59	0.53 + 0.031*SL	0.54 + 0.024*SL	0.60 + 0.018*SL
	t_R	0.24	0.18 + 0.028*SL	0.19 + 0.024*SL	0.17 + 0.025*SL
	t_F	0.30	0.22 + 0.038*SL	0.23 + 0.032*SL	0.22 + 0.033*SL
S0 to Y	t_{PLH}	0.50	0.45 + 0.025*SL	0.47 + 0.017*SL	0.52 + 0.012*SL
	t_{PHL}	0.57	0.51 + 0.031*SL	0.53 + 0.024*SL	0.58 + 0.018*SL
	t_R	0.24	0.19 + 0.025*SL	0.20 + 0.023*SL	0.17 + 0.025*SL
	t_F	0.29	0.22 + 0.037*SL	0.23 + 0.032*SL	0.22 + 0.033*SL
S1 to Y	t_{PLH}	0.37	0.32 + 0.023*SL	0.33 + 0.017*SL	0.38 + 0.012*SL
	t_{PHL}	0.44	0.37 + 0.032*SL	0.39 + 0.024*SL	0.45 + 0.018*SL
	t_R	0.21	0.16 + 0.028*SL	0.16 + 0.025*SL	0.16 + 0.026*SL
	t_F	0.27	0.19 + 0.039*SL	0.20 + 0.033*SL	0.20 + 0.033*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.65	0.55 + 0.047*SL	0.57 + 0.040*SL	0.61 + 0.035*SL
	t_{PHL}	0.84	0.70 + 0.068*SL	0.74 + 0.056*SL	0.78 + 0.050*SL
	t_R	0.35	0.21 + 0.071*SL	0.21 + 0.068*SL	0.21 + 0.069*SL
	t_F	0.46	0.28 + 0.087*SL	0.30 + 0.080*SL	0.31 + 0.079*SL
D1 to Y	t_{PLH}	0.64	0.55 + 0.047*SL	0.57 + 0.039*SL	0.60 + 0.035*SL
	t_{PHL}	0.84	0.71 + 0.067*SL	0.74 + 0.056*SL	0.79 + 0.050*SL
	t_R	0.35	0.21 + 0.070*SL	0.22 + 0.068*SL	0.21 + 0.069*SL
	t_F	0.46	0.29 + 0.086*SL	0.30 + 0.080*SL	0.31 + 0.079*SL
D2 to Y	t_{PLH}	0.64	0.55 + 0.047*SL	0.57 + 0.040*SL	0.60 + 0.035*SL
	t_{PHL}	0.84	0.71 + 0.067*SL	0.74 + 0.056*SL	0.78 + 0.050*SL
	t_R	0.35	0.21 + 0.070*SL	0.22 + 0.068*SL	0.21 + 0.069*SL
	t_F	0.45	0.28 + 0.086*SL	0.30 + 0.080*SL	0.31 + 0.079*SL
D3 to Y	t_{PLH}	0.64	0.54 + 0.047*SL	0.57 + 0.039*SL	0.59 + 0.035*SL
	t_{PHL}	0.84	0.71 + 0.067*SL	0.74 + 0.056*SL	0.79 + 0.050*SL
	t_R	0.35	0.21 + 0.070*SL	0.21 + 0.068*SL	0.21 + 0.069*SL
	t_F	0.46	0.28 + 0.087*SL	0.30 + 0.080*SL	0.31 + 0.079*SL
S0 to Y	t_{PLH}	0.71	0.61 + 0.047*SL	0.64 + 0.040*SL	0.67 + 0.035*SL
	t_{PHL}	0.84	0.70 + 0.067*SL	0.74 + 0.056*SL	0.78 + 0.050*SL
	t_R	0.35	0.21 + 0.070*SL	0.22 + 0.068*SL	0.21 + 0.069*SL
	t_F	0.46	0.29 + 0.085*SL	0.30 + 0.080*SL	0.31 + 0.079*SL
S1 to Y	t_{PLH}	0.50	0.41 + 0.046*SL	0.43 + 0.039*SL	0.45 + 0.035*SL
	t_{PHL}	0.61	0.47 + 0.067*SL	0.51 + 0.056*SL	0.55 + 0.049*SL
	t_R	0.33	0.19 + 0.073*SL	0.20 + 0.069*SL	0.19 + 0.070*SL
	t_F	0.42	0.23 + 0.091*SL	0.26 + 0.082*SL	0.27 + 0.080*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX4D2

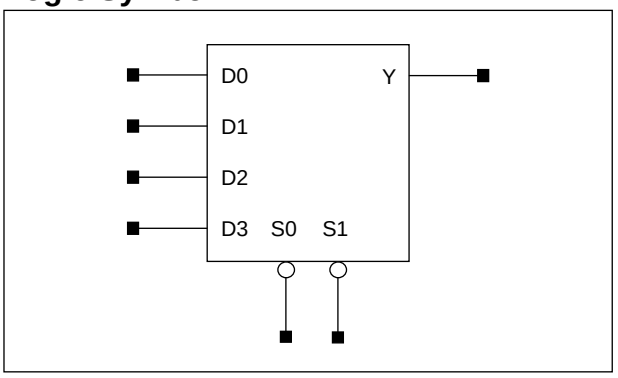
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.66	0.60 + 0.031*SL	0.62 + 0.025*SL	0.65 + 0.021*SL
	t_{PHL}	0.86	0.77 + 0.043*SL	0.80 + 0.035*SL	0.83 + 0.029*SL
	t_R	0.29	0.22 + 0.036*SL	0.22 + 0.035*SL	0.23 + 0.035*SL
	t_F	0.40	0.30 + 0.048*SL	0.32 + 0.042*SL	0.34 + 0.039*SL
D1 to Y	t_{PLH}	0.66	0.60 + 0.031*SL	0.62 + 0.025*SL	0.64 + 0.021*SL
	t_{PHL}	0.86	0.78 + 0.043*SL	0.80 + 0.035*SL	0.84 + 0.029*SL
	t_R	0.29	0.22 + 0.035*SL	0.22 + 0.036*SL	0.23 + 0.034*SL
	t_F	0.40	0.31 + 0.048*SL	0.32 + 0.042*SL	0.35 + 0.039*SL
D2 to Y	t_{PLH}	0.65	0.59 + 0.031*SL	0.61 + 0.025*SL	0.64 + 0.021*SL
	t_{PHL}	0.85	0.77 + 0.043*SL	0.79 + 0.034*SL	0.83 + 0.029*SL
	t_R	0.29	0.22 + 0.036*SL	0.22 + 0.036*SL	0.23 + 0.034*SL
	t_F	0.40	0.30 + 0.048*SL	0.32 + 0.042*SL	0.34 + 0.040*SL
D3 to Y	t_{PLH}	0.65	0.59 + 0.031*SL	0.61 + 0.025*SL	0.63 + 0.021*SL
	t_{PHL}	0.86	0.77 + 0.043*SL	0.80 + 0.034*SL	0.83 + 0.029*SL
	t_R	0.29	0.22 + 0.036*SL	0.22 + 0.035*SL	0.23 + 0.034*SL
	t_F	0.40	0.31 + 0.047*SL	0.32 + 0.042*SL	0.34 + 0.039*SL
S0 to Y	t_{PLH}	0.72	0.66 + 0.031*SL	0.68 + 0.025*SL	0.70 + 0.021*SL
	t_{PHL}	0.86	0.77 + 0.043*SL	0.80 + 0.035*SL	0.84 + 0.029*SL
	t_R	0.30	0.22 + 0.036*SL	0.23 + 0.035*SL	0.23 + 0.034*SL
	t_F	0.40	0.30 + 0.048*SL	0.32 + 0.042*SL	0.34 + 0.040*SL
S1 to Y	t_{PLH}	0.51	0.45 + 0.031*SL	0.47 + 0.024*SL	0.49 + 0.021*SL
	t_{PHL}	0.63	0.54 + 0.043*SL	0.56 + 0.035*SL	0.60 + 0.029*SL
	t_R	0.27	0.20 + 0.037*SL	0.20 + 0.037*SL	0.22 + 0.035*SL
	t_F	0.37	0.28 + 0.048*SL	0.29 + 0.044*SL	0.31 + 0.040*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

YMX4/YMX4D2

Fast 4 > 1 Non-Inverting MUX with 1X/2X Drive

Logic Symbol



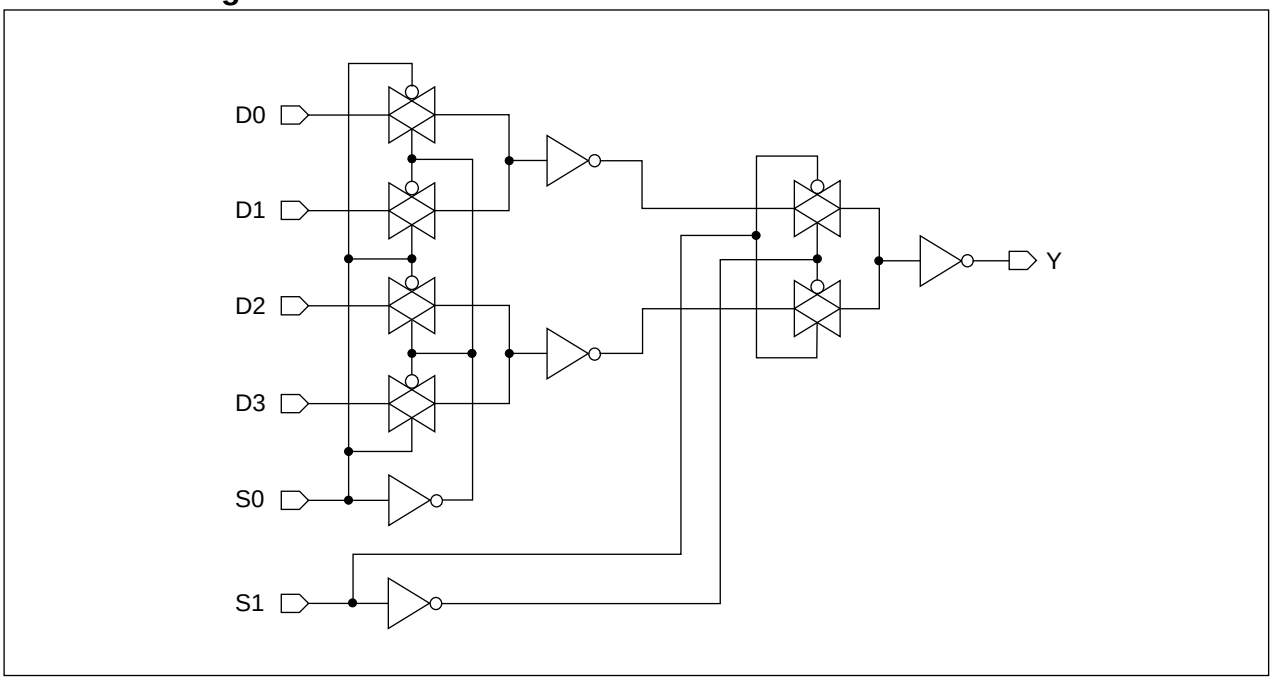
Truth Table

S0	S1	Y
0	0	D0
1	0	D1
0	1	D2
1	1	D3

Cell Data

Input Load (SL)												Gate Count	
STD80													
YMX4						*YMX4D2*						*YMX4*	*YMX4D2*
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1		
1.9	1.9	1.8	1.9	1.5	1.3	1.9	1.9	1.8	1.9	1.5	1.3	5.7	6.0
STDM80													
YMX4						*YMX4D2*						*YMX4*	*YMX4D2*
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1		
0.5	2.1	0.5	2.1	1.5	1.2	0.5	2.1	0.5	2.1	1.5	1.2	5.7	6.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 YMX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.38	0.33 + 0.029*SL	0.34 + 0.025*SL	0.35 + 0.024*SL
	t_{PHL}	0.49	0.40 + 0.044*SL	0.41 + 0.039*SL	0.43 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.15 + 0.064*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
D1 to Y	t_{PLH}	0.39	0.32 + 0.032*SL	0.34 + 0.025*SL	0.35 + 0.024*SL
	t_{PHL}	0.49	0.40 + 0.044*SL	0.41 + 0.039*SL	0.43 + 0.037*SL
	t_R	0.22	0.12 + 0.047*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.15 + 0.064*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
D2 to Y	t_{PLH}	0.38	0.32 + 0.030*SL	0.33 + 0.025*SL	0.34 + 0.024*SL
	t_{PHL}	0.49	0.40 + 0.044*SL	0.41 + 0.039*SL	0.43 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.15 + 0.063*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
D3 to Y	t_{PLH}	0.38	0.32 + 0.030*SL	0.34 + 0.025*SL	0.34 + 0.024*SL
	t_{PHL}	0.49	0.40 + 0.044*SL	0.41 + 0.039*SL	0.43 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.15 + 0.063*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
S0 to Y	t_{PLH}	0.50	0.44 + 0.029*SL	0.45 + 0.025*SL	0.46 + 0.024*SL
	t_{PHL}	0.46	0.37 + 0.044*SL	0.38 + 0.039*SL	0.40 + 0.037*SL
	t_R	0.21	0.12 + 0.047*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.27	0.14 + 0.065*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
S1 to Y	t_{PLH}	0.32	0.27 + 0.029*SL	0.28 + 0.025*SL	0.29 + 0.024*SL
	t_{PHL}	0.40	0.31 + 0.044*SL	0.32 + 0.039*SL	0.34 + 0.037*SL
	t_R	0.20	0.11 + 0.046*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.066*SL	0.10 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 YMX4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.40	0.36 + 0.020*SL	0.37 + 0.015*SL	0.40 + 0.012*SL
	t_{PHL}	0.50	0.44 + 0.028*SL	0.45 + 0.022*SL	0.49 + 0.018*SL
	t_R	0.18	0.14 + 0.023*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.23	0.17 + 0.032*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
D1 to Y	t_{PLH}	0.40	0.36 + 0.019*SL	0.37 + 0.015*SL	0.40 + 0.012*SL
	t_{PHL}	0.49	0.44 + 0.027*SL	0.45 + 0.022*SL	0.49 + 0.018*SL
	t_R	0.18	0.14 + 0.022*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.23	0.17 + 0.032*SL	0.17 + 0.031*SL	0.14 + 0.033*SL
D2 to Y	t_{PLH}	0.39	0.35 + 0.019*SL	0.36 + 0.015*SL	0.39 + 0.012*SL
	t_{PHL}	0.49	0.44 + 0.027*SL	0.45 + 0.022*SL	0.48 + 0.018*SL
	t_R	0.18	0.14 + 0.022*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.23	0.16 + 0.033*SL	0.17 + 0.031*SL	0.14 + 0.033*SL
D3 to Y	t_{PLH}	0.39	0.36 + 0.019*SL	0.37 + 0.015*SL	0.39 + 0.012*SL
	t_{PHL}	0.49	0.44 + 0.028*SL	0.45 + 0.021*SL	0.48 + 0.018*SL
	t_R	0.18	0.14 + 0.023*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.23	0.16 + 0.034*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
S0 to Y	t_{PLH}	0.51	0.47 + 0.019*SL	0.48 + 0.015*SL	0.50 + 0.012*SL
	t_{PHL}	0.47	0.41 + 0.028*SL	0.42 + 0.022*SL	0.46 + 0.018*SL
	t_R	0.18	0.13 + 0.023*SL	0.13 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.23	0.16 + 0.033*SL	0.17 + 0.031*SL	0.14 + 0.033*SL
S1 to Y	t_{PLH}	0.33	0.29 + 0.019*SL	0.30 + 0.015*SL	0.33 + 0.012*SL
	t_{PHL}	0.40	0.34 + 0.027*SL	0.36 + 0.022*SL	0.39 + 0.018*SL
	t_R	0.17	0.12 + 0.024*SL	0.12 + 0.024*SL	0.10 + 0.026*SL
	t_F	0.22	0.15 + 0.034*SL	0.16 + 0.032*SL	0.14 + 0.033*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 YMX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.55	0.47 + 0.040*SL	0.48 + 0.035*SL	0.50 + 0.033*SL
	t_{PHL}	0.69	0.57 + 0.058*SL	0.60 + 0.049*SL	0.63 + 0.046*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.36	0.21 + 0.079*SL	0.21 + 0.079*SL	0.20 + 0.079*SL
D1 to Y	t_{PLH}	0.56	0.47 + 0.041*SL	0.49 + 0.035*SL	0.50 + 0.034*SL
	t_{PHL}	0.68	0.57 + 0.058*SL	0.59 + 0.049*SL	0.62 + 0.046*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.36	0.20 + 0.079*SL	0.21 + 0.079*SL	0.20 + 0.079*SL
D2 to Y	t_{PLH}	0.54	0.46 + 0.040*SL	0.47 + 0.035*SL	0.49 + 0.034*SL
	t_{PHL}	0.69	0.57 + 0.058*SL	0.60 + 0.049*SL	0.62 + 0.046*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.36	0.20 + 0.081*SL	0.21 + 0.078*SL	0.20 + 0.080*SL
D3 to Y	t_{PLH}	0.55	0.47 + 0.040*SL	0.48 + 0.035*SL	0.49 + 0.034*SL
	t_{PHL}	0.68	0.57 + 0.058*SL	0.59 + 0.049*SL	0.62 + 0.046*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.36	0.20 + 0.081*SL	0.21 + 0.078*SL	0.20 + 0.080*SL
S0 to Y	t_{PLH}	0.69	0.61 + 0.041*SL	0.62 + 0.035*SL	0.64 + 0.034*SL
	t_{PHL}	0.90	0.78 + 0.059*SL	0.81 + 0.049*SL	0.83 + 0.046*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.36	0.20 + 0.081*SL	0.20 + 0.079*SL	0.20 + 0.080*SL
S1 to Y	t_{PLH}	0.44	0.36 + 0.040*SL	0.38 + 0.035*SL	0.39 + 0.033*SL
	t_{PHL}	0.54	0.43 + 0.058*SL	0.46 + 0.049*SL	0.48 + 0.046*SL
	t_R	0.29	0.15 + 0.069*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.35	0.18 + 0.083*SL	0.20 + 0.079*SL	0.19 + 0.080*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

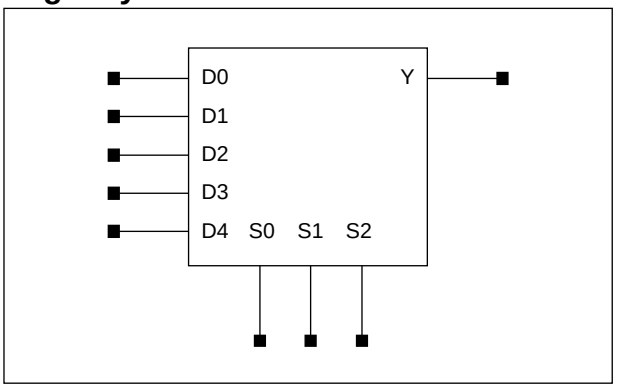
(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 YMX4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.56	0.51 + 0.026*SL	0.52 + 0.021*SL	0.54 + 0.019*SL
	t_{PHL}	0.70	0.63 + 0.037*SL	0.65 + 0.031*SL	0.68 + 0.026*SL
	t_R	0.23	0.16 + 0.034*SL	0.16 + 0.034*SL	0.16 + 0.034*SL
	t_F	0.31	0.22 + 0.043*SL	0.23 + 0.040*SL	0.24 + 0.038*SL
D1 to Y	t_{PLH}	0.57	0.51 + 0.026*SL	0.53 + 0.021*SL	0.55 + 0.019*SL
	t_{PHL}	0.70	0.62 + 0.037*SL	0.64 + 0.030*SL	0.67 + 0.026*SL
	t_R	0.23	0.15 + 0.035*SL	0.16 + 0.034*SL	0.16 + 0.034*SL
	t_F	0.31	0.22 + 0.043*SL	0.23 + 0.040*SL	0.25 + 0.038*SL
D2 to Y	t_{PLH}	0.55	0.50 + 0.025*SL	0.51 + 0.021*SL	0.53 + 0.019*SL
	t_{PHL}	0.70	0.62 + 0.037*SL	0.64 + 0.031*SL	0.68 + 0.026*SL
	t_R	0.22	0.15 + 0.035*SL	0.15 + 0.035*SL	0.16 + 0.034*SL
	t_F	0.31	0.22 + 0.044*SL	0.23 + 0.040*SL	0.25 + 0.038*SL
D3 to Y	t_{PLH}	0.56	0.50 + 0.026*SL	0.52 + 0.021*SL	0.54 + 0.019*SL
	t_{PHL}	0.70	0.62 + 0.037*SL	0.64 + 0.030*SL	0.67 + 0.026*SL
	t_R	0.22	0.15 + 0.036*SL	0.16 + 0.034*SL	0.16 + 0.034*SL
	t_F	0.31	0.22 + 0.043*SL	0.23 + 0.040*SL	0.24 + 0.038*SL
S0 to Y	t_{PLH}	0.70	0.65 + 0.025*SL	0.66 + 0.021*SL	0.68 + 0.019*SL
	t_{PHL}	0.91	0.83 + 0.037*SL	0.86 + 0.030*SL	0.89 + 0.026*SL
	t_R	0.22	0.15 + 0.036*SL	0.16 + 0.034*SL	0.16 + 0.034*SL
	t_F	0.30	0.22 + 0.044*SL	0.23 + 0.040*SL	0.24 + 0.038*SL
S1 to Y	t_{PLH}	0.45	0.39 + 0.026*SL	0.41 + 0.021*SL	0.43 + 0.019*SL
	t_{PHL}	0.56	0.48 + 0.037*SL	0.50 + 0.031*SL	0.53 + 0.026*SL
	t_R	0.22	0.15 + 0.035*SL	0.15 + 0.035*SL	0.16 + 0.034*SL
	t_F	0.29	0.20 + 0.045*SL	0.22 + 0.040*SL	0.23 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Logic Symbol



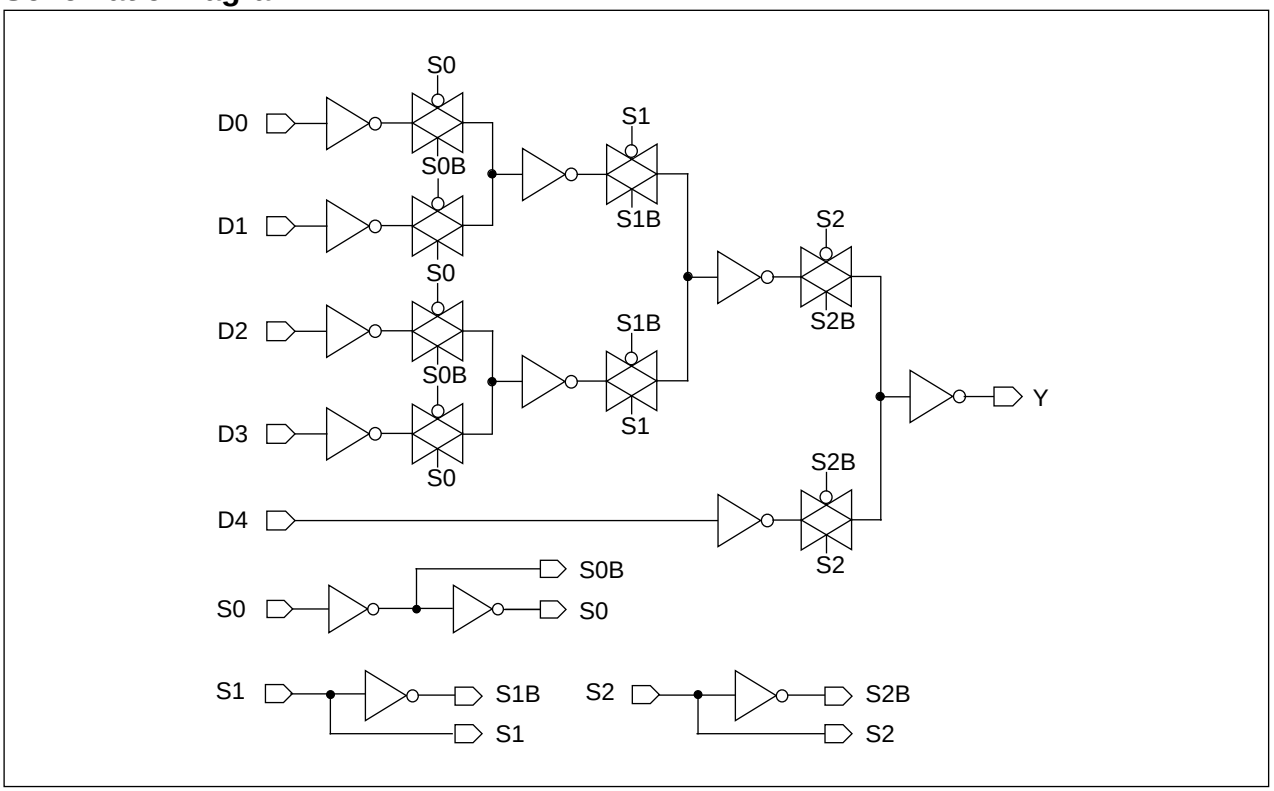
Truth Table

S0	S1	S2	Y
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
x	x	1	D4

Cell Data

Input Load (SL)																Gate Count	
STD80																	
MX5								*MX5D2*								*MX5*	*MX5D2*
D0	D1	D2	D3	D4	S0	S1	S2	D0	D1	D2	D3	D4	S0	S1	S2		
0.6	0.6	0.6	0.7	0.7	0.6	1.1	1.0	0.6	0.6	0.6	0.7	0.7	0.6	1.1	1.0	9.3	9.7
STDM80																	
MX5								*MX5D2*								*MX5*	*MX5D2*
D0	D1	D2	D3	D4	S0	S1	S2	D0	D1	D2	D3	D4	S0	S1	S2		
0.8	0.7	0.7	0.7	0.8	0.8	1.5	1.5	0.8	0.7	0.7	0.7	0.8	0.8	1.5	1.5	9.3	9.7

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.74	0.68 + 0.031*SL	0.69 + 0.025*SL	0.70 + 0.024*SL
	t_{PHL}	0.85	0.76 + 0.044*SL	0.77 + 0.039*SL	0.79 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.14 + 0.063*SL	0.13 + 0.065*SL	0.10 + 0.069*SL
D1 to Y	t_{PLH}	0.74	0.68 + 0.030*SL	0.69 + 0.025*SL	0.70 + 0.024*SL
	t_{PHL}	0.85	0.76 + 0.044*SL	0.77 + 0.039*SL	0.79 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.14 + 0.063*SL	0.13 + 0.065*SL	0.10 + 0.069*SL
D2 to Y	t_{PLH}	0.71	0.65 + 0.031*SL	0.66 + 0.025*SL	0.68 + 0.024*SL
	t_{PHL}	0.81	0.73 + 0.044*SL	0.74 + 0.039*SL	0.75 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.14 + 0.065*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
D3 to Y	t_{PLH}	0.71	0.65 + 0.031*SL	0.66 + 0.025*SL	0.68 + 0.024*SL
	t_{PHL}	0.81	0.73 + 0.044*SL	0.74 + 0.039*SL	0.75 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.14 + 0.065*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
D4 to Y	t_{PLH}	0.31	0.25 + 0.030*SL	0.27 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.42	0.34 + 0.044*SL	0.35 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.064*SL	0.13 + 0.065*SL	0.09 + 0.069*SL
S0 to Y	t_{PLH}	0.86	0.80 + 0.030*SL	0.81 + 0.025*SL	0.83 + 0.024*SL
	t_{PHL}	0.91	0.82 + 0.044*SL	0.83 + 0.039*SL	0.85 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.26	0.14 + 0.064*SL	0.13 + 0.065*SL	0.10 + 0.069*SL
S1 to Y	t_{PLH}	0.51	0.45 + 0.031*SL	0.47 + 0.025*SL	0.48 + 0.024*SL
	t_{PHL}	0.54	0.45 + 0.044*SL	0.46 + 0.039*SL	0.48 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.14 + 0.063*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
S2 to Y	t_{PLH}	0.34	0.28 + 0.028*SL	0.29 + 0.025*SL	0.30 + 0.024*SL
	t_{PHL}	0.39	0.31 + 0.044*SL	0.32 + 0.039*SL	0.33 + 0.037*SL
	t_R	0.21	0.11 + 0.047*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.25	0.12 + 0.066*SL	0.12 + 0.066*SL	0.09 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.75	0.71 + 0.020*SL	0.72 + 0.015*SL	0.75 + 0.012*SL
	t_{PHL}	0.85	0.80 + 0.027*SL	0.81 + 0.021*SL	0.84 + 0.018*SL
	t_R	0.19	0.14 + 0.024*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.22	0.15 + 0.033*SL	0.16 + 0.031*SL	0.13 + 0.033*SL
D1 to Y	t_{PLH}	0.75	0.71 + 0.021*SL	0.72 + 0.015*SL	0.75 + 0.012*SL
	t_{PHL}	0.85	0.80 + 0.027*SL	0.81 + 0.021*SL	0.84 + 0.018*SL
	t_R	0.19	0.15 + 0.022*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.22	0.15 + 0.033*SL	0.16 + 0.031*SL	0.13 + 0.033*SL
D2 to Y	t_{PLH}	0.72	0.68 + 0.021*SL	0.69 + 0.015*SL	0.72 + 0.012*SL
	t_{PHL}	0.82	0.76 + 0.027*SL	0.77 + 0.021*SL	0.81 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.22	0.15 + 0.033*SL	0.16 + 0.031*SL	0.13 + 0.033*SL
D3 to Y	t_{PLH}	0.72	0.68 + 0.021*SL	0.69 + 0.015*SL	0.72 + 0.012*SL
	t_{PHL}	0.82	0.76 + 0.027*SL	0.77 + 0.021*SL	0.81 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.22	0.15 + 0.034*SL	0.16 + 0.031*SL	0.13 + 0.033*SL
D4 to Y	t_{PLH}	0.32	0.29 + 0.018*SL	0.29 + 0.015*SL	0.32 + 0.012*SL
	t_{PHL}	0.43	0.38 + 0.026*SL	0.39 + 0.021*SL	0.41 + 0.018*SL
	t_R	0.18	0.13 + 0.023*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.21	0.14 + 0.033*SL	0.15 + 0.031*SL	0.13 + 0.033*SL
S0 to Y	t_{PLH}	0.87	0.83 + 0.021*SL	0.84 + 0.015*SL	0.87 + 0.012*SL
	t_{PHL}	0.91	0.86 + 0.027*SL	0.87 + 0.021*SL	0.90 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.22	0.15 + 0.034*SL	0.16 + 0.031*SL	0.13 + 0.033*SL
S1 to Y	t_{PLH}	0.52	0.48 + 0.021*SL	0.49 + 0.015*SL	0.52 + 0.012*SL
	t_{PHL}	0.54	0.49 + 0.027*SL	0.50 + 0.022*SL	0.53 + 0.018*SL
	t_R	0.19	0.14 + 0.025*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.22	0.16 + 0.032*SL	0.16 + 0.031*SL	0.13 + 0.033*SL
S2 to Y	t_{PLH}	0.34	0.30 + 0.021*SL	0.31 + 0.015*SL	0.34 + 0.012*SL
	t_{PHL}	0.39	0.34 + 0.027*SL	0.35 + 0.021*SL	0.38 + 0.018*SL
	t_R	0.18	0.13 + 0.024*SL	0.13 + 0.024*SL	0.11 + 0.026*SL
	t_F	0.20	0.13 + 0.034*SL	0.14 + 0.032*SL	0.12 + 0.034*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	1.07	0.98 + 0.042*SL	1.00 + 0.036*SL	1.01 + 0.034*SL
	t_{PHL}	1.21	1.10 + 0.058*SL	1.12 + 0.049*SL	1.15 + 0.046*SL
	t_R	0.30	0.17 + 0.067*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.35	0.19 + 0.082*SL	0.20 + 0.078*SL	0.19 + 0.080*SL
D1 to Y	t_{PLH}	1.07	0.98 + 0.041*SL	1.00 + 0.036*SL	1.02 + 0.034*SL
	t_{PHL}	1.21	1.10 + 0.058*SL	1.12 + 0.049*SL	1.15 + 0.046*SL
	t_R	0.30	0.17 + 0.067*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.35	0.19 + 0.081*SL	0.20 + 0.079*SL	0.19 + 0.080*SL
D2 to Y	t_{PLH}	1.02	0.94 + 0.042*SL	0.96 + 0.036*SL	0.97 + 0.034*SL
	t_{PHL}	1.16	1.05 + 0.058*SL	1.07 + 0.049*SL	1.10 + 0.046*SL
	t_R	0.30	0.16 + 0.067*SL	0.16 + 0.068*SL	0.14 + 0.070*SL
	t_F	0.35	0.19 + 0.081*SL	0.20 + 0.079*SL	0.19 + 0.080*SL
D3 to Y	t_{PLH}	1.02	0.94 + 0.042*SL	0.96 + 0.036*SL	0.97 + 0.034*SL
	t_{PHL}	1.16	1.05 + 0.058*SL	1.07 + 0.049*SL	1.10 + 0.046*SL
	t_R	0.30	0.16 + 0.067*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.35	0.19 + 0.081*SL	0.20 + 0.079*SL	0.19 + 0.080*SL
D4 to Y	t_{PLH}	0.42	0.34 + 0.040*SL	0.36 + 0.035*SL	0.37 + 0.033*SL
	t_{PHL}	0.57	0.46 + 0.057*SL	0.48 + 0.048*SL	0.51 + 0.045*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.34	0.18 + 0.080*SL	0.18 + 0.079*SL	0.18 + 0.080*SL
S0 to Y	t_{PLH}	1.23	1.15 + 0.041*SL	1.17 + 0.036*SL	1.18 + 0.034*SL
	t_{PHL}	1.29	1.18 + 0.058*SL	1.20 + 0.049*SL	1.23 + 0.046*SL
	t_R	0.30	0.16 + 0.067*SL	0.16 + 0.068*SL	0.14 + 0.070*SL
	t_F	0.35	0.19 + 0.081*SL	0.20 + 0.079*SL	0.19 + 0.080*SL
S1 to Y	t_{PLH}	0.72	0.64 + 0.042*SL	0.66 + 0.036*SL	0.67 + 0.034*SL
	t_{PHL}	0.77	0.65 + 0.058*SL	0.68 + 0.049*SL	0.71 + 0.046*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.14 + 0.070*SL
	t_F	0.35	0.19 + 0.082*SL	0.20 + 0.078*SL	0.19 + 0.080*SL
S2 to Y	t_{PLH}	0.46	0.38 + 0.041*SL	0.39 + 0.035*SL	0.41 + 0.034*SL
	t_{PHL}	0.54	0.43 + 0.057*SL	0.45 + 0.048*SL	0.47 + 0.045*SL
	t_R	0.29	0.15 + 0.068*SL	0.15 + 0.069*SL	0.14 + 0.070*SL
	t_F	0.34	0.18 + 0.081*SL	0.18 + 0.079*SL	0.17 + 0.080*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX5D2

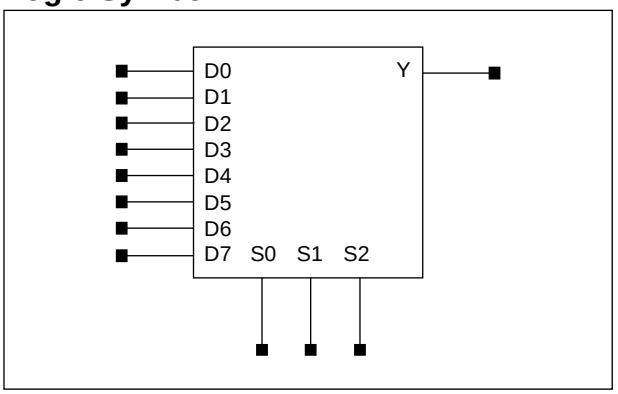
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	1.08	1.02 + 0.027*SL	1.04 + 0.022*SL	1.06 + 0.019*SL
	t_{PHL}	1.22	1.15 + 0.036*SL	1.17 + 0.030*SL	1.20 + 0.026*SL
	t_R	0.24	0.17 + 0.034*SL	0.17 + 0.034*SL	0.17 + 0.033*SL
	t_F	0.29	0.20 + 0.044*SL	0.22 + 0.039*SL	0.23 + 0.038*SL
D1 to Y	t_{PLH}	1.08	1.02 + 0.027*SL	1.04 + 0.022*SL	1.06 + 0.019*SL
	t_{PHL}	1.22	1.15 + 0.036*SL	1.17 + 0.030*SL	1.20 + 0.025*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.29	0.20 + 0.043*SL	0.21 + 0.040*SL	0.22 + 0.038*SL
D2 to Y	t_{PLH}	1.03	0.98 + 0.027*SL	0.99 + 0.022*SL	1.01 + 0.019*SL
	t_{PHL}	1.17	1.10 + 0.036*SL	1.12 + 0.030*SL	1.14 + 0.026*SL
	t_R	0.24	0.16 + 0.035*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.29	0.20 + 0.043*SL	0.21 + 0.040*SL	0.22 + 0.038*SL
D3 to Y	t_{PLH}	1.03	0.98 + 0.027*SL	0.99 + 0.022*SL	1.01 + 0.019*SL
	t_{PHL}	1.17	1.10 + 0.036*SL	1.12 + 0.030*SL	1.14 + 0.026*SL
	t_R	0.24	0.16 + 0.035*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.29	0.20 + 0.043*SL	0.21 + 0.040*SL	0.22 + 0.038*SL
D4 to Y	t_{PLH}	0.43	0.38 + 0.026*SL	0.39 + 0.021*SL	0.41 + 0.019*SL
	t_{PHL}	0.58	0.51 + 0.035*SL	0.53 + 0.029*SL	0.56 + 0.025*SL
	t_R	0.22	0.15 + 0.035*SL	0.15 + 0.035*SL	0.16 + 0.034*SL
	t_F	0.27	0.19 + 0.043*SL	0.20 + 0.040*SL	0.21 + 0.038*SL
S0 to Y	t_{PLH}	1.24	1.19 + 0.027*SL	1.20 + 0.022*SL	1.22 + 0.019*SL
	t_{PHL}	1.30	1.23 + 0.036*SL	1.25 + 0.030*SL	1.27 + 0.026*SL
	t_R	0.24	0.16 + 0.035*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.29	0.20 + 0.043*SL	0.21 + 0.040*SL	0.22 + 0.038*SL
S1 to Y	t_{PLH}	0.73	0.68 + 0.027*SL	0.69 + 0.022*SL	0.71 + 0.019*SL
	t_{PHL}	0.78	0.70 + 0.036*SL	0.72 + 0.030*SL	0.75 + 0.026*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.29	0.20 + 0.043*SL	0.21 + 0.040*SL	0.22 + 0.038*SL
S2 to Y	t_{PLH}	0.46	0.41 + 0.026*SL	0.42 + 0.021*SL	0.44 + 0.019*SL
	t_{PHL}	0.54	0.47 + 0.035*SL	0.49 + 0.029*SL	0.51 + 0.025*SL
	t_R	0.23	0.16 + 0.035*SL	0.16 + 0.035*SL	0.16 + 0.034*SL
	t_F	0.27	0.18 + 0.043*SL	0.19 + 0.040*SL	0.21 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

MX8/MX8D2

8 > 1 Non-Inverting MUX with 1X/2X Drive

Logic Symbol



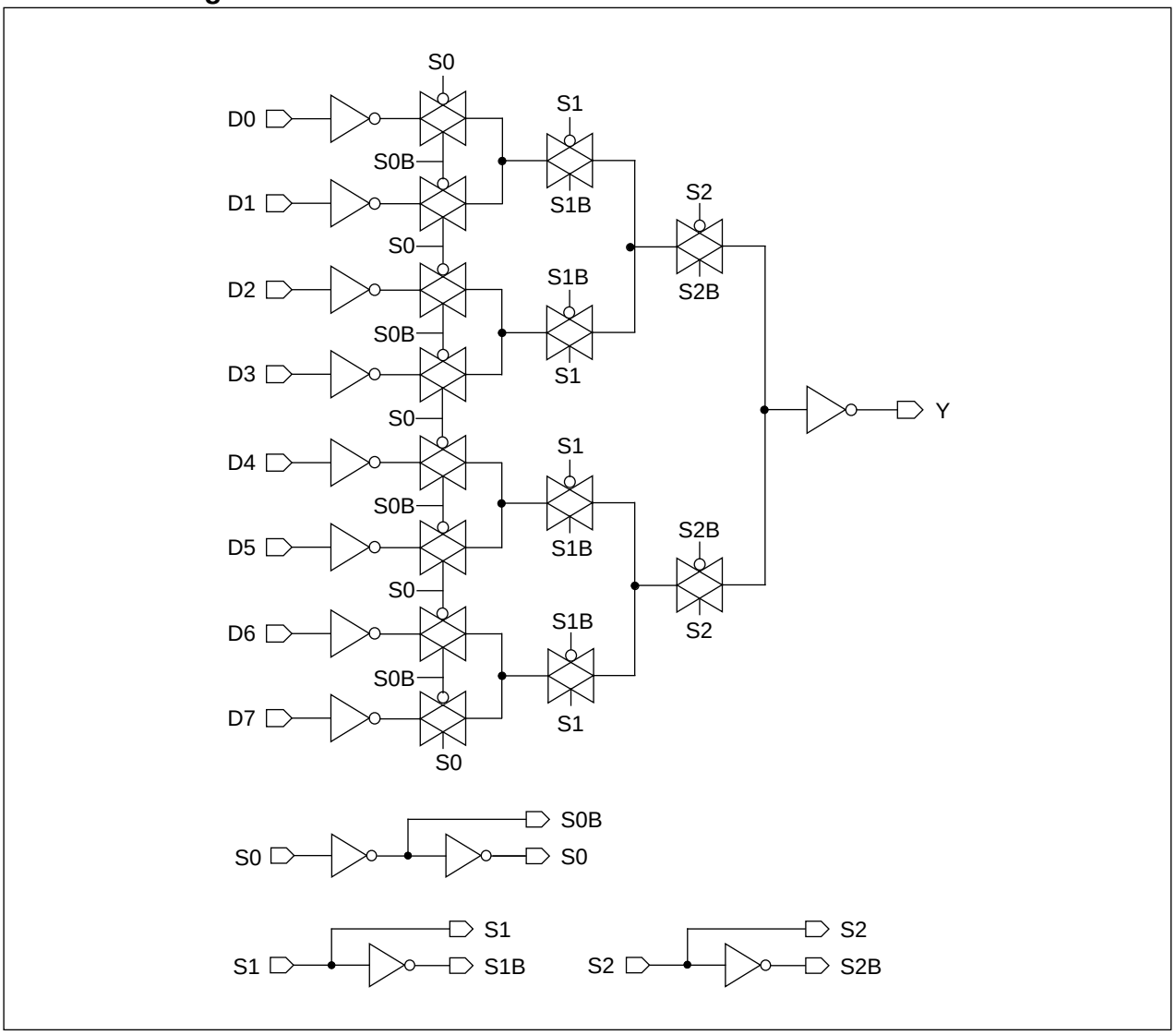
Truth Table

S0	S1	S2	Y
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D7

Cell Data

Input Load (SL)											Gate Count
STD80											
MX8											*MX8*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.6	0.7	0.7	0.7	0.6	0.7	0.7	0.7	0.7	1.2	1.3	12.7
MX8D2											*MX8D2*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.6	0.7	0.7	0.7	0.6	0.7	0.7	0.7	0.6	1.2	1.0	13.0
STDM80											
MX8											*MX8*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	2.2	1.5	12.7
MX8D2											*MX8D2*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	2.2	1.5	13.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.66	0.57 + 0.044*SL	0.60 + 0.031*SL	0.67 + 0.024*SL
	t_{PHL}	0.82	0.70 + 0.060*SL	0.73 + 0.046*SL	0.82 + 0.037*SL
	t_R	0.35	0.24 + 0.052*SL	0.25 + 0.048*SL	0.22 + 0.051*SL
	t_F	0.45	0.31 + 0.072*SL	0.33 + 0.065*SL	0.30 + 0.068*SL
D1 to Y	t_{PLH}	0.66	0.57 + 0.044*SL	0.60 + 0.032*SL	0.68 + 0.024*SL
	t_{PHL}	0.82	0.70 + 0.060*SL	0.73 + 0.046*SL	0.82 + 0.037*SL
	t_R	0.35	0.24 + 0.051*SL	0.25 + 0.048*SL	0.22 + 0.051*SL
	t_F	0.45	0.31 + 0.072*SL	0.33 + 0.065*SL	0.30 + 0.068*SL
D2 to Y	t_{PLH}	0.64	0.56 + 0.044*SL	0.58 + 0.031*SL	0.65 + 0.024*SL
	t_{PHL}	0.81	0.69 + 0.060*SL	0.72 + 0.046*SL	0.80 + 0.037*SL
	t_R	0.34	0.24 + 0.050*SL	0.25 + 0.048*SL	0.21 + 0.051*SL
	t_F	0.45	0.30 + 0.071*SL	0.32 + 0.065*SL	0.29 + 0.068*SL
D3 to Y	t_{PLH}	0.64	0.56 + 0.044*SL	0.58 + 0.031*SL	0.65 + 0.024*SL
	t_{PHL}	0.81	0.69 + 0.060*SL	0.72 + 0.046*SL	0.80 + 0.037*SL
	t_R	0.34	0.24 + 0.051*SL	0.25 + 0.048*SL	0.21 + 0.051*SL
	t_F	0.45	0.30 + 0.071*SL	0.32 + 0.065*SL	0.29 + 0.068*SL
D4 to Y	t_{PLH}	0.65	0.56 + 0.044*SL	0.59 + 0.031*SL	0.66 + 0.024*SL
	t_{PHL}	0.82	0.70 + 0.060*SL	0.73 + 0.046*SL	0.81 + 0.037*SL
	t_R	0.35	0.25 + 0.050*SL	0.25 + 0.047*SL	0.22 + 0.051*SL
	t_F	0.45	0.31 + 0.072*SL	0.32 + 0.065*SL	0.30 + 0.068*SL
D5 to Y	t_{PLH}	0.65	0.56 + 0.044*SL	0.59 + 0.031*SL	0.66 + 0.024*SL
	t_{PHL}	0.82	0.70 + 0.060*SL	0.73 + 0.046*SL	0.81 + 0.037*SL
	t_R	0.35	0.25 + 0.050*SL	0.25 + 0.047*SL	0.22 + 0.051*SL
	t_F	0.45	0.31 + 0.072*SL	0.32 + 0.065*SL	0.30 + 0.068*SL
D6 to Y	t_{PLH}	0.64	0.56 + 0.044*SL	0.58 + 0.031*SL	0.66 + 0.024*SL
	t_{PHL}	0.81	0.69 + 0.060*SL	0.72 + 0.046*SL	0.81 + 0.037*SL
	t_R	0.34	0.24 + 0.050*SL	0.25 + 0.047*SL	0.22 + 0.051*SL
	t_F	0.45	0.31 + 0.073*SL	0.32 + 0.065*SL	0.29 + 0.068*SL
D7 to Y	t_{PLH}	0.64	0.56 + 0.044*SL	0.58 + 0.031*SL	0.66 + 0.024*SL
	t_{PHL}	0.81	0.69 + 0.060*SL	0.72 + 0.046*SL	0.81 + 0.037*SL
	t_R	0.34	0.24 + 0.050*SL	0.25 + 0.048*SL	0.22 + 0.051*SL
	t_F	0.45	0.31 + 0.073*SL	0.32 + 0.065*SL	0.29 + 0.068*SL
S0 to Y	t_{PLH}	0.93	0.84 + 0.044*SL	0.86 + 0.031*SL	0.94 + 0.024*SL
	t_{PHL}	1.04	0.92 + 0.060*SL	0.95 + 0.046*SL	1.04 + 0.037*SL
	t_R	0.35	0.25 + 0.050*SL	0.25 + 0.048*SL	0.22 + 0.051*SL
	t_F	0.45	0.31 + 0.072*SL	0.32 + 0.065*SL	0.30 + 0.068*SL
S1 to Y	t_{PLH}	0.56	0.48 + 0.044*SL	0.50 + 0.031*SL	0.58 + 0.024*SL
	t_{PHL}	0.69	0.57 + 0.060*SL	0.60 + 0.046*SL	0.69 + 0.037*SL
	t_R	0.33	0.24 + 0.050*SL	0.24 + 0.048*SL	0.21 + 0.051*SL
	t_F	0.44	0.30 + 0.071*SL	0.31 + 0.065*SL	0.29 + 0.068*SL
S2 to Y	t_{PLH}	0.38	0.30 + 0.039*SL	0.32 + 0.030*SL	0.37 + 0.024*SL
	t_{PHL}	0.45	0.34 + 0.057*SL	0.36 + 0.046*SL	0.44 + 0.037*SL
	t_R	0.26	0.15 + 0.053*SL	0.16 + 0.052*SL	0.16 + 0.051*SL
	t_F	0.34	0.19 + 0.077*SL	0.20 + 0.070*SL	0.22 + 0.068*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 MX8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.67	0.61 + 0.029*SL	0.63 + 0.021*SL	0.71 + 0.012*SL
	t_{PHL}	0.83	0.76 + 0.037*SL	0.78 + 0.028*SL	0.87 + 0.019*SL
	t_R	0.32	0.26 + 0.030*SL	0.27 + 0.025*SL	0.27 + 0.025*SL
	t_F	0.42	0.33 + 0.041*SL	0.35 + 0.034*SL	0.37 + 0.032*SL
D1 to Y	t_{PLH}	0.67	0.62 + 0.029*SL	0.63 + 0.021*SL	0.71 + 0.012*SL
	t_{PHL}	0.83	0.76 + 0.037*SL	0.78 + 0.028*SL	0.87 + 0.019*SL
	t_R	0.32	0.26 + 0.031*SL	0.27 + 0.025*SL	0.27 + 0.025*SL
	t_F	0.42	0.33 + 0.044*SL	0.35 + 0.034*SL	0.37 + 0.032*SL
D2 to Y	t_{PLH}	0.65	0.60 + 0.029*SL	0.62 + 0.020*SL	0.69 + 0.012*SL
	t_{PHL}	0.82	0.74 + 0.037*SL	0.76 + 0.028*SL	0.85 + 0.019*SL
	t_R	0.31	0.26 + 0.029*SL	0.27 + 0.025*SL	0.26 + 0.025*SL
	t_F	0.41	0.33 + 0.042*SL	0.34 + 0.034*SL	0.36 + 0.032*SL
D3 to Y	t_{PLH}	0.65	0.60 + 0.029*SL	0.62 + 0.020*SL	0.69 + 0.012*SL
	t_{PHL}	0.82	0.74 + 0.037*SL	0.76 + 0.028*SL	0.85 + 0.019*SL
	t_R	0.31	0.25 + 0.030*SL	0.27 + 0.025*SL	0.26 + 0.025*SL
	t_F	0.41	0.33 + 0.042*SL	0.34 + 0.034*SL	0.36 + 0.032*SL
D4 to Y	t_{PLH}	0.66	0.60 + 0.029*SL	0.62 + 0.020*SL	0.70 + 0.012*SL
	t_{PHL}	0.82	0.75 + 0.037*SL	0.77 + 0.028*SL	0.86 + 0.019*SL
	t_R	0.32	0.26 + 0.030*SL	0.27 + 0.025*SL	0.27 + 0.025*SL
	t_F	0.41	0.33 + 0.041*SL	0.35 + 0.034*SL	0.36 + 0.032*SL
D5 to Y	t_{PLH}	0.66	0.60 + 0.029*SL	0.62 + 0.021*SL	0.70 + 0.012*SL
	t_{PHL}	0.82	0.75 + 0.038*SL	0.77 + 0.028*SL	0.86 + 0.019*SL
	t_R	0.32	0.26 + 0.029*SL	0.27 + 0.025*SL	0.27 + 0.025*SL
	t_F	0.41	0.33 + 0.043*SL	0.35 + 0.034*SL	0.36 + 0.032*SL
D6 to Y	t_{PLH}	0.65	0.60 + 0.029*SL	0.61 + 0.020*SL	0.69 + 0.012*SL
	t_{PHL}	0.82	0.75 + 0.037*SL	0.77 + 0.028*SL	0.85 + 0.019*SL
	t_R	0.32	0.26 + 0.029*SL	0.27 + 0.025*SL	0.27 + 0.025*SL
	t_F	0.41	0.33 + 0.041*SL	0.34 + 0.034*SL	0.36 + 0.032*SL
D7 to Y	t_{PLH}	0.65	0.60 + 0.029*SL	0.61 + 0.020*SL	0.69 + 0.012*SL
	t_{PHL}	0.82	0.75 + 0.037*SL	0.77 + 0.028*SL	0.85 + 0.019*SL
	t_R	0.32	0.26 + 0.029*SL	0.27 + 0.025*SL	0.27 + 0.025*SL
	t_F	0.41	0.33 + 0.040*SL	0.34 + 0.034*SL	0.36 + 0.032*SL
S0 to Y	t_{PLH}	0.94	0.88 + 0.029*SL	0.90 + 0.020*SL	0.98 + 0.012*SL
	t_{PHL}	1.05	0.98 + 0.037*SL	1.00 + 0.028*SL	1.09 + 0.019*SL
	t_R	0.32	0.26 + 0.028*SL	0.27 + 0.025*SL	0.27 + 0.025*SL
	t_F	0.41	0.33 + 0.043*SL	0.35 + 0.034*SL	0.36 + 0.032*SL
S1 to Y	t_{PLH}	0.57	0.51 + 0.029*SL	0.53 + 0.020*SL	0.61 + 0.012*SL
	t_{PHL}	0.69	0.62 + 0.037*SL	0.64 + 0.028*SL	0.73 + 0.019*SL
	t_R	0.31	0.25 + 0.029*SL	0.26 + 0.025*SL	0.26 + 0.025*SL
	t_F	0.40	0.32 + 0.040*SL	0.34 + 0.034*SL	0.35 + 0.032*SL
S2 to Y	t_{PLH}	0.38	0.33 + 0.026*SL	0.34 + 0.020*SL	0.41 + 0.012*SL
	t_{PHL}	0.46	0.38 + 0.036*SL	0.40 + 0.028*SL	0.49 + 0.019*SL
	t_R	0.24	0.18 + 0.029*SL	0.19 + 0.027*SL	0.20 + 0.025*SL
	t_F	0.32	0.23 + 0.045*SL	0.24 + 0.037*SL	0.28 + 0.033*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.97	0.86 + 0.056*SL	0.89 + 0.045*SL	0.93 + 0.039*SL
	t_{PHL}	1.25	1.08 + 0.082*SL	1.13 + 0.065*SL	1.19 + 0.056*SL
	t_R	0.44	0.29 + 0.075*SL	0.30 + 0.070*SL	0.32 + 0.068*SL
	t_F	0.63	0.45 + 0.093*SL	0.47 + 0.084*SL	0.50 + 0.080*SL
D1 to Y	t_{PLH}	0.97	0.86 + 0.056*SL	0.89 + 0.045*SL	0.94 + 0.039*SL
	t_{PHL}	1.24	1.08 + 0.082*SL	1.13 + 0.065*SL	1.19 + 0.056*SL
	t_R	0.44	0.29 + 0.075*SL	0.30 + 0.070*SL	0.32 + 0.068*SL
	t_F	0.63	0.45 + 0.093*SL	0.47 + 0.084*SL	0.50 + 0.080*SL
D2 to Y	t_{PLH}	0.94	0.83 + 0.056*SL	0.87 + 0.045*SL	0.91 + 0.039*SL
	t_{PHL}	1.22	1.06 + 0.081*SL	1.11 + 0.065*SL	1.17 + 0.056*SL
	t_R	0.44	0.29 + 0.075*SL	0.30 + 0.069*SL	0.31 + 0.068*SL
	t_F	0.62	0.43 + 0.093*SL	0.46 + 0.084*SL	0.49 + 0.080*SL
D3 to Y	t_{PLH}	0.94	0.83 + 0.055*SL	0.87 + 0.045*SL	0.91 + 0.039*SL
	t_{PHL}	1.22	1.06 + 0.081*SL	1.11 + 0.065*SL	1.17 + 0.056*SL
	t_R	0.44	0.29 + 0.075*SL	0.30 + 0.070*SL	0.31 + 0.068*SL
	t_F	0.62	0.43 + 0.093*SL	0.46 + 0.084*SL	0.49 + 0.080*SL
D4 to Y	t_{PLH}	0.96	0.84 + 0.056*SL	0.88 + 0.045*SL	0.92 + 0.039*SL
	t_{PHL}	1.23	1.07 + 0.082*SL	1.12 + 0.065*SL	1.18 + 0.056*SL
	t_R	0.44	0.29 + 0.075*SL	0.30 + 0.070*SL	0.32 + 0.068*SL
	t_F	0.63	0.44 + 0.093*SL	0.47 + 0.084*SL	0.50 + 0.080*SL
D5 to Y	t_{PLH}	0.96	0.84 + 0.056*SL	0.88 + 0.045*SL	0.92 + 0.039*SL
	t_{PHL}	1.23	1.07 + 0.082*SL	1.12 + 0.065*SL	1.18 + 0.056*SL
	t_R	0.44	0.29 + 0.075*SL	0.30 + 0.070*SL	0.32 + 0.068*SL
	t_F	0.63	0.44 + 0.093*SL	0.47 + 0.084*SL	0.50 + 0.080*SL
D6 to Y	t_{PLH}	0.95	0.83 + 0.056*SL	0.87 + 0.045*SL	0.91 + 0.039*SL
	t_{PHL}	1.23	1.07 + 0.081*SL	1.11 + 0.065*SL	1.18 + 0.056*SL
	t_R	0.44	0.29 + 0.076*SL	0.31 + 0.069*SL	0.31 + 0.068*SL
	t_F	0.63	0.44 + 0.092*SL	0.47 + 0.084*SL	0.50 + 0.080*SL
D7 to Y	t_{PLH}	0.95	0.83 + 0.056*SL	0.87 + 0.045*SL	0.91 + 0.039*SL
	t_{PHL}	1.23	1.07 + 0.081*SL	1.11 + 0.065*SL	1.18 + 0.056*SL
	t_R	0.44	0.29 + 0.075*SL	0.31 + 0.070*SL	0.31 + 0.068*SL
	t_F	0.63	0.44 + 0.092*SL	0.47 + 0.084*SL	0.50 + 0.080*SL
S0 to Y	t_{PLH}	1.35	1.24 + 0.056*SL	1.27 + 0.045*SL	1.31 + 0.039*SL
	t_{PHL}	1.56	1.39 + 0.081*SL	1.44 + 0.065*SL	1.50 + 0.056*SL
	t_R	0.44	0.29 + 0.075*SL	0.31 + 0.070*SL	0.32 + 0.068*SL
	t_F	0.63	0.44 + 0.093*SL	0.47 + 0.084*SL	0.50 + 0.080*SL
S1 to Y	t_{PLH}	0.83	0.72 + 0.056*SL	0.75 + 0.045*SL	0.79 + 0.039*SL
	t_{PHL}	1.03	0.87 + 0.082*SL	0.92 + 0.065*SL	0.98 + 0.056*SL
	t_R	0.43	0.28 + 0.075*SL	0.30 + 0.070*SL	0.31 + 0.068*SL
	t_F	0.61	0.43 + 0.093*SL	0.45 + 0.085*SL	0.49 + 0.080*SL
S2 to Y	t_{PLH}	0.52	0.41 + 0.051*SL	0.44 + 0.044*SL	0.47 + 0.039*SL
	t_{PHL}	0.62	0.47 + 0.074*SL	0.50 + 0.063*SL	0.56 + 0.055*SL
	t_R	0.36	0.20 + 0.080*SL	0.22 + 0.074*SL	0.24 + 0.071*SL
	t_F	0.45	0.25 + 0.102*SL	0.28 + 0.092*SL	0.33 + 0.085*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 MX8D2

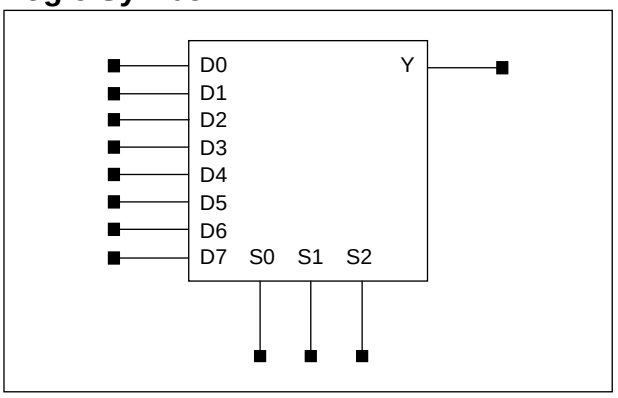
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	1.00	0.92 + 0.037*SL	0.95 + 0.029*SL	0.98 + 0.024*SL
	t_{PHL}	1.27	1.17 + 0.053*SL	1.20 + 0.042*SL	1.25 + 0.034*SL
	t_R	0.38	0.30 + 0.041*SL	0.31 + 0.037*SL	0.32 + 0.036*SL
	t_F	0.58	0.47 + 0.057*SL	0.50 + 0.046*SL	0.53 + 0.041*SL
D1 to Y	t_{PLH}	1.00	0.93 + 0.038*SL	0.95 + 0.029*SL	0.99 + 0.024*SL
	t_{PHL}	1.27	1.16 + 0.053*SL	1.20 + 0.042*SL	1.25 + 0.034*SL
	t_R	0.38	0.30 + 0.041*SL	0.31 + 0.037*SL	0.32 + 0.036*SL
	t_F	0.58	0.47 + 0.057*SL	0.50 + 0.046*SL	0.53 + 0.041*SL
D2 to Y	t_{PLH}	0.97	0.90 + 0.038*SL	0.92 + 0.029*SL	0.96 + 0.024*SL
	t_{PHL}	1.25	1.14 + 0.053*SL	1.18 + 0.041*SL	1.23 + 0.034*SL
	t_R	0.38	0.30 + 0.040*SL	0.31 + 0.037*SL	0.32 + 0.036*SL
	t_F	0.57	0.46 + 0.057*SL	0.49 + 0.046*SL	0.52 + 0.041*SL
D3 to Y	t_{PLH}	0.97	0.90 + 0.038*SL	0.92 + 0.029*SL	0.96 + 0.024*SL
	t_{PHL}	1.25	1.14 + 0.052*SL	1.17 + 0.041*SL	1.23 + 0.034*SL
	t_R	0.38	0.30 + 0.040*SL	0.31 + 0.037*SL	0.32 + 0.036*SL
	t_F	0.57	0.46 + 0.057*SL	0.49 + 0.046*SL	0.52 + 0.041*SL
D4 to Y	t_{PLH}	0.98	0.91 + 0.037*SL	0.93 + 0.029*SL	0.96 + 0.024*SL
	t_{PHL}	1.25	1.15 + 0.053*SL	1.18 + 0.041*SL	1.23 + 0.034*SL
	t_R	0.38	0.30 + 0.041*SL	0.31 + 0.037*SL	0.32 + 0.036*SL
	t_F	0.57	0.46 + 0.057*SL	0.49 + 0.046*SL	0.53 + 0.041*SL
D5 to Y	t_{PLH}	0.98	0.90 + 0.038*SL	0.93 + 0.029*SL	0.96 + 0.024*SL
	t_{PHL}	1.25	1.15 + 0.052*SL	1.18 + 0.041*SL	1.23 + 0.034*SL
	t_R	0.38	0.30 + 0.040*SL	0.31 + 0.038*SL	0.32 + 0.036*SL
	t_F	0.57	0.46 + 0.057*SL	0.49 + 0.046*SL	0.53 + 0.041*SL
D6 to Y	t_{PLH}	0.97	0.89 + 0.037*SL	0.92 + 0.029*SL	0.96 + 0.024*SL
	t_{PHL}	1.25	1.14 + 0.053*SL	1.18 + 0.041*SL	1.23 + 0.034*SL
	t_R	0.38	0.30 + 0.041*SL	0.31 + 0.037*SL	0.31 + 0.036*SL
	t_F	0.57	0.46 + 0.057*SL	0.49 + 0.046*SL	0.52 + 0.042*SL
D7 to Y	t_{PLH}	0.97	0.89 + 0.037*SL	0.92 + 0.029*SL	0.96 + 0.024*SL
	t_{PHL}	1.25	1.14 + 0.053*SL	1.18 + 0.041*SL	1.23 + 0.034*SL
	t_R	0.38	0.30 + 0.040*SL	0.30 + 0.038*SL	0.32 + 0.036*SL
	t_F	0.57	0.46 + 0.056*SL	0.49 + 0.046*SL	0.52 + 0.042*SL
S0 to Y	t_{PLH}	1.38	1.30 + 0.038*SL	1.33 + 0.029*SL	1.36 + 0.024*SL
	t_{PHL}	1.58	1.48 + 0.053*SL	1.51 + 0.041*SL	1.56 + 0.034*SL
	t_R	0.38	0.30 + 0.039*SL	0.31 + 0.038*SL	0.32 + 0.036*SL
	t_F	0.57	0.46 + 0.056*SL	0.49 + 0.046*SL	0.52 + 0.041*SL
S1 to Y	t_{PLH}	0.85	0.77 + 0.037*SL	0.80 + 0.029*SL	0.83 + 0.024*SL
	t_{PHL}	1.06	0.95 + 0.053*SL	0.99 + 0.041*SL	1.04 + 0.034*SL
	t_R	0.38	0.29 + 0.040*SL	0.30 + 0.038*SL	0.32 + 0.036*SL
	t_F	0.57	0.45 + 0.056*SL	0.49 + 0.046*SL	0.51 + 0.042*SL
S2 to Y	t_{PLH}	0.53	0.46 + 0.035*SL	0.48 + 0.028*SL	0.51 + 0.024*SL
	t_{PHL}	0.64	0.54 + 0.050*SL	0.57 + 0.040*SL	0.61 + 0.034*SL
	t_R	0.31	0.23 + 0.042*SL	0.24 + 0.040*SL	0.25 + 0.038*SL
	t_F	0.43	0.31 + 0.058*SL	0.34 + 0.049*SL	0.37 + 0.045*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

YMX8/YMX8D2

Fast 8 > 1 Non-Inverting MUX with 1X/2X Drive

Logic Symbol



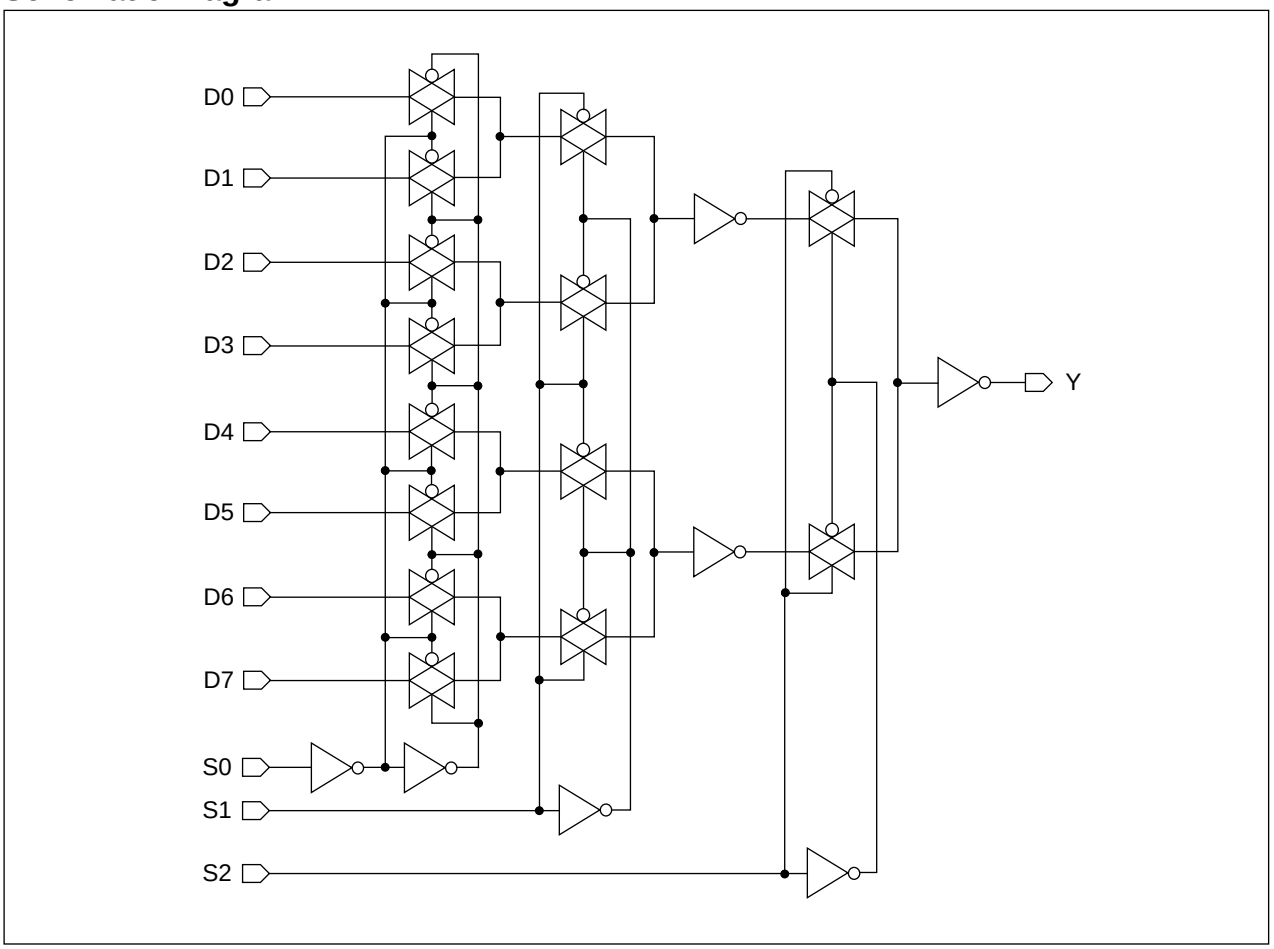
Truth Table

S0	S1	S2	Y
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D7

Cell Data

Input Load (SL)											Gate Count	
STD80												
YMX8/YMX8D2											*YMX8*	*YMX8D2*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2		
3.2	3.2	3.0	3.1	3.2	3.1	2.9	3.0	0.6	1.6	1.1	11.0	11.3
STDM80												
YMX8/YMX8D2											*YMX8*	*YMX8D2*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2		
3.7	3.7	3.5	3.6	3.6	3.6	3.4	3.4	0.6	1.8	1.2	11.0	11.3

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 YMX8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.50	0.44 + 0.031*SL	0.45 + 0.025*SL	0.46 + 0.024*SL
	t_{PHL}	0.59	0.50 + 0.045*SL	0.51 + 0.039*SL	0.53 + 0.037*SL
	t_R	0.23	0.14 + 0.044*SL	0.13 + 0.047*SL	0.09 + 0.052*SL
	t_F	0.28	0.15 + 0.063*SL	0.15 + 0.065*SL	0.11 + 0.069*SL
D1 to Y	t_{PLH}	0.50	0.43 + 0.031*SL	0.45 + 0.025*SL	0.46 + 0.024*SL
	t_{PHL}	0.59	0.50 + 0.044*SL	0.51 + 0.039*SL	0.53 + 0.037*SL
	t_R	0.23	0.14 + 0.045*SL	0.13 + 0.047*SL	0.09 + 0.052*SL
	t_F	0.27	0.15 + 0.064*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
D2 to Y	t_{PLH}	0.49	0.43 + 0.031*SL	0.44 + 0.025*SL	0.46 + 0.024*SL
	t_{PHL}	0.58	0.49 + 0.045*SL	0.51 + 0.039*SL	0.52 + 0.037*SL
	t_R	0.23	0.14 + 0.044*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.28	0.15 + 0.062*SL	0.15 + 0.065*SL	0.10 + 0.069*SL
D3 to Y	t_{PLH}	0.49	0.43 + 0.031*SL	0.45 + 0.025*SL	0.46 + 0.024*SL
	t_{PHL}	0.59	0.49 + 0.045*SL	0.51 + 0.039*SL	0.53 + 0.037*SL
	t_R	0.23	0.14 + 0.044*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.28	0.15 + 0.063*SL	0.15 + 0.065*SL	0.10 + 0.069*SL
D4 to Y	t_{PLH}	0.48	0.42 + 0.030*SL	0.44 + 0.025*SL	0.45 + 0.024*SL
	t_{PHL}	0.58	0.49 + 0.044*SL	0.50 + 0.039*SL	0.52 + 0.037*SL
	t_R	0.22	0.14 + 0.044*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.15 + 0.063*SL	0.15 + 0.065*SL	0.10 + 0.069*SL
D5 to Y	t_{PLH}	0.48	0.42 + 0.031*SL	0.43 + 0.025*SL	0.45 + 0.024*SL
	t_{PHL}	0.58	0.49 + 0.044*SL	0.50 + 0.039*SL	0.52 + 0.037*SL
	t_R	0.23	0.14 + 0.044*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.15 + 0.063*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
D6 to Y	t_{PLH}	0.48	0.42 + 0.030*SL	0.43 + 0.025*SL	0.44 + 0.024*SL
	t_{PHL}	0.57	0.48 + 0.044*SL	0.50 + 0.039*SL	0.51 + 0.037*SL
	t_R	0.23	0.13 + 0.045*SL	0.13 + 0.047*SL	0.09 + 0.052*SL
	t_F	0.27	0.15 + 0.064*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
D7 to Y	t_{PLH}	0.48	0.42 + 0.030*SL	0.43 + 0.025*SL	0.44 + 0.024*SL
	t_{PHL}	0.57	0.48 + 0.044*SL	0.49 + 0.039*SL	0.51 + 0.037*SL
	t_R	0.22	0.14 + 0.044*SL	0.13 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.15 + 0.063*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
S0 to Y	t_{PLH}	0.96	0.90 + 0.030*SL	0.91 + 0.025*SL	0.92 + 0.024*SL
	t_{PHL}	0.93	0.85 + 0.044*SL	0.86 + 0.039*SL	0.87 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.27	0.15 + 0.063*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
S1 to Y	t_{PLH}	0.57	0.51 + 0.030*SL	0.52 + 0.025*SL	0.53 + 0.024*SL
	t_{PHL}	0.51	0.42 + 0.044*SL	0.44 + 0.039*SL	0.45 + 0.037*SL
	t_R	0.22	0.13 + 0.045*SL	0.12 + 0.048*SL	0.08 + 0.052*SL
	t_F	0.27	0.15 + 0.062*SL	0.14 + 0.065*SL	0.10 + 0.069*SL
S2 to Y	t_{PLH}	0.32	0.27 + 0.029*SL	0.28 + 0.025*SL	0.29 + 0.024*SL
	t_{PHL}	0.40	0.31 + 0.044*SL	0.32 + 0.039*SL	0.34 + 0.037*SL
	t_R	0.20	0.11 + 0.049*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.066*SL	0.10 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 YMX8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.51	0.47 + 0.020*SL	0.48 + 0.015*SL	0.51 + 0.012*SL
	t_{PHL}	0.60	0.54 + 0.028*SL	0.55 + 0.022*SL	0.59 + 0.018*SL
	t_R	0.19	0.15 + 0.024*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.24	0.17 + 0.033*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
D1 to Y	t_{PLH}	0.51	0.47 + 0.021*SL	0.48 + 0.015*SL	0.51 + 0.012*SL
	t_{PHL}	0.60	0.54 + 0.028*SL	0.55 + 0.022*SL	0.59 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.24	0.17 + 0.033*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
D2 to Y	t_{PLH}	0.51	0.47 + 0.020*SL	0.48 + 0.015*SL	0.51 + 0.012*SL
	t_{PHL}	0.59	0.54 + 0.028*SL	0.55 + 0.022*SL	0.58 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.24	0.17 + 0.034*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
D3 to Y	t_{PLH}	0.51	0.47 + 0.020*SL	0.48 + 0.015*SL	0.51 + 0.012*SL
	t_{PHL}	0.59	0.54 + 0.028*SL	0.55 + 0.022*SL	0.58 + 0.018*SL
	t_R	0.19	0.15 + 0.024*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.24	0.17 + 0.034*SL	0.18 + 0.031*SL	0.15 + 0.033*SL
D4 to Y	t_{PLH}	0.50	0.46 + 0.020*SL	0.47 + 0.015*SL	0.50 + 0.012*SL
	t_{PHL}	0.59	0.53 + 0.028*SL	0.55 + 0.022*SL	0.58 + 0.018*SL
	t_R	0.19	0.15 + 0.023*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.23	0.17 + 0.034*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
D5 to Y	t_{PLH}	0.50	0.46 + 0.020*SL	0.47 + 0.015*SL	0.50 + 0.012*SL
	t_{PHL}	0.59	0.53 + 0.028*SL	0.55 + 0.022*SL	0.58 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.23	0.17 + 0.033*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
D6 to Y	t_{PLH}	0.49	0.45 + 0.020*SL	0.46 + 0.015*SL	0.49 + 0.012*SL
	t_{PHL}	0.58	0.52 + 0.028*SL	0.54 + 0.022*SL	0.57 + 0.018*SL
	t_R	0.19	0.14 + 0.024*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.23	0.17 + 0.034*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
D7 to Y	t_{PLH}	0.49	0.45 + 0.020*SL	0.46 + 0.015*SL	0.49 + 0.012*SL
	t_{PHL}	0.58	0.53 + 0.027*SL	0.54 + 0.022*SL	0.57 + 0.018*SL
	t_R	0.19	0.14 + 0.024*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.24	0.17 + 0.034*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
S0 to Y	t_{PLH}	0.97	0.93 + 0.020*SL	0.94 + 0.015*SL	0.97 + 0.012*SL
	t_{PHL}	0.94	0.89 + 0.028*SL	0.90 + 0.022*SL	0.93 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.23	0.17 + 0.033*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
S1 to Y	t_{PLH}	0.58	0.54 + 0.020*SL	0.55 + 0.015*SL	0.58 + 0.012*SL
	t_{PHL}	0.52	0.47 + 0.028*SL	0.48 + 0.022*SL	0.51 + 0.018*SL
	t_R	0.18	0.14 + 0.020*SL	0.14 + 0.023*SL	0.11 + 0.026*SL
	t_F	0.23	0.17 + 0.032*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
S2 to Y	t_{PLH}	0.33	0.29 + 0.020*SL	0.30 + 0.015*SL	0.33 + 0.012*SL
	t_{PHL}	0.40	0.34 + 0.028*SL	0.36 + 0.022*SL	0.39 + 0.018*SL
	t_R	0.17	0.13 + 0.021*SL	0.12 + 0.024*SL	0.10 + 0.026*SL
	t_F	0.22	0.15 + 0.034*SL	0.16 + 0.032*SL	0.14 + 0.033*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 YMX8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.76	0.68 + 0.042*SL	0.69 + 0.036*SL	0.71 + 0.034*SL
	t_{PHL}	0.85	0.73 + 0.059*SL	0.76 + 0.050*SL	0.79 + 0.046*SL
	t_R	0.30	0.17 + 0.066*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.37	0.21 + 0.081*SL	0.21 + 0.078*SL	0.21 + 0.079*SL
D1 to Y	t_{PLH}	0.76	0.68 + 0.042*SL	0.69 + 0.036*SL	0.71 + 0.034*SL
	t_{PHL}	0.85	0.73 + 0.059*SL	0.76 + 0.050*SL	0.79 + 0.046*SL
	t_R	0.30	0.17 + 0.067*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.37	0.21 + 0.081*SL	0.21 + 0.078*SL	0.21 + 0.079*SL
D2 to Y	t_{PLH}	0.75	0.67 + 0.042*SL	0.69 + 0.036*SL	0.70 + 0.034*SL
	t_{PHL}	0.84	0.72 + 0.059*SL	0.75 + 0.050*SL	0.78 + 0.046*SL
	t_R	0.30	0.17 + 0.067*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.37	0.21 + 0.081*SL	0.21 + 0.078*SL	0.21 + 0.079*SL
D3 to Y	t_{PLH}	0.76	0.67 + 0.042*SL	0.69 + 0.036*SL	0.71 + 0.034*SL
	t_{PHL}	0.84	0.72 + 0.059*SL	0.75 + 0.050*SL	0.78 + 0.046*SL
	t_R	0.30	0.17 + 0.066*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.37	0.21 + 0.080*SL	0.21 + 0.078*SL	0.21 + 0.079*SL
D4 to Y	t_{PLH}	0.74	0.66 + 0.042*SL	0.67 + 0.036*SL	0.69 + 0.034*SL
	t_{PHL}	0.84	0.72 + 0.059*SL	0.75 + 0.050*SL	0.78 + 0.046*SL
	t_R	0.30	0.17 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.36	0.20 + 0.080*SL	0.21 + 0.078*SL	0.20 + 0.079*SL
D5 to Y	t_{PLH}	0.74	0.65 + 0.041*SL	0.67 + 0.036*SL	0.69 + 0.034*SL
	t_{PHL}	0.84	0.72 + 0.059*SL	0.75 + 0.050*SL	0.77 + 0.046*SL
	t_R	0.30	0.17 + 0.067*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.36	0.20 + 0.080*SL	0.21 + 0.078*SL	0.20 + 0.079*SL
D6 to Y	t_{PLH}	0.73	0.64 + 0.042*SL	0.66 + 0.036*SL	0.68 + 0.034*SL
	t_{PHL}	0.82	0.70 + 0.059*SL	0.73 + 0.050*SL	0.76 + 0.046*SL
	t_R	0.30	0.16 + 0.068*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.37	0.21 + 0.081*SL	0.21 + 0.078*SL	0.20 + 0.079*SL
D7 to Y	t_{PLH}	0.73	0.64 + 0.042*SL	0.66 + 0.035*SL	0.67 + 0.034*SL
	t_{PHL}	0.82	0.71 + 0.059*SL	0.73 + 0.050*SL	0.76 + 0.046*SL
	t_R	0.30	0.16 + 0.068*SL	0.17 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.36	0.20 + 0.081*SL	0.21 + 0.078*SL	0.20 + 0.079*SL
S0 to Y	t_{PLH}	1.40	1.32 + 0.042*SL	1.34 + 0.036*SL	1.35 + 0.034*SL
	t_{PHL}	1.36	1.24 + 0.059*SL	1.27 + 0.049*SL	1.30 + 0.046*SL
	t_R	0.30	0.16 + 0.067*SL	0.16 + 0.068*SL	0.15 + 0.070*SL
	t_F	0.36	0.20 + 0.080*SL	0.21 + 0.078*SL	0.20 + 0.080*SL
S1 to Y	t_{PLH}	0.79	0.71 + 0.041*SL	0.72 + 0.036*SL	0.74 + 0.034*SL
	t_{PHL}	0.75	0.63 + 0.059*SL	0.66 + 0.050*SL	0.69 + 0.046*SL
	t_R	0.30	0.16 + 0.067*SL	0.16 + 0.068*SL	0.14 + 0.070*SL
	t_F	0.36	0.20 + 0.081*SL	0.21 + 0.078*SL	0.20 + 0.079*SL
S2 to Y	t_{PLH}	0.44	0.36 + 0.040*SL	0.37 + 0.035*SL	0.39 + 0.034*SL
	t_{PHL}	0.54	0.43 + 0.058*SL	0.45 + 0.050*SL	0.48 + 0.046*SL
	t_R	0.28	0.15 + 0.069*SL	0.15 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.35	0.18 + 0.083*SL	0.19 + 0.079*SL	0.19 + 0.080*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 YMX8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.78	0.72 + 0.027*SL	0.74 + 0.022*SL	0.76 + 0.019*SL
	t_{PHL}	0.87	0.79 + 0.038*SL	0.81 + 0.031*SL	0.84 + 0.026*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.31	0.23 + 0.044*SL	0.24 + 0.040*SL	0.25 + 0.038*SL
D1 to Y	t_{PLH}	0.78	0.72 + 0.027*SL	0.74 + 0.022*SL	0.76 + 0.019*SL
	t_{PHL}	0.87	0.79 + 0.038*SL	0.81 + 0.031*SL	0.84 + 0.026*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.31	0.23 + 0.044*SL	0.24 + 0.040*SL	0.25 + 0.038*SL
D2 to Y	t_{PLH}	0.77	0.72 + 0.027*SL	0.73 + 0.022*SL	0.75 + 0.019*SL
	t_{PHL}	0.86	0.78 + 0.037*SL	0.80 + 0.031*SL	0.83 + 0.026*SL
	t_R	0.24	0.17 + 0.034*SL	0.17 + 0.035*SL	0.18 + 0.033*SL
	t_F	0.32	0.23 + 0.044*SL	0.24 + 0.040*SL	0.25 + 0.038*SL
D3 to Y	t_{PLH}	0.77	0.72 + 0.026*SL	0.73 + 0.022*SL	0.75 + 0.019*SL
	t_{PHL}	0.86	0.78 + 0.038*SL	0.80 + 0.031*SL	0.84 + 0.026*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.31	0.22 + 0.044*SL	0.24 + 0.040*SL	0.25 + 0.038*SL
D4 to Y	t_{PLH}	0.76	0.70 + 0.026*SL	0.72 + 0.022*SL	0.74 + 0.019*SL
	t_{PHL}	0.85	0.78 + 0.038*SL	0.80 + 0.031*SL	0.83 + 0.026*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.31	0.22 + 0.044*SL	0.23 + 0.040*SL	0.25 + 0.038*SL
D5 to Y	t_{PLH}	0.75	0.70 + 0.026*SL	0.72 + 0.022*SL	0.73 + 0.019*SL
	t_{PHL}	0.85	0.78 + 0.037*SL	0.80 + 0.031*SL	0.83 + 0.026*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.18 + 0.033*SL
	t_F	0.31	0.22 + 0.044*SL	0.23 + 0.040*SL	0.25 + 0.038*SL
D6 to Y	t_{PLH}	0.74	0.69 + 0.027*SL	0.71 + 0.021*SL	0.72 + 0.019*SL
	t_{PHL}	0.84	0.76 + 0.037*SL	0.78 + 0.031*SL	0.82 + 0.026*SL
	t_R	0.24	0.17 + 0.034*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.31	0.22 + 0.044*SL	0.23 + 0.040*SL	0.25 + 0.038*SL
D7 to Y	t_{PLH}	0.74	0.69 + 0.026*SL	0.71 + 0.021*SL	0.72 + 0.019*SL
	t_{PHL}	0.84	0.76 + 0.038*SL	0.79 + 0.031*SL	0.82 + 0.026*SL
	t_R	0.24	0.17 + 0.034*SL	0.17 + 0.034*SL	0.17 + 0.034*SL
	t_F	0.31	0.22 + 0.044*SL	0.24 + 0.040*SL	0.25 + 0.038*SL
S0 to Y	t_{PLH}	1.42	1.37 + 0.026*SL	1.38 + 0.022*SL	1.40 + 0.019*SL
	t_{PHL}	1.38	1.30 + 0.037*SL	1.32 + 0.031*SL	1.35 + 0.026*SL
	t_R	0.23	0.16 + 0.035*SL	0.17 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.31	0.22 + 0.044*SL	0.24 + 0.040*SL	0.25 + 0.038*SL
S1 to Y	t_{PLH}	0.81	0.75 + 0.026*SL	0.77 + 0.021*SL	0.78 + 0.019*SL
	t_{PHL}	0.77	0.69 + 0.037*SL	0.71 + 0.031*SL	0.75 + 0.026*SL
	t_R	0.23	0.16 + 0.035*SL	0.16 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.31	0.22 + 0.044*SL	0.24 + 0.040*SL	0.25 + 0.038*SL
S2 to Y	t_{PLH}	0.45	0.40 + 0.026*SL	0.41 + 0.021*SL	0.43 + 0.019*SL
	t_{PHL}	0.55	0.48 + 0.038*SL	0.50 + 0.031*SL	0.53 + 0.026*SL
	t_R	0.22	0.15 + 0.035*SL	0.15 + 0.035*SL	0.16 + 0.034*SL
	t_F	0.30	0.21 + 0.044*SL	0.22 + 0.041*SL	0.24 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

Input/Output Cells 4

Contents

Overview 4-1
Summary Tables 4-2
Input Buffers 4-8
Output Buffers 4-23
Bi-Directional Buffers 4-97
Input Clock Drivers 4-99
Oscillators 4-122
PCI Buffers 4-145
PCMCIA Buffers 4-152
CardBus I/O Buffers 4-159
USB I/O Buffers 4-168
Voltage Detector 4-173
Power Pads 4-174

OVERVIEW

The fourth chapter describes various kinds of Input/Output cells (5V/3.3V, normal and interface operations) in STD80/STDM80 libraries.

The switching characteristics of each cell are attached to its basic cell information. The AC characteristics of bi-directional buffers are not included in this data sheet, however, they can be derived from different combinations of input and output buffers.

There are so many possible combinations of input/output cells, therefore, the naming conventions are adopted to help you memorize and use this cell library efficiently. You can refer to the naming conventions contained in “Summary Tables” section.

The “Summary Tables” section shows the list of 5V and 3.3V I/O cells separated by the category (input, output, bi-directional, etc.), and the more detailed description tables can be found on the leading part of each category.

SUMMARY TABLES

Input Buffers

Cell Type	Cell Name	STD80	STDM80	Page
CMOS Level	PIC/PICD/PICU	o	o	4-9
	PHIC/PHICD/PHICU	–	o	
	PLIC/PLICD/PLICU	o	–	
TTL Schmitt Trigger Level	PIL/PILD/PILU	o	–	4-13
	PHIL/PHILD/PHILU	–	o	
CMOS Schmitt Trigger Level	PIS/PISD/PISU	o	o	4-16
	PHIS/PHISD/PHISU	–	o	
	PLIS/PLISD/PLISU	o	–	
TTL Level	PIT/PITD/PITU	o	–	4-20
	PHIT/PHITD/PHITU	–	o	

<Naming Convention of Input Buffers>

P v l a b			
v		**a**	
None	Normal operation	C	CMOS level
H	5V interface in STDM80	L	TTL Schmitt trigger level
L	3.3V interface in STD80	S	CMOS Schmitt trigger level
b		T	TTL level
None	No resistor		
D	Pull-down resistor		
U	Pull-up resistor		

Output Buffers

Cell Type	Cell Name	Current Drive (mA)		Page
		STD80	STDM80	
Normal	POBy	1/2/4/8/12/16/20/24	1/2/4/6/8/10/12/16	4-24
	POBySH	12/16/20/24	–	
	POBySM	4/8/12/16/20/24	4/6/8/10/12/16	
	PHOBy	–	1/2/4/8/12/16/20/24	
	PHOBySH	–	12/16/20/24	
	PHOBySM	–	4/8/12/16/20/24	
	PLOBy	1/2/4/6/8/10/12/16	–	
	PLOBySM	4/6/8/10/12/16	–	

Cell Type	Cell Name	Current Drive (mA)		Page
		STD80	STDM80	
Open Drain	PODy	1/2/4/8/12/16/20/24	1/2/4/6/8/10/12/16	4-41
	PODySH	12/16/20/24	–	
	PODySM	4/8/12/16/20/24	4/6/8/10/12/16	
	PHODy	–	1/2/4/8/12/16/20/24	
	PHODySH	–	12/16/20/24	
	PHODySM	–	4/8/12/16/20/24	
	PLODy	1/2/4/6/8/10/12/16	–	
	PLODySM	4/6/8/10/12/16	–	
Tri-State	POTy	1/2/4/8/12/16/20/24	1/2/4/6/8/10/12/16	4-64
	POTySH	12/16/20/24	–	
	POTySM	4/8/12/16/20/24	4/6/8/10/12/16	
	PHOTy	–	1/2/4/8/12/16/20/24	
	PHOTySH	–	12/16/20/24	
	PHOTySM	–	4/8/12/16/20/24	
	PLOTy	1/2/4/6/8/10/12/16	–	
	PLOTySM	4/6/8/10/12/16	–	

<Naming Convention of Output Buffers>

P v O x y z			
v		**y**	
None	Normal operation	1	1mA drive
H	5V interface in STDM80	2	2mA drive
L	3.3V interface in STD80	4	4mA drive
x		6	6mA drive
B	Normal buffer	8	8mA drive
D	Open drain buffer	10	10mA drive
T	Tri-state buffer	12	12mA drive
z		16	16mA drive
None	No slew-rate control	20	20mA drive
SH	High slew-rate control	24	24mA drive
SM	Medium slew-rate control		

Bi-Directional Buffers

Cell Type	Cell Name	STD80	STDM80	Page
Open Drain	PBaDyz/PBaUDyz	o	o	4-98
	PHBaDyz/PHBaUDyz	–	o	
	PLBaDyz/PLBaUDyz	o	–	
Tri-State	PBaTyz/PBaDTyz/PBaUTyz	o	o	
	PHBaTyz/PHBaDTyz/PHBaUTyz	–	o	
	PLBaTyz/PLBaDTyz/PLBaUTyz	o	–	

<Naming Convention of Bi-Directional Buffers>

P v B a b x y z			
v		**a**	
None	Normal operation	C	CMOS level
H	5V interface in STDM80	L	TTL Schmitt trigger level
L	3.3V interface in STD80	S	CMOS Schmitt trigger level
b		T	TTL level
None	No resistor	**y**	
D	Pull-down resistor	1	1mA drive
U	Pull-up resistor	2	2mA drive
x		4	4mA drive
D	Open drain buffer	6	6mA drive
T	Tri-state buffer	8	8mA drive
z		10	10mA drive
None	No slew-rate control	12	12mA drive
SH	High slew-rate control	16	16mA drive
SM	Medium slew-rate control	20	20mA drive
		24	24mA drive

Input Clock Drivers

Cell Type	Cell Name	Current Drive (mA)		Page
		STD80	STDM80	
CMOS Level	PSCKDCy	2/4/8/12	2/4/6/8	4-100
	PSCKDCDy	2/4/8/12	2/4/6/8	
	PSCKDCUy	2/4/8/12	2/4/6/8	
TTL Schmitt Trigger Level	PSCKDLy	2/4/8/12	–	4-107
	PSCKDLDy	2/4/8/12	–	
	PSCKDLUy	2/4/8/12	–	
CMOS Schmitt Trigger Level	PSCKDSy	2/4/8/12	2/4/6/8	4-111
	PSCKDSDy	2/4/8/12	2/4/6/8	
	PSCKDSUy	2/4/8/12	2/4/6/8	
TTL Level	PSCKDTy	2/4/8/12	–	4-118
	PSCKDTDy	2/4/8/12	–	
	PSCKDTUy	2/4/8/12	–	

<Naming Convention of Input Clock Drivers>

PSCKD a b y			
a		**y**	
C	CMOS level	2	2mA drive
L	TTL Schmitt trigger level	4	4mA drive
S	CMOS Schmitt trigger level	6	6mA drive
T	TTL level	8	8mA drive
b		12	12mA drive
None	No resistor		
D	Pull-down resistor		
U	Pull-up resistor		

Oscillators

Cell Type	Cell Name		Page
	STD80	STDM80	
Oscillator	PSOSCK(1/2) PSOSCK(16/26)	PSOSCK(1/2) PSOSCK(16/26)	4-123
	PSOSCM(1/2/3/4/5/6) PSOSCM(16/26/36/46/56/66)	PSOSCM(1/2/3/4/5/6) PSOSCM(16/26/36/46/56/66)	4-132

PCI Buffers

Cell Type	Cell Name		Page
	STD80	STDM80	
PCI Input	PSIPCIA/PLSIPCIA	PSIPCIA3/PHSIPCIA	4-148
PCI Output	PSOPCIA/PLSOPCIA	PSOPCIA3/PHSOPCIA	4-149
Universal PCI Input	PSIPCIAU	PSIPCIAU	4-150
Universal PCI Output	PSOPCIAU	PSOPCIAU	4-151

PCMCIA Buffers

Cell Type	Cell Name	Page
PCMCIA Input	PVIC(5/3)	4-155
	PVIL/PVILD/PVILU(5/3)	
	PVIT/PVITD/PITU(5/3)	
PCMCIA Output	PVOB4/PVOB8/PVOB12(5/3)	4-156
	PVOD4/PVOD8/PVOD12(5/3)	
	PVOT4/PVOT8/PVOT12(5/3)	4-157
	PVOT8SM/PVOT12SM(5/3)	
PCMCIA Bi-Directional	PVBTT4/PVBTT8/PVBTT12(5/3)	4-158
	PVBTDT8SM/PVBCT8SM(5/3)	

CardBus I/O Buffers

Cell Type	Cell Name		Page
	STD80	STDM80	
CardBus Input	PLITCBU	PITCBU	4-162
CardBus Output	PLOTCBU/ PLOTCCKCBU/ PLOTCVSCBU	POTCBU/ POTCCKCBU/ POTCVSCBU	4-163
	PLODCCKCBU	PODCCKCBU	4-164
CardBus Bi-Directional	PLBTTCBU/ PLBTCCKCBU/ PLBTCVSCBU	PBTTCBU/ PBTCCKCBU/ PBTCVSCBU	4-165
	PLBDCCKCBU	PBDCCKCBU	4-166
Level Shifter	PLSCB	PLSCB	4-167

USB I/O Buffers

Cell Type	Cell Name		Page
	STD80	STDM80	
USB	PBUSB/PBUSB1	PBUSB/PBUSB1	4-170

Voltage Detector

Cell Type	Cell Name	Page
Voltage Detector	VDET	4-173

Power Pads

Cell Type	Cell Name		Page
	STD80	STDM80	
5V VDD	VDD5(I/P/O/IP/OI/OP/T)	VDD5(P/O/OP)	4-174
3.3V VDD	VDD3(P/O/OP)	VDD3(I/P/O/IP/OI/OP/T)	
5V VSS	VSS5(I/P/O/IP/OI/OP/T)	VSS5(P/O/OP)	
3.3V VSS	VSS3(P/O/OP)	VSS3(I/P/O/IP/OI/OP/T)	

INPUT BUFFERS

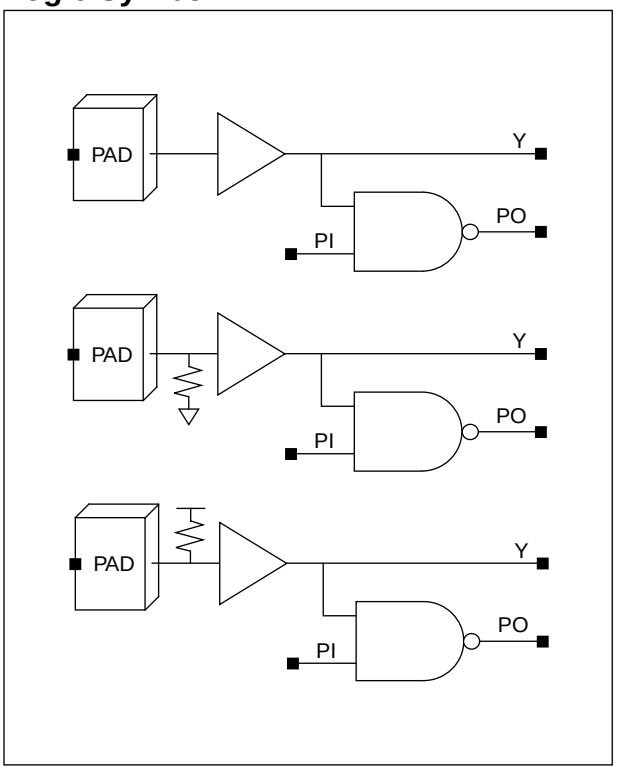
Cell List

Cell Name	Function Description
STD80	
PIC/PICD/PICU	5V CMOS Level Input Buffers
PIL/PILD/PILU	5V TTL Schmitt Trigger Level Input Buffers
PIS/PISD/PISU	5V CMOS Schmitt Trigger Level Input Buffers
PIT/PITD/PITU	5V TTL Level Input Buffers
PLIC/PLICD/PLICU	3.3V Interface CMOS Level Input Buffers
PLIS/PLISD/PLISU	3.3V Interface CMOS Schmitt Trigger Level Input Buffers
STDM80	
PIC/PICD/PICU	3.3V CMOS Level Input Buffers
PIS/PISD/PISU	3.3V CMOS Schmitt Trigger Level Input Buffers
PHIC/PHICD/PHICU	5V Interface CMOS Level Input Buffers
PHIL/PHILD/PHILU	5V Interface TTL Schmitt Trigger Level Input Buffers
PHIS/PHISD/PHISU	5V Interface CMOS Schmitt Trigger Level Input Buffers
PHIT/PHITD/PHITU	5V Interface TTL Level Input Buffers

Cell Availability

Library	5V Operation	3.3V Operation
STD80	PIC/PICD/PICU	PLIC/PLICD/PLICU
STDM80	PHIC/PHICD/PHICU	PIC/PICD/PICU

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Input Load (SL)

STD80	
	PI
PIC/PICD/PICU	1.6
PLIC/PLICD/PLICU	1.2
STDM80	
	PI
PIC/PICD/PICU	1.9
PHIC/PHICD/PHICU	1.4

I/O Slot

STD80/STDM80	
PvIC/PvICD/PvICU	1.0

NOTES:

1. STD80 3.3V interface input buffers (PLIC/PLICD/PLICU) are not available to receive input signals from 5V devices.
2. Fail-safe input buffers are available to receive signals from 5V devices without reducing reliability. However, if you want to use fail-safe input buffers, please contact to SEC ASIC first.

STD80 PIC Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.23	0.21 + 0.009*SL	0.22 + 0.008*SL	0.22 + 0.008*SL
	t_{PHL}	0.24	0.21 + 0.011*SL	0.21 + 0.010*SL	0.22 + 0.010*SL
	t_R	0.13	0.10 + 0.014*SL	0.10 + 0.014*SL	0.09 + 0.015*SL
	t_F	0.13	0.10 + 0.016*SL	0.10 + 0.018*SL	0.09 + 0.018*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STD80 PICD Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.24	0.23 + 0.008*SL	0.23 + 0.008*SL	0.23 + 0.008*SL
	t_{PHL}	0.24	0.22 + 0.011*SL	0.22 + 0.011*SL	0.22 + 0.010*SL
	t_R	0.13	0.10 + 0.013*SL	0.10 + 0.015*SL	0.09 + 0.016*SL
	t_F	0.13	0.10 + 0.015*SL	0.10 + 0.018*SL	0.09 + 0.018*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STD80 PICU Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.23	0.21 + 0.010*SL	0.22 + 0.008*SL	0.22 + 0.007*SL
	t_{PHL}	0.24	0.22 + 0.012*SL	0.22 + 0.010*SL	0.22 + 0.010*SL
	t_R	0.13	0.11 + 0.014*SL	0.11 + 0.014*SL	0.10 + 0.015*SL
	t_F	0.13	0.10 + 0.018*SL	0.10 + 0.017*SL	0.09 + 0.018*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STD80 PLIC Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.49	0.47 + 0.009*SL	0.48 + 0.007*SL	0.48 + 0.007*SL
	t_{PHL}	0.78	0.76 + 0.010*SL	0.76 + 0.012*SL	0.80 + 0.005*SL
	t_R	0.15	0.13 + 0.011*SL	0.12 + 0.012*SL	0.12 + 0.013*SL
	t_F	0.16	0.13 + 0.012*SL	0.13 + 0.014*SL	0.15 + 0.011*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STD80 PLICD Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.48	0.47 + 0.008*SL	0.47 + 0.007*SL	0.47 + 0.007*SL
	t_{PHL}	0.79	0.77 + 0.011*SL	0.76 + 0.012*SL	0.81 + 0.006*SL
	t_R	0.15	0.12 + 0.012*SL	0.12 + 0.012*SL	0.12 + 0.013*SL
	t_F	0.17	0.15 + 0.012*SL	0.15 + 0.012*SL	0.16 + 0.010*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

STD80 PLICU Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.49	0.48 + 0.008*SL	0.48 + 0.008*SL	0.49 + 0.006*SL
	t_{PHL}	0.78	0.76 + 0.011*SL	0.77 + 0.007*SL	0.74 + 0.011*SL
	t_R	0.15	0.12 + 0.013*SL	0.13 + 0.011*SL	0.11 + 0.014*SL
	t_F	0.17	0.15 + 0.012*SL	0.14 + 0.016*SL	0.19 + 0.009*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

STDM80 PIC Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.27	0.25 + 0.011*SL	0.25 + 0.009*SL	0.26 + 0.009*SL
	t_{PHL}	0.28	0.26 + 0.012*SL	0.26 + 0.010*SL	0.27 + 0.010*SL
	t_R	0.17	0.14 + 0.016*SL	0.13 + 0.019*SL	0.13 + 0.019*SL
	t_F	0.16	0.12 + 0.019*SL	0.11 + 0.023*SL	0.19 + 0.015*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

STDM80 PICD Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.26	0.24 + 0.007*SL	0.23 + 0.011*SL	0.26 + 0.009*SL
	t_{PHL}	0.29	0.26 + 0.013*SL	0.27 + 0.011*SL	0.27 + 0.010*SL
	t_R	0.18	0.14 + 0.019*SL	0.15 + 0.016*SL	0.11 + 0.020*SL
	t_F	0.17	0.13 + 0.020*SL	0.13 + 0.018*SL	0.11 + 0.019*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

STDM80 PICU Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.28	0.25 + 0.011*SL	0.26 + 0.009*SL	0.26 + 0.009*SL
	t_{PHL}	0.29	0.27 + 0.009*SL	0.26 + 0.011*SL	0.27 + 0.010*SL
	t_R	0.17	0.14 + 0.016*SL	0.13 + 0.018*SL	0.11 + 0.019*SL
	t_F	0.17	0.12 + 0.022*SL	0.13 + 0.021*SL	0.19 + 0.015*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PHIC Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.43	0.42 + 0.010*SL	0.42 + 0.009*SL	0.43 + 0.008*SL
	t_{PHL}	0.63	0.63 + 0.003*SL	0.60 + 0.012*SL	0.64 + 0.008*SL
	t_R	0.16	0.11 + 0.022*SL	0.13 + 0.017*SL	0.13 + 0.017*SL
	t_F	0.20	0.17 + 0.012*SL	0.17 + 0.014*SL	0.18 + 0.012*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PHICD Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.44	0.43 + 0.005*SL	0.42 + 0.009*SL	0.44 + 0.007*SL
	t_{PHL}	0.64	0.63 + 0.004*SL	0.61 + 0.012*SL	0.64 + 0.009*SL
	t_R	0.15	0.13 + 0.013*SL	0.12 + 0.017*SL	0.12 + 0.017*SL
	t_F	0.20	0.17 + 0.014*SL	0.17 + 0.014*SL	0.17 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PHICU Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

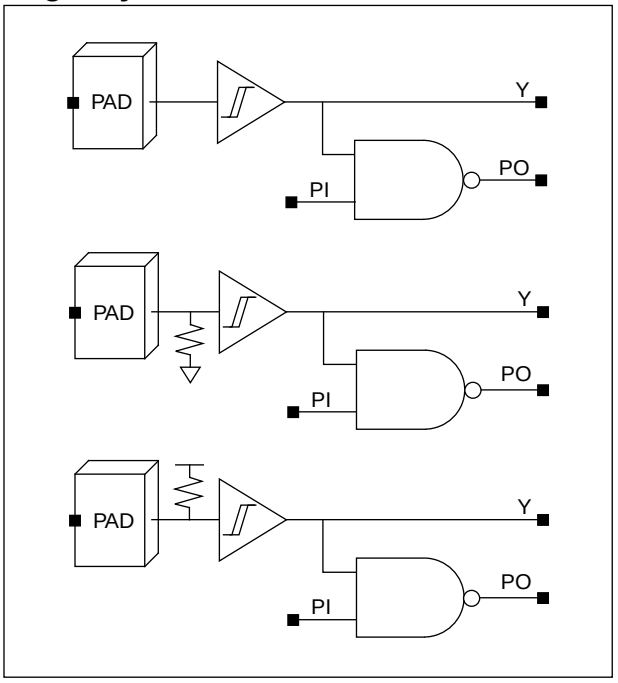
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.44	0.42 + 0.009*SL	0.42 + 0.009*SL	0.43 + 0.008*SL
	t_{PHL}	0.64	0.63 + 0.002*SL	0.61 + 0.013*SL	0.65 + 0.008*SL
	t_R	0.15	0.12 + 0.016*SL	0.11 + 0.019*SL	0.15 + 0.015*SL
	t_F	0.20	0.16 + 0.018*SL	0.18 + 0.013*SL	0.16 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Cell Availability

Library	5V Operation	3.3V Operation
STD80	PIL/PILD/PILU	–
STDM80	PHIL/PHILD/PHILU	–

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Input Load (SL)

STD80	
	PI
PIL/PILD/PILU	1.6
STDM80	
	PI
PHIL/PHILD/PHILU	1.4

I/O Slot

STD80/STDM80	
PvIL/PvILD/PvILU	1.0

STD80 PIL Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.44	0.43 + 0.009*SL	0.43 + 0.008*SL	0.43 + 0.008*SL
	t_{PHL}	1.52	1.49 + 0.014*SL	1.49 + 0.013*SL	1.51 + 0.011*SL
	t_R	0.16	0.14 + 0.014*SL	0.13 + 0.015*SL	0.13 + 0.015*SL
	t_F	0.52	0.49 + 0.013*SL	0.50 + 0.011*SL	0.51 + 0.010*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STD80 PILD Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.46	0.44 + 0.009*SL	0.44 + 0.008*SL	0.44 + 0.008*SL
	t_{PHL}	1.53	1.50 + 0.014*SL	1.51 + 0.013*SL	1.52 + 0.011*SL
	t_R	0.17	0.14 + 0.014*SL	0.14 + 0.015*SL	0.14 + 0.015*SL
	t_F	0.52	0.50 + 0.012*SL	0.50 + 0.012*SL	0.51 + 0.010*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STD80 PILU Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.45	0.43 + 0.009*SL	0.43 + 0.008*SL	0.44 + 0.008*SL
	t_{PHL}	1.55	1.52 + 0.014*SL	1.53 + 0.013*SL	1.54 + 0.011*SL
	t_R	0.17	0.14 + 0.015*SL	0.14 + 0.014*SL	0.14 + 0.015*SL
	t_F	0.52	0.50 + 0.013*SL	0.50 + 0.012*SL	0.51 + 0.010*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STDM80 PHIL Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.53	0.51 + 0.009*SL	0.51 + 0.009*SL	0.51 + 0.008*SL
	t_{PHL}	2.21	2.19 + 0.010*SL	2.19 + 0.010*SL	2.21 + 0.008*SL
	t_R	0.15	0.12 + 0.016*SL	0.12 + 0.017*SL	0.11 + 0.017*SL
	t_F	0.20	0.15 + 0.024*SL	0.19 + 0.012*SL	0.11 + 0.019*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PHILD Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] (SL : Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.54	0.52 + 0.009*SL	0.52 + 0.008*SL	0.53 + 0.008*SL
	t_{PHL}	2.22	2.20 + 0.013*SL	2.21 + 0.010*SL	2.22 + 0.008*SL
	t_R	0.15	0.12 + 0.017*SL	0.12 + 0.016*SL	0.10 + 0.019*SL
	t_F	0.20	0.16 + 0.020*SL	0.18 + 0.012*SL	0.16 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PHILU Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] (SL : Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.53	0.51 + 0.009*SL	0.51 + 0.008*SL	0.52 + 0.008*SL
	t_{PHL}	2.24	2.22 + 0.013*SL	2.22 + 0.010*SL	2.24 + 0.009*SL
	t_R	0.15	0.12 + 0.017*SL	0.12 + 0.017*SL	0.10 + 0.018*SL
	t_F	0.22	0.19 + 0.016*SL	0.20 + 0.010*SL	0.16 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

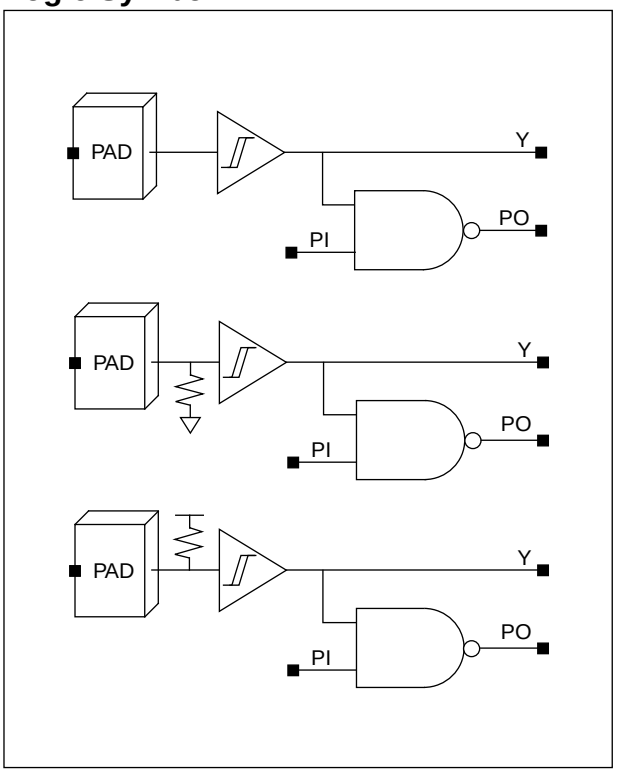
PvIS/PvISD/PvISU

CMOS Schmitt Trigger Level Input Buffers

Cell Availability

Library	5V Operation	3.3V Operation
STD80	PIS/PISD/PISU	PLIS/PLISD/PLISU
STDM80	PHIS/PHISD/PHISU	PIS/PISD/PISU

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Input Load (SL)

STD80	
	PI
PIS/PISD/PISU	1.6
PLIS/PLISD/PLISU	1.2
STDM80	
	PI
PIS/PISD/PISU	1.9
PHIS/PHISD/PHISU	1.2

I/O Slot

STD80/STDM80	
PvIS/PvISD/PvISU	1.0

NOTES:

1. STD80 3.3V interface input buffers (PLIS/PLISD/PLISU) are not available to receive input signals from 5V devices.
2. Fail-safe input buffers are available to receive signals from 5V devices without reducing reliability. However, if you want to use fail-safe input buffers, please contact to SEC ASIC first.

STD80 PIS Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.28	0.26 + 0.013*SL	0.26 + 0.011*SL	0.26 + 0.011*SL
	t_{PHL}	0.43	0.40 + 0.015*SL	0.40 + 0.013*SL	0.41 + 0.012*SL
	t_R	0.16	0.12 + 0.023*SL	0.12 + 0.022*SL	0.11 + 0.023*SL
	t_F	0.20	0.17 + 0.018*SL	0.17 + 0.017*SL	0.17 + 0.017*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STD80 PISD Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.29	0.27 + 0.012*SL	0.27 + 0.012*SL	0.27 + 0.011*SL
	t_{PHL}	0.44	0.41 + 0.015*SL	0.41 + 0.013*SL	0.42 + 0.012*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.023*SL	0.12 + 0.023*SL
	t_F	0.20	0.17 + 0.018*SL	0.17 + 0.017*SL	0.16 + 0.017*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STD80 PISU Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.29	0.26 + 0.013*SL	0.27 + 0.012*SL	0.27 + 0.011*SL
	t_{PHL}	0.44	0.40 + 0.015*SL	0.41 + 0.013*SL	0.42 + 0.012*SL
	t_R	0.16	0.12 + 0.023*SL	0.12 + 0.022*SL	0.11 + 0.023*SL
	t_F	0.20	0.17 + 0.018*SL	0.17 + 0.017*SL	0.17 + 0.017*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STD80 PLIS Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.75	0.73 + 0.008*SL	0.73 + 0.008*SL	0.74 + 0.006*SL
	t_{PHL}	1.63	1.61 + 0.010*SL	1.61 + 0.011*SL	1.65 + 0.006*SL
	t_R	0.15	0.13 + 0.013*SL	0.13 + 0.011*SL	0.11 + 0.014*SL
	t_F	0.17	0.12 + 0.023*SL	0.15 + 0.013*SL	0.18 + 0.009*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STD80 PLISD Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.77	0.75 + 0.008*SL	0.75 + 0.007*SL	0.76 + 0.007*SL
	t_{PHL}	1.65	1.63 + 0.011*SL	1.63 + 0.011*SL	1.66 + 0.007*SL
	t_R	0.15	0.13 + 0.012*SL	0.13 + 0.011*SL	0.11 + 0.013*SL
	t_F	0.17	0.15 + 0.014*SL	0.15 + 0.010*SL	0.15 + 0.011*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

STD80 PLISU Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.76	0.75 + 0.008*SL	0.75 + 0.007*SL	0.75 + 0.007*SL
	t_{PHL}	1.64	1.62 + 0.010*SL	1.62 + 0.012*SL	1.66 + 0.006*SL
	t_R	0.15	0.13 + 0.011*SL	0.13 + 0.012*SL	0.13 + 0.012*SL
	t_F	0.16	0.14 + 0.011*SL	0.13 + 0.013*SL	0.13 + 0.013*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

STDM80 PIS Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.51	0.50 + 0.009*SL	0.50 + 0.008*SL	0.51 + 0.007*SL
	t_{PHL}	1.11	1.09 + 0.012*SL	1.09 + 0.009*SL	1.11 + 0.008*SL
	t_R	0.25	0.22 + 0.018*SL	0.24 + 0.008*SL	0.20 + 0.012*SL
	t_F	0.34	0.32 + 0.010*SL	0.32 + 0.010*SL	0.32 + 0.010*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

STDM80 PISD Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.53	0.52 + 0.008*SL	0.52 + 0.008*SL	0.53 + 0.007*SL
	t_{PHL}	1.13	1.11 + 0.010*SL	1.11 + 0.010*SL	1.13 + 0.008*SL
	t_R	0.24	0.20 + 0.017*SL	0.22 + 0.011*SL	0.22 + 0.011*SL
	t_F	0.34	0.32 + 0.012*SL	0.32 + 0.010*SL	0.33 + 0.009*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

STDM80 PISU Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.53	0.51 + 0.009*SL	0.52 + 0.008*SL	0.53 + 0.007*SL
	t_{PHL}	1.12	1.10 + 0.011*SL	1.10 + 0.009*SL	1.12 + 0.008*SL
	t_R	0.23	0.22 + 0.008*SL	0.21 + 0.011*SL	0.21 + 0.011*SL
	t_F	0.36	0.34 + 0.010*SL	0.34 + 0.008*SL	0.33 + 0.010*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PHIS Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.55	0.53 + 0.009*SL	0.53 + 0.009*SL	0.54 + 0.008*SL
	t_{PHL}	1.07	1.06 + 0.005*SL	1.04 + 0.011*SL	1.07 + 0.009*SL
	t_R	0.16	0.11 + 0.022*SL	0.13 + 0.016*SL	0.13 + 0.016*SL
	t_F	0.19	0.17 + 0.014*SL	0.17 + 0.014*SL	0.17 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PHISD Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.55	0.53 + 0.009*SL	0.53 + 0.009*SL	0.53 + 0.008*SL
	t_{PHL}	1.08	1.06 + 0.009*SL	1.06 + 0.011*SL	1.08 + 0.009*SL
	t_R	0.15	0.12 + 0.014*SL	0.12 + 0.017*SL	0.09 + 0.019*SL
	t_F	0.19	0.17 + 0.015*SL	0.17 + 0.013*SL	0.16 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PHISU Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.56	0.54 + 0.009*SL	0.54 + 0.009*SL	0.54 + 0.008*SL
	t_{PHL}	1.08	1.06 + 0.009*SL	1.05 + 0.011*SL	1.08 + 0.009*SL
	t_R	0.16	0.11 + 0.023*SL	0.13 + 0.015*SL	0.09 + 0.019*SL
	t_F	0.20	0.17 + 0.013*SL	0.17 + 0.013*SL	0.16 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

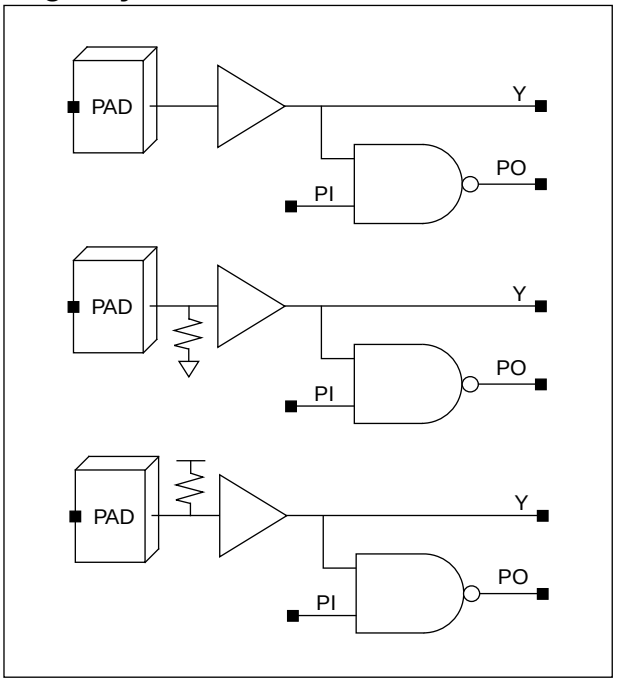
PvIT/PvITD/PvITU

TTL Level Input Buffers

Cell Availability

Library	5V Operation	3.3V Operation
STD80	PIT/PITD/PITU	–
STDM80	PHIT/PHITD/PHITU	–

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Input Load (SL)

STD80	
	PI
PIT/PITD/PITU	1.6
STDM80	
	PI
PHIT/PHITD/PHITU	1.4

I/O Slot

STD80/STDM80	
PvIT/PvITD/PvITU	1.0

STD80 PIT Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.25	0.23 + 0.011*SL	0.23 + 0.011*SL	0.23 + 0.011*SL
	t_{PHL}	0.32	0.30 + 0.011*SL	0.31 + 0.009*SL	0.32 + 0.008*SL
	t_R	0.15	0.11 + 0.023*SL	0.11 + 0.023*SL	0.10 + 0.024*SL
	t_F	0.17	0.15 + 0.010*SL	0.15 + 0.010*SL	0.15 + 0.009*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STD80 PITD Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.26	0.24 + 0.011*SL	0.24 + 0.011*SL	0.24 + 0.011*SL
	t_{PHL}	0.34	0.31 + 0.011*SL	0.32 + 0.009*SL	0.33 + 0.008*SL
	t_R	0.15	0.11 + 0.023*SL	0.11 + 0.023*SL	0.10 + 0.024*SL
	t_F	0.17	0.15 + 0.010*SL	0.15 + 0.010*SL	0.15 + 0.009*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STD80 PITU Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.25	0.23 + 0.011*SL	0.23 + 0.011*SL	0.23 + 0.011*SL
	t_{PHL}	0.33	0.31 + 0.011*SL	0.31 + 0.009*SL	0.32 + 0.007*SL
	t_R	0.15	0.11 + 0.024*SL	0.11 + 0.023*SL	0.10 + 0.024*SL
	t_F	0.17	0.15 + 0.009*SL	0.15 + 0.010*SL	0.15 + 0.009*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

STDM80 PHIT Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.25	0.23 + 0.009*SL	0.23 + 0.009*SL	0.23 + 0.008*SL
	t_{PHL}	0.93	0.91 + 0.007*SL	0.90 + 0.011*SL	0.93 + 0.008*SL
	t_R	0.17	0.16 + 0.004*SL	0.12 + 0.016*SL	0.11 + 0.017*SL
	t_F	0.20	0.17 + 0.012*SL	0.17 + 0.014*SL	0.15 + 0.016*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PHITD Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.27	0.26 + 0.009*SL	0.26 + 0.009*SL	0.26 + 0.008*SL
	t_{PHL}	0.93	0.92 + 0.006*SL	0.91 + 0.011*SL	0.94 + 0.009*SL
	t_R	0.16	0.13 + 0.014*SL	0.12 + 0.016*SL	0.11 + 0.017*SL
	t_F	0.20	0.17 + 0.017*SL	0.17 + 0.014*SL	0.17 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PHITU Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.25	0.23 + 0.009*SL	0.23 + 0.009*SL	0.23 + 0.008*SL
	t_{PHL}	0.93	0.92 + 0.008*SL	0.91 + 0.011*SL	0.94 + 0.008*SL
	t_R	0.17	0.16 + 0.004*SL	0.12 + 0.016*SL	0.11 + 0.018*SL
	t_F	0.20	0.17 + 0.013*SL	0.17 + 0.013*SL	0.15 + 0.015*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Cell List

Cell Name	Function Description
STD80	
POB(1/2/4/8/12/16/20/24)	5V Normal Output Buffers
POB(12/16/20/24)SH	5V Normal Output Buffers with High Slew-Rate
POB(4/8/12/16/20/24)SM	5V Normal Output Buffers with Medium Slew-Rate
POD(1/2/4/8/12/16/20/24)	5V Open Drain Output Buffers
POD(12/16/20/24)SH	5V Open Drain Output Buffers with High Slew-Rate
POD(4/8/12/16/20/24)SM	5V Open Drain Output Buffers with Medium Slew-Rate
POT(1/2/4/8/12/16/20/24)	5V Tri-State Output Buffers
POT(12/16/20/24)SH	5V Tri-State Output Buffers with High Slew-Rate
POT(4/8/12/16/20/24)SM	5V Tri-State Output Buffers with Medium Slew-Rate
PLOB(1/2/4/6/8/10/12/16)	3.3V Interface Normal Output Buffers
PLOB(4/6/8/10/12/16)SM	3.3V Interface Normal Output Buffers with Medium Slew-Rate
PLOD(1/2/4/6/8/10/12/16)	3.3V Interface Open Drain Output Buffers
PLOD(4/6/8/10/12/16)SM	3.3V Interface Open Drain Output Buffers with Medium Slew-Rate
PLOT(1/2/4/6/8/10/12/16)	3.3V Interface Tri-State Output Buffers
PLOT(4/6/8/10/12/16)SM	3.3V Interface Tri-State Output Buffers with Medium Slew-Rate
STDM80	
POB(1/2/4/6/8/10/12/16)	3.3V Normal Output Buffers
POB(4/6/8/10/12/16)SM	3.3V Normal Output Buffers with Medium Slew-Rate Control
POD(1/2/4/6/8/10/12/16)	3.3V Open Drain Output Buffers
POD(4/6/8/10/12/16)SM	3.3V Open Drain Output Buffers with Medium Slew-Rate Control
POT(1/2/4/6/8/10/12/16)	3.3V Tri-State Output Buffers
POT(4/6/8/10/12/16)SM	3.3V Tri-State Output Buffers with Medium Slew-Rate Control
PHOB(1/2/4/8/12/16/20/24)	5V Interface Normal Output Buffers
PHOB(12/16/20/24)SH	5V Interface Normal Output Buffers with High Slew-Rate Control
PHOB(4/8/12/16/20/24)SM	5V Interface Normal Output Buffers with Medium Slew-Rate Control
PHOD(1/2/4/8/12/16/20/24)	5V Interface Open Drain Output Buffers
PHOD(12/16/20/24)SH	5V Interface Open Drain Output Buffers with High Slew-Rate Control
PHOD(4/8/12/16/20/24)SM	5V Interface Open Drain Output Buffers with Medium Slew-Rate Control
PHOT(1/2/4/8/12/16/20/24)	5V Interface Tri-State Output Buffers
PHOT(12/16/20/24)SH	5V Interface Tri-State Output Buffers with High Slew-Rate Control
PHOT(4/8/12/16/20/24)SM	5V Interface Tri-State Output Buffers with Medium Slew-Rate Control

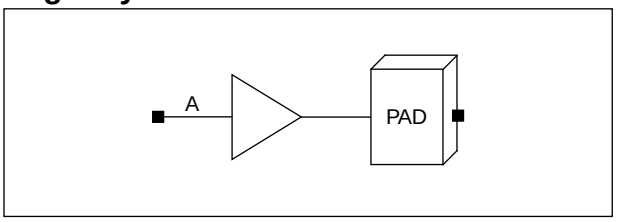
PvOByz

Normal Output Buffers

Cell Availability

Library	5V Operation	3.3V Operation
STD80	POB(1/2/4/8/12/16/20/24) POB(12/16/20/24)SH POB(4/8/12/16/20/24)SM	PLOB(1/2/4/6/8/10/12/16) PLOB(4/6/8/10/12/16)SM
STDM80	PHOB(1/2/4/8/12/16/20/24) PHOB(12/16/20/24)SH PHOB(4/8/12/16/20/24)SM	POB(1/2/4/6/8/10/12/16) POB(4/6/8/10/12/16)SM

Logic Symbol



Truth Table

A	PAD
0	0
1	1

I/O Slot

STD80/STDM80	
PvOByz	1.0

Input Load (SL)

STD80	
	A
POB(1/2/4/8/12/16)	5.5
POB20	9.5
POB24	10.2
POB12SH	20.6
POB16SH	20.0
POB(20/24)SH	10.44
POB4SM	21.3
POB(8/12)SM	20.6
POB16SM	20.0
POB(20/24)SM	11.7
PLOB(1/2/4/6/8/10/12/16)	2.3
PLOB(4/6/8/10/12/16)SM	2.3
STDM80	
	A
POB1	6.5
POB(2/12/16)	6.1
POB(4/6)	4.8
POB8	4.6
POB10	5.2
POB(4/6/8/10/12)SM	13.3
POB16SM	13.4
PHOB(1/2/4/8/12/16/20/24)	2.8
PHOB(12/16/20/24)SH	2.8
PHOB(4/8/12/16/20/24)SM	2.8

STD80 POB1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	14.98	0.36 + 0.292*CL	0.37 + 0.292*CL	0.37 + 0.292*CL
	t_{PHL}	12.03	0.39 + 0.233*CL	0.39 + 0.233*CL	0.39 + 0.233*CL
	t_R	33.59	0.59 + 0.660*CL	0.60 + 0.660*CL	0.59 + 0.660*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	7.60	0.30 + 0.146*CL	0.29 + 0.146*CL	0.30 + 0.146*CL
	t_{PHL}	6.13	0.31 + 0.116*CL	0.31 + 0.116*CL	0.31 + 0.116*CL
	t_R	16.81	0.31 + 0.330*CL	0.31 + 0.330*CL	0.31 + 0.330*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.242*CL	0.21 + 0.243*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.98	0.29 + 0.094*CL	0.29 + 0.094*CL	0.29 + 0.094*CL
	t_{PHL}	4.02	0.31 + 0.074*CL	0.30 + 0.074*CL	0.31 + 0.074*CL
	t_R	10.81	0.21 + 0.212*CL	0.21 + 0.212*CL	0.21 + 0.212*CL
	t_F	7.88	0.14 + 0.155*CL	0.15 + 0.155*CL	0.14 + 0.155*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.70	0.36 + 0.047*CL	0.36 + 0.047*CL	0.36 + 0.047*CL
	t_{PHL}	2.22	0.36 + 0.037*CL	0.36 + 0.037*CL	0.36 + 0.037*CL
	t_R	5.43	0.13 + 0.106*CL	0.13 + 0.106*CL	0.13 + 0.106*CL
	t_F	3.96	0.10 + 0.077*CL	0.09 + 0.077*CL	0.09 + 0.077*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.14	0.42 + 0.034*CL	0.42 + 0.034*CL	0.41 + 0.035*CL
	t_{PHL}	1.78	0.42 + 0.027*CL	0.42 + 0.027*CL	0.41 + 0.027*CL
	t_R	4.02	0.12 + 0.078*CL	0.12 + 0.078*CL	0.11 + 0.078*CL
	t_F	2.93	0.11 + 0.056*CL	0.10 + 0.057*CL	0.09 + 0.057*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.77	0.52 + 0.025*CL	0.52 + 0.025*CL	0.51 + 0.025*CL
	t_{PHL}	1.49	0.50 + 0.020*CL	0.50 + 0.020*CL	0.50 + 0.020*CL
	t_R	2.97	0.13 + 0.057*CL	0.12 + 0.057*CL	0.12 + 0.057*CL
	t_F	2.19	0.14 + 0.041*CL	0.13 + 0.041*CL	0.12 + 0.041*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB20 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.36	0.37 + 0.020*CL	0.37 + 0.020*CL	0.36 + 0.020*CL
	t_{PHL}	1.24	0.45 + 0.016*CL	0.45 + 0.016*CL	0.45 + 0.016*CL
	t_R	2.33	0.10 + 0.045*CL	0.08 + 0.045*CL	0.09 + 0.045*CL
	t_F	1.74	0.13 + 0.032*CL	0.12 + 0.032*CL	0.11 + 0.032*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB24 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.28	0.41 + 0.017*CL	0.41 + 0.017*CL	0.40 + 0.017*CL
	t_{PHL}	1.17	0.48 + 0.014*CL	0.48 + 0.014*CL	0.48 + 0.014*CL
	t_R	2.07	0.10 + 0.039*CL	0.09 + 0.039*CL	0.09 + 0.039*CL
	t_F	1.56	0.15 + 0.028*CL	0.14 + 0.028*CL	0.13 + 0.028*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB12SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.78	1.00 + 0.036*CL	1.02 + 0.035*CL	1.03 + 0.035*CL
	t_{PHL}	3.24	1.65 + 0.032*CL	1.76 + 0.030*CL	1.81 + 0.030*CL
	t_R	4.33	0.48 + 0.077*CL	0.44 + 0.078*CL	0.41 + 0.078*CL
	t_F	3.73	0.96 + 0.055*CL	0.97 + 0.055*CL	0.97 + 0.055*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB16SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.57	1.22 + 0.027*CL	1.28 + 0.026*CL	1.31 + 0.026*CL
	t_{PHL}	2.95	1.70 + 0.025*CL	1.82 + 0.024*CL	1.87 + 0.023*CL
	t_R	3.42	0.69 + 0.055*CL	0.66 + 0.055*CL	0.65 + 0.055*CL
	t_F	2.99	0.95 + 0.041*CL	1.01 + 0.040*CL	1.02 + 0.040*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB20SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.03	0.98 + 0.021*CL	1.03 + 0.020*CL	1.04 + 0.020*CL
	t_{PHL}	2.09	1.22 + 0.017*CL	1.26 + 0.017*CL	1.28 + 0.017*CL
	t_R	2.70	0.56 + 0.043*CL	0.53 + 0.043*CL	0.52 + 0.043*CL
	t_F	2.22	0.69 + 0.031*CL	0.68 + 0.031*CL	0.67 + 0.031*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB24SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.03	1.06 + 0.019*CL	1.12 + 0.019*CL	1.15 + 0.018*CL
	t_{PHL}	2.15	1.36 + 0.016*CL	1.40 + 0.015*CL	1.42 + 0.015*CL
	t_R	2.52	0.63 + 0.038*CL	0.63 + 0.038*CL	0.61 + 0.038*CL
	t_F	2.14	0.79 + 0.027*CL	0.79 + 0.027*CL	0.78 + 0.027*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB4SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.22	0.53 + 0.094*CL	0.53 + 0.094*CL	0.53 + 0.094*CL
	t_{PHL}	4.76	1.03 + 0.074*CL	1.04 + 0.074*CL	1.05 + 0.074*CL
	t_R	10.83	0.24 + 0.212*CL	0.23 + 0.212*CL	0.24 + 0.212*CL
	t_F	8.05	0.42 + 0.153*CL	0.37 + 0.153*CL	0.35 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB8SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.16	0.81 + 0.047*CL	0.82 + 0.047*CL	0.82 + 0.047*CL
	t_{PHL}	3.37	1.41 + 0.039*CL	1.48 + 0.038*CL	1.52 + 0.038*CL
	t_R	5.57	0.34 + 0.105*CL	0.29 + 0.105*CL	0.28 + 0.105*CL
	t_F	4.46	0.74 + 0.074*CL	0.72 + 0.075*CL	0.69 + 0.075*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB12SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.59	0.85 + 0.035*CL	0.87 + 0.035*CL	0.86 + 0.035*CL
	t_{PHL}	2.88	1.34 + 0.031*CL	1.44 + 0.029*CL	1.48 + 0.029*CL
	t_R	4.21	0.40 + 0.076*CL	0.36 + 0.077*CL	0.34 + 0.077*CL
	t_F	3.54	0.80 + 0.055*CL	0.82 + 0.055*CL	0.82 + 0.055*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB16SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.27	0.96 + 0.026*CL	1.00 + 0.026*CL	1.01 + 0.026*CL
	t_{PHL}	2.46	1.28 + 0.024*CL	1.36 + 0.022*CL	1.41 + 0.022*CL
	t_R	3.27	0.52 + 0.055*CL	0.49 + 0.055*CL	0.48 + 0.056*CL
	t_F	2.77	0.73 + 0.041*CL	0.77 + 0.040*CL	0.78 + 0.040*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB20SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.70	0.69 + 0.020*CL	0.70 + 0.020*CL	0.70 + 0.020*CL
	t_{PHL}	1.72	0.83 + 0.018*CL	0.88 + 0.017*CL	0.92 + 0.017*CL
	t_R	2.52	0.35 + 0.043*CL	0.33 + 0.044*CL	0.31 + 0.044*CL
	t_F	2.10	0.54 + 0.031*CL	0.55 + 0.031*CL	0.55 + 0.031*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POB24SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.68	0.77 + 0.018*CL	0.79 + 0.018*CL	0.81 + 0.018*CL
	t_{PHL}	1.74	0.91 + 0.017*CL	0.98 + 0.016*CL	1.02 + 0.015*CL
	t_R	2.31	0.42 + 0.038*CL	0.40 + 0.038*CL	0.39 + 0.038*CL
	t_F	2.01	0.62 + 0.028*CL	0.63 + 0.028*CL	0.64 + 0.027*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	21.37	0.92 + 0.409*CL	0.93 + 0.409*CL	0.92 + 0.409*CL
	t_{PHL}	13.83	0.63 + 0.264*CL	0.63 + 0.264*CL	0.63 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	10.45	0.80 + 0.193*CL	0.80 + 0.193*CL	0.80 + 0.193*CL
	t_{PHL}	6.71	0.54 + 0.124*CL	0.54 + 0.123*CL	0.53 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.52	0.70 + 0.096*CL	0.69 + 0.097*CL	0.70 + 0.096*CL
	t_{PHL}	3.66	0.58 + 0.062*CL	0.58 + 0.062*CL	0.58 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.16 + 0.133*CL	0.15 + 0.133*CL	0.16 + 0.133*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.98	0.76 + 0.064*CL	0.76 + 0.064*CL	0.76 + 0.064*CL
	t_{PHL}	2.73	0.69 + 0.041*CL	0.67 + 0.041*CL	0.67 + 0.041*CL
	t_R	7.52	0.20 + 0.146*CL	0.19 + 0.147*CL	0.20 + 0.146*CL
	t_F	4.58	0.17 + 0.088*CL	0.14 + 0.089*CL	0.13 + 0.089*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.24	0.84 + 0.048*CL	0.83 + 0.048*CL	0.83 + 0.048*CL
	t_{PHL}	2.33	0.81 + 0.030*CL	0.81 + 0.030*CL	0.79 + 0.031*CL
	t_R	5.66	0.18 + 0.110*CL	0.17 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.51	0.24 + 0.065*CL	0.22 + 0.066*CL	0.17 + 0.066*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB10 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.90	0.98 + 0.038*CL	0.97 + 0.039*CL	0.97 + 0.039*CL
	t_{PHL}	2.06	0.83 + 0.025*CL	0.83 + 0.025*CL	0.83 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.18 + 0.088*CL	0.16 + 0.088*CL
	t_F	2.83	0.21 + 0.052*CL	0.21 + 0.052*CL	0.17 + 0.053*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.72	1.11 + 0.032*CL	1.11 + 0.032*CL	1.11 + 0.032*CL
	t_{PHL}	1.94	0.90 + 0.021*CL	0.92 + 0.021*CL	0.92 + 0.021*CL
	t_R	3.84	0.20 + 0.073*CL	0.18 + 0.073*CL	0.18 + 0.073*CL
	t_F	2.43	0.27 + 0.043*CL	0.24 + 0.044*CL	0.24 + 0.044*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.49	1.28 + 0.024*CL	1.26 + 0.024*CL	1.27 + 0.024*CL
	t_{PHL}	1.86	1.04 + 0.016*CL	1.07 + 0.016*CL	1.08 + 0.016*CL
	t_R	3.00	0.25 + 0.055*CL	0.23 + 0.055*CL	0.24 + 0.055*CL
	t_F	1.98	0.36 + 0.033*CL	0.38 + 0.032*CL	0.32 + 0.033*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	6.25	1.29 + 0.099*CL	1.28 + 0.099*CL	1.29 + 0.099*CL
	t_{PHL}	4.16	0.97 + 0.064*CL	0.97 + 0.064*CL	0.98 + 0.064*CL
	t_R	11.58	0.28 + 0.226*CL	0.27 + 0.226*CL	0.28 + 0.226*CL
	t_F	7.10	0.26 + 0.137*CL	0.23 + 0.137*CL	0.22 + 0.137*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB6SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.76	1.48 + 0.066*CL	1.48 + 0.066*CL	1.48 + 0.066*CL
	t_{PHL}	3.43	1.31 + 0.042*CL	1.32 + 0.042*CL	1.32 + 0.042*CL
	t_R	7.71	0.27 + 0.149*CL	0.24 + 0.149*CL	0.25 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.41 + 0.089*CL	0.37 + 0.089*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.11	1.66 + 0.049*CL	1.66 + 0.049*CL	1.67 + 0.049*CL
	t_{PHL}	3.21	1.58 + 0.033*CL	1.63 + 0.032*CL	1.65 + 0.032*CL
	t_R	5.86	0.35 + 0.110*CL	0.30 + 0.111*CL	0.29 + 0.111*CL
	t_F	3.91	0.69 + 0.065*CL	0.65 + 0.065*CL	0.60 + 0.066*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB10SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.60	1.67 + 0.039*CL	1.67 + 0.039*CL	1.67 + 0.039*CL
	t_{PHL}	2.85	1.50 + 0.027*CL	1.57 + 0.026*CL	1.61 + 0.026*CL
	t_R	4.72	0.42 + 0.086*CL	0.36 + 0.087*CL	0.34 + 0.087*CL
	t_F	3.34	0.85 + 0.050*CL	0.78 + 0.051*CL	0.80 + 0.050*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.46	1.83 + 0.032*CL	1.85 + 0.032*CL	1.85 + 0.032*CL
	t_{PHL}	2.89	1.66 + 0.025*CL	1.77 + 0.023*CL	1.83 + 0.022*CL
	t_R	4.07	0.54 + 0.071*CL	0.46 + 0.072*CL	0.46 + 0.072*CL
	t_F	3.09	1.01 + 0.042*CL	1.04 + 0.041*CL	1.00 + 0.042*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOB16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.40	2.11 + 0.026*CL	2.17 + 0.025*CL	2.18 + 0.025*CL
	t_{PHL}	3.07	1.95 + 0.022*CL	2.09 + 0.020*CL	2.17 + 0.020*CL
	t_R	3.39	0.75 + 0.053*CL	0.68 + 0.054*CL	0.66 + 0.054*CL
	t_F	2.88	1.24 + 0.033*CL	1.35 + 0.031*CL	1.28 + 0.032*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	20.96	0.52 + 0.409*CL	0.52 + 0.409*CL	0.52 + 0.409*CL
	t_{PHL}	13.70	0.50 + 0.264*CL	0.50 + 0.264*CL	0.50 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	10.05	0.40 + 0.193*CL	0.40 + 0.193*CL	0.40 + 0.193*CL
	t_{PHL}	6.58	0.41 + 0.124*CL	0.41 + 0.124*CL	0.41 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.18	0.36 + 0.096*CL	0.36 + 0.096*CL	0.36 + 0.096*CL
	t_{PHL}	3.54	0.46 + 0.062*CL	0.46 + 0.062*CL	0.45 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.26 + 0.220*CL
	t_F	6.81	0.16 + 0.133*CL	0.15 + 0.133*CL	0.15 + 0.133*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.63	0.41 + 0.064*CL	0.41 + 0.064*CL	0.41 + 0.064*CL
	t_{PHL}	2.60	0.56 + 0.041*CL	0.55 + 0.041*CL	0.55 + 0.041*CL
	t_R	7.52	0.20 + 0.146*CL	0.19 + 0.147*CL	0.20 + 0.146*CL
	t_F	4.58	0.16 + 0.088*CL	0.15 + 0.089*CL	0.13 + 0.089*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.89	0.48 + 0.048*CL	0.48 + 0.048*CL	0.48 + 0.048*CL
	t_{PHL}	2.20	0.69 + 0.030*CL	0.68 + 0.030*CL	0.66 + 0.031*CL
	t_R	5.67	0.18 + 0.110*CL	0.16 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.51	0.24 + 0.065*CL	0.20 + 0.066*CL	0.19 + 0.066*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB10 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.50	0.58 + 0.038*CL	0.57 + 0.039*CL	0.57 + 0.039*CL
	t_{PHL}	1.94	0.71 + 0.025*CL	0.71 + 0.025*CL	0.71 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.17 + 0.088*CL	0.17 + 0.088*CL
	t_F	2.84	0.22 + 0.052*CL	0.21 + 0.052*CL	0.18 + 0.053*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.27	0.67 + 0.032*CL	0.67 + 0.032*CL	0.66 + 0.032*CL
	t_{PHL}	1.82	0.78 + 0.021*CL	0.78 + 0.021*CL	0.79 + 0.021*CL
	t_R	3.84	0.20 + 0.073*CL	0.19 + 0.073*CL	0.17 + 0.073*CL
	t_F	2.43	0.28 + 0.043*CL	0.25 + 0.043*CL	0.24 + 0.044*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.04	0.83 + 0.024*CL	0.83 + 0.024*CL	0.82 + 0.024*CL
	t_{PHL}	1.73	0.92 + 0.016*CL	0.94 + 0.016*CL	0.95 + 0.016*CL
	t_R	3.00	0.26 + 0.055*CL	0.23 + 0.055*CL	0.23 + 0.055*CL
	t_F	1.99	0.37 + 0.032*CL	0.37 + 0.032*CL	0.34 + 0.033*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.50	0.54 + 0.099*CL	0.54 + 0.099*CL	0.54 + 0.099*CL
	t_{PHL}	3.98	0.79 + 0.064*CL	0.78 + 0.064*CL	0.79 + 0.064*CL
	t_R	11.58	0.28 + 0.226*CL	0.27 + 0.226*CL	0.28 + 0.226*CL
	t_F	7.10	0.26 + 0.137*CL	0.24 + 0.137*CL	0.22 + 0.137*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB6SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.98	0.72 + 0.065*CL	0.69 + 0.066*CL	0.70 + 0.066*CL
	t_{PHL}	3.24	1.12 + 0.042*CL	1.14 + 0.042*CL	1.14 + 0.042*CL
	t_R	7.71	0.26 + 0.149*CL	0.26 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.41 + 0.089*CL	0.38 + 0.089*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.32	0.87 + 0.049*CL	0.87 + 0.049*CL	0.87 + 0.049*CL
	t_{PHL}	3.02	1.39 + 0.033*CL	1.43 + 0.032*CL	1.46 + 0.032*CL
	t_R	5.85	0.32 + 0.110*CL	0.29 + 0.111*CL	0.27 + 0.111*CL
	t_F	3.91	0.69 + 0.064*CL	0.62 + 0.065*CL	0.60 + 0.066*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB10SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.82	0.88 + 0.039*CL	0.89 + 0.039*CL	0.88 + 0.039*CL
	t_{PHL}	2.66	1.31 + 0.027*CL	1.38 + 0.026*CL	1.43 + 0.026*CL
	t_R	4.70	0.38 + 0.086*CL	0.33 + 0.087*CL	0.32 + 0.087*CL
	t_F	3.34	0.85 + 0.050*CL	0.79 + 0.051*CL	0.80 + 0.050*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.66	1.04 + 0.032*CL	1.06 + 0.032*CL	1.06 + 0.032*CL
	t_{PHL}	2.70	1.47 + 0.025*CL	1.58 + 0.023*CL	1.63 + 0.022*CL
	t_R	4.05	0.50 + 0.071*CL	0.45 + 0.072*CL	0.42 + 0.072*CL
	t_F	3.09	1.03 + 0.041*CL	1.02 + 0.041*CL	1.00 + 0.042*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POB16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.59	1.31 + 0.026*CL	1.35 + 0.025*CL	1.37 + 0.025*CL
	t_{PHL}	2.87	1.76 + 0.022*CL	1.89 + 0.020*CL	1.98 + 0.020*CL
	t_R	3.36	0.70 + 0.053*CL	0.66 + 0.054*CL	0.66 + 0.054*CL
	t_F	2.88	1.25 + 0.033*CL	1.30 + 0.032*CL	1.31 + 0.032*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	15.36	0.75 + 0.292*CL	0.75 + 0.292*CL	0.75 + 0.292*CL
	t_{PHL}	12.37	0.73 + 0.233*CL	0.61 + 0.234*CL	0.83 + 0.232*CL
	t_R	33.59	0.59 + 0.660*CL	0.59 + 0.660*CL	0.59 + 0.660*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	7.99	0.68 + 0.146*CL	0.68 + 0.146*CL	0.68 + 0.146*CL
	t_{PHL}	6.46	0.61 + 0.117*CL	0.65 + 0.116*CL	0.75 + 0.115*CL
	t_R	16.81	0.31 + 0.330*CL	0.31 + 0.330*CL	0.31 + 0.330*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.243*CL	0.21 + 0.243*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.37	0.68 + 0.094*CL	0.68 + 0.094*CL	0.68 + 0.094*CL
	t_{PHL}	4.35	0.64 + 0.074*CL	0.64 + 0.074*CL	0.56 + 0.075*CL
	t_R	10.81	0.21 + 0.212*CL	0.22 + 0.212*CL	0.21 + 0.212*CL
	t_F	7.88	0.14 + 0.155*CL	0.14 + 0.155*CL	0.15 + 0.155*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.09	0.75 + 0.047*CL	0.74 + 0.047*CL	0.75 + 0.047*CL
	t_{PHL}	2.56	0.70 + 0.037*CL	0.70 + 0.037*CL	0.76 + 0.036*CL
	t_R	5.43	0.13 + 0.106*CL	0.12 + 0.106*CL	0.13 + 0.106*CL
	t_F	3.96	0.09 + 0.077*CL	0.10 + 0.077*CL	0.10 + 0.077*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.53	0.81 + 0.034*CL	0.81 + 0.034*CL	0.81 + 0.035*CL
	t_{PHL}	2.11	0.73 + 0.028*CL	0.76 + 0.027*CL	0.81 + 0.027*CL
	t_R	4.02	0.12 + 0.078*CL	0.12 + 0.078*CL	0.11 + 0.078*CL
	t_F	2.93	0.11 + 0.056*CL	0.12 + 0.056*CL	0.08 + 0.057*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.16	0.91 + 0.025*CL	0.91 + 0.025*CL	0.91 + 0.025*CL
	t_{PHL}	1.83	0.83 + 0.020*CL	0.77 + 0.021*CL	0.88 + 0.019*CL
	t_R	2.97	0.14 + 0.057*CL	0.12 + 0.057*CL	0.11 + 0.057*CL
	t_F	2.20	0.15 + 0.041*CL	0.14 + 0.041*CL	0.14 + 0.041*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB20 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.90	0.91 + 0.020*CL	0.90 + 0.020*CL	0.91 + 0.020*CL
	t_{PHL}	1.65	0.87 + 0.016*CL	0.87 + 0.016*CL	0.86 + 0.016*CL
	t_R	2.34	0.11 + 0.045*CL	0.08 + 0.045*CL	0.10 + 0.045*CL
	t_F	1.75	0.15 + 0.032*CL	0.10 + 0.033*CL	0.13 + 0.032*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB24 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.85	0.99 + 0.017*CL	0.98 + 0.017*CL	0.98 + 0.017*CL
	t_{PHL}	1.60	0.91 + 0.014*CL	0.92 + 0.014*CL	0.91 + 0.014*CL
	t_R	2.08	0.12 + 0.039*CL	0.11 + 0.039*CL	0.08 + 0.040*CL
	t_F	1.57	0.17 + 0.028*CL	0.13 + 0.028*CL	0.13 + 0.028*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB12SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.76	1.98 + 0.036*CL	2.00 + 0.035*CL	2.01 + 0.035*CL
	t_{PHL}	3.90	2.31 + 0.032*CL	2.42 + 0.030*CL	2.47 + 0.030*CL
	t_R	4.37	0.54 + 0.077*CL	0.48 + 0.077*CL	0.46 + 0.078*CL
	t_F	3.74	0.96 + 0.056*CL	0.99 + 0.055*CL	0.98 + 0.055*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB16SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.54	2.19 + 0.027*CL	2.25 + 0.026*CL	2.28 + 0.026*CL
	t_{PHL}	3.60	2.35 + 0.025*CL	2.46 + 0.024*CL	2.52 + 0.023*CL
	t_R	3.47	0.76 + 0.054*CL	0.73 + 0.055*CL	0.69 + 0.055*CL
	t_F	3.00	0.96 + 0.041*CL	1.00 + 0.040*CL	1.04 + 0.040*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB20SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.62	1.56 + 0.021*CL	1.61 + 0.020*CL	1.63 + 0.020*CL
	t_{PHL}	2.54	1.67 + 0.017*CL	1.71 + 0.017*CL	1.73 + 0.017*CL
	t_R	2.73	0.60 + 0.043*CL	0.54 + 0.043*CL	0.56 + 0.043*CL
	t_F	2.23	0.71 + 0.031*CL	0.71 + 0.030*CL	0.65 + 0.031*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB24SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.62	1.65 + 0.019*CL	1.71 + 0.019*CL	1.73 + 0.018*CL
	t_{PHL}	2.60	1.81 + 0.016*CL	1.85 + 0.015*CL	1.86 + 0.015*CL
	t_R	2.54	0.67 + 0.037*CL	0.63 + 0.038*CL	0.65 + 0.038*CL
	t_F	2.15	0.82 + 0.027*CL	0.78 + 0.027*CL	0.80 + 0.027*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB4SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	6.14	1.45 + 0.094*CL	1.44 + 0.094*CL	1.46 + 0.094*CL
	t_{PHL}	5.43	1.71 + 0.074*CL	1.72 + 0.074*CL	1.72 + 0.074*CL
	t_R	10.84	0.25 + 0.212*CL	0.25 + 0.212*CL	0.24 + 0.212*CL
	t_F	8.06	0.43 + 0.153*CL	0.39 + 0.153*CL	0.36 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB8SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.12	1.77 + 0.047*CL	1.78 + 0.047*CL	1.78 + 0.047*CL
	t_{PHL}	4.04	2.08 + 0.039*CL	2.14 + 0.038*CL	2.18 + 0.038*CL
	t_R	5.60	0.38 + 0.104*CL	0.34 + 0.105*CL	0.32 + 0.105*CL
	t_F	4.47	0.74 + 0.074*CL	0.73 + 0.075*CL	0.69 + 0.075*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB12SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.54	1.79 + 0.035*CL	1.81 + 0.035*CL	1.82 + 0.035*CL
	t_{PHL}	3.53	2.00 + 0.031*CL	2.09 + 0.030*CL	2.13 + 0.029*CL
	t_R	4.25	0.46 + 0.076*CL	0.41 + 0.077*CL	0.40 + 0.077*CL
	t_F	3.56	0.83 + 0.055*CL	0.81 + 0.055*CL	0.83 + 0.055*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB16SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.19	1.87 + 0.026*CL	1.92 + 0.026*CL	1.93 + 0.026*CL
	t_{PHL}	3.10	1.91 + 0.024*CL	2.01 + 0.022*CL	2.05 + 0.022*CL
	t_R	3.32	0.59 + 0.055*CL	0.56 + 0.055*CL	0.53 + 0.055*CL
	t_F	2.78	0.74 + 0.041*CL	0.77 + 0.040*CL	0.80 + 0.040*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB20SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.35	1.33 + 0.020*CL	1.36 + 0.020*CL	1.36 + 0.020*CL
	t_{PHL}	2.19	1.30 + 0.018*CL	1.35 + 0.017*CL	1.39 + 0.017*CL
	t_R	2.54	0.39 + 0.043*CL	0.35 + 0.044*CL	0.33 + 0.044*CL
	t_F	2.12	0.56 + 0.031*CL	0.57 + 0.031*CL	0.56 + 0.031*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOB24SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

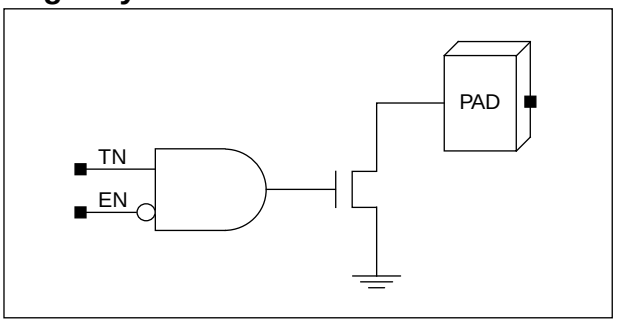
Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.33	1.42 + 0.018*CL	1.44 + 0.018*CL	1.47 + 0.018*CL
	t_{PHL}	2.21	1.38 + 0.017*CL	1.45 + 0.016*CL	1.48 + 0.015*CL
	t_R	2.34	0.46 + 0.038*CL	0.44 + 0.038*CL	0.42 + 0.038*CL
	t_F	2.02	0.65 + 0.028*CL	0.65 + 0.027*CL	0.66 + 0.027*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Cell Availability

Library	5V Operation	3.3V Operation
STD80	POD(1/2/4/8/12/16/20/24) POD(12/16/20/24)SH POD(4/8/12/16/20/24)SM	PLOD(1/2/4/6/8/10/12/16) PLOD(4/6/8/10/12/16)SM
STDM80	PHOD(1/2/4/8/12/16/20/24) PHOD(12/16/20/24)SH PHOD(4/8/12/16/20/24)SM	POD(1/2/4/6/8/10/12/16) POD(4/6/8/10/12/16)SM

Logic Symbol



NOTES:

1. STD80 standard open-drain output buffers, POD(1/2/4/8/12/16/20/24), cannot tolerate external pull-ups to more than 5.5V. And STDM80 standard open-drain output buffers, POD(1/2/4/6/8/10/12/16), cannot tolerate external pull-ups to more than 3.6V.
2. Fail-safe open-drain output buffers with external pull-ups to more than 5.5V (in case of STD80) / 3.6V (in case of STDM80) can drive signals to that voltage range. However, if you want to use fail-safe open-drains, please contact to SEC ASIC first.

I/O Slot

STD80/STDM80	
PvODyz	1.0

Truth Table

TN	EN	PAD
1	0	0
0	x	Hi-Z
x	1	Hi-Z

Input Load (SL)

STD80		
	TN	EN
POD(1/2/4/8/12/16/20/24)	1.4	1.6
POD(12/16/20/24)SH	1.4	1.6
POD(4/8/12/16/20/24)SM	1.4	1.6
PLOD(1/2/4/6/8/10/12/16)	1.2	1.2
PLOD(4/6/8/10/12/16)SM	1.2	1.2
STDM80		
	TN	EN
POD(1/2/4/6/8/10/12/16)	1.8	1.8
POD(4/6/8/10/12/16)SM	1.8	1.8
PHOD(1/2/4/8/12/16/20/24)	1.4	1.4
PHOD(12/16/20/24)SH	1.4	1.4
PHOD(4/8/12/16/20/24)SM	1.4	1.4

STD80 POD1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	12.21	0.56 + 0.233*CL	0.57 + 0.233*CL	0.56 + 0.233*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.39 + 0.485*CL
	t_{PLZ}	0.50	0.50 + 0.000*CL	0.50 + 0.000*CL	0.50 + 0.000*CL
EN to PAD	t_{PHL}	12.36	0.72 + 0.233*CL	0.71 + 0.233*CL	0.73 + 0.233*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.39 + 0.485*CL
	t_{PLZ}	0.41	0.41 + 0.000*CL	0.41 + 0.000*CL	0.41 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	6.29	0.47 + 0.116*CL	0.47 + 0.116*CL	0.47 + 0.116*CL
	t_F	12.34	0.21 + 0.243*CL	0.20 + 0.243*CL	0.21 + 0.243*CL
	t_{PLZ}	0.53	0.53 + 0.000*CL	0.53 + 0.000*CL	0.53 + 0.000*CL
EN to PAD	t_{PHL}	6.45	0.63 + 0.116*CL	0.63 + 0.116*CL	0.62 + 0.116*CL
	t_F	12.34	0.21 + 0.243*CL	0.20 + 0.243*CL	0.21 + 0.243*CL
	t_{PLZ}	0.44	0.44 + 0.000*CL	0.44 + 0.000*CL	0.44 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	4.19	0.48 + 0.074*CL	0.48 + 0.074*CL	0.47 + 0.074*CL
	t_F	7.88	0.14 + 0.155*CL	0.15 + 0.155*CL	0.14 + 0.155*CL
	t_{PLZ}	0.54	0.54 + 0.000*CL	0.54 + 0.000*CL	0.54 + 0.000*CL
EN to PAD	t_{PHL}	4.34	0.63 + 0.074*CL	0.64 + 0.074*CL	0.63 + 0.074*CL
	t_F	7.88	0.14 + 0.155*CL	0.15 + 0.155*CL	0.14 + 0.155*CL
	t_{PLZ}	0.45	0.45 + 0.000*CL	0.45 + 0.000*CL	0.45 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.38	0.53 + 0.037*CL	0.53 + 0.037*CL	0.53 + 0.037*CL
	t_F	3.96	0.10 + 0.077*CL	0.09 + 0.077*CL	0.09 + 0.077*CL
	t_{PLZ}	0.62	0.62 + 0.000*CL	0.62 + 0.000*CL	0.62 + 0.000*CL
EN to PAD	t_{PHL}	2.54	0.69 + 0.037*CL	0.69 + 0.037*CL	0.69 + 0.037*CL
	t_F	3.96	0.10 + 0.077*CL	0.09 + 0.077*CL	0.09 + 0.077*CL
	t_{PLZ}	0.54	0.54 + 0.000*CL	0.54 + 0.000*CL	0.54 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.95	0.58 + 0.027*CL	0.58 + 0.027*CL	0.58 + 0.027*CL
	t_F	2.93	0.11 + 0.056*CL	0.10 + 0.057*CL	0.10 + 0.057*CL
	t_{PLZ}	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.68 + 0.000*CL
EN to PAD	t_{PHL}	2.10	0.74 + 0.027*CL	0.74 + 0.027*CL	0.74 + 0.027*CL
	t_F	2.93	0.11 + 0.056*CL	0.10 + 0.057*CL	0.10 + 0.057*CL
	t_{PLZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.66	0.66 + 0.020*CL	0.66 + 0.020*CL	0.67 + 0.020*CL
	t_F	2.19	0.15 + 0.041*CL	0.13 + 0.041*CL	0.12 + 0.041*CL
	t_{PLZ}	0.76	0.76 + 0.000*CL	0.76 + 0.000*CL	0.76 + 0.000*CL
EN to PAD	t_{PHL}	1.82	0.82 + 0.020*CL	0.83 + 0.020*CL	0.82 + 0.020*CL
	t_F	2.19	0.15 + 0.041*CL	0.13 + 0.041*CL	0.12 + 0.041*CL
	t_{PLZ}	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.67 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD20 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.53	0.74 + 0.016*CL	0.74 + 0.016*CL	0.75 + 0.016*CL
	t_F	1.79	0.20 + 0.032*CL	0.19 + 0.032*CL	0.17 + 0.032*CL
	t_{PLZ}	0.85	0.84 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL
EN to PAD	t_{PHL}	1.69	0.89 + 0.016*CL	0.90 + 0.016*CL	0.90 + 0.016*CL
	t_F	1.79	0.20 + 0.032*CL	0.19 + 0.032*CL	0.17 + 0.032*CL
	t_{PLZ}	0.76	0.76 + 0.000*CL	0.76 + 0.000*CL	0.76 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD24 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.48	0.77 + 0.014*CL	0.79 + 0.014*CL	0.79 + 0.014*CL
	t_F	1.62	0.23 + 0.028*CL	0.22 + 0.028*CL	0.21 + 0.028*CL
	t_{PLZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL
EN to PAD	t_{PHL}	1.64	0.93 + 0.014*CL	0.95 + 0.014*CL	0.95 + 0.014*CL
	t_F	1.62	0.23 + 0.028*CL	0.22 + 0.028*CL	0.21 + 0.028*CL
	t_{PLZ}	0.81	0.81 + 0.000*CL	0.82 + 0.000*CL	0.82 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD12SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.58	1.17 + 0.028*CL	1.19 + 0.028*CL	1.20 + 0.028*CL
	t_F	3.19	0.41 + 0.056*CL	0.37 + 0.056*CL	0.35 + 0.056*CL
	t_{PLZ}	0.52	0.52 + 0.000*CL	0.52 + 0.000*CL	0.52 + 0.000*CL
EN to PAD	t_{PHL}	2.74	1.33 + 0.028*CL	1.35 + 0.028*CL	1.35 + 0.028*CL
	t_F	3.19	0.41 + 0.056*CL	0.37 + 0.056*CL	0.35 + 0.056*CL
	t_{PLZ}	0.44	0.44 + 0.000*CL	0.44 + 0.000*CL	0.44 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD16SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.45	1.36 + 0.022*CL	1.42 + 0.021*CL	1.44 + 0.021*CL
	t_F	2.56	0.60 + 0.039*CL	0.57 + 0.040*CL	0.56 + 0.040*CL
	t_{PLZ}	0.52	0.52 + 0.000*CL	0.52 + 0.000*CL	0.52 + 0.000*CL
EN to PAD	t_{PHL}	2.61	1.52 + 0.022*CL	1.57 + 0.021*CL	1.61 + 0.021*CL
	t_F	2.56	0.60 + 0.039*CL	0.57 + 0.040*CL	0.56 + 0.040*CL
	t_{PLZ}	0.44	0.44 + 0.000*CL	0.44 + 0.000*CL	0.44 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD20SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.27	1.34 + 0.019*CL	1.42 + 0.018*CL	1.45 + 0.017*CL
	t_F	2.26	0.73 + 0.031*CL	0.73 + 0.031*CL	0.72 + 0.031*CL
	t_{PLZ}	0.56	0.56 + 0.000*CL	0.56 + 0.000*CL	0.56 + 0.000*CL
EN to PAD	t_{PHL}	2.43	1.49 + 0.019*CL	1.57 + 0.018*CL	1.62 + 0.017*CL
	t_F	2.26	0.73 + 0.031*CL	0.73 + 0.031*CL	0.72 + 0.031*CL
	t_{PLZ}	0.47	0.47 + 0.000*CL	0.47 + 0.000*CL	0.47 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD24SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.29	1.40 + 0.018*CL	1.50 + 0.017*CL	1.54 + 0.016*CL
	t_F	2.17	0.81 + 0.027*CL	0.82 + 0.027*CL	0.82 + 0.027*CL
	t_{PLZ}	0.56	0.56 + 0.000*CL	0.56 + 0.000*CL	0.56 + 0.000*CL
EN to PAD	t_{PHL}	2.45	1.56 + 0.018*CL	1.66 + 0.016*CL	1.70 + 0.016*CL
	t_F	2.17	0.81 + 0.027*CL	0.82 + 0.027*CL	0.82 + 0.027*CL
	t_{PLZ}	0.47	0.47 + 0.000*CL	0.47 + 0.000*CL	0.47 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD4SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	4.43	0.71 + 0.074*CL	0.72 + 0.074*CL	0.71 + 0.074*CL
	t_F	7.89	0.16 + 0.155*CL	0.15 + 0.155*CL	0.16 + 0.155*CL
	t_{PLZ}	0.57	0.57 + 0.000*CL	0.57 + 0.000*CL	0.57 + 0.000*CL
EN to PAD	t_{PHL}	4.58	0.87 + 0.074*CL	0.87 + 0.074*CL	0.87 + 0.074*CL
	t_F	7.89	0.16 + 0.155*CL	0.15 + 0.155*CL	0.16 + 0.155*CL
	t_{PLZ}	0.49	0.49 + 0.000*CL	0.49 + 0.000*CL	0.49 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD8SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.87	1.01 + 0.037*CL	1.01 + 0.037*CL	1.02 + 0.037*CL
	t_F	4.07	0.27 + 0.076*CL	0.24 + 0.076*CL	0.22 + 0.077*CL
	t_{PLZ}	0.57	0.57 + 0.000*CL	0.57 + 0.000*CL	0.57 + 0.000*CL
EN to PAD	t_{PHL}	3.03	1.17 + 0.037*CL	1.17 + 0.037*CL	1.17 + 0.037*CL
	t_F	4.07	0.27 + 0.076*CL	0.24 + 0.076*CL	0.22 + 0.077*CL
	t_{PLZ}	0.49	0.49 + 0.000*CL	0.49 + 0.000*CL	0.49 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD12SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.38	1.00 + 0.028*CL	1.01 + 0.027*CL	1.03 + 0.027*CL
	t_F	3.10	0.36 + 0.055*CL	0.33 + 0.055*CL	0.30 + 0.056*CL
	t_{PLZ}	0.56	0.56 + 0.000*CL	0.56 + 0.000*CL	0.56 + 0.000*CL
EN to PAD	t_{PHL}	2.54	1.16 + 0.028*CL	1.17 + 0.027*CL	1.18 + 0.027*CL
	t_F	3.10	0.36 + 0.055*CL	0.33 + 0.055*CL	0.30 + 0.056*CL
	t_{PLZ}	0.48	0.48 + 0.000*CL	0.48 + 0.000*CL	0.48 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD16SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.12	1.06 + 0.021*CL	1.10 + 0.021*CL	1.12 + 0.020*CL
	t_F	2.47	0.51 + 0.039*CL	0.48 + 0.040*CL	0.46 + 0.040*CL
	t_{PLZ}	0.59	0.59 + 0.000*CL	0.59 + 0.000*CL	0.59 + 0.000*CL
EN to PAD	t_{PHL}	2.27	1.21 + 0.021*CL	1.26 + 0.021*CL	1.28 + 0.020*CL
	t_F	2.47	0.51 + 0.039*CL	0.48 + 0.040*CL	0.46 + 0.040*CL
	t_{PLZ}	0.51	0.51 + 0.000*CL	0.51 + 0.000*CL	0.51 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD20SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.98	1.08 + 0.018*CL	1.15 + 0.017*CL	1.17 + 0.017*CL
	t_F	2.15	0.62 + 0.031*CL	0.61 + 0.031*CL	0.60 + 0.031*CL
	t_{PLZ}	0.62	0.62 + 0.000*CL	0.62 + 0.000*CL	0.62 + 0.000*CL
EN to PAD	t_{PHL}	2.14	1.24 + 0.018*CL	1.30 + 0.017*CL	1.34 + 0.017*CL
	t_F	2.15	0.62 + 0.031*CL	0.61 + 0.031*CL	0.60 + 0.031*CL
	t_{PLZ}	0.53	0.53 + 0.000*CL	0.53 + 0.000*CL	0.53 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POD24SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.00	1.14 + 0.017*CL	1.22 + 0.016*CL	1.27 + 0.016*CL
	t_F	2.07	0.71 + 0.027*CL	0.73 + 0.027*CL	0.73 + 0.027*CL
	t_{PLZ}	0.62	0.62 + 0.000*CL	0.62 + 0.000*CL	0.62 + 0.000*CL
EN to PAD	t_{PHL}	2.16	1.30 + 0.017*CL	1.38 + 0.016*CL	1.42 + 0.016*CL
	t_F	2.07	0.71 + 0.027*CL	0.73 + 0.027*CL	0.73 + 0.027*CL
	t_{PLZ}	0.53	0.53 + 0.000*CL	0.53 + 0.000*CL	0.53 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	14.09	0.89 + 0.264*CL	0.88 + 0.264*CL	0.88 + 0.264*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.80	0.80 + 0.000*CL	0.80 + 0.000*CL	0.80 + 0.000*CL
EN to PAD	t_{PHL}	14.20	1.00 + 0.264*CL	1.00 + 0.264*CL	1.00 + 0.264*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.73	0.73 + 0.000*CL	0.73 + 0.000*CL	0.73 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	6.97	0.79 + 0.124*CL	0.79 + 0.124*CL	0.80 + 0.123*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	0.84	0.84 + 0.000*CL	0.84 + 0.000*CL	0.84 + 0.000*CL
EN to PAD	t_{PHL}	7.08	0.91 + 0.123*CL	0.90 + 0.124*CL	0.90 + 0.124*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	0.78	0.78 + 0.000*CL	0.78 + 0.000*CL	0.78 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.92	0.83 + 0.062*CL	0.83 + 0.062*CL	0.82 + 0.062*CL
	t_F	6.81	0.15 + 0.133*CL	0.15 + 0.133*CL	0.16 + 0.133*CL
	t_{PLZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
EN to PAD	t_{PHL}	4.03	0.94 + 0.062*CL	0.94 + 0.062*CL	0.94 + 0.062*CL
	t_F	6.81	0.16 + 0.133*CL	0.16 + 0.133*CL	0.15 + 0.133*CL
	t_{PLZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.96	0.90 + 0.041*CL	0.90 + 0.041*CL	0.91 + 0.041*CL
	t_F	4.57	0.14 + 0.089*CL	0.13 + 0.089*CL	0.13 + 0.089*CL
	t_{PLZ}	0.98	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL
EN to PAD	t_{PHL}	3.07	1.01 + 0.041*CL	1.02 + 0.041*CL	1.01 + 0.041*CL
	t_F	4.57	0.14 + 0.089*CL	0.12 + 0.089*CL	0.13 + 0.089*CL
	t_{PLZ}	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.54	0.99 + 0.031*CL	0.99 + 0.031*CL	0.99 + 0.031*CL
	t_F	3.48	0.18 + 0.066*CL	0.15 + 0.066*CL	0.16 + 0.066*CL
	t_{PLZ}	1.05	1.05 + 0.000*CL	1.05 + 0.000*CL	1.05 + 0.000*CL
EN to PAD	t_{PHL}	2.65	1.10 + 0.031*CL	1.10 + 0.031*CL	1.11 + 0.031*CL
	t_F	3.47	0.18 + 0.066*CL	0.15 + 0.066*CL	0.13 + 0.066*CL
	t_{PLZ}	0.98	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD10 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.32	1.08 + 0.025*CL	1.08 + 0.025*CL	1.09 + 0.025*CL
	t_F	2.84	0.24 + 0.052*CL	0.17 + 0.053*CL	0.19 + 0.053*CL
	t_{PLZ}	1.12	1.12 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL
EN to PAD	t_{PHL}	2.43	1.19 + 0.025*CL	1.20 + 0.025*CL	1.19 + 0.025*CL
	t_F	2.84	0.23 + 0.052*CL	0.19 + 0.053*CL	0.19 + 0.053*CL
	t_{PLZ}	1.05	1.05 + 0.000*CL	1.05 + 0.000*CL	1.05 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.20	1.16 + 0.021*CL	1.17 + 0.021*CL	1.18 + 0.021*CL
	t_F	2.43	0.28 + 0.043*CL	0.25 + 0.044*CL	0.26 + 0.043*CL
	t_{PLZ}	1.19	1.19 + 0.000*CL	1.19 + 0.000*CL	1.19 + 0.000*CL
EN to PAD	t_{PHL}	2.31	1.27 + 0.021*CL	1.28 + 0.021*CL	1.28 + 0.021*CL
	t_F	2.44	0.28 + 0.043*CL	0.27 + 0.043*CL	0.26 + 0.043*CL
	t_{PLZ}	1.12	1.12 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.11	1.29 + 0.016*CL	1.32 + 0.016*CL	1.32 + 0.016*CL
	t_F	1.99	0.37 + 0.032*CL	0.38 + 0.032*CL	0.34 + 0.033*CL
	t_{PLZ}	1.31	1.31 + 0.000*CL	1.31 + 0.000*CL	1.31 + 0.000*CL
EN to PAD	t_{PHL}	2.22	1.40 + 0.016*CL	1.42 + 0.016*CL	1.44 + 0.016*CL
	t_F	2.00	0.39 + 0.032*CL	0.37 + 0.032*CL	0.36 + 0.033*CL
	t_{PLZ}	1.25	1.24 + 0.000*CL	1.25 + 0.000*CL	1.25 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	4.51	1.32 + 0.064*CL	1.32 + 0.064*CL	1.32 + 0.064*CL
	t_F	7.11	0.28 + 0.137*CL	0.24 + 0.137*CL	0.22 + 0.137*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PHL}	4.62	1.43 + 0.064*CL	1.43 + 0.064*CL	1.43 + 0.064*CL
	t_F	7.10	0.27 + 0.137*CL	0.24 + 0.137*CL	0.23 + 0.137*CL
	t_{PLZ}	0.81	0.81 + 0.000*CL	0.81 + 0.000*CL	0.81 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD6SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.77	1.65 + 0.042*CL	1.66 + 0.042*CL	1.67 + 0.042*CL
	t_F	4.89	0.48 + 0.088*CL	0.44 + 0.089*CL	0.39 + 0.089*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PHL}	3.88	1.76 + 0.042*CL	1.78 + 0.042*CL	1.79 + 0.042*CL
	t_F	4.89	0.48 + 0.088*CL	0.42 + 0.089*CL	0.39 + 0.089*CL
	t_{PLZ}	0.81	0.81 + 0.000*CL	0.81 + 0.000*CL	0.81 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.56	1.92 + 0.033*CL	1.98 + 0.032*CL	1.99 + 0.032*CL
	t_F	3.93	0.72 + 0.064*CL	0.65 + 0.065*CL	0.61 + 0.066*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PHL}	3.67	2.03 + 0.033*CL	2.09 + 0.032*CL	2.10 + 0.032*CL
	t_F	3.93	0.72 + 0.064*CL	0.65 + 0.065*CL	0.62 + 0.066*CL
	t_{PLZ}	0.81	0.81 + 0.000*CL	0.81 + 0.000*CL	0.81 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD10SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.20	1.83 + 0.027*CL	1.92 + 0.026*CL	1.95 + 0.026*CL
	t_F	3.38	0.91 + 0.049*CL	0.84 + 0.050*CL	0.82 + 0.050*CL
	t_{PLZ}	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + 0.000*CL
EN to PAD	t_{PHL}	3.31	1.94 + 0.027*CL	2.03 + 0.026*CL	2.07 + 0.026*CL
	t_F	3.38	0.92 + 0.049*CL	0.88 + 0.050*CL	0.82 + 0.050*CL
	t_{PLZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.23	1.99 + 0.025*CL	2.10 + 0.023*CL	2.16 + 0.023*CL
	t_F	3.15	1.12 + 0.041*CL	1.06 + 0.041*CL	1.08 + 0.041*CL
	t_{PLZ}	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + 0.000*CL
EN to PAD	t_{PHL}	3.34	2.10 + 0.025*CL	2.21 + 0.023*CL	2.28 + 0.023*CL
	t_F	3.15	1.12 + 0.041*CL	1.11 + 0.041*CL	1.06 + 0.041*CL
	t_{PLZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOD16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.38	2.23 + 0.023*CL	2.41 + 0.021*CL	2.48 + 0.020*CL
	t_F	2.98	1.43 + 0.031*CL	1.44 + 0.031*CL	1.41 + 0.031*CL
	t_{PLZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
EN to PAD	t_{PHL}	3.50	2.35 + 0.023*CL	2.51 + 0.021*CL	2.60 + 0.020*CL
	t_F	2.99	1.45 + 0.031*CL	1.42 + 0.031*CL	1.42 + 0.031*CL
	t_{PLZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	13.96	0.76 + 0.264*CL	0.76 + 0.264*CL	0.76 + 0.264*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.64	0.64 + 0.000*CL	0.64 + 0.000*CL	0.64 + 0.000*CL
EN to PAD	t_{PHL}	14.16	0.96 + 0.264*CL	0.96 + 0.264*CL	0.96 + 0.264*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.53	0.53 + 0.000*CL	0.53 + 0.000*CL	0.53 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	6.85	0.68 + 0.124*CL	0.67 + 0.124*CL	0.68 + 0.123*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.68 + 0.000*CL
EN to PAD	t_{PHL}	7.04	0.87 + 0.124*CL	0.87 + 0.123*CL	0.87 + 0.124*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	0.57	0.57 + 0.000*CL	0.57 + 0.000*CL	0.57 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.80	0.71 + 0.062*CL	0.71 + 0.062*CL	0.71 + 0.062*CL
	t_F	6.81	0.15 + 0.133*CL	0.15 + 0.133*CL	0.15 + 0.133*CL
	t_{PLZ}	0.75	0.75 + 0.000*CL	0.75 + 0.000*CL	0.75 + 0.000*CL
EN to PAD	t_{PHL}	3.99	0.90 + 0.062*CL	0.90 + 0.062*CL	0.90 + 0.062*CL
	t_F	6.81	0.15 + 0.133*CL	0.15 + 0.133*CL	0.15 + 0.133*CL
	t_{PLZ}	0.64	0.64 + 0.000*CL	0.64 + 0.000*CL	0.64 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.85	0.79 + 0.041*CL	0.79 + 0.041*CL	0.79 + 0.041*CL
	t_F	4.57	0.14 + 0.089*CL	0.14 + 0.089*CL	0.13 + 0.089*CL
	t_{PLZ}	0.82	0.82 + 0.000*CL	0.82 + 0.000*CL	0.82 + 0.000*CL
EN to PAD	t_{PHL}	3.04	0.98 + 0.041*CL	0.98 + 0.041*CL	0.98 + 0.041*CL
	t_F	4.57	0.14 + 0.089*CL	0.13 + 0.089*CL	0.14 + 0.089*CL
	t_{PLZ}	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.71 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.40	0.86 + 0.031*CL	0.85 + 0.031*CL	0.86 + 0.031*CL
	t_F	3.49	0.21 + 0.066*CL	0.18 + 0.066*CL	0.16 + 0.066*CL
	t_{PLZ}	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL
EN to PAD	t_{PHL}	2.61	1.07 + 0.031*CL	1.06 + 0.031*CL	1.07 + 0.031*CL
	t_F	3.47	0.18 + 0.066*CL	0.15 + 0.066*CL	0.15 + 0.066*CL
	t_{PLZ}	0.78	0.78 + 0.000*CL	0.78 + 0.000*CL	0.78 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD10 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.18	0.95 + 0.025*CL	0.95 + 0.025*CL	0.95 + 0.025*CL
	t_F	2.86	0.27 + 0.052*CL	0.22 + 0.052*CL	0.21 + 0.053*CL
	t_{PLZ}	0.95	0.95 + 0.000*CL	0.95 + 0.000*CL	0.95 + 0.000*CL
EN to PAD	t_{PHL}	2.39	1.15 + 0.025*CL	1.16 + 0.025*CL	1.15 + 0.025*CL
	t_F	2.84	0.24 + 0.052*CL	0.19 + 0.053*CL	0.20 + 0.053*CL
	t_{PLZ}	0.85	0.84 + 0.000*CL	0.84 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.07	1.03 + 0.021*CL	1.03 + 0.021*CL	1.03 + 0.021*CL
	t_F	2.46	0.33 + 0.043*CL	0.30 + 0.043*CL	0.25 + 0.044*CL
	t_{PLZ}	1.02	1.02 + 0.000*CL	1.02 + 0.000*CL	1.02 + 0.000*CL
EN to PAD	t_{PHL}	2.27	1.23 + 0.021*CL	1.25 + 0.021*CL	1.25 + 0.021*CL
	t_F	2.44	0.28 + 0.043*CL	0.25 + 0.044*CL	0.26 + 0.043*CL
	t_{PLZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.98	1.16 + 0.016*CL	1.18 + 0.016*CL	1.20 + 0.016*CL
	t_F	2.01	0.39 + 0.032*CL	0.39 + 0.032*CL	0.38 + 0.032*CL
	t_{PLZ}	1.15	1.15 + 0.000*CL	1.15 + 0.000*CL	1.15 + 0.000*CL
EN to PAD	t_{PHL}	2.18	1.36 + 0.016*CL	1.40 + 0.016*CL	1.39 + 0.016*CL
	t_F	2.00	0.39 + 0.032*CL	0.36 + 0.033*CL	0.34 + 0.033*CL
	t_{PLZ}	1.04	1.04 + 0.000*CL	1.04 + 0.000*CL	1.04 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	4.39	1.20 + 0.064*CL	1.20 + 0.064*CL	1.20 + 0.064*CL
	t_F	7.11	0.28 + 0.137*CL	0.24 + 0.137*CL	0.22 + 0.137*CL
	t_{PLZ}	0.70	0.70 + 0.000*CL	0.70 + 0.000*CL	0.70 + 0.000*CL
EN to PAD	t_{PHL}	4.58	1.39 + 0.064*CL	1.39 + 0.064*CL	1.39 + 0.064*CL
	t_F	7.10	0.27 + 0.137*CL	0.24 + 0.137*CL	0.22 + 0.137*CL
	t_{PLZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD6SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.65	1.54 + 0.042*CL	1.55 + 0.042*CL	1.55 + 0.042*CL
	t_F	4.89	0.48 + 0.088*CL	0.43 + 0.089*CL	0.39 + 0.089*CL
	t_{PLZ}	0.70	0.70 + 0.000*CL	0.70 + 0.000*CL	0.70 + 0.000*CL
EN to PAD	t_{PHL}	3.85	1.73 + 0.042*CL	1.74 + 0.042*CL	1.74 + 0.042*CL
	t_F	4.89	0.48 + 0.088*CL	0.43 + 0.089*CL	0.39 + 0.089*CL
	t_{PLZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.44	1.80 + 0.033*CL	1.85 + 0.032*CL	1.88 + 0.032*CL
	t_F	3.93	0.73 + 0.064*CL	0.64 + 0.065*CL	0.63 + 0.065*CL
	t_{PLZ}	0.70	0.70 + 0.000*CL	0.70 + 0.000*CL	0.70 + 0.000*CL
EN to PAD	t_{PHL}	3.63	2.00 + 0.033*CL	2.04 + 0.032*CL	2.07 + 0.032*CL
	t_F	3.93	0.72 + 0.064*CL	0.66 + 0.065*CL	0.62 + 0.065*CL
	t_{PLZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD10SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.08	1.72 + 0.027*CL	1.80 + 0.026*CL	1.84 + 0.026*CL
	t_F	3.38	0.91 + 0.049*CL	0.86 + 0.050*CL	0.83 + 0.050*CL
	t_{PLZ}	0.75	0.75 + 0.000*CL	0.75 + 0.000*CL	0.75 + 0.000*CL
EN to PAD	t_{PHL}	3.27	1.91 + 0.027*CL	1.99 + 0.026*CL	2.03 + 0.026*CL
	t_F	3.38	0.92 + 0.049*CL	0.87 + 0.050*CL	0.83 + 0.050*CL
	t_{PLZ}	0.65	0.65 + 0.000*CL	0.65 + 0.000*CL	0.65 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.11	1.87 + 0.025*CL	1.99 + 0.023*CL	2.04 + 0.023*CL
	t_F	3.15	1.13 + 0.040*CL	1.07 + 0.041*CL	1.07 + 0.041*CL
	t_{PLZ}	0.75	0.75 + 0.000*CL	0.75 + 0.000*CL	0.75 + 0.000*CL
EN to PAD	t_{PHL}	3.30	2.06 + 0.025*CL	2.18 + 0.023*CL	2.24 + 0.023*CL
	t_F	3.15	1.12 + 0.041*CL	1.09 + 0.041*CL	1.08 + 0.041*CL
	t_{PLZ}	0.65	0.65 + 0.000*CL	0.65 + 0.000*CL	0.65 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POD16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.27	2.12 + 0.023*CL	2.28 + 0.021*CL	2.37 + 0.020*CL
	t_F	2.98	1.43 + 0.031*CL	1.46 + 0.031*CL	1.43 + 0.031*CL
	t_{PLZ}	0.75	0.75 + 0.000*CL	0.75 + 0.000*CL	0.75 + 0.000*CL
EN to PAD	t_{PHL}	3.46	2.31 + 0.023*CL	2.48 + 0.021*CL	2.56 + 0.020*CL
	t_F	2.98	1.43 + 0.031*CL	1.45 + 0.031*CL	1.43 + 0.031*CL
	t_{PLZ}	0.65	0.65 + 0.000*CL	0.65 + 0.000*CL	0.65 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	12.57	0.93 + 0.233*CL	0.93 + 0.233*CL	0.93 + 0.233*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL
	t_{PLZ}	0.84	0.84 + 0.000*CL	0.84 + 0.000*CL	0.84 + 0.000*CL
EN to PAD	t_{PHL}	12.75	1.10 + 0.233*CL	1.10 + 0.233*CL	1.10 + 0.233*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL
	t_{PLZ}	0.77	0.77 + 0.000*CL	0.77 + 0.000*CL	0.77 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	6.66	0.84 + 0.116*CL	0.84 + 0.116*CL	0.84 + 0.116*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.243*CL	0.21 + 0.243*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PHL}	6.83	1.01 + 0.116*CL	1.01 + 0.116*CL	1.01 + 0.116*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.243*CL	0.21 + 0.243*CL
	t_{PLZ}	0.80	0.80 + 0.000*CL	0.80 + 0.000*CL	0.80 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	4.56	0.85 + 0.074*CL	0.85 + 0.074*CL	0.85 + 0.074*CL
	t_F	7.88	0.14 + 0.155*CL	0.14 + 0.155*CL	0.15 + 0.155*CL
	t_{PLZ}	0.88	0.88 + 0.000*CL	0.88 + 0.000*CL	0.88 + 0.000*CL
EN to PAD	t_{PHL}	4.73	1.02 + 0.074*CL	1.02 + 0.074*CL	1.02 + 0.074*CL
	t_F	7.88	0.15 + 0.155*CL	0.15 + 0.155*CL	0.15 + 0.155*CL
	t_{PLZ}	0.80	0.80 + 0.000*CL	0.80 + 0.000*CL	0.80 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.76	0.90 + 0.037*CL	0.90 + 0.037*CL	0.90 + 0.037*CL
	t_F	3.96	0.10 + 0.077*CL	0.10 + 0.077*CL	0.10 + 0.077*CL
	t_{PLZ}	0.96	0.96 + 0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL
EN to PAD	t_{PHL}	2.93	1.07 + 0.037*CL	1.07 + 0.037*CL	1.07 + 0.037*CL
	t_F	3.96	0.10 + 0.077*CL	0.10 + 0.077*CL	0.10 + 0.077*CL
	t_{PLZ}	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.32	0.95 + 0.027*CL	0.96 + 0.027*CL	0.96 + 0.027*CL
	t_F	2.93	0.11 + 0.056*CL	0.12 + 0.056*CL	0.09 + 0.057*CL
	t_{PLZ}	1.03	1.03 + 0.000*CL	1.03 + 0.000*CL	1.03 + 0.000*CL
EN to PAD	t_{PHL}	2.49	1.13 + 0.027*CL	1.13 + 0.027*CL	1.13 + 0.027*CL
	t_F	2.94	0.12 + 0.056*CL	0.09 + 0.057*CL	0.10 + 0.057*CL
	t_{PLZ}	0.95	0.95 + 0.000*CL	0.95 + 0.000*CL	0.95 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.03	1.04 + 0.020*CL	1.03 + 0.020*CL	1.04 + 0.020*CL
	t_F	2.20	0.15 + 0.041*CL	0.15 + 0.041*CL	0.15 + 0.041*CL
	t_{PLZ}	1.11	1.11 + 0.000*CL	1.10 + 0.000*CL	1.11 + 0.000*CL
EN to PAD	t_{PHL}	2.21	1.21 + 0.020*CL	1.21 + 0.020*CL	1.20 + 0.020*CL
	t_F	2.20	0.15 + 0.041*CL	0.16 + 0.041*CL	0.14 + 0.041*CL
	t_{PLZ}	1.03	1.03 + 0.000*CL	1.03 + 0.000*CL	1.03 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD20 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.90	1.11 + 0.016*CL	1.12 + 0.016*CL	1.12 + 0.016*CL
	t_F	1.80	0.23 + 0.031*CL	0.18 + 0.032*CL	0.18 + 0.032*CL
	t_{PLZ}	1.19	1.19 + 0.000*CL	1.18 + 0.000*CL	1.19 + 0.000*CL
EN to PAD	t_{PHL}	2.08	1.28 + 0.016*CL	1.29 + 0.016*CL	1.29 + 0.016*CL
	t_F	1.80	0.22 + 0.032*CL	0.19 + 0.032*CL	0.20 + 0.032*CL
	t_{PLZ}	1.12	1.11 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD24 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.86	1.15 + 0.014*CL	1.16 + 0.014*CL	1.16 + 0.014*CL
	t_F	1.63	0.24 + 0.028*CL	0.22 + 0.028*CL	0.22 + 0.028*CL
	t_{PLZ}	1.24	1.24 + 0.000*CL	1.24 + 0.000*CL	1.24 + 0.000*CL
EN to PAD	t_{PHL}	2.03	1.32 + 0.014*CL	1.33 + 0.014*CL	1.34 + 0.014*CL
	t_F	1.64	0.25 + 0.028*CL	0.23 + 0.028*CL	0.24 + 0.028*CL
	t_{PLZ}	1.17	1.17 + 0.000*CL	1.17 + 0.000*CL	1.17 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD12SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.95	1.54 + 0.028*CL	1.57 + 0.028*CL	1.57 + 0.028*CL
	t_F	3.20	0.42 + 0.056*CL	0.37 + 0.056*CL	0.35 + 0.056*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PHL}	3.13	1.71 + 0.028*CL	1.74 + 0.028*CL	1.75 + 0.028*CL
	t_F	3.20	0.42 + 0.056*CL	0.38 + 0.056*CL	0.34 + 0.057*CL
	t_{PLZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.79 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD16SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.82	1.73 + 0.022*CL	1.79 + 0.021*CL	1.81 + 0.021*CL
	t_F	2.57	0.61 + 0.039*CL	0.57 + 0.040*CL	0.57 + 0.040*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PHL}	2.99	1.90 + 0.022*CL	1.96 + 0.021*CL	1.99 + 0.021*CL
	t_F	2.57	0.62 + 0.039*CL	0.57 + 0.040*CL	0.56 + 0.040*CL
	t_{PLZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.79 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD20SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.64	1.70 + 0.019*CL	1.78 + 0.018*CL	1.83 + 0.017*CL
	t_F	2.27	0.74 + 0.031*CL	0.76 + 0.030*CL	0.72 + 0.031*CL
	t_{PLZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL
EN to PAD	t_{PHL}	2.82	1.88 + 0.019*CL	1.95 + 0.018*CL	2.00 + 0.017*CL
	t_F	2.27	0.75 + 0.030*CL	0.73 + 0.031*CL	0.74 + 0.031*CL
	t_{PLZ}	0.83	0.83 + 0.000*CL	0.83 + 0.000*CL	0.83 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD24SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.66	1.77 + 0.018*CL	1.87 + 0.017*CL	1.91 + 0.016*CL
	t_F	2.18	0.82 + 0.027*CL	0.81 + 0.027*CL	0.84 + 0.027*CL
	t_{PLZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL
EN to PAD	t_{PHL}	2.83	1.94 + 0.018*CL	2.04 + 0.017*CL	2.08 + 0.016*CL
	t_F	2.18	0.84 + 0.027*CL	0.84 + 0.027*CL	0.86 + 0.027*CL
	t_{PLZ}	0.83	0.83 + 0.000*CL	0.83 + 0.000*CL	0.83 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD4SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	4.80	1.08 + 0.074*CL	1.09 + 0.074*CL	1.08 + 0.074*CL
	t_F	7.89	0.16 + 0.155*CL	0.15 + 0.155*CL	0.16 + 0.155*CL
	t_{PLZ}	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + 0.000*CL
EN to PAD	t_{PHL}	4.97	1.26 + 0.074*CL	1.25 + 0.074*CL	1.26 + 0.074*CL
	t_F	7.89	0.16 + 0.155*CL	0.15 + 0.155*CL	0.16 + 0.155*CL
	t_{PLZ}	0.84	0.84 + 0.000*CL	0.84 + 0.000*CL	0.84 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD8SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.24	1.38 + 0.037*CL	1.38 + 0.037*CL	1.39 + 0.037*CL
	t_F	4.08	0.28 + 0.076*CL	0.25 + 0.076*CL	0.23 + 0.077*CL
	t_{PLZ}	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + 0.000*CL
EN to PAD	t_{PHL}	3.41	1.55 + 0.037*CL	1.56 + 0.037*CL	1.56 + 0.037*CL
	t_F	4.08	0.28 + 0.076*CL	0.24 + 0.076*CL	0.23 + 0.077*CL
	t_{PLZ}	0.84	0.84 + 0.000*CL	0.84 + 0.000*CL	0.84 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD12SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.75	1.37 + 0.028*CL	1.39 + 0.027*CL	1.40 + 0.027*CL
	t_F	3.11	0.37 + 0.055*CL	0.33 + 0.055*CL	0.30 + 0.056*CL
	t_{PLZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL
EN to PAD	t_{PHL}	2.92	1.54 + 0.028*CL	1.56 + 0.027*CL	1.57 + 0.027*CL
	t_F	3.11	0.36 + 0.055*CL	0.33 + 0.055*CL	0.30 + 0.056*CL
	t_{PLZ}	0.83	0.83 + 0.000*CL	0.83 + 0.000*CL	0.83 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD16SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.49	1.43 + 0.021*CL	1.47 + 0.021*CL	1.50 + 0.020*CL
	t_F	2.48	0.52 + 0.039*CL	0.49 + 0.040*CL	0.46 + 0.040*CL
	t_{PLZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL
EN to PAD	t_{PHL}	2.66	1.60 + 0.021*CL	1.65 + 0.021*CL	1.66 + 0.020*CL
	t_F	2.48	0.52 + 0.039*CL	0.51 + 0.039*CL	0.47 + 0.040*CL
	t_{PLZ}	0.86	0.86 + 0.000*CL	0.86 + 0.000*CL	0.86 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD20SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.35	1.45 + 0.018*CL	1.52 + 0.017*CL	1.55 + 0.017*CL
	t_F	2.16	0.62 + 0.031*CL	0.63 + 0.031*CL	0.61 + 0.031*CL
	t_{PLZ}	0.96	0.96 + 0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL
EN to PAD	t_{PHL}	2.52	1.62 + 0.018*CL	1.69 + 0.017*CL	1.72 + 0.017*CL
	t_F	2.16	0.64 + 0.031*CL	0.60 + 0.031*CL	0.61 + 0.031*CL
	t_{PLZ}	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOD24SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.37	1.51 + 0.017*CL	1.59 + 0.016*CL	1.63 + 0.016*CL
	t_F	2.08	0.72 + 0.027*CL	0.74 + 0.027*CL	0.74 + 0.027*CL
	t_{PLZ}	0.96	0.96 + 0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL
EN to PAD	t_{PHL}	2.54	1.68 + 0.017*CL	1.76 + 0.016*CL	1.81 + 0.016*CL
	t_F	2.08	0.73 + 0.027*CL	0.72 + 0.027*CL	0.74 + 0.027*CL
	t_{PLZ}	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

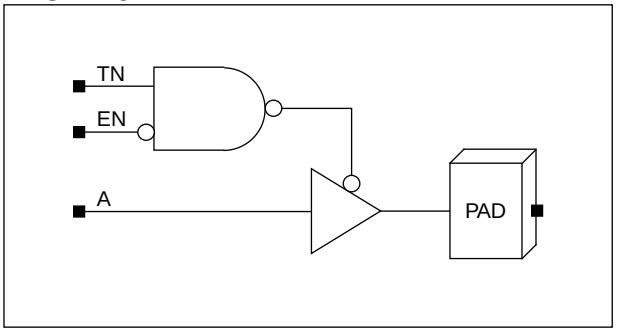
PvOTyz

Tri-State Output Buffers

Cell Availability

Library	5V Operation	3.3V Operation
STD80	POT(1/2/4/8/12/16/20/24) POT(12/16/20/24)SH POT(4/8/12/16/20/24)SM	PLOT(1/2/4/6/8/10/12/16) PLOT(4/6/8/10/12/16)SM
STDM80	PHOT(1/2/4/8/12/16/20/24) PHOT(12/16/20/24)SH PHOT(4/8/12/16/20/24)SM	POT(1/2/4/6/8/10/12/16) POT(4/6/8/10/12/16)SM

Logic Symbol



Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi-Z
0	x	x	Hi-Z

I/O Slot

STD80/STDM80	
PvOTyz	1.0

Input Load (SL)

STD80			
	TN	EN	A
POT(1/2/4/8/12/16/20/24)	1.4	1.6	2.4
POT(12/16/20/24)SH	1.4	1.6	2.4
POT(4/8/12/16/20/24)SM	1.4	1.6	2.4
PLOT(1/2/4/6/8/10/12/16)	1.2	1.2	2.3
PLOT(4/6/8/10/12/16)SM	1.2	1.2	2.3
STDM80			
	TN	EN	A
POT(1/2/4/6/8/10/12/16)	1.8	1.8	2.6
POT(4/6/8/10/12/16)SM	1.8	1.8	2.6
PHOT(1/2/4/8/12/16/20/24)	1.4	1.4	2.8
PHOT(12/16/20/24)SH	1.4	1.4	2.8
PHOT(4/8/12/16/20/24)SM	1.4	1.4	2.8

STD80 POT1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	15.24	0.63 + 0.292*CL	0.63 + 0.292*CL	0.63 + 0.292*CL
	t_{PHL}	12.28	0.63 + 0.233*CL	0.63 + 0.233*CL	0.63 + 0.233*CL
	t_R	33.59	0.59 + 0.660*CL	0.59 + 0.660*CL	0.59 + 0.660*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL
TN to PAD	t_{PLH}	15.23	0.73 + 0.290*CL	1.33 + 0.282*CL	2.49 + 0.268*CL
	t_{PHL}	12.30	0.65 + 0.233*CL	0.65 + 0.233*CL	0.65 + 0.233*CL
	t_R	33.59	0.59 + 0.660*CL	0.60 + 0.660*CL	0.59 + 0.660*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL
	t_{PLZ}	0.63	0.63 + 0.000*CL	0.63 + 0.000*CL	0.63 + 0.000*CL
	t_{PHZ}	0.58	0.58 + 0.000*CL	0.58 + 0.000*CL	0.58 + 0.000*CL
EN to PAD	t_{PLH}	15.39	0.88 + 0.290*CL	1.49 + 0.282*CL	2.68 + 0.268*CL
	t_{PHL}	12.45	0.81 + 0.233*CL	0.81 + 0.233*CL	0.81 + 0.233*CL
	t_R	33.59	0.59 + 0.660*CL	0.60 + 0.660*CL	0.59 + 0.660*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL
	t_{PLZ}	0.55	0.55 + 0.000*CL	0.55 + 0.000*CL	0.55 + 0.000*CL
	t_{PHZ}	0.50	0.50 + 0.000*CL	0.50 + 0.000*CL	0.50 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	7.86	0.56 + 0.146*CL	0.55 + 0.146*CL	0.56 + 0.146*CL
	t_{PHL}	6.37	0.55 + 0.116*CL	0.55 + 0.116*CL	0.55 + 0.116*CL
	t_R	16.81	0.31 + 0.330*CL	0.31 + 0.330*CL	0.31 + 0.330*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.242*CL	0.21 + 0.243*CL
TN to PAD	t_{PLH}	7.86	0.55 + 0.146*CL	0.54 + 0.146*CL	0.56 + 0.146*CL
	t_{PHL}	6.39	0.57 + 0.116*CL	0.57 + 0.116*CL	0.57 + 0.116*CL
	t_R	16.81	0.31 + 0.330*CL	0.31 + 0.330*CL	0.31 + 0.330*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.242*CL	0.21 + 0.243*CL
	t_{PLZ}	0.69	0.69 + 0.000*CL	0.69 + 0.000*CL	0.69 + 0.000*CL
	t_{PHZ}	0.63	0.63 + 0.000*CL	0.63 + 0.000*CL	0.63 + 0.000*CL
EN to PAD	t_{PLH}	8.01	0.70 + 0.146*CL	0.71 + 0.146*CL	0.70 + 0.146*CL
	t_{PHL}	6.55	0.73 + 0.116*CL	0.72 + 0.117*CL	0.73 + 0.116*CL
	t_R	16.81	0.31 + 0.330*CL	0.31 + 0.330*CL	0.31 + 0.330*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.242*CL	0.21 + 0.243*CL
	t_{PLZ}	0.61	0.61 + 0.000*CL	0.61 + 0.000*CL	0.61 + 0.000*CL
	t_{PHZ}	0.55	0.55 + 0.000*CL	0.55 + 0.000*CL	0.55 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.25	0.56 + 0.094*CL	0.56 + 0.094*CL	0.56 + 0.094*CL
	t_{PHL}	4.25	0.54 + 0.074*CL	0.54 + 0.074*CL	0.55 + 0.074*CL
	t_R	10.81	0.21 + 0.212*CL	0.21 + 0.212*CL	0.21 + 0.212*CL
	t_F	7.88	0.14 + 0.155*CL	0.15 + 0.155*CL	0.14 + 0.155*CL
TN to PAD	t_{PLH}	5.24	0.55 + 0.094*CL	0.55 + 0.094*CL	0.55 + 0.094*CL
	t_{PHL}	4.27	0.56 + 0.074*CL	0.56 + 0.074*CL	0.57 + 0.074*CL
	t_R	10.81	0.21 + 0.212*CL	0.21 + 0.212*CL	0.21 + 0.212*CL
	t_F	7.88	0.14 + 0.155*CL	0.15 + 0.155*CL	0.14 + 0.155*CL
	t_{PLZ}	0.75	0.75 + 0.000*CL	0.75 + 0.000*CL	0.75 + 0.000*CL
	t_{PHZ}	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.68 + 0.000*CL
EN to PAD	t_{PLH}	5.39	0.70 + 0.094*CL	0.70 + 0.094*CL	0.70 + 0.094*CL
	t_{PHL}	4.43	0.72 + 0.074*CL	0.71 + 0.074*CL	0.72 + 0.074*CL
	t_R	10.81	0.21 + 0.212*CL	0.21 + 0.212*CL	0.21 + 0.212*CL
	t_F	7.88	0.14 + 0.155*CL	0.15 + 0.155*CL	0.14 + 0.155*CL
	t_{PLZ}	0.67	0.67 + 0.000*CL	0.67 + 0.000*CL	0.67 + 0.000*CL
	t_{PHZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.96	0.62 + 0.047*CL	0.62 + 0.047*CL	0.62 + 0.047*CL
	t_{PHL}	2.45	0.60 + 0.037*CL	0.60 + 0.037*CL	0.60 + 0.037*CL
	t_R	5.43	0.13 + 0.106*CL	0.13 + 0.106*CL	0.13 + 0.106*CL
	t_F	3.96	0.10 + 0.077*CL	0.09 + 0.077*CL	0.09 + 0.077*CL
TN to PAD	t_{PLH}	2.95	0.61 + 0.047*CL	0.61 + 0.047*CL	0.61 + 0.047*CL
	t_{PHL}	2.47	0.62 + 0.037*CL	0.61 + 0.037*CL	0.62 + 0.037*CL
	t_R	5.43	0.13 + 0.106*CL	0.13 + 0.106*CL	0.13 + 0.106*CL
	t_F	3.96	0.10 + 0.077*CL	0.09 + 0.077*CL	0.09 + 0.077*CL
	t_{PLZ}	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + 0.000*CL
	t_{PHZ}	0.82	0.82 + 0.000*CL	0.82 + 0.000*CL	0.82 + 0.000*CL
EN to PAD	t_{PLH}	3.11	0.76 + 0.047*CL	0.76 + 0.047*CL	0.76 + 0.047*CL
	t_{PHL}	2.63	0.77 + 0.037*CL	0.77 + 0.037*CL	0.77 + 0.037*CL
	t_R	5.43	0.13 + 0.106*CL	0.13 + 0.106*CL	0.13 + 0.106*CL
	t_F	3.96	0.10 + 0.077*CL	0.09 + 0.077*CL	0.09 + 0.077*CL
	t_{PLZ}	0.84	0.84 + 0.000*CL	0.83 + 0.000*CL	0.84 + 0.000*CL
	t_{PHZ}	0.74	0.74 + 0.000*CL	0.74 + 0.000*CL	0.74 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.41	0.68 + 0.035*CL	0.68 + 0.035*CL	0.68 + 0.035*CL
	t_{PHL}	2.02	0.66 + 0.027*CL	0.66 + 0.027*CL	0.66 + 0.027*CL
	t_R	4.02	0.12 + 0.078*CL	0.12 + 0.078*CL	0.11 + 0.078*CL
	t_F	2.93	0.11 + 0.056*CL	0.10 + 0.057*CL	0.09 + 0.057*CL
TN to PAD	t_{PLH}	2.39	0.66 + 0.035*CL	0.67 + 0.035*CL	0.66 + 0.035*CL
	t_{PHL}	2.03	0.67 + 0.027*CL	0.67 + 0.027*CL	0.67 + 0.027*CL
	t_R	4.02	0.12 + 0.078*CL	0.12 + 0.078*CL	0.11 + 0.078*CL
	t_F	2.93	0.11 + 0.056*CL	0.10 + 0.057*CL	0.09 + 0.057*CL
	t_{PLZ}	1.04	1.04 + 0.000*CL	1.04 + 0.000*CL	1.04 + 0.000*CL
	t_{PHZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL
EN to PAD	t_{PLH}	2.54	0.82 + 0.035*CL	0.81 + 0.035*CL	0.82 + 0.035*CL
	t_{PHL}	2.19	0.82 + 0.027*CL	0.83 + 0.027*CL	0.83 + 0.027*CL
	t_R	4.02	0.12 + 0.078*CL	0.12 + 0.078*CL	0.11 + 0.078*CL
	t_F	2.93	0.11 + 0.056*CL	0.10 + 0.057*CL	0.09 + 0.057*CL
	t_{PLZ}	0.96	0.96 + 0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL
	t_{PHZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.84 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.03	0.78 + 0.025*CL	0.77 + 0.025*CL	0.77 + 0.025*CL
	t_{PHL}	1.74	0.75 + 0.020*CL	0.74 + 0.020*CL	0.74 + 0.020*CL
	t_R	2.97	0.13 + 0.057*CL	0.13 + 0.057*CL	0.12 + 0.057*CL
	t_F	2.19	0.14 + 0.041*CL	0.13 + 0.041*CL	0.12 + 0.041*CL
TN to PAD	t_{PLH}	2.01	0.75 + 0.025*CL	0.74 + 0.025*CL	0.75 + 0.025*CL
	t_{PHL}	1.75	0.75 + 0.020*CL	0.75 + 0.020*CL	0.75 + 0.020*CL
	t_R	2.97	0.14 + 0.057*CL	0.12 + 0.057*CL	0.12 + 0.057*CL
	t_F	2.19	0.14 + 0.041*CL	0.13 + 0.041*CL	0.12 + 0.041*CL
	t_{PLZ}	1.20	1.20 + 0.000*CL	1.20 + 0.000*CL	1.20 + 0.000*CL
	t_{PHZ}	1.07	1.07 + 0.000*CL	1.07 + 0.000*CL	1.07 + 0.000*CL
EN to PAD	t_{PLH}	2.16	0.90 + 0.025*CL	0.91 + 0.025*CL	0.90 + 0.025*CL
	t_{PHL}	1.90	0.91 + 0.020*CL	0.90 + 0.020*CL	0.91 + 0.020*CL
	t_R	2.97	0.14 + 0.057*CL	0.13 + 0.057*CL	0.12 + 0.057*CL
	t_F	2.19	0.14 + 0.041*CL	0.13 + 0.041*CL	0.12 + 0.041*CL
	t_{PLZ}	1.12	1.12 + 0.000*CL	1.11 + 0.000*CL	1.12 + 0.000*CL
	t_{PHZ}	0.99	0.99 + 0.000*CL	0.99 + 0.000*CL	0.99 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT20 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.66	0.67 + 0.020*CL	0.67 + 0.020*CL	0.66 + 0.020*CL
	t_{PHL}	1.51	0.72 + 0.016*CL	0.73 + 0.016*CL	0.72 + 0.016*CL
	t_R	2.33	0.09 + 0.045*CL	0.09 + 0.045*CL	0.08 + 0.045*CL
	t_F	1.74	0.13 + 0.032*CL	0.11 + 0.032*CL	0.11 + 0.032*CL
TN to PAD	t_{PLH}	1.65	0.65 + 0.020*CL	0.65 + 0.020*CL	0.65 + 0.020*CL
	t_{PHL}	1.52	0.73 + 0.016*CL	0.74 + 0.016*CL	0.73 + 0.016*CL
	t_R	2.33	0.10 + 0.045*CL	0.09 + 0.045*CL	0.08 + 0.045*CL
	t_F	1.74	0.13 + 0.032*CL	0.12 + 0.032*CL	0.11 + 0.032*CL
	t_{PLZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL
	t_{PHZ}	0.98	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL
EN to PAD	t_{PLH}	1.80	0.81 + 0.020*CL	0.81 + 0.020*CL	0.81 + 0.020*CL
	t_{PHL}	1.67	0.88 + 0.016*CL	0.89 + 0.016*CL	0.89 + 0.016*CL
	t_R	2.33	0.10 + 0.045*CL	0.09 + 0.045*CL	0.08 + 0.045*CL
	t_F	1.74	0.13 + 0.032*CL	0.12 + 0.032*CL	0.11 + 0.032*CL
	t_{PLZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL
	t_{PHZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT24 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.59	0.72 + 0.017*CL	0.72 + 0.018*CL	0.72 + 0.018*CL
	t_{PHL}	1.45	0.75 + 0.014*CL	0.76 + 0.014*CL	0.75 + 0.014*CL
	t_R	2.07	0.11 + 0.039*CL	0.09 + 0.039*CL	0.09 + 0.039*CL
	t_F	1.56	0.15 + 0.028*CL	0.13 + 0.028*CL	0.13 + 0.028*CL
TN to PAD	t_{PLH}	1.58	0.70 + 0.018*CL	0.71 + 0.017*CL	0.70 + 0.018*CL
	t_{PHL}	1.46	0.76 + 0.014*CL	0.77 + 0.014*CL	0.77 + 0.014*CL
	t_R	2.07	0.11 + 0.039*CL	0.09 + 0.039*CL	0.09 + 0.039*CL
	t_F	1.56	0.15 + 0.028*CL	0.14 + 0.028*CL	0.13 + 0.028*CL
	t_{PLZ}	1.07	1.07 + 0.000*CL	1.06 + 0.000*CL	1.07 + 0.000*CL
	t_{PHZ}	0.97	0.97 + 0.000*CL	0.97 + 0.000*CL	0.96 + 0.000*CL
EN to PAD	t_{PLH}	1.73	0.86 + 0.018*CL	0.86 + 0.018*CL	0.86 + 0.018*CL
	t_{PHL}	1.62	0.92 + 0.014*CL	0.92 + 0.014*CL	0.93 + 0.014*CL
	t_R	2.07	0.11 + 0.039*CL	0.09 + 0.039*CL	0.09 + 0.039*CL
	t_F	1.56	0.15 + 0.028*CL	0.14 + 0.028*CL	0.13 + 0.028*CL
	t_{PLZ}	0.99	0.99 + 0.000*CL	0.99 + 0.000*CL	0.99 + 0.000*CL
	t_{PHZ}	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT12SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.17	1.39 + 0.036*CL	1.41 + 0.035*CL	1.42 + 0.035*CL
	t_{PHL}	3.66	2.06 + 0.032*CL	2.17 + 0.030*CL	2.23 + 0.030*CL
	t_R	4.34	0.49 + 0.077*CL	0.44 + 0.078*CL	0.43 + 0.078*CL
	t_F	3.73	0.96 + 0.055*CL	0.97 + 0.055*CL	0.98 + 0.055*CL
TN to PAD	t_{PLH}	3.12	1.34 + 0.036*CL	1.37 + 0.035*CL	1.37 + 0.035*CL
	t_{PHL}	3.67	2.07 + 0.032*CL	2.18 + 0.031*CL	2.24 + 0.030*CL
	t_R	4.34	0.49 + 0.077*CL	0.44 + 0.078*CL	0.43 + 0.078*CL
	t_F	3.74	0.98 + 0.055*CL	0.98 + 0.055*CL	0.98 + 0.055*CL
	t_{PLZ}	1.30	1.30 + 0.000*CL	1.30 + 0.000*CL	1.30 + 0.000*CL
	t_{PHZ}	1.09	1.09 + 0.000*CL	1.09 + 0.000*CL	1.09 + 0.000*CL
EN to PAD	t_{PLH}	3.28	1.50 + 0.036*CL	1.53 + 0.035*CL	1.53 + 0.035*CL
	t_{PHL}	3.82	2.22 + 0.032*CL	2.34 + 0.031*CL	2.39 + 0.030*CL
	t_R	4.34	0.49 + 0.077*CL	0.44 + 0.078*CL	0.43 + 0.078*CL
	t_F	3.74	0.98 + 0.055*CL	0.98 + 0.055*CL	0.98 + 0.055*CL
	t_{PLZ}	1.22	1.22 + 0.000*CL	1.22 + 0.000*CL	1.22 + 0.000*CL
	t_{PHZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT16SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.97	1.61 + 0.027*CL	1.68 + 0.026*CL	1.70 + 0.026*CL
	t_{PHL}	3.36	2.11 + 0.025*CL	2.21 + 0.024*CL	2.28 + 0.023*CL
	t_R	3.43	0.70 + 0.055*CL	0.68 + 0.055*CL	0.66 + 0.055*CL
	t_F	3.00	0.95 + 0.041*CL	1.01 + 0.040*CL	1.02 + 0.040*CL
TN to PAD	t_{PLH}	2.92	1.56 + 0.027*CL	1.63 + 0.026*CL	1.65 + 0.026*CL
	t_{PHL}	3.35	2.07 + 0.025*CL	2.21 + 0.024*CL	2.26 + 0.023*CL
	t_R	3.43	0.71 + 0.055*CL	0.68 + 0.055*CL	0.66 + 0.055*CL
	t_F	3.03	1.01 + 0.040*CL	1.05 + 0.040*CL	1.06 + 0.040*CL
	t_{PLZ}	1.27	1.27 + 0.000*CL	1.27 + 0.000*CL	1.27 + 0.000*CL
	t_{PHZ}	1.09	1.09 + 0.000*CL	1.09 + 0.000*CL	1.09 + 0.000*CL
EN to PAD	t_{PLH}	3.07	1.72 + 0.027*CL	1.78 + 0.026*CL	1.80 + 0.026*CL
	t_{PHL}	3.50	2.23 + 0.025*CL	2.36 + 0.024*CL	2.42 + 0.023*CL
	t_R	3.43	0.71 + 0.055*CL	0.68 + 0.055*CL	0.66 + 0.055*CL
	t_F	3.03	1.01 + 0.040*CL	1.05 + 0.040*CL	1.06 + 0.040*CL
	t_{PLZ}	1.19	1.19 + 0.000*CL	1.19 + 0.000*CL	1.19 + 0.000*CL
	t_{PHZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT20SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.36	1.30 + 0.021*CL	1.35 + 0.021*CL	1.36 + 0.020*CL
	t_{PHL}	2.38	1.52 + 0.017*CL	1.55 + 0.017*CL	1.57 + 0.017*CL
	t_R	2.71	0.57 + 0.043*CL	0.55 + 0.043*CL	0.53 + 0.043*CL
	t_F	2.23	0.71 + 0.030*CL	0.69 + 0.031*CL	0.68 + 0.031*CL
TN to PAD	t_{PLH}	2.31	1.25 + 0.021*CL	1.29 + 0.021*CL	1.32 + 0.020*CL
	t_{PHL}	2.29	1.35 + 0.019*CL	1.43 + 0.018*CL	1.47 + 0.017*CL
	t_R	2.72	0.59 + 0.043*CL	0.55 + 0.043*CL	0.54 + 0.043*CL
	t_F	2.22	0.67 + 0.031*CL	0.68 + 0.031*CL	0.67 + 0.031*CL
	t_{PLZ}	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.71 + 0.000*CL
	t_{PHZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
EN to PAD	t_{PLH}	2.47	1.41 + 0.021*CL	1.46 + 0.021*CL	1.47 + 0.020*CL
	t_{PHL}	2.44	1.51 + 0.019*CL	1.58 + 0.018*CL	1.63 + 0.017*CL
	t_R	2.72	0.59 + 0.043*CL	0.55 + 0.043*CL	0.54 + 0.043*CL
	t_F	2.22	0.67 + 0.031*CL	0.68 + 0.031*CL	0.67 + 0.031*CL
	t_{PLZ}	0.62	0.62 + 0.000*CL	0.62 + 0.000*CL	0.62 + 0.000*CL
	t_{PHZ}	0.83	0.83 + 0.000*CL	0.83 + 0.000*CL	0.83 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT24SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.35	1.38 + 0.019*CL	1.44 + 0.019*CL	1.47 + 0.018*CL
	t_{PHL}	2.45	1.66 + 0.016*CL	1.69 + 0.015*CL	1.72 + 0.015*CL
	t_R	2.53	0.65 + 0.038*CL	0.64 + 0.038*CL	0.63 + 0.038*CL
	t_F	2.15	0.82 + 0.027*CL	0.81 + 0.027*CL	0.79 + 0.027*CL
TN to PAD	t_{PLH}	2.30	1.33 + 0.020*CL	1.39 + 0.019*CL	1.42 + 0.018*CL
	t_{PHL}	2.30	1.42 + 0.018*CL	1.52 + 0.016*CL	1.55 + 0.016*CL
	t_R	2.55	0.68 + 0.037*CL	0.66 + 0.038*CL	0.64 + 0.038*CL
	t_F	2.12	0.74 + 0.028*CL	0.77 + 0.027*CL	0.76 + 0.027*CL
	t_{PLZ}	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.70 + 0.000*CL
	t_{PHZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
EN to PAD	t_{PLH}	2.46	1.48 + 0.020*CL	1.54 + 0.019*CL	1.58 + 0.018*CL
	t_{PHL}	2.46	1.57 + 0.018*CL	1.67 + 0.016*CL	1.71 + 0.016*CL
	t_R	2.55	0.68 + 0.037*CL	0.66 + 0.037*CL	0.64 + 0.038*CL
	t_F	2.12	0.74 + 0.028*CL	0.77 + 0.027*CL	0.76 + 0.027*CL
	t_{PLZ}	0.62	0.62 + 0.000*CL	0.63 + 0.000*CL	0.63 + 0.000*CL
	t_{PHZ}	0.83	0.83 + 0.000*CL	0.83 + 0.000*CL	0.83 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT4SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.59	0.90 + 0.094*CL	0.90 + 0.094*CL	0.90 + 0.094*CL
	t_{PHL}	5.18	1.45 + 0.074*CL	1.46 + 0.074*CL	1.47 + 0.074*CL
	t_R	10.83	0.24 + 0.212*CL	0.24 + 0.212*CL	0.23 + 0.212*CL
	t_F	8.06	0.42 + 0.153*CL	0.38 + 0.153*CL	0.35 + 0.154*CL
TN to PAD	t_{PLH}	5.55	0.85 + 0.094*CL	0.86 + 0.094*CL	0.86 + 0.094*CL
	t_{PHL}	5.19	1.47 + 0.074*CL	1.48 + 0.074*CL	1.49 + 0.074*CL
	t_R	10.83	0.24 + 0.212*CL	0.24 + 0.212*CL	0.23 + 0.212*CL
	t_F	8.06	0.42 + 0.153*CL	0.38 + 0.153*CL	0.35 + 0.154*CL
	t_{PLZ}	1.33	1.33 + 0.000*CL	1.33 + 0.000*CL	1.33 + 0.000*CL
	t_{PHZ}	1.10	1.10 + 0.000*CL	1.10 + 0.000*CL	1.10 + 0.000*CL
EN to PAD	t_{PLH}	5.70	1.01 + 0.094*CL	1.01 + 0.094*CL	1.01 + 0.094*CL
	t_{PHL}	5.35	1.63 + 0.074*CL	1.64 + 0.074*CL	1.64 + 0.074*CL
	t_R	10.83	0.24 + 0.212*CL	0.24 + 0.212*CL	0.23 + 0.212*CL
	t_F	8.06	0.42 + 0.153*CL	0.38 + 0.153*CL	0.35 + 0.154*CL
	t_{PLZ}	1.25	1.25 + 0.000*CL	1.25 + 0.000*CL	1.25 + 0.000*CL
	t_{PHZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT8SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.55	1.20 + 0.047*CL	1.20 + 0.047*CL	1.21 + 0.047*CL
	t_{PHL}	3.79	1.83 + 0.039*CL	1.89 + 0.038*CL	1.93 + 0.038*CL
	t_R	5.57	0.34 + 0.105*CL	0.31 + 0.105*CL	0.28 + 0.105*CL
	t_F	4.46	0.74 + 0.074*CL	0.72 + 0.075*CL	0.69 + 0.075*CL
TN to PAD	t_{PLH}	3.51	1.16 + 0.047*CL	1.16 + 0.047*CL	1.16 + 0.047*CL
	t_{PHL}	3.80	1.84 + 0.039*CL	1.91 + 0.038*CL	1.94 + 0.038*CL
	t_R	5.57	0.34 + 0.105*CL	0.31 + 0.105*CL	0.28 + 0.105*CL
	t_F	4.47	0.74 + 0.074*CL	0.72 + 0.075*CL	0.70 + 0.075*CL
	t_{PLZ}	1.30	1.30 + 0.000*CL	1.30 + 0.000*CL	1.30 + 0.000*CL
	t_{PHZ}	1.09	1.09 + 0.000*CL	1.09 + 0.000*CL	1.09 + 0.000*CL
EN to PAD	t_{PLH}	3.66	1.31 + 0.047*CL	1.31 + 0.047*CL	1.32 + 0.047*CL
	t_{PHL}	3.96	1.99 + 0.039*CL	2.07 + 0.038*CL	2.10 + 0.038*CL
	t_R	5.57	0.34 + 0.105*CL	0.31 + 0.105*CL	0.28 + 0.105*CL
	t_F	4.47	0.74 + 0.074*CL	0.72 + 0.075*CL	0.70 + 0.075*CL
	t_{PLZ}	1.22	1.22 + 0.000*CL	1.22 + 0.000*CL	1.22 + 0.000*CL
	t_{PHZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT12SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.98	1.24 + 0.035*CL	1.25 + 0.035*CL	1.26 + 0.035*CL
	t_{PHL}	3.29	1.75 + 0.031*CL	1.85 + 0.029*CL	1.89 + 0.029*CL
	t_R	4.22	0.41 + 0.076*CL	0.37 + 0.077*CL	0.35 + 0.077*CL
	t_F	3.55	0.81 + 0.055*CL	0.82 + 0.055*CL	0.82 + 0.055*CL
TN to PAD	t_{PLH}	2.93	1.19 + 0.035*CL	1.20 + 0.035*CL	1.21 + 0.035*CL
	t_{PHL}	3.30	1.76 + 0.031*CL	1.86 + 0.030*CL	1.91 + 0.029*CL
	t_R	4.22	0.41 + 0.076*CL	0.37 + 0.077*CL	0.36 + 0.077*CL
	t_F	3.55	0.82 + 0.055*CL	0.83 + 0.055*CL	0.82 + 0.055*CL
	t_{PLZ}	1.54	1.54 + 0.000*CL	1.54 + 0.000*CL	1.54 + 0.000*CL
	t_{PHZ}	1.39	1.39 + 0.000*CL	1.39 + 0.000*CL	1.38 + 0.000*CL
EN to PAD	t_{PLH}	3.09	1.34 + 0.035*CL	1.36 + 0.035*CL	1.36 + 0.035*CL
	t_{PHL}	3.46	1.92 + 0.031*CL	2.02 + 0.030*CL	2.06 + 0.029*CL
	t_R	4.22	0.41 + 0.076*CL	0.37 + 0.077*CL	0.36 + 0.077*CL
	t_F	3.55	0.82 + 0.055*CL	0.83 + 0.055*CL	0.82 + 0.055*CL
	t_{PLZ}	1.46	1.45 + 0.000*CL	1.45 + 0.000*CL	1.45 + 0.000*CL
	t_{PHZ}	1.31	1.30 + 0.000*CL	1.31 + 0.000*CL	1.31 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT16SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.66	1.34 + 0.026*CL	1.38 + 0.026*CL	1.40 + 0.026*CL
	t_{PHL}	2.86	1.68 + 0.024*CL	1.76 + 0.022*CL	1.81 + 0.022*CL
	t_R	3.28	0.53 + 0.055*CL	0.51 + 0.055*CL	0.49 + 0.056*CL
	t_F	2.77	0.73 + 0.041*CL	0.77 + 0.040*CL	0.78 + 0.040*CL
TN to PAD	t_{PLH}	2.61	1.29 + 0.026*CL	1.33 + 0.026*CL	1.34 + 0.026*CL
	t_{PHL}	2.86	1.66 + 0.024*CL	1.76 + 0.023*CL	1.80 + 0.022*CL
	t_R	3.29	0.54 + 0.055*CL	0.51 + 0.055*CL	0.49 + 0.056*CL
	t_F	2.79	0.76 + 0.040*CL	0.79 + 0.040*CL	0.80 + 0.040*CL
	t_{PLZ}	1.72	1.72 + 0.000*CL	1.71 + 0.000*CL	1.72 + 0.000*CL
	t_{PHZ}	1.65	1.65 + 0.000*CL	1.64 + 0.000*CL	1.65 + 0.000*CL
EN to PAD	t_{PLH}	2.76	1.44 + 0.026*CL	1.49 + 0.026*CL	1.50 + 0.026*CL
	t_{PHL}	3.02	1.82 + 0.024*CL	1.91 + 0.023*CL	1.97 + 0.022*CL
	t_R	3.29	0.54 + 0.055*CL	0.51 + 0.055*CL	0.49 + 0.056*CL
	t_F	2.79	0.76 + 0.040*CL	0.79 + 0.040*CL	0.80 + 0.040*CL
	t_{PLZ}	1.64	1.64 + 0.000*CL	1.64 + 0.000*CL	1.63 + 0.000*CL
	t_{PHZ}	1.57	1.57 + 0.000*CL	1.57 + 0.000*CL	1.56 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT20SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.03	1.02 + 0.020*CL	1.04 + 0.020*CL	1.04 + 0.020*CL
	t_{PHL}	2.01	1.13 + 0.018*CL	1.18 + 0.017*CL	1.21 + 0.017*CL
	t_R	2.53	0.36 + 0.043*CL	0.33 + 0.044*CL	0.32 + 0.044*CL
	t_F	2.11	0.54 + 0.031*CL	0.55 + 0.031*CL	0.54 + 0.031*CL
TN to PAD	t_{PLH}	2.00	0.99 + 0.020*CL	1.01 + 0.020*CL	1.01 + 0.020*CL
	t_{PHL}	2.01	1.11 + 0.018*CL	1.17 + 0.017*CL	1.21 + 0.017*CL
	t_R	2.53	0.37 + 0.043*CL	0.34 + 0.044*CL	0.32 + 0.044*CL
	t_F	2.12	0.57 + 0.031*CL	0.57 + 0.031*CL	0.57 + 0.031*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
	t_{PHZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.78 + 0.000*CL
EN to PAD	t_{PLH}	2.16	1.14 + 0.020*CL	1.16 + 0.020*CL	1.17 + 0.020*CL
	t_{PHL}	2.17	1.27 + 0.018*CL	1.33 + 0.017*CL	1.37 + 0.017*CL
	t_R	2.53	0.37 + 0.043*CL	0.34 + 0.044*CL	0.32 + 0.044*CL
	t_F	2.12	0.57 + 0.031*CL	0.57 + 0.031*CL	0.57 + 0.031*CL
	t_{PLZ}	0.79	0.79 + 0.000*CL	0.78 + 0.000*CL	0.79 + 0.000*CL
	t_{PHZ}	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.71 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 POT24SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.01	1.10 + 0.018*CL	1.12 + 0.018*CL	1.14 + 0.018*CL
	t_{PHL}	2.04	1.21 + 0.017*CL	1.27 + 0.016*CL	1.31 + 0.015*CL
	t_R	2.33	0.44 + 0.038*CL	0.42 + 0.038*CL	0.40 + 0.038*CL
	t_F	2.01	0.62 + 0.028*CL	0.64 + 0.028*CL	0.64 + 0.027*CL
TN to PAD	t_{PLH}	1.98	1.06 + 0.018*CL	1.10 + 0.018*CL	1.10 + 0.018*CL
	t_{PHL}	2.03	1.17 + 0.017*CL	1.25 + 0.016*CL	1.29 + 0.016*CL
	t_R	2.34	0.46 + 0.038*CL	0.43 + 0.038*CL	0.41 + 0.038*CL
	t_F	2.04	0.66 + 0.027*CL	0.67 + 0.027*CL	0.68 + 0.027*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
	t_{PHZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.79 + 0.000*CL
EN to PAD	t_{PLH}	2.13	1.21 + 0.018*CL	1.25 + 0.018*CL	1.26 + 0.018*CL
	t_{PHL}	2.18	1.33 + 0.017*CL	1.41 + 0.016*CL	1.45 + 0.016*CL
	t_R	2.34	0.46 + 0.038*CL	0.43 + 0.038*CL	0.41 + 0.038*CL
	t_F	2.04	0.66 + 0.027*CL	0.67 + 0.027*CL	0.68 + 0.027*CL
	t_{PLZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.79 + 0.000*CL
	t_{PHZ}	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.71 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	21.62	1.17 + 0.409*CL	1.17 + 0.409*CL	1.17 + 0.409*CL
	t_{PHL}	14.16	0.96 + 0.264*CL	0.96 + 0.264*CL	0.96 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
TN to PAD	t_{PLH}	21.41	1.49 + 0.398*CL	3.49 + 0.372*CL	6.57 + 0.335*CL
	t_{PHL}	14.16	0.96 + 0.264*CL	0.96 + 0.264*CL	0.96 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	1.04	1.04 + 0.000*CL	1.04 + 0.000*CL	1.04 + 0.000*CL
	t_{PHZ}	0.98	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL
EN to PAD	t_{PLH}	21.52	1.61 + 0.398*CL	3.63 + 0.371*CL	6.73 + 0.335*CL
	t_{PHL}	14.29	1.09 + 0.264*CL	1.08 + 0.264*CL	1.08 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.98	0.93 + 0.001*CL	1.00 + 0.000*CL	1.00 + 0.000*CL
	t_{PHZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	10.70	1.05 + 0.193*CL	1.05 + 0.193*CL	1.05 + 0.193*CL
	t_{PHL}	7.04	0.87 + 0.124*CL	0.87 + 0.124*CL	0.87 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
TN to PAD	t_{PLH}	10.50	0.85 + 0.193*CL	0.85 + 0.193*CL	0.87 + 0.193*CL
	t_{PHL}	7.05	0.87 + 0.124*CL	0.87 + 0.124*CL	0.87 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	1.13	1.13 + 0.000*CL	1.13 + 0.000*CL	1.13 + 0.000*CL
	t_{PHZ}	1.06	1.06 + 0.000*CL	1.05 + 0.000*CL	1.06 + 0.000*CL
EN to PAD	t_{PLH}	10.63	1.02 + 0.192*CL	0.84 + 0.195*CL	1.10 + 0.192*CL
	t_{PHL}	7.17	1.00 + 0.124*CL	1.00 + 0.124*CL	0.99 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	1.06	1.06 + 0.000*CL	1.06 + 0.000*CL	1.06 + 0.000*CL
	t_{PHZ}	1.02	1.05 + -0.001*CL	0.88 + 0.002*CL	1.02 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.81	0.98 + 0.096*CL	0.98 + 0.097*CL	0.98 + 0.096*CL
	t_{PHL}	4.00	0.92 + 0.062*CL	0.91 + 0.062*CL	0.91 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.16 + 0.133*CL	0.16 + 0.133*CL	0.15 + 0.133*CL
TN to PAD	t_{PLH}	5.60	0.78 + 0.096*CL	0.78 + 0.096*CL	0.78 + 0.096*CL
	t_{PHL}	4.00	0.92 + 0.062*CL	0.91 + 0.062*CL	0.92 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.15 + 0.133*CL	0.16 + 0.133*CL	0.15 + 0.133*CL
	t_{PLZ}	1.25	1.25 + 0.000*CL	1.25 + 0.000*CL	1.25 + 0.000*CL
	t_{PHZ}	1.70	1.70 + 0.000*CL	1.70 + 0.000*CL	1.70 + 0.000*CL
EN to PAD	t_{PLH}	5.72	0.90 + 0.096*CL	0.90 + 0.097*CL	0.90 + 0.096*CL
	t_{PHL}	4.14	1.06 + 0.062*CL	1.05 + 0.062*CL	1.06 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.15 + 0.133*CL	0.14 + 0.133*CL	0.16 + 0.133*CL
	t_{PLZ}	1.19	1.19 + 0.000*CL	1.14 + 0.001*CL	1.19 + 0.000*CL
	t_{PHZ}	1.65	1.65 + 0.000*CL	1.72 + -0.001*CL	1.64 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.26	1.04 + 0.064*CL	1.04 + 0.064*CL	1.05 + 0.064*CL
	t_{PHL}	3.07	1.02 + 0.041*CL	1.01 + 0.041*CL	1.01 + 0.041*CL
	t_R	7.52	0.20 + 0.146*CL	0.19 + 0.146*CL	0.20 + 0.146*CL
	t_F	4.58	0.17 + 0.088*CL	0.14 + 0.089*CL	0.14 + 0.089*CL
TN to PAD	t_{PLH}	4.05	0.84 + 0.064*CL	0.82 + 0.064*CL	0.85 + 0.064*CL
	t_{PHL}	3.05	0.99 + 0.041*CL	0.99 + 0.041*CL	0.99 + 0.041*CL
	t_R	7.52	0.19 + 0.146*CL	0.19 + 0.146*CL	0.20 + 0.146*CL
	t_F	4.57	0.14 + 0.089*CL	0.12 + 0.089*CL	0.13 + 0.089*CL
	t_{PLZ}	1.40	1.40 + 0.000*CL	1.54 + -0.002*CL	1.38 + 0.000*CL
	t_{PHZ}	2.09	2.09 + 0.000*CL	2.09 + 0.000*CL	2.09 + 0.000*CL
EN to PAD	t_{PLH}	4.17	0.95 + 0.064*CL	0.94 + 0.064*CL	0.96 + 0.064*CL
	t_{PHL}	3.19	1.13 + 0.041*CL	1.13 + 0.041*CL	1.14 + 0.041*CL
	t_R	7.52	0.19 + 0.146*CL	0.19 + 0.147*CL	0.20 + 0.146*CL
	t_F	4.57	0.14 + 0.089*CL	0.14 + 0.089*CL	0.12 + 0.089*CL
	t_{PLZ}	1.35	1.41 + -0.001*CL	1.32 + 0.000*CL	1.32 + 0.000*CL
	t_{PHZ}	2.02	2.02 + 0.000*CL	2.02 + 0.000*CL	2.02 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.52	1.11 + 0.048*CL	1.11 + 0.048*CL	1.11 + 0.048*CL
	t_{PHL}	2.67	1.15 + 0.030*CL	1.14 + 0.031*CL	1.13 + 0.031*CL
	t_R	5.66	0.18 + 0.110*CL	0.16 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.51	0.24 + 0.065*CL	0.20 + 0.066*CL	0.18 + 0.066*CL
TN to PAD	t_{PLH}	3.32	0.90 + 0.048*CL	0.89 + 0.048*CL	0.92 + 0.048*CL
	t_{PHL}	2.62	1.08 + 0.031*CL	1.08 + 0.031*CL	1.08 + 0.031*CL
	t_R	5.66	0.18 + 0.110*CL	0.17 + 0.110*CL	0.16 + 0.110*CL
	t_F	3.47	0.17 + 0.066*CL	0.15 + 0.066*CL	0.14 + 0.066*CL
	t_{PLZ}	1.51	1.47 + 0.001*CL	1.68 + -0.002*CL	1.40 + 0.001*CL
	t_{PHZ}	2.48	2.47 + 0.000*CL	2.48 + 0.000*CL	2.48 + 0.000*CL
EN to PAD	t_{PLH}	3.45	1.07 + 0.048*CL	0.89 + 0.050*CL	1.14 + 0.047*CL
	t_{PHL}	2.77	1.22 + 0.031*CL	1.22 + 0.031*CL	1.22 + 0.031*CL
	t_R	5.66	0.18 + 0.110*CL	0.17 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.47	0.17 + 0.066*CL	0.14 + 0.066*CL	0.15 + 0.066*CL
	t_{PLZ}	1.45	1.45 + 0.000*CL	1.44 + 0.000*CL	1.31 + 0.002*CL
	t_{PHZ}	2.41	2.41 + 0.000*CL	2.41 + 0.000*CL	2.40 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT10 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.16	1.23 + 0.039*CL	1.23 + 0.039*CL	1.23 + 0.039*CL
	t_{PHL}	2.41	1.18 + 0.025*CL	1.17 + 0.025*CL	1.18 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.18 + 0.088*CL	0.16 + 0.088*CL
	t_F	2.83	0.21 + 0.052*CL	0.17 + 0.053*CL	0.20 + 0.053*CL
TN to PAD	t_{PLH}	2.95	1.01 + 0.039*CL	1.02 + 0.039*CL	0.99 + 0.039*CL
	t_{PHL}	2.40	1.16 + 0.025*CL	1.18 + 0.025*CL	1.17 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.18 + 0.088*CL	0.16 + 0.088*CL
	t_F	2.84	0.23 + 0.052*CL	0.18 + 0.053*CL	0.20 + 0.053*CL
	t_{PLZ}	1.65	1.68 + -0.001*CL	1.55 + 0.001*CL	1.72 + -0.001*CL
	t_{PHZ}	1.88	1.88 + 0.000*CL	1.88 + 0.000*CL	1.88 + 0.000*CL
EN to PAD	t_{PLH}	3.07	1.13 + 0.039*CL	1.14 + 0.039*CL	1.13 + 0.039*CL
	t_{PHL}	2.55	1.31 + 0.025*CL	1.30 + 0.025*CL	1.31 + 0.025*CL
	t_R	4.56	0.19 + 0.088*CL	0.18 + 0.088*CL	0.16 + 0.088*CL
	t_F	2.83	0.21 + 0.052*CL	0.21 + 0.052*CL	0.17 + 0.053*CL
	t_{PLZ}	1.57	1.53 + 0.001*CL	1.77 + -0.002*CL	1.57 + 0.000*CL
	t_{PHZ}	1.82	1.82 + 0.000*CL	1.82 + 0.000*CL	1.82 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.95	1.34 + 0.032*CL	1.34 + 0.032*CL	1.34 + 0.032*CL
	t_{PHL}	2.28	1.24 + 0.021*CL	1.25 + 0.021*CL	1.25 + 0.021*CL
	t_R	3.84	0.21 + 0.073*CL	0.20 + 0.073*CL	0.16 + 0.073*CL
	t_F	2.43	0.26 + 0.043*CL	0.26 + 0.043*CL	0.22 + 0.044*CL
TN to PAD	t_{PLH}	2.74	1.12 + 0.032*CL	1.13 + 0.032*CL	1.14 + 0.032*CL
	t_{PHL}	2.28	1.24 + 0.021*CL	1.26 + 0.021*CL	1.26 + 0.021*CL
	t_R	3.84	0.21 + 0.073*CL	0.18 + 0.073*CL	0.18 + 0.073*CL
	t_F	2.43	0.27 + 0.043*CL	0.25 + 0.043*CL	0.24 + 0.044*CL
	t_{PLZ}	1.76	1.74 + 0.000*CL	1.77 + 0.000*CL	1.76 + 0.000*CL
	t_{PHZ}	1.69	1.69 + 0.000*CL	1.69 + 0.000*CL	1.69 + 0.000*CL
EN to PAD	t_{PLH}	2.86	1.25 + 0.032*CL	1.13 + 0.034*CL	1.36 + 0.031*CL
	t_{PHL}	2.40	1.37 + 0.021*CL	1.37 + 0.021*CL	1.37 + 0.021*CL
	t_R	3.84	0.20 + 0.073*CL	0.19 + 0.073*CL	0.18 + 0.073*CL
	t_F	2.43	0.26 + 0.043*CL	0.26 + 0.043*CL	0.22 + 0.044*CL
	t_{PLZ}	1.73	1.72 + 0.000*CL	1.72 + 0.000*CL	1.85 + -0.002*CL
	t_{PHZ}	1.63	1.63 + 0.000*CL	1.63 + 0.000*CL	1.63 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.71	1.49 + 0.024*CL	1.49 + 0.024*CL	1.49 + 0.024*CL
	t_{PHL}	2.20	1.38 + 0.016*CL	1.40 + 0.016*CL	1.41 + 0.016*CL
	t_R	3.00	0.26 + 0.055*CL	0.24 + 0.055*CL	0.23 + 0.055*CL
	t_F	1.98	0.36 + 0.032*CL	0.38 + 0.032*CL	0.31 + 0.033*CL
TN to PAD	t_{PLH}	2.49	1.26 + 0.025*CL	1.26 + 0.025*CL	1.26 + 0.025*CL
	t_{PHL}	2.19	1.37 + 0.016*CL	1.40 + 0.016*CL	1.40 + 0.016*CL
	t_R	3.01	0.27 + 0.055*CL	0.27 + 0.055*CL	0.23 + 0.055*CL
	t_F	1.99	0.36 + 0.032*CL	0.38 + 0.032*CL	0.35 + 0.033*CL
	t_{PLZ}	2.01	1.99 + 0.000*CL	2.00 + 0.000*CL	2.00 + 0.000*CL
	t_{PHZ}	1.94	1.93 + 0.000*CL	1.93 + 0.000*CL	1.93 + 0.000*CL
EN to PAD	t_{PLH}	2.61	1.38 + 0.025*CL	1.38 + 0.025*CL	1.39 + 0.025*CL
	t_{PHL}	2.31	1.49 + 0.016*CL	1.52 + 0.016*CL	1.53 + 0.016*CL
	t_R	3.01	0.28 + 0.055*CL	0.23 + 0.055*CL	0.23 + 0.055*CL
	t_F	1.99	0.37 + 0.032*CL	0.32 + 0.033*CL	0.35 + 0.033*CL
	t_{PLZ}	1.96	1.99 + -0.001*CL	1.94 + 0.000*CL	1.81 + 0.002*CL
	t_{PHZ}	1.88	1.87 + 0.000*CL	1.87 + 0.000*CL	1.87 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	6.25	1.28 + 0.099*CL	1.28 + 0.099*CL	1.28 + 0.099*CL
	t_{PHL}	4.52	1.33 + 0.064*CL	1.33 + 0.064*CL	1.33 + 0.064*CL
	t_R	11.58	0.27 + 0.226*CL	0.27 + 0.226*CL	0.28 + 0.226*CL
	t_F	7.10	0.27 + 0.137*CL	0.23 + 0.137*CL	0.22 + 0.137*CL
TN to PAD	t_{PLH}	6.03	1.06 + 0.099*CL	1.06 + 0.099*CL	1.06 + 0.099*CL
	t_{PHL}	4.53	1.34 + 0.064*CL	1.34 + 0.064*CL	1.34 + 0.064*CL
	t_R	11.58	0.28 + 0.226*CL	0.27 + 0.226*CL	0.27 + 0.226*CL
	t_F	7.10	0.27 + 0.137*CL	0.23 + 0.137*CL	0.23 + 0.137*CL
	t_{PLZ}	1.19	1.16 + 0.001*CL	1.20 + 0.000*CL	1.20 + 0.000*CL
	t_{PHZ}	1.09	1.09 + 0.000*CL	1.09 + 0.000*CL	1.09 + 0.000*CL
EN to PAD	t_{PLH}	6.15	1.18 + 0.099*CL	1.18 + 0.099*CL	1.18 + 0.099*CL
	t_{PHL}	4.67	1.48 + 0.064*CL	1.47 + 0.064*CL	1.48 + 0.064*CL
	t_R	11.58	0.27 + 0.226*CL	0.27 + 0.226*CL	0.28 + 0.226*CL
	t_F	7.10	0.26 + 0.137*CL	0.23 + 0.137*CL	0.22 + 0.137*CL
	t_{PLZ}	1.15	1.20 + -0.001*CL	1.12 + 0.000*CL	1.12 + 0.000*CL
	t_{PHZ}	1.03	1.03 + 0.000*CL	1.03 + 0.000*CL	1.03 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT6SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.76	1.48 + 0.066*CL	1.48 + 0.066*CL	1.48 + 0.066*CL
	t_{PHL}	3.76	1.65 + 0.042*CL	1.66 + 0.042*CL	1.67 + 0.042*CL
	t_R	7.71	0.26 + 0.149*CL	0.24 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.41 + 0.089*CL	0.37 + 0.089*CL
TN to PAD	t_{PLH}	4.53	1.25 + 0.066*CL	1.25 + 0.066*CL	1.25 + 0.066*CL
	t_{PHL}	3.77	1.65 + 0.042*CL	1.66 + 0.042*CL	1.68 + 0.042*CL
	t_R	7.71	0.26 + 0.149*CL	0.25 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.47 + 0.088*CL	0.41 + 0.089*CL	0.39 + 0.089*CL
	t_{PLZ}	1.14	1.14 + 0.000*CL	1.14 + 0.000*CL	1.14 + 0.000*CL
	t_{PHZ}	1.06	1.06 + 0.000*CL	1.06 + 0.000*CL	1.06 + 0.000*CL
EN to PAD	t_{PLH}	4.65	1.37 + 0.066*CL	1.37 + 0.066*CL	1.37 + 0.066*CL
	t_{PHL}	3.89	1.78 + 0.042*CL	1.78 + 0.042*CL	1.79 + 0.042*CL
	t_R	7.71	0.27 + 0.149*CL	0.24 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.40 + 0.089*CL	0.39 + 0.089*CL
	t_{PLZ}	1.09	1.09 + 0.000*CL	1.26 + -0.002*CL	1.06 + 0.000*CL
	t_{PHZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.10	1.65 + 0.049*CL	1.65 + 0.049*CL	1.66 + 0.049*CL
	t_{PHL}	3.55	1.92 + 0.033*CL	1.97 + 0.032*CL	1.99 + 0.032*CL
	t_R	5.85	0.33 + 0.110*CL	0.29 + 0.111*CL	0.28 + 0.111*CL
	t_F	3.91	0.68 + 0.065*CL	0.64 + 0.065*CL	0.58 + 0.066*CL
TN to PAD	t_{PLH}	3.88	1.42 + 0.049*CL	1.43 + 0.049*CL	1.43 + 0.049*CL
	t_{PHL}	3.56	1.92 + 0.033*CL	1.97 + 0.032*CL	1.99 + 0.032*CL
	t_R	5.85	0.33 + 0.110*CL	0.30 + 0.111*CL	0.29 + 0.111*CL
	t_F	3.91	0.68 + 0.065*CL	0.67 + 0.065*CL	0.60 + 0.066*CL
	t_{PLZ}	1.12	1.12 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL
	t_{PHZ}	1.06	1.06 + 0.000*CL	1.06 + 0.000*CL	1.06 + 0.000*CL
EN to PAD	t_{PLH}	3.99	1.54 + 0.049*CL	1.55 + 0.049*CL	1.55 + 0.049*CL
	t_{PHL}	3.68	2.04 + 0.033*CL	2.09 + 0.032*CL	2.11 + 0.032*CL
	t_R	5.85	0.33 + 0.110*CL	0.30 + 0.111*CL	0.29 + 0.111*CL
	t_F	3.91	0.68 + 0.065*CL	0.64 + 0.065*CL	0.61 + 0.065*CL
	t_{PLZ}	1.09	1.14 + -0.001*CL	1.07 + 0.000*CL	1.07 + 0.000*CL
	t_{PHZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT10SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.57	1.64 + 0.039*CL	1.64 + 0.039*CL	1.65 + 0.039*CL
	t_{PHL}	3.21	1.86 + 0.027*CL	1.94 + 0.026*CL	1.97 + 0.026*CL
	t_R	4.71	0.40 + 0.086*CL	0.34 + 0.087*CL	0.34 + 0.087*CL
	t_F	3.35	0.86 + 0.050*CL	0.85 + 0.050*CL	0.78 + 0.051*CL
TN to PAD	t_{PLH}	3.35	1.41 + 0.039*CL	1.43 + 0.039*CL	1.41 + 0.039*CL
	t_{PHL}	3.21	1.85 + 0.027*CL	1.93 + 0.026*CL	1.97 + 0.026*CL
	t_R	4.70	0.39 + 0.086*CL	0.35 + 0.087*CL	0.32 + 0.087*CL
	t_F	3.35	0.87 + 0.050*CL	0.85 + 0.050*CL	0.80 + 0.051*CL
	t_{PLZ}	1.26	1.24 + 0.000*CL	1.27 + 0.000*CL	1.27 + 0.000*CL
	t_{PHZ}	1.19	1.19 + 0.000*CL	1.19 + 0.000*CL	1.19 + 0.000*CL
EN to PAD	t_{PLH}	3.46	1.53 + 0.039*CL	1.53 + 0.039*CL	1.53 + 0.039*CL
	t_{PHL}	3.33	1.97 + 0.027*CL	2.06 + 0.026*CL	2.09 + 0.026*CL
	t_R	4.70	0.40 + 0.086*CL	0.35 + 0.087*CL	0.32 + 0.087*CL
	t_F	3.35	0.88 + 0.050*CL	0.85 + 0.050*CL	0.80 + 0.050*CL
	t_{PLZ}	1.23	1.28 + -0.001*CL	1.01 + 0.003*CL	1.38 + -0.002*CL
	t_{PHZ}	1.13	1.13 + 0.000*CL	1.13 + 0.000*CL	1.13 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.42	1.79 + 0.033*CL	1.80 + 0.032*CL	1.82 + 0.032*CL
	t_{PHL}	3.25	2.02 + 0.025*CL	2.13 + 0.023*CL	2.19 + 0.022*CL
	t_R	4.06	0.50 + 0.071*CL	0.46 + 0.072*CL	0.43 + 0.072*CL
	t_F	3.10	1.03 + 0.041*CL	1.03 + 0.041*CL	1.02 + 0.041*CL
TN to PAD	t_{PLH}	3.19	1.56 + 0.033*CL	1.56 + 0.033*CL	1.60 + 0.032*CL
	t_{PHL}	3.24	2.00 + 0.025*CL	2.12 + 0.023*CL	2.17 + 0.023*CL
	t_R	4.06	0.52 + 0.071*CL	0.44 + 0.072*CL	0.45 + 0.072*CL
	t_F	3.12	1.08 + 0.041*CL	1.07 + 0.041*CL	1.04 + 0.041*CL
	t_{PLZ}	1.27	1.27 + 0.000*CL	1.27 + 0.000*CL	1.27 + 0.000*CL
	t_{PHZ}	1.19	1.19 + 0.000*CL	1.19 + 0.000*CL	1.19 + 0.000*CL
EN to PAD	t_{PLH}	3.31	1.68 + 0.033*CL	1.69 + 0.032*CL	1.71 + 0.032*CL
	t_{PHL}	3.36	2.12 + 0.025*CL	2.24 + 0.023*CL	2.30 + 0.023*CL
	t_R	4.06	0.51 + 0.071*CL	0.47 + 0.072*CL	0.43 + 0.072*CL
	t_F	3.11	1.07 + 0.041*CL	1.04 + 0.041*CL	1.04 + 0.041*CL
	t_{PLZ}	1.23	1.28 + -0.001*CL	1.20 + 0.000*CL	1.06 + 0.002*CL
	t_{PHZ}	1.13	1.13 + 0.000*CL	1.13 + 0.000*CL	1.13 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STD80 PLOT16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.35	2.06 + 0.026*CL	2.11 + 0.025*CL	2.13 + 0.025*CL
	t_{PHL}	3.43	2.31 + 0.022*CL	2.45 + 0.020*CL	2.53 + 0.020*CL
	t_R	3.38	0.74 + 0.053*CL	0.69 + 0.053*CL	0.64 + 0.054*CL
	t_F	2.88	1.25 + 0.033*CL	1.31 + 0.032*CL	1.29 + 0.032*CL
TN to PAD	t_{PLH}	3.11	1.82 + 0.026*CL	1.86 + 0.025*CL	1.90 + 0.025*CL
	t_{PHL}	3.40	2.26 + 0.023*CL	2.42 + 0.021*CL	2.50 + 0.020*CL
	t_R	3.39	0.76 + 0.053*CL	0.71 + 0.053*CL	0.68 + 0.054*CL
	t_F	2.94	1.37 + 0.031*CL	1.40 + 0.031*CL	1.38 + 0.031*CL
	t_{PLZ}	1.25	1.25 + 0.000*CL	1.25 + 0.000*CL	1.17 + 0.001*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL
EN to PAD	t_{PLH}	3.23	1.93 + 0.026*CL	1.98 + 0.025*CL	2.01 + 0.025*CL
	t_{PHL}	3.52	2.38 + 0.023*CL	2.54 + 0.021*CL	2.63 + 0.020*CL
	t_R	3.38	0.76 + 0.053*CL	0.70 + 0.053*CL	0.67 + 0.054*CL
	t_F	2.94	1.36 + 0.032*CL	1.40 + 0.031*CL	1.38 + 0.031*CL
	t_{PLZ}	1.20	1.19 + 0.000*CL	1.19 + 0.000*CL	1.19 + 0.000*CL
	t_{PHZ}	1.12	1.12 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	21.36	0.92 + 0.409*CL	0.92 + 0.409*CL	0.92 + 0.409*CL
	t_{PHL}	14.04	0.84 + 0.264*CL	0.84 + 0.264*CL	0.84 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
TN to PAD	t_{PLH}	21.33	1.42 + 0.398*CL	3.44 + 0.371*CL	6.52 + 0.335*CL
	t_{PHL}	14.08	0.88 + 0.264*CL	0.88 + 0.264*CL	0.88 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.86	0.86 + 0.000*CL	0.86 + 0.000*CL	0.86 + 0.000*CL
	t_{PHZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.79 + 0.000*CL
EN to PAD	t_{PLH}	21.52	1.61 + 0.398*CL	3.67 + 0.371*CL	6.79 + 0.334*CL
	t_{PHL}	14.28	1.08 + 0.264*CL	1.08 + 0.264*CL	1.08 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.77	0.77 + 0.000*CL	0.76 + 0.000*CL	0.76 + 0.000*CL
	t_{PHZ}	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.71 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	10.45	0.80 + 0.193*CL	0.80 + 0.193*CL	0.80 + 0.193*CL
	t_{PHL}	6.93	0.75 + 0.124*CL	0.75 + 0.124*CL	0.75 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
TN to PAD	t_{PLH}	10.43	0.78 + 0.193*CL	0.78 + 0.193*CL	0.79 + 0.193*CL
	t_{PHL}	6.97	0.79 + 0.124*CL	0.80 + 0.123*CL	0.79 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	0.95	0.95 + 0.000*CL	0.95 + 0.000*CL	0.95 + 0.000*CL
	t_{PHZ}	0.86	0.86 + 0.000*CL	0.86 + 0.000*CL	0.86 + 0.000*CL
EN to PAD	t_{PLH}	10.62	0.97 + 0.193*CL	0.97 + 0.193*CL	0.99 + 0.193*CL
	t_{PHL}	7.16	0.99 + 0.124*CL	0.98 + 0.124*CL	0.99 + 0.123*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
	t_{PHZ}	0.79	0.79 + 0.000*CL	0.78 + 0.000*CL	0.79 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.55	0.72 + 0.097*CL	0.73 + 0.096*CL	0.73 + 0.096*CL
	t_{PHL}	3.89	0.80 + 0.062*CL	0.80 + 0.062*CL	0.80 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.16 + 0.133*CL	0.16 + 0.133*CL	0.15 + 0.133*CL
TN to PAD	t_{PLH}	5.53	0.71 + 0.096*CL	0.71 + 0.097*CL	0.71 + 0.097*CL
	t_{PHL}	3.92	0.83 + 0.062*CL	0.83 + 0.062*CL	0.83 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.15 + 0.133*CL	0.15 + 0.133*CL	0.15 + 0.133*CL
	t_{PLZ}	1.08	1.07 + 0.000*CL	1.08 + 0.000*CL	1.06 + 0.000*CL
	t_{PHZ}	1.52	1.50 + 0.000*CL	1.51 + 0.000*CL	1.51 + 0.000*CL
EN to PAD	t_{PLH}	5.72	0.89 + 0.097*CL	0.89 + 0.097*CL	0.89 + 0.097*CL
	t_{PHL}	4.11	1.02 + 0.062*CL	1.02 + 0.062*CL	1.03 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.15 + 0.133*CL	0.16 + 0.133*CL	0.15 + 0.133*CL
	t_{PLZ}	0.98	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL
	t_{PHZ}	1.40	1.40 + 0.000*CL	1.40 + 0.000*CL	1.40 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.00	0.79 + 0.064*CL	0.79 + 0.064*CL	0.78 + 0.064*CL
	t_{PHL}	2.95	0.91 + 0.041*CL	0.90 + 0.041*CL	0.90 + 0.041*CL
	t_R	7.52	0.19 + 0.146*CL	0.20 + 0.146*CL	0.20 + 0.146*CL
	t_F	4.58	0.16 + 0.088*CL	0.15 + 0.089*CL	0.13 + 0.089*CL
TN to PAD	t_{PLH}	3.98	0.77 + 0.064*CL	0.76 + 0.064*CL	0.77 + 0.064*CL
	t_{PHL}	2.97	0.91 + 0.041*CL	0.91 + 0.041*CL	0.91 + 0.041*CL
	t_R	7.52	0.19 + 0.146*CL	0.19 + 0.147*CL	0.20 + 0.146*CL
	t_F	4.57	0.14 + 0.089*CL	0.13 + 0.089*CL	0.13 + 0.089*CL
	t_{PLZ}	1.21	1.21 + 0.000*CL	1.21 + 0.000*CL	1.20 + 0.000*CL
	t_{PHZ}	1.89	1.89 + 0.000*CL	1.89 + 0.000*CL	1.89 + 0.000*CL
EN to PAD	t_{PLH}	4.17	0.95 + 0.064*CL	0.95 + 0.064*CL	0.95 + 0.064*CL
	t_{PHL}	3.16	1.10 + 0.041*CL	1.10 + 0.041*CL	1.11 + 0.041*CL
	t_R	7.52	0.19 + 0.146*CL	0.20 + 0.146*CL	0.19 + 0.146*CL
	t_F	4.57	0.14 + 0.089*CL	0.14 + 0.089*CL	0.13 + 0.089*CL
	t_{PLZ}	1.13	1.18 + -0.001*CL	1.11 + 0.000*CL	1.11 + 0.000*CL
	t_{PHZ}	1.79	1.78 + 0.000*CL	1.78 + 0.000*CL	1.78 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.27	0.86 + 0.048*CL	0.85 + 0.048*CL	0.86 + 0.048*CL
	t_{PHL}	2.55	1.04 + 0.030*CL	1.02 + 0.031*CL	1.01 + 0.031*CL
	t_R	5.66	0.17 + 0.110*CL	0.17 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.51	0.25 + 0.065*CL	0.20 + 0.066*CL	0.18 + 0.066*CL
TN to PAD	t_{PLH}	3.25	0.83 + 0.048*CL	0.83 + 0.048*CL	0.83 + 0.048*CL
	t_{PHL}	2.54	1.00 + 0.031*CL	0.99 + 0.031*CL	1.00 + 0.031*CL
	t_R	5.66	0.17 + 0.110*CL	0.17 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.47	0.17 + 0.066*CL	0.15 + 0.066*CL	0.15 + 0.066*CL
	t_{PLZ}	1.33	1.32 + 0.000*CL	1.39 + -0.001*CL	1.33 + 0.000*CL
	t_{PHZ}	2.28	2.28 + 0.000*CL	2.28 + 0.000*CL	2.28 + 0.000*CL
EN to PAD	t_{PLH}	3.43	1.02 + 0.048*CL	1.02 + 0.048*CL	1.02 + 0.048*CL
	t_{PHL}	2.73	1.18 + 0.031*CL	1.19 + 0.031*CL	1.18 + 0.031*CL
	t_R	5.66	0.17 + 0.110*CL	0.17 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.47	0.17 + 0.066*CL	0.16 + 0.066*CL	0.14 + 0.066*CL
	t_{PLZ}	1.24	1.24 + 0.000*CL	1.24 + 0.000*CL	1.24 + 0.000*CL
	t_{PHZ}	2.17	2.17 + 0.000*CL	2.17 + 0.000*CL	2.17 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT10 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.90	0.97 + 0.039*CL	0.97 + 0.039*CL	0.97 + 0.039*CL
	t_{PHL}	2.29	1.06 + 0.025*CL	1.05 + 0.025*CL	1.06 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.18 + 0.088*CL	0.16 + 0.088*CL
	t_F	2.83	0.22 + 0.052*CL	0.17 + 0.053*CL	0.19 + 0.053*CL
TN to PAD	t_{PLH}	2.88	0.95 + 0.039*CL	0.94 + 0.039*CL	0.95 + 0.039*CL
	t_{PHL}	2.32	1.08 + 0.025*CL	1.09 + 0.025*CL	1.09 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.17 + 0.088*CL	0.16 + 0.088*CL
	t_F	2.84	0.22 + 0.052*CL	0.18 + 0.053*CL	0.19 + 0.053*CL
	t_{PLZ}	1.46	1.46 + 0.000*CL	1.44 + 0.000*CL	1.45 + 0.000*CL
	t_{PHZ}	1.69	1.69 + 0.000*CL	1.69 + 0.000*CL	1.69 + 0.000*CL
EN to PAD	t_{PLH}	3.07	1.14 + 0.039*CL	1.13 + 0.039*CL	1.14 + 0.039*CL
	t_{PHL}	2.51	1.28 + 0.025*CL	1.28 + 0.025*CL	1.28 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.16 + 0.088*CL	0.17 + 0.088*CL
	t_F	2.83	0.22 + 0.052*CL	0.19 + 0.053*CL	0.18 + 0.053*CL
	t_{PLZ}	1.37	1.37 + 0.000*CL	1.36 + 0.000*CL	1.37 + 0.000*CL
	t_{PHZ}	1.58	1.58 + 0.000*CL	1.58 + 0.000*CL	1.58 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.70	1.09 + 0.032*CL	1.09 + 0.032*CL	1.08 + 0.032*CL
	t_{PHL}	2.16	1.13 + 0.021*CL	1.14 + 0.021*CL	1.13 + 0.021*CL
	t_R	3.84	0.20 + 0.073*CL	0.18 + 0.073*CL	0.17 + 0.073*CL
	t_F	2.42	0.26 + 0.043*CL	0.23 + 0.044*CL	0.24 + 0.044*CL
TN to PAD	t_{PLH}	2.67	1.06 + 0.032*CL	1.06 + 0.032*CL	1.07 + 0.032*CL
	t_{PHL}	2.20	1.16 + 0.021*CL	1.18 + 0.021*CL	1.17 + 0.021*CL
	t_R	3.84	0.21 + 0.073*CL	0.18 + 0.073*CL	0.18 + 0.073*CL
	t_F	2.43	0.26 + 0.043*CL	0.26 + 0.043*CL	0.24 + 0.044*CL
	t_{PLZ}	1.59	1.58 + 0.000*CL	1.58 + 0.000*CL	1.59 + 0.000*CL
	t_{PHZ}	1.50	1.50 + 0.000*CL	1.50 + 0.000*CL	1.50 + 0.000*CL
EN to PAD	t_{PLH}	2.86	1.25 + 0.032*CL	1.25 + 0.032*CL	1.25 + 0.032*CL
	t_{PHL}	2.39	1.36 + 0.021*CL	1.36 + 0.021*CL	1.37 + 0.021*CL
	t_R	3.84	0.21 + 0.073*CL	0.18 + 0.073*CL	0.18 + 0.073*CL
	t_F	2.43	0.28 + 0.043*CL	0.26 + 0.043*CL	0.24 + 0.044*CL
	t_{PLZ}	1.49	1.49 + 0.000*CL	1.49 + 0.000*CL	1.49 + 0.000*CL
	t_{PHZ}	1.43	1.38 + 0.001*CL	1.45 + 0.000*CL	1.45 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.46	1.24 + 0.024*CL	1.24 + 0.024*CL	1.24 + 0.024*CL
	t_{PHL}	2.08	1.27 + 0.016*CL	1.29 + 0.016*CL	1.30 + 0.016*CL
	t_R	3.00	0.26 + 0.055*CL	0.23 + 0.055*CL	0.23 + 0.055*CL
	t_F	1.98	0.34 + 0.033*CL	0.34 + 0.033*CL	0.34 + 0.033*CL
TN to PAD	t_{PLH}	2.42	1.19 + 0.025*CL	1.20 + 0.025*CL	1.20 + 0.025*CL
	t_{PHL}	2.11	1.29 + 0.016*CL	1.32 + 0.016*CL	1.33 + 0.016*CL
	t_R	3.01	0.27 + 0.055*CL	0.24 + 0.055*CL	0.24 + 0.055*CL
	t_F	1.98	0.35 + 0.033*CL	0.35 + 0.033*CL	0.32 + 0.033*CL
	t_{PLZ}	1.83	1.83 + 0.000*CL	1.83 + 0.000*CL	1.83 + 0.000*CL
	t_{PHZ}	1.74	1.74 + 0.000*CL	1.74 + 0.000*CL	1.74 + 0.000*CL
EN to PAD	t_{PLH}	2.61	1.38 + 0.025*CL	1.38 + 0.025*CL	1.39 + 0.025*CL
	t_{PHL}	2.30	1.48 + 0.016*CL	1.51 + 0.016*CL	1.52 + 0.016*CL
	t_R	3.01	0.28 + 0.055*CL	0.24 + 0.055*CL	0.23 + 0.055*CL
	t_F	1.98	0.36 + 0.032*CL	0.36 + 0.032*CL	0.32 + 0.033*CL
	t_{PLZ}	1.73	1.73 + 0.000*CL	1.73 + 0.000*CL	1.72 + 0.000*CL
	t_{PHZ}	1.66	1.65 + 0.000*CL	1.66 + 0.000*CL	1.65 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.99	1.03 + 0.099*CL	1.03 + 0.099*CL	1.03 + 0.099*CL
	t_{PHL}	4.41	1.22 + 0.064*CL	1.22 + 0.064*CL	1.22 + 0.064*CL
	t_R	11.58	0.28 + 0.226*CL	0.28 + 0.226*CL	0.28 + 0.226*CL
	t_F	7.10	0.27 + 0.137*CL	0.23 + 0.137*CL	0.22 + 0.137*CL
TN to PAD	t_{PLH}	5.96	1.00 + 0.099*CL	1.00 + 0.099*CL	1.00 + 0.099*CL
	t_{PHL}	4.45	1.26 + 0.064*CL	1.25 + 0.064*CL	1.26 + 0.064*CL
	t_R	11.58	0.28 + 0.226*CL	0.27 + 0.226*CL	0.27 + 0.226*CL
	t_F	7.10	0.27 + 0.137*CL	0.23 + 0.137*CL	0.22 + 0.137*CL
	t_{PLZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL
	t_{PHZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL
EN to PAD	t_{PLH}	6.15	1.18 + 0.099*CL	1.19 + 0.099*CL	1.15 + 0.100*CL
	t_{PHL}	4.64	1.45 + 0.064*CL	1.45 + 0.064*CL	1.45 + 0.064*CL
	t_R	11.58	0.28 + 0.226*CL	0.27 + 0.226*CL	0.27 + 0.226*CL
	t_F	7.10	0.27 + 0.137*CL	0.23 + 0.137*CL	0.23 + 0.137*CL
	t_{PLZ}	0.91	0.85 + 0.001*CL	0.94 + 0.000*CL	0.94 + 0.000*CL
	t_{PHZ}	0.81	0.81 + 0.000*CL	0.81 + 0.000*CL	0.81 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT6SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.51	1.23 + 0.066*CL	1.23 + 0.066*CL	1.23 + 0.066*CL
	t_{PHL}	3.65	1.53 + 0.042*CL	1.55 + 0.042*CL	1.55 + 0.042*CL
	t_R	7.71	0.27 + 0.149*CL	0.24 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.42 + 0.089*CL	0.38 + 0.089*CL
TN to PAD	t_{PLH}	4.47	1.19 + 0.066*CL	1.20 + 0.066*CL	1.19 + 0.066*CL
	t_{PHL}	3.69	1.58 + 0.042*CL	1.59 + 0.042*CL	1.59 + 0.042*CL
	t_R	7.71	0.26 + 0.149*CL	0.25 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.42 + 0.089*CL	0.37 + 0.089*CL
	t_{PLZ}	0.95	0.95 + 0.000*CL	0.95 + 0.000*CL	0.95 + 0.000*CL
	t_{PHZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PLH}	4.66	1.38 + 0.066*CL	1.38 + 0.066*CL	1.38 + 0.066*CL
	t_{PHL}	3.89	1.77 + 0.042*CL	1.78 + 0.042*CL	1.79 + 0.042*CL
	t_R	7.71	0.26 + 0.149*CL	0.25 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.41 + 0.089*CL	0.38 + 0.089*CL
	t_{PLZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL
	t_{PHZ}	0.77	0.77 + 0.000*CL	0.77 + 0.000*CL	0.77 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.85	1.40 + 0.049*CL	1.40 + 0.049*CL	1.40 + 0.049*CL
	t_{PHL}	3.44	1.80 + 0.033*CL	1.85 + 0.032*CL	1.87 + 0.032*CL
	t_R	5.85	0.33 + 0.110*CL	0.30 + 0.111*CL	0.28 + 0.111*CL
	t_F	3.91	0.68 + 0.065*CL	0.63 + 0.065*CL	0.61 + 0.066*CL
TN to PAD	t_{PLH}	3.81	1.36 + 0.049*CL	1.22 + 0.051*CL	1.39 + 0.049*CL
	t_{PHL}	3.48	1.84 + 0.033*CL	1.89 + 0.032*CL	1.91 + 0.032*CL
	t_R	5.85	0.33 + 0.110*CL	0.29 + 0.111*CL	0.28 + 0.111*CL
	t_F	3.91	0.68 + 0.065*CL	0.63 + 0.065*CL	0.62 + 0.065*CL
	t_{PLZ}	0.95	0.95 + 0.000*CL	0.93 + 0.000*CL	0.95 + 0.000*CL
	t_{PHZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PLH}	4.00	1.55 + 0.049*CL	1.55 + 0.049*CL	1.55 + 0.049*CL
	t_{PHL}	3.67	2.04 + 0.033*CL	2.08 + 0.032*CL	2.10 + 0.032*CL
	t_R	5.85	0.33 + 0.110*CL	0.29 + 0.111*CL	0.28 + 0.111*CL
	t_F	3.91	0.69 + 0.064*CL	0.61 + 0.065*CL	0.62 + 0.065*CL
	t_{PLZ}	0.88	0.93 + -0.001*CL	0.85 + 0.000*CL	0.85 + 0.000*CL
	t_{PHZ}	0.77	0.77 + 0.000*CL	0.77 + 0.000*CL	0.77 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT10SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.32	1.38 + 0.039*CL	1.39 + 0.039*CL	1.39 + 0.039*CL
	t_{PHL}	3.10	1.74 + 0.027*CL	1.82 + 0.026*CL	1.86 + 0.026*CL
	t_R	4.70	0.39 + 0.086*CL	0.35 + 0.087*CL	0.34 + 0.087*CL
	t_F	3.34	0.85 + 0.050*CL	0.83 + 0.050*CL	0.80 + 0.050*CL
TN to PAD	t_{PLH}	3.28	1.35 + 0.039*CL	1.35 + 0.039*CL	1.35 + 0.039*CL
	t_{PHL}	3.13	1.77 + 0.027*CL	1.86 + 0.026*CL	1.89 + 0.026*CL
	t_R	4.71	0.40 + 0.086*CL	0.35 + 0.087*CL	0.32 + 0.087*CL
	t_F	3.36	0.88 + 0.049*CL	0.84 + 0.050*CL	0.79 + 0.051*CL
	t_{PLZ}	1.09	1.09 + 0.000*CL	1.08 + 0.000*CL	1.08 + 0.000*CL
	t_{PHZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL
EN to PAD	t_{PLH}	3.47	1.53 + 0.039*CL	1.54 + 0.039*CL	1.54 + 0.039*CL
	t_{PHL}	3.33	1.97 + 0.027*CL	2.05 + 0.026*CL	2.08 + 0.026*CL
	t_R	4.70	0.39 + 0.086*CL	0.35 + 0.087*CL	0.32 + 0.087*CL
	t_F	3.36	0.88 + 0.049*CL	0.84 + 0.050*CL	0.80 + 0.051*CL
	t_{PLZ}	0.99	0.99 + 0.000*CL	0.99 + 0.000*CL	0.99 + 0.000*CL
	t_{PHZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.17	1.54 + 0.033*CL	1.55 + 0.032*CL	1.56 + 0.032*CL
	t_{PHL}	3.14	1.91 + 0.025*CL	2.02 + 0.023*CL	2.07 + 0.022*CL
	t_R	4.06	0.51 + 0.071*CL	0.45 + 0.072*CL	0.44 + 0.072*CL
	t_F	3.10	1.03 + 0.041*CL	1.00 + 0.042*CL	1.01 + 0.042*CL
TN to PAD	t_{PLH}	3.14	1.51 + 0.033*CL	1.64 + 0.031*CL	1.43 + 0.033*CL
	t_{PHL}	3.17	1.93 + 0.025*CL	2.04 + 0.023*CL	2.10 + 0.023*CL
	t_R	4.06	0.51 + 0.071*CL	0.46 + 0.072*CL	0.43 + 0.072*CL
	t_F	3.12	1.08 + 0.041*CL	1.06 + 0.041*CL	1.02 + 0.042*CL
	t_{PLZ}	1.09	1.09 + 0.000*CL	1.07 + 0.000*CL	1.07 + 0.000*CL
	t_{PHZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL
EN to PAD	t_{PLH}	3.32	1.69 + 0.033*CL	1.70 + 0.032*CL	1.70 + 0.032*CL
	t_{PHL}	3.36	2.12 + 0.025*CL	2.24 + 0.023*CL	2.29 + 0.023*CL
	t_R	4.06	0.52 + 0.071*CL	0.46 + 0.072*CL	0.43 + 0.072*CL
	t_F	3.12	1.08 + 0.041*CL	1.06 + 0.041*CL	1.03 + 0.041*CL
	t_{PLZ}	0.99	0.98 + 0.000*CL	0.99 + 0.000*CL	0.99 + 0.000*CL
	t_{PHZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 POT16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.10	1.80 + 0.026*CL	1.86 + 0.025*CL	1.87 + 0.025*CL
	t_{PHL}	3.31	2.19 + 0.022*CL	2.33 + 0.020*CL	2.41 + 0.020*CL
	t_R	3.37	0.73 + 0.053*CL	0.70 + 0.053*CL	0.66 + 0.054*CL
	t_F	2.88	1.25 + 0.033*CL	1.32 + 0.032*CL	1.30 + 0.032*CL
TN to PAD	t_{PLH}	3.05	1.72 + 0.026*CL	1.82 + 0.025*CL	1.84 + 0.025*CL
	t_{PHL}	3.32	2.18 + 0.023*CL	2.34 + 0.021*CL	2.43 + 0.020*CL
	t_R	3.38	0.76 + 0.052*CL	0.70 + 0.053*CL	0.67 + 0.054*CL
	t_F	2.95	1.38 + 0.031*CL	1.41 + 0.031*CL	1.37 + 0.031*CL
	t_{PLZ}	1.08	1.07 + 0.000*CL	1.08 + 0.000*CL	1.08 + 0.000*CL
	t_{PHZ}	0.99	0.99 + 0.000*CL	0.99 + 0.000*CL	0.99 + 0.000*CL
EN to PAD	t_{PLH}	3.23	1.94 + 0.026*CL	2.00 + 0.025*CL	2.01 + 0.025*CL
	t_{PHL}	3.52	2.37 + 0.023*CL	2.54 + 0.021*CL	2.62 + 0.020*CL
	t_R	3.39	0.77 + 0.052*CL	0.69 + 0.053*CL	0.68 + 0.054*CL
	t_F	2.94	1.37 + 0.031*CL	1.41 + 0.031*CL	1.37 + 0.031*CL
	t_{PLZ}	0.99	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL
	t_{PHZ}	0.89	0.88 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	15.51	0.90 + 0.292*CL	0.90 + 0.292*CL	0.89 + 0.292*CL
	t_{PHL}	12.56	0.91 + 0.233*CL	0.92 + 0.233*CL	0.91 + 0.233*CL
	t_R	33.59	0.59 + 0.660*CL	0.60 + 0.660*CL	0.59 + 0.660*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL
TN to PAD	t_{PLH}	10.17	1.03 + 0.183*CL	1.63 + 0.175*CL	2.79 + 0.161*CL
	t_{PHL}	17.31	1.10 + 0.324*CL	1.11 + 0.324*CL	1.10 + 0.324*CL
	t_R	16.39	0.24 + 0.323*CL	0.24 + 0.323*CL	0.24 + 0.323*CL
	t_F	20.78	0.31 + 0.409*CL	0.31 + 0.409*CL	0.31 + 0.409*CL
	t_{PLZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL
	t_{PHZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
EN to PAD	t_{PLH}	10.34	1.19 + 0.183*CL	1.80 + 0.175*CL	2.98 + 0.161*CL
	t_{PHL}	17.47	1.27 + 0.324*CL	1.27 + 0.324*CL	1.27 + 0.324*CL
	t_R	16.39	0.24 + 0.323*CL	0.24 + 0.323*CL	0.24 + 0.323*CL
	t_F	20.78	0.31 + 0.409*CL	0.31 + 0.409*CL	0.31 + 0.409*CL
	t_{PLZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	8.13	0.83 + 0.146*CL	0.82 + 0.146*CL	0.83 + 0.146*CL
	t_{PHL}	6.65	0.83 + 0.116*CL	0.84 + 0.116*CL	0.84 + 0.116*CL
	t_R	16.81	0.31 + 0.330*CL	0.30 + 0.330*CL	0.31 + 0.330*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.243*CL	0.21 + 0.243*CL
TN to PAD	t_{PLH}	5.51	0.88 + 0.093*CL	0.88 + 0.093*CL	0.89 + 0.093*CL
	t_{PHL}	9.09	0.99 + 0.162*CL	0.99 + 0.162*CL	0.99 + 0.162*CL
	t_R	8.20	0.12 + 0.161*CL	0.13 + 0.161*CL	0.12 + 0.161*CL
	t_F	10.40	0.17 + 0.205*CL	0.17 + 0.205*CL	0.17 + 0.205*CL
	t_{PLZ}	1.06	1.06 + 0.000*CL	1.06 + 0.000*CL	1.05 + 0.000*CL
	t_{PHZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL
EN to PAD	t_{PLH}	5.68	1.05 + 0.093*CL	1.05 + 0.093*CL	1.05 + 0.093*CL
	t_{PHL}	9.25	1.15 + 0.162*CL	1.15 + 0.162*CL	1.15 + 0.162*CL
	t_R	8.20	0.12 + 0.161*CL	0.13 + 0.161*CL	0.12 + 0.161*CL
	t_F	10.40	0.17 + 0.205*CL	0.17 + 0.205*CL	0.17 + 0.205*CL
	t_{PLZ}	0.99	0.99 + 0.000*CL	0.99 + 0.000*CL	0.99 + 0.000*CL
	t_{PHZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.52	0.83 + 0.094*CL	0.83 + 0.094*CL	0.83 + 0.094*CL
	t_{PHL}	4.54	0.83 + 0.074*CL	0.82 + 0.074*CL	0.83 + 0.074*CL
	t_R	10.81	0.21 + 0.212*CL	0.21 + 0.212*CL	0.21 + 0.212*CL
	t_F	7.88	0.15 + 0.155*CL	0.14 + 0.155*CL	0.15 + 0.155*CL
TN to PAD	t_{PLH}	3.87	0.90 + 0.059*CL	0.90 + 0.059*CL	0.89 + 0.059*CL
	t_{PHL}	6.14	0.97 + 0.103*CL	0.97 + 0.103*CL	0.98 + 0.103*CL
	t_R	5.27	0.09 + 0.104*CL	0.09 + 0.104*CL	0.09 + 0.104*CL
	t_F	6.64	0.12 + 0.130*CL	0.12 + 0.130*CL	0.11 + 0.131*CL
	t_{PLZ}	1.13	1.12 + 0.000*CL	1.12 + 0.000*CL	1.07 + 0.001*CL
	t_{PHZ}	0.96	0.96 + 0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL
EN to PAD	t_{PLH}	4.03	1.06 + 0.059*CL	1.03 + 0.060*CL	1.08 + 0.059*CL
	t_{PHL}	6.30	1.13 + 0.103*CL	1.14 + 0.103*CL	1.13 + 0.103*CL
	t_R	5.27	0.09 + 0.104*CL	0.09 + 0.104*CL	0.08 + 0.104*CL
	t_F	6.64	0.12 + 0.130*CL	0.13 + 0.130*CL	0.11 + 0.131*CL
	t_{PLZ}	1.06	1.06 + 0.000*CL	1.06 + 0.000*CL	1.06 + 0.000*CL
	t_{PHZ}	0.88	0.88 + 0.000*CL	0.88 + 0.000*CL	0.88 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.23	0.89 + 0.047*CL	0.89 + 0.047*CL	0.89 + 0.047*CL
	t_{PHL}	2.74	0.88 + 0.037*CL	0.88 + 0.037*CL	0.89 + 0.037*CL
	t_R	5.43	0.13 + 0.106*CL	0.13 + 0.106*CL	0.13 + 0.106*CL
	t_F	3.96	0.10 + 0.077*CL	0.10 + 0.077*CL	0.10 + 0.077*CL
TN to PAD	t_{PLH}	2.45	0.97 + 0.030*CL	0.96 + 0.030*CL	0.97 + 0.030*CL
	t_{PHL}	3.61	1.03 + 0.052*CL	1.02 + 0.052*CL	1.07 + 0.051*CL
	t_R	2.64	0.06 + 0.052*CL	0.05 + 0.052*CL	0.05 + 0.052*CL
	t_F	3.34	0.08 + 0.065*CL	0.09 + 0.065*CL	0.08 + 0.065*CL
	t_{PLZ}	1.30	1.30 + 0.000*CL	1.29 + 0.000*CL	1.30 + 0.000*CL
	t_{PHZ}	1.04	1.04 + 0.000*CL	1.04 + 0.000*CL	1.04 + 0.000*CL
EN to PAD	t_{PLH}	2.62	1.13 + 0.030*CL	1.13 + 0.030*CL	1.13 + 0.030*CL
	t_{PHL}	3.77	1.18 + 0.052*CL	1.19 + 0.052*CL	1.18 + 0.052*CL
	t_R	2.64	0.06 + 0.052*CL	0.05 + 0.052*CL	0.05 + 0.052*CL
	t_F	3.34	0.08 + 0.065*CL	0.08 + 0.065*CL	0.08 + 0.065*CL
	t_{PLZ}	1.25	1.28 + -0.001*CL	1.23 + 0.000*CL	1.23 + 0.000*CL
	t_{PHZ}	0.96	0.96 + 0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.68	0.95 + 0.034*CL	0.95 + 0.035*CL	0.95 + 0.035*CL
	t_{PHL}	2.30	0.94 + 0.027*CL	0.95 + 0.027*CL	0.94 + 0.027*CL
	t_R	4.02	0.12 + 0.078*CL	0.11 + 0.078*CL	0.11 + 0.078*CL
	t_F	2.93	0.11 + 0.056*CL	0.11 + 0.056*CL	0.09 + 0.057*CL
TN to PAD	t_{PLH}	2.12	1.03 + 0.022*CL	1.03 + 0.022*CL	1.03 + 0.022*CL
	t_{PHL}	2.97	1.07 + 0.038*CL	1.07 + 0.038*CL	1.04 + 0.038*CL
	t_R	1.96	0.06 + 0.038*CL	0.05 + 0.038*CL	0.05 + 0.038*CL
	t_F	2.47	0.08 + 0.048*CL	0.08 + 0.048*CL	0.08 + 0.048*CL
	t_{PLZ}	1.43	1.42 + 0.000*CL	1.33 + 0.001*CL	1.50 + -0.001*CL
	t_{PHZ}	1.10	1.10 + 0.000*CL	1.10 + 0.000*CL	1.10 + 0.000*CL
EN to PAD	t_{PLH}	2.29	1.19 + 0.022*CL	1.19 + 0.022*CL	1.19 + 0.022*CL
	t_{PHL}	3.14	1.24 + 0.038*CL	1.24 + 0.038*CL	1.24 + 0.038*CL
	t_R	1.96	0.06 + 0.038*CL	0.06 + 0.038*CL	0.05 + 0.038*CL
	t_F	2.47	0.08 + 0.048*CL	0.09 + 0.048*CL	0.07 + 0.048*CL
	t_{PLZ}	1.37	1.35 + 0.000*CL	1.36 + 0.000*CL	1.36 + 0.000*CL
	t_{PHZ}	1.02	1.02 + 0.000*CL	1.02 + 0.000*CL	1.02 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.30	1.05 + 0.025*CL	1.05 + 0.025*CL	1.04 + 0.025*CL
	t_{PHL}	2.02	1.03 + 0.020*CL	1.04 + 0.020*CL	1.02 + 0.020*CL
	t_R	2.97	0.14 + 0.057*CL	0.12 + 0.057*CL	0.12 + 0.057*CL
	t_F	2.19	0.15 + 0.041*CL	0.14 + 0.041*CL	0.14 + 0.041*CL
TN to PAD	t_{PLH}	1.91	1.11 + 0.016*CL	1.11 + 0.016*CL	1.11 + 0.016*CL
	t_{PHL}	2.54	1.16 + 0.028*CL	1.15 + 0.028*CL	1.17 + 0.028*CL
	t_R	1.47	0.10 + 0.027*CL	0.09 + 0.027*CL	0.08 + 0.028*CL
	t_F	1.82	0.07 + 0.035*CL	0.08 + 0.035*CL	0.07 + 0.035*CL
	t_{PLZ}	1.60	1.58 + 0.000*CL	1.68 + -0.001*CL	1.60 + 0.000*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL
EN to PAD	t_{PLH}	2.08	1.27 + 0.016*CL	1.28 + 0.016*CL	1.27 + 0.016*CL
	t_{PHL}	2.71	1.33 + 0.028*CL	1.27 + 0.028*CL	1.32 + 0.028*CL
	t_R	1.47	0.10 + 0.027*CL	0.09 + 0.028*CL	0.08 + 0.028*CL
	t_F	1.82	0.07 + 0.035*CL	0.07 + 0.035*CL	0.08 + 0.035*CL
	t_{PLZ}	1.53	1.53 + 0.000*CL	1.53 + 0.000*CL	1.53 + 0.000*CL
	t_{PHZ}	1.10	1.10 + 0.000*CL	1.10 + 0.000*CL	1.10 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT20 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.93	0.94 + 0.020*CL	0.94 + 0.020*CL	0.94 + 0.020*CL
	t_{PHL}	1.79	1.01 + 0.016*CL	1.01 + 0.016*CL	1.00 + 0.016*CL
	t_R	2.34	0.10 + 0.045*CL	0.10 + 0.045*CL	0.08 + 0.045*CL
	t_F	1.75	0.16 + 0.032*CL	0.14 + 0.032*CL	0.12 + 0.032*CL
TN to PAD	t_{PLH}	1.65	1.02 + 0.013*CL	1.02 + 0.013*CL	1.02 + 0.013*CL
	t_{PHL}	2.23	1.14 + 0.022*CL	1.13 + 0.022*CL	1.12 + 0.022*CL
	t_R	1.15	0.07 + 0.022*CL	0.05 + 0.022*CL	0.05 + 0.022*CL
	t_F	1.44	0.06 + 0.028*CL	0.06 + 0.028*CL	0.06 + 0.028*CL
	t_{PLZ}	1.40	1.39 + 0.000*CL	1.47 + -0.001*CL	1.40 + 0.000*CL
	t_{PHZ}	1.15	1.15 + 0.000*CL	1.14 + 0.000*CL	1.15 + 0.000*CL
EN to PAD	t_{PLH}	1.82	1.18 + 0.013*CL	1.22 + 0.012*CL	1.19 + 0.013*CL
	t_{PHL}	2.39	1.29 + 0.022*CL	1.29 + 0.022*CL	1.29 + 0.022*CL
	t_R	1.15	0.07 + 0.022*CL	0.06 + 0.022*CL	0.05 + 0.022*CL
	t_F	1.44	0.07 + 0.028*CL	0.05 + 0.028*CL	0.06 + 0.028*CL
	t_{PLZ}	1.33	1.29 + 0.001*CL	1.51 + -0.002*CL	1.33 + 0.000*CL
	t_{PHZ}	1.07	1.07 + 0.000*CL	1.07 + 0.000*CL	1.07 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT24 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.86	0.99 + 0.017*CL	0.98 + 0.018*CL	0.99 + 0.018*CL
	t_{PHL}	1.73	1.04 + 0.014*CL	1.04 + 0.014*CL	1.04 + 0.014*CL
	t_R	2.07	0.10 + 0.039*CL	0.12 + 0.039*CL	0.09 + 0.040*CL
	t_F	1.57	0.17 + 0.028*CL	0.16 + 0.028*CL	0.15 + 0.028*CL
TN to PAD	t_{PLH}	1.62	1.07 + 0.011*CL	1.07 + 0.011*CL	1.07 + 0.011*CL
	t_{PHL}	2.13	1.16 + 0.019*CL	1.17 + 0.019*CL	1.17 + 0.019*CL
	t_R	1.03	0.09 + 0.019*CL	0.06 + 0.019*CL	0.07 + 0.019*CL
	t_F	1.28	0.07 + 0.024*CL	0.09 + 0.024*CL	0.05 + 0.024*CL
	t_{PLZ}	1.46	1.45 + 0.000*CL	1.40 + 0.001*CL	1.46 + 0.000*CL
	t_{PHZ}	1.14	1.14 + 0.000*CL	1.14 + 0.000*CL	1.14 + 0.000*CL
EN to PAD	t_{PLH}	1.79	1.23 + 0.011*CL	1.23 + 0.011*CL	1.23 + 0.011*CL
	t_{PHL}	2.29	1.33 + 0.019*CL	1.31 + 0.020*CL	1.33 + 0.019*CL
	t_R	1.03	0.09 + 0.019*CL	0.07 + 0.019*CL	0.07 + 0.019*CL
	t_F	1.28	0.07 + 0.024*CL	0.06 + 0.024*CL	0.05 + 0.024*CL
	t_{PLZ}	1.39	1.39 + 0.000*CL	1.38 + 0.000*CL	1.39 + 0.000*CL
	t_{PHZ}	1.07	1.07 + 0.000*CL	1.07 + 0.000*CL	1.06 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT12SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.44	1.66 + 0.036*CL	1.69 + 0.035*CL	1.69 + 0.035*CL
	t_{PHL}	3.94	2.34 + 0.032*CL	2.45 + 0.031*CL	2.51 + 0.030*CL
	t_R	4.34	0.50 + 0.077*CL	0.44 + 0.078*CL	0.43 + 0.078*CL
	t_F	3.74	0.97 + 0.055*CL	1.00 + 0.055*CL	0.99 + 0.055*CL
TN to PAD	t_{PLH}	2.80	1.64 + 0.023*CL	1.68 + 0.023*CL	1.70 + 0.022*CL
	t_{PHL}	4.69	2.58 + 0.042*CL	2.69 + 0.041*CL	2.74 + 0.040*CL
	t_R	2.26	0.43 + 0.037*CL	0.41 + 0.037*CL	0.38 + 0.037*CL
	t_F	2.79	0.45 + 0.047*CL	0.43 + 0.047*CL	0.39 + 0.048*CL
	t_{PLZ}	1.75	1.74 + 0.000*CL	1.71 + 0.001*CL	1.81 + -0.001*CL
	t_{PHZ}	1.25	1.25 + 0.000*CL	1.25 + 0.000*CL	1.25 + 0.000*CL
EN to PAD	t_{PLH}	2.97	1.81 + 0.023*CL	1.85 + 0.023*CL	1.86 + 0.022*CL
	t_{PHL}	4.86	2.75 + 0.042*CL	2.84 + 0.041*CL	2.90 + 0.040*CL
	t_R	2.26	0.43 + 0.037*CL	0.40 + 0.037*CL	0.38 + 0.037*CL
	t_F	2.79	0.45 + 0.047*CL	0.40 + 0.047*CL	0.41 + 0.047*CL
	t_{PLZ}	1.68	1.68 + 0.000*CL	1.68 + 0.000*CL	1.68 + 0.000*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT16SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.24	1.89 + 0.027*CL	1.94 + 0.026*CL	1.97 + 0.026*CL
	t_{PHL}	3.64	2.39 + 0.025*CL	2.50 + 0.024*CL	2.56 + 0.023*CL
	t_R	3.43	0.71 + 0.055*CL	0.68 + 0.055*CL	0.67 + 0.055*CL
	t_F	3.00	0.96 + 0.041*CL	1.01 + 0.040*CL	1.02 + 0.040*CL
TN to PAD	t_{PLH}	2.73	1.81 + 0.019*CL	1.88 + 0.017*CL	1.91 + 0.017*CL
	t_{PHL}	4.24	2.60 + 0.033*CL	2.72 + 0.031*CL	2.78 + 0.030*CL
	t_R	1.90	0.61 + 0.026*CL	0.60 + 0.026*CL	0.59 + 0.026*CL
	t_F	2.17	0.50 + 0.033*CL	0.47 + 0.034*CL	0.47 + 0.034*CL
	t_{PLZ}	1.72	1.72 + 0.000*CL	1.72 + 0.000*CL	1.72 + 0.000*CL
	t_{PHZ}	1.25	1.25 + 0.000*CL	1.25 + 0.000*CL	1.25 + 0.000*CL
EN to PAD	t_{PLH}	2.90	1.97 + 0.018*CL	2.04 + 0.018*CL	2.08 + 0.017*CL
	t_{PHL}	4.40	2.77 + 0.033*CL	2.89 + 0.031*CL	2.94 + 0.031*CL
	t_R	1.90	0.61 + 0.026*CL	0.61 + 0.026*CL	0.59 + 0.026*CL
	t_F	2.17	0.49 + 0.033*CL	0.48 + 0.034*CL	0.47 + 0.034*CL
	t_{PLZ}	1.65	1.65 + 0.000*CL	1.65 + 0.000*CL	1.65 + 0.000*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT20SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.63	1.57 + 0.021*CL	1.62 + 0.021*CL	1.63 + 0.020*CL
	t_{PHL}	2.66	1.80 + 0.017*CL	1.84 + 0.017*CL	1.85 + 0.017*CL
	t_R	2.72	0.58 + 0.043*CL	0.55 + 0.043*CL	0.55 + 0.043*CL
	t_F	2.24	0.72 + 0.030*CL	0.70 + 0.031*CL	0.69 + 0.031*CL
TN to PAD	t_{PLH}	2.25	1.52 + 0.015*CL	1.58 + 0.014*CL	1.61 + 0.014*CL
	t_{PHL}	3.05	1.82 + 0.024*CL	1.91 + 0.023*CL	1.93 + 0.023*CL
	t_R	1.53	0.53 + 0.020*CL	0.50 + 0.020*CL	0.51 + 0.020*CL
	t_F	1.63	0.32 + 0.026*CL	0.29 + 0.027*CL	0.27 + 0.027*CL
	t_{PLZ}	1.08	1.06 + 0.000*CL	1.16 + -0.001*CL	1.08 + 0.000*CL
	t_{PHZ}	1.12	1.12 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL
EN to PAD	t_{PLH}	2.42	1.69 + 0.015*CL	1.75 + 0.014*CL	1.78 + 0.013*CL
	t_{PHL}	3.21	1.98 + 0.025*CL	2.07 + 0.023*CL	2.09 + 0.023*CL
	t_R	1.53	0.53 + 0.020*CL	0.50 + 0.020*CL	0.50 + 0.020*CL
	t_F	1.63	0.30 + 0.026*CL	0.32 + 0.026*CL	0.27 + 0.027*CL
	t_{PLZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL
	t_{PHZ}	1.05	1.05 + 0.000*CL	1.05 + 0.000*CL	1.05 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT24SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.62	1.65 + 0.019*CL	1.72 + 0.019*CL	1.73 + 0.018*CL
	t_{PHL}	2.73	1.94 + 0.016*CL	1.97 + 0.015*CL	1.99 + 0.015*CL
	t_R	2.54	0.66 + 0.038*CL	0.67 + 0.037*CL	0.63 + 0.038*CL
	t_F	2.15	0.81 + 0.027*CL	0.82 + 0.027*CL	0.79 + 0.027*CL
TN to PAD	t_{PLH}	2.27	1.58 + 0.014*CL	1.65 + 0.013*CL	1.68 + 0.012*CL
	t_{PHL}	3.04	1.90 + 0.023*CL	1.99 + 0.022*CL	2.04 + 0.021*CL
	t_R	1.47	0.59 + 0.018*CL	0.60 + 0.018*CL	0.57 + 0.018*CL
	t_F	1.52	0.37 + 0.023*CL	0.38 + 0.023*CL	0.34 + 0.023*CL
	t_{PLZ}	1.08	1.08 + 0.000*CL	1.08 + 0.000*CL	1.08 + 0.000*CL
	t_{PHZ}	1.12	1.12 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL
EN to PAD	t_{PLH}	2.43	1.74 + 0.014*CL	1.82 + 0.013*CL	1.84 + 0.012*CL
	t_{PHL}	3.20	2.07 + 0.023*CL	2.16 + 0.021*CL	2.19 + 0.021*CL
	t_R	1.48	0.60 + 0.018*CL	0.61 + 0.017*CL	0.57 + 0.018*CL
	t_F	1.52	0.37 + 0.023*CL	0.35 + 0.023*CL	0.35 + 0.023*CL
	t_{PLZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL
	t_{PHZ}	1.05	1.05 + 0.000*CL	1.05 + 0.000*CL	1.05 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT4SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.86	1.16 + 0.094*CL	1.17 + 0.094*CL	1.17 + 0.094*CL
	t_{PHL}	5.46	1.74 + 0.074*CL	1.75 + 0.074*CL	1.75 + 0.074*CL
	t_R	10.83	0.24 + 0.212*CL	0.23 + 0.212*CL	0.24 + 0.212*CL
	t_F	8.06	0.43 + 0.153*CL	0.38 + 0.153*CL	0.36 + 0.153*CL
TN to PAD	t_{PLH}	4.17	1.20 + 0.059*CL	1.20 + 0.059*CL	1.20 + 0.059*CL
	t_{PHL}	7.07	1.90 + 0.103*CL	1.90 + 0.103*CL	1.91 + 0.103*CL
	t_R	5.29	0.13 + 0.103*CL	0.11 + 0.103*CL	0.11 + 0.104*CL
	t_F	6.69	0.18 + 0.130*CL	0.16 + 0.130*CL	0.16 + 0.130*CL
	t_{PLZ}	1.77	1.77 + 0.000*CL	1.77 + 0.000*CL	1.77 + 0.000*CL
	t_{PHZ}	1.26	1.26 + 0.000*CL	1.26 + 0.000*CL	1.26 + 0.000*CL
EN to PAD	t_{PLH}	4.33	1.36 + 0.059*CL	1.36 + 0.060*CL	1.37 + 0.059*CL
	t_{PHL}	7.24	2.07 + 0.103*CL	2.04 + 0.104*CL	2.07 + 0.103*CL
	t_R	5.29	0.13 + 0.103*CL	0.11 + 0.103*CL	0.11 + 0.104*CL
	t_F	6.69	0.17 + 0.130*CL	0.16 + 0.130*CL	0.16 + 0.130*CL
	t_{PLZ}	1.71	1.70 + 0.000*CL	1.71 + 0.000*CL	1.71 + 0.000*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT8SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.82	1.47 + 0.047*CL	1.48 + 0.047*CL	1.48 + 0.047*CL
	t_{PHL}	4.07	2.11 + 0.039*CL	2.18 + 0.038*CL	2.21 + 0.038*CL
	t_R	5.58	0.35 + 0.105*CL	0.31 + 0.105*CL	0.29 + 0.105*CL
	t_F	4.47	0.75 + 0.074*CL	0.72 + 0.075*CL	0.70 + 0.075*CL
TN to PAD	t_{PLH}	2.99	1.49 + 0.030*CL	1.50 + 0.030*CL	1.50 + 0.030*CL
	t_{PHL}	4.98	2.31 + 0.053*CL	2.37 + 0.053*CL	2.38 + 0.052*CL
	t_R	2.80	0.29 + 0.050*CL	0.26 + 0.051*CL	0.23 + 0.051*CL
	t_F	3.50	0.31 + 0.064*CL	0.28 + 0.064*CL	0.25 + 0.065*CL
	t_{PLZ}	1.76	1.74 + 0.000*CL	1.66 + 0.001*CL	1.76 + 0.000*CL
	t_{PHZ}	1.25	1.25 + 0.000*CL	1.25 + 0.000*CL	1.25 + 0.000*CL
EN to PAD	t_{PLH}	3.15	1.65 + 0.030*CL	1.67 + 0.030*CL	1.67 + 0.030*CL
	t_{PHL}	5.14	2.48 + 0.053*CL	2.54 + 0.053*CL	2.56 + 0.052*CL
	t_R	2.80	0.29 + 0.050*CL	0.26 + 0.051*CL	0.23 + 0.051*CL
	t_F	3.50	0.31 + 0.064*CL	0.28 + 0.064*CL	0.25 + 0.065*CL
	t_{PLZ}	1.71	1.70 + 0.000*CL	1.69 + 0.000*CL	1.69 + 0.000*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT12SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.25	1.51 + 0.035*CL	1.52 + 0.035*CL	1.53 + 0.035*CL
	t_{PHL}	3.57	2.04 + 0.031*CL	2.13 + 0.029*CL	2.18 + 0.029*CL
	t_R	4.22	0.41 + 0.076*CL	0.37 + 0.077*CL	0.35 + 0.077*CL
	t_F	3.55	0.81 + 0.055*CL	0.83 + 0.055*CL	0.82 + 0.055*CL
TN to PAD	t_{PLH}	2.63	1.50 + 0.023*CL	1.53 + 0.022*CL	1.55 + 0.022*CL
	t_{PHL}	4.30	2.26 + 0.041*CL	2.35 + 0.040*CL	2.39 + 0.039*CL
	t_R	2.18	0.37 + 0.036*CL	0.32 + 0.037*CL	0.32 + 0.037*CL
	t_F	2.69	0.39 + 0.046*CL	0.37 + 0.046*CL	0.33 + 0.047*CL
	t_{PLZ}	1.99	1.99 + 0.000*CL	1.93 + 0.001*CL	2.05 + -0.001*CL
	t_{PHZ}	1.42	1.42 + 0.000*CL	1.41 + 0.000*CL	1.42 + 0.000*CL
EN to PAD	t_{PLH}	2.80	1.67 + 0.022*CL	1.67 + 0.022*CL	1.71 + 0.022*CL
	t_{PHL}	4.47	2.42 + 0.041*CL	2.51 + 0.040*CL	2.55 + 0.039*CL
	t_R	2.18	0.37 + 0.036*CL	0.33 + 0.037*CL	0.32 + 0.037*CL
	t_F	2.69	0.38 + 0.046*CL	0.36 + 0.047*CL	0.34 + 0.047*CL
	t_{PLZ}	1.92	1.92 + 0.000*CL	1.92 + 0.000*CL	1.84 + 0.001*CL
	t_{PHZ}	1.35	1.35 + 0.000*CL	1.35 + 0.000*CL	1.35 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT16SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.93	1.61 + 0.026*CL	1.65 + 0.026*CL	1.67 + 0.026*CL
	t_{PHL}	3.14	1.96 + 0.024*CL	2.05 + 0.023*CL	2.09 + 0.022*CL
	t_R	3.29	0.54 + 0.055*CL	0.50 + 0.056*CL	0.50 + 0.055*CL
	t_F	2.77	0.74 + 0.041*CL	0.77 + 0.040*CL	0.79 + 0.040*CL
TN to PAD	t_{PLH}	2.45	1.56 + 0.018*CL	1.59 + 0.017*CL	1.67 + 0.016*CL
	t_{PHL}	3.72	2.16 + 0.031*CL	2.25 + 0.030*CL	2.30 + 0.029*CL
	t_R	1.77	0.45 + 0.026*CL	0.46 + 0.026*CL	0.46 + 0.026*CL
	t_F	2.07	0.38 + 0.034*CL	0.38 + 0.034*CL	0.36 + 0.034*CL
	t_{PLZ}	2.19	2.23 + -0.001*CL	2.17 + 0.000*CL	2.11 + 0.001*CL
	t_{PHZ}	1.56	1.56 + 0.000*CL	1.56 + 0.000*CL	1.56 + 0.000*CL
EN to PAD	t_{PLH}	2.61	1.73 + 0.018*CL	1.78 + 0.017*CL	1.80 + 0.017*CL
	t_{PHL}	3.89	2.32 + 0.031*CL	2.41 + 0.030*CL	2.47 + 0.029*CL
	t_R	1.77	0.46 + 0.026*CL	0.47 + 0.026*CL	0.45 + 0.026*CL
	t_F	2.07	0.38 + 0.034*CL	0.39 + 0.034*CL	0.36 + 0.034*CL
	t_{PLZ}	2.12	2.10 + 0.000*CL	2.11 + 0.000*CL	2.11 + 0.000*CL
	t_{PHZ}	1.49	1.49 + 0.000*CL	1.49 + 0.000*CL	1.49 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT20SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.30	1.29 + 0.020*CL	1.30 + 0.020*CL	1.31 + 0.020*CL
	t_{PHL}	2.30	1.41 + 0.018*CL	1.46 + 0.017*CL	1.49 + 0.017*CL
	t_R	2.53	0.36 + 0.043*CL	0.34 + 0.044*CL	0.31 + 0.044*CL
	t_F	2.11	0.54 + 0.031*CL	0.56 + 0.031*CL	0.56 + 0.031*CL
TN to PAD	t_{PLH}	1.98	1.30 + 0.013*CL	1.34 + 0.013*CL	1.34 + 0.013*CL
	t_{PHL}	2.76	1.57 + 0.024*CL	1.61 + 0.023*CL	1.64 + 0.023*CL
	t_R	1.36	0.35 + 0.020*CL	0.32 + 0.021*CL	0.30 + 0.021*CL
	t_F	1.58	0.26 + 0.026*CL	0.24 + 0.027*CL	0.22 + 0.027*CL
	t_{PLZ}	1.25	1.24 + 0.000*CL	1.18 + 0.001*CL	1.31 + -0.001*CL
	t_{PHZ}	1.05	1.05 + 0.000*CL	1.05 + 0.000*CL	1.05 + 0.000*CL
EN to PAD	t_{PLH}	2.14	1.47 + 0.013*CL	1.50 + 0.013*CL	1.51 + 0.013*CL
	t_{PHL}	2.92	1.74 + 0.024*CL	1.79 + 0.023*CL	1.83 + 0.023*CL
	t_R	1.35	0.33 + 0.020*CL	0.34 + 0.020*CL	0.29 + 0.021*CL
	t_F	1.59	0.28 + 0.026*CL	0.24 + 0.027*CL	0.22 + 0.027*CL
	t_{PLZ}	1.18	1.15 + 0.001*CL	1.19 + 0.000*CL	1.19 + 0.000*CL
	t_{PHZ}	0.97	0.97 + 0.000*CL	0.97 + 0.000*CL	0.97 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDM80 PHOT24SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

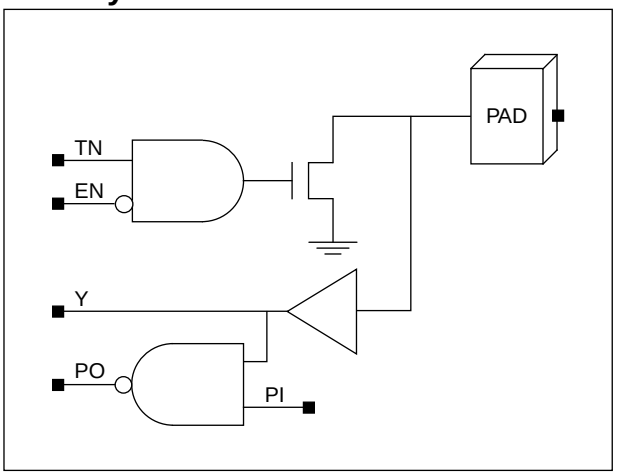
Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.28	1.36 + 0.018*CL	1.40 + 0.018*CL	1.41 + 0.018*CL
	t_{PHL}	2.32	1.49 + 0.017*CL	1.56 + 0.016*CL	1.59 + 0.015*CL
	t_R	2.33	0.44 + 0.038*CL	0.43 + 0.038*CL	0.41 + 0.038*CL
	t_F	2.01	0.62 + 0.028*CL	0.66 + 0.027*CL	0.65 + 0.027*CL
TN to PAD	t_{PLH}	1.98	1.35 + 0.013*CL	1.40 + 0.012*CL	1.42 + 0.012*CL
	t_{PHL}	2.75	1.65 + 0.022*CL	1.73 + 0.021*CL	1.76 + 0.021*CL
	t_R	1.30	0.42 + 0.018*CL	0.43 + 0.017*CL	0.39 + 0.018*CL
	t_F	1.47	0.32 + 0.023*CL	0.32 + 0.023*CL	0.31 + 0.023*CL
	t_{PLZ}	1.25	1.24 + 0.000*CL	1.24 + 0.000*CL	1.25 + 0.000*CL
	t_{PHZ}	1.05	1.05 + 0.000*CL	1.05 + 0.000*CL	1.05 + 0.000*CL
EN to PAD	t_{PLH}	2.14	1.52 + 0.013*CL	1.56 + 0.012*CL	1.58 + 0.012*CL
	t_{PHL}	2.92	1.80 + 0.022*CL	1.93 + 0.021*CL	1.94 + 0.020*CL
	t_R	1.29	0.40 + 0.018*CL	0.43 + 0.017*CL	0.41 + 0.018*CL
	t_F	1.47	0.33 + 0.023*CL	0.30 + 0.023*CL	0.31 + 0.023*CL
	t_{PLZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.17 + 0.000*CL
	t_{PHZ}	0.97	0.97 + 0.000*CL	0.97 + 0.000*CL	0.97 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

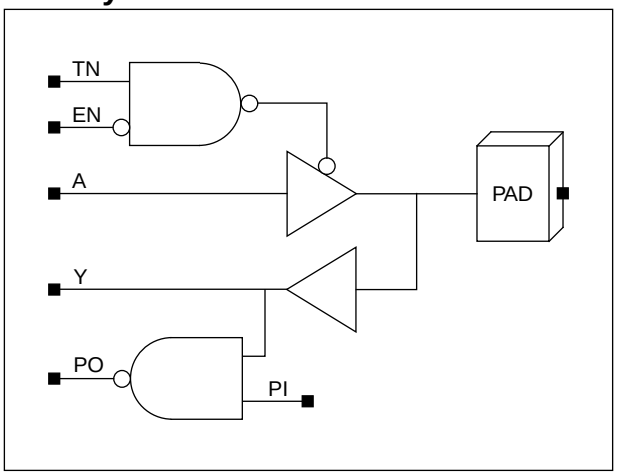
Cell List

Cell Name	Function Description
STD80	
PBaDyz	5V Open-Drain Bi-Directional Buffers
PBaUDyz	5V Open-Drain Bi-Directional Buffers with Pull-Up
PBaTyz	5V Tri-State Bi-Directional Buffers
PBaDTyz	5V Tri-State Bi-Directional Buffers with Pull-Down
PBaUTyz	5V Tri-State Bi-Directional Buffers with Pull-Up
PLBaDyz	3.3V Interface Open-Drain Bi-Directional Buffers
PLBaUDyz	3.3V Interface Open-Drain Bi-Directional Buffers with Pull-Up
PLBaTyz	3.3V Interface Tri-State Bi-Directional Buffers
PLBaDTyz	3.3V Interface Tri-State Bi-Directional Buffers with Pull-Down
PLBaUTyz	3.3V Interface Tri-State Bi-Directional Buffers with Pull-Up
STDM80	
PBaDyz	3.3V Open-Drain Bi-Directional Buffers
PBaUDyz	3.3V Open-Drain Bi-Directional Buffers with Pull-Up
PBaTyz	3.3V Tri-State Bi-Directional Buffers
PBaDTyz	3.3V Tri-State Bi-Directional Buffers with Pull-Down
PBaUTyz	3.3V Tri-State Bi-Directional Buffers with Pull-Up
PHBaDyz	5V Interface Open-Drain Bi-Directional Buffers
PHBaUDyz	5V Interface Open-Drain Bi-Directional Buffers with Pull-Up
PHBaTyz	5V Interface Tri-State Bi-Directional Buffers
PHBaDTyz	5V Interface Tri-State Bi-Directional Buffers with Pull-Down
PHBaUTyz	5V Interface Tri-State Bi-Directional Buffers with Pull-Up

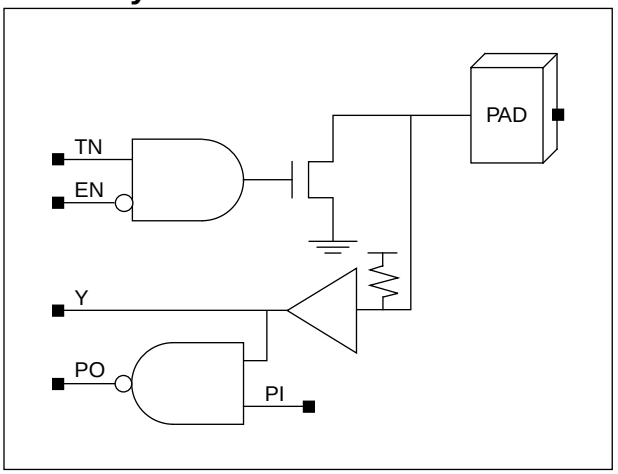
PvBaDyz



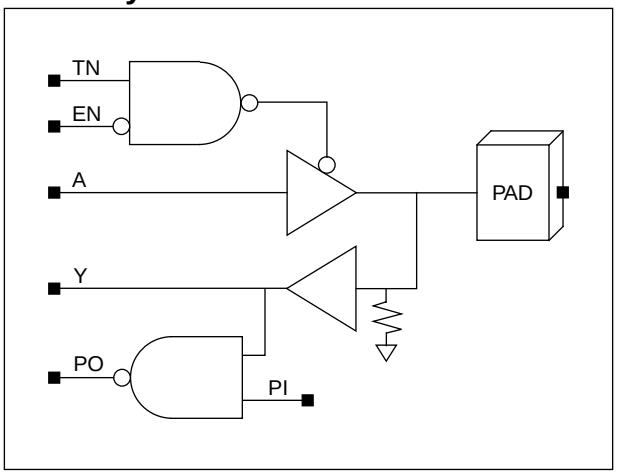
PvBaTyz



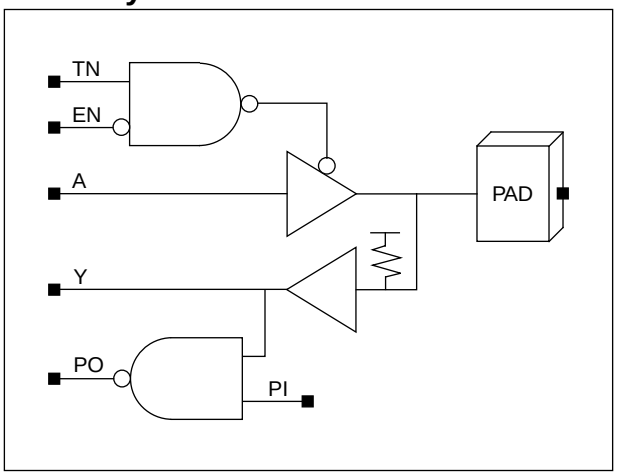
PvBaUDyz



PvBaDTyz



PvBaUTyz



Cell List

Cell Name	Function Description
STD80	
PSCKDC(2/4/8/12)	5V CMOS Level Input Clock Drivers
PSCKDCD(2/4/8/12)	5V CMOS Level Input Clock Drivers with Pull-Down
PSCKDCU(2/4/8/12)	5V CMOS Level Input Clock Drivers with Pull-Up
PSCKDL(2/4/8/12)	5V TTL Schmitt Trigger Level Input Clock Drivers
PSCKDLD(2/4/8/12)	5V TTL Schmitt Trigger Level Input Clock Drivers with Pull-Down
PSCKDLU(2/4/8/12)	5V TTL Schmitt Trigger Level Input Clock Drivers with Pull-Up
PSCKDS(2/4/8/12)	5V CMOS Schmitt Trigger Level Input Clock Drivers
PSCKDSD(2/4/8/12)	5V CMOS Schmitt Trigger Level Input Clock Drivers with Pull-Down
PSCKDSU(2/4/8/12)	5V CMOS Schmitt Trigger Level Input Clock Drivers with Pull-Up
PSCKDT(2/4/8/12)	5V TTL Level Input Clock Drivers
PSCKDTD(2/4/8/12)	5V TTL Level Input Clock Drivers with Pull-Down
PSCKDTU(2/4/8/12)	5V TTL Level Input Clock Drivers with Pull-Up
STDM80	
PSCKDC(2/4/6/8)	3.3V CMOS Level Input Clock Drivers
PSCKDCD(2/4/6/8)	3.3V CMOS Level Input Clock Drivers with Pull-Down
PSCKDCU(2/4/6/8)	3.3V CMOS Level Input Clock Drivers with Pull-Up
PSCKDS(2/4/6/8)	3.3V CMOS Schmitt Trigger Level Input Clock Drivers
PSCKDSD(2/4/6/8)	3.3V CMOS Schmitt Trigger Level Input Clock Drivers with Pull-Down
PSCKDSU(2/4/6/8)	3.3V CMOS Schmitt Trigger Level Input Clock Drivers with Pull-Up

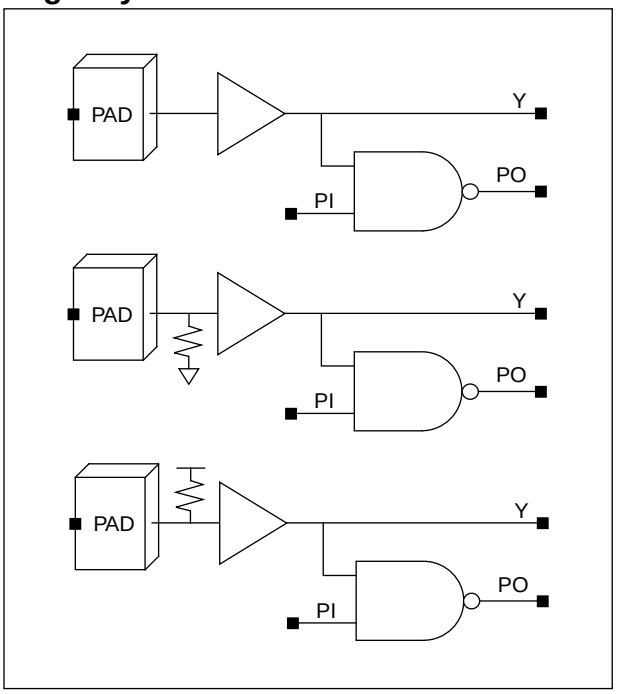
PSCKDCy/PSCKDCDy/PSCKDCUy

CMOS Level Input Clock Drivers

Cell Availability

Library	5V Operation	3.3V Operation
STD80	PSCKDC(2/4/8/12) PSCKDCD(2/4/8/12) PSCKDCU(2/4/8/12)	–
STDM80	–	PSCKDC(2/4/6/8) PSCKDCD(2/4/6/8) PSCKDCU(2/4/6/8)

Logic Symbol



Input Load (SL)

STD80	
	PI
PSCKDC(2/4/8/12)	1.6
PSCKDCD(2/4/8/12)	1.6
PSCKDCU(2/4/8/12)	1.6
STDM80	
	PI
PSCKDC(2/4/6/8)	1.9
PSCKDCD(2/4/6/8)	1.9
PSCKDCU(2/4/6/8)	1.9

I/O Slot

STD80/STDM80	
PSCKDCy/PSCKDCDy/PSCKDCUy	1.0

STD80 PSCKDC2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.70	0.24 + 0.005*SL	0.24 + 0.006*SL	0.24 + 0.005*SL
	t_{PHL}	0.64	0.22 + 0.005*SL	0.22 + 0.005*SL	0.22 + 0.005*SL
	t_R	1.08	0.09 + 0.012*SL	0.08 + 0.012*SL	0.07 + 0.012*SL
	t_F	0.84	0.08 + 0.009*SL	0.07 + 0.009*SL	0.06 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

STD80 PSCKDC4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.75	0.30 + 0.003*SL	0.30 + 0.003*SL	0.30 + 0.003*SL
	t_{PHL}	0.68	0.27 + 0.003*SL	0.27 + 0.003*SL	0.27 + 0.002*SL
	t_R	1.07	0.10 + 0.006*SL	0.09 + 0.006*SL	0.08 + 0.006*SL
	t_F	0.83	0.09 + 0.004*SL	0.08 + 0.005*SL	0.07 + 0.005*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

STD80 PSCKDC8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.76	0.32 + 0.001*SL	0.32 + 0.001*SL	0.32 + 0.001*SL
	t_{PHL}	0.73	0.32 + 0.001*SL	0.32 + 0.001*SL	0.32 + 0.001*SL
	t_R	1.06	0.10 + 0.003*SL	0.09 + 0.003*SL	0.08 + 0.003*SL
	t_F	0.82	0.10 + 0.002*SL	0.09 + 0.002*SL	0.07 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

STD80 PSCKDC12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.82	0.38 + 0.001*SL	0.38 + 0.001*SL	0.38 + 0.001*SL
	t_{PHL}	0.78	0.37 + 0.001*SL	0.38 + 0.001*SL	0.38 + 0.001*SL
	t_R	1.06	0.13 + 0.002*SL	0.11 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.84	0.12 + 0.001*SL	0.11 + 0.001*SL	0.10 + 0.002*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

STD80 PSCKDCD2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.71	0.26 + 0.005*SL	0.25 + 0.006*SL	0.26 + 0.005*SL
	t_{PHL}	0.64	0.22 + 0.005*SL	0.23 + 0.005*SL	0.22 + 0.005*SL
	t_R	1.08	0.09 + 0.012*SL	0.08 + 0.012*SL	0.08 + 0.012*SL
	t_F	0.84	0.08 + 0.009*SL	0.07 + 0.009*SL	0.06 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦ SL ≦ 83, *Group3 : 83 < SL

STD80 PSCKDCD4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.76	0.31 + 0.003*SL	0.31 + 0.003*SL	0.31 + 0.003*SL
	t_{PHL}	0.68	0.27 + 0.003*SL	0.27 + 0.003*SL	0.28 + 0.002*SL
	t_R	1.07	0.10 + 0.006*SL	0.09 + 0.006*SL	0.08 + 0.006*SL
	t_F	0.83	0.09 + 0.004*SL	0.08 + 0.005*SL	0.07 + 0.005*SL

*Group1 : SL < 109, *Group2 : 109 ≦ SL ≦ 164, *Group3 : 164 < SL

STD80 PSCKDCD8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.78	0.33 + 0.001*SL	0.33 + 0.001*SL	0.33 + 0.001*SL
	t_{PHL}	0.73	0.32 + 0.001*SL	0.33 + 0.001*SL	0.32 + 0.001*SL
	t_R	1.06	0.10 + 0.003*SL	0.09 + 0.003*SL	0.08 + 0.003*SL
	t_F	0.83	0.10 + 0.002*SL	0.08 + 0.002*SL	0.08 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦ SL ≦ 325, *Group3 : 325 < SL

STD80 PSCKDCD12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.83	0.39 + 0.001*SL	0.39 + 0.001*SL	0.39 + 0.001*SL
	t_{PHL}	0.79	0.38 + 0.001*SL	0.38 + 0.001*SL	0.39 + 0.001*SL
	t_R	1.06	0.12 + 0.002*SL	0.11 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.84	0.13 + 0.001*SL	0.11 + 0.001*SL	0.10 + 0.002*SL

*Group1 : SL < 324, *Group2 : 324 ≦ SL ≦ 486, *Group3 : 486 < SL

STD80 PSCKDCU2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.70	0.25 + 0.005*SL	0.25 + 0.005*SL	0.25 + 0.005*SL
	t_{PHL}	0.64	0.23 + 0.005*SL	0.23 + 0.005*SL	0.23 + 0.005*SL
	t_R	1.08	0.09 + 0.012*SL	0.08 + 0.012*SL	0.08 + 0.012*SL
	t_F	0.84	0.08 + 0.009*SL	0.07 + 0.009*SL	0.06 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

STD80 PSCKDCU4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.75	0.30 + 0.003*SL	0.30 + 0.003*SL	0.30 + 0.003*SL
	t_{PHL}	0.69	0.27 + 0.003*SL	0.28 + 0.002*SL	0.27 + 0.003*SL
	t_R	1.07	0.10 + 0.006*SL	0.09 + 0.006*SL	0.08 + 0.006*SL
	t_F	0.83	0.09 + 0.004*SL	0.08 + 0.005*SL	0.07 + 0.005*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

STD80 PSCKDCU8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.77	0.32 + 0.001*SL	0.32 + 0.001*SL	0.32 + 0.001*SL
	t_{PHL}	0.74	0.33 + 0.001*SL	0.33 + 0.001*SL	0.33 + 0.001*SL
	t_R	1.06	0.10 + 0.003*SL	0.09 + 0.003*SL	0.08 + 0.003*SL
	t_F	0.83	0.10 + 0.002*SL	0.08 + 0.002*SL	0.08 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

STD80 PSCKDCU12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.82	0.38 + 0.001*SL	0.38 + 0.001*SL	0.38 + 0.001*SL
	t_{PHL}	0.79	0.38 + 0.001*SL	0.39 + 0.001*SL	0.39 + 0.001*SL
	t_R	1.06	0.13 + 0.002*SL	0.11 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.83	0.12 + 0.001*SL	0.11 + 0.001*SL	0.09 + 0.002*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

STDM80 PSCKDC2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.14	0.36 + 0.004*SL	0.29 + 0.004*SL	0.30 + 0.004*SL
	t_{PHL}	0.95	0.31 + 0.003*SL	0.31 + 0.003*SL	0.32 + 0.003*SL
	t_R	1.97	0.14 + 0.009*SL	0.11 + 0.010*SL	0.14 + 0.009*SL
	t_F	1.31	0.11 + 0.006*SL	0.09 + 0.006*SL	0.08 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

STDM80 PSCKDC4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.26	0.42 + 0.002*SL	0.42 + 0.002*SL	0.43 + 0.002*SL
	t_{PHL}	1.05	0.41 + 0.002*SL	0.42 + 0.002*SL	0.41 + 0.002*SL
	t_R	1.96	0.16 + 0.005*SL	0.14 + 0.005*SL	0.13 + 0.005*SL
	t_F	1.32	0.13 + 0.003*SL	0.15 + 0.003*SL	0.13 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

STDM80 PSCKDC6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.23	0.39 + 0.001*SL	0.38 + 0.001*SL	0.39 + 0.001*SL
	t_{PHL}	1.05	0.41 + 0.001*SL	0.41 + 0.001*SL	0.41 + 0.001*SL
	t_R	1.96	0.14 + 0.003*SL	0.11 + 0.003*SL	0.14 + 0.003*SL
	t_F	1.33	0.23 + 0.002*SL	0.17 + 0.002*SL	0.14 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

STDM80 PSCKDC8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.28	0.44 + 0.001*SL	0.44 + 0.001*SL	0.44 + 0.001*SL
	t_{PHL}	1.13	0.49 + 0.001*SL	0.49 + 0.001*SL	0.49 + 0.001*SL
	t_R	1.95	0.15 + 0.002*SL	0.14 + 0.002*SL	0.14 + 0.002*SL
	t_F	1.33	0.17 + 0.001*SL	0.12 + 0.002*SL	0.15 + 0.002*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

STDM80 PSCKDCD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.17	0.32 + 0.004*SL	0.31 + 0.004*SL	0.33 + 0.004*SL
	t_{PHL}	0.96	0.32 + 0.003*SL	0.32 + 0.003*SL	0.32 + 0.003*SL
	t_R	1.97	0.14 + 0.009*SL	0.10 + 0.010*SL	0.15 + 0.009*SL
	t_F	1.30	0.12 + 0.006*SL	0.09 + 0.006*SL	0.08 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

STDM80 PSCKDCD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.27	0.43 + 0.002*SL	0.43 + 0.002*SL	0.44 + 0.002*SL
	t_{PHL}	1.06	0.42 + 0.002*SL	0.42 + 0.002*SL	0.42 + 0.002*SL
	t_R	1.96	0.16 + 0.005*SL	0.15 + 0.005*SL	0.14 + 0.005*SL
	t_F	1.31	0.18 + 0.003*SL	0.12 + 0.003*SL	0.11 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

STDM80 PSCKDCD6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.24	0.40 + 0.001*SL	0.40 + 0.001*SL	0.41 + 0.001*SL
	t_{PHL}	1.08	0.43 + 0.001*SL	0.43 + 0.001*SL	0.44 + 0.001*SL
	t_R	1.96	0.15 + 0.003*SL	0.11 + 0.003*SL	0.13 + 0.003*SL
	t_F	1.32	0.15 + 0.002*SL	0.10 + 0.002*SL	0.12 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

STDM80 PSCKDCD8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.28	0.44 + 0.001*SL	0.44 + 0.001*SL	0.44 + 0.001*SL
	t_{PHL}	1.13	0.49 + 0.001*SL	0.50 + 0.001*SL	0.50 + 0.001*SL
	t_R	1.96	0.16 + 0.002*SL	0.12 + 0.002*SL	0.15 + 0.002*SL
	t_F	1.31	0.16 + 0.001*SL	0.16 + 0.001*SL	0.10 + 0.002*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

STDM80 PSCKDCU2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.15	0.29 + 0.004*SL	0.30 + 0.004*SL	0.31 + 0.004*SL
	t_{PHL}	0.96	0.32 + 0.003*SL	0.32 + 0.003*SL	0.32 + 0.003*SL
	t_R	1.98	0.14 + 0.009*SL	0.11 + 0.010*SL	0.16 + 0.009*SL
	t_F	1.31	0.11 + 0.006*SL	0.10 + 0.006*SL	0.09 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

STDM80 PSCKDCU4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.26	0.42 + 0.002*SL	0.43 + 0.002*SL	0.43 + 0.002*SL
	t_{PHL}	1.06	0.42 + 0.002*SL	0.42 + 0.002*SL	0.42 + 0.002*SL
	t_R	1.96	0.18 + 0.005*SL	0.13 + 0.005*SL	0.14 + 0.005*SL
	t_F	1.31	0.15 + 0.003*SL	0.13 + 0.003*SL	0.11 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

STDM80 PSCKDCU6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.23	0.39 + 0.001*SL	0.39 + 0.001*SL	0.39 + 0.001*SL
	t_{PHL}	1.07	0.43 + 0.001*SL	0.43 + 0.001*SL	0.44 + 0.001*SL
	t_R	1.96	0.16 + 0.003*SL	0.13 + 0.003*SL	0.13 + 0.003*SL
	t_F	1.32	0.16 + 0.002*SL	0.13 + 0.002*SL	0.13 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

STDM80 PSCKDCU8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

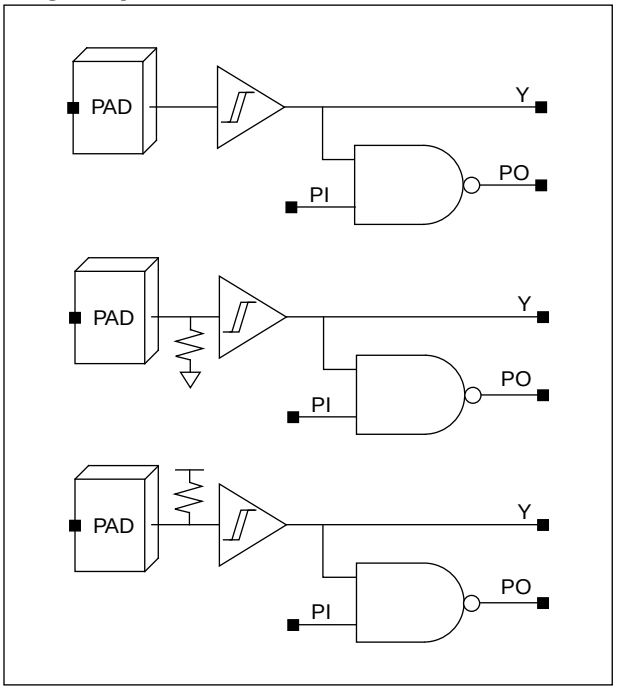
Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.28	0.45 + 0.001*SL	0.45 + 0.001*SL	0.45 + 0.001*SL
	t_{PHL}	1.13	0.49 + 0.001*SL	0.49 + 0.001*SL	0.50 + 0.001*SL
	t_R	1.95	0.15 + 0.002*SL	0.15 + 0.002*SL	0.13 + 0.002*SL
	t_F	1.32	0.17 + 0.001*SL	0.12 + 0.002*SL	0.13 + 0.002*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

Cell Availability

Library	5V Operation	3.3V Operation
STD80	PSCKDL(2/4/8/12) PSCKDLD(2/4/8/12) PSCKDLU(2/4/8/12)	–
STDM80	–	–

Logic Symbol



Input Load (SL)

STD80	
	PI
PSCKDL(2/4/8/12)	1.6
PSCKDLD(2/4/8/12)	1.6
PSCKDLU(2/4/8/12)	1.6

I/O Slot

STD80/STDM80	
PSCKDLy/PSCKDLDy/PSCKDLUy	1.0

STD80 PSCKDL2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.90	0.44 + 0.006*SL	0.45 + 0.005*SL	0.45 + 0.005*SL
	t_{PHL}	2.28	1.75 + 0.007*SL	1.79 + 0.006*SL	1.82 + 0.006*SL
	t_R	1.09	0.13 + 0.012*SL	0.11 + 0.012*SL	0.10 + 0.012*SL
	t_F	1.24	0.58 + 0.008*SL	0.58 + 0.008*SL	0.57 + 0.008*SL

*Group1 : SL < 56, *Group2 : 56 ≦ SL ≦ 83, *Group3 : 83 < SL

STD80 PSCKDL4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.99	0.53 + 0.003*SL	0.54 + 0.003*SL	0.54 + 0.003*SL
	t_{PHL}	2.94	2.36 + 0.004*SL	2.42 + 0.003*SL	2.46 + 0.003*SL
	t_R	1.10	0.16 + 0.006*SL	0.15 + 0.006*SL	0.13 + 0.006*SL
	t_F	1.48	0.83 + 0.004*SL	0.84 + 0.004*SL	0.84 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦ SL ≦ 164, *Group3 : 164 < SL

STD80 PSCKDL8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.92	0.47 + 0.001*SL	0.47 + 0.001*SL	0.47 + 0.001*SL
	t_{PHL}	2.51	1.99 + 0.002*SL	2.03 + 0.001*SL	2.06 + 0.001*SL
	t_R	1.08	0.14 + 0.003*SL	0.13 + 0.003*SL	0.12 + 0.003*SL
	t_F	1.36	0.73 + 0.002*SL	0.73 + 0.002*SL	0.72 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦ SL ≦ 325, *Group3 : 325 < SL

STD80 PSCKDL12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.01	0.55 + 0.001*SL	0.56 + 0.001*SL	0.57 + 0.001*SL
	t_{PHL}	3.22	2.65 + 0.001*SL	2.70 + 0.001*SL	2.74 + 0.001*SL
	t_R	1.10	0.18 + 0.002*SL	0.17 + 0.002*SL	0.15 + 0.002*SL
	t_F	1.64	1.02 + 0.001*SL	1.03 + 0.001*SL	1.03 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦ SL ≦ 486, *Group3 : 486 < SL

STD80 PSCKDLD2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.91	0.46 + 0.006*SL	0.46 + 0.005*SL	0.46 + 0.005*SL
	t_{PHL}	2.29	1.76 + 0.007*SL	1.80 + 0.006*SL	1.83 + 0.006*SL
	t_R	1.09	0.13 + 0.012*SL	0.11 + 0.012*SL	0.10 + 0.012*SL
	t_F	1.24	0.58 + 0.008*SL	0.58 + 0.008*SL	0.57 + 0.008*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

STD80 PSCKDLD4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.00	0.54 + 0.003*SL	0.55 + 0.003*SL	0.55 + 0.003*SL
	t_{PHL}	2.95	2.38 + 0.004*SL	2.43 + 0.003*SL	2.47 + 0.003*SL
	t_R	1.10	0.16 + 0.006*SL	0.15 + 0.006*SL	0.13 + 0.006*SL
	t_F	1.48	0.83 + 0.004*SL	0.85 + 0.004*SL	0.83 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

STD80 PSCKDLD8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.93	0.48 + 0.001*SL	0.48 + 0.001*SL	0.48 + 0.001*SL
	t_{PHL}	2.53	2.00 + 0.002*SL	2.05 + 0.001*SL	2.08 + 0.001*SL
	t_R	1.08	0.14 + 0.003*SL	0.13 + 0.003*SL	0.12 + 0.003*SL
	t_F	1.36	0.73 + 0.002*SL	0.73 + 0.002*SL	0.72 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

STD80 PSCKDLD12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.02	0.57 + 0.001*SL	0.58 + 0.001*SL	0.58 + 0.001*SL
	t_{PHL}	3.24	2.67 + 0.001*SL	2.72 + 0.001*SL	2.76 + 0.001*SL
	t_R	1.10	0.19 + 0.002*SL	0.17 + 0.002*SL	0.15 + 0.002*SL
	t_F	1.64	1.01 + 0.001*SL	1.03 + 0.001*SL	1.03 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

STD80 PSCKDLU2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.90	0.45 + 0.005*SL	0.45 + 0.005*SL	0.45 + 0.005*SL
	t_{PHL}	2.32	1.78 + 0.007*SL	1.83 + 0.006*SL	1.85 + 0.006*SL
	t_R	1.09	0.13 + 0.012*SL	0.11 + 0.012*SL	0.10 + 0.012*SL
	t_F	1.24	0.59 + 0.008*SL	0.58 + 0.008*SL	0.57 + 0.008*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

STD80 PSCKDLU4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.99	0.53 + 0.003*SL	0.54 + 0.003*SL	0.54 + 0.003*SL
	t_{PHL}	2.98	2.41 + 0.004*SL	2.47 + 0.003*SL	2.50 + 0.003*SL
	t_R	1.10	0.16 + 0.006*SL	0.15 + 0.006*SL	0.13 + 0.006*SL
	t_F	1.48	0.83 + 0.004*SL	0.85 + 0.004*SL	0.84 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

STD80 PSCKDLU8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.92	0.47 + 0.001*SL	0.47 + 0.001*SL	0.47 + 0.001*SL
	t_{PHL}	2.55	2.03 + 0.002*SL	2.07 + 0.001*SL	2.10 + 0.001*SL
	t_R	1.08	0.14 + 0.003*SL	0.13 + 0.003*SL	0.12 + 0.003*SL
	t_F	1.36	0.74 + 0.002*SL	0.74 + 0.002*SL	0.72 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

STD80 PSCKDLU12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

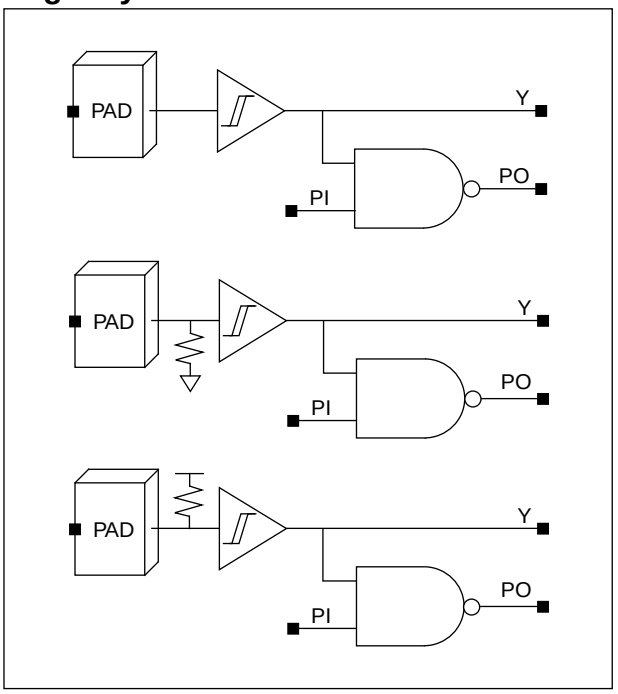
Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.01	0.56 + 0.001*SL	0.57 + 0.001*SL	0.57 + 0.001*SL
	t_{PHL}	3.27	2.70 + 0.001*SL	2.75 + 0.001*SL	2.79 + 0.001*SL
	t_R	1.10	0.18 + 0.002*SL	0.17 + 0.002*SL	0.15 + 0.002*SL
	t_F	1.65	1.02 + 0.001*SL	1.04 + 0.001*SL	1.04 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

Cell Availability

Library	5V Operation	3.3V Operation
STD80	PSCKDS(2/4/8/12) PSCKDSD(2/4/8/12) PSCKDSU(2/4/8/12)	–
STDM80	–	PSCKDS(2/4/6/8) PSCKDSD(2/4/6/8) PSCKDSU(2/4/6/8)

Logic Symbol



Input Load (SL)

STD80	
	PI
PSCKDS(2/4/8/12)	1.6
PSCKDSD(2/4/8/12)	1.6
PSCKDSU(2/4/8/12)	1.6
STDM80	
	PI
PSCKDS(2/4/6/8)	1.9
PSCKDSD(2/4/6/8)	1.9
PSCKDSU(2/4/6/8)	1.9

I/O Slot

STD80/STDM80	
PSCKDSy/PSCKDSDy/PSCKDSUy	1.0

STD80 PSCKDS2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.77	0.32 + 0.005*SL	0.31 + 0.006*SL	0.32 + 0.005*SL
	t_{PHL}	1.00	0.55 + 0.006*SL	0.57 + 0.005*SL	0.58 + 0.005*SL
	t_R	1.09	0.11 + 0.012*SL	0.10 + 0.012*SL	0.09 + 0.012*SL
	t_F	0.93	0.22 + 0.009*SL	0.21 + 0.009*SL	0.19 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

STD80 PSCKDS4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.88	0.43 + 0.003*SL	0.43 + 0.003*SL	0.43 + 0.003*SL
	t_{PHL}	1.27	0.79 + 0.003*SL	0.82 + 0.003*SL	0.84 + 0.003*SL
	t_R	1.09	0.15 + 0.006*SL	0.13 + 0.006*SL	0.12 + 0.006*SL
	t_F	1.02	0.35 + 0.004*SL	0.34 + 0.004*SL	0.32 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

STD80 PSCKDS8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.92	0.48 + 0.001*SL	0.48 + 0.001*SL	0.48 + 0.001*SL
	t_{PHL}	1.31	0.84 + 0.002*SL	0.87 + 0.001*SL	0.89 + 0.001*SL
	t_R	1.08	0.15 + 0.003*SL	0.13 + 0.003*SL	0.12 + 0.003*SL
	t_F	1.02	0.35 + 0.002*SL	0.34 + 0.002*SL	0.33 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

STD80 PSCKDS12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.04	0.59 + 0.001*SL	0.59 + 0.001*SL	0.60 + 0.001*SL
	t_{PHL}	1.58	1.08 + 0.001*SL	1.12 + 0.001*SL	1.14 + 0.001*SL
	t_R	1.11	0.19 + 0.002*SL	0.17 + 0.002*SL	0.15 + 0.002*SL
	t_F	1.14	0.49 + 0.001*SL	0.48 + 0.001*SL	0.47 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

STD80 PSCKDSD2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.78	0.33 + 0.005*SL	0.33 + 0.005*SL	0.33 + 0.005*SL
	t_{PHL}	1.01	0.56 + 0.006*SL	0.58 + 0.005*SL	0.59 + 0.005*SL
	t_R	1.09	0.11 + 0.012*SL	0.10 + 0.012*SL	0.09 + 0.012*SL
	t_F	0.93	0.22 + 0.009*SL	0.21 + 0.009*SL	0.19 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦ SL ≦ 83, *Group3 : 83 < SL

STD80 PSCKDSD4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.89	0.44 + 0.003*SL	0.44 + 0.003*SL	0.44 + 0.003*SL
	t_{PHL}	1.28	0.81 + 0.003*SL	0.83 + 0.003*SL	0.85 + 0.003*SL
	t_R	1.09	0.15 + 0.006*SL	0.13 + 0.006*SL	0.12 + 0.006*SL
	t_F	1.02	0.35 + 0.004*SL	0.34 + 0.004*SL	0.33 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦ SL ≦ 164, *Group3 : 164 < SL

STD80 PSCKDSD8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.94	0.49 + 0.001*SL	0.50 + 0.001*SL	0.50 + 0.001*SL
	t_{PHL}	1.33	0.85 + 0.001*SL	0.88 + 0.001*SL	0.90 + 0.001*SL
	t_R	1.08	0.15 + 0.003*SL	0.13 + 0.003*SL	0.12 + 0.003*SL
	t_F	1.02	0.35 + 0.002*SL	0.34 + 0.002*SL	0.33 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦ SL ≦ 325, *Group3 : 325 < SL

STD80 PSCKDSD12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.06	0.60 + 0.001*SL	0.61 + 0.001*SL	0.61 + 0.001*SL
	t_{PHL}	1.59	1.10 + 0.001*SL	1.13 + 0.001*SL	1.15 + 0.001*SL
	t_R	1.11	0.19 + 0.002*SL	0.18 + 0.002*SL	0.16 + 0.002*SL
	t_F	1.14	0.48 + 0.001*SL	0.48 + 0.001*SL	0.47 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦ SL ≦ 486, *Group3 : 486 < SL

STD80 PSCKDSU2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.78	0.32 + 0.005*SL	0.33 + 0.005*SL	0.32 + 0.005*SL
	t_{PHL}	1.01	0.56 + 0.006*SL	0.58 + 0.005*SL	0.58 + 0.005*SL
	t_R	1.09	0.11 + 0.012*SL	0.10 + 0.012*SL	0.09 + 0.012*SL
	t_F	0.93	0.22 + 0.009*SL	0.21 + 0.009*SL	0.20 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦ SL ≦ 83, *Group3 : 83 < SL

STD80 PSCKDSU4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.89	0.44 + 0.003*SL	0.44 + 0.003*SL	0.44 + 0.003*SL
	t_{PHL}	1.28	0.80 + 0.003*SL	0.83 + 0.003*SL	0.85 + 0.003*SL
	t_R	1.09	0.15 + 0.006*SL	0.13 + 0.006*SL	0.12 + 0.006*SL
	t_F	1.03	0.35 + 0.004*SL	0.34 + 0.004*SL	0.33 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦ SL ≦ 164, *Group3 : 164 < SL

STD80 PSCKDSU8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.93	0.48 + 0.001*SL	0.49 + 0.001*SL	0.49 + 0.001*SL
	t_{PHL}	1.33	0.85 + 0.002*SL	0.88 + 0.001*SL	0.90 + 0.001*SL
	t_R	1.08	0.15 + 0.003*SL	0.13 + 0.003*SL	0.12 + 0.003*SL
	t_F	1.02	0.35 + 0.002*SL	0.34 + 0.002*SL	0.33 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦ SL ≦ 325, *Group3 : 325 < SL

STD80 PSCKDSU12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.05	0.59 + 0.001*SL	0.60 + 0.001*SL	0.61 + 0.001*SL
	t_{PHL}	1.60	1.10 + 0.001*SL	1.13 + 0.001*SL	1.16 + 0.001*SL
	t_R	1.11	0.19 + 0.002*SL	0.17 + 0.002*SL	0.15 + 0.002*SL
	t_F	1.14	0.49 + 0.001*SL	0.48 + 0.001*SL	0.47 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦ SL ≦ 486, *Group3 : 486 < SL

STDM80 PSCKDS2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.48	0.62 + 0.004*SL	0.63 + 0.004*SL	0.63 + 0.004*SL
	t_{PHL}	2.03	1.28 + 0.004*SL	1.34 + 0.004*SL	1.37 + 0.003*SL
	t_R	2.01	0.23 + 0.009*SL	0.21 + 0.009*SL	0.18 + 0.009*SL
	t_F	1.52	0.39 + 0.006*SL	0.39 + 0.006*SL	0.42 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

STDM80 PSCKDS4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.73	0.84 + 0.002*SL	0.87 + 0.002*SL	0.88 + 0.002*SL
	t_{PHL}	2.70	1.86 + 0.002*SL	1.93 + 0.002*SL	1.99 + 0.002*SL
	t_R	2.07	0.32 + 0.005*SL	0.31 + 0.005*SL	0.30 + 0.005*SL
	t_F	1.74	0.62 + 0.003*SL	0.64 + 0.003*SL	0.64 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

STDM80 PSCKDS6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.62	0.75 + 0.002*SL	0.77 + 0.001*SL	0.78 + 0.001*SL
	t_{PHL}	2.37	1.57 + 0.001*SL	1.64 + 0.001*SL	1.68 + 0.001*SL
	t_R	2.03	0.28 + 0.003*SL	0.23 + 0.003*SL	0.24 + 0.003*SL
	t_F	1.61	0.51 + 0.002*SL	0.48 + 0.002*SL	0.49 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

STDM80 PSCKDS8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.74	0.86 + 0.001*SL	0.89 + 0.001*SL	0.90 + 0.001*SL
	t_{PHL}	2.70	1.87 + 0.001*SL	1.94 + 0.001*SL	2.00 + 0.001*SL
	t_R	2.06	0.30 + 0.002*SL	0.31 + 0.002*SL	0.28 + 0.002*SL
	t_F	1.72	0.61 + 0.001*SL	0.63 + 0.001*SL	0.63 + 0.001*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

STDM80 PSCKDSD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.50	0.63 + 0.004*SL	0.65 + 0.004*SL	0.65 + 0.004*SL
	t_{PHL}	2.05	1.30 + 0.004*SL	1.35 + 0.004*SL	1.39 + 0.003*SL
	t_R	2.01	0.23 + 0.009*SL	0.21 + 0.009*SL	0.18 + 0.009*SL
	t_F	1.51	0.39 + 0.006*SL	0.42 + 0.006*SL	0.37 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

STDM80 PSCKDSD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.74	0.85 + 0.002*SL	0.89 + 0.002*SL	0.91 + 0.002*SL
	t_{PHL}	2.72	1.88 + 0.002*SL	1.96 + 0.002*SL	2.01 + 0.002*SL
	t_R	2.07	0.31 + 0.005*SL	0.35 + 0.004*SL	0.28 + 0.005*SL
	t_F	1.73	0.63 + 0.003*SL	0.63 + 0.003*SL	0.62 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

STDM80 PSCKDSD6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.63	0.76 + 0.002*SL	0.78 + 0.001*SL	0.79 + 0.001*SL
	t_{PHL}	2.39	1.59 + 0.001*SL	1.66 + 0.001*SL	1.70 + 0.001*SL
	t_R	2.03	0.26 + 0.003*SL	0.25 + 0.003*SL	0.22 + 0.003*SL
	t_F	1.62	0.51 + 0.002*SL	0.48 + 0.002*SL	0.50 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

STDM80 PSCKDSD8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.76	0.87 + 0.001*SL	0.90 + 0.001*SL	0.91 + 0.001*SL
	t_{PHL}	2.72	1.88 + 0.001*SL	1.96 + 0.001*SL	2.02 + 0.001*SL
	t_R	2.06	0.32 + 0.002*SL	0.31 + 0.002*SL	0.26 + 0.002*SL
	t_F	1.72	0.64 + 0.001*SL	0.62 + 0.001*SL	0.60 + 0.001*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

STDM80 PSCKDSU2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.49	0.63 + 0.004*SL	0.64 + 0.004*SL	0.65 + 0.004*SL
	t_{PHL}	2.05	1.29 + 0.004*SL	1.35 + 0.004*SL	1.38 + 0.003*SL
	t_R	2.01	0.24 + 0.009*SL	0.19 + 0.009*SL	0.20 + 0.009*SL
	t_F	1.52	0.40 + 0.006*SL	0.41 + 0.006*SL	0.39 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

STDM80 PSCKDSU4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.74	0.85 + 0.002*SL	0.88 + 0.002*SL	0.89 + 0.002*SL
	t_{PHL}	2.72	1.88 + 0.002*SL	1.96 + 0.002*SL	2.02 + 0.002*SL
	t_R	2.06	0.32 + 0.005*SL	0.32 + 0.005*SL	0.28 + 0.005*SL
	t_F	1.74	0.64 + 0.003*SL	0.65 + 0.003*SL	0.63 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

STDM80 PSCKDSU6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.63	0.76 + 0.002*SL	0.78 + 0.001*SL	0.78 + 0.001*SL
	t_{PHL}	2.38	1.59 + 0.001*SL	1.66 + 0.001*SL	1.70 + 0.001*SL
	t_R	2.03	0.28 + 0.003*SL	0.23 + 0.003*SL	0.24 + 0.003*SL
	t_F	1.61	0.51 + 0.002*SL	0.49 + 0.002*SL	0.49 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

STDM80 PSCKDSU8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.75	0.87 + 0.001*SL	0.90 + 0.001*SL	0.91 + 0.001*SL
	t_{PHL}	2.72	1.88 + 0.001*SL	1.96 + 0.001*SL	2.02 + 0.001*SL
	t_R	2.06	0.30 + 0.002*SL	0.30 + 0.002*SL	0.27 + 0.002*SL
	t_F	1.72	0.62 + 0.001*SL	0.63 + 0.001*SL	0.61 + 0.001*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

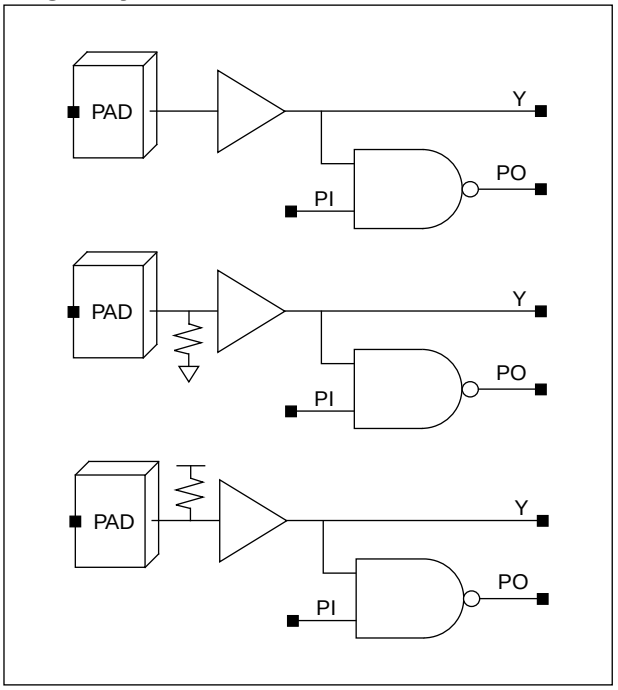
PSCKDTy/PSCKDTDy/PSCKDTUy

TTL Level Input Clock Drivers

Cell Availability

Library	5V Operation	3.3V Operation
STD80	PSCKDT(2/4/8/12) PSCKDTD(2/4/8/12) PSCKDTU(2/4/8/12)	–
STDM80	–	–

Logic Symbol



Input Load (SL)

STD80	
	PI
PSCKDT(2/4/8/12)	1.6
PSCKDTD(2/4/8/12)	1.6
PSCKDTU(2/4/8/12)	1.6

I/O Slot

STD80/STDM80	
PSCKDTy/PSCKDTDy/PSCKDTUy	1.0

STD80 PSCKDT2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.68	0.23 + 0.005*SL	0.22 + 0.006*SL	0.22 + 0.006*SL
	t_{PHL}	0.90	0.45 + 0.006*SL	0.47 + 0.005*SL	0.48 + 0.005*SL
	t_R	1.08	0.08 + 0.012*SL	0.08 + 0.012*SL	0.07 + 0.012*SL
	t_F	0.92	0.20 + 0.009*SL	0.19 + 0.009*SL	0.18 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦ SL ≦ 83, *Group3 : 83 < SL

STD80 PSCKDT4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.72	0.27 + 0.003*SL	0.27 + 0.003*SL	0.27 + 0.003*SL
	t_{PHL}	1.13	0.65 + 0.003*SL	0.68 + 0.003*SL	0.70 + 0.003*SL
	t_R	1.06	0.08 + 0.006*SL	0.07 + 0.006*SL	0.07 + 0.006*SL
	t_F	1.01	0.33 + 0.004*SL	0.31 + 0.004*SL	0.31 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦ SL ≦ 164, *Group3 : 164 < SL

STD80 PSCKDT8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.75	0.30 + 0.001*SL	0.30 + 0.001*SL	0.30 + 0.001*SL
	t_{PHL}	1.17	0.69 + 0.001*SL	0.72 + 0.001*SL	0.74 + 0.001*SL
	t_R	1.05	0.08 + 0.003*SL	0.07 + 0.003*SL	0.07 + 0.003*SL
	t_F	1.00	0.32 + 0.002*SL	0.32 + 0.002*SL	0.30 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦ SL ≦ 325, *Group3 : 325 < SL

STD80 PSCKDT12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.78	0.34 + 0.001*SL	0.34 + 0.001*SL	0.34 + 0.001*SL
	t_{PHL}	1.39	0.89 + 0.001*SL	0.92 + 0.001*SL	0.95 + 0.001*SL
	t_R	1.05	0.09 + 0.002*SL	0.08 + 0.002*SL	0.07 + 0.002*SL
	t_F	1.12	0.45 + 0.001*SL	0.45 + 0.001*SL	0.44 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦ SL ≦ 486, *Group3 : 486 < SL

STD80 PSCKDTD2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.70	0.24 + 0.005*SL	0.24 + 0.006*SL	0.24 + 0.005*SL
	t_{PHL}	0.91	0.46 + 0.006*SL	0.48 + 0.005*SL	0.49 + 0.005*SL
	t_R	1.08	0.08 + 0.012*SL	0.08 + 0.012*SL	0.07 + 0.012*SL
	t_F	0.92	0.20 + 0.009*SL	0.20 + 0.009*SL	0.18 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

STD80 PSCKDTD4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.73	0.28 + 0.003*SL	0.28 + 0.003*SL	0.28 + 0.003*SL
	t_{PHL}	1.14	0.66 + 0.003*SL	0.69 + 0.003*SL	0.71 + 0.003*SL
	t_R	1.06	0.08 + 0.006*SL	0.07 + 0.006*SL	0.07 + 0.006*SL
	t_F	1.01	0.33 + 0.004*SL	0.32 + 0.004*SL	0.31 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

STD80 PSCKDTD8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.76	0.32 + 0.001*SL	0.31 + 0.001*SL	0.31 + 0.001*SL
	t_{PHL}	1.18	0.70 + 0.002*SL	0.73 + 0.001*SL	0.75 + 0.001*SL
	t_R	1.05	0.09 + 0.003*SL	0.07 + 0.003*SL	0.07 + 0.003*SL
	t_F	1.00	0.32 + 0.002*SL	0.32 + 0.002*SL	0.31 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

STD80 PSCKDTD12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.80	0.35 + 0.001*SL	0.35 + 0.001*SL	0.35 + 0.001*SL
	t_{PHL}	1.40	0.90 + 0.001*SL	0.93 + 0.001*SL	0.95 + 0.001*SL
	t_R	1.05	0.09 + 0.002*SL	0.08 + 0.002*SL	0.07 + 0.002*SL
	t_F	1.12	0.45 + 0.001*SL	0.45 + 0.001*SL	0.43 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

STD80 PSCKDTU2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.68	0.23 + 0.005*SL	0.22 + 0.006*SL	0.23 + 0.005*SL
	t_{PHL}	0.91	0.46 + 0.006*SL	0.48 + 0.005*SL	0.49 + 0.005*SL
	t_R	1.08	0.08 + 0.012*SL	0.07 + 0.012*SL	0.07 + 0.012*SL
	t_F	0.92	0.20 + 0.009*SL	0.19 + 0.009*SL	0.19 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦ SL ≦ 83, *Group3 : 83 < SL

STD80 PSCKDTU4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.72	0.27 + 0.003*SL	0.27 + 0.003*SL	0.27 + 0.003*SL
	t_{PHL}	1.14	0.66 + 0.003*SL	0.69 + 0.003*SL	0.71 + 0.003*SL
	t_R	1.06	0.08 + 0.006*SL	0.07 + 0.006*SL	0.07 + 0.006*SL
	t_F	1.01	0.33 + 0.004*SL	0.32 + 0.004*SL	0.31 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦ SL ≦ 164, *Group3 : 164 < SL

STD80 PSCKDTU8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.75	0.30 + 0.001*SL	0.30 + 0.001*SL	0.30 + 0.001*SL
	t_{PHL}	1.18	0.70 + 0.002*SL	0.73 + 0.001*SL	0.75 + 0.001*SL
	t_R	1.05	0.08 + 0.003*SL	0.07 + 0.003*SL	0.07 + 0.003*SL
	t_F	1.01	0.33 + 0.002*SL	0.32 + 0.002*SL	0.31 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦ SL ≦ 325, *Group3 : 325 < SL

STD80 PSCKDTU12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.78	0.34 + 0.001*SL	0.34 + 0.001*SL	0.34 + 0.001*SL
	t_{PHL}	1.40	0.90 + 0.001*SL	0.93 + 0.001*SL	0.96 + 0.001*SL
	t_R	1.05	0.09 + 0.002*SL	0.08 + 0.002*SL	0.07 + 0.002*SL
	t_F	1.12	0.46 + 0.001*SL	0.45 + 0.001*SL	0.44 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦ SL ≦ 486, *Group3 : 486 < SL

OSCILLATORS

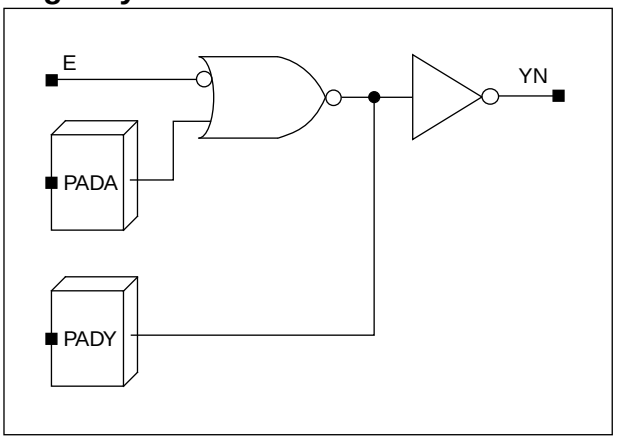
Cell List

Cell Name	Function Description
STD80/STDM80	
PSOSCK1	Oscillator Cell with Enable (~ 100KHz)
PSOSCK2	Oscillator Cell with Enable (100K ~ 1MHz)
PSOSCK16	Oscillator Cell with Enable and Resistor (~ 100KHz)
PSOSCK26	Oscillator Cell with Enable and Resistor (100K ~ 1MHz)
PSOSCM1	Oscillator Cell with Enable (1M ~ 10MHz)
PSOSCM2	Oscillator Cell with Enable (10M ~ 30MHz)
PSOSCM3	Oscillator Cell with Enable (30M ~ 60MHz)
PSOSCM4	Oscillator Cell with Enable (60M ~ 80MHz)
PSOSCM5	Oscillator Cell with Enable (80M ~ 100MHz)
PSOSCM6	Oscillator Cell with Enable (50M ~ 100MHz)
PSOSCM16	Oscillator Cell with Enable and Resistor (1M ~ 10MHz)
PSOSCM26	Oscillator Cell with Enable and Resistor (10M ~ 30MHz)
PSOSCM36	Oscillator Cell with Enable and Resistor (30M ~ 60MHz)
PSOSCM46	Oscillator Cell with Enable and Resistor (60M ~ 80MHz)
PSOSCM56	Oscillator Cell with Enable and Resistor (80M ~ 100MHz)
PSOSCM66	Oscillator Cell with Enable and Resistor (50M ~ 100MHz)

PSOSCK(1/2)

Oscillator Cell with Enable

Logic Symbol



Truth Table

PADA	E	PADY	YN
0	0	0	1
0	1	1	0
1	0	0	1
1	1	0	1

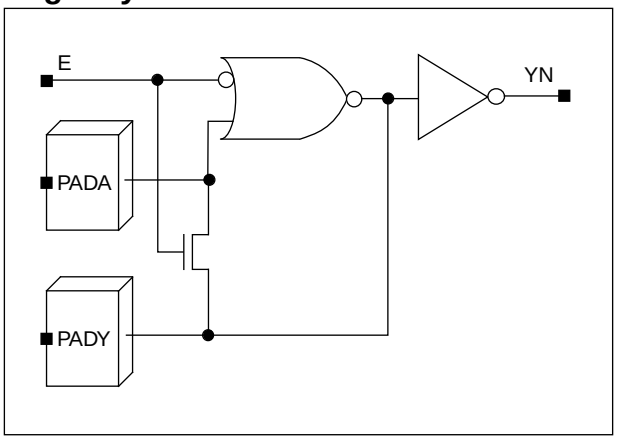
Cell Data

Input Load (SL)	I/O Slots
PSOSCK1/2	*PSOSCK1/2*
E	
2.6	2.0

PSOSCK(16/26)

Oscillator Cell with Enable and Resistor

Logic Symbol



Truth Table

PADA	E	PADY	YN
0	0	0	1
0	1	1	0
1	0	0	1
1	1	0	1

Cell Data

Input Load (SL)	I/O Slots
PSOSCK(16/26)	*PSOSCK(16/26)*
E	
2.6	2.0

STD80 PSOSCK1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	259.38	0.46 + 5.178*CL	0.49 + 5.178*CL	0.44 + 5.179*CL
	t_{PHL}	349.70	0.50 + 6.984*CL	0.50 + 6.984*CL	0.50 + 6.984*CL
	t_R	582.75	0.55 + 11.644*CL	0.62 + 11.643*CL	0.77 + 11.641*CL
	t_F	772.14	0.82 + 15.426*CL	0.55 + 15.430*CL	0.83 + 15.427*CL

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to PADY	t_{PLH}	259.45	0.53 + 5.178*CL	0.48 + 5.179*CL	0.57 + 5.178*CL
	t_{PHL}	349.81	0.61 + 6.984*CL	0.61 + 6.984*CL	0.61 + 6.984*CL
	t_R	582.75	0.59 + 11.643*CL	0.54 + 11.644*CL	0.70 + 11.642*CL
	t_F	772.14	0.82 + 15.426*CL	0.55 + 15.430*CL	0.83 + 15.427*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.60	0.60 + 0.179*SL	0.61 + 0.178*SL	0.60 + 0.178*SL
	t_{PHL}	0.53	0.53 + 0.130*SL	0.54 + 0.129*SL	0.54 + 0.129*SL
	t_R	0.26	0.26 + 0.082*SL	0.25 + 0.086*SL	0.24 + 0.087*SL
	t_F	0.18	0.18 + 0.068*SL	0.17 + 0.071*SL	0.17 + 0.072*SL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to YN	t_{PLH}	0.72	0.72 + 0.178*SL	0.72 + 0.178*SL	0.72 + 0.178*SL
	t_{PHL}	0.60	0.60 + 0.130*SL	0.61 + 0.129*SL	0.61 + 0.129*SL
	t_R	0.25	0.25 + 0.084*SL	0.25 + 0.086*SL	0.24 + 0.087*SL
	t_F	0.18	0.18 + 0.069*SL	0.17 + 0.071*SL	0.17 + 0.072*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCK2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	26.32	0.43 + 0.518*CL	0.42 + 0.518*CL	0.43 + 0.518*CL
	t_{PHL}	35.38	0.46 + 0.698*CL	0.46 + 0.698*CL	0.46 + 0.698*CL
	t_R	58.61	0.39 + 1.164*CL	0.40 + 1.164*CL	0.37 + 1.165*CL
	t_F	77.67	0.54 + 1.543*CL	0.51 + 1.543*CL	0.54 + 1.543*CL

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to PADY	t_{PLH}	26.40	0.50 + 0.518*CL	0.50 + 0.518*CL	0.51 + 0.518*CL
	t_{PHL}	35.48	0.56 + 0.698*CL	0.56 + 0.698*CL	0.56 + 0.698*CL
	t_R	58.61	0.39 + 1.164*CL	0.40 + 1.164*CL	0.37 + 1.165*CL
	t_F	77.67	0.52 + 1.543*CL	0.59 + 1.542*CL	0.53 + 1.543*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.54	0.54 + 0.022*SL	0.54 + 0.021*SL	0.55 + 0.020*SL
	t_{PHL}	0.46	0.46 + 0.015*SL	0.46 + 0.014*SL	0.47 + 0.013*SL
	t_R	0.20	0.20 + 0.008*SL	0.20 + 0.009*SL	0.19 + 0.010*SL
	t_F	0.14	0.14 + 0.007*SL	0.14 + 0.007*SL	0.13 + 0.008*SL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to YN	t_{PLH}	0.66	0.66 + 0.020*SL	0.66 + 0.020*SL	0.66 + 0.020*SL
	t_{PHL}	0.54	0.54 + 0.015*SL	0.54 + 0.014*SL	0.54 + 0.013*SL
	t_R	0.18	0.18 + 0.009*SL	0.18 + 0.010*SL	0.18 + 0.010*SL
	t_F	0.13	0.13 + 0.007*SL	0.13 + 0.007*SL	0.13 + 0.008*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCK1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	259.38	0.46 + 5.178*CL	0.49 + 5.178*CL	0.44 + 5.179*CL
	t_{PHL}	349.70	0.50 + 6.984*CL	0.50 + 6.984*CL	0.50 + 6.984*CL
	t_R	582.75	0.55 + 11.644*CL	0.62 + 11.643*CL	0.77 + 11.641*CL
	t_F	772.14	0.82 + 15.426*CL	0.55 + 15.430*CL	0.83 + 15.427*CL

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to PADY	t_{PLH}	259.45	0.53 + 5.178*CL	0.48 + 5.179*CL	0.57 + 5.178*CL
	t_{PHL}	349.81	0.61 + 6.984*CL	0.61 + 6.984*CL	0.61 + 6.984*CL
	t_R	582.75	0.59 + 11.643*CL	0.54 + 11.644*CL	0.70 + 11.642*CL
	t_F	772.14	0.82 + 15.426*CL	0.55 + 15.430*CL	0.83 + 15.427*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.60	0.60 + 0.179*SL	0.61 + 0.178*SL	0.60 + 0.178*SL
	t_{PHL}	0.53	0.53 + 0.130*SL	0.54 + 0.129*SL	0.54 + 0.129*SL
	t_R	0.26	0.26 + 0.082*SL	0.25 + 0.086*SL	0.24 + 0.087*SL
	t_F	0.18	0.18 + 0.068*SL	0.17 + 0.071*SL	0.17 + 0.072*SL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to YN	t_{PLH}	0.72	0.72 + 0.178*SL	0.72 + 0.178*SL	0.72 + 0.178*SL
	t_{PHL}	0.60	0.60 + 0.130*SL	0.61 + 0.129*SL	0.61 + 0.129*SL
	t_R	0.25	0.25 + 0.084*SL	0.25 + 0.086*SL	0.24 + 0.087*SL
	t_F	0.18	0.18 + 0.069*SL	0.17 + 0.071*SL	0.17 + 0.072*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCK2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	26.32	0.43 + 0.518*CL	0.42 + 0.518*CL	0.43 + 0.518*CL
	t_{PHL}	35.38	0.46 + 0.698*CL	0.46 + 0.698*CL	0.46 + 0.698*CL
	t_R	58.61	0.39 + 1.164*CL	0.40 + 1.164*CL	0.37 + 1.165*CL
	t_F	77.67	0.54 + 1.543*CL	0.51 + 1.543*CL	0.54 + 1.543*CL

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to PADY	t_{PLH}	26.40	0.50 + 0.518*CL	0.50 + 0.518*CL	0.51 + 0.518*CL
	t_{PHL}	35.48	0.56 + 0.698*CL	0.56 + 0.698*CL	0.56 + 0.698*CL
	t_R	58.61	0.39 + 1.164*CL	0.40 + 1.164*CL	0.37 + 1.165*CL
	t_F	77.67	0.52 + 1.543*CL	0.59 + 1.542*CL	0.53 + 1.543*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.54	0.54 + 0.022*SL	0.54 + 0.021*SL	0.55 + 0.020*SL
	t_{PHL}	0.46	0.46 + 0.015*SL	0.46 + 0.014*SL	0.47 + 0.013*SL
	t_R	0.20	0.20 + 0.008*SL	0.20 + 0.009*SL	0.19 + 0.010*SL
	t_F	0.14	0.14 + 0.007*SL	0.14 + 0.007*SL	0.13 + 0.008*SL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to YN	t_{PLH}	0.66	0.66 + 0.020*SL	0.66 + 0.020*SL	0.66 + 0.020*SL
	t_{PHL}	0.54	0.54 + 0.015*SL	0.54 + 0.014*SL	0.54 + 0.013*SL
	t_R	0.18	0.18 + 0.009*SL	0.18 + 0.010*SL	0.18 + 0.010*SL
	t_F	0.13	0.13 + 0.007*SL	0.13 + 0.007*SL	0.13 + 0.008*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCK16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	259.38	0.46 + 5.178*CL	0.49 + 5.178*CL	0.44 + 5.179*CL
	t_{PHL}	349.70	0.50 + 6.984*CL	0.50 + 6.984*CL	0.50 + 6.984*CL
	t_R	582.75	0.55 + 11.644*CL	0.62 + 11.643*CL	0.77 + 11.641*CL
	t_F	772.14	0.82 + 15.426*CL	0.55 + 15.430*CL	0.83 + 15.427*CL

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to PADY	t_{PLH}	259.45	0.53 + 5.178*CL	0.48 + 5.179*CL	0.57 + 5.178*CL
	t_{PHL}	349.81	0.61 + 6.984*CL	0.61 + 6.984*CL	0.61 + 6.984*CL
	t_R	582.75	0.59 + 11.643*CL	0.54 + 11.644*CL	0.70 + 11.642*CL
	t_F	772.14	0.82 + 15.426*CL	0.55 + 15.430*CL	0.83 + 15.427*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.60	0.60 + 0.179*SL	0.61 + 0.178*SL	0.60 + 0.178*SL
	t_{PHL}	0.53	0.53 + 0.130*SL	0.54 + 0.129*SL	0.54 + 0.129*SL
	t_R	0.26	0.26 + 0.082*SL	0.25 + 0.086*SL	0.24 + 0.087*SL
	t_F	0.18	0.18 + 0.068*SL	0.17 + 0.071*SL	0.17 + 0.072*SL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to YN	t_{PLH}	0.72	0.72 + 0.178*SL	0.72 + 0.178*SL	0.72 + 0.178*SL
	t_{PHL}	0.60	0.60 + 0.130*SL	0.61 + 0.129*SL	0.61 + 0.129*SL
	t_R	0.25	0.25 + 0.084*SL	0.25 + 0.086*SL	0.24 + 0.087*SL
	t_F	0.18	0.18 + 0.069*SL	0.17 + 0.071*SL	0.17 + 0.072*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCK26 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	26.32	0.43 + 0.518*CL	0.42 + 0.518*CL	0.43 + 0.518*CL
	t_{PHL}	35.38	0.46 + 0.698*CL	0.46 + 0.698*CL	0.46 + 0.698*CL
	t_R	58.61	0.39 + 1.164*CL	0.40 + 1.164*CL	0.37 + 1.165*CL
	t_F	77.67	0.54 + 1.543*CL	0.51 + 1.543*CL	0.54 + 1.543*CL

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to PADY	t_{PLH}	26.40	0.50 + 0.518*CL	0.50 + 0.518*CL	0.51 + 0.518*CL
	t_{PHL}	35.48	0.56 + 0.698*CL	0.56 + 0.698*CL	0.56 + 0.698*CL
	t_R	58.61	0.39 + 1.164*CL	0.40 + 1.164*CL	0.37 + 1.165*CL
	t_F	77.67	0.52 + 1.543*CL	0.59 + 1.542*CL	0.53 + 1.543*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.54	0.54 + 0.022*SL	0.54 + 0.021*SL	0.55 + 0.020*SL
	t_{PHL}	0.46	0.46 + 0.015*SL	0.46 + 0.014*SL	0.47 + 0.013*SL
	t_R	0.20	0.20 + 0.008*SL	0.20 + 0.009*SL	0.19 + 0.010*SL
	t_F	0.14	0.14 + 0.007*SL	0.14 + 0.007*SL	0.13 + 0.008*SL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to YN	t_{PLH}	0.66	0.66 + 0.020*SL	0.66 + 0.020*SL	0.66 + 0.020*SL
	t_{PHL}	0.54	0.54 + 0.015*SL	0.54 + 0.014*SL	0.54 + 0.013*SL
	t_R	0.18	0.18 + 0.009*SL	0.18 + 0.010*SL	0.18 + 0.010*SL
	t_F	0.13	0.13 + 0.007*SL	0.13 + 0.007*SL	0.13 + 0.008*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCK16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	259.38	0.46 + 5.178*CL	0.49 + 5.178*CL	0.44 + 5.179*CL
	t_{PHL}	349.70	0.50 + 6.984*CL	0.50 + 6.984*CL	0.50 + 6.984*CL
	t_R	582.75	0.55 + 11.644*CL	0.62 + 11.643*CL	0.77 + 11.641*CL
	t_F	772.14	0.82 + 15.426*CL	0.55 + 15.430*CL	0.83 + 15.427*CL

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to PADY	t_{PLH}	259.45	0.53 + 5.178*CL	0.48 + 5.179*CL	0.57 + 5.178*CL
	t_{PHL}	349.81	0.61 + 6.984*CL	0.61 + 6.984*CL	0.61 + 6.984*CL
	t_R	582.75	0.59 + 11.643*CL	0.54 + 11.644*CL	0.70 + 11.642*CL
	t_F	772.14	0.82 + 15.426*CL	0.55 + 15.430*CL	0.83 + 15.427*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.60	0.60 + 0.179*SL	0.61 + 0.178*SL	0.60 + 0.178*SL
	t_{PHL}	0.53	0.53 + 0.130*SL	0.54 + 0.129*SL	0.54 + 0.129*SL
	t_R	0.26	0.26 + 0.082*SL	0.25 + 0.086*SL	0.24 + 0.087*SL
	t_F	0.18	0.18 + 0.068*SL	0.17 + 0.071*SL	0.17 + 0.072*SL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to YN	t_{PLH}	0.72	0.72 + 0.178*SL	0.72 + 0.178*SL	0.72 + 0.178*SL
	t_{PHL}	0.60	0.60 + 0.130*SL	0.61 + 0.129*SL	0.61 + 0.129*SL
	t_R	0.25	0.25 + 0.084*SL	0.25 + 0.086*SL	0.24 + 0.087*SL
	t_F	0.18	0.18 + 0.069*SL	0.17 + 0.071*SL	0.17 + 0.072*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCK26 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	26.32	0.43 + 0.518*CL	0.42 + 0.518*CL	0.43 + 0.518*CL
	t_{PHL}	35.38	0.46 + 0.698*CL	0.46 + 0.698*CL	0.46 + 0.698*CL
	t_R	58.61	0.39 + 1.164*CL	0.40 + 1.164*CL	0.37 + 1.165*CL
	t_F	77.67	0.54 + 1.543*CL	0.51 + 1.543*CL	0.54 + 1.543*CL

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to PADY	t_{PLH}	26.40	0.50 + 0.518*CL	0.50 + 0.518*CL	0.51 + 0.518*CL
	t_{PHL}	35.48	0.56 + 0.698*CL	0.56 + 0.698*CL	0.56 + 0.698*CL
	t_R	58.61	0.39 + 1.164*CL	0.40 + 1.164*CL	0.37 + 1.165*CL
	t_F	77.67	0.52 + 1.543*CL	0.59 + 1.542*CL	0.53 + 1.543*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.54	0.54 + 0.022*SL	0.54 + 0.021*SL	0.55 + 0.020*SL
	t_{PHL}	0.46	0.46 + 0.015*SL	0.46 + 0.014*SL	0.47 + 0.013*SL
	t_R	0.20	0.20 + 0.008*SL	0.20 + 0.009*SL	0.19 + 0.010*SL
	t_F	0.14	0.14 + 0.007*SL	0.14 + 0.007*SL	0.13 + 0.008*SL

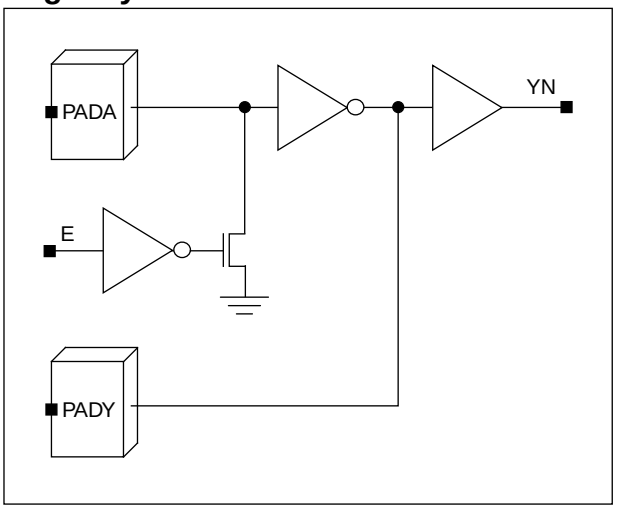
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to YN	t_{PLH}	0.66	0.66 + 0.020*SL	0.66 + 0.020*SL	0.66 + 0.020*SL
	t_{PHL}	0.54	0.54 + 0.015*SL	0.54 + 0.014*SL	0.54 + 0.013*SL
	t_R	0.18	0.18 + 0.009*SL	0.18 + 0.010*SL	0.18 + 0.010*SL
	t_F	0.13	0.13 + 0.007*SL	0.13 + 0.007*SL	0.13 + 0.008*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

PSOSCM(1/2/3/4/5/6)

Oscillator Cell with Enable

Logic Symbol



Truth Table

SEC Tester Standard

PADA	E	PADY	YN
0	0	1	1
0	1	1	1
1	0	x	x
1	1	0	0

Real Application

PADA	E	PADY	YN
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

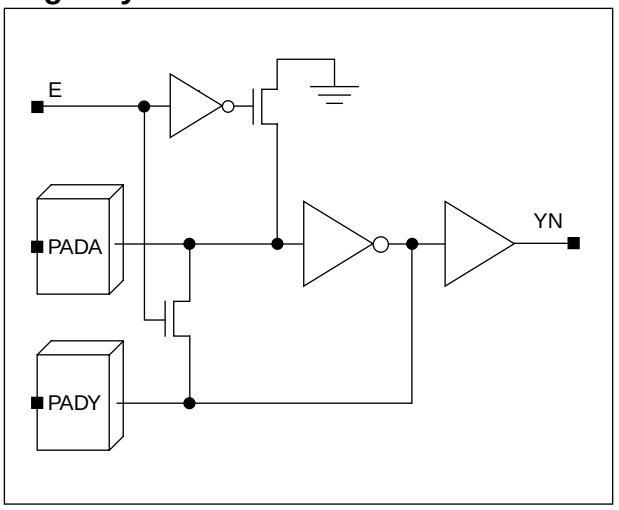
Cell Data

Input Load (SL)	I/O Slots
PSOSCM(1/2/3/4/5/6)	*PSOSCM(1/2/3/4/5/6)*
E	
2.6	2.0

PSOSCM(16/26/36/46/56/66)

Oscillator Cell with Enable and Resistor

Logic Symbol



Truth Table

SEC Tester Standard

PADA	E	PADY	YN
0	0	1	1
0	1	1	1
1	0	x	x
1	1	0	0

Real Application

PADA	E	PADY	YN
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

Cell Data

Input Load (SL)	I/O Slots
PSOSCM (16/26/36/46/56/66)	*PSOSCM (16/26/36/46/56/66)*
E	
2.6	2.0

STD80 PSOSCM1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.24 + 0.004*SL	0.24 + 0.003*SL
	t_R	0.10	0.10 + 0.001*SL	0.09 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCM2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.24 + 0.004*SL	0.24 + 0.003*SL
	t_R	0.10	0.10 + 0.001*SL	0.09 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCM3 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	1.41	0.12 + 0.026*CL	0.12 + 0.026*CL	0.12 + 0.026*CL
	t_{PHL}	1.87	0.12 + 0.035*CL	0.12 + 0.035*CL	0.12 + 0.035*CL
	t_R	3.00	0.10 + 0.058*CL	0.09 + 0.058*CL	0.09 + 0.058*CL
	t_F	3.96	0.11 + 0.077*CL	0.11 + 0.077*CL	0.10 + 0.077*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.19	0.19 + 0.003*SL	0.19 + 0.003*SL	0.20 + 0.002*SL
	t_{PHL}	0.21	0.21 + 0.002*SL	0.21 + 0.003*SL	0.21 + 0.003*SL
	t_R	0.10	0.10 + 0.002*SL	0.10 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.08	0.08 + 0.004*SL	0.09 + 0.001*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCM4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.76	0.12 + 0.013*CL	0.12 + 0.013*CL	0.12 + 0.013*CL
	t_{PHL}	0.99	0.12 + 0.017*CL	0.11 + 0.017*CL	0.12 + 0.017*CL
	t_R	1.54	0.10 + 0.029*CL	0.09 + 0.029*CL	0.09 + 0.029*CL
	t_F	2.02	0.10 + 0.038*CL	0.10 + 0.038*CL	0.10 + 0.038*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.001*SL	0.23 + 0.002*SL	0.23 + 0.001*SL
	t_R	0.11	0.11 + 0.000*SL	0.11 + 0.000*SL	0.10 + 0.001*SL
	t_F	0.09	0.09 + 0.001*SL	0.09 + 0.001*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCM5 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.55	0.11 + 0.009*CL	0.11 + 0.009*CL	0.12 + 0.009*CL
	t_{PHL}	0.70	0.12 + 0.012*CL	0.12 + 0.012*CL	0.11 + 0.012*CL
	t_R	1.06	0.10 + 0.019*CL	0.09 + 0.019*CL	0.09 + 0.019*CL
	t_F	1.38	0.10 + 0.025*CL	0.10 + 0.026*CL	0.09 + 0.026*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.001*SL	0.23 + 0.001*SL	0.23 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.000*SL	0.10 + 0.001*SL
	t_F	0.10	0.10 + 0.001*SL	0.10 + 0.000*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCM6 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.44	0.11 + 0.007*CL	0.11 + 0.007*CL	0.12 + 0.006*CL
	t_{PHL}	0.55	0.11 + 0.009*CL	0.12 + 0.009*CL	0.11 + 0.009*CL
	t_R	0.82	0.11 + 0.014*CL	0.11 + 0.014*CL	0.09 + 0.014*CL
	t_F	1.06	0.11 + 0.019*CL	0.10 + 0.019*CL	0.10 + 0.019*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.25	0.25 + 0.001*SL	0.25 + 0.001*SL	0.25 + 0.001*SL
	t_{PHL}	0.26	0.26 + 0.001*SL	0.26 + 0.001*SL	0.26 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.001*SL	0.11 + 0.001*SL
	t_F	0.11	0.11 + 0.000*SL	0.11 + 0.001*SL	0.10 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCM1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.24 + 0.004*SL	0.24 + 0.003*SL
	t_R	0.10	0.10 + 0.001*SL	0.09 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCM2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.24 + 0.004*SL	0.24 + 0.003*SL
	t_R	0.10	0.10 + 0.001*SL	0.09 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCM3 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	1.41	0.12 + 0.026*CL	0.12 + 0.026*CL	0.12 + 0.026*CL
	t_{PHL}	1.87	0.12 + 0.035*CL	0.12 + 0.035*CL	0.12 + 0.035*CL
	t_R	3.00	0.10 + 0.058*CL	0.09 + 0.058*CL	0.09 + 0.058*CL
	t_F	3.96	0.11 + 0.077*CL	0.11 + 0.077*CL	0.10 + 0.077*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.19	0.19 + 0.003*SL	0.19 + 0.003*SL	0.20 + 0.002*SL
	t_{PHL}	0.21	0.21 + 0.002*SL	0.21 + 0.003*SL	0.21 + 0.003*SL
	t_R	0.10	0.10 + 0.002*SL	0.10 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.08	0.08 + 0.004*SL	0.09 + 0.001*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCM4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.76	0.12 + 0.013*CL	0.12 + 0.013*CL	0.12 + 0.013*CL
	t_{PHL}	0.99	0.12 + 0.017*CL	0.11 + 0.017*CL	0.12 + 0.017*CL
	t_R	1.54	0.10 + 0.029*CL	0.09 + 0.029*CL	0.09 + 0.029*CL
	t_F	2.02	0.10 + 0.038*CL	0.10 + 0.038*CL	0.10 + 0.038*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.001*SL	0.23 + 0.002*SL	0.23 + 0.001*SL
	t_R	0.11	0.11 + 0.000*SL	0.11 + 0.000*SL	0.10 + 0.001*SL
	t_F	0.09	0.09 + 0.001*SL	0.09 + 0.001*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCM5 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.55	0.11 + 0.009*CL	0.11 + 0.009*CL	0.12 + 0.009*CL
	t_{PHL}	0.70	0.12 + 0.012*CL	0.12 + 0.012*CL	0.11 + 0.012*CL
	t_R	1.06	0.10 + 0.019*CL	0.09 + 0.019*CL	0.09 + 0.019*CL
	t_F	1.38	0.10 + 0.025*CL	0.10 + 0.026*CL	0.09 + 0.026*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.001*SL	0.23 + 0.001*SL	0.23 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.000*SL	0.10 + 0.001*SL
	t_F	0.10	0.10 + 0.001*SL	0.10 + 0.000*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCM6 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.44	0.11 + 0.007*CL	0.11 + 0.007*CL	0.12 + 0.006*CL
	t_{PHL}	0.55	0.11 + 0.009*CL	0.12 + 0.009*CL	0.11 + 0.009*CL
	t_R	0.82	0.11 + 0.014*CL	0.11 + 0.014*CL	0.09 + 0.014*CL
	t_F	1.06	0.11 + 0.019*CL	0.10 + 0.019*CL	0.10 + 0.019*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.25	0.25 + 0.001*SL	0.25 + 0.001*SL	0.25 + 0.001*SL
	t_{PHL}	0.26	0.26 + 0.001*SL	0.26 + 0.001*SL	0.26 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.001*SL	0.11 + 0.001*SL
	t_F	0.11	0.11 + 0.000*SL	0.11 + 0.001*SL	0.10 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCM16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.24 + 0.004*SL	0.24 + 0.003*SL
	t_R	0.10	0.10 + 0.001*SL	0.09 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCM26 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.24 + 0.004*SL	0.24 + 0.003*SL
	t_R	0.10	0.10 + 0.001*SL	0.09 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCM36 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	1.41	0.12 + 0.026*CL	0.12 + 0.026*CL	0.12 + 0.026*CL
	t_{PHL}	1.87	0.12 + 0.035*CL	0.12 + 0.035*CL	0.12 + 0.035*CL
	t_R	3.00	0.10 + 0.058*CL	0.09 + 0.058*CL	0.09 + 0.058*CL
	t_F	3.96	0.11 + 0.077*CL	0.11 + 0.077*CL	0.10 + 0.077*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.19	0.19 + 0.003*SL	0.19 + 0.003*SL	0.20 + 0.002*SL
	t_{PHL}	0.21	0.21 + 0.002*SL	0.21 + 0.003*SL	0.21 + 0.003*SL
	t_R	0.10	0.10 + 0.002*SL	0.10 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.08	0.08 + 0.004*SL	0.09 + 0.001*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCM46 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.76	0.12 + 0.013*CL	0.12 + 0.013*CL	0.12 + 0.013*CL
	t_{PHL}	0.99	0.12 + 0.017*CL	0.11 + 0.017*CL	0.12 + 0.017*CL
	t_R	1.54	0.10 + 0.029*CL	0.09 + 0.029*CL	0.09 + 0.029*CL
	t_F	2.02	0.10 + 0.038*CL	0.10 + 0.038*CL	0.10 + 0.038*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.001*SL	0.23 + 0.002*SL	0.23 + 0.001*SL
	t_R	0.11	0.11 + 0.000*SL	0.11 + 0.000*SL	0.10 + 0.001*SL
	t_F	0.09	0.09 + 0.001*SL	0.09 + 0.001*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCM56 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.55	0.11 + 0.009*CL	0.11 + 0.009*CL	0.12 + 0.009*CL
	t_{PHL}	0.70	0.12 + 0.012*CL	0.12 + 0.012*CL	0.11 + 0.012*CL
	t_R	1.06	0.10 + 0.019*CL	0.09 + 0.019*CL	0.09 + 0.019*CL
	t_F	1.38	0.10 + 0.025*CL	0.10 + 0.026*CL	0.09 + 0.026*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.001*SL	0.23 + 0.001*SL	0.23 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.000*SL	0.10 + 0.001*SL
	t_F	0.10	0.10 + 0.001*SL	0.10 + 0.000*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STD80 PSOSCM66 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.44	0.11 + 0.007*CL	0.11 + 0.007*CL	0.12 + 0.006*CL
	t_{PHL}	0.55	0.11 + 0.009*CL	0.12 + 0.009*CL	0.11 + 0.009*CL
	t_R	0.82	0.11 + 0.014*CL	0.11 + 0.014*CL	0.09 + 0.014*CL
	t_F	1.06	0.11 + 0.019*CL	0.10 + 0.019*CL	0.10 + 0.019*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.25	0.25 + 0.001*SL	0.25 + 0.001*SL	0.25 + 0.001*SL
	t_{PHL}	0.26	0.26 + 0.001*SL	0.26 + 0.001*SL	0.26 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.001*SL	0.11 + 0.001*SL
	t_F	0.11	0.11 + 0.000*SL	0.11 + 0.001*SL	0.10 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCM16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.24 + 0.004*SL	0.24 + 0.003*SL
	t_R	0.10	0.10 + 0.001*SL	0.09 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCM26 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.24 + 0.004*SL	0.24 + 0.003*SL
	t_R	0.10	0.10 + 0.001*SL	0.09 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCM36 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	1.41	0.12 + 0.026*CL	0.12 + 0.026*CL	0.12 + 0.026*CL
	t_{PHL}	1.87	0.12 + 0.035*CL	0.12 + 0.035*CL	0.12 + 0.035*CL
	t_R	3.00	0.10 + 0.058*CL	0.09 + 0.058*CL	0.09 + 0.058*CL
	t_F	3.96	0.11 + 0.077*CL	0.11 + 0.077*CL	0.10 + 0.077*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.19	0.19 + 0.003*SL	0.19 + 0.003*SL	0.20 + 0.002*SL
	t_{PHL}	0.21	0.21 + 0.002*SL	0.21 + 0.003*SL	0.21 + 0.003*SL
	t_R	0.10	0.10 + 0.002*SL	0.10 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.08	0.08 + 0.004*SL	0.09 + 0.001*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCM46 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.76	0.12 + 0.013*CL	0.12 + 0.013*CL	0.12 + 0.013*CL
	t_{PHL}	0.99	0.12 + 0.017*CL	0.11 + 0.017*CL	0.12 + 0.017*CL
	t_R	1.54	0.10 + 0.029*CL	0.09 + 0.029*CL	0.09 + 0.029*CL
	t_F	2.02	0.10 + 0.038*CL	0.10 + 0.038*CL	0.10 + 0.038*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.001*SL	0.23 + 0.002*SL	0.23 + 0.001*SL
	t_R	0.11	0.11 + 0.000*SL	0.11 + 0.000*SL	0.10 + 0.001*SL
	t_F	0.09	0.09 + 0.001*SL	0.09 + 0.001*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCM56 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.55	0.11 + 0.009*CL	0.11 + 0.009*CL	0.12 + 0.009*CL
	t_{PHL}	0.70	0.12 + 0.012*CL	0.12 + 0.012*CL	0.11 + 0.012*CL
	t_R	1.06	0.10 + 0.019*CL	0.09 + 0.019*CL	0.09 + 0.019*CL
	t_F	1.38	0.10 + 0.025*CL	0.10 + 0.026*CL	0.09 + 0.026*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.001*SL	0.23 + 0.001*SL	0.23 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.000*SL	0.10 + 0.001*SL
	t_F	0.10	0.10 + 0.001*SL	0.10 + 0.000*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

STDM80 PSOSCM66 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.44	0.11 + 0.007*CL	0.11 + 0.007*CL	0.12 + 0.006*CL
	t_{PHL}	0.55	0.11 + 0.009*CL	0.12 + 0.009*CL	0.11 + 0.009*CL
	t_R	0.82	0.11 + 0.014*CL	0.11 + 0.014*CL	0.09 + 0.014*CL
	t_F	1.06	0.11 + 0.019*CL	0.10 + 0.019*CL	0.10 + 0.019*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.25	0.25 + 0.001*SL	0.25 + 0.001*SL	0.25 + 0.001*SL
	t_{PHL}	0.26	0.26 + 0.001*SL	0.26 + 0.001*SL	0.26 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.001*SL	0.11 + 0.001*SL
	t_F	0.11	0.11 + 0.000*SL	0.11 + 0.001*SL	0.10 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Overview

PCI buffers are designed for PCI local bus application which is an industry-standard, high-performance 32- or 64-bit bus architecture.

SEC ASIC supports 5V and 3.3V signalling environment PCI bi-directional buffers including a Universal buffer. The Universal buffer requires a select control (EN3V) signal. EN3V pin should be tied to the Voltage Detector output directly.

Features

– High performance
– Low cost
– Easy use
– Longevity: both 5V and 3.3V signalling environments specified.

General Description

The PCI buffer's signalling environment is controlled by EN3V pin which is logically low in a 5V operation and logically high in a 3.3V operation. If you use a Voltage Detector cell with the PCI buffer, you have to connect this EN3V pin to VDET (Voltage Detector) output. Do not use a Level Shifter buffer (PLSCB).

Cell List

Cell Name	Function Description
STD80	
PSIPCIA	5V PCI Input Buffer
PSOPCIA	5V PCI Output Buffer
PLSIPCIA	Internal 5V/External 3.3V PCI Input Buffer
PLSOPCIA	Internal 5V/External 3.3V PCI Output Buffer
PSIPCIAU	Universal PCI Input Buffer
PSOPCIAU	Universal PCI Output Buffer
STDM80	
PSIPCIA3	3.3V PCI Input Buffer
PSOPCIA3	3.3V PCI Output Buffer
PHSIPCIA	Internal 3.3V/External 5V PCI Input Buffer
PHSOPCIA	Internal 3.3V/External 5V PCI Output Buffer
PSIPCIAU	Universal PCI Input Buffer
PSOPCIAU	Universal PCI Output Buffer

Electrical Characteristics

SEC ASIC guarantees PCI buffer's electrical characteristics under all conditions (V_{CC} = 3.6V, Temp. = 0°C ~ V_{CC} = 3.0V, Temp. = 125°C).

5V DC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IL}	Input Low Voltage		–0.5	0.8	
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5		–70	µA
I_{IH}	Input High Leakage Current	V_{IN} = 2.7		70	
V_{OL}	Output Low Voltage	I_{OUT} = 3mA, 6mA		0.55	V
V_{OH}	Output High Voltage	I_{OUT} = –2mA	2.4		
C_{IN}	Input Pin Capacitance			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	
C_{IDSEL}	IDSEL Pin Capacitance			8	
L_{PIN}	Pin Inductance			20	nH

5V AC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
$I_{OH\ (AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4$	–44		mA
		$1.4 < V_{OUT} < 2.4$	–44 (VOUT – 1.4) / 0.024		
		$3.1 < V_{OUT} < V_{CC}$		Eqt'n A[1]	
	(Test Point)	V_{OUT} = 3.1		–142	
$I_{OL\ (AC)}$	Switching Current Low	$V_{OUT} \geq 2.2$	95		
		$2.2 > V_{OUT} > 0.55$	V_{OUT}/0.023		
		$0.71 > V_{OUT} > 0$		Eqt'n B[2]	
	(Test Point)	V_{OUT} = 0.71		206	
I_{CL}	Low Clamp Current	$–5 < V_{IN} \leq –1$	$–25 + (V_{IN} + 1) / 0.015$		
$Slew_R$[3]	Output Rise Slew Rate	0.4V to 2.4V load	1	5	V/ns
$Slew_F$[3]	Output Fall Slew Rate	2.4V to 0.4V load	1	5	

NOTES:

1. **Equation A**: $I_{OH} = 11.9 * (V_{OUT} – 5.25) * (V_{OUT} + 2.45)$ for $V_{CC} > V_{OUT} > 3.1v$
2. **Equation B**: $I_{OL} = 78.5 * V_{OUT} * (4.4 – V_{OUT})$ for $0v < V_{OUT} < 0.71v$
3. The minimum slew rate (slowest signal edge) is guaranteed. The maximum slew rate (fastest signal edge) is a guideline, and rise and fall times faster than the maximum can occur.
   Designers should ensure that signal integrity modelling includes the potential for rise and fall times faster than the maximum shown in the table.

3.3V DC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage		3.0	3.6	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CC}$	V
V_{IH}	Input High Voltage		$0.5V_{CC}$	V_{CC} + 0.5	V
V_{IPU}	Input Pull-Up Voltage		$0.7V_{CC}$		V
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{CC}$		±10	µA
V_{OL}	Output Low Voltage	I_{OUT} = 1500µA		$0.1V_{CC}$	V
V_{OH}	Output High Voltage	I_{OUT} = –500µA	$0.9V_{CC}$		V
C_{IN}	Input Pin Capacitance			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance			8	pF
L_{PIN}	Pin Inductance			20	nH

3.3V AC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$I_{OH (AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{CC}$	$-12V_{CC}$		mA
		$0.3V_{CC} < V_{OUT} < 0.9V_{CC}$	$-17.1 (V_{CC} - V_{OUT})$		mA
		$0.7V_{CC} < V_{OUT} < V_{CC}$		Eqt'n C[1]	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$		$-32V_{CC}$	mA
$I_{OL (AC)}$	Switching Current Low	$V_{CC} > V_{OUT} \ge 0.6V_{CC}$	$16V_{CC}$		mA
		$0.6V_{CC} > V_{OUT} > 0.1V_{CC}$	$26.7V_{OUT}$		mA
		$0.18V_{CC} > V_{OUT} > 0$		Eqt'n D[2]	
	(Test Point)	$V_{OUT} = 0.18V_{CC}$		$38V_{CC}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1) / 0.015$		mA
I_{CH}	High Clamp Current	$V_{CC} + 4 > V_{IN} \ge V_{CC} + 1$	$25 + (V_{IN} - V_{CC} - 1) / 0.015$		mA
$Slew_R$[3]	Output Rise Slew Rate	$0.2V_{CC}$ to $0.6V_{CC}$ load	1	4	V/ns
$Slew_F$[3]	Output Fall Slew Rate	$0.6V_{CC}$ to $0.2V_{CC}$ load	1	4	V/ns

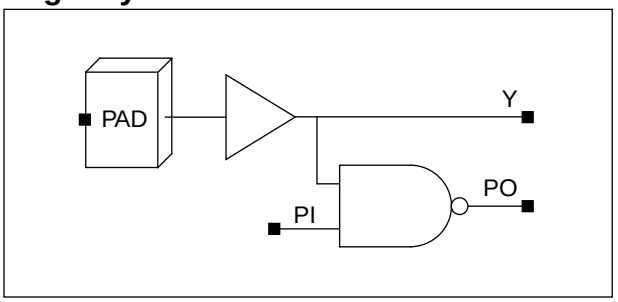
NOTES:

1. **Equation C**: $I_{OH} = (98.0 / V_{CC}) * (V_{OUT} - V_{CC}) * (V_{OUT} + 0.4V_{CC})$ for $V_{CC} > V_{OUT} > 0.7v$
2. **Equation D**: $I_{OL} = (256 / V_{CC}) * V_{OUT} * (V_{CC} - V_{OUT})$ for $0v < V_{OUT} < 0.18V_{CC}$
3. The minimum slew rate (slowest signal edge) is guaranteed. The maximum slew rate (fastest signal edge) is a guideline, and rise and fall times faster than the maximum can occur.
   Designers should ensure that signal integrity modelling includes the potential for rise and fall times faster than the maximum shown in the table.

PSIPCIA/PLSIPCIA/PSIPCIA3/PHSIPCIA

PCI Input Buffers

Logic Symbol



Input Load (SL)

STD80				
	TN	EN	A	PI
PSIPCIA/PLSIPCIA	1.0	1.6	3.6	1.0
STDM80				
	TN	EN	A	PI
PSIPCIA3/PHSIPCIA	1.0	1.6	3.6	1.0

Truth Table

Input Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

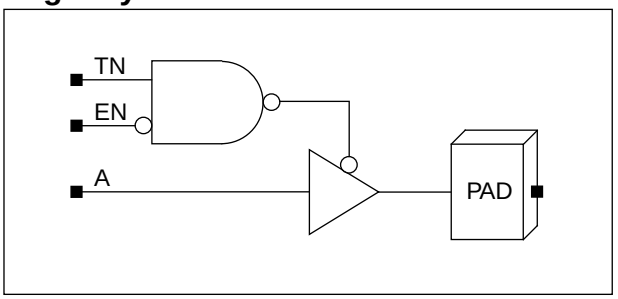
Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

I/O Slot

STD80/STDM80	
PSIPCIA/PLSIPCIA PSIPCIA3/PHSIPCIA	1.0

Logic Symbol



Input Load (SL)

STD80				
	TN	EN	A	PI
PSOPCIA/PLSOPCIA	1.0	1.6	3.6	1.0
STDM80				
	TN	EN	A	PI
PSOPCIA3/PHSOPCIA	1.0	1.6	3.6	1.0

Truth Table

Input Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

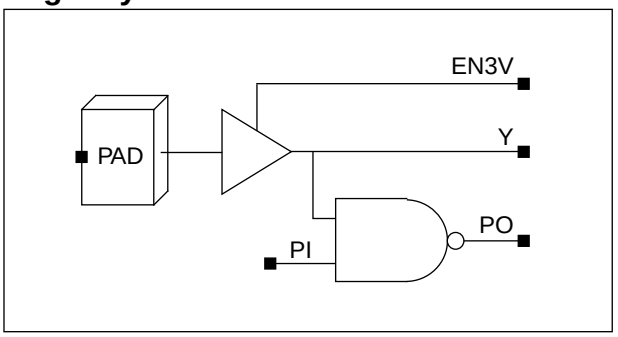
I/O Slot

STD80/STDM80	
PSOPCIA/PLSOPCIA PSOPCIA3/PHSOPCIA	1.0

PSIPCIAU

Universal PCI Input Buffer

Logic Symbol



Input Load (SL)

STD80/STDM80				
	TN	EN	A	PI
PSIPCIAU	1.0	1.6	3.6	1.0

Truth Table

Input Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Output Truth Table

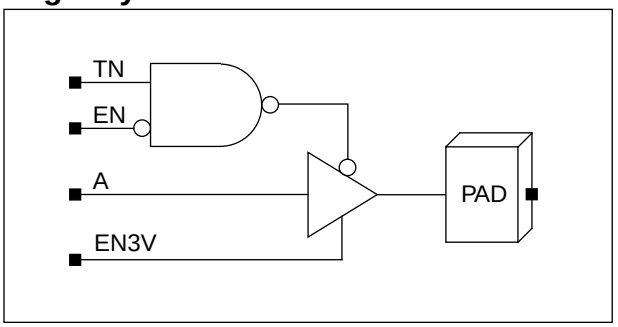
A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

* EN3V (active-high) enables the 3.3V mode.

I/O Slot

STD80/STDM80	
PSIPCIAU	1.0

Logic Symbol



Input Load (SL)

STD80/STDM80				
	TN	EN	A	PI
PSOPCIAU	1.0	1.6	3.6	1.0

Truth Table

Input Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

* EN3V (active-high) enables the 3.3V mode.

I/O Slot

STD80/STDM80	
PSOPCIAU	1.0

PCMCIA BUFFERS

Overview

PC card technology is used in a wide variety of products including notebook computers, palmtop computers, pen computers, desktop computers, printers, telephones, medical instruments and others embedded application hosts.

For PCMCIA interface, SEC ASIC supports various kinds of PCMCIA buffers.
These PCMCIA buffers enable you to

– Maintain interface conditions and speed independent of Battery Voltage
– Allow groups of card interface input buffers to be powered down
– Use a Voltage Detector cell
– Select pull-up/pull-down option (50K/100K/200K, default = 100K).

General Description

All of PCMCIA buffers are controlled by S3V5V signal that is logically low in a 5V operation and logically high in a 3.3V operation. If you use a Voltage Detector cell with a PCMCIA buffer, you have to connect the S3V5V pin to VDET (Voltage Detector) output.

Logic Levels

Parameter	Min	Max
V_{IH}	2.0V	
V_{IL}		0.8V
V_{OH}	2.4V	
V_{OL}		0.5V

NOTES:

1. PCMCIA input buffer is TTL compatible.
2. PCMCIA output buffer has a balanced T_R & T_F.

Cell List

Cell Name	Function Description
STD80/STDM80	
PVIC(5/3)	5V/3.3V CMOS Level PCMCIA Input Buffers
PVIL(5/3)	5V/3.3V TTL Schmitt Trigger Level PCMCIA Input Buffers
PVILD(5/3)	5V/3.3V TTL Schmitt Trigger Level PCMCIA Input Buffers with Pull-Down
PVILU(5/3)	5V/3.3V TTL Schmitt Trigger Level PCMCIA Input Buffers with Pull-Up
PVIT(5/3)	5V/3.3V TTL Level PCMCIA Input Buffers
PVITD(5/3)	5V/3.3V TTL Level PCMCIA Input Buffers with Pull-Down
PVITU(5/3)	5V/3.3V TTL Level PCMCIA Input Buffers with Pull-Up
PVOB4(5/3)	5V/3.3V 4mA PCMCIA Output Buffers without SRC
PVOB8(5/3)	5V/3.3V 8mA PCMCIA Output Buffers without SRC
PVOB12(5/3)	5V/3.3V 12mA PCMCIA Output Buffers without SRC
PVOD4(5/3)	5V/3.3V 4mA Open-Drain PCMCIA Output Buffers without SRC
PVOD8(5/3)	5V/3.3V 8mA Open-Drain PCMCIA Output Buffers without SRC
PVOD12(5/3)	5V/3.3V 12mA Open-Drain PCMCIA Output Buffers without SRC
PVOT4(5/3)	5V/3.3V 4mA Tri-State PCMCIA Output Buffers without SRC
PVOT8(5/3)	5V/3.3V 8mA Tri-State PCMCIA Output Buffers without SRC
PVOT12(5/3)	5V/3.3V 12mA Tri-State PCMCIA Output Buffers without SRC
PVOT8SM(5/3)	5V/3.3V 8mA Tri-State PCMCIA Output Buffers with SRC
PVOT12SM(5/3)	5V/3.3V 12mA Tri-State PCMCIA Output Buffers with SRC
PVBTT4(5/3)	5V/3.3V 4mA PCMCIA Bi-Directional Buffers without SRC
PVBTT8(5/3)	5V/3.3V 8mA PCMCIA Bi-Directional Buffers without SRC
PVBTT12(5/3)	5V/3.3V 12mA PCMCIA Bi-Directional Buffers without SRC
PVBTDT8SM(5/3)	5V/3.3V 8mA PCMCIA Bi-Directional Buffers with SRC, Pull-Down
PVBCT8SM(5/3)	5V/3.3V 8mA PCMCIA Bi-Directional Buffers with SRC

PCMCIA BUFFERS

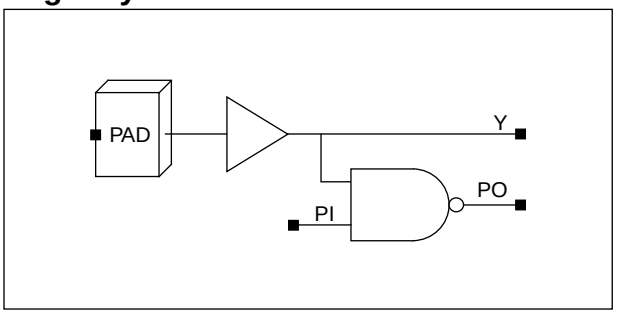
Naming Conventions

PCMCIA Input Buffers (PVI a b v)			
PCMCIA Output Buffers (PVO x y z v)			
PCMCIA Bi-Directional Buffers (PVB a b x y z v)			
a		**b**	
C	CMOS level	None	No resistor
L	TTL Schmitt trigger level	D	Pull-down resistor
S	CMOS Schmitt trigger level	U	Pull-up resistor
T	TTL level	**y**	
x		4	4mA drive
B	Normal buffer	8	8mA drive
D	Open-drain buffer	12	12mA drive
T	Tri-state buffer	**v**	
z		5	5V
None	No slew-rate control (fastest)	3	3.3V
SM	Medium slew-rate control		
SH	High slew-rate control		

PVIC(5/3)

CMOS Level PCMCIA Input Buffers

Logic Symbol



Pin Connection

Input	Output
PAD	Y
PI	PO

Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

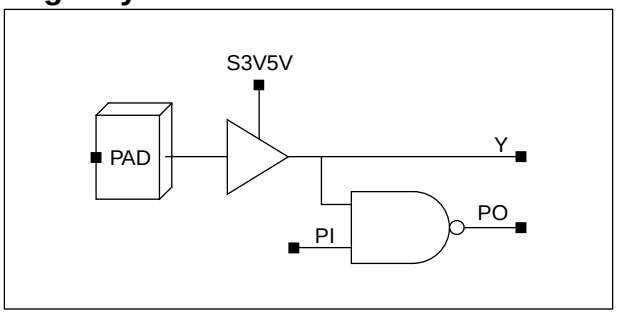
Cell Availability

5V Operation	3.3V Operation
PVIC5	PVIC3

PVIL(D/U)(5/3)/PVIT(D/U)(5/3)

TTL Level PCMCIA Input Buffers

Logic Symbol



Pin Connection

Input	Output
PAD	Y
PI	PO
S3V5V	

Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

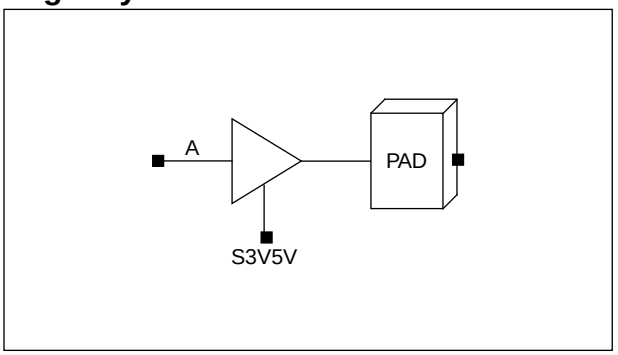
Cell Availability

5V Operation	3.3V Operation
PVIL5	PVIL3
PVILD5	PVILD3
PVILU5	PVILU3
PVIT5	PVIT3
PVITD5	PVITD3
PVITU5	PVITU3

PVOB(4/8/12)(5/3)

PCMCIA Output Buffers

Logic Symbol



Pin Connection

Input	Output
A S3V5V	PAD

Truth Table

A	PAD
0	0
1	1

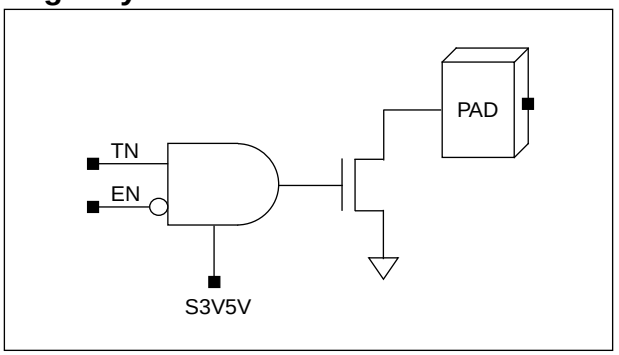
Cell Availability

5V Operation	3.3V Operation
PVOB45	PVOB43
PVOB85	PVOB83
PVOB125	PVOB123

PVOD(4/8/12)(5/3)

Open Drain PCMCIA Output Buffers

Logic Symbol



Pin Connection

Input	Output
TN EN S3V5V	PAD

Truth Table

TN	EN	PAD
1	0	0
0	x	Hi-Z
x	1	Hi-Z

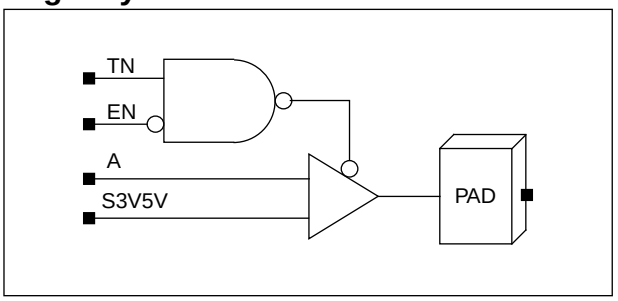
Cell Availability

5V Operation	3.3V Operation
PVOD45	PVOD43
PVOD85	PVOD83
PVOD125	PVOD123

PVOT(4/8/12)(5/3)

Tri-State PCMCIA Output Buffers

Logic Symbol



Pin Connection

Input	Output
TN	PAD
EN	
A	
S3V5V	

Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi-Z
0	x	x	Hi-Z

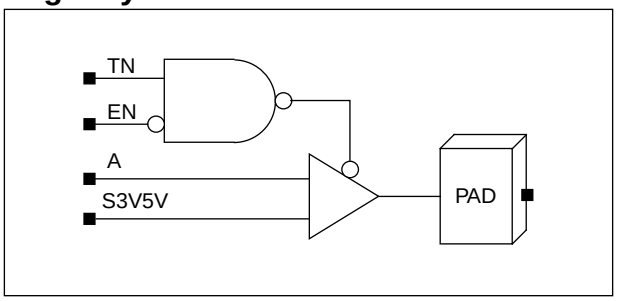
Cell Availability

5V Operation	3.3V Operation
PVOT45	PVOT43
PVOT85	PVOT83
PVOT125	PVOT123

PVOT(8/12)SM(5/3)

Tri-State PCMCIA Output Buffers

Logic Symbol



Pin Connection

Input	Output
TN	PAD
EN	
A	
S3V5V	

Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi-Z
0	x	x	Hi-Z

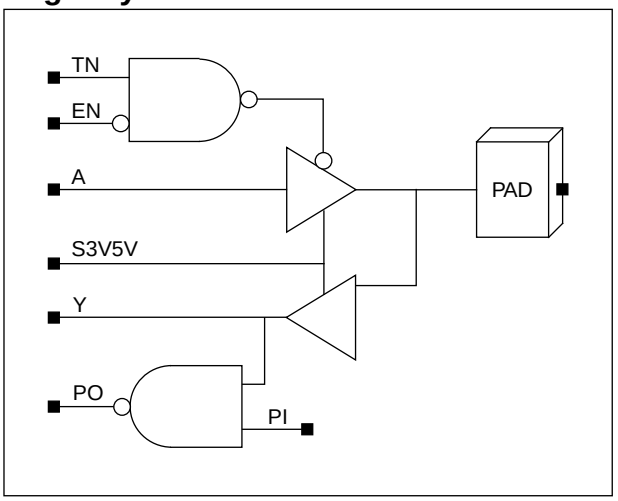
Cell Availability

5V Operation	3.3V Operation
PVOT8SM5	PVOT8SM3
PVOT12SM5	PVOT12SM3

PVBTT(4/8/12)(5/3)

PCMCIA Bi-Directional Buffers

Logic Symbol



Pin Connection

Input	Output
TN	PAD
EN	Y
A	PO
S3V5V	
PI	

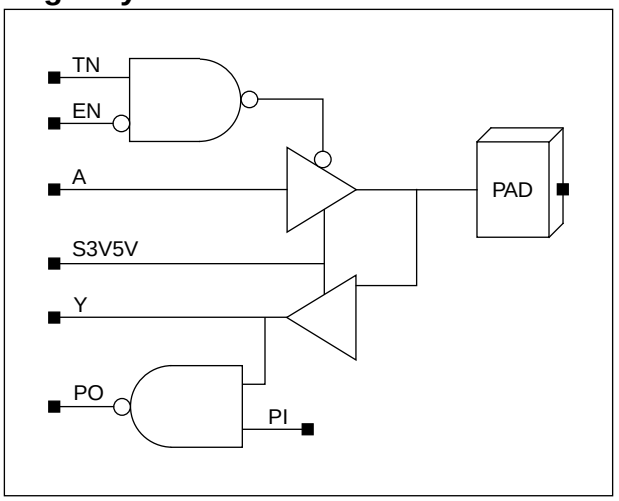
Cell Availability

5V Operation	3.3V Operation
PVBTT45	PVBTT43
PVBTT85	PVBTT83
PVBTT125	PVBTT123

PVBTDT8SM/PVBCT8SM(5/3)

PCMCIA Bi-Directional Buffers

Logic Symbol



Pin Connection

Input	Output
TN	PAD
EN	Y
A	PO
S3V5V	
PI	

Cell Availability

5V Operation	3.3V Operation
PVBTDT8SM5	PVBTDT8SM3
PVBCT8SM5	PVBCT8SM3

Overview

CardBus I/O buffers have 3.3V operation, 32-bit bus width and 33MHz of transmission speed. The latest version of the PC card standard adds information to improve compatibility with the standard by requiring a Card Information Structure (CIS) on every PC card.

The standard has also been enhanced to support the following optional features:

– Low-Voltage Only Operation (3.3V)
– Hardware Direct Memory Access (DMA)
– Multiple-Function Cards
– Industry Standard Power Management Interface (APM)
– High Throughput 32-Bit Bus Mastering Interface (CardBus)

SEC ASIC supports nine different CardBus I/O buffers. If necessary, a Voltage Detector cell can be used with them. For maximum flexibility, CardBus I/O buffers have not only a Level Shifter but also a pull-up enable control pin.

CardBus I/O buffers have only 3.3V electrical specifications, however, we can support 5V/3.3V flexible operation by using of a level shifter. Regardless of the I/O voltage, S3V5V pin controls the same input level and output driving current. S3V5V pin should be tied to the voltage detector in a mixed system, or ground in a 3.3V-only system.

We can not attribute a level shifter to PUEN (Pull-Up Enable) pin, because we have only four level shifters. In order to control the PUEN pin with an internal signal, you should use the level shifter butter (PLSCB) in a mixed system.

For minimizing power consumption, CardBus I/O buffers have a nand type input with a control pin. Therefore, the input buffers operate as active-high input buffers. However, if the control pin is in low state, the output Y is low and not tri-state.

General Description

The CardBus I/O buffer is controlled by S3V5V signal that is logically low in a 5V operation and logically high in a 3.3V operation. If you use a voltage detector cell with the CardBus I/O buffer, you have to connect this S3V5V pin to VDET (voltage detector) output. Do not use a level shifter buffer (PLSCB).

CSTSCHG Buffer Specification

The CSTSCHG pin can be used by the CardBus PC card to remotely power up the system. The design of the CardBus PC card's output buffer and the system's input buffer must ensure no electrical damage results.

– An output buffer for CSTSCHG pin never exceed 1mA.
– An input buffer for CSTSCHG pin is able to withstand sustained forward bias current of 1mA.

CCLK Specification

The electrical characteristics of CCLK follows 3.3V signalling of PCI Local bus specification Revision 2.1. Refer to the PCI buffer electrical characteristics.

CARDBUS I/O BUFFERS

Cell List

Cell Name	Function Description
STD80	
PLITCBU	3.3V Interface Universal TTL CardBus Input Buffer with Pull-Up
PLOTCBU	3.3V Interface Tri-State CardBus Output Buffer with Pull-Up
PLOTCCKCBU	3.3V Interface Tri-State CardBus Output Clock Driver with Pull-Up
PLOTCVSCBU	3.3V Interface Tri-State Output Card Voltage Sense with Pull-Up
PLODCCKCBU	3.3V Interface Open Drain CardBus Output Clock Driver with Pull-Up
PLBTTCBU	3.3V Interface Tri-State CardBus Bi-Directional Buffer with Pull-Up
PLBTCCKCBU	3.3V Interface CardBus Bi-Directional Clock Driver with Pull-Up
PLBTCVSCBU	3.3V Interface Tri-State Bi-Directional Card Voltage Sense with Pull-Up
PLBDCCKCBU	3.3V Interface Open Drain CardBus Bi-Directional Clock Driver with Pull-Up
PLSCB	3.3V Interface Level Shifter Buffer
STDM80	
PITCBU	Universal TTL CardBus Input Buffer with Pull-Up
POTCBU	Tri-State CardBus Output Buffer with Pull-Up
POTCCKCBU	Tri-State CardBus Output Clock Driver with Pull-Up
POTCVSCBU	Tri-State Output Card Voltage Sense with Pull-Up
PODCCKCBU	Open Drain CardBus Output Clock Driver with Pull-Up
PBTTCBU	Tri-State CardBus Bi-Directional Buffer with Pull-Up
PBTCCKCBU	CardBus Bi-Directional Clock Driver with Pull-Up
PBTCVSCBU	Tri-State Bi-Directional Card Voltage Sense with Pull-Up
PBDCCKCBU	Open Drain CardBus Bi-Directional Clock Driver with Pull-Up
PLSCB	Level Shifter Buffer

Electrical Characteristics
(Normal CardBus interface type buffers)

3.3V DC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage		3.0	3.6	V
V_{IH}	Input High Voltage		$0.475V_{CC}$	V_{CC} + 0.5	
V_{IL}	Input Low Voltage		–0.5	$0.325V_{CC}$	
V_{OH}	Output High Voltage	I_{OUT} = –150µA	$0.9V_{CC}$		
V_{OL}	Output Low Voltage	I_{OUT} = 700µA		$0.1V_{CC}$	
I_{CC}[1]	Supply Current			1	A
I_{IL}[2]	Input Leakage Current	$0 < V_{IN} < V_{CC}$		±10	µA

NOTES:

1. This is determined solely by the maximum current capacity of the V_{CC} pins on the connector.
2. Input leakage currents include High-Z output leakage for all bi-directional buffers with High-Z outputs. CCD1#, CCD2#, CVS1 and CVS2 do not have to meet leakage requirements.

3.3V AC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
t_{RCB}[1]	Output Rise Time	$0.2V_{CC} – 0.6V_{CC}$	0.25	1.0	V/ns
t_{FCB}[1]	Output Fall Time	$0.6V_{CC} – 0.2V_{CC}$	0.25	1.0	
I_{CL}	Low Clamp Current	$–3 < V_{IN} < –1$	$–25 + (V_{IN} + 1) / 0.015$		mA
I_{CH}	High Clamp Current	$V_{CC} + 4 > V_{IN} > V_{CC} + 1$	$25 + (V_{IN} – V_{CC} – 1) / 0.015$		

NOTE:

1. This does not apply to **CCLK**. Minimum and maximum rates are measured with the minimum capacitive load a driver will see (7pF). The values ensure the fastest edge rate will not switch rail-to-rail faster than 3.6ns.

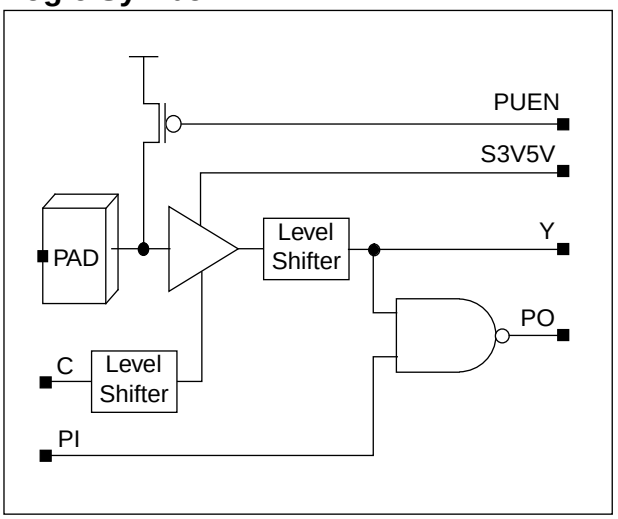
PvITCBU

Universal TTL CardBus Input Buffer with Pull-Up

Cell Availability

Library	5V Operation	3.3V Operation
STD80	–	PLITCBU
STDM80	–	PITCBU

Logic Symbol



Truth Table

PAD	C	PI	Y	PO
1	1	1	1	0
0	1	x	0	1
1	1	0	1	1
x	0	x	0	1

* PUEN (Pull-up control pin) is low enable.

Cell Data

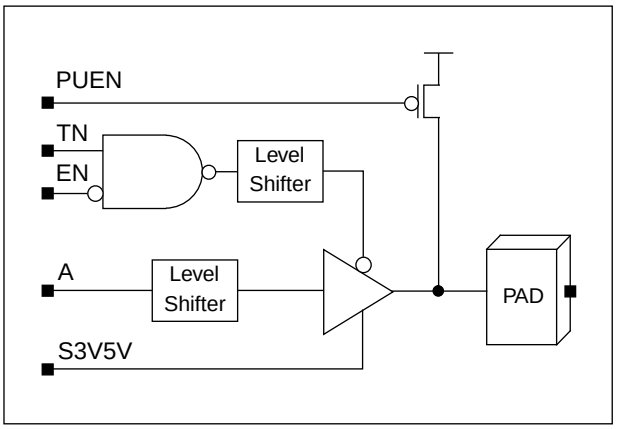
Input Load (SL)		I/O Slot
C	PI	
4.0	1.6	1.0

Cell Availability

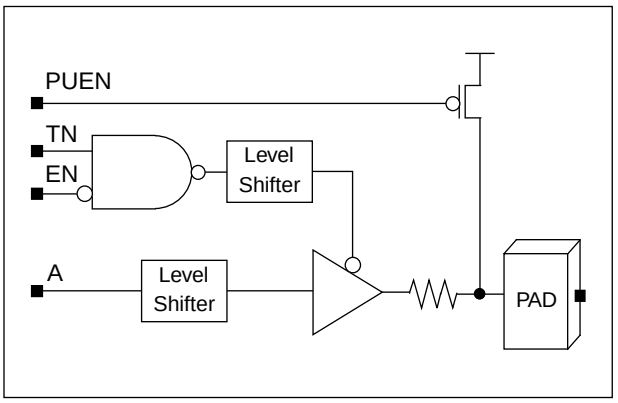
Library	5V Operation	3.3V Operation
STD80	–	PLOTCBU/PLOTCCKCBU/PLOTCVSCBU
STDM80	–	POTCBU/POTCCKCBU/POTCVSCBU

Logic Symbol

PLOTCBU/PLOTCCKCBU



PLOTCVSCBU



Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

* PUEN (Pull-up control pin) is low enable.

Cell Data

Input Load (SL)				I/O Slot
A	EN	TN	PUEN	
2.3	1.2	1.2	0.5	1.0

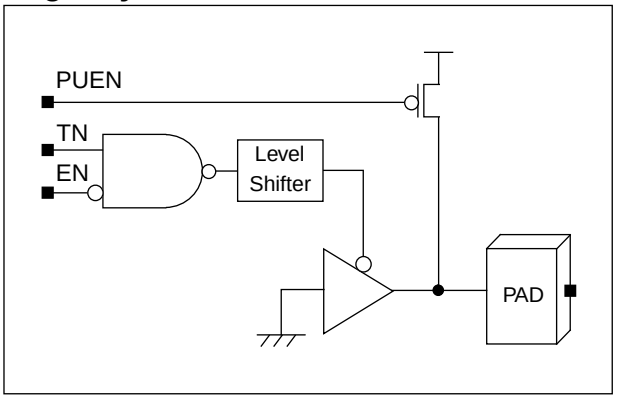
PvODCCKCBU

Open Drain CardBus Output Clock Driver with Pull-Up

Cell Availability

Library	5V Operation	3.3V Operation
STD80	–	PLODCCKCBU
STDM80	–	PODCCKCBU

Logic Symbol



Truth Table

EN	TN	PAD
0	1	0
1	x	Hi-Z
x	0	Hi-Z

* PUEN (Pull-up control pin) is low enable.

Cell Data

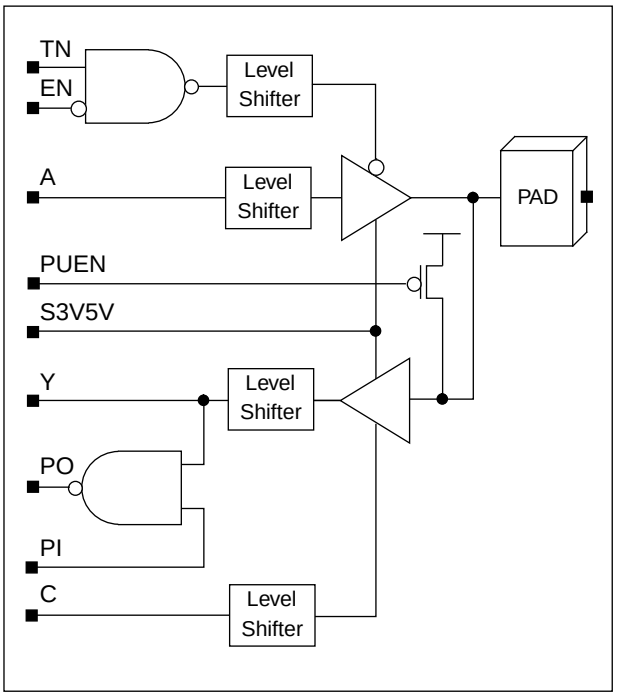
Input Load (SL)			I/O Slot
EN	TN	PUEN	
1.2	1.2	0.5	1.0

Cell Availability

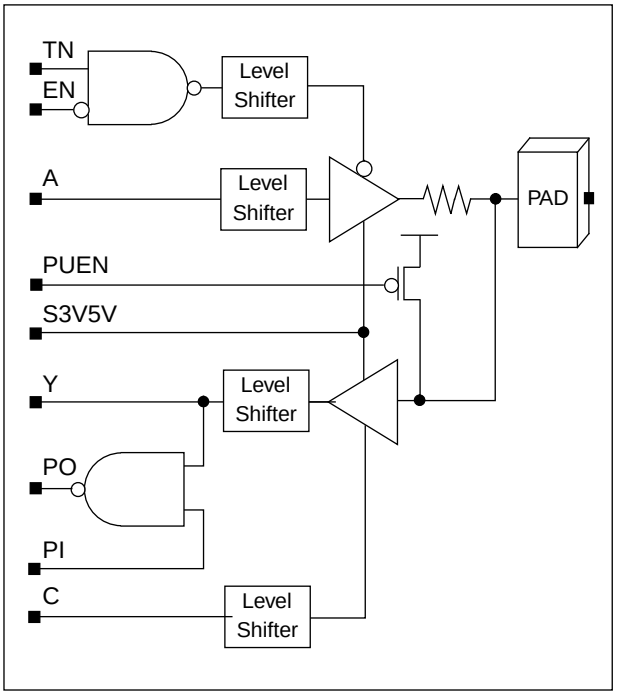
Library	5V Operation	3.3V Operation
STD80	–	PLBTTCBU/PLBTCCKCBU/PLBTCVSCBU
STDM80	–	PODCCKCBU

Logic Symbol

PLBTTCBU/PLBTCCKCBU



PLBTCVSCBU



Truth Table

Input Truth Table

PAD	C	PI	Y	PO
1	1	1	1	0
0	1	x	0	1
1	1	0	1	1
x	0	x	0	1

Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

* PUEN (Pull-up control pin) is low enable.

Cell Data

Input Load (SL)						I/O Slot
A	EN	TN	PUEN	C	PI	
2.3	1.2	1.2	0.5	4.0	1.6	1.0

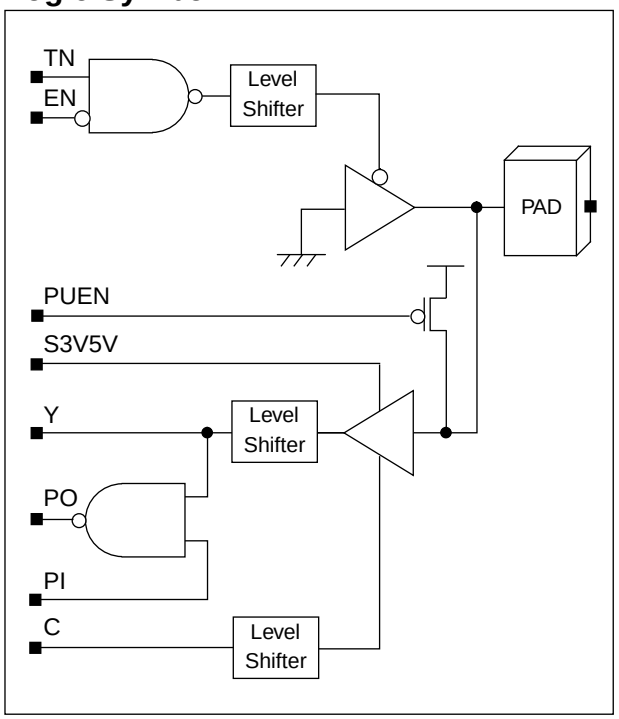
PvBDCCKCBU

Open Drain CardBus Bi-Directional Clock Driver with Pull-Up

Cell Availability

Library	5V Operation	3.3V Operation
STD80	–	PLBDCCKCBU
STDM80	–	PBDCCKCBU

Logic Symbol



Truth Table

Input Truth Table

PAD	C	PI	Y	PO
1	1	1	1	0
0	1	x	0	1
1	1	0	1	1
x	0	x	0	1

Output Truth Table

EN	TN	PAD
0	1	0
1	x	Hi-Z
x	0	Hi-Z

* PUEN (Pull-up control pin) is low enable.

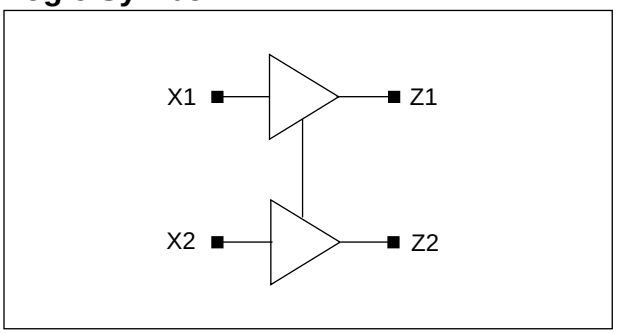
Cell Data

Input Load (SL)					I/O Slot
EN	TN	PUEN	C	PI	
1.2	1.2	0.5	4.0	1.6	1.0

Cell Availability

Library	5V Operation	3.3V Operation
STD80	–	PLSCB
STDM80	–	PLSCB

Logic Symbol



Truth Table

Xn	Zn
0	0
1 (VDDXI)	1 (VDDXO)

Cell Data

Input Load (SL)		I/O Slot
X1	X2	
2.4	2.4	1.0

USB (Universal Serial Bus) I/O Buffers

Overview

USB I/O buffer consists of a differential input receiver, a differential output driver, two single-ended drivers and two pads. The differential input receiver has 0.8V ~ 2.5V common mode input voltage range and both of the two single-ended receivers have 0.8V and 2.0V as their low and high input threshold voltages, V_{IL}, V_{IH}.

For low power consumption in a stand-by mode, the stand-by (STBYS) pins of two kinds of receivers should be in high state. The differential output drivers has LOw speed Slew Rate (LOSR) pin to select the operation speed and has ENL to achieve bi-directional half duplex operation.

Electrical Specifications

DC Electrical Characteristics

Parameter	Symbol	Condition (Notes 1, 2)	Min	Max	Unit
Supply Voltage					
VDD	V_{BUS}		4.75	5.25	V
Supply Current					
High Power Function	I_{CCHPF}			500	mA
Low Power Function	I_{CCLPF}			100	
Unconfig. Function / Hub	I_{CCINIT}			100	
Suspended Device	I_{CCS}			500	µA
Leakage Current					
Hi-Z State Data Line Leakage	I_{LO}	0V < VIN < 3.3V	–10	10	µA
Input Levels					
Differential Input Sensitivity	V_{DI}		0.2		V
Differential Common Mode Range	V_{CM}	Includes V_{DI} range	0.8	2.5	
Single Ended Receiver Threshold	V_{SE}		0.8	2.0	
Output Levels					
Static Output Low	V_{OL}	RL of 1.5KΩ to 3.6V		0.3	V
Static Output High	V_{OH}	RL of 15KΩ to GND	2.8	4.0	

Full Speed Source Electrical Characteristics

Parameter	Symbol	Condition (Notes 1, 2, 3)	Min	Max	Unit
Driver Characteristics					
Transition Time		Notes 5, 6 and Figure 1			ns
Rise Time	T_R	CL = 50pF	4.0	20.0	
Fall Time	T_F	CL = 50pF	4.0	20.0	
Rise/Fall Time Matching	T_{REM}	(T_R/T_F)	90	110	%
Output Signal Crossover Voltage	V_{CRS}		1.3	2.0	V

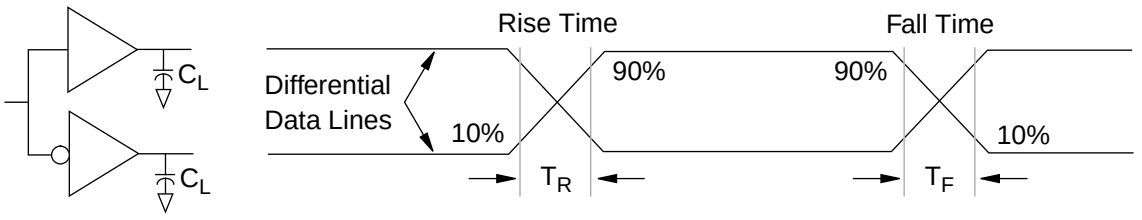
Low Speed Source Electrical Characteristics

Parameter	Symbol	Condition (Notes 1, 2, 4)	Min	Max	Unit
Driver Characteristics					
Transition Time		Notes 5, 6 and Figure 1			ns
Rise Time	T_R	CL = 50pF	75		
		CL = 350pF		300	
Fall Time	T_F	CL = 50pF	75		
		CL = 350pF		300	
Rise/Fall Time Matching	T_{REM}	(T_R/T_F)	80	120	%
Output Signal Crossover Voltage	V_{CRS}		1.3	2.0	V

NOTES:

1. All voltages are measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load (CL) to ground of 50pF, unless otherwise specified.
3. Full speed timings have a 1.5KΩ pull-up to 2.8V on the D+ data line.
4. Low speed timings have a 1.5KΩ pull-up to 2.8V on the D– data line.
5. Measured from 10% to 90% of the data signal.
6. The rising and falling edges should be smoothly transitioning (monotonic).

FIGURE 1: Data Signal Rise and Fall Time

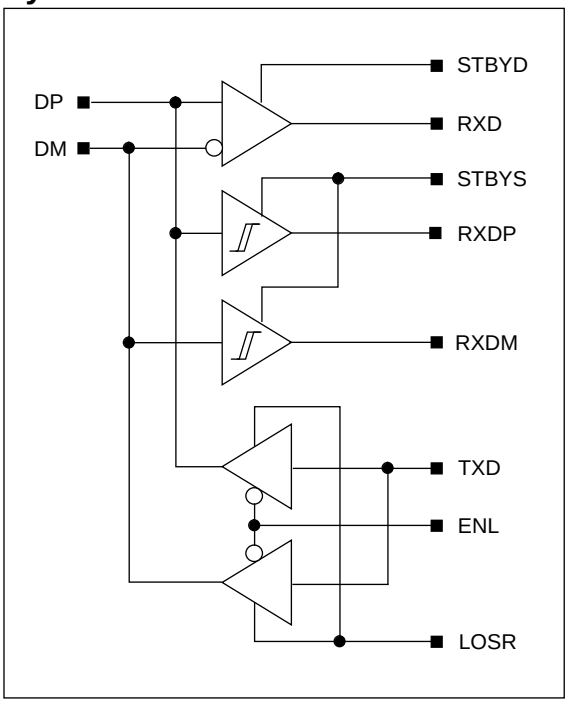


Full Speed: 4 to 20ns at C_L = 50pF Low Speed: 75ns at C_L = 50pF, 300ns at C_L = 350pF

PBUSB/PBUSB1

Universal Serial Bus Buffer

Symbol



Pin Connection

Input	Output	Bi-Direction
STBYD	RXD	DP
STBYS	RXDP	DM
TXD	RXDM	
ENL		
LOSR		

Cell Structure

PBUSB = PICDR + PISER + POTFLS (+ NDT3)

PBUSB1 = PICDR + PISER + POTFLS1 (+ NDT3)

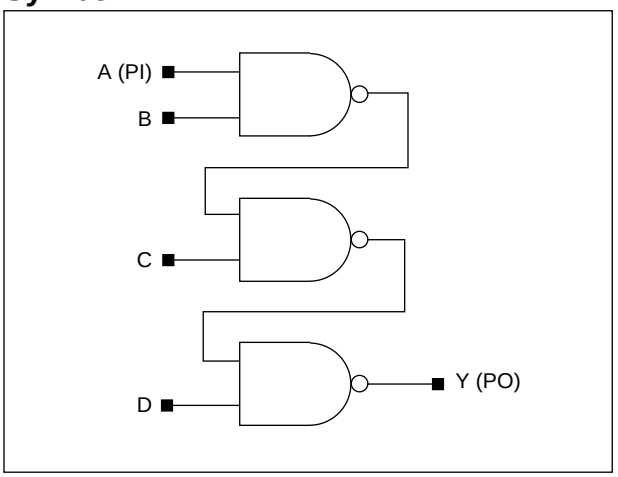
NDT3	Input Nand Tree (Soft-Macro Internal Cell)
PICDR	Differential Receiver
PISER	Single-Ended Receiver
POTFLS	Tri-State Output Buffer with Low Speed
POTFLS1	Tri-State Output Buffer with Full Speed

There only exists PBUSB not PBUSB1 in the physical DB. The division of cell name (PBUSB/PBUSB1) is caused to notify that one of their component cells, POTFLS/POTFLS1 has different AC timing values each other.

NDT3

Input Nand Tree (Soft-Macro Internal Cell)

Symbol



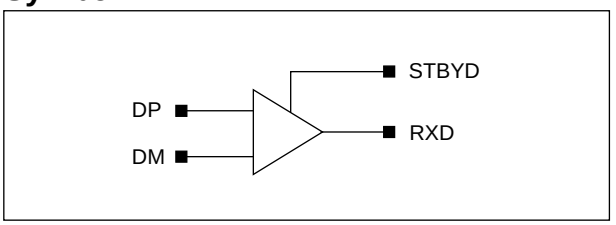
Pin Connection

Input	Output
A (PI) B C D	Y (PO)

PICDR

Differential Receiver

Symbol



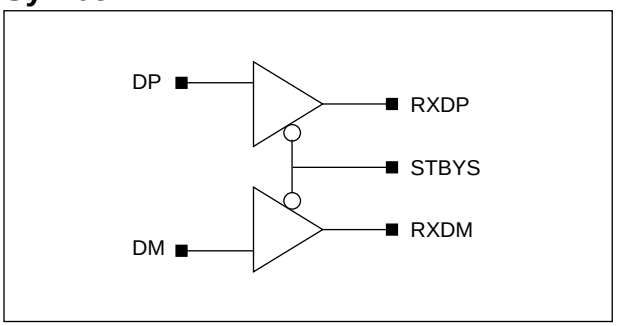
Pin Connection

Input	Output
STBYD DP DM	RXD

PISER

Single-Ended Receiver

Symbol



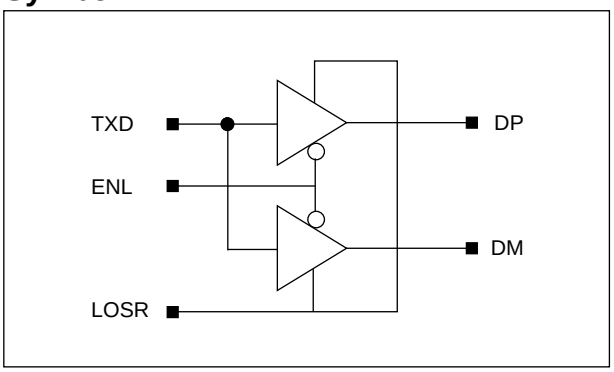
Pin Connection

Input	Output
STBYS	RXDP
DP	RXDM
DM	

POTFLS/POTFLS1

Tri-State Output Buffer with Low/Full Speed

Symbol



Pin Connection

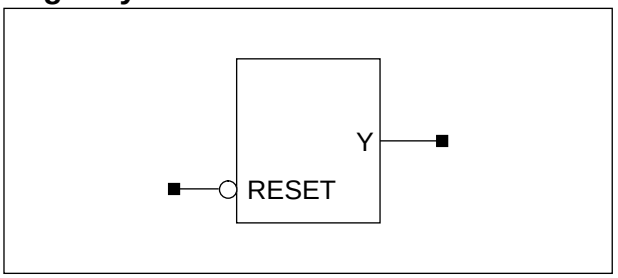
Input	Output
TXD	DP
ENL	DM
LOSR	

POTFLS has AC characteristics for low speed, and POTFLS1 for full speed.

Cell List

Cell Name	Function Description
VDET	Voltage Detector

Logic Symbol



* Y pin should be connected to S3V5V pin directly.
Do not use a level shifter buffer (PLSCB).

Pin Connection

Input	Output
RESET	Y

Truth Table

RESET	Y
0	0
1	0 (1) *

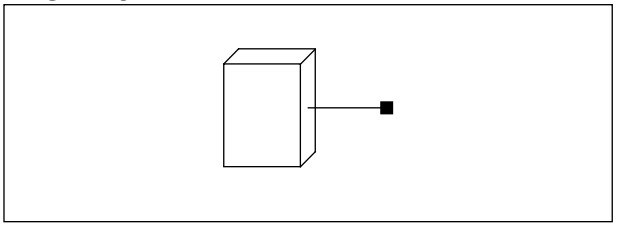
* If I/O supply voltage is 3.3V, output Y is high state.

POWER PADS

Cell List

Cell Name		Function Description
STD80		
VDD Power Pads	**VSS Power Pads**	
VDD5I	VSS5I	5V Internal
VDD5P	VSS5P	5V Pre-Driver
VDD5O	VSS5O	5V Output-Driver
VDD5IP	VSS5IP	5V Internal and Pre-Driver
VDD5OI	VSS5OI	5V Output-Driver and Internal
VDD5OP	VSS5OP	5V Output-Driver and Pre-Driver
VDD5T	VSS5T	5V Total
VDD3P	VSS3P	3.3V Pre-Driver
VDD3O	VSS3O	3.3V Output-Driver
VDD3OP	VSS3OP	3.3V Output-Driver and Pre-Driver
STDM80		
VDD Power Pads	**VSS Power Pads**	
VDD3I	VSS3I	3.3V Internal
VDD3P	VSS3P	3.3V Pre-Driver
VDD3O	VSS3O	3.3V Output-Driver
VDD3IP	VSS3IP	3.3V Internal and Pre-Driver
VDD3OI	VSS3OI	3.3V Output-Driver and Internal
VDD3OP	VSS3OP	3.3V Output-Driver and Pre-Driver
VDD3T	VSS3T	3.3V Total
VDD5P	VSS5P	5V Pre-Driver
VDD5O	VSS5O	5V Output-Driver
VDD5OP	VSS5OP	5V Output-Driver and Pre-Driver

Logic Symbol



Memory Compilers 5

Contents

Overview 5-1
Memory Compilers Selection Guide 5-2
CROM Gen 5-3
DROM Gen 5-10
SPSRAM Gen 5-17
SPSRAMA Gen 5-27
SPARAM Gen 5-39
DPSRAM Gen 5-48
DPSRAMA Gen 5-59
DPARAM Gen 5-72

OVERVIEW

This chapter contains information for memory compilers available in STD80/STDM80 cell library. These are complete compilers that consist of various generators to satisfy the requirements of the circuit at hand. Each of the final building block, the physical layout, will be implemented as a stand-alone, densely packed, pitch-matched array. Using this complex layout generator and adopting state-of-the-art logic and circuit design technique, these memory cells can realize extreme density and performance. In each layout generator, we added an option which makes the aspect ratio of the physical layout selectable so that the ASIC designers can choose the aspect ratio according to the convenience of the chip level layout.

In the STD80/STDM80 cell library, there are 4 groups of memory compilers — ROMs; Static RAMs; Register File; FIFO.

Generators

Each memory compiler is a set of various, parameterized generators. The generators are:

- Layout Generator
  : generates an array of custom, pitch-matched leaf cells.
- Schematic Generator & Netlister
  : extracts a netlist which can be used for both LVS check and functional verification.
- Function & Timing Model Generators
  : for gate level simulation, dynamic/static timing analysis and synthesis
- Symbol Generator
  : for schematic capture
- Critical Path Generator & ETC
  : there are many special purpose generators such as critical path generator used for both circuit design and AC timing characterization.

Advanced Design Technique

All of 0.5μm CMOS standard cell memory compilers adopt very advanced design technique to obtain extremely high performance in terms of both speed and power consumption. Below are major techniques.

For reducing power consumption

- Minimized bit-line precharge/discharge voltage swing
- Zero static current consuming sense amplifier
- Automatic power down after an access

For optimizing and minimizing the read access time

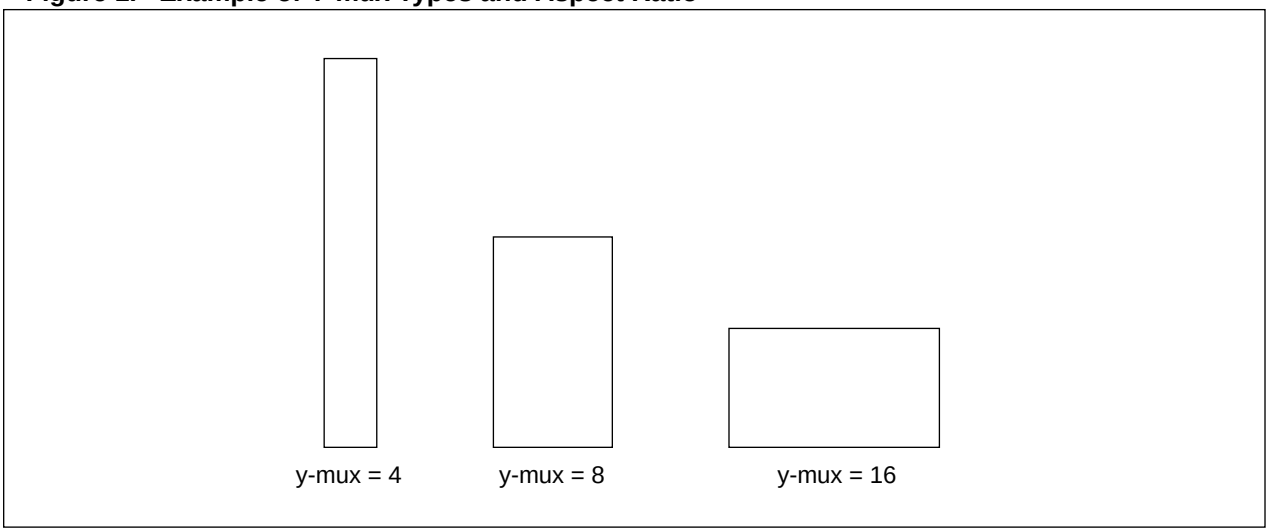
- Size sensitive self-timer delay
- Extremely simple tri-state output circuit

Flexible Aspect Ratio

The size of a memory cell is defined by its number of words (WORDS) and number of bits per word (BPW). But, this size is only a logical size. The physical size of a memory is defined by the number of rows (ROWS) and the number of columns (COLS) of its bit cell array. Usually, we can't make the bit cell array with WORDS and BPW because the range of WORDS is much larger than the range of BPW. If we make the bit cell array with WORDS and BPW, most of memory layouts will have too tall and too thin aspect ratio. Therefore, column decoder and y-mux circuit are included in most of memory cells to adjust the aspect ratio.

In 0.5μm CMOS standard cell memory compilers, the y-mux type selecting option was added to give the customers freedom selecting aspect ratio of the memory layout. Many of the characteristics of a memory cell depend on its y-mux type. So, when you change the y-mux type from one to the other to change the aspect ratio, you have to know that it will change many major characteristics, such as access time, area and power consumption, of the memory.

< Figure 1. Example of Y-mux Types and Aspect Ratio >



Dual Banks

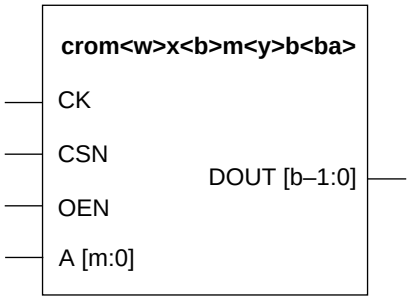
In some of 0.5μm CMOS standard cell memory compilers is a generator option which defines the number of bit array banks. This dual bank scheme doubles the maximum capacity of the memory compilers.

MEMORY COMPILERS SELECTION GUIDE

Memory Group	Cell Name	Function Description
ROM	CROM Gen	Contact Programmable Synchronous ROM Generator
	DROM Gen	Diffusion Programmable Synchronous ROM Generator
Static RAM	SPSRAM Gen	Single-Port Synchronous RAM Generator – Reads and writes at the same edge of clock
	SPSRAMA Gen	Single-Port Synchronous RAM Generator – Alternative – Reads and writes at different edges of clock
	SPARAM Gen	Single-Port Asynchronous RAM Generator – Fully asynchronous read, WEN synchronized write
	DPSRAM Gen	Dual-Port Synchronous RAM Generator – Reads and writes at the same edge of clock
	DPARAM* Gen	Dual-Port Asynchronous RAM Generator – Fully asynchronous read, WEN synchronized write
	DPSRAMA Gen	Dual-Port Synchronous RAM Generator – Alternative – Reads and writes at different edges of clock
Register File	IRIW*	1 Read Port, 1 Write Port Synchronous Register File
FIFO	FIFO*	Synchronous FIFO

* Under-Developed

Logic Symbol



NOTES:

1. Words (w) is the number of words in CROM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Static differential operation
- Stand-by (power down) mode available
- Tri-state output
- Low noise output circuit
- Programmable with contact layer
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 128K bits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

CROM Gen is a contact programmable synchronous ROM. When CK rises, DOUT [ ] presents data programmed in the location addressed by A [ ]. CSN is used to enable/disable the clock. OEN is used to enable/disable the data output driver.

Generators and Cell Configurations

CROM Gen. generates layout, netlist, symbol and functional & timing model of CROM. The layout of CROM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of CROM, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	32	64	128	256
		Max	1024	2048	4096	8192
		Step	8	16	32	64
Bpw (b)	ba = 1	Min	1	1	1	1
		Max	64	32	16	8
		Step	1	1	1	1
	ba = 2	Min	2	2	2	2
		Max	128	64	32	16
		Step	1	1	1	1

CROM Gen

Contact Programmable Synchronous ROM Generator

Pin Descriptions

Name	I/O	Description
CK	I	“Clock” serves as the input clock to the memory block. When CK is low the memory is in a precharge state. Upon the rising edge, an access cycle begins.
CSN	I	“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read access occur. CSN may not change during CK is high.
OEN	I	“Output Enable Negative” controls the output drivers from driven to tri-state condition. OEN may not change during CK is high.
A [ ]	I	“Address” selects the location to be accessed. A [ ] may not change during CK is high.
DOUT [ ]	O	During a read access, data word programmed will be presented to the “Data Out” ports. DOUT [ ] is tri-statable. When CK is high, CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state.

Pin Capacitance

(Unit = SL)

	CK	CSN	OEN	A	DOUT			
					Ymux 4	Ymux 8	Ymux 16	Ymux 32
1-bank	5.8	1.8	2.2	1.7	4.0	8.7	18.0	37.0
2-bank	11.5	3.7	4.4	1.7	4.0	8.7	18.0	37.0

Application Notes

1) Putting Busholders on DOUT [ ]

As you will see in the timing diagrams, DOUT [ ] is valid only when CK is high. If you want DOUT [ ] to be stable regardless of CK state, you should put STD80/STDM80 Busholder cells on the DOUT [ ] bus externally.

2) Customizing Aspect Ratio

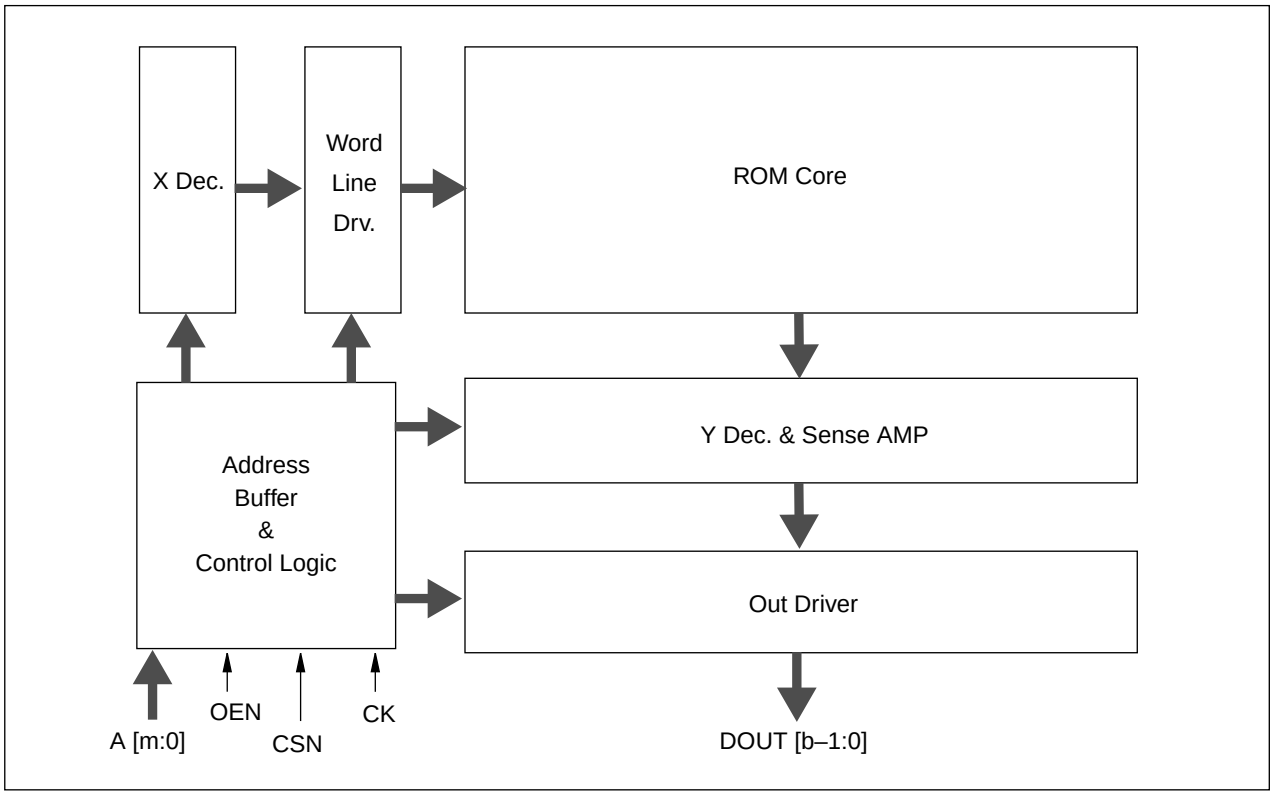
Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 4 selections of Ymux for the same Words and the same Bpw CROM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of CROM, In general, larger Ymux CROM has faster speed and bigger area than smaller Ymux CROM.

3) Selecting Number of Banks

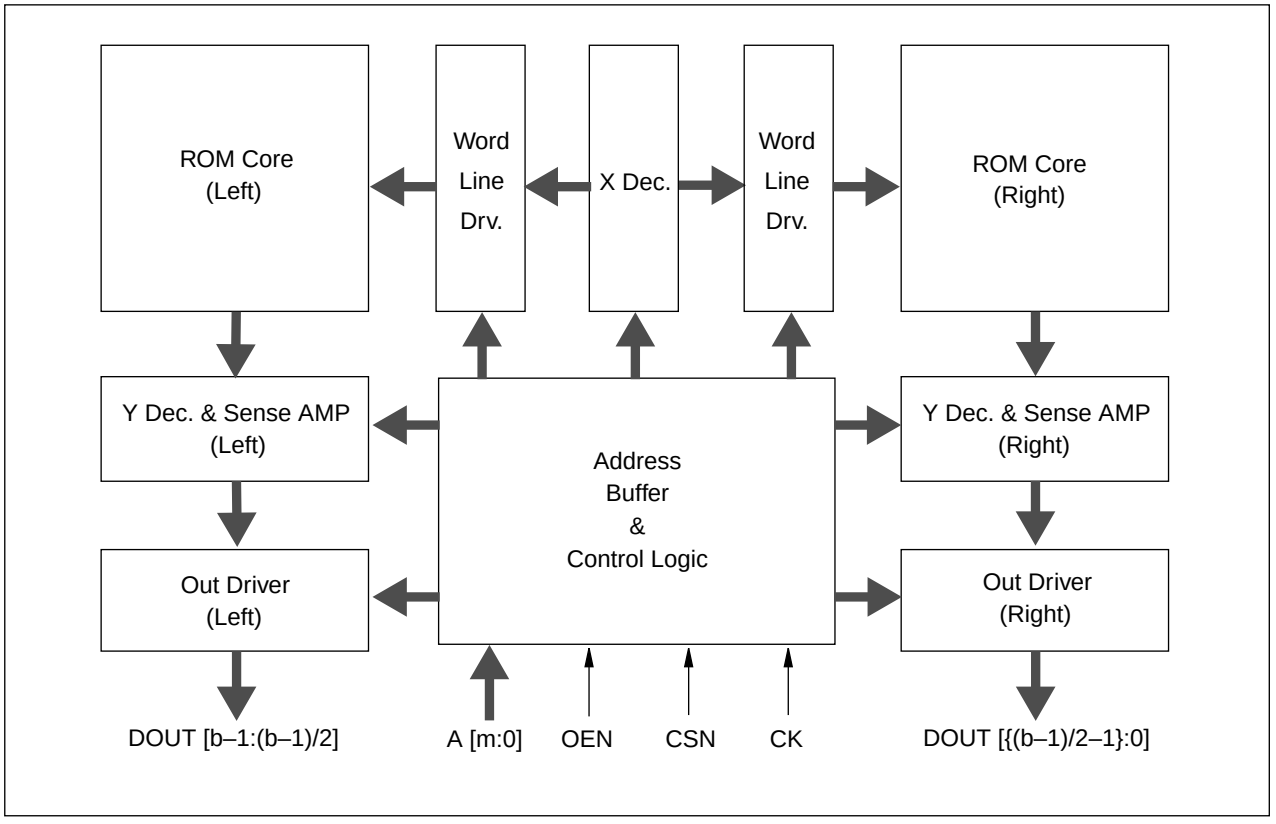
To enlarge the capacity of CROM, we added one more option to choose number of banks. If you want to use larger CROM than 64K bit CROM, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 64K bit CROM. Dual bank CROM is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

Block Diagrams

< 1-bank >



< 2-bank >



Characteristic Reference Table

STD80

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 5V, 25 ^{o}C, Output load = 10SL, Unit = ns)							
minckl	Minimum Clock Pulse Width Low	2.60	2.60	3.00	3.00	3.90	3.90
minckh	Minimum Clock Pulse Width High	4.90	4.90	5.90	5.90	7.80	7.80
t_{as}	Address Setup Time	0.40	0.40	0.60	0.60	1.00	1.00
t_{ah}	Address Hold Time	0	0	1.40	1.40	1.70	1.70
t_{cs}	CSN Setup Time	0.38	0.38	0.38	0.38	0.38	0.38
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{os}	OEN Setup Time	0	0	0	0	0	0
t_{oh}	OEN Hold Time	1.80	1.80	1.90	1.90	2.10	1.90
t_{acc}	Access Time	3.10	3.10	3.50	3.50	4.20	4.20
t_{da}	Deaccess Time	1.90	1.90	1.90	1.90	1.90	1.90
SIZE (μm)							
Width		466	595	757	886	1329	1458
Height		443	443	638	638	1028	1028
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)			1283		2700		6475
power_csn (stand-by mode: CSN High)			45		71		121

STDM80

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{o}C, Output load = 10SL, Unit = ns)							
minckl	Minimum Clock Pulse Width Low	3.60	3.60	4.20	4.20	5.50	5.50
minckh	Minimum Clock Pulse Width High	7.10	7.10	8.50	8.50	11.40	11.40
t_{as}	Address Setup Time	0.40	0.40	0.70	0.70	1.40	1.30
t_{ah}	Address Hold Time	0	0	1.80	1.80	2.30	2.20
t_{cs}	CSN Setup Time	0.60	0.60	0.60	0.60	0.60	0.60
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{os}	OEN Setup Time	0	0	0	0	0	0
t_{oh}	OEN Hold Time	2.50	2.40	2.60	2.50	2.90	2.60
t_{acc}	Access Time	4.40	4.40	5.00	5.00	6.10	6.10
t_{da}	Deaccess Time	2.60	2.60	2.60	2.60	2.60	2.60
SIZE (μm)							
Width		466	595	757	886	1329	1458
Height		443	443	638	638	1028	1028
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)			604		1299		3321
power_csn (stand-by mode: CSN High)			18		29		50

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
BA: Number of Banks (1 or 2)
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

STD80

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 4
minckh	(3.3175e – 03 * W + 1.4583e – 01 * S + 2.2165e – 01 * 0.019 * SL + 2.7969) * 1.1
minckl	(1.7122e – 03 * W + 1.8311e – 01 * S + 5.8198e – 03 * 0.019 * SL + 1.9047)
tacc	(1.5030e – 03 * W + 1.6557e – 01 * S + 3.9827e – 01 * 0.019 * SL + 2.3576)
	Y = 8
minckh	(1.6322e – 03 * W + 1.4692e – 01 * S + 2.5139e – 01 * 0.019 * SL + 2.7965) * 1.1
minckl	(8.5614e – 04 * W + 1.8311e – 01 * S + 5.8198e – 03 * 0.019 * SL + 1.9047)
tacc	(7.5152e – 04 * W + 1.6557e – 01 * S + 3.9827e – 01 * 0.019 * SL + 2.3576)
	Y = 16
minckh	(8.0853e – 04 * W + 1.4912e – 01 * S + 2.9137e – 01 * 0.019 * SL + 2.7911) * 1.1
minckl	(4.2807e – 04 * W + 1.8311e – 01 * S + 5.8198e – 03 * 0.019 * SL + 1.9047)
tacc	(3.7576e – 04 * W + 1.6557e – 01 * S + 3.9827e – 01 * 0.019 * SL + 2.3576)
	Y = 32
minckh	(3.8015e – 04 * W + 1.6008e – 01 * S + 3.9802e – 01 * 0.019 * SL + 2.8462) * 1.1
minckl	(2.1403e – 04 * W + 1.8311e – 01 * S + 5.8198e – 03 * 0.019 * SL + 1.9047)
tacc	(1.8788e – 04 * W + 1.6557e – 01 * S + 3.9827e – 0 1 * 0.019 * SL + 2.3576)

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 4
power_ck	(4.6376e – 02 * W + 1.5361 * B + 4.7973 + 2.4698e – 03 * W * B) * VDD^2 * F
power_csn	(1.4304e – 05 * W + 6.4197e – 02 * B + 8.0019e – 01 – 1.1140e – 06 * W * B) * VDD^2 * F
	Y = 8
power_ck	(2.7020e – 02 * W + 2.6893 * B + 3.6826 + 2.0572e – 03 * W * B) * VDD^2 * F
power_csn	(7.1521e – 06 * W + 1.2839e – 01 * B + 8.0019e – 01 – 1.1140e – 06 * W * B) * VDD^2 * F
	Y = 16
power_ck	(1.3385e – 02 * W + 4.9883 * B + 3.7560 + 1.8472e – 03 * W * B) * VDD^2 * F
power_csn	(3.5760e – 06 * W + 2.5679e – 01 * B + 8.0019e – 01 – 1.1140e – 06 * W * B) * VDD^2 * F
	Y = 32
power_ck	(6.3702e – 03 * W + 9.5401 * B + 4.8783 + 1.8001e – 03 * W * B) * VDD^2 * F
power_csn	(1.7880e – 06 * W + 5.1358e – 01 * B + 8.0019e – 01 – 1.1140e – 06 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 8.75 * ($\lceil \log_2 (W / Y) \rceil$) + 129.65 * BA + 4.4 * (B * Y) + 1.4 [μm]
Height = 247.15 + 3.05 * W / Y [μm]

STDM80

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 4
minckh	(4.9874e – 03 * W + 1.2996e – 01 * S + 3.0225e – 01 * 0.019 * SL + 4.1325) * 1.1
minckl	(2.5384e – 03 * W + 2.2222e – 01 * S + 2.5303e – 03 * 0.019 * SL + 2.6714)
tacc	(2.1877e – 03 * W + 1.8452e – 01 * S + 5.0657e – 01 * 0.019 * SL + 3.3008)
	Y = 8
minckh	(2.4557e – 03 * W + 1.8154e – 01 * S + 3.2224e – 01 * 0.019 * SL + 4.1080) * 1.1
minckl	(1.2692e – 03 * W + 2.2222e – 01 * S + 2.5303e – 03 * 0.019 * SL + 2.6714)
tacc	(1.0938e – 03 * W + 1.8452e – 01 * S + 5.0657e – 01 * 0.019 * SL + 3.3008)
	Y = 16
minckh	(1.2061e – 03 * W +1.9444e – 01 * S + 3.9119e – 01 * 0.019 * SL + 4.1096) * 1.1
minckl	(6.3462e – 04 * W + 2.2222e – 01 * S + 2.5303e – 03 * 0.019 * SL + 2.6714)
tacc	(5.4693e – 04 * W + 1.8452e – 01 * S + 5.0657e – 01 * 0.019 * SL + 3.3008)
	Y = 32
minckh	(5.6878e – 04 * W + 2.0039e – 01 * S + 5.2378e – 01 * 0.019 * SL + 4.2085) * 1.1
minckl	(3.1731e – 04 * W + 2.2222e – 01 * S + 2.5303e – 03 * 0.019 * SL + 2.6714)
tacc	(2.7346e – 04 * W + 1.8452e – 01 * S + 5.0657e – 01 * 0.019 * SL + 3.3008)

2) Power Characteristics [Unit: μW]

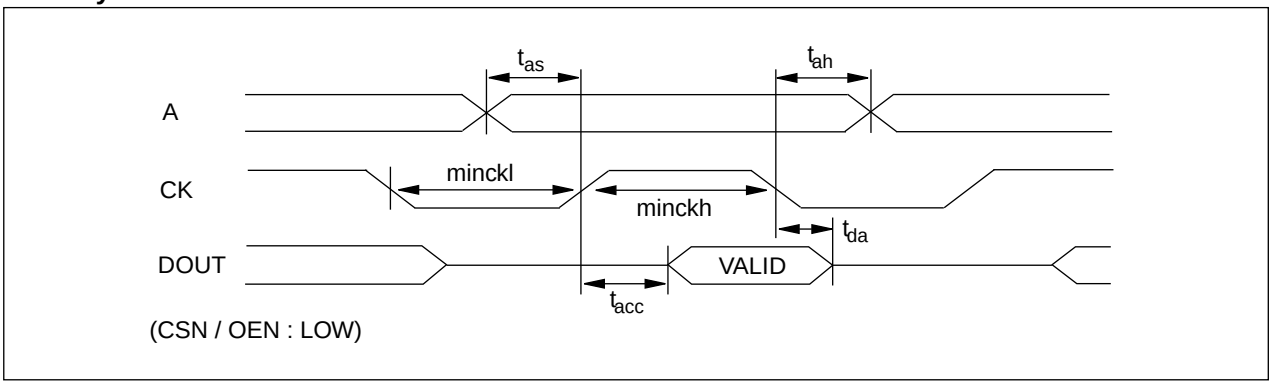
Power Type	Power Equation
	Y = 4
power_ck	(3.6222e – 02 * W + 1.5020 * B + 7.9632 + 3.4749e – 03 * W * B) * VDD^2 * F
power_csn	(2.0622e – 05 * W + 6.2300e – 02 * B + 7.3939e – 01 – 1.6060e – 06 * W * B) * VDD^2 * F
	Y = 8
power_ck	(2.0111e – 02 * W + 2.6231 * B + 7.1117 + 3.0340e – 03 * W * B) * VDD^2 * F
power_csn	(1.0311e – 05 * W + 1.2460e – 01 * B + 7.3939e – 01 -1.6060e – 06 * W * B) * VDD^2 * F
	Y = 16
power_ck	(9.9589e – 03 * W + 4.9313 * B + 7.1000 + 2.7268e – 03 * W * B) * VDD^2 * F
power_csn	(5.1556e – 06 * W + 2.4920e – 01 * B + 7.3939e – 01 -1.6060e – 06 * W * B) * VDD^2 * F
	Y = 32
power_ck	(5.3331e – 03 * W + 9.6566 * B + 6.9698 + 2.5764e – 03 * W * B) * VDD^2 * F
power_csn	(2.5778e – 06 * W + 4.9840e – 01 * B + 7.3939e – 01 -1.6060e – 06 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

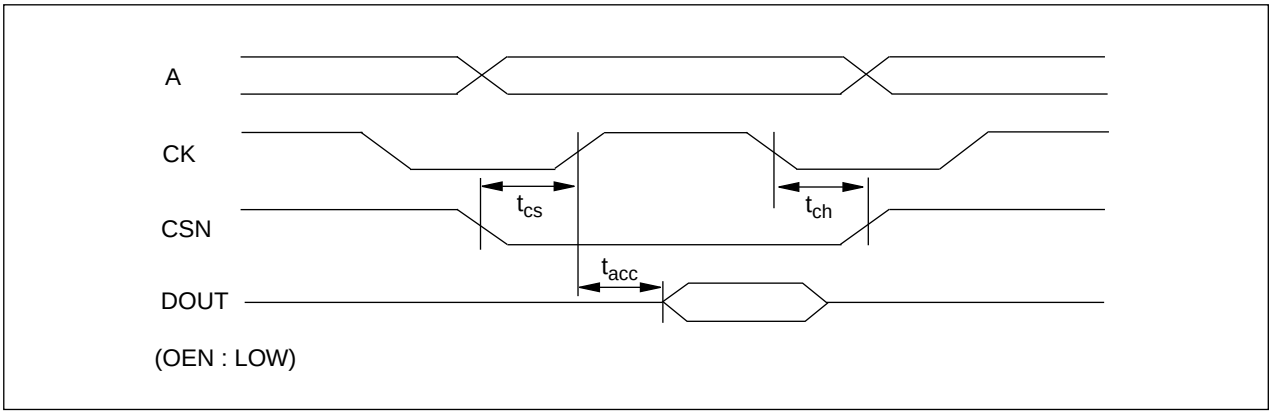
Width = 8.75 * ($\lceil \log_2 (W / Y) \rceil$) + 129.65 * BA + 4.4 * (B * Y) + 1.4 [μm]
Height = 247.15 + 3.05 * W / Y [μm]

Timing Diagrams

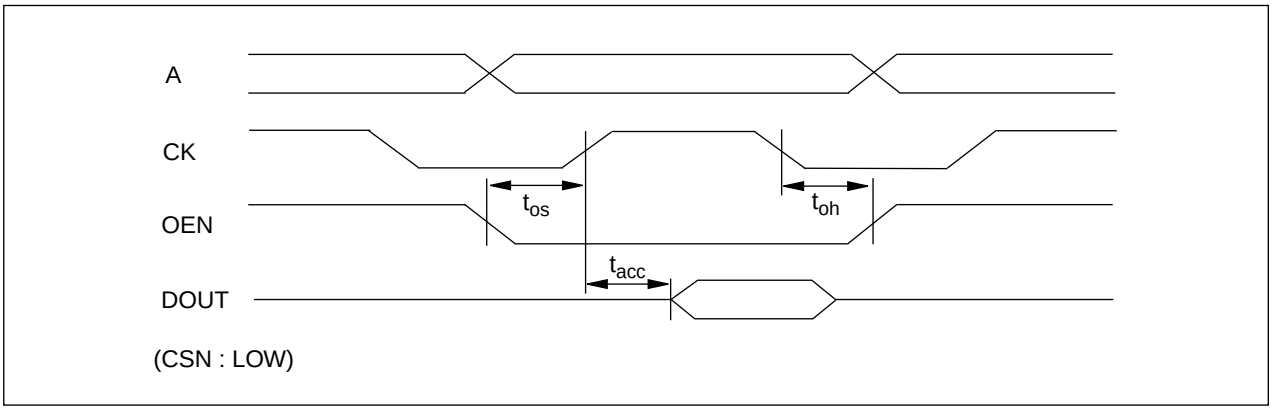
Read Cycle



CSN Control



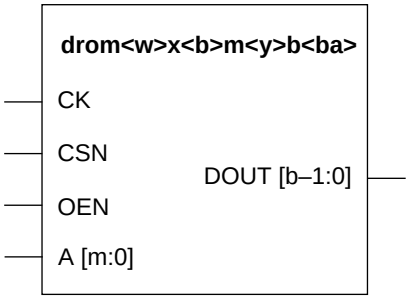
OEN Control



DROM Gen

Diffusion Programmable Synchronous ROM Generator

Logic Symbol



NOTES:

1. Words (w) is the number of words in a DROM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Stand-by (power down) mode available
- Latched output
- Unconditionally controlled tri-state output
- Low noise output circuit
- Programmable with diffusion layer
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 512K bits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

DROM is a diffusion programmable synchronous ROM. When CK rises, DOUT [ ] presents data programmed in the location addressed by A [ ]. CSN is used to enable/disable the clock. OEN is used to enable/disable the data output driver.

Generators and Cell Configurations

DROM Gen. generates layout, netlist, symbol and functional & timing model of DROM. The layout of DROM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of DROM, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	16	32	64
		Max	4096	8192	16384
		Step	16	32	64
Bpw (b)	ba = 1	Min	2	2	2
		Max	64	32	16
		Step	1	1	1
	ba = 2	Min	4	4	4
		Max	128	64	32
		Step	1	1	1

Pin Descriptions

Name	I/O	Description
CK	I	“Clock” serves as the input clock to the memory block. When CK is low the memory is in a precharge state. Upon the rising edge, an access cycle begins.
CSN	I	“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read access occur. CSN may not change during CK is high.
OEN	I	“Output Enable Negative” unconditionally controls the output drivers from driven to tri-state condition.
A [ ]	I	“Address” selects the location to be accessed. A [ ] may not change during CK is high.
DOUT [ ]	O	During a read access, data word programmed will be presented to the “Data Out” ports. DOUT [ ] is latched during a full cycle. When CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state.

Pin Capacitance

(Unit = SL)

	CK	CSN	OEN	A	DOUT
1-bank	2.1	0.6	1.1	2.3	44.0
2-bank	4.2	1.2	2.2	2.3	44.0

Application Notes

1) Customizing Aspect Ratio

Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 3 selections of Ymux for the same Words and the same Bpw DROM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of DROM, In general, larger Ymux DROM has faster speed and bigger area than smaller Ymux DROM.

2) Selecting Number of Banks

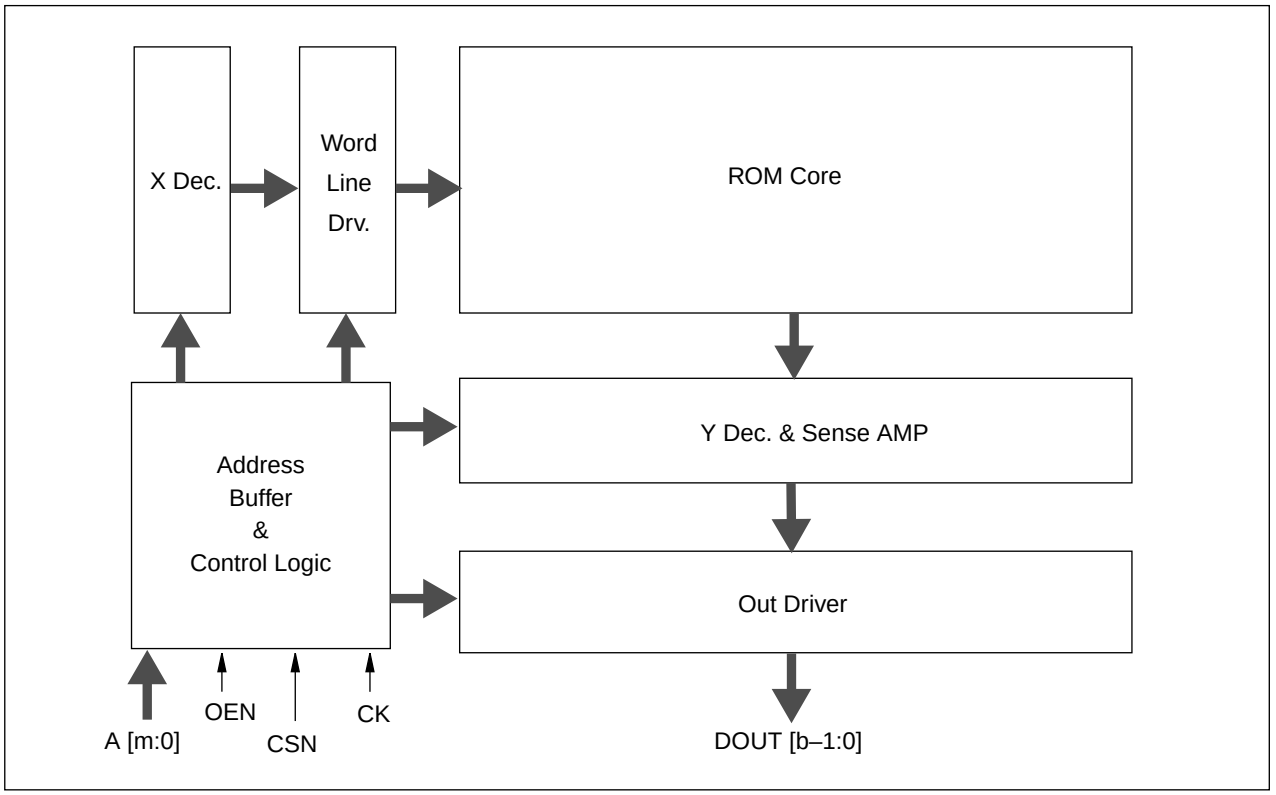
To enlarge the capacity of DROM, we added one more option to choose number of banks. If you want to use larger DROM than 256K bit DROM, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 256K bit DROM. Dual bank DROM is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

DROM Gen

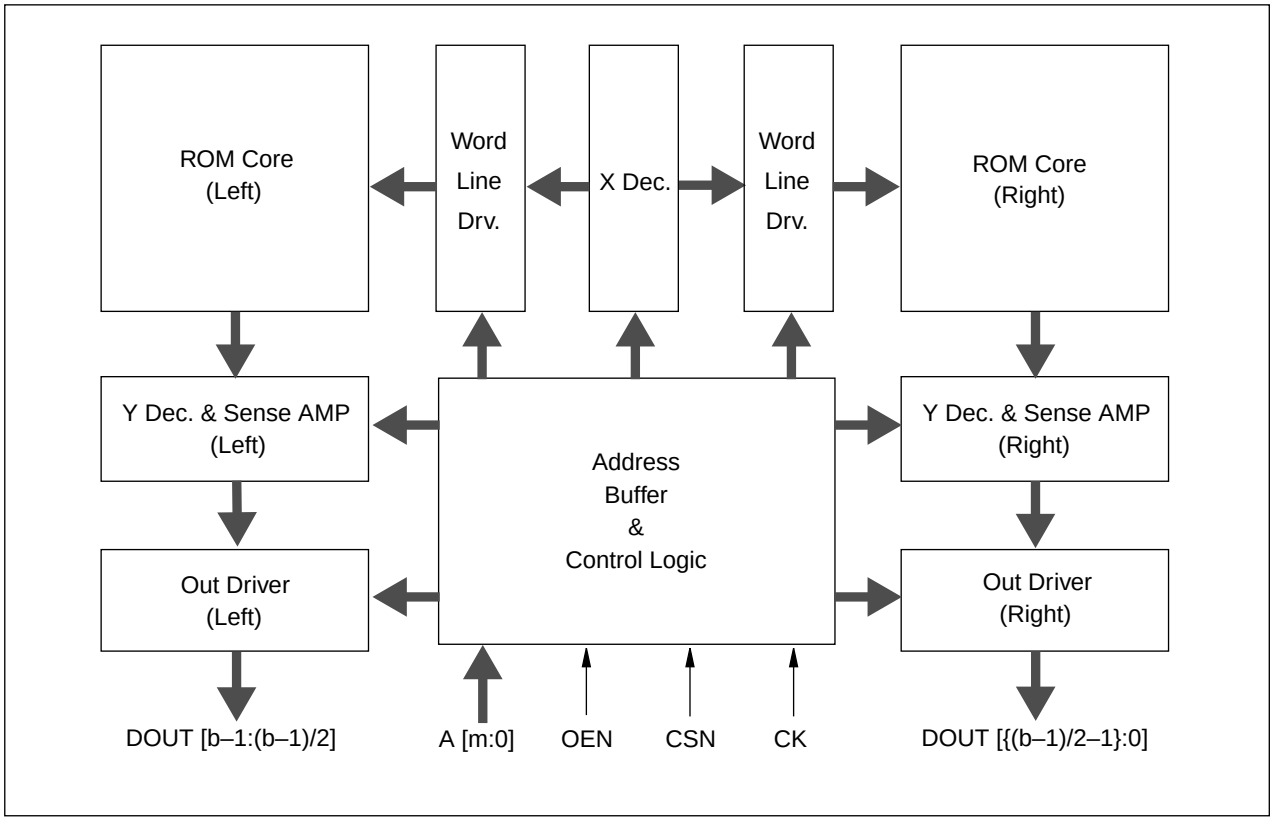
Diffusion Programmable Synchronous ROM Generator

Block Diagrams

< 1-bank >



< 2-bank >



Characteristic Reference Table

STD80

Symbol	Description	256x16m8		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 5V, 25 ^{o}C, Output load = 10SL, Unit = ns)							
minckl	Minimum Clock Pulse Width Low	1.60	1.50	1.60	1.50	1.90	1.60
minckh	Minimum Clock Pulse Width High	4.40	4.20	5.0	4.8	6.5	6.2
t_{as}	Address Setup Time	0.10	0.10	0.20	0.20	0.30	0.30
t_{ah}	Address Hold Time	0	0	0	0	0	0
t_{cs}	CSN Setup Time	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{acc}	Access Time	5.20	5.10	5.90	5.70	7.10	6.70
t_{da}	Deaccess Time	3.80	3.60	4.40	4.20	5.60	5.20
t_{zd}	Hi-Z to Valid Data	1.70	1.70	1.70	1.70	1.70	1.70
t_{dz}	Valid Data to Hi-Z	1.00	0.90	1.00	0.90	1.00	1.00
mincyc	Minimum Clock Cycle Time	5.70	5.40	7.30	7.00	10.20	9.70
SIZE (μm)							
Width		556	720	576	740	917	1081
Height		305	305	526	526	823	823
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)			785		1452		3842
power_csn (stand-by mode: CSN High)			15		15		24

STDM80

Symbol	Description	256x16m8		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{o}C, Output load = 10SL, Unit = ns)							
minckl	Minimum Clock Pulse Width Low	2.30	2.10	2.30	2.10	2.60	2.30
minckh	Minimum Clock Pulse Width High	6.70	6.40	7.70	7.50	10.10	9.60
t_{as}	Address Setup Time	0.20	0.20	0.30	0.30	0.40	0.40
t_{ah}	Address Hold Time	0	0	0	0	0	0
t_{cs}	CSN Setup Time	0.50	0.50	0.50	0.50	0.50	0.50
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{acc}	Access Time	7.80	7.50	8.80	8.60	10.70	10.20
t_{da}	Deaccess Time	5.90	5.60	6.90	6.70	8.80	8.30
t_{zd}	Hi-Z to Valid Data	2.40	2.40	2.40	2.40	2.40	2.40
t_{dz}	Valid Data to Hi-Z	1.90	1.80	1.90	1.80	2.00	1.90
mincyc	Minimum Clock Cycle Time	8.40	8.10	11.10	10.80	15.60	14.90
SIZE (μm)							
Width		556	720	576	740	917	1081
Height		305	305	526	526	823	823
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)			364		705		1962
power_csn (stand-by mode: CSN High)			9		9		13

DROM Gen

Diffusion Programmable Synchronous ROM Generator

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
BA: Number of Banks (1 or 2)
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

STD80

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 8
minckh	(8.2203e – 04 * W + 2.3006e – 02 * B / BA + 8.6348e – 02 * S + 3.6997)
mincyc	(2.1349e – 03 * W + 3.1585e – 02 * B / BA + 7.9769e – 02 * S + 4.5076)
minckl	(1.7851e – 02 * B / BA + 2.4313e – 01 * S + 1.0586 – 1.4159e – 03 * B / BA * S)
tacc	(8.1748e – 04 * W + 2.2545e – 02 * B / BA + 9.3201e – 02 * S + 6.9313e – 01 * 0.019 * SL + 4.4137)
	Y = 16
minckh	(4.1293e – 04 * W + 4.5635e – 02 * B / BA + 8.2236e – 02 * S + 4.0192)
mincyc	(1.0224e – 03 * W + 6.6842e – 02 * B / BA + 2.0888e – 01 * S + 4.6828)
minckl	(3.5702e – 02 * B / BA + 2.4313e – 01 * S + 1.0586 – 2.8318e – 03 * B / BA * S)
tacc	(4.0874e – 04 * W + 4.5090e – 02 * B / BA + 9.3201e – 02 * S + 6.9313e – 01 * 0.019 * SL + 4.4137)
	Y = 32
minckh	(2.0606e – 04 * W + 8.9923e – 02 * B / BA + 9.7039e – 02 * S + 4.6465)
mincyc	(4.6249e – 04 * W + 1.3320e – 01 * B / BA + 1.6529e – 01 * S + 5.3888)
minckl	(7.1405e – 02 * B / BA + 2.4313e – 01 * S + 1.0586 – 5.6636e – 03 * B / BA * S)
tacc	(2.0437e – 04 * W + 9.0181e – 02 * B / BA + 9.3201e – 02 * S + 6.9313e – 01 * 0.019 * SL + 4.4137)

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 8
power_ck	(1.5962e – 02 * W + 1.0692 * B + 5.3930 + 1.1779e – 03 * W * B) * VDD^2 * F
power_csn	(1.0460e – 10 * W + 2.2399e – 02 * B + 2.5200e – 01 – 1.4450e – 11 * W * B) * VDD^2 * F
	Y = 16
power_ck	(7.5901e – 03 * W + 1.7134 * B + 5.4951 + 1.3695e – 03 * W * B) * VDD^2 * F
power_csn	(5.1138e – 11 * W + 4.4799e – 02 * B + 2.5200e – 01 – 1.4319e – 11 * W * B) * VDD^2 * F
	Y = 32
power_ck	(3.4176e – 03 * W + 3.2755 * B + 6.0417 + 1.5281e – 03 * W * B) * VDD^2 * F
power_csn	(2.5284e – 11 * W + 8.9599e – 02 * B + 2.5200e – 01 – 1.4253e – 11 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 10.2 * ($\lceil \log_2 (W / Y) \rceil$) + 164.8 * BA + 2.5843 (B * Y) + 8.2 [μm]
Height = 225.1 + 2.30 * W / Y + M [μm]
M = 6.05 (if Y = 8), M = 8.45 (if Y = 16), M = 10.85 (if Y = 32)

STDM80

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 8
mincyc	(3.5198e – 03 * W + 4.5826e – 02 * B / BA + 2.4255e – 01 * S + 6.4868)
minckh	(1.3433e – 03 * W + 3.3260e – 02 * B / BA + 1.2351e – 01 * S + 5.6854)
minckl	(2.3158e – 02 * B / BA + 2.9813e – 01 * S + 1.6106 – 2.4974e – 03 * B / BA * S)
tacc	(1.3364e – 03 * W + 3.3374e – 02 * B / BA + 1.0962e – 01 * S + 8.2600e – 01 * 0.019 * SL + 6.6360)
	Y = 16
mincyc	(1.6536e – 03 * W + 9.2665e – 02 * B / BA + 2.9389e – 01 * S + 6.9996)
minckh	(6.6951e – 04 * W + 6.6059e – 02 * B / BA + 1.1160e – 01 * S + 6.1996)
minckl	(4.6317e – 02 * B / BA + 2.9813e – 01 * S + 1.6106 – 4.9948e – 03 * B / BA * S)
tacc	(6.6823e – 04 * W + 6.6748e – 02 * B / BA + 1.0962e – 01 * S + 8.2600e – 01 * 0.019 * SL + 6.6360)
	Y = 32
mincyc	(7.6109e – 04 * W + 1.9146e – 01 * B / BA + 2.5595e – 01 * S + 8.0221)
minckh	(3.3361e – 04 * W + 1.3092e – 01 * B / BA + 1.1383e – 01 * S + 7.1958)
minckl	(9.2635e – 02 * B / BA + 2.9813e – 01 * S + 1.6106 – 9.9896e – 03 * B / BA * S)
tacc	(3.3411e – 04 * W + 1.3349e – 01 * B / BA + 1.0962e – 01 * S + 8.2600e -01 * 0.019 * SL + 6.6360)

2) Power Characteristics [Unit: μW]

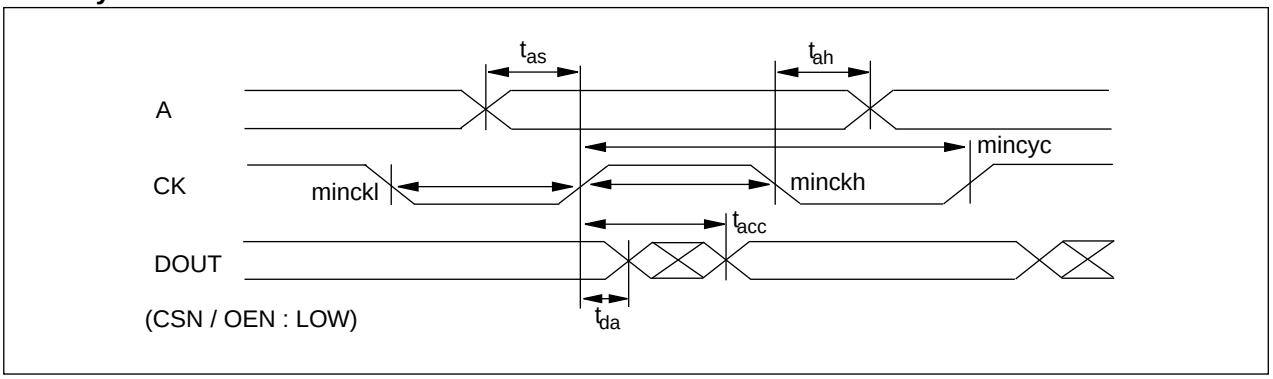
Power Type	Power Equation
	Y = 8
power_ck	(1.6785e – 02 * W + 1.1261 * B + 5.1661 + 1.4915e – 03 * W * B) * VDD^2 * F
power_csn	(1.2353e – 05 * W + 2.9755e – 02 * B + 3.4939e – 01 – 1.2733e – 06 * W * B) * VDD^2 * F
	Y = 16
power_ck	(7.8633e – 03 * W + 1.7350 * B + 5.5361 + 1.7510e – 03 * W * B) * VDD^2 * F
power_csn	(6.1769e – 06 * W + 5.9511e – 02 * B + 3.4939e – 01 – 1.2733e – 06 * W * B) * VDD^2 * F
	Y = 32
power_ck	(4.0198e – 03 * W + 3.7202 * B + 5.2484 + 1.7655e – 03 * W * B) * VDD^2 * F
power_csn	(3.0884e – 06 * W + 1.1902e – 01 * B + 3.4939e – 01 – 1.2733e – 06 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

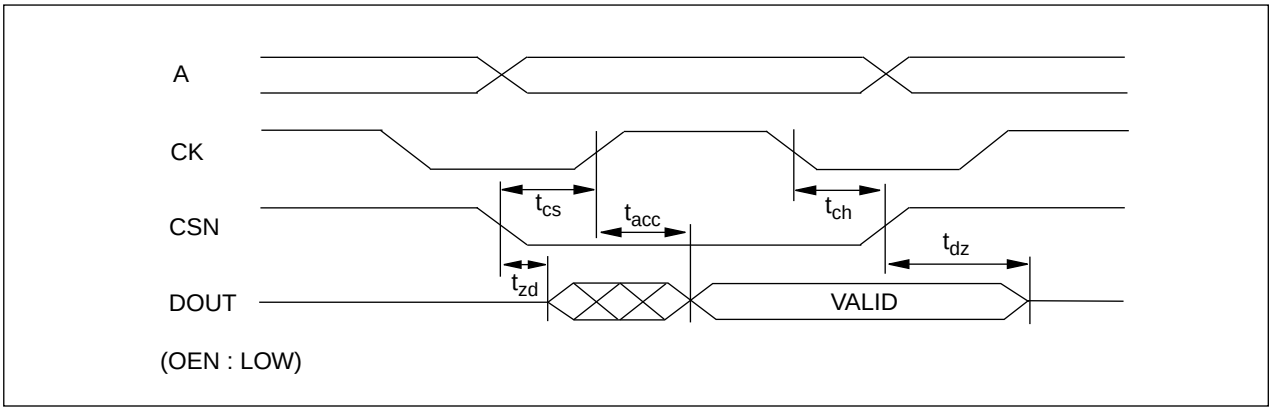
Width = 10.2 * ($\lceil \log_2 (W / Y) \rceil$) + 164.8 * BA + 2.5843 (B * Y) + 8.2 [μm]
Height = 225.1 + 2.30 * W / Y + M [μm]
M = 6.05 (if Y = 8), M = 8.45 (if Y = 16), M = 10.85 (if Y = 32)

Timing Diagrams

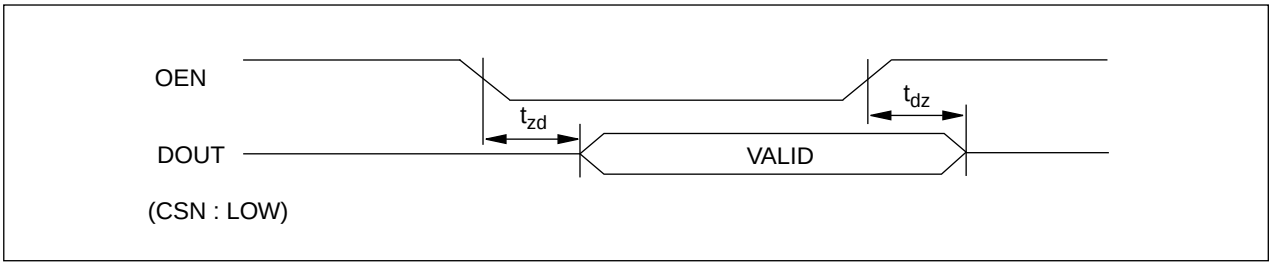
Read Cycle



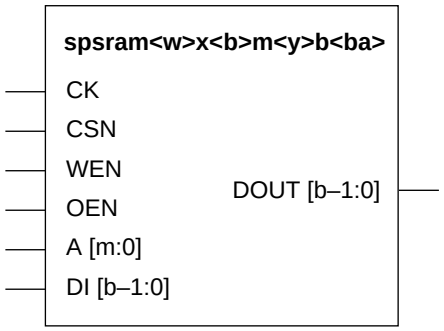
CSN Control



OEN Control



Logic Symbol



NOTES:

1. Words (w) is the number of words in SPSRAM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Write completed at rising edge of clock
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 128K bits capacity
- Up to 8K number of words
- Up to 256 number of bits per word

Function Description

SPSRAM is a single-port synchronous static RAM. When CK rises, if WEN is high, DOUT [ ] presents data stored in the location addressed by A [ ], otherwise the value of DI [ ] is written into the location addressed by A [ ]. CSN is used to enable/disable the clock. OEN is used to enable/disable the data output driver.

Generators and Cell Configurations

SPSRAM Gen. generates layout, netlist, symbol and functional & timing model of SPSRAM. The layout of SPSRAM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of SPSRAM, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	4	8	16	32	64
		Max	512	1024	2048	4096	8192
		Step	2	4	8	16	32
Bpw (b)	ba = 1	Min	1	1	1	1	1
		Max	128	64	32	16	8
		Step	1	1	1	1	1
	ba = 2	Min	2	2	2	2	2
		Max	256	128	64	32	16
		Step	1	1	1	1	1

SPSRAM Gen

Single-Port Synchronous RAM Generator

Pin Descriptions

Name	I/O	Description
CK	I	“Clock” serves as the input clock to the memory block. When CK is low, the memory is in a precharge state. Upon the rising edge, an access begins.
CSN	I	“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read or write access occur. CSN may not change during CK is high.
WEN	I	“Write Enable Negative” selects the type of memory access. Read is the high state, and write is the low state.
OEN	I	“Output Enable Negative” controls the output drivers from driven to tri-state condition. OEN may not change during CK is high.
A [ ]	I	“Address” selects the location to be accessed. A [ ] may not change during CK is high.
DI [ ]	I	When CK rises while WEN is low, the “Data In” word value is written to the accessed location.
DOUT [ ]	O	During a read access, data word stored will be presented to the “Data Out” ports. DOUT [ ] is tri-statable. When CK is high, CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state. During a write access, data word written will be presented at the “Data Out” ports if output driver is enabled.

Pin Capacitance

(Unit = SL)

	CK	CSN	WEN	OEN	A	DI	DOUT				
							Ymux 2	Ymux 4	Ymux 8	Ymux 16	Ymux 32
1-bank	3.5	1.0	0.5	1.6	1.2	2.1	3.1	3.3	7.7	15.0	31.0
2-bank	7.0	2.1	1.0	3.1	1.2	2.1	3.1	3.3	7.7	15.0	31.0

Application Notes

1) Putting Busholders on DOUT [ ]

As you will see in the timing diagrams, DOUT [ ] is valid only when CK is high. If you want DOUT [ ] to be stable regardless of CK state, you should put STD80/STDM80 Busholder cells on the DOUT [ ] bus externally.

2) Customizing Aspect Ratio

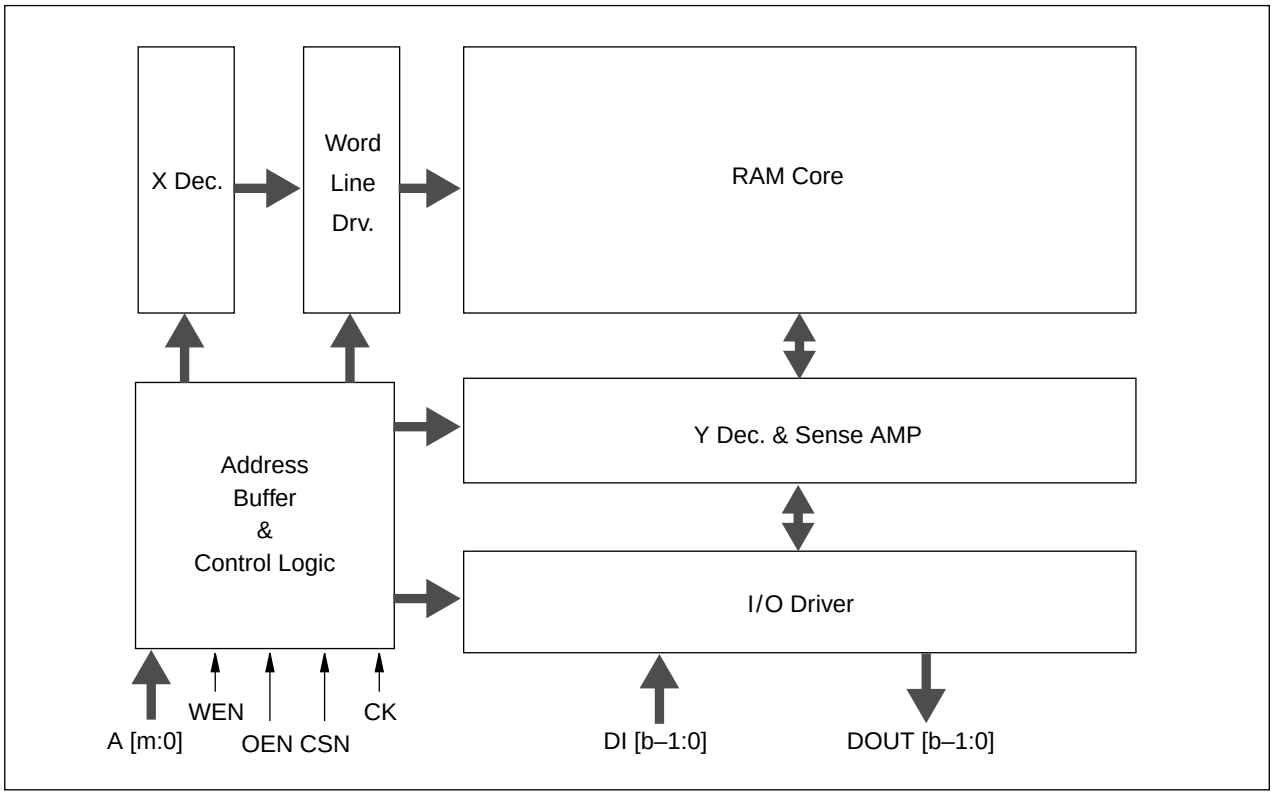
Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 5 selections of Ymux for the same Words and the same Bpw SPSRAM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of SPSRAM, In general, larger Ymux SPSRAM has faster speed and bigger area than smaller Ymux SPSRAM.

3) Selecting Number of Banks

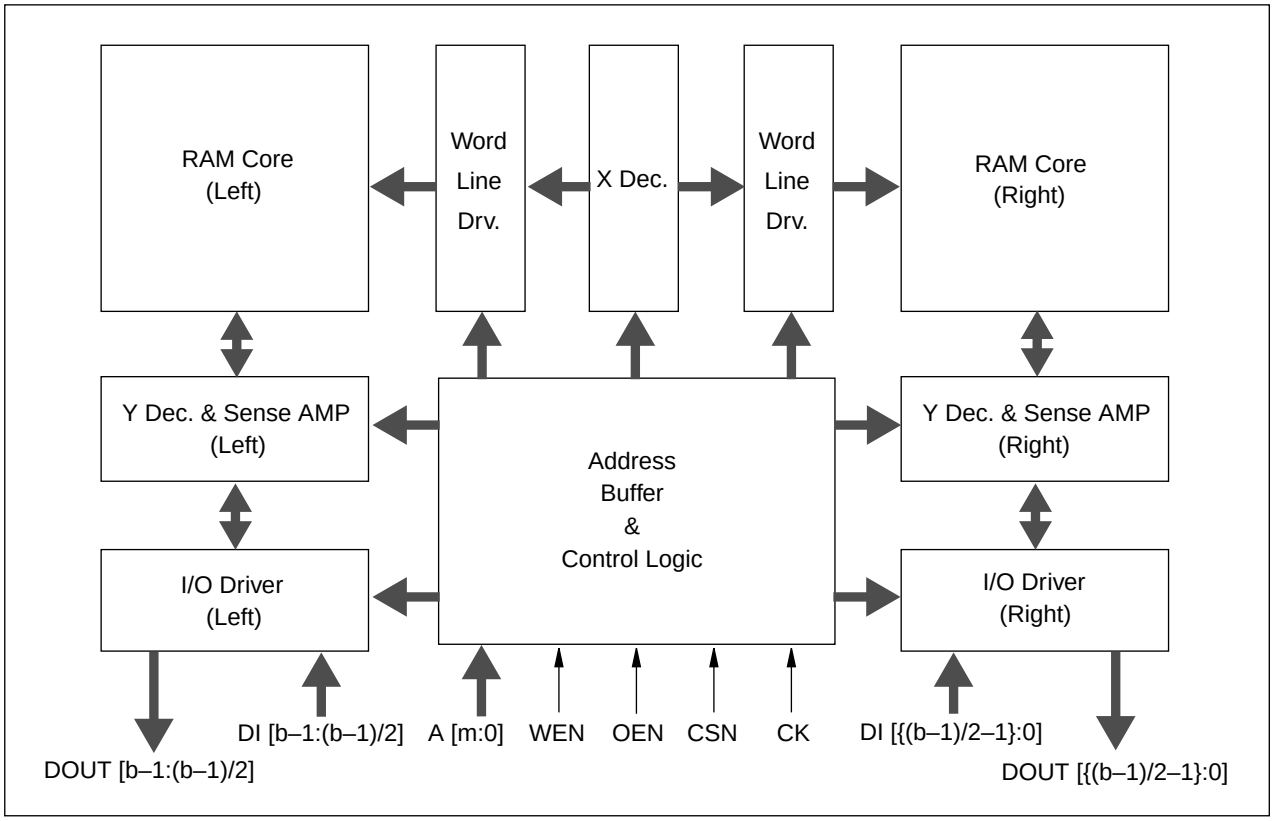
To enlarge the capacity of SPSRAM, we added one more option to choose number of banks. If you want to use larger SPSRAM than 64K bit SPSRAM, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 64K bit SPSRAM. Dual bank SPSRAM is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

Block Diagrams

< 1-bank >



< 2-bank >



Characteristic Reference Table

STD80

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 5V, 25 ^{o}C, Output load = 10SL, Unit = ns)							
minckl	Minimum Clock Pulse Width Low	2.00	1.90	2.40	2.30	3.17	2.90
minckh	Minimum Clock Pulse Width High	5.60	5.60	5.90	5.80	6.56	6.45
t_{as}	Address Setup Time	0.36	0.38	0.59	0.56	1.10	0.98
t_{ah}	Address Hold Time	0.34	0.34	0.39	0.46	0.50	0.63
t_{cs}	CSN Setup Time	0.51	0.51	0.51	0.51	0.51	0.51
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{ds}	Data Input Setup Time	0	0	0	0	0	0
t_{dh}	Data Input Hold Time	2.90	2.70	3.60	3.30	5.00	4.40
t_{os}	OEN Setup Time	0	0	0	0	0	0
t_{oh}	OEN Hold Time	1.30	1.30	1.50	1.50	2.00	1.80
t_{ws}	WEN Setup Time	0	0	0	0	0	0
t_{wh}	WEN Hold Time	0	0	0	0	0	0
t_{acc}	Access Time	2.95	2.86	3.50	3.30	4.60	4.24
t_{da}	Deaccess Time	2.10	2.00	2.20	2.10	2.50	2.20
mincyc	Minimum Clock Cycle Time	7.85	7.70	8.90	8.60	11.00	10.10
SIZE (μm)							
Width		622	703	1131	1212	2142	2222
Height		902	902	1501	1501	2697	2697
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)			1261		2412		5150
power_csn (stand-by mode: CSN High)			107		155		300

Characteristic Reference Table (Cont.)

STDM80

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)							
minckl	Minimum Clock Pulse Width Low	2.80	2.70	3.40	3.20	4.50	4.10
minckh	Minimum Clock Pulse Width High	8.40	8.40	8.80	8.80	9.40	9.50
t_{as}	Address Setup Time	0.40	0.40	0.68	0.65	1.40	1.20
t_{ah}	Address Hold Time	0.36	0.40	0.40	0.40	0.60	0.60
t_{cs}	CSN Setup Time	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{ds}	Data Input Setup Time	0	0	0	0	0	0
t_{dh}	Data Input Hold Time	4.00	3.80	4.90	4.50	6.70	5.90
t_{os}	OEN Setup Time	0	0	0	0	0	0
t_{oh}	OEN Hold Time	2.00	2.00	2.30	2.20	2.70	2.60
t_{ws}	WEN Setup Time	0	0	0	0	0	0
t_{wh}	WEN Hold Time	0	0	0	0	0	0
t_{acc}	Access Time	4.30	4.20	5.10	4.80	6.70	6.10
t_{da}	Deaccess Time	2.80	2.70	3.00	2.80	3.40	3.00
mincyc	Minimum Clock Cycle Time	11.50	11.20	13.20	12.60	16.50	15.40
SIZE (μm)							
Width		622	703	1131	1212	2142	2222
Height		902	902	1501	1501	2697	2697
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)			529		1063		2395
power_csn (stand-by mode: CSN High)			52		92		163

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
B: Bits per Word
Y: Ymux Type
BA: Number of Banks (1 or 2)
S: Input Slope (Unit: ns)
SL: Number of Fanouts (Unit: Standard Load)
VDD: Operating Voltage (Unit: V)
F: Operating Frequency (Unit: MHz)

STD80

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
minckh	(2.0583e – 03 * W + 1.8220e – 03 * B / BA + 1.2739 * 0.019 * SL + 1.6496)
minckl	(1.9900e – 03 * W + 3.8135e – 03 * B / BA + 1.6302 + 6.2396e – 07 * W * B / BA)
mincyc	(5.4783e – 03 * W + 8.6924e – 03 * B / BA + 1.0451 * 0.019 * SL + 3.3130) * 1.08
tacc	(2.8771e – 03 * W + 5.6933e – 03 * B / BA + 9.7039e – 02 * S + 5.6468e – 01 * 0.019 * SL + 2.1791)
	Y = 4
minckh	(1.0291e – 03 * W + 3.6440e – 03 * B / BA + 1.2739 * 0.019 * SL + 1.6496)
minckl	(9.9503e – 04 * W + 7.6271e – 03 * B / BA + 1.6302 + 6.2396e – 07 * W * B / BA)
mincyc	(2.7391e – 03 * W + 1.7384e – 02 * B / BA + 1.0451 * 0.019 * SL + 3.3130) * 1.08
tacc	(1.4385e – 03 * W + 1.1386e – 02 * B / BA + 9.7039e – 02 * S + 5.6468e – 01 * 0.019 * SL + 2.1791)
	Y = 8
minckh	(5.1457e – 04 * W + 7.2880e – 03 * B / BA + 1.2739 * 0.019 * SL + 1.6496)
minckl	(4.9751e – 04 * W + 1.5254e – 02 * B / BA + 1.6302 + 6.2396e – 07 * W * B / BA)
mincyc	(1.3695e – 03 * W + 3.4769e – 02 * B / BA + 1.0451 * 0.019 * SL + 3.3130) * 1.08
tacc	(7.1928e – 04 * W + 2.2773e – 02 * B / BA + 9.7039e – 02 * S + 5.6468e – 01 * 0.019 * SL + 2.1791)
	Y = 16
minckh	(2.5728e – 04 * W + 1.4576e – 02 * B / BA + 1.2739 * 0.019 * SL + 1.6496)
minckl	(2.4875e – 04 * W + 3.0508e – 02 * B / BA + 1.6302 + 6.2396e – 07 * W *B / BA)
mincyc	(6.8479e – 04 * W + 6.9539e – 02 * B / BA + 1.0451 * 0.019 * SL + 3.3130) * 1.08
tacc	(3.5964e – 04 * W + 4.5547e – 02 * B / BA + 9.7039e – 02 * S + 5.6468e – 01 * 0.019 * SL + 2.1791)
	Y = 32
minckh	(1.2864e – 04 * W + 2.9152e – 02 * B / BA + 1.2739 * 0.019 * SL + 1.6496)
minckl	(1.2437e – 04 * W + 6.1017e – 02 * B / BA + 1.6302 + 6.2394e – 07 * W * B / BA)
mincyc	(3.4239e – 04 * W +1.3907e – 01 * B / BA + 1.0451 * 0.019 * SL + 3.3130) * 1.08
tacc	(1.7982e – 04 * W + 9.1094e – 02 * B / BA + 9.7039e – 02 * S + 5.6468e – 01 * 0.019 * SL + 2.1791)

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 2
power_ck	(1.3452e – 01 * W + 9.8737e – 01 * B + 1.9854 + 2.5351e – 03 * W * B) * VDD^2 * F
power_csn	(8.8861e – 03 * W + 1.3209e – 01 * B + 1.1430e – 01 – 2.8037e – 04 * W * B) * VDD^2 * F
	Y = 4
power_ck	(6.9202e – 02 * W + 1.4519 * B + 3.0524 + 1.5738e – 03 * W * B) * VDD^2 * F
power_csn	(4.4430e – 03 * W + 2.6419e – 01 * B + 1.1430e – 01 – 2.8037e – 04 * W * B) * VDD^2 * F
	Y = 8
power_ck	(3.3665e – 02 * W + 2.2848 * B + 3.6310 + 1.3354e – 03 * W * B) * VDD^2 * F
power_csn	(2.2215e – 3 * W + 5.2839e – 01 * B + 1.1430e – 01 – 2.8037e – 04 * W * B) * VDD^2 * F
	Y = 16
power_ck	(1.6925e – 02 * W + 4.0510 * B + 3.4129 + 1.0574e – 03 * W * B) * VDD^2 * F
power_csn	(1.1107e – 03 * W + 1.0567 * B + 1.1430e – 01 – 2.8037e – 04 * W * B) * VDD^2 * F
	Y = 32
power_ck	(8.4295e – 03 * W + 7.5842 * B + 2.9152 + 9.5723e – 04 * W * B) * VDD^2 * F
power_csn	(5.5538e – 04 * W + 2.1135 * B + 1.1430e – 01 – 2.8037e – 04 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 6 * ($\lceil \log2 (W / Y) \rceil$) + 76.3 * BA + 4.4 (B * Y / 4 + BA) + 6.75 * B * Y + 2.25 [μm]
Height = 297.5 + 9.35 * W / Y + M [μm]
M = 5.75 (if Y = 2, 4, 8, 16), M = 8.15 (if Y = 32)

STDM80

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
minckh	(2.7855e – 03 * W + 2.7711e – 03 * B / BA + 1.7719 * 0.019 * SL + 3.0534 – 1.2983e – 03 * B / BA * 0.019 * SL)
minckl	(2.9979e – 03 * W + 5.1004e – 03 * B / BA + 2.2601 – 5.1494e – 09 * B / BA * W)
mincyc	(8.1165e – 03 * W + 1.6054e – 02 * B / BA + 1.4542 * 0.019 * SL + 4.9456) * 1.08
tacc	(3.9714e – 03 * W + 7.8602e – 03 * B /BA + 1.7038e – 01 * S + 7.1508e – 01 * 0.019 * SL + 3.1048)
	Y = 4
minckh	(1.3927e – 03 * W + 5.5423e – 03 * B /BA + 1.7719 * 0.019 * SL + 3.0534 – 2.5966e – 03 * B / BA * 0.019 * SL)
minckl	(1.4989e – 03 * W + 1.0200e – 02 * B / BA + 2.2601 – 5.1639e – 09 * B / BA * W)
mincyc	(4.0582e – 03 * W + 3.2109e – 02 * B / BA + 1.4542 * 0.019 * SL + 4.9456) * 1.08
tacc	(1.9857e – 03 * W + 1.5720e – 02 * B / BA + 1.7038e – 01 * S +7.1508e – 01 * 0.019 * SL + 3.1048)
	Y = 8
minckh	(6.9638e – 04 * W + 1.1084e – 02 * B / BA + 1.7719 * 0.019 * SL + 3.0534 – 5.1932e – 03 * B / BA * 0.019 * SL)
minckl	(7.4948e – 04 * W + 2.0401e – 02 * B / BA + 2.2601 – 5.1817e – 09 * B / BA * W)
mincyc	(2.0291e – 03 * W + 6.4219e – 02 * B / BA + 1.4542 * 0.019 * SL + 4.9456) * 1.08

Timing Type	Timing Equation
tacc	(9.9285e – 04 * W + 3.1441e – 02 * B / BA + 1.7038e – 01 * S + 7.1508e – 01 * 0.019 * SL+ 3.1048)
	Y = 16
minckh	(3.4819e – 04 * W + 2.2169e – 02 * B / BA + 1.7719 * 0.019 * SL + 3.0534 – 1.0386e – 02 * B / BA * 0.019 * SL)
minckl	(3.7474e – 04 * W + 4.0803e – 02 * B / BA + 2.2601 – 5.1761e – 09 * B / BA * W)
mincyc	(1.0145e – 03 * W + 1.2843e – 01 * B / BA + 1.4542 * 0.019 * SL + 4.9456) * 1.08
tacc	(4.9642e – 04 * W + 6.2882e – 02 * B / BA + 1.7038e – 01 * S + 7.1508e – 01 * 0.019 * SL + 3.1048)
	Y = 32
minckh	(1.7409e – 04 * W + 4.4338e – 02 * B / BA + 1.7719 * 0.019 * SL + 3.0534 – 2.0773e – 02 * B / BA * 0.019 * SL)
minckl	(1.8737e – 04 * W + 8.1606e – 02 * B / BA + 2.2601 – 5.1446e – 09 * B / BA * W)
mincyc	(5.0728e – 04 * W + 2.5687e – 01 * B / BA + 1.4542 * 0.019 * SL + 4.9456) * 1.08
tacc	(2.4821e – 04 * W + 1.2576e – 01 * B / BA + 1.7038e – 01 * S + 7.1508e – 01 * 0.019 * SL + 3.1048)

2) Power Characteristics [Unit: μW]

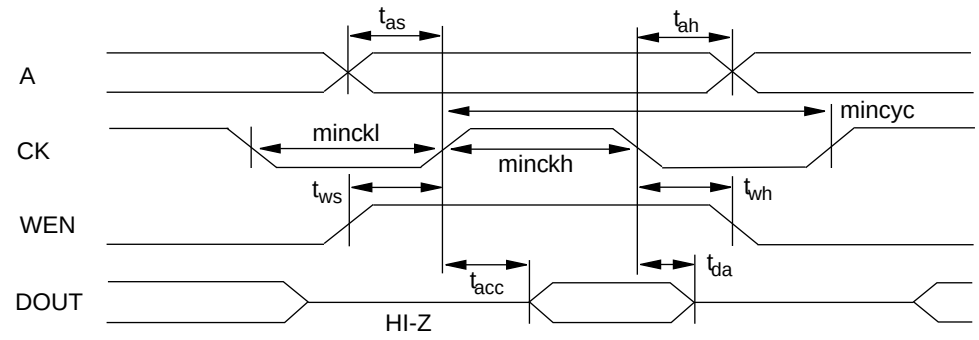
Power Type	Power Equation
	Y = 2
power_ck	(1.3167e – 01 * W + 7.9148e – 01 * B + 1.7625 + 1.1349e – 03 *W * B) * VDD^2 * F
power_csn	(3.1611e – 03 * W + 1.2166e – 01 * B + 6.3691e – 01 – 4.2817e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(6.5837e – 02 * W + 1.5829 * B + 1.7625 + 1.1349e – 03 * W * B) * VDD^2 * F
power_csn	(1.5805e – 03 * W + 2.4333e – 01 * B + 6.3691e – 01 – 4.2817e – 05 * W * B) * VDD^2 * F
	Y = 8
power_ck	(3.0498e – 02 * W + 2.4446 * B + 4.0763 + 1.4227e – 03 * W * B) * VDD^2 * F
power_csn	(7.9029e – 04 * W + 4.8667e – 01 * B + 6.3691e – 01 – 4.2817e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(1.5183e – 02 * W + 4.0522 * B + 4.5947 + 1.34e – 03 * W * B) * VDD^2 * F
power_csn	(3.9514e – 04 * W + 9.7335e – 01 * B + 6.3691e – 01 – 4.2817e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(7.8479e – 03 * W + 8.1911 * B + 3.4364 + 1.0426e – 03 * W * B) * VDD^2 * F
power_csn	(1.9757e – 04 * W + 1.9467 * B + 6.3691e – 01 – 4.2817e – 05 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 6 * ($\lceil \log2 (W / Y) \rceil$) + 76.3 * BA + 4.4 (B * Y / 4 + BA) + 6.75 * B * Y + 2.25 [μm]
Height = 297.5 + 9.35 * W / Y + M [μm]
M = 5.75 (if Y = 2, 4, 8, 16), M = 8.15 (if Y = 32)

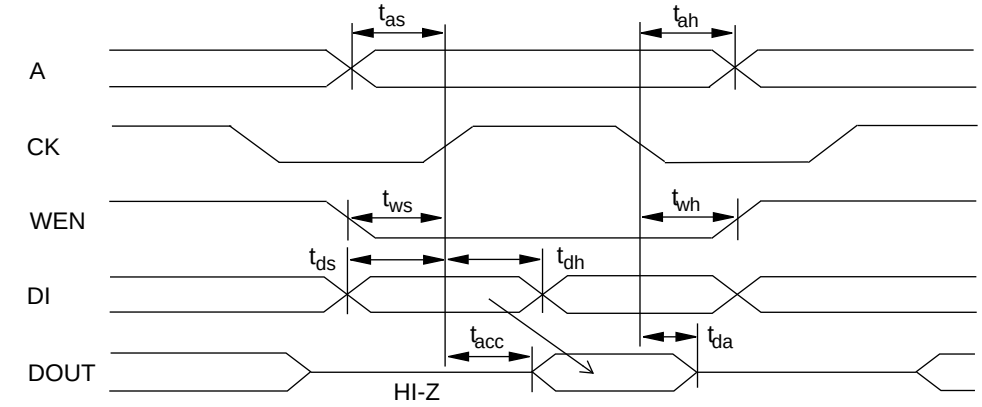
Timing Diagrams

Read Cycle



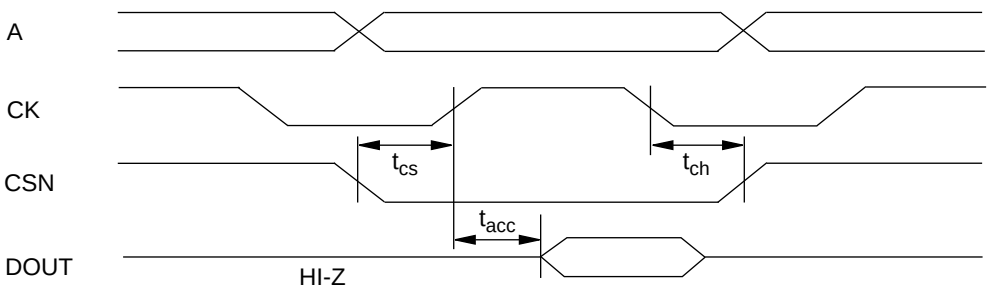
(CSN / OEN : LOW)

Write Cycle



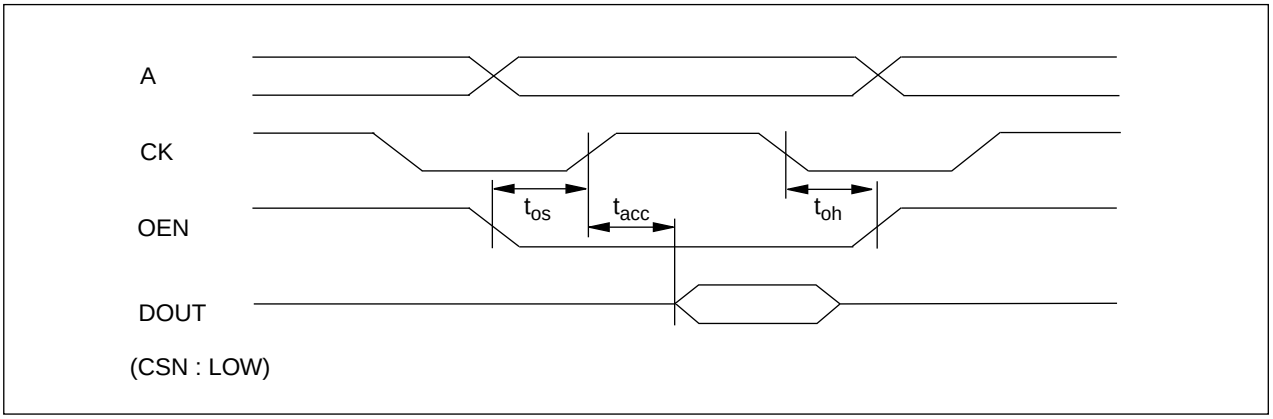
(CSN / OEN : LOW)

CSN Control

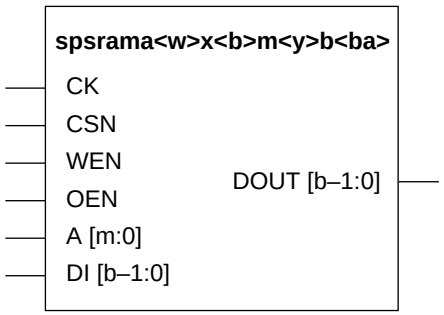


(OEN : LOW)

OEN Control



Logic Symbol



NOTES:

1. Words (w) is the number of words in SPSRAMA.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Write completed at falling edge of clock
- Possible read modified write cycle
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Possible bi-directional operation
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 128K bits capacity
- Up to 8K number of words
- Up to 256 number of bits per word

Function Description

SPSRAMA is a single-port synchronous static RAM. When WEN is high and CK rises, DOUT [ ] presents data stored in the location addressed by A [ ]. When WEN is low and CK falls, or when CK is high and WEN rises, the value of DI [ ] is written into the location addressed by A [ ]. CSN is used to enable/disable the clock. OEN is used to enable/disable the data output driver.
SPSRAMA is an alternative of SPSRAM. The major difference of these two RAMs is the timing of read and write. SPSRAMA reads and writes at different edge of the clock since SPSRAM reads and writes at the same edge of the clock.

Generators and Cell Configurations

SPSRAMA Gen. generates layout, netlist, symbol and functional & timing model of SPSRAMA. The layout of SPSRAMA is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of SPSRAMA, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	4	8	16	32	64
		Max	512	1024	2048	4096	8192
		Step	2	4	8	16	32
Bpw (b)	ba = 1	Min	1	1	1	1	1
		Max	128	64	32	16	8
		Step	1	1	1	1	1
	ba = 2	Min	2	2	2	2	2
		Max	256	128	64	32	16
		Step	1	1	1	1	1

Pin Descriptions

Name	I/O	Description
CK	I	“Clock” serves as the input clock to the memory block. When CK is low, the memory is in a precharge state. Upon the rising edge, a read cycle begins. Upon the falling edge, a write cycle ends.
CSN	I	“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read or write access occur. CSN may not change during CK is high.
WEN	I	“Write Enable Negative” selects the type of memory access. Read is the high state, and write is the low state. When WEN rises while CK is high, a write cycle ends.
OEN	I	“Output Enable Negative” controls the output drivers from driven to tri-state condition. OEN may not change during CK is high.
A [ ]	I	“Address” selects the location to be accessed. A [ ] may not change during CK is high.
DI [ ]	I	When CK falls while WEN is low, or when WEN rises while CK is high, the “Data In” word value is written to the accessed location.
DOUT [ ]	O	During a read access, data word stored will be presented to the “Data Out” ports. DOUT [ ] is tri-statable. When CK is high, CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state. During a write access, the value of DOUT [ ] is unpredictable.

Pin Capacitance

(Unit = SL)

	CK	CSN	WEN	OEN	A	DI	DOUT				
							Ymux 2	Ymux 4	Ymux 8	Ymux 16	Ymux 32
1-bank	3.5	1.0	0.5	1.6	1.2	2.1	3.1	3.3	7.7	15.0	31.0
2-bank	7.0	2.1	1.0	3.1	1.2	2.1	3.1	3.3	7.7	15.0	31.0

Application Notes

1) Putting Busholders on DOUT [ ]

As you will see in the timing diagrams, DOUT [ ] is valid only when CK is high. If you want DOUT [ ] to be stable regardless of CK state, you should put STD80/STDM80 Busholder cells on the DOUT [ ] bus externally.

2) Customizing Aspect Ratio

Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 5 selections of Ymux for the same Words and the same Bpw SPSRAMA. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of SPSRAM, In general, larger Ymux SPSRAMA has faster speed and bigger area than smaller Ymux SPSRAMA.

3) Selecting Number of Banks

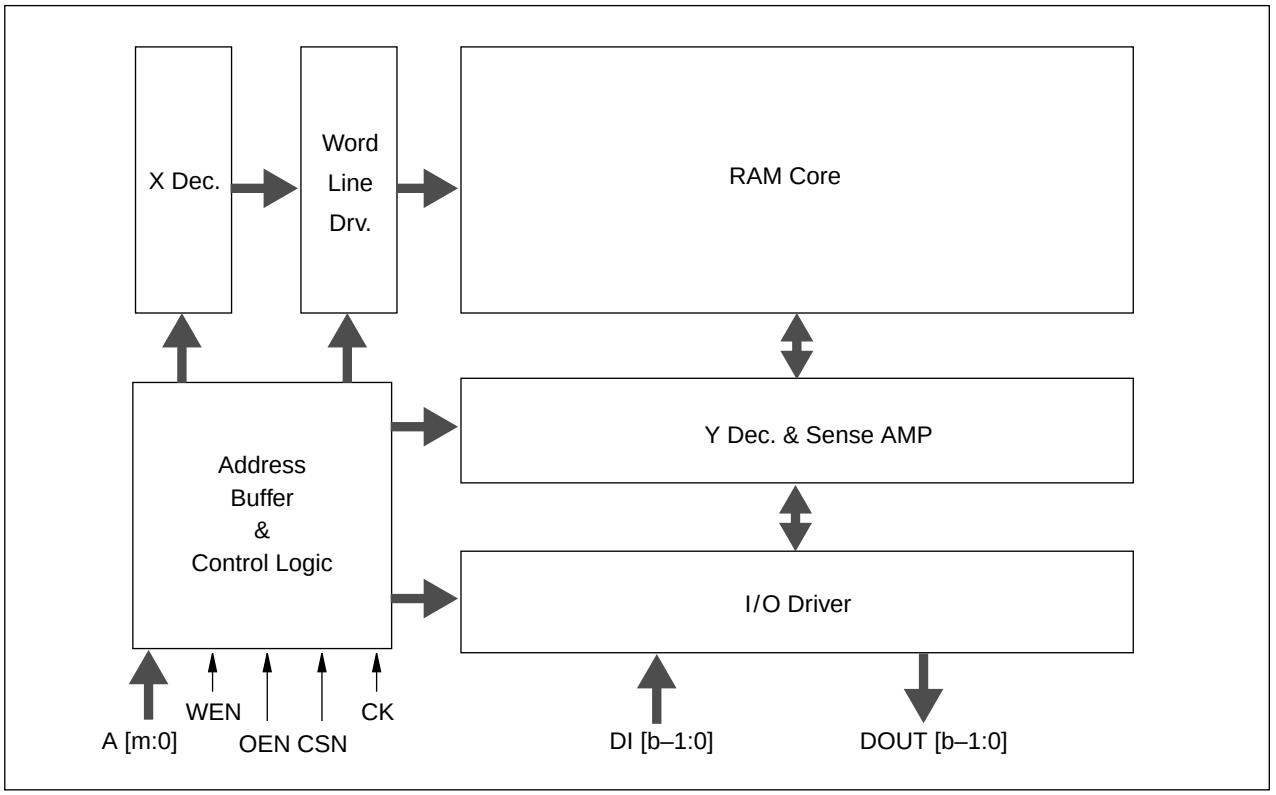
To enlarge the capacity of SPSRAMA, we added one more option to choose number of banks. If you want to use larger SPSRAMA than 64K bit SPSRAMA, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 64K bit SPSRAMA. Dual bank SPSRAMA is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

4) Using Bi-Directional Data Port

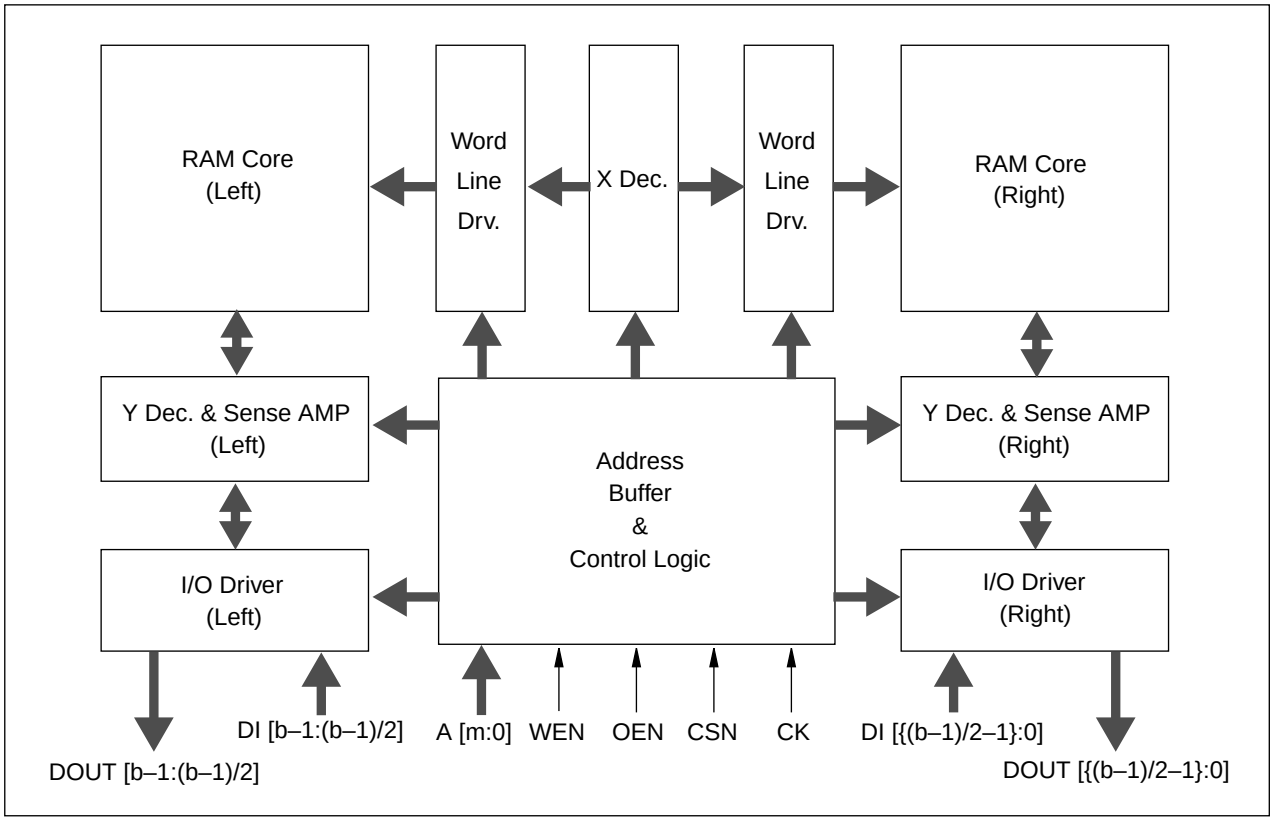
Because having the same phase, DI [ ] and DOUT [ ] of SPSRAMA can be tied directly. With tying them up together and controlling WEN and OEN properly, you can use them as bi-directional data ports.

Block Diagrams

< 1-bank >



< 2-bank >



Characteristic Reference Table

STD80

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2--ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 5V, 25 ^{o}C, Output load = 10SL, Unit = ns)							
t_{rp}	Minimum Read Pulse Width	6.35	6.28	6.87	6.72	7.91	7.61
t_{pc}	Minimum Pre-Charge Period	2.56	2.25	3.64	3.20	5.78	4.90
t_{wp}	Minimum Write Pulse Width	1.13	1.16	1.40	1.40	1.95	2.00
t_{as}	Address Setup Time	0.45	0.44	0.68	0.68	0.98	1.00
t_{ah}	Address Hold Time	0.83	0.77	1.16	1.00	1.82	1.57
t_{cs}	CSN Setup Time	0.37	0.37	0.37	0.37	0.37	0.37
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{ds}	Data Input Setup Time	0.69	0.76	0.86	0.98	1.19	1.44
t_{dh}	Data Input Hold Time	1.67	1.52	1.99	1.69	2.61	2.01
t_{os}	OEN Setup Time	0	0	0	0	0	0
t_{oh}	OEN Hold Time	1.25	1.21	1.44	1.37	1.83	1.67
t_{wh}	WEN Hold Time	0.71	0.70	0.73	0.71	0.76	0.72
t_{acc}	Access Time	4.60	4.50	5.10	5.00	6.27	5.90
t_{da}	Deaccess Time	1.90	1.70	2.10	1.90	2.30	1.90
SIZE (μm)							
Width		622	703	1131	1212	2142	2222
Height		902	902	1501	1501	2697	2697
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)		1416		3575		9673	
power_csn (stand-by mode: CSN High)		102		191		385	

Characteristic Reference Table (Cont.)

STDM80

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)							
t_{rp}	Minimum Read Pulse Width	9.37	9.30	10.00	9.80	11.40	11.0
t_{pc}	Minimum Pre-Charge Period	3.58	3.30	5.10	5.10	8.10	7.00
t_{wp}	Minimum Write Pulse Width	1.63	1.63	2.06	2.10	2.90	3.00
t_{as}	Address Setup Time	0.54	0.54	0.82	0.83	1.29	1.37
t_{ah}	Address Hold Time	0.17	1.10	1.48	1.33	2.10	1.80
t_{cs}	CSN Setup Time	0.55	0.55	0.55	0.55	0.55	0.55
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{ds}	Data Input Setup Time	0.82	0.90	1.14	1.33	1.75	2.10
t_{dh}	Data Input Hold Time	2.25	2.00	2.65	2.20	3.45	2.60
t_{os}	OEN Setup Time	0	0	0	0	0	0
t_{oh}	OEN Hold Time	1.83	1.79	2.00	1.90	2.36	2.21
t_{wh}	WEN Hold Time	0.91	0.90	0.93	0.91	0.98	0.93
t_{acc}	Access Time	6.50	5.30	7.30	7.00	8.98	8.35
t_{da}	Deaccess Time	2.60	2.30	2.80	2.40	3.20	2.60
SIZE (µm)							
Width		622	703	1131	1212	2142	2222
Height		902	902	1501	1501	2697	2697
POWER (µW/MHz)							
power_ck (normal mode: CSN Low)		685		1718		4867	
power_csn (stand-by mode: CSN High)		46		88		180	

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
B: Bits per Word
Y: Ymux Type
BA: Number of Banks (1 or 2)
S: Input Slope (Unit: ns)
SL: Number of Fanouts (Unit: Standard Load)
VDD: Operating Voltage (Unit: V)
F: Operating Frequency (Unit: MHz)

STD80

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
tpc	5.05e – 03 * W + 1.32e – 02 * B / BA + 3.12e – 01 * S + 1.1222
trp	2.88e – 03 * W + 4.63e – 03 * B / BA – 2.55e – 01 * S + 1.4029 * 0.019 * SL + 2.1511
tacc	2.94e – 03 * W + 5.16e – 03 * B / BA + 6.26e – 01 * 0.019 * SL + 2.2007 + 8.28e – 07 * W * B / BA + 1.79e – 05 * W * 0.019 * SL – 1.39e – 04 * B / BA * 0.019 * SL
	Y = 4
tpc	2.52e – 03 * W + 2.65e – 02 * B / BA + 3.12e – 01 * S + 1.1222
trp	1.44e – 03 * W + 9.26e – 03 * B / BA – 2.55e – 01 * S + 1.4029 * 0.019 * SL + 2.1511
tacc	1.47e – 03 * W + 1.03e – 02 * B / BA + 6.26e – 01 * 0.019 * SL + 2.2007 + 8.28e – 07 * W * B / BA + 8.97e – 06 * W * 0.019 * SL – 2.78e – 04 * B / BA * 0.019 * SL
	Y = 8
tpc	1.26e – 03 * W + 5.31e – 02 * B / BA + 3.12e – 01 * S + 1.1222
trp	7.20e – 04 * W + 1.85e – 02 * B / BA – 2.55e – 01 * S + 1.4029 * 0.019 * SL + 2.1511
tacc	7.36e – 04 * W + 2.06e – 02 * B / BA + 6.26e – 01 * 0.019 * SL + 2.2007 + 8.28e – 07 * W * B / BA + 4.48e – 06 * W * 0.019 * SL – 5.57e – 04 * B / BA * 0.019 * SL
	Y = 16
tpc	6.31e – 04 * W + 1.06e – 01 * B / BA + 3.12e – 01 * S + 1.1222
trp	3.60e – 04 * W + 3.70e – 02 * B / BA – 2.55e – 01 * S + 1.4029 * 0.019 * SL + 2.1511
tacc	3.68e – 04 * W + 4.13e – 02 * B / BA + 6.26e – 01 * 0.019 * SL + 2.2007 + 8.28e – 07 * W * B / BA + 2.24e – 06 * W * 0.019 * SL – 1.11e – 03 * B / BA * 0.019 * SL
	Y = 32
tpc	3.15e – 04 * W + 2.12e – 01 * B / BA + 3.12e – 01 * S + 1.1222
trp	1.80e – 04 * W + 7.41e – 02 * B / BA – 2.55e – 01 * S + 1.4029 * 0.019 * SL + 2.1511
tacc	1.84e – 04 * W + 8.26e – 02 * B / BA + 6.26e – 01 * 0.019 * SL + 2.2007 + 8.28e – 07 * W * B / BA + 1.12e – 06 * W * 0.019 * SL – 2.23e – 03 * B / BA * 0.019 * SL

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 2
power_ck	(1.8029e – 01 * W + 8.6499e – 01 * B – 5.9569 + 2.8970e – 03 * W * B) * VDD^2 * F
power_csn	(3.2494e – 03 * W + 8.7595e – 02 * B + 7.7824e – 01 + 2.6855e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(9.0149e – 02 * W + 1.7299 * B – 5.9569 + 2.8970e – 03 * W * B) * VDD^2 * F
power_csn	(1.6247e – 03 * W + 1.7519e – 01 * B + 7.7824e – 01 + 2.6855e – 05 * W * B) * VDD^2 * F

Power Type	Power Equation
	Y = 8
power_ck	(4.5074e – 02 * W + 3.4599 * B – 5.9569 + 2.8970e – 03 * W * B) * VDD^2 * F
power_csn	(8.1236e – 04 * W + 3.5038e – 01 * B + 7.7824e – 01 + 2.6855e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(2.2537e – 02 * W + 6.9199 * B – 5.9569 + 2.8970e – 03 * W * B) * VDD^2 * F
power_csn	(4.0618e – 04 * W + 7.0076e – 01 * B + 7.7824e – 01 + 2.6855e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(1.1268e – 02 * W + 1.3839e + 01 * B – 5.9569 + 2.8970e – 03 * W * B) * VDD^2 * F
power_csn	(2.0309e – 04 * W + 1.4015 * B + 7.7824e – 01 + 2.6855e – 05* W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 6 * ($\lceil \log_2 (W / Y) \rceil$) + 76.3 * BA + 4.4 (B * Y / 4 + BA) + 6.75 * B * Y + 2.25 [μm]
Height = 297.5 + 9.35 * W / Y + M [μm]
M = 5.75 (if Y = 2, 4, 8, 16), M = 8.15 (if Y = 32)

STDM80

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
tpc	7.56e – 03 * W + 1.75e – 02 * B / BA + 4.15e – 01 * S + 1.5587
trp	3.66e – 03 * W + 3.61e – 03 * B / BA – 9.61e – 02 * S + 1.8958 * 0.019 * SL + 3.5506 + 9.78e – 06 * W * B / BA – 2.65e – 04 * W * S – 9.07e – 04 * B / BA * S + 3.97e – 05 * W * 0.019 * SL – 2.35e – 04 * B / BA * 0.019 * SL – 2.86e – 03 * S * 0.019 * SL
tacc	3.97e – 03 * W + 9.69e – 03 * B / BA + 8.90e – 01 * 0.019 * SL + 3.0333
	Y = 4
tpc	3.78e – 03 * W + 3.50e – 02 * B / BA + 4.15e – 01 * S + 1.5587
trp	1.83e – 03 * W + 7.22e – 03 * B / BA – 9.61e – 02 * S + 1.8958 * 0.019 * SL + 3.5506 + 9.78e – 06 * W * B / BA – 1.32e – 04 * W * S – 1.81e – 03 * B / BA * S + 1.98e – 05 * W * 0.019 * SL – 4.70e – 04 * B / BA * 0.019 * SL – 2.86e – 03 * S * 0.019 * SL
tacc	1.98e – 03 * W + 1.93e – 02 * B / BA + 8.90e – 01 * 0.019 * SL + 3.0333
	Y = 8
tpc	1.89e – 03 * W + 7.00e – 02 * B / BA + 4.15e – 01 * S + 1.5587
trp	9.15e – 04 * W + 1.44e – 02 * B / BA – 9.61e – 02 * S + 1.8958 * 0.019 * SL + 3.5506 + 9.79e – 06 * W * B / BA – 6.64e – 05 * W * S – 3.63e – 03 * B / BA * S + 9.92e – 06 * W * 0.019 * SL – 9.41e – 04 * B / BA * 0.019 * SL – 2.86e -03 * S * 0.019 * SL
tacc	9.93e – 04 * W + 3.87e – 02 * B / BA + 8.90e – 01 * 0.019 * SL + 3.0333
	Y = 16
tpc	9.46e – 04 * W + 1.40e – 01 * B / BA + 4.15e – 01 * S + 1.5587
trp	4.57e – 04 * W + 2.88e – 02 * B / BA – 9.61e – 02 * S + 1.8958 * 0.019 * SL + 3.5506 + 9.79e – 06 * W * B / BA – 3.32e – 05 * W * S – 7.26e – 03 * B / BA * S + 4.96e – 06 * W * 0.019 * SL – 1.88e – 03 * B / BA * 0.019 * SL – 2.86e – 03 * S * 0.019*SL
tacc	4.96e – 04 * W + 7.75e – 02 * B / BA + 8.90e – 01 * 0.019 * SL + 3.0333
	Y = 32
tpc	4.73e – 04 * W + 2.80e – 01 * B / BA + 4.15e – 01 * S + 1.5587

Timing Type	Timing Equation
trp	2.28e – 04 * W + 5.77e – 02 * B / BA – 9.61e – 02 * S + 1.8958 * 0.019 * SL + 3.5506 + 9.78e – 06 * W * B / BA – 1.66e – 05 * W * S – 1.45e – 02 * B / BA * S + 2.48e – 06 * W * 0.019 * SL – 3.76e – 03 * B / BA * 0.019 * SL – 2.86e – 03 * S * 0.019 * SL
tacc	2.48e – 04 * W + 1.55e – 01 * B / BA + 8.90e – 01 * 0.019 * SL + 3.0333

2) Power Characteristics [Unit: μW]

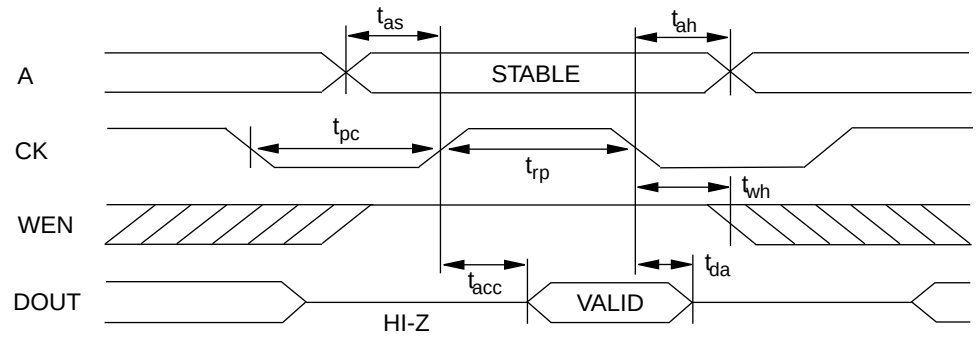
Power Type	Power Equation
	Y = 2
power_ck	(1.4598e – 01 * W + 8.2665e – 01 * B + 1.2695 + 4.0463e – 03 * W * B) * VDD^2 * F
power_csn	(3.1326e – 03 * W + 9.6584e – 02 * B + 6.3753e – 01 + 2.9811e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(7.2994e – 02 * W + 1.6533 * B + 1.2695 + 4.0463e – 03 * W * B) * VDD^2 * F
power_csn	(1.5663e – 03 * W + 1.9316e – 01 * B + 6.3753e – 01 + 2.9811e – 05 * W * B) * VDD^2 * F
	Y = 8
power_ck	(3.6497e – 02 * W + 3.3066 * B + 1.2695 + 4.0463e – 03 * W * B) * VDD^2 * F
power_csn	(7.8315e – 04 * W + 3.8633e – 01 * B + 6.3753e – 01 + 2.9811e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(1.8248e – 02 * W + 6.6132 * B + 1.2695 + 4.0463e – 03 * W * B) * VDD^2 * F
power_csn	(3.9157e – 04 * W + 7.7267e – 01 * B + 6.3753e – 01 + 2.9811e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(9.1243e – 03 * W + 1.3226e + 01 * B + 1.2695 + 4.0463e – 03 * W * B) * VDD^2 * F
power_csn	(1.9578e – 04 * W + 1.5453 * B + 6.3753e – 01 + 2.9811e – 05 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 6 * ($\lceil \log_2 (W / Y) \rceil$) + 76.3 * BA + 4.4 (B * Y / 4 + BA) + 6.75 * B * Y + 2.25 [μm]
Height = 297.5 + 9.35 * W / Y + M [μm]
M = 5.75 (if Y = 2, 4, 8, 16), M = 8.15 (if Y = 32)

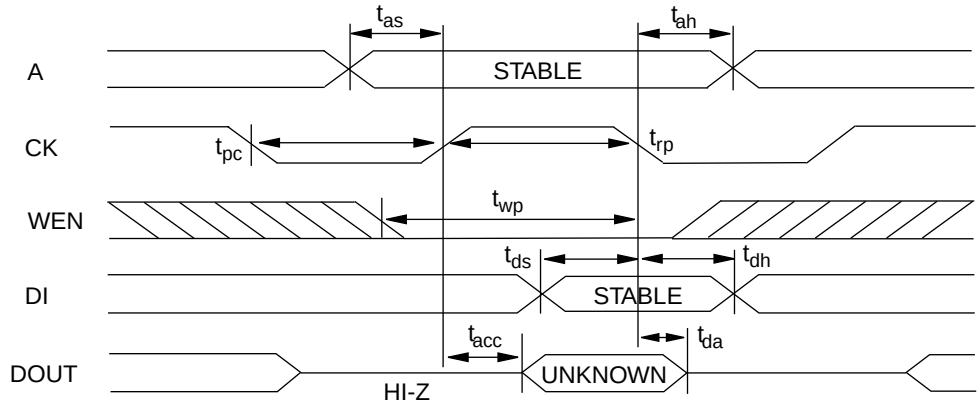
Timing Diagrams

Read Cycle



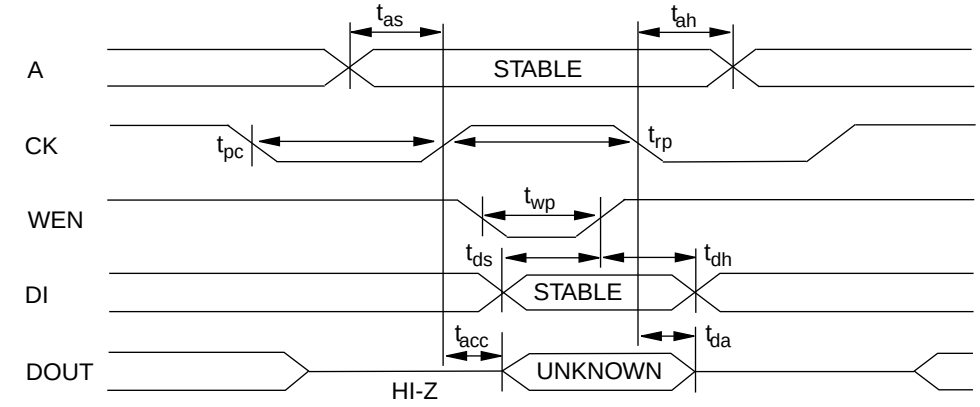
(CSN / OEN : LOW, DI :DON'T CARE)

CK Defined Write Cycle



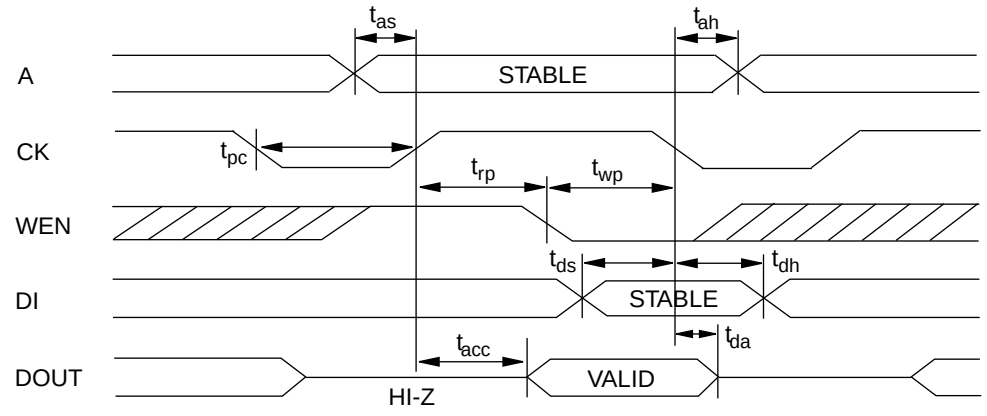
(CSN / OEN : LOW)

WEN Defined Write Cycle



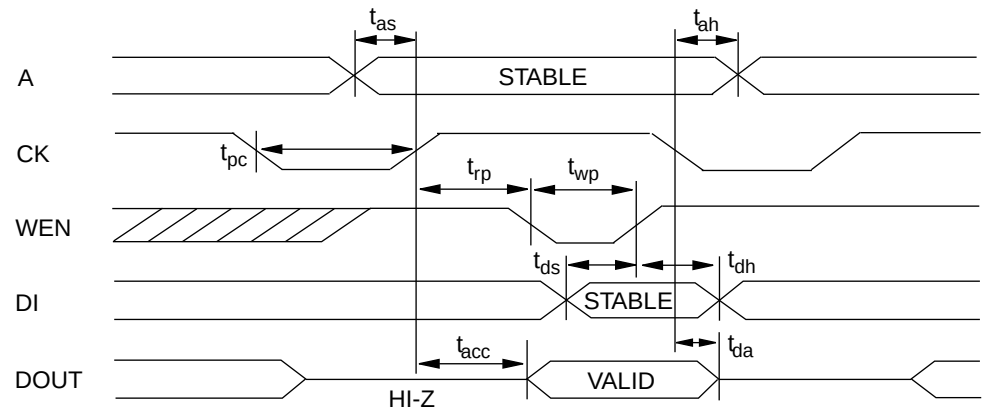
(CSN / OEN : LOW)

CK Defined Read-Modified-Write Cycle



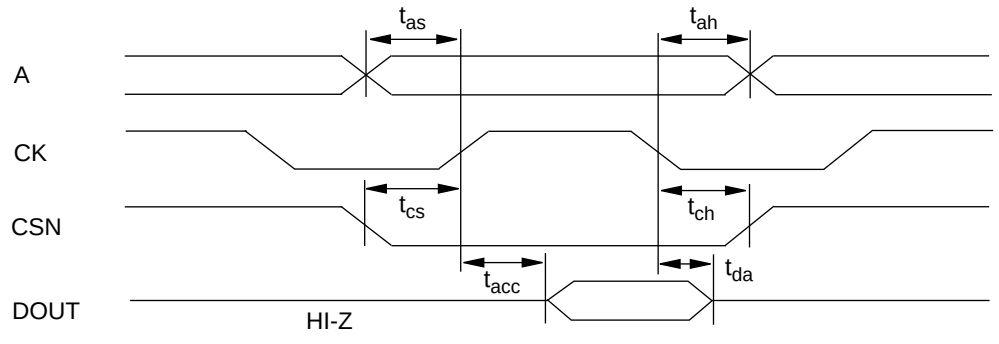
(CSN / OEN : LOW)

WEN Defined Read-Modified-Write Cycle



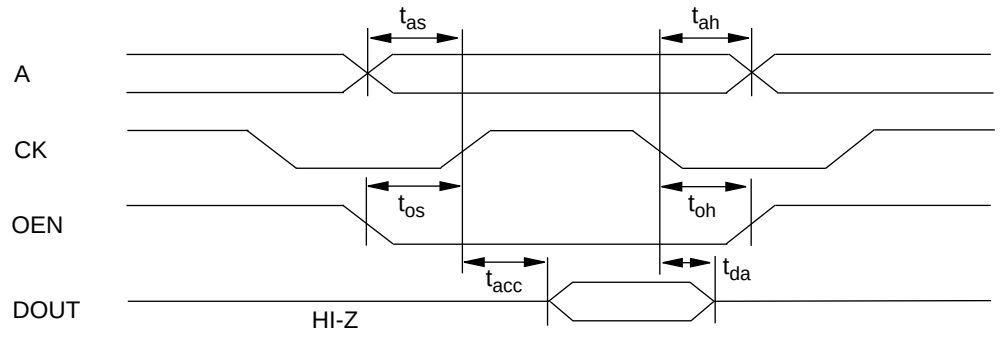
(CSN / OEN : LOW)

CSN Control



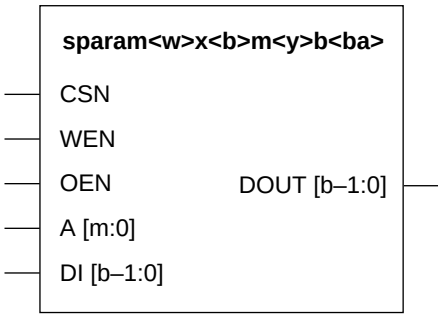
(OEN : LOW, WEN / DI : DON'T CARE)

OEN Control



(CSN : LOW, WEN / DI : DON'T CARE)

Logic Symbol



NOTES:

1. Words (w) is the number of words in SPARAM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Asynchronous operation
- Address transition detectors
- Write enable transition detector
- Chip select transition detector
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 128K bits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

SPARAM is a single-port asynchronous static RAM. When WEN is high, just after the address (A [ ]) transition, DOUT [ ] presents data stored in the location addressed by A [ ]. Upon WEN rising edge, the value of DI [ ] is written into the location addressed by A [ ]. CSN is used to enable/disable the access. OEN is used to enable/disable the data output driver.

Generators and Cell Configurations

SPARAM generates layout, netlist, symbol and functional & timing model of a SPARAM. The layout of SPARAM is an automatically generated array of custom, pitch-matched leaf cells. There are four generator parameters to resolve the configuration of a SPARAM.

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	16	32	64	128
		Max	1024	2048	4096	8192
		Step	8	16	32	64
Bpw (b)	ba = 1	Min	1	1	1	1
		Max	64	32	16	8
		Step	1	1	1	1
	ba = 2	Min	2	2	2	2
		Max	128	64	32	16
		Step	1	1	1	1

SPARAM Gen

Single-Port Asynchronous RAM Generator

Pin Descriptions

Name	I/O	Description
CSN	I	"Chip Select Negative" acts as the memory enable signal for selecting one of multiple memory blocks. When CSN is high, DOUT[ ] goes to Hi-Z state, the memory goes to stand-by (power down) mode and no access to the memory can occur. Conversely, if CSN is low only then may a read or write access occur. When CSN falls, a read access is initiated. CSN should be stable when WEN is low.
WEN	I	"Write Enable Negative" selects the type of memory access. When WEN is high, the SPARAM is in read mode. Otherwise, it is in write mode. Upon the rising edge of WEN, a write access completed and a read access initiated. When WEN is low, A[ ] and CSN should be stable.
OEN	I	"Output Enable Negative" unconditionally enables or disables the output drivers.
A [ ]	I	"Address" selects the location to be accessed. When A[ ] changes, the transition is detected and the internal clock pulse will be generated. A[ ] should be stable when WEN is low.
DI [ ]	I	When WEN rises, the "Data In" word value is written to the location addressed.
DOUT [ ]	O	During a read access, the data word stored will be presented to the "Data OUT" ports. DOUT[ ] is tri-statable. When CSN is low and OEN is low, only then, DOUT[ ] drives a certain value. Otherwise, DOUT[ ] keeps Hi-Z state. During a write access, the data on DOUT is unpredictable.

Pin Capacitance

(Unit = SL)

	CSN	WEN	OEN	A	DI	DOUT			
						Ymux 4	Ymux 8	Ymux 16	Ymux 32
1-bank	9.7	4.2	0.7	4.2	1.9	5.5	11.7	24.1	49.0
2-bank	19.3	8.4	1.3	4.2	1.9	5.5	11.7	24.1	49.0

Application Notes

1) Fitting the Layout Shape (Aspect Ratio)

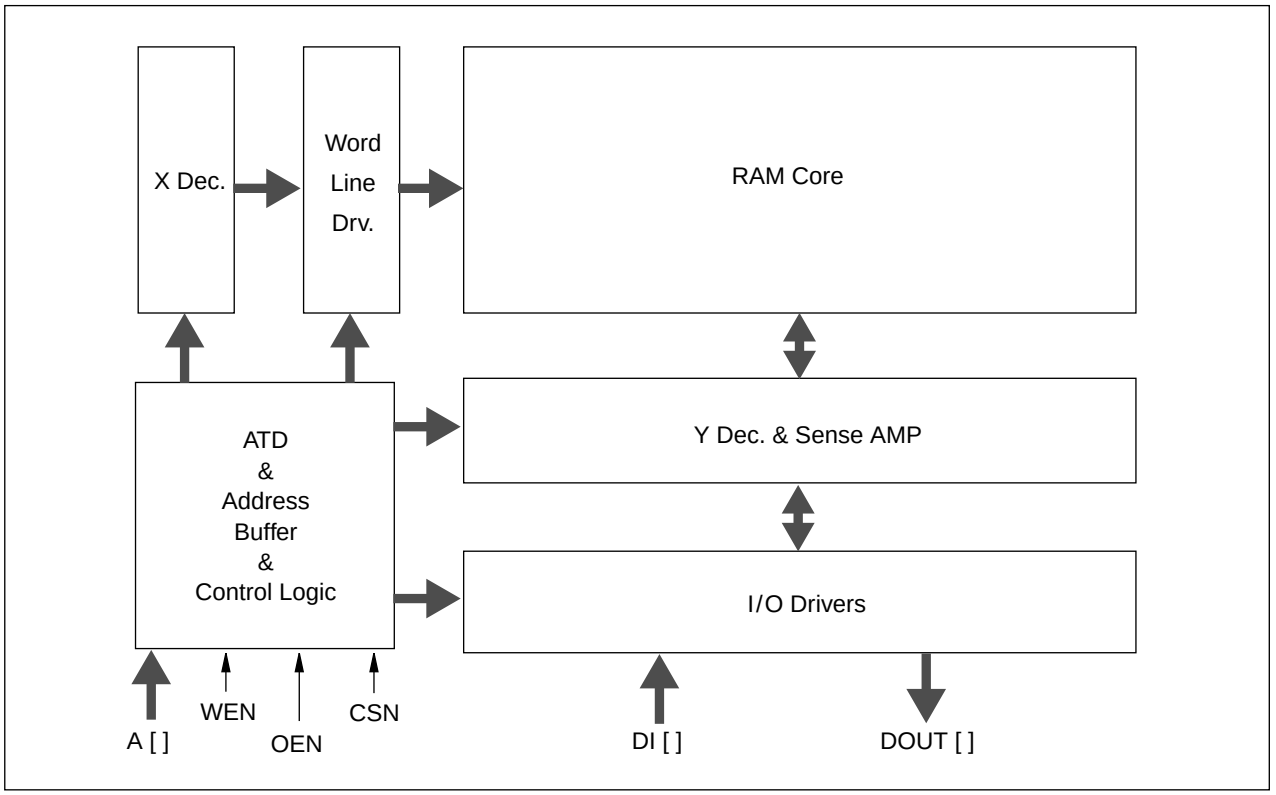
Layout Shape can be fitted by choosing one of 4 Ymux parameters in the above configuration table in accordance with your chip level layout design preference. Larger one makes the layout shape flat and short. Smaller one makes it thin and tall. In general, flat and short SPARAM is faster than thin and tall one.

2) Selecting Number of Banks

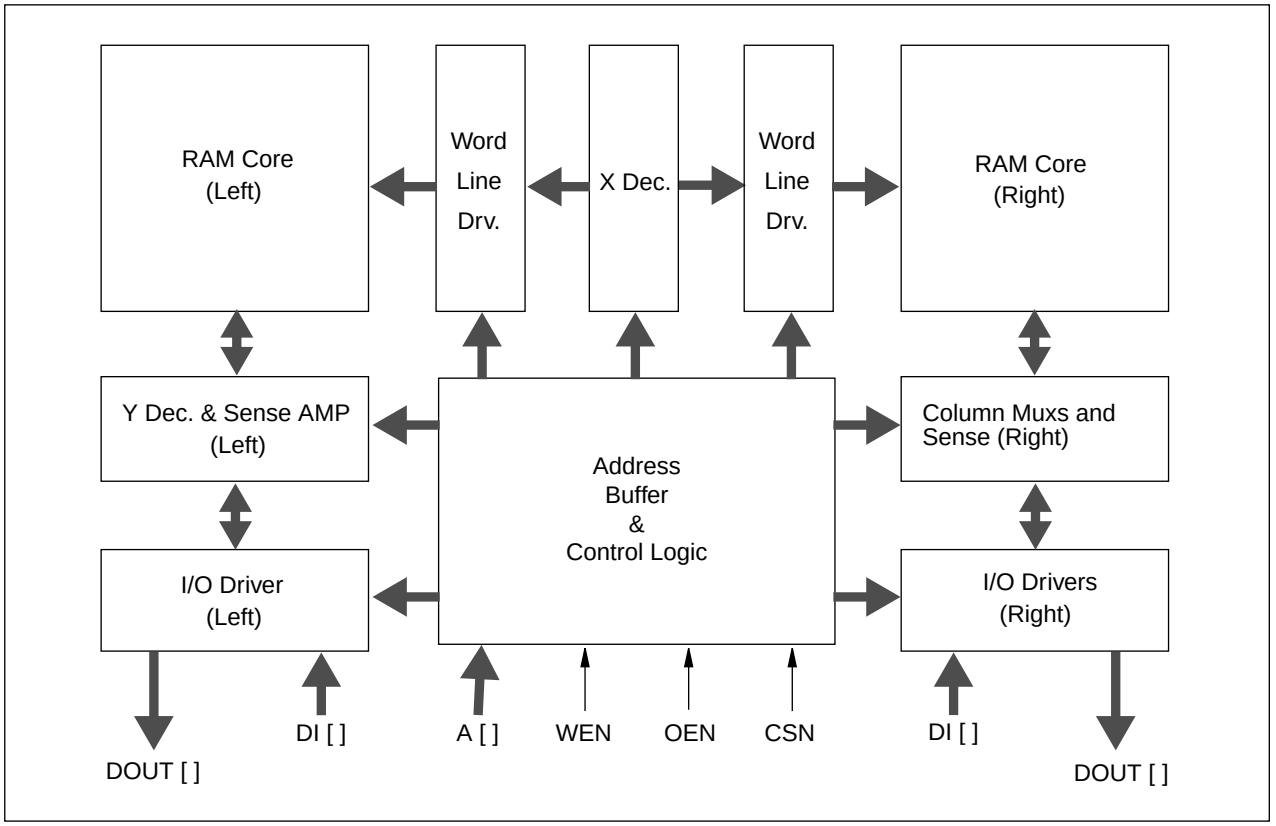
The maximum capacity of SPARAM (ba=1) reaches to 64K. It can be doubled by setting the bank parameter (ba) 2 and the bpw double. In that case, note that the words can't be doubled. By the way, the bank parameter ba=2 can be applied to the configuration smaller than 64K. Please refer to the configuration table above. SPARAM (ba=2) is a little bigger than SPARAM(ba=1) for the same capacity.

Block Diagrams (1 Bank)

< 1-bank >



< 2-bank >



Characteristic Reference Table

STD80

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING (Typical process, 5V, 25 ^{O}C, Output load = 10SL, Input slope = 0.2 ns Unit = ns)							
t_{acc}	Access Time	5.6	5.6	5.9	5.9	6.3	6.3
t_{da}	Deaccess Time	0.7	0.7	0.7	0.7	0.7	0.7
t_{dz}	Active to Hi-Z	1.2	1.2	1.2	1.2	1.2	1.2
t_{zd}	Hi-Z to Active	1.6	1.6	1.6	1.6	1.6	1.6
t_{as}	Address Setup Time	0.1	0.1	0.1	0.1	0.1	0.1
t_{ah}	Address Hold Time	1.1	1.0	1.2	1.0	1.3	1.1
t_{ds}	Input Data Setup Time	0.6	0.6	0.7	0.8	0.9	1.2
t_{dh}	Input Data Hold Time	0.8	0.8	1.0	0.8	1.4	1.0
t_{wen}	Min. WEN Pulse Width Low	2.6	2.6	2.7	2.7	2.9	2.9
t_{cs}	CSN Setup Time	0.1	0.1	0.1	0.1	0.1	0.1
t_{ch}	CSN Hold Time	0.9	0.9	0.9	0.9	0.9	0.9
SIZE (μm)							
Width		723	891	1206	1374	2172	2340
Height		972	972	1577	1577	2786	2786
POWER (μW/MHz)							
power_add (normal mode: CSN Low)			2825		5250		11350
power_csn (stand-by mode: CSN High)			250		455		862

Characteristic Reference Table (Cont.)

STDM80

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING (Typical process, 3.3V, 25 ^{o}C, Output load = 10SL, Input slope = 0.2 ns Unit = ns)							
t_{acc}	Access Time	8.3	8.3	8.7	8.7	9.4	9.4
t_{da}	Deaccess Time	0.9	0.9	0.9	0.9	0.9	0.9
t_{dz}	Active to Hi-Z	1.8	1.8	1.8	1.8	1.8	1.8
t_{zd}	Hi-Z to Active	2.2	2.2	2.2	2.2	2.2	2.2
t_{as}	Address Setup Time	0.1	0.1	0.1	0.1	0.1	0.1
t_{ah}	Address Hold Time	1.4	1.4	1.5	1.4	1.7	1.4
t_{ds}	Input Data Setup Time	0.8	0.9	1.0	1.2	1.3	1.7
t_{dh}	Input Data Hold Time	1.1	1.0	1.4	1.1	1.8	1.4
t_{wen}	Min. WEN Pulse Width Low	4.0	4.0	4.1	4.1	4.3	4.3
t_{cs}	CSN Setup Time	0.1	0.1	0.1	0.1	0.1	0.1
t_{ch}	CSN Hold Time	1.7	1.7	1.7	1.7	1.7	1.7
SIZE (μm)							
Width		723	891	1206	1374	2172	2340
Height		972	972	1577	1577	2786	2786
POWER (μW/MHz)							
power_add (normal mode: CSN Low)			1262		2395		5618
power_csn (stand-by mode: CSN High)			163		304		577

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words	B: Bits per Word
Y: Ymux Type	BA: Number of Banks (1 or 2)
S: Input Slope (Unit: ns)	SL: Number of Fanouts (Unit: Standard Load)
VDD: Operating Voltage (Unit: V)	F: Operating Frequency (Unit: MHz)

STD80 (Typical process, 5V, 25 ^{O}C)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 4
tacc	(9.15e-04*W+4.93e-02*S+1.59e-01*SL*0.019+5.33)
twen	(4.24e-04*W+2.12e-01*S+2.36-3.57e-06*W*S)
	Y = 8
tacc	(4.57e-04*W+4.93e-02*S+1.59e-01*SL*0.019+5.33)
twen	(2.12e-04*W+2.12e-01*S+2.36-1.78e-06*W*S)
	Y = 16
tacc	(2.28e-04*W+4.93e-02*S+1.59e-01*SL*0.019+5.33)
twen	(1.06e-04*W+2.12e-01*S+2.36-8.93e-07*W*S)
	Y = 32
tacc	(1.14e-04*W+4.93e-02*S+1.59e-01*SL*0.019+5.33)
twen	(5.30e-05*W+2.12e-01*S+2.36-4.46e-07*W*S)

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 4
power_add	(2.9072e-02*W+3.4109*B+3.5237e+01 +3.8993e-03*W*B)*VDD^2*F
power_csn	(1.5442e-02*W+2.5843e-01*B+2.0571 +6.8027e-07*W*B)*VDD^2*F
	Y = 8
power_add	(1.5487e-02*W+5.7627*B+3.5725e+01 +4.0492e-03*W*B)*VDD^2*F
power_csn	(7.7211e-03*W+5.1686e-01*B+2.0571 +6.8026e-07*W*B)*VDD^2*F
	Y = 16
power_add	(5.8213e-03*W+1.1800e+01*B+4.1049e+01 +3.0633e-03*W*B)*VDD^2*F
power_csn	(3.8605e-03*W+1.0337*B+2.0571 +6.8026e-07*W*B)*VDD^2*F
	Y = 32
power_add	(2.4814e-03*W+2.3136e+01*B+4.2708e+01 +3.1289e-03*W*B)*VDD^2*F
power_csn	(1.9302e-03*W+2.0674*B+2.0571 +6.8026e-07*W*B)*VDD^2*F

NOTES:

1. power_add : This is a normal mode power of memory. When CSN is low.
2. power_csn : This is a standby mode power of memory. When CSN is high.

3) Size Equation [Unit: μm]

Width = 12*(log2(W/Y))+170*BA+7.55*(B*Y)-5
Height = 366.7+9.45*W/Y

STDM80 (Typical process, 3.3V, 25 ^{o}C)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 4
tacc	(1.35e-03*W+8.73e-02*S+1.93e-01*SL*0.019+7.89)
twen	(4.77e-04*W+2.91e-01*S+3.69-2.98e-05*W*S)
	Y = 8
tacc	(6.76e-04*W+8.73e-02*S+1.93e-01*SL*0.019+7.89)
twen	(2.38e-04*W+2.91e-01*S+3.69-1.49e-05*W*S)
	Y = 16
tacc	(3.38e-04*W+8.73e-02*S+1.93e-01*SL*0.019+7.89)
twen	(1.19e-04*W+2.91e-01*S+3.69-7.47e-06*W*S)
	Y = 32
tacc	(1.69e-04*W+8.73e-02*S+1.93e-01*SL*0.019+7.89)
twen	(5.97e-05*W+2.91e-01*S+3.69-3.73e-06*W*S)

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 4
power_add	(2.7532e-02*W+3.8304*B+3.0565e+01 +4.1607e-03*W*B)*VDD^{2}*F
power_csn	(1.4978e-02*W+5.8712e-01*B+2.5513 -2.2987e-05*W*B)*VDD^{2}*F
	Y = 8
power_add	(1.8626e-02*W+6.6841*B+3.0143e+01 +3.8965e-03*W*B)*VDD^{2}*F
power_csn	(7.4892e-03*W+1.1742*B+2.5513 -2.2987e-05*W*B)*VDD^{2}*F
	Y = 16
power_add	(4.5158e-03*W+1.2019e+01*B+4.0375e+01 +4.0406e-03*W*B)*VDD^{2}*F
power_csn	(3.7446e-03*W+2.3484*B+2.5513 -2.2987e-05*W*B)*VDD^{2}*F
	Y = 32
power_add	(1.7548e-03*W+2.3408e+01*B+4.2508e+01 +4.1451e-03*W*B)*VDD^{2}*F
power_csn	(1.8723e-03*W+4.6969*B+2.5513 -2.2987e-05*W*B)*VDD^{2}*F

NOTES:

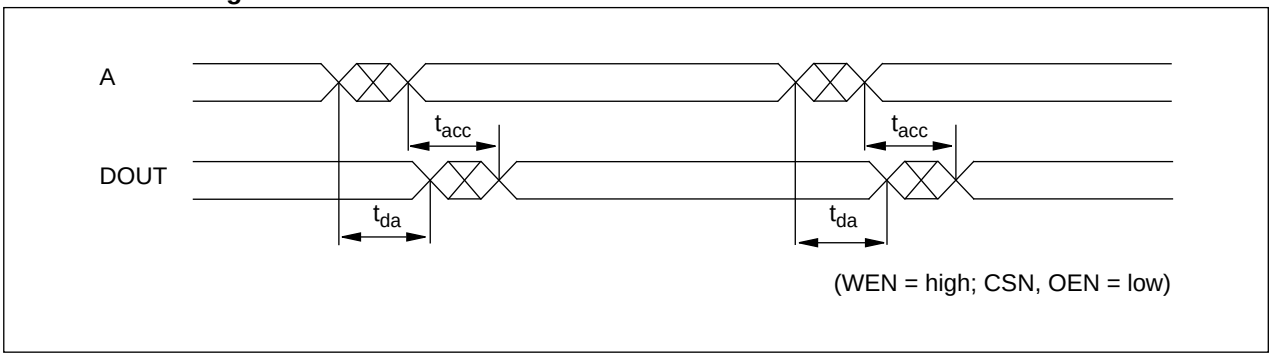
1. power_add : This is a normal mode power of memory. When CSN is low.
2. power_csn : This is a standby mode power of memory. When CSN is high.

3) Size Equation [Unit: μm]

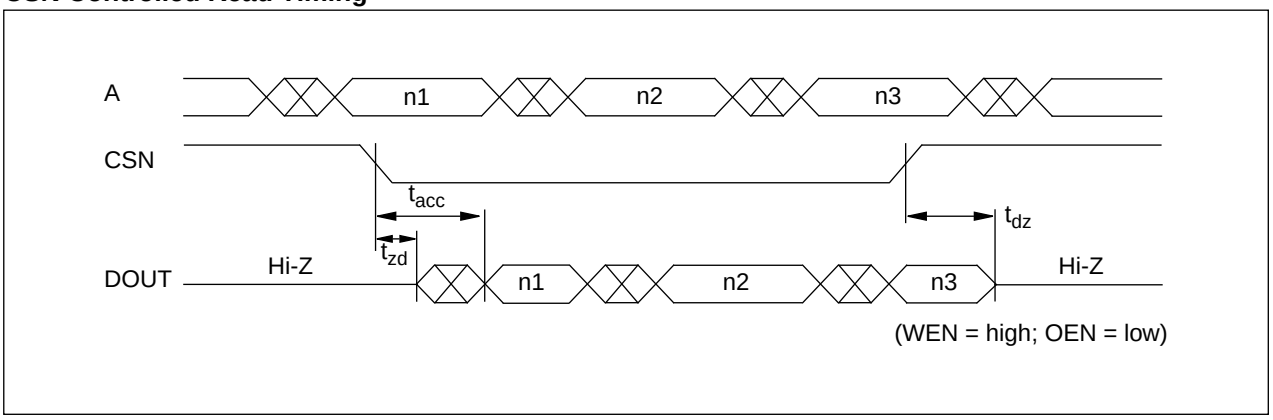
Width = 12*(log2(W/Y))+170*BA+7.55*(B*Y)-5
Height = 366.7+9.45*W/Y

Timing Diagrams

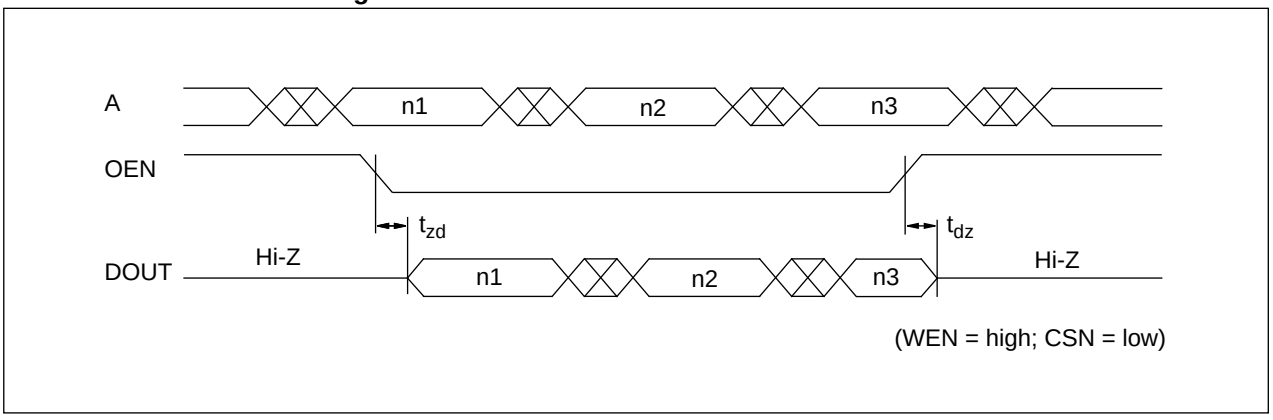
Basic Read Timing



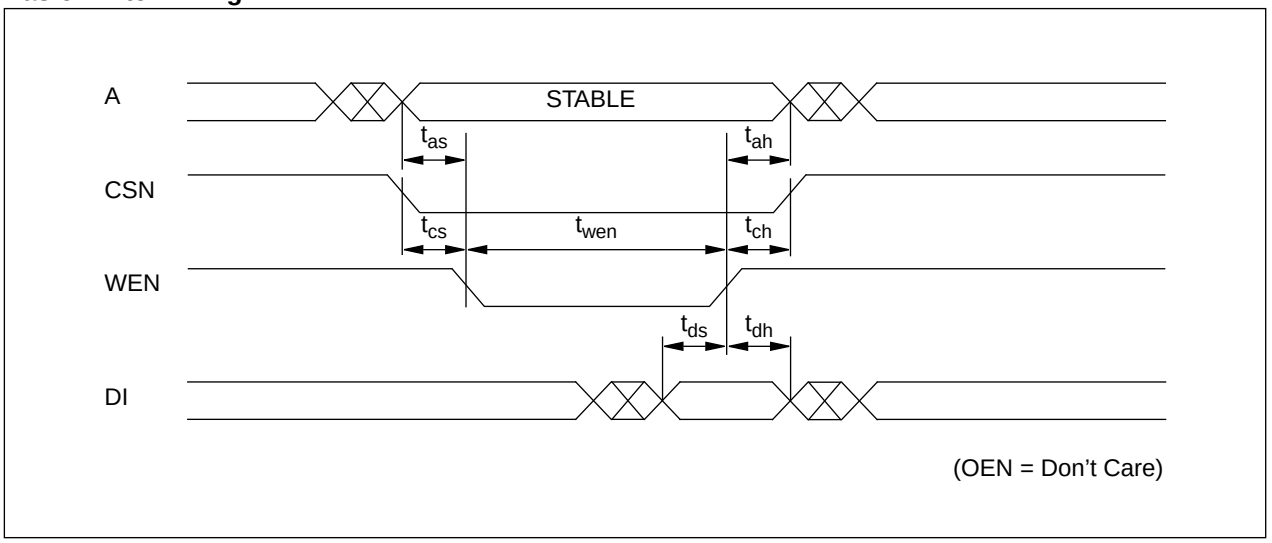
CSN Controlled Read Timing



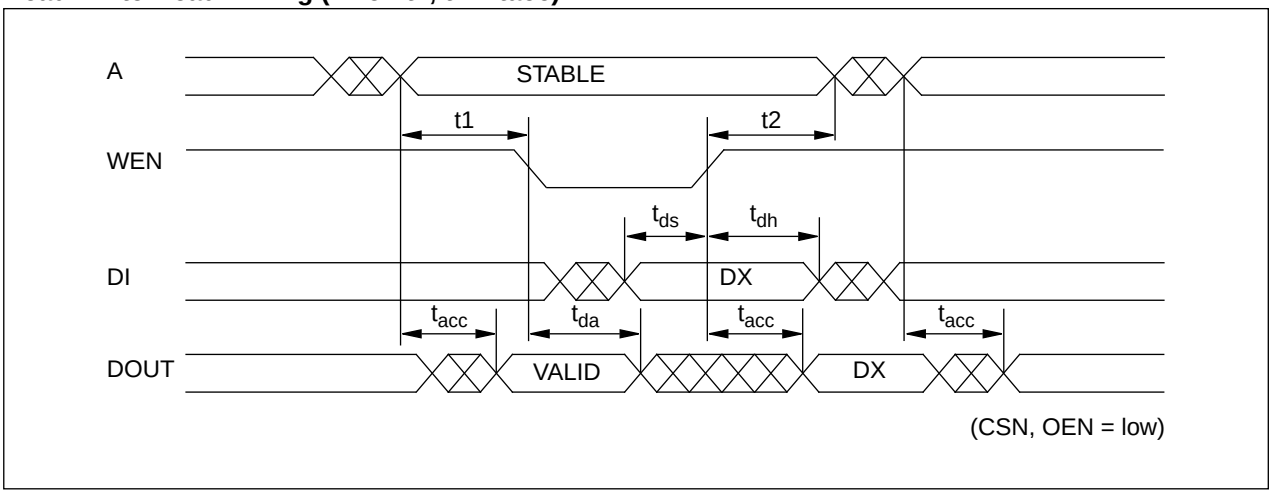
OEN Controlled Read Timing



Basic Write Timing



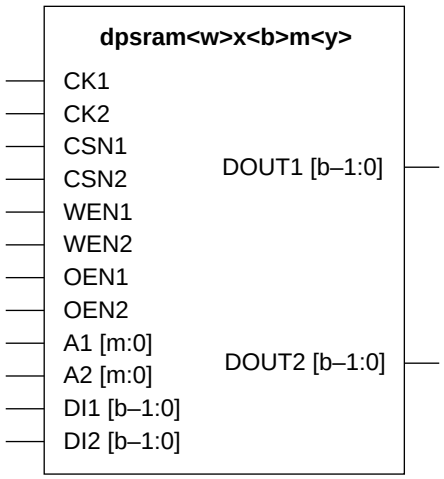
Read-Write-Read Timing (when t1, t2 > tacc)



DPSRAM Gen

Dual-Port Synchronous RAM Generator

Logic Symbol



NOTES:

1. Words (w) is the number of words in DPSRAM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Write completed at rising edge of clock
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Flexible aspect ratio
- Up to 64K bits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

DPSRAM is a dual-port synchronous static RAM. When CK1 rises, if WEN1 is high, DOUT1 [ ] presents data stored in the location addressed by A1 [ ], otherwise the value of DI1 [ ] is written into the location addressed by A1 [ ]. CSN1 is used to enable/disable CK1. OEN1 is used to enable/disable tri-state drivers of DOUT1 [ ]. The functionality of port2 is the same to port1. The port1 and port2 function independently each other.

Generators and Cell Configurations

DPSRAM Gen. generates layout, netlist, symbol and functional & timing model of DPSRAM. The layout of DPSRAM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of DPSRAM, you can give certain values to following three generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y).

The valid range of these parameters is specified in the following table:

Parameters		YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	Min	4	8	16	32	64
	Max	512	1024	2048	4096	8192
	Step	2	4	8	16	32
Bpw (b)	Min	1	1	1	1	1
	Max	128	64	32	16	8
	Step	1	1	1	1	1

Pin Descriptions

Name	I/O	Description
CK1 CK2	I	“Clock”s serve as input clocks to each port of the memory block. When CK1 (CK2) is low, port1 (port2) is in a precharge state. Upon the rising edge, an access begins.
CSN1 CSN2	I	“Chip Select Negative”s act as each port’s enable signal for selections of multiple blocks on a common clock. When CSN1 (CSN2) is high, port1 (port2) goes to stand-by (power down) mode and no access can occur, conversely, if low only then may a read or write access occur. CSN1 (CSN2) may not change during CK1 (CK2) is high.
WEN1 WEN2	I	“Write Enable Negative”s select the type of memory access. Read is the high state, and write is the low state.
OEN1 OEN2	I	“Output Enable Negative”s control the output drivers from driven to tri-state condition. OEN1 (OEN2) may not change during CK1 (CK2) is high.
A1 [ ] A2 [ ]	I	“Address”es select the location to be accessed. A1 [ ] (A2 [ ]) may not change during CK1 (CK2) is high.
DI1 [ ] DI2 [ ]	I	When CK1 (CK2) rises while WEN1 (WEN2) is low, the “Data In” word value is written to the accessed location.
DOUT1 [ ] DOUT2 [ ]	O	During a read access, data word stored will be presented to the “Data Out” ports. DOUT1 [ ] and DOUT2 [ ] are tri-statable. Only when CK1 (CK2) is high, CSN1 (CSN2) and OEN1 (OEN2) is low, DOUT1 [ ] (DOUT2 [ ]) drives a certain value. Otherwise, DOUT1 [ ] (DOUT2 [ ]) keeps Hi-Z state. During a write access, data word written will be presented at the “Data Out” ports if output driver is enabled.

Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	DI	DOUT				
						Ymux 2	Ymux 4	Ymux 8	Ymux 16	Ymux 32
5.8	1.9	0.9	2.3	1.0	2.0	5.4	5.4	12.0	25.0	51.0

Application Notes

1) Putting Busholders on DOUT1 [ ] and DOUT2 [ ]

As you will see in the timing diagrams, DOUT1 [ ] (DOUT2 [ ]) is valid only when CK1 (CK2) is high. If you want DOUT1 [ ] (DOUT2 [ ]) to be stable regardless of CK1 (CK2) state, you should put STD80/STDM80 Busholder cells on the DOUT1 [ ] (DOUT2 [ ]) bus externally.

2) Customizing Aspect Ratio

Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 5 selections of Ymux for the same Words and the same Bpw DPSRAM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of DPSRAM, In general, larger Ymux DPSRAM has faster speed and bigger area than smaller Ymux DPSRAM.

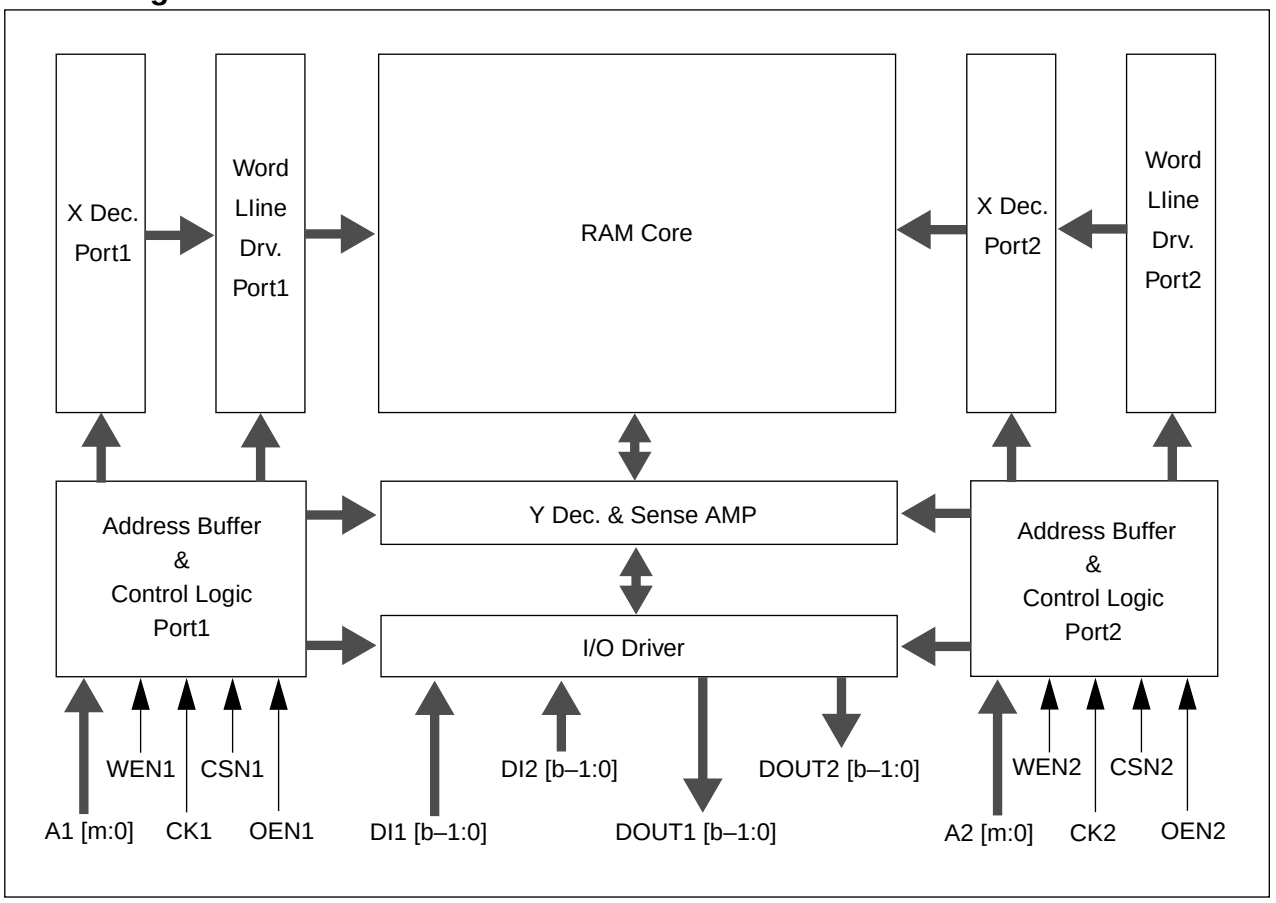
3) Contention Modes

Simultaneous accesses to the same location through both ports cause a contention. DPSRAM has no contention preventing scheme. You have to take care of the contention modes. Please refer to the timing diagrams of contention modes to get more information of contention modes.

DPSRAM Gen

Dual-Port Synchronous RAM Generator

Block Diagram



Characteristic Reference Table

STD80

Symbol	Description	256x16m4	1024x16m8	4Kx16m16
TIMING REQUIREMENTS & DELAY (Typical process, 5V, 25 ^{o}C, Output load = 10SL, Unit = ns)				
minckl	Minimum Clock Pulse Width Low	2.20	2.70	3.90
minckh	Minimum Clock Pulse Width High	4.10	4.40	5.20
t_{cc}	Clock to Clock Setup Time	3.10	4.10	6.30
t_{as}	Address Setup Time	0.34	0.54	0.77
t_{ah}	Address Hold Time	0.48	0.43	0.33
t_{cs}	CSN Setup Time	0.45	0.45	0.45
t_{ch}	CSN Hold Time	0	0	0
t_{ds}	Data Input Setup Time	0	0	0
t_{dh}	Data Input Hold Time	3.10	3.90	5.40
t_{os}	OEN Setup Time	0	0	0
t_{oh}	OEN Hold Time	1.25	1.35	1.55
t_{ws}	WEN Setup Time	0	0	0
t_{wh}	WEN Hold Time	0	0	0
t_{acc}	Access Time	3.10	3.80	5.10
t_{da}	Deaccess Time	1.90	2.10	2.40
mincyc	Minimum Clock Cycle Time	6.70	8.60	12.50
SIZE (μm)				
Width		996	1787	3353
Height		1110	1802	3194
POWER (μW/MHz)				
power_ck (normal mode: CSN Low)		1632	3150	6512
power_csn (stand-by mode: CSN High)		250	475	900

Characteristic Reference Table (Cont.)

STDM80

Symbol	Description	256x16m4	1024x16m8	4Kx16m16
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)				
minckl	Minimum Clock Pulse Width Low	3.00	3.80	5.40
minckh	Minimum Clock Pulse Width High	5.50	6.40	7.90
t_{cc}	Clock to Clock Setup Time	4.20	5.60	8.40
t_{as}	Address Setup Time	0.37	0.67	1.20
t_{ah}	Address Hold Time	0.58	0.54	0.50
t_{cs}	CSN Setup Time	0.56	0.56	0.56
t_{ch}	CSN Hold Time	0	0	0
t_{ds}	Data Input Setup Time	0	0	0
t_{dh}	Data Input Hold Time	4.30	5.20	7.20
t_{os}	OEN Setup Time	0	0	0
t_{oh}	OEN Hold Time	1.90	2.00	2.30
t_{ws}	WEN Setup Time	0	0	0
t_{wh}	WEN Hold Time	0	0	0
t_{acc}	Access Time	4.50	5.40	7.10
t_{da}	Deaccess Time	2.40	2.60	3.00
mincyc	Minimum Clock Cycle Time	9.90	12.90	18.90
SIZE (µm)				
Width		996	1787	3353
Height		1110	1802	3194
POWER (µW/MHz)				
power_ck (normal mode: CSN Low)		762	1546	3659
power_csn (stand-by mode: CSN High)		108	206	435

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
B: Bits per Word
Y: Ymux Type
SL: Number of Fanouts (Unit: Standard Load)
S: Input Slope (Unit: ns)
F: Operating Frequency (Unit: MHz)
VDD: Operating Voltage (Unit: V)

STD80

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
minckh	(2.3646e – 03 * W + 2.8351e – 03 * B + 9.8324e – 01 * 0.019 * SL + 1.2350 + 2.1938e – 05 * W * B – 6.3558e – 04 * W * 0.019 * SL – 2.4658e – 03 * B * 0.019 * SL)
minckl	(3.0467e – 03 * W + 5.8227e – 03 * B + 1.5699 + 1.7795e – 07 * W * B)
mincyc	(1.18e – 02 * W + 7.9429e – 03 * B – 1.4125e – 01 * 0.019 * SL + 3.5681 + 1.3689e – 01 * 0.019 * SL * 0.019 * SL) * 1.1
tacc	(3.1469e – 03 * W + 6.8856e – 03 * B + 1.4939e – 01 * S + 3.6108e – 01 * 0.019 * SL + 2.3066)
	Y = 4
minckh	(1.1823e – 03 * W + 5.6702e – 03 * B + 9.8324e – 01 * 0.019 * SL + 1.2350 + 2.1938e – 05 * W * B – 3.1779e – 04 * W * 0.019 * SL – 4.9317e – 03 * B * 0.019 * SL)
minckl	(1.5233e – 03 * W + 1.1645e – 02 * B + 1.5699 + 1.7796e – 07 * W * B)
mincyc	(5.94e – 03 * W + 1.5885e – 02 * B – 1.4125e – 01 * 0.019 * SL + 3.5681 + 1.3689e – 01 * 0.019 * SL * 0.019 * SL) * 1.1
tacc	(1.5734e – 03 * W + 1.3771e – 02 * B + 1.4939e – 01 * S + 3.6108e – 01 * 0.019 * SL + 2.3066)
	Y = 8
minckh	(6.1758e – 04 * W + 1.3960e – 02 * B + 7.2178e – 01 * 0.019 * SL + 1.4573)
minckl	(7.6168e – 04 * W + 2.3291e – 02 * B + 1.5699 + 1.7794e – 07 * W * B)
mincyc	(2.97e – 03 * W + 3.1771e – 02 * B – 1.4125e – 01 * 0.019 * SL + 3.5681 + 1.3689e – 01 * 0.019 * SL * 0.019 * SL) * 1.1
tacc	(7.8672e – 04 * W + 2.7542e – 02 * B + 1.4939e – 01 * S + 3.6108e – 01 * 0.019 * SL + 2.3066)
	Y = 16
minckh	(4.9053e – 04 * W + 2.5687e – 02 * B + 8.1759e – 01 * 0.019 * SL + 1.4633 – 7.5634e – 06 * W * B – 6.0306e – 05 * W * 0.019 * SL + 4.8660e – 03 * B * 0.019 * SL)
minckl	(3.8084e – 04 * W + 4.6582e – 02 * B + 1.5699 + 1.7794e – 07 * W * B)
mincyc	(1.48e – 03 * W + 6.3543e – 02 * B – 1.4125e – 01 * 0.019 * SL + 3.5681 + 1.3689e – 01 * 0.019 * SL * 0.019 * SL) *1.1
tacc	(3.9701e – 04 * W + 5.7737e – 02 * B + 1.4501e – 01 * S + 1.5318e – 01 * 0.019 * SL + 2.2527)
	Y = 32
minckh	(1.4662e – 04 * W + 4.1246e – 02 * B + 8.0560e – 01 * 0.019 * SL + 2.0499)
minckl	(1.9042e – 04 * W + 9.3164e – 02 * B + 1.5699 + 1.7791e – 07 * W * B)
mincyc	(7.43e – 04 * W + 1.2708e – 01 * B – 1.4125e – 01 * 0.019 * SL + 3.5681 + 1.3689e – 01 * 0.019 * SL * 0.019 * SL) * 1.1

Timing Type	Timing Equation
tacc	(1.9668e – 04 * W + 1.1017e – 01 * B + 1.4939e – 01 * S + 3.6108e – 01 * 0.019 * SL + 2.3066)

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 2
power_ck	(2.0763e – 01 * W + 1.1277 * B + 3.1186 – 1.0486e – 04 * W * B) * VDD^2 * F
power_csn	(1.0551e – 02 * W + 2.4929e – 01 * B + 9.5587e – 01 – 3.1253e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(1.0381e – 01 * W + 2.2555 * B + 3.1186 – 1.0486e – 04 * W * B) * VDD^2 * F
power_csn	(5.2757e – 03 * W + 4.9858e – 01 * B + 9.5587e – 01 – 3.1253e – 05 * W * B) * VDD^2 * F
	Y = 8
power_ck	(4.9408e – 02 * W + 3.5969 * B + 4.6093 + 8.6446e – 04 * W * B) * VDD^2 * F
power_csn	(2.6378e – 03 * W + 9.9716e – 01 * B + 9.5587e – 01 – 3.1253e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(2.4666e – 02 * W + 6.0326 * B + 4.9311 + 8.8607e – 04 * W * B) * VDD^2 * F
power_csn	(1.3189e – 03 * W + 1.9943 * B + 9.5587e – 01 – 3.1253e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(1.2221e – 02 * W + 1.0298e + 01 * B + 5.7362 + 7.6259e – 04 * W * B) * VDD^2 * F
power_csn	(6.5946e – 04 * W + 3.9886 * B + 9.5587e – 01 – 3.1253e – 05 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 16.6 * ($\lceil \log2\ (W / Y) \rceil$) + 12.1 * B * Y + 121.7 [μm]
Height = 404.95 + 10.85 * W/Y + M [μm]
(M = 8.15 (if Y = 2, 8), M = 10.55 (if Y = 4, 16), M = 12.95 (if Y = 32))

STDM80

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
minckh	(4.1092e – 03 * W + 4.0747e – 03 * B + 9.0315e – 01 * 0.019 * SL + 2.2883)
minckl	(4.1417e – 03 * W + 7.9201e – 03 * B + 2.2145 + 1.1253e – 06 * W * B)
mincyc	(2.1473e – 02 * W + 5.8971e – 03 * B + 5.9619e – 01 * 0.019 * SL + 4.6027 – 6.1247e – 04 * W * 0.019 * SL) * 1.1
tacc	(4.1701e – 03 * W + 9.8971e – 03 * B + 1.7063e – 01 * S + 4.3595e – 01 * 0.019 * SL + 3.3675)
	Y = 4
minckh	(2.0546e – 03 * W + 8.1494e – 03 * B + 9.0315e – 01 * 0.019 * SL + 2.2883)
minckl	(2.0708e – 03 * W + 1.5840e – 02 * B + 2.2145 + 1.1253e – 06 * W * B)
mincyc	(1.0736e – 02 * W + 1.1794e – 02 * B + 5.9619e – 01 * 0.019 * SL + 4.6027 – 3.0623e – 04 * W * 0.019 * SL) * 1.1
tacc	(2.0850e – 03 * W + 1.9794e – 02 * B + 1.7063e – 01 * S + 4.3595e – 01 * 0.019 * SL + 3.3675)

Timing Type	Timing Equation
	Y = 8
minckh	(5.6171e – 04 * W – 1.3181e – 02 * B + 6.8946e – 01 * 0.019 * SL + 2.8571 + 2.7457e – 05 * W * B + 1.1695e – 04 * W * 0.019 * SL + 9.4850e – 03 * B * 0.019 * SL)
minckl	(1.0354e – 03 * W + 3.1680e – 02 * B + 2.2145 + 1.1253e – 06 * W * B)
mincyc	(5.3684e – 03 * W + 2.3588e – 02 * B + 5.9619e – 01 * 0.019 * SL + 4.6027 – 1.5311e – 04 * W * 0.019 * SL) * 1.1
tacc	(1.0425e – 03 * W + 3.9588e – 02 * B + 1.7063e – 01 * S + 4.3595e – 01 * 0.019 * SL + 3.3675)
	Y = 16
minckh	(5.1367e – 04 * W + 3.1572e – 02 * B + 9.3585e – 01 * 0.019 * SL + 2.6593)
minckl	(5.1771e – 04 * W + 6.3361e – 02 * B + 2.2145 + 1.1253e – 06 * W * B)
mincyc	(2.6842e – 03 * W + 4.7177e – 02 * B + 5.9619e – 01 * 0.019 * SL + 4.6027 – 7.6559e – 05 * W * 0.019 * SL) * 1.1
tacc	(5.2127e – 04 * W + 7.9177e – 02 * B + 1.7063e – 01 * S + 4.3595e – 01 * 0.019 * SL + 3.3675)
	Y = 32
minckh	(2.4832e – 04 * W + 6.6898e – 02 * B + 9.2358e – 01 * 0.019 * SL + 3.1671)
minckl	(2.5885e – 04 * W + 1.2672e – 01 * B + 2.2145 + 1.1253e – 06 * W * B)
mincyc	(1.3421e – 03 * W + 9.4355e – 02 * B + 5.9619e – 01 * 0.019 * SL + 4.6027 – 3.8279e – 05 * W * 0.019 * SL) * 1.1
tacc	(2.6063e – 04 * W + 1.5835e – 01 * B + 1.7063e – 01 * S + 4.3595e – 01 * 0.019 * SL + 3.3675)

2) Power Characteristics [Unit: μW]

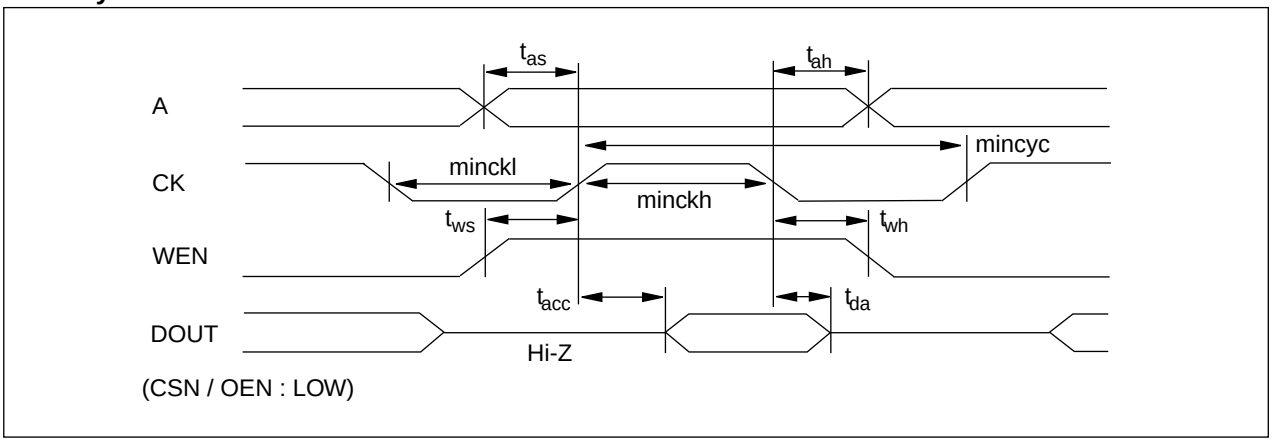
Power Type	Power Equation
	Y = 2
power_ck	(1.6148e – 01 * W + 9.5794e – 01 * B + 9.7215 + 2.3042e – 03 * W * B) * VDD^2 * F
power_csn	(7.3480e – 03 * W + 2.3132e – 01 * B + 1.7751 + 7.5474e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(8.0741e – 02 * W + 1.9158 * B + 9.7215 + 2.3042e – 03 * W * B) * VDD^2 * F
power_csn	(3.6740e – 03 * W + 4.6264e – 01 * B + 1.7751 + 7.5474e – 05 * W * B) * VDD^2 * F
	Y = 8
power_ck	(4.0704e – 02 * W + 3.0779 * B + 1.1325e + 01 + 2.4858e – 03 * W * B) * VDD^2 * F
power_csn	(1.8370e – 03 * W + 9.2529e – 01 * B + 1.7751 + 7.5474e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(2.1023e – 02 * W + 5.0567 * B + 9.5773 + 2.4457e – 03 * W * B) * VDD^2 * F
power_csn	(9.1850e – 04 * W + 1.8505 * B + 1.7751 + 7.5474e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(1.0031e – 02 * W + 7.8426 * B + 1.0827e + 01 + 2.6112e – 03 * W * B) * VDD^2 * F
power_csn	(4.5925e – 04 * W + 3.7011 * B + 1.7751 + 7.5474e – 05 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

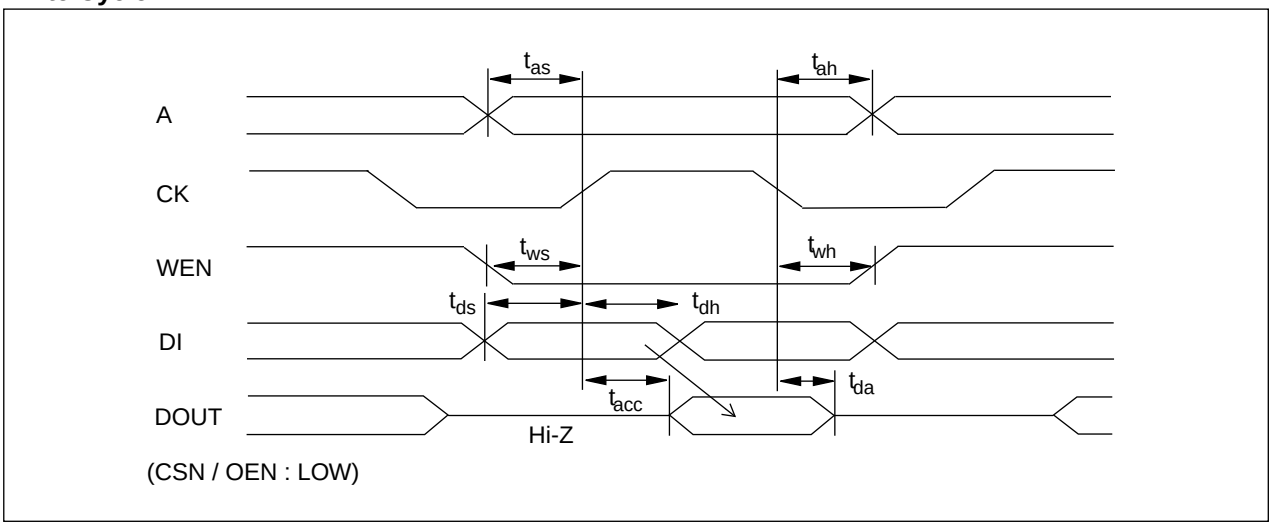
Width = 16.6 * ($\lceil \log_2 (W / Y) \rceil$) + 12.1 * B * Y + 121.7 [μm]
Height = 404.95 + 10.85 * W / Y + M [μm]
(M = 8.15 (if Y = 2, 8), M = 10.55 (if Y = 4, 16), M = 12.95 (if Y = 32))

Timing Diagrams

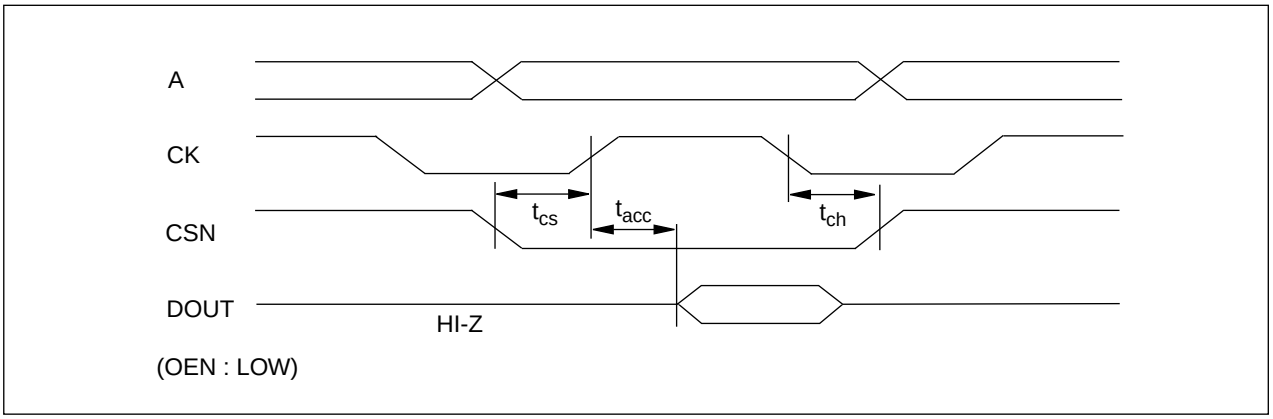
Read Cycle



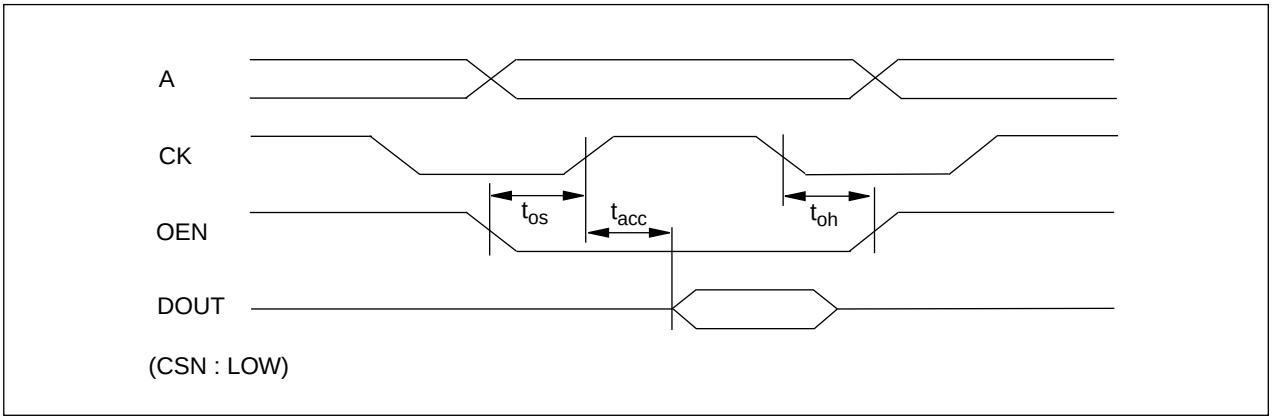
Write Cycle



CSN Control

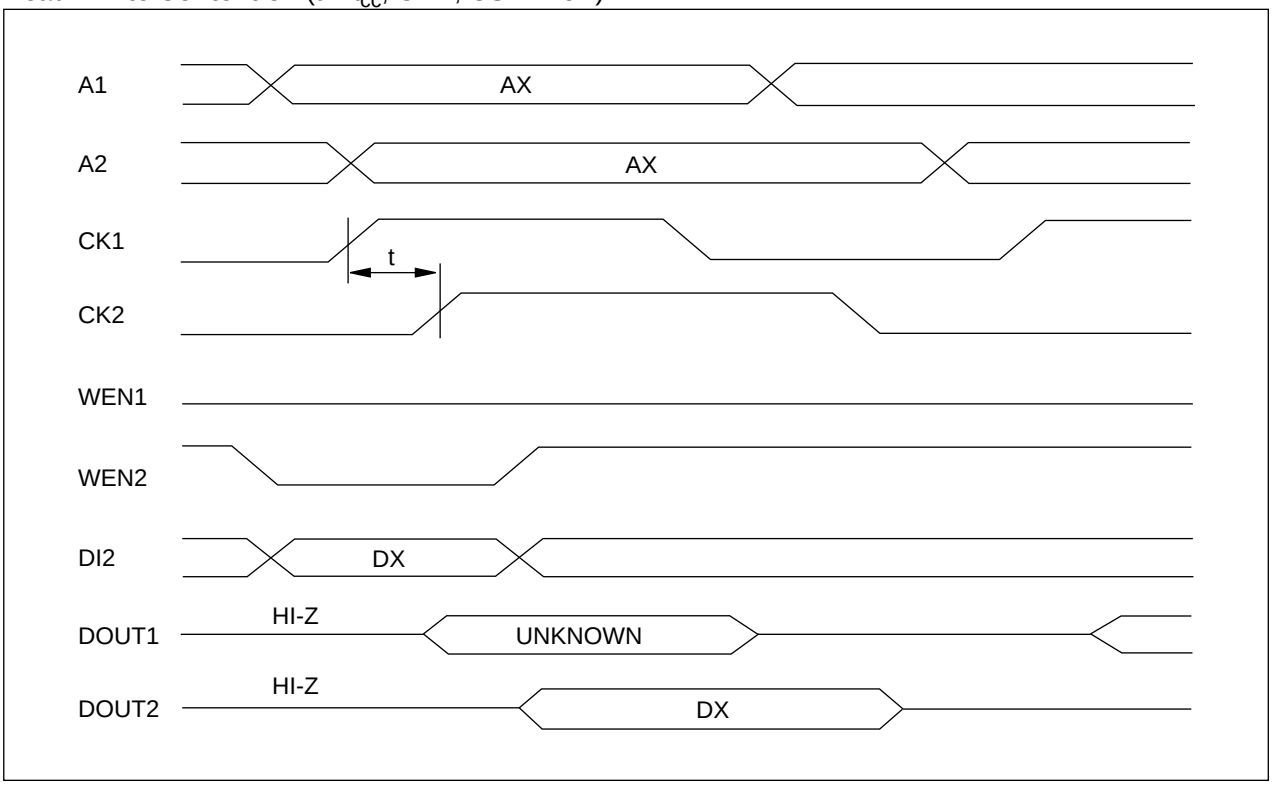


OEN Control

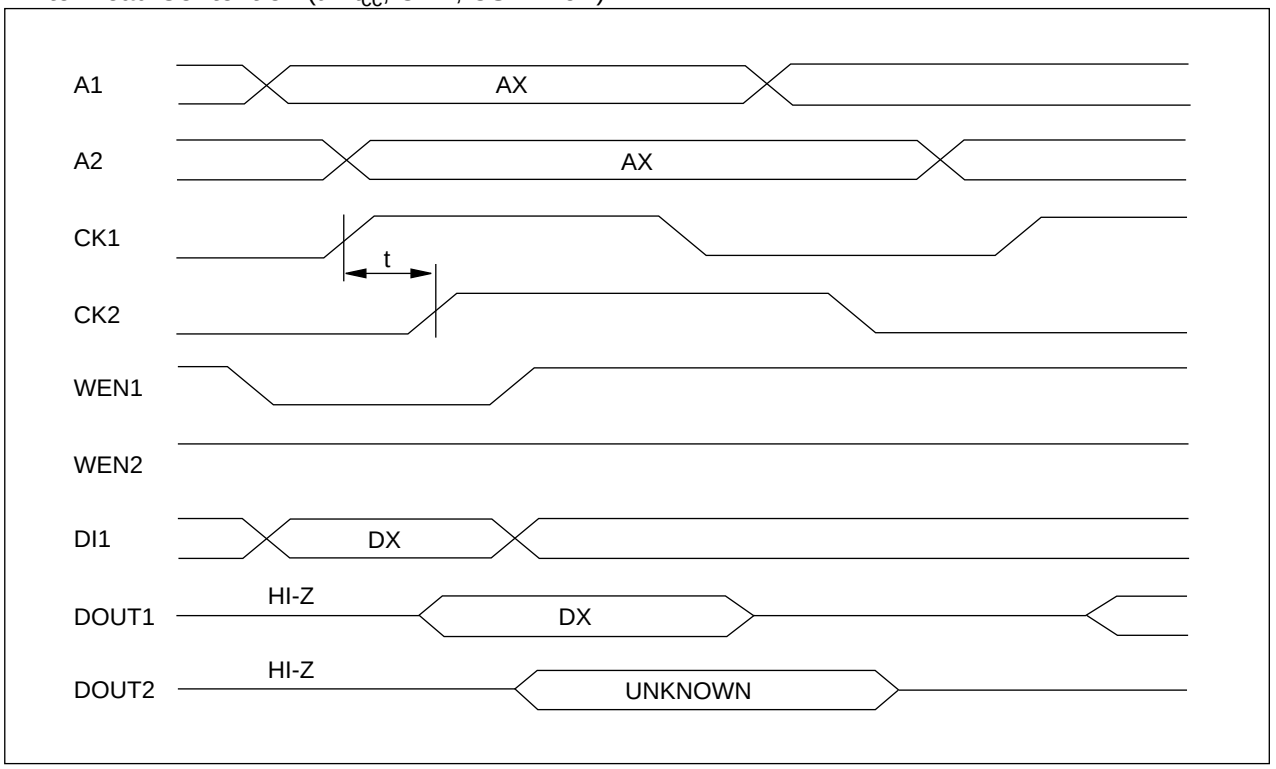


Function Diagrams

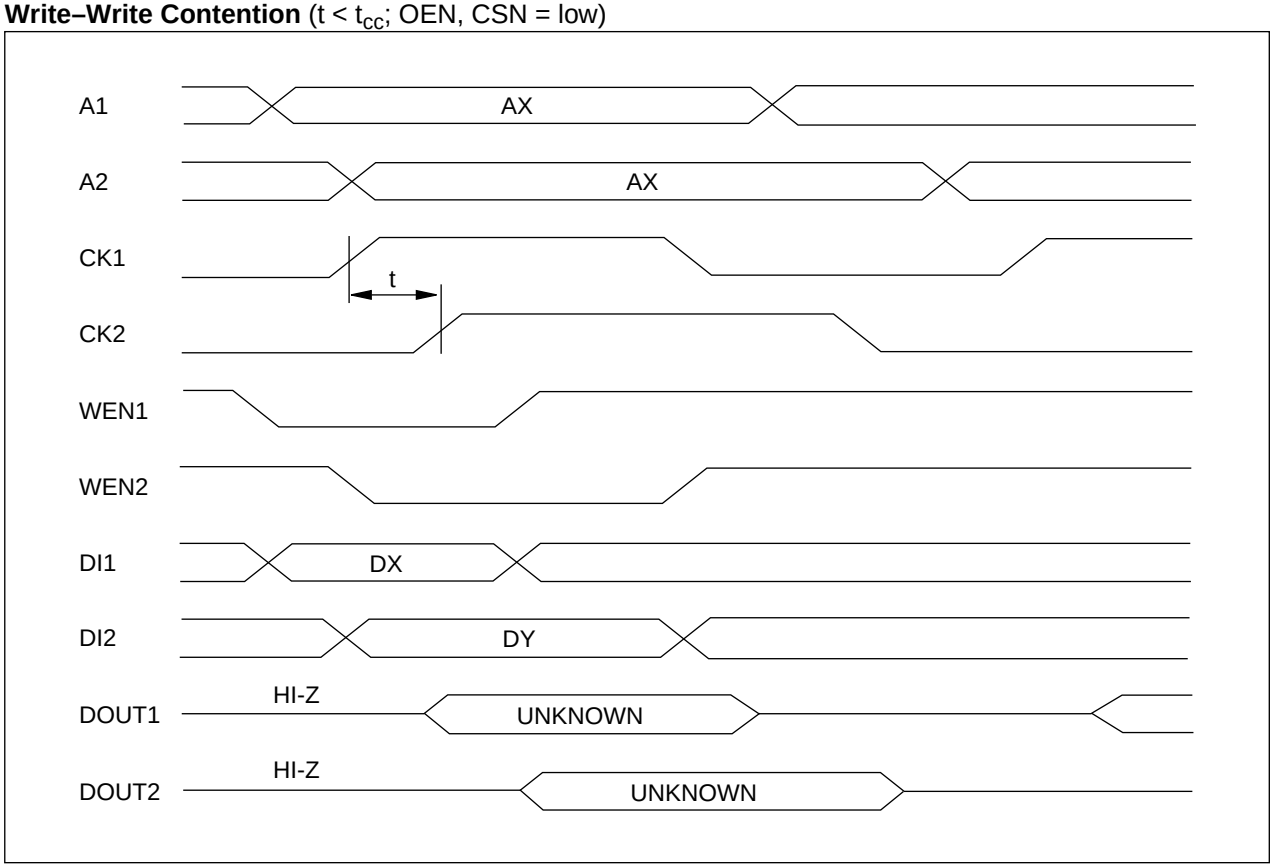
Read–Write Contention ($t < t_{cc}$; OEN, CSN = low)



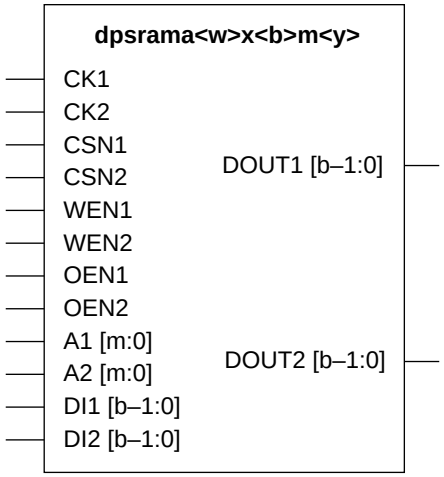
Write–Read Contention ($t < t_{cc}$; OEN, CSN = low)



Write–Write Contention ($t < t_{cc}$; OEN, CSN = low)



Logic Symbol



NOTES:

1. Words (w) is the number of words in DPSRAMA.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Write completed at falling edge of clock
- Possible read modified write cycle
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Possible bi-directional operation
- Flexible aspect ratio
- Up to 64K bits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

DPSRAMA is a dual-port synchronous static RAM. When WEN1 is high and CK1 rises, DOUT1 [ ] presents data stored in the location addressed by A1 [ ]. When WEN1 is low and CK1 falls, or when CK1 is high and WEN1 rises, the value of DI1 [ ] is written into the location addressed by A1 [ ]. CSN1 is used to enable/disable CK1. OEN1 is used to enable/disable tri-state drivers of DOUT1 [ ]. The functionality of port2 is the same to port1. The port1 and port2 function independently each other.
DPSRAMA is an alternative of DPSRAM. The major difference of these two RAMs is the timing of read and write. DPSRAMA reads and writes at different edge of the clock since DPSRAM reads and writes at the same edge of the clock.

Generators and Cell Configurations

DPSRAMA Gen. generates layout, netlist, symbol and functional & timing model of DPSRAMA. The layout of DPSRAMA is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of DPSRAMA, you can give certain values to following three generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y).

The valid range of these parameters is specified in the following table:

Parameters		YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	Min	4	8	16	32	64
	Max	512	1024	2048	4096	8192
	Step	2	4	8	16	32
Bpw (b)	Min	1	1	1	1	1
	Max	128	64	32	16	8
	Step	1	1	1	1	1

Pin Descriptions

Name	I/O	Description
CK1 CK2	I	“Clock”s serve as input clocks to each port of the memory block. When CK1 (CK2) is low, port1 (port2) is in a precharge state. Upon the rising edge, a read cycle begins. Upon the falling edge, a write cycle ends.
CSN1 CSN2	I	“Chip Select Negative”s act as each port’s enable signal for selections of multiple blocks on a common clock. When CSN1 (CSN2) is high, port1 (port2) goes to stand-by (power down) mode and no access can occur, conversely, if low only then may a read or write access occur. CSN1 (CSN2) may not change during CK1 (CK2) is high.
WEN1 WEN2	I	“Write Enable Negative”s select the type of memory access. Read is the high state, and write is the low state.
OEN1 OEN2	I	“Output Enable Negative”s control the output drivers from driven to tri-state condition. OEN1 (OEN2) may not change during CK1 (CK2) is high.
A1 [ ] A2 [ ]	I	“Address”es select the location to be accessed. A1 [ ] (A2 [ ]) may not change during CK1 (CK2) is high.
DI1 [ ] DI2 [ ]	I	When CK1 (CK2) falls while WEN1 (WEN2) is low, or when WEN1 (WEN2) rises while CK1 (CK2) is high, the “Data In” word value is written to the accessed location.
DOUT1 [ ] DOUT2 [ ]	O	During a read access, data word stored will be presented to the “Data Out” ports. DOUT1 [ ] and DOUT2 [ ] are tri-statable. When CK1 (CK2) is high, CSN1 (CSN2) is low and OEN1 (OEN2) is low, only then, DOUT1 [ ] (DOUT2 [ ]) drives a certain value. Otherwise, DOUT1 [ ] (DOUT2 [ ]) keeps Hi-Z state. During a write access, the value of DOUT1 [ ] (DOUT2 [ ]) is unpredictable.

Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	DI	DOUT				
						Ymux 2	Ymux 4	Ymux 8	Ymux 16	Ymux 32
5.8	1.9	0.9	2.3	1.0	2.0	5.4	5.4	12.0	25.0	51.0

Application Notes

1) Putting Busholders on DOUT1 [ ] and DOUT2 [ ]

As you will see in the timing diagrams, DOUT1 [ ] (DOUT2 [ ]) is valid only when CK1 (CK2) is high. If you want DOUT1 [ ] (DOUT2 [ ]) to be stable regardless of CK1 (CK2) state, you should put STD80/STDM80 Busholder cells on the DOUT1 [ ] (DOUT2 [ ]) bus externally.

2) Customizing Aspect Ratio

Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 5 selections of Ymux for the same Words and the same Bpw DPSRAMA. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of DPSRAM, In general, larger Ymux DPSRAMA has faster speed and bigger area than smaller Ymux DPSRAMA.

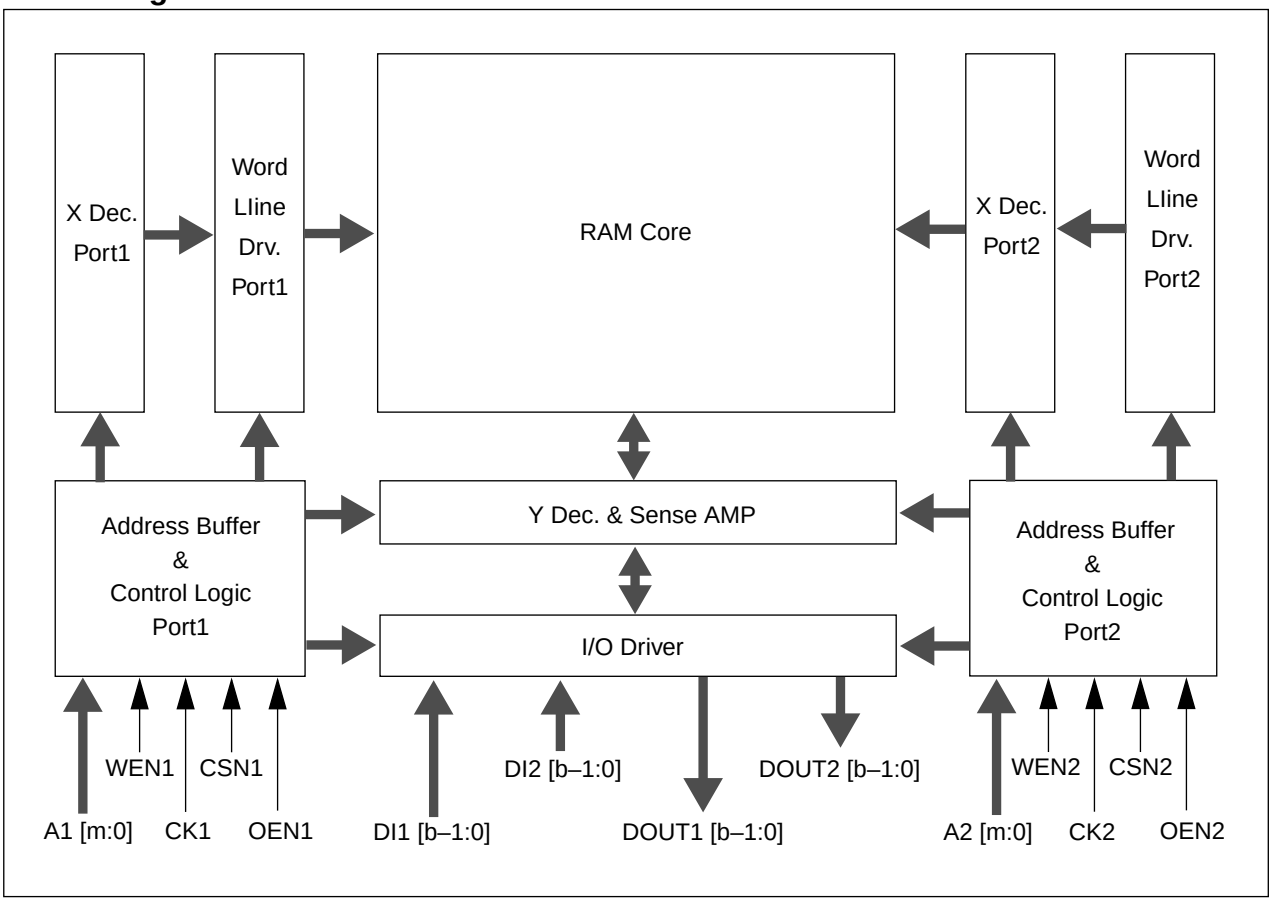
3) Contention Modes

Simultaneous accesses to the same location through both ports cause a contention. DPSRAMA has no contention preventing scheme. You have to take care of the contention modes. Please refer to the timing diagrams of contention modes to get more information of contention modes.

4) Using Bi-Directional Data Port

Because having the same phase, DI1 [ ] (DI2 [ ]) and DOUT1 [ ] (DOUT2 [ ]) of DPSRAMA can be tied directly. With tying them up together and controlling WEN1 (WEN2) and OEN1 (OEN2) properly, you can use them as bi-directional data ports.

Block Diagram



Characteristic Reference Table

STD80

Symbol	Description	256x16m4	1024x16m8	4Kx16m16
TIMING REQUIREMENTS & DELAY (Typical process, 5V, 25 ^{o}C, Output load = 10SL, Unit = ns)				
t_{rp}	Minimum Read Pulse Width	3.40	4.00	5.00
t_{pc}	Minimum Pre-Charge Period	3.70	5.29	10.5
t_{wp}	Minimum Write Pulse Width	1.63	2.29	3.51
t_{rwc}	Read-Write Contention	1.17	1.75	2.92
t_{wrc}	Write-Read Contention	0	0	0
t_{wwc}	Write-Write Contention	1.12	1.92	3.44
t_{as}	Address Setup Time	0.44	0.65	0.87
t_{ah}	Address Hold Time	1.11	1.91	2.20
t_{cs}	CSN Setup Time	0.48	0.48	0.48
t_{ch}	CSN Hold Time	0	0	0
t_{ds}	Data Input Setup Time	1.22	1.76	2.84
t_{dh}	Data Input Hold Time	1.42	1.72	2.31
t_{os}	OEN Setup Time	0	0	0
t_{oh}	OEN Hold Time	1.12	1.23	1.48
t_{wh}	WEN Hold Time	0.57	0.54	0.48
t_{acc}	Access Time	4.00	4.70	6.00
t_{da}	Deaccess Time	1.80	1.90	2.20
SIZE (μm)				
Width		996	1787	3353
Height		1110	1802	3194
POWER (μW/MHz)				
power_ck (normal mode: CSN Low)		1877	4497	12177
power_csn (stand-by mode: CSN High)		243	465	919

Characteristic Reference Table (Cont.)

STDM80

Symbol	Description	256x16m4	1024x16m8	4Kx16m16
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)				
t_{rp}	Minimum Read Pulse Width	5.03	6.24	7.78
t_{pc}	Minimum Pre-Charge Period	7.45	8.14	15.20
t_{wp}	Minimum Write Pulse Width	2.32	3.23	5.03
t_{rwc}	Read-Write Contention	1.83	2.62	4.18
t_{wrc}	Write-Read Contention	0	0	0
t_{wwc}	Write-Write Contention	1.41	2.36	4.26
t_{as}	Address Setup Time	0.45	0.89	1.75
t_{ah}	Address Hold Time	1.45	2.33	4.10
t_{cs}	CSN Setup Time	0.65	0.65	0.65
t_{ch}	CSN Hold Time	0	0	0
t_{ds}	Data Input Setup Time	1.57	2.50	4.43
t_{dh}	Data Input Hold Time	1.93	2.30	3.05
t_{os}	OEN Setup Time	0	0	0
t_{oh}	OEN Hold Time	1.63	1.75	2.00
t_{wh}	WEN Hold Time	0.67	0.56	0.63
t_{acc}	Access Time	5.70	6.50	8.30
t_{da}	Deaccess Time	2.40	2.60	3.00
SIZE (μm)				
Width		996	1787	3353
Height		1110	1802	3194
POWER (μW/MHz)				
power_ck (normal mode: CSN Low)		882	2009	5374
power_csn (stand-by mode: CSN High)		107	201	404

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

STD80

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
tpc	1.41e – 02 * W + 6.61e – 03 * B + 3.33e – 01 * S + 1.2822
trp	3.10e – 03 * W + 4.03e – 03 * B – 2.28e – 01 * S + 8.93e – 01 * 0.019 * SL + 2.2859
tacc	3.19e – 03 * W + 7.64e – 03 * B + 1.21e – 01 * S + 3.96e – 01 * 0.019 * SL + 2.1815
	Y = 4
tpc	7.09e – 03 * W + 1.32e – 02 * B + 3.33e – 01 * S + 1.2822
trp	1.55e – 03 * W + 8.07e – 03 * B – 2.28e – 01 * S + 8.93e – 01 * 0.019 * SL + 2.2859
tacc	1.59e – 03 * W + 1.52e – 02 * B + 1.21e – 01 * S + 3.96e – 01 * 0.019 * SL + 2.1815
	Y = 8
tpc	3.54e – 03 * W + 2.64e – 02 * B + 3.33e – 01 * S + 1.2822
trp	7.75e – 04 * W + 1.61e – 02 * B – 2.28e – 01 * S + 8.93e – 01 * 0.019 * SL + 2.2859
tacc	7.97e – 04 * W + 3.05e – 02 * B + 1.21e – 01 * S + 3.96e – 01 * 0.019 * SL + 2.1815
	Y = 16
tpc	1.77e – 03 * W + 5.29e – 02 * B + 3.33e – 01 * S + 1.2822
trp	3.87e – 04 * W + 3.23e – 02 * B – 2.28e – 01 * S + 8.93e – 01 * 0.019 * SL + 2.2859
tacc	3.98e – 04 * W + 6.11e – 02 * B + 1.21e – 01 * S + 3.96e – 01 * 0.019 * SL + 2.1815
	Y = 32
tpc	8.86e – 04 * W + 1.05e – 01 * B + 3.33e – 01 * S + 1.2822
trp	1.93e – 04 * W + 6.46e – 02 * B – 2.28e – 01 * S + 8.93e – 01 * 0.019 * SL + 2.2859
tacc	1.99e – 04 * W + 1.22e – 01 * B + 1.21e – 01 * S + 3.96e – 01 * 0.019 * SL + 2.1815

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 2
power_ck	(1.8534e – 01 * W + 1.0095 * B + 2.7972 + 3.9703e – 03 * W * B) * VDD^2 * F
power_csn	(9.7679e – 03 * W + 2.3114e – 01 * B + 1.0169 + 1.8078e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(9.2672e – 02 * W + 2.0190 * B + 2.7972 + 3.9703e – 03 * W * B) * VDD^2 * F
power_csn	(4.8839e – 03 * W + 4.6228e – 01 * B + 1.0169 + 1.8078e – 05 * W * B) * VDD^2 * F
	Y = 8
power_ck	(4.6336e – 02 * W + 4.0381 * B + 2.7972 + 3.9703e – 03 * W * B) * VDD^2 * F
power_csn	(2.4419e – 03 * W + 9.2456e – 01 * B + 1.0169 + 1.8078e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(2.3168e – 02 * W + 8.0763 * B + 2.7972 + 3.9703e – 03 * W * B) * VDD^2 * F

Power Type	Power Equation
power_csn	(1.2209e – 03 * W + 1.8491 * B + 1.0169 + 1.8078e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(1.1584e – 02 * W + 1.6152e + 01 * B + 2.7971 + 3.9703e – 03 * W * B) * VDD^2 * F
power_csn	(6.1049e – 04 * W + 3.6982 * B + 1.0169 + 1.8078e – 05 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 16.6 * ($\lceil \log_2 (W / Y) \rceil$) + 12.1 * B * Y + 121.7 [μm]
Height = 404.95 + 10.85 * W / Y + M [μm]
M = 8.15 (if Y = 2, 8), M = 10.55 (if Y = 4, 16), M = 12.95 (if Y = 32)

STDM80

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
tpc	1.99e – 02 * W + 1.01e – 02 * B + 2.53e – 01 * S + 2.0311
trp	4.25e – 03 * W + 6.96e – 03 * B – 9.32e – 02 * S + 1.2362 * 0.019 * SL + 3.3780
tacc	4.19e – 03 * W + 1.01e – 02 * B + 1.05e – 01 * S + 5.13e – 01 * 0.019 * SL + 3.2329
	Y = 4
tpc	9.99e – 03 * W + 2.02e – 02 * B + 2.53e – 01 * S + 2.0311
trp	2.12e – 03 * W + 1.39e – 02 * B – 9.32e – 02 * S + 1.2362 * 0.019 * SL + 3.3780
tacc	2.09e – 03 * W + 2.03e – 02 * B + 1.05e – 01 * S + 5.13e – 01 * 0.019 * SL + 3.2329
	Y = 8
tpc	4.99e – 03 * W + 4.04e – 02 * B + 2.53e – 01 * S + 2.0311
trp	1.06e – 03 * W + 2.78e – 02 * B – 9.32e – 02 * S + 1.2362 * 0.019 * SL + 3.3780
tacc	1.04e – 03 * W + 4.07e – 02 * B + 1.05e – 01 * S + 5.13e – 01 * 0.019 * SL + 3.2329
	Y = 16
tpc	2.49e – 03 * W + 8.09e – 02 * B + 2.53e – 01 * S + 2.0311
trp	5.31e – 04 * W + 5.57e – 02 * B – 9.32e – 02 * S + 1.2362 * 0.019 * SL + 3.3780
tacc	5.24e – 04 * W + 8.14e – 02 * B + 1.05e – 01 * S + 5.13e – 01 * 0.019 * SL + 3.2329
	Y = 32
tpc	1.24e – 03 * W + 1.61e – 01 * B + 2.53e – 01 * S + 2.0311
trp	2.65e – 04 * W + 1.11e – 01 * B – 9.32e – 02 * S + 1.2362 * 0.019 * SL + 3.3780
tacc	2.62e – 04 * W + 1.62e – 01 * B + 1.05e – 01 * S + 5.13e – 01 * 0.019 * SL + 3.2329

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 2
power_ck	(1.7365e – 01 * W + 9.5041e – 01 * B +1.1391e + 01 + 4.1433e – 03 * W * B) * VDD^2 * F
power_csn	(7.3119e – 03 * W + 2.2202e – 01 * B + 1.6135 + 5.1415e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(8.6829e – 02 * W + 1.9008 * B + 1.1391e + 01 + 4.1433e – 03 * W * B) * VDD^2 * F
power_csn	(3.6559e – 03 * W + 4.4405e – 01 * B + 1.6135 + 5.1415e – 05 * W * B) * VDD^2 * F
	Y = 8
power_ck	(4.3414e – 02 * W + 3.8016 * B + 1.1391e + 01 + 4.1433e – 03 * W * B) * VDD^2 * F

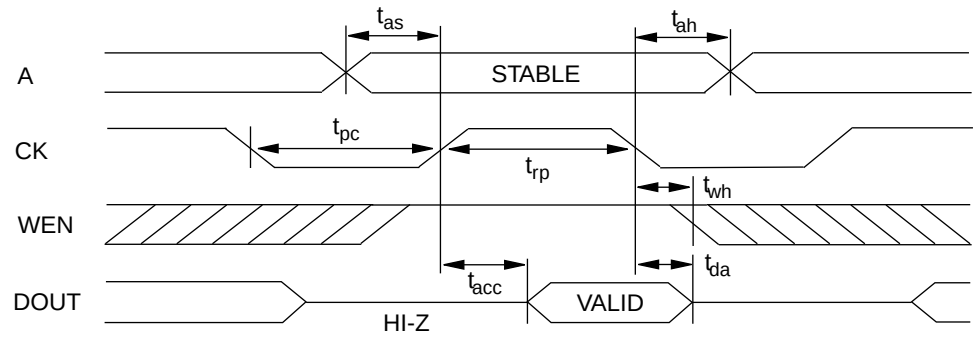
Power Type	Power Equation
power_csn	(1.8279e – 03 * W + 8.8811e – 01 * B + 1.6135 + 5.1415e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(2.1707e – 02 * W + 7.6033 * B + 1.1391e + 01 + 4.1433e – 03 * W * B) * VDD^2 * F
power_csn	(9.1398e – 04 * W + 1.7762 * B + 1.6135 + 5.1415e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(1.0853e – 02 * W + 1.5206e + 01 * B + 1.1391e + 01 + 4.1433e – 03 * W * B) * VDD^2 * F
power_csn	(4.5699e – 04 * W + 3.5524 * B + 1.6135 + 5.1415e – 05 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 16.6 * ($\lceil \log_2 (W / Y) \rceil$) + 12.1 * B * Y + 121.7 [μm]
Height = 404.95 + 10.85 * W / Y + M [μm]
M = 8.15 (if Y = 2, 8), M = 10.55 (if Y = 4, 16), M = 12.95 (if Y = 32)

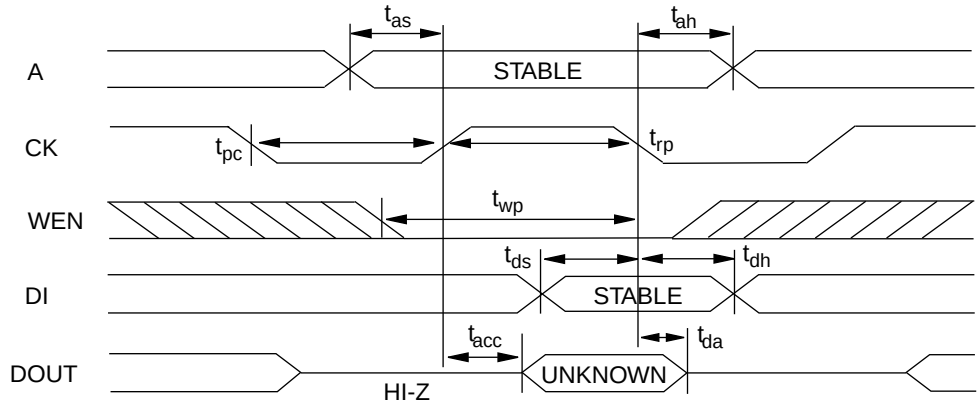
Timing Diagrams

Read Cycle



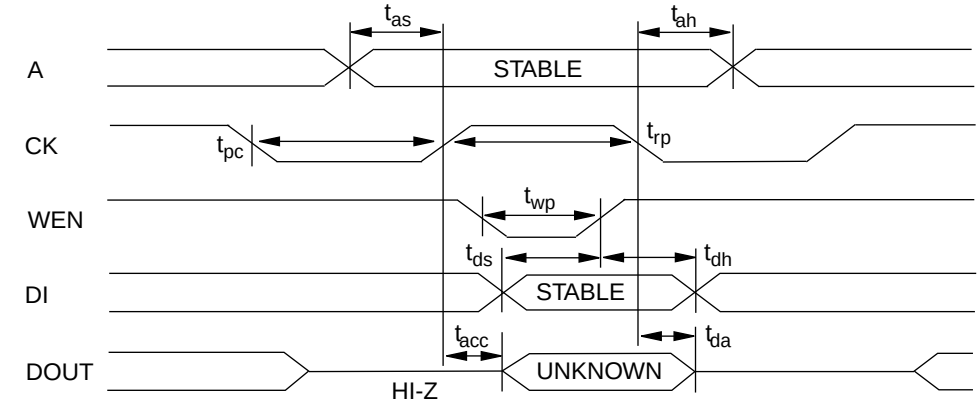
(CSN / OEN : LOW, DI :DON'T CARE)

CK Defined Write Cycle



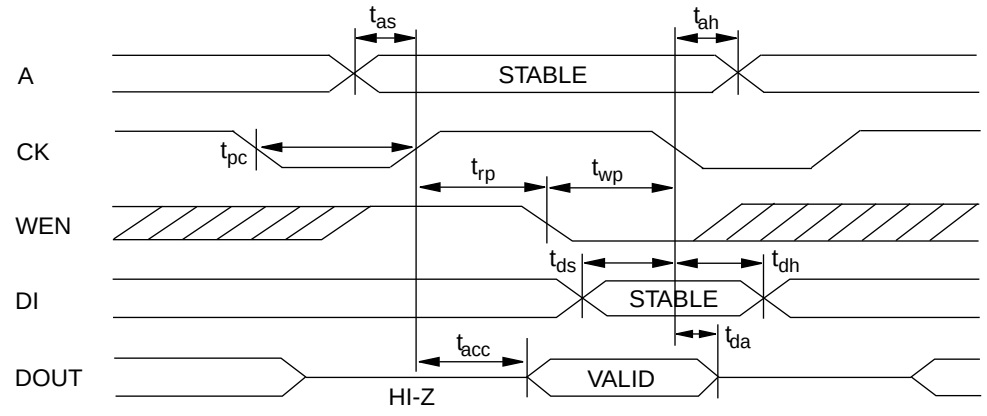
(CSN / OEN : LOW)

WEN Defined Write Cycle



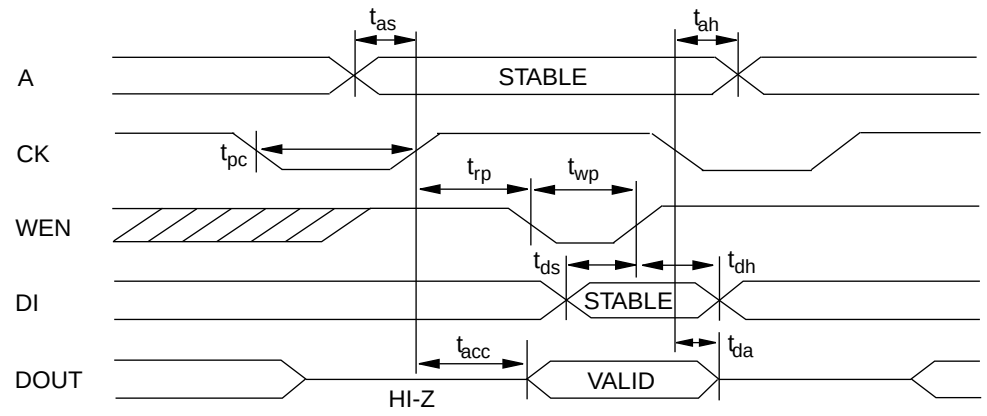
(CSN / OEN : LOW)

CK Defined Read-Modified-Write Cycle



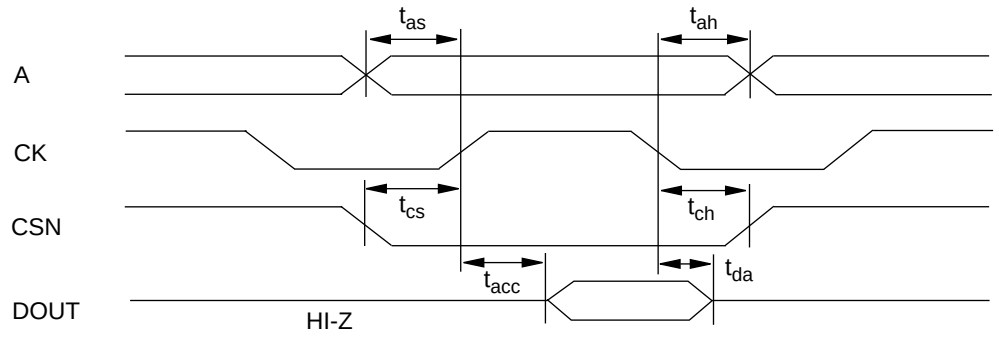
(CSN / OEN : LOW)

WEN Defined Read-Modified-Write Cycle



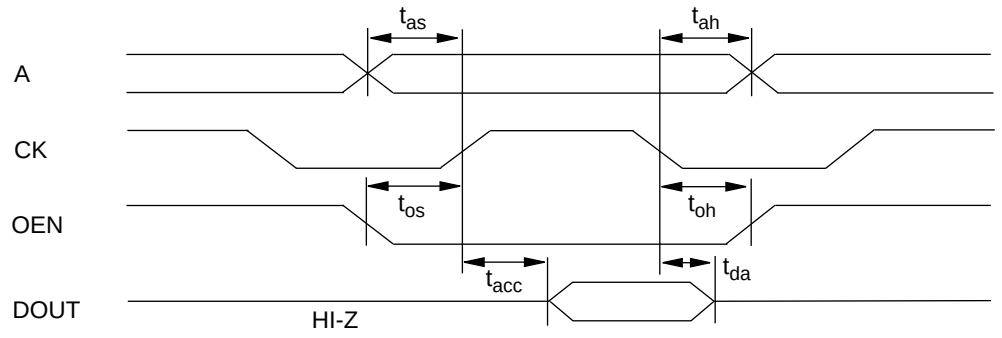
(CSN / OEN : LOW)

CSN Control



(OEN : LOW, WEN / DI : DON'T CARE)

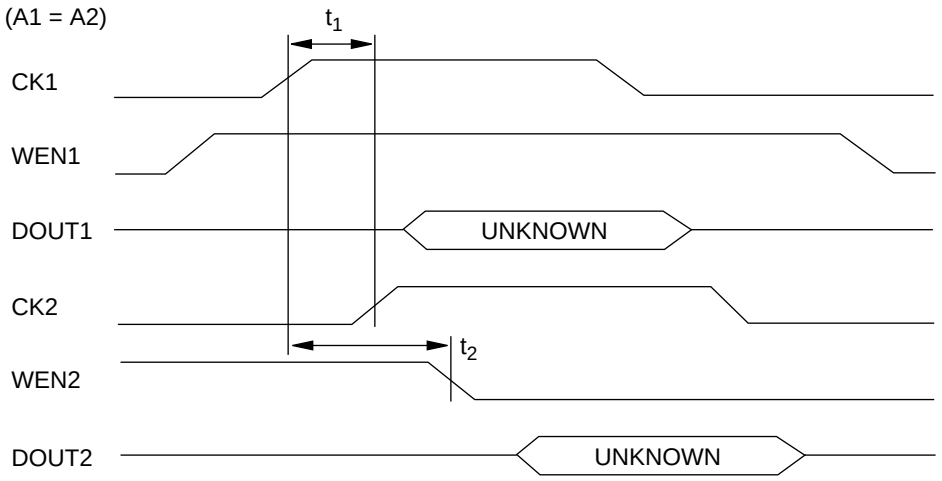
OEN Control



(CSN : LOW, WEN / DI : DON'T CARE)

Function Diagrams

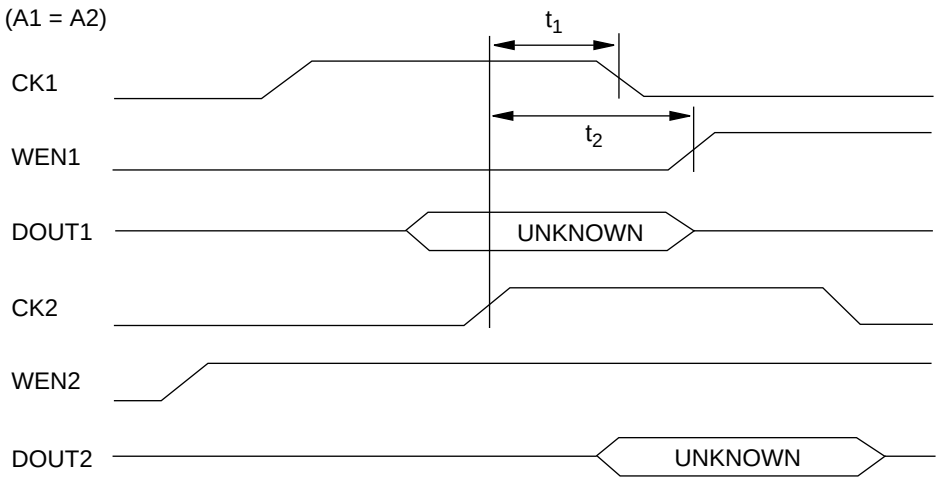
Read–Write Contention (max (t_1, t_2) ≤ t_{rwc})



(CSN1 / CSN2 / OEN1 / OEN2 : LOW, DI1 : DON'T CARE, DI2 : VALID)

* If the greater of t_1 or t_2 is smaller than or equal to t_{rwc}, it is Read-Write Contention.
The read by port1 is invalid, the write by port2 is still valid.

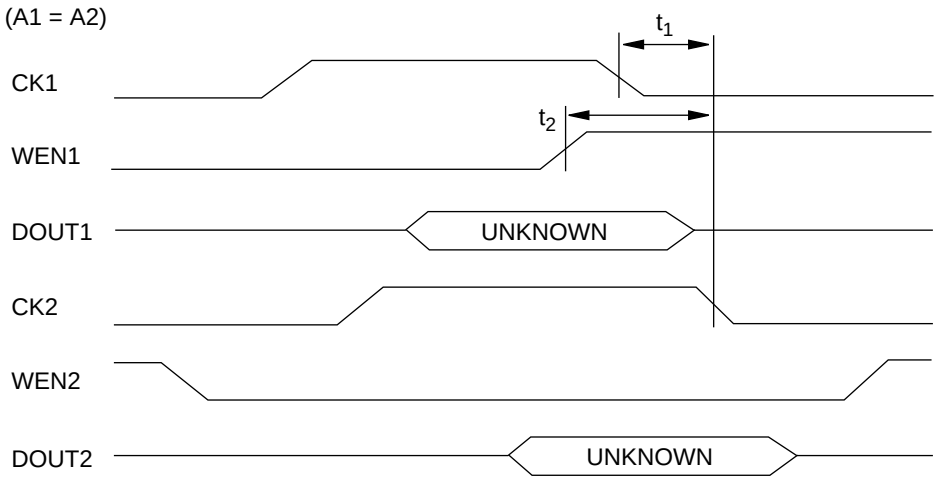
Write–Read Contention (min (t_1, t_2) ≥ t_{wrc})



(CSN1 / CSN2 / OEN1 / OEN2 : LOW, DI1 : VALID, DI2 : DON'T CARE)

* If the smaller of t_1 or t_2 is greater than or equal to t_{wrc}, it is Write-Read Contention.
The read by port2 is invalid, the write by port1 is still valid.

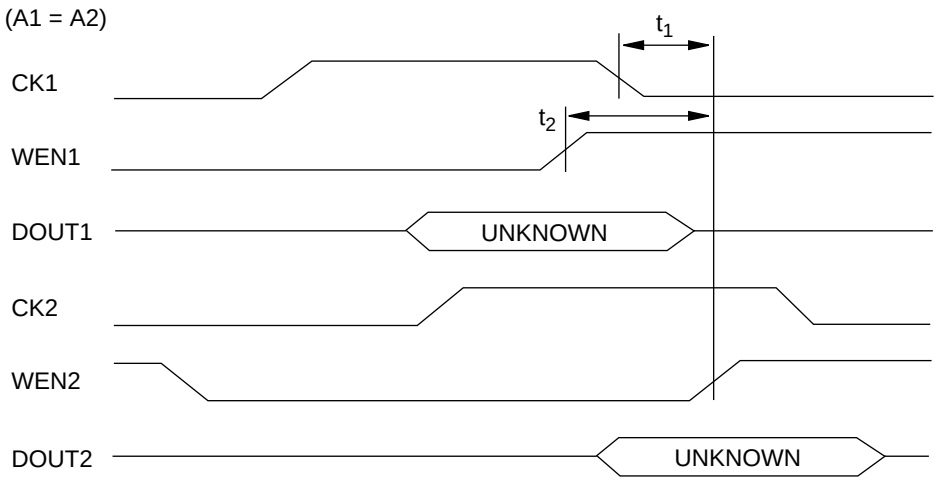
Write–Write Contention (max (t_1, t_2) ≤ t_{wwc} at CK Defined Write Cycle)



(CSN1 / CSN2 / OEN1 / OEN2 : LOW, DI1 / DI2 : VALID)

* If the greater of t_1 or t_2 is smaller than or equal to t_{wwc}, it is Write-Write Contention.
Data stored at current address will be unpredictable.

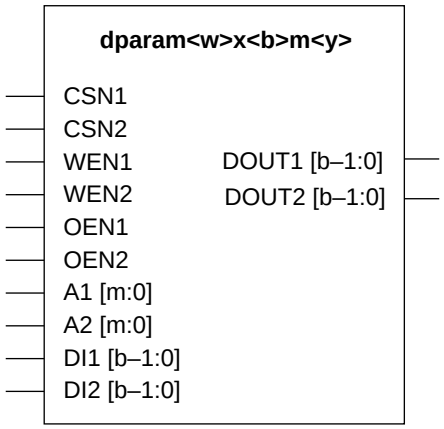
Write–Write Contention (max (t_1, t_2) ≤ t_{wwc} at WEN Defined Write Cycle)



(CSN1 / CSN2 / OEN1 / OEN2 : LOW, DI1 / DI2 : VALID)

* If the greater of t_1 or t_2 is smaller than or equal to t_{wwc}, it is Write-Write Contention. Data stored at current address will be unpredictable.

Logic Symbol



NOTES:

1. Words (w) is the number of words in DPARAM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. $m = \lceil \log_2 w \rceil - 1$

Features

- Asynchronous operation
- Address transition detectors
- Write enable transition detector
- Chip select transition detector
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Flexible aspect ratio
- Up to 64K bits capacity
- Up to 8K number of words
- Up to 64 number of bits per word

Function Description

DPARAM is a dual port asynchronous static RAM. When WEN1 is high, just after the address(A1[ ]) transition, DOUT1[ ] presents the data stored in the location addressed by A1[ ]. Upon WEN1 rising edge, the value of DI1[ ] is written into the location addressed by A1[ ]. CSN1 is used to enable/disable the accesses. OEN1 is used to enable/disable the data output driver. Port2 has the same functionalities as those of port1, and two functionalities are independent of each other.

Generators and Cell Configurations

SPARAM generates layout, netlist, symbol and functional & timing model of a SPARAM. The layout of SPARAM is an automatically generated array of custom, pitch-matched leaf cells. There are four generator parameters to resolve the configuration of a SPARAM.

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y).

The valid range of these parameters is specified in the following table:

Parameters		YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	Min	16	32	64	128
	Max	1024	2048	4096	8192
	Step	8	16	32	64
Bpw (b)	Min	1	1	1	1
	Max	64	32	16	8
	Step	1	1	1	1

DPARAM Gen

Dual-Port Asynchronous RAM Generator

Pin Descriptions

Name	I/O	Description
CSN	I	"Chip Select Negative" acts as the memory enable signal for selecting one of multiple memory blocks. When CSN is high, DOUT[ ] goes to Hi-Z state, the memory goes to stand-by (power down) mode and no access to the memory can occur. Conversely, if CSN is low only then may a read or write access occur. When CSN falls, a read access is initiated. CSN should be stable when WEN is low.
WEN1	I	"Write Enable Negative" selects the type of memory access. When WEN is high, the SPARAM is in read mode. Otherwise, it is in write mode. Upon the rising edge of WEN, a write access completed and a read access initiated. When WEN is low, A[ ] and CSN should be stable.
OEN1	I	"Output Enable Negative" unconditionally enables or disables the output drivers.
A [ ]	I	"Address" selects the location to be accessed. When A[ ] changes, the transition is detected and the internal clock pulse will be generated. A[ ] should be stable when WEN is low.
D [ ]	I	When WEN rises, the "Data In" word value is written to the location addressed.
DOUT [ ]	O	During a read access, the data word stored will be presented to the "Data OUT" ports. DOUT[ ] is tri-statable. When CSN is low and OEN is low, only then, DOUT[ ] drives a certain value. Otherwise, DOUT[ ] keeps Hi-Z state. During a write access, the data on DOUT is unpredictable.

Pin Capacitance

(Unit = SL)

CSN	WEN	OEN	A	DI	DOUT			
					Ymux 4	Ymux 8	Ymux 16	Ymux 32
STD80/STDM80								
11.4	4.9	0.8	4.9	2.4	6.0	13.2	27.5	56.0

Application Notes

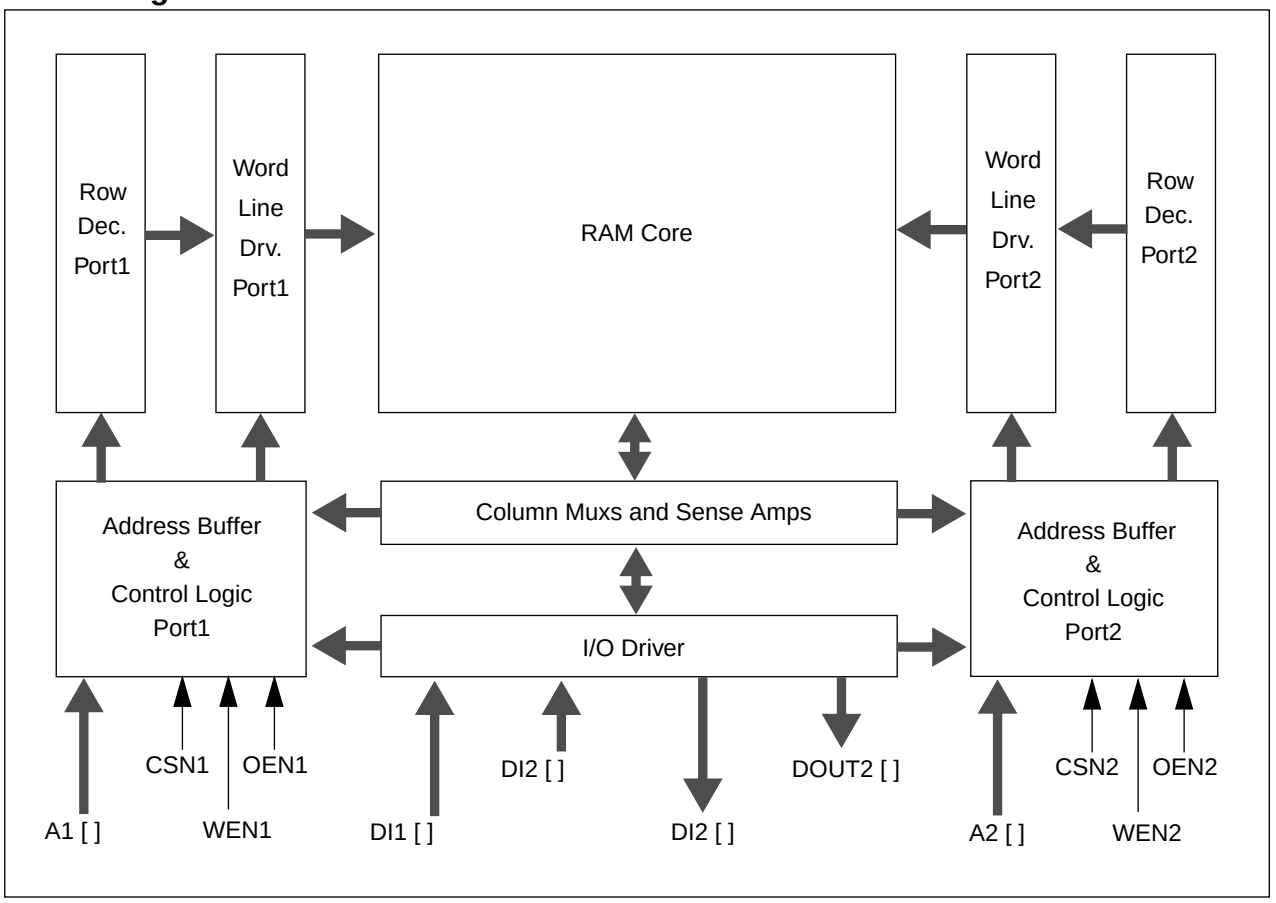
1) Fitting the Layout Shape (Aspect Ratio)

Layout Shape can be fitted by choosing one of 4 Ymux parameters in the above configuration table in accordance with your chip level layout design preference. Larger one makes the layout shape flat and short. Smaller one makes it thin and tall. In general, flat and short DPARAM is faster than thin and tall one.

2) Contention Modes

Simultaneous accesses to the same location through both ports cause a contention. DPARAM has no contention-preventing scheme. User has to take care of the contention modes. Please refer to the timing diagrams of contention modes to get more information of contention modes.

Block Diagram



Characteristic Reference Table

STD80

Symbol	Description	256x16m4	1024x16m8	4Kx16m16
TIMING (Typical process, 5V, 25 ^{O}C, Output load = 10SL, Input slope = 0.2ns Unit = ns)				
t_{acc}	Access Time	6.3	6.7	7.7
t_{da}	Deaccess Time	4.8	4.9	4.9
t_{dz}	Active to Hi-z	0.8	0.8	0.8
t_{zd}	Hi-z to Active	1.7	1.7	1.7
t_{as}	Address Setup Time	0.1	0.1	0.1
t_{ah}	Address Hold Time	1.2	1.5	2.0
t_{ds}	Input Data Setup Time	2.0	2.7	4.1
t_{dh}	Input Data Hold Time	0.9	1.1	1.7
t_{wen}	Minimum WEN Pulse Width Low	3.1	3.4	3.9
t_{cs}	CSN Setup Time	0.1	0.1	0.1
t_{ch}	CSN Hold Time	0.9	0.9	0.9
t_{rwc}	Read-Write Contention Time	6.3	6.8	7.8
t_{wwc}	Write-Write Contention Time	3.1	3.4	3.9
SIZE (μm)				
Width		1239	2013	3562
Height		1075	1770	3158
POWER (μW/MHz)				
power_add (normal mode: CSN Low)		3150	4950	8960
power_csn (stand-by mode: CSN High)		485	855	1595

Characteristic Reference Table

STDM80

Symbol	Description	256x16m4	1024x16m8	4Kx16m16
TIMING (Typical process, 3.3V, 25 ^{o}C, Output load = 10SL, Input slope = 0.2ns Unit = ns)				
t_{acc}	Access Time	9.2	9.9	11.2
t_{da}	Deaccess Time	7.2	7.2	7.3
t_{dz}	Active to Hi-z	1.8	1.8	1.8
t_{zd}	Hi-z to Active	2.4	2.4	2.4
t_{as}	Address Setup Time	0.1	0.1	0.1
t_{ah}	Address Hold Time	1.6	1.9	2.5
t_{ds}	Input Data Setup Time	1.3	1.8	2.8
t_{dh}	Input Data Hold Time	1.2	1.5	2.1
t_{wen}	Minimum WEN Pulse Width Low	4.6	4.9	5.5
t_{cs}	CSN Setup Time	0.1	0.1	0.1
t_{ch}	CSN Hold Time	1.7	1.7	1.7
t_{rwc}	Read-Write Contention Time	9.2	9.9	11.2
t_{wwc}	Write-Write Contention Time	4.6	4.9	5.5
SIZE (μm)				
Width		1239	2013	3562
Height		1075	1770	3158
POWER (μW/MHz)				
power_add (normal mode: CSN Low)		1409	2253	3967
power_csn (stand-by mode: CSN High)		221	380	700

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

STD80 (Typical process, 5V, 25 ^{o}C**)**

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 4
tacc	(1.81e-03*W+4.05e-02*S+1.73e-01*SL*0.019+5.74)
twen	(1.01e-03*W+2.17e-01*S+2.78+5.13e-06*W*S)
	Y = 8
tacc	(9.23e-04*W+6.35e-02*S+1.81e-01*SL*0.019+5.72)
twen	(5.06e-04*W+2.17e-01*S+2.78+2.56e-06*W*S)
	Y = 16
tacc	(4.52e-04*W+5.59e-02*S+1.69e-01*SL*0.019+5.81)
twen	(2.53e-04*W+2.17e-01*S+2.78+1.28e-06*W*S)
	Y = 32
tacc	(2.26e-04*W+5.81e-02*S+1.58e-01*SL*0.019+5.91)
twen	(1.26e-04*W+2.17e-01*S+2.78+6.42e-07*W*S)

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 4
power_add	((0.409*W+24*B+141)/5.0)*VDD^2*F
power_csn	((0.148*W+2.27*B+22.3)/5.0)*VDD^2*F
	Y = 8
power_add	((0.217*W+38.1*B+158)/5.0)*VDD^2*F
power_csn	((0.074*W+4.54*B+22.3)/5.0)*VDD^2*F
	Y = 16
power_add	((0.0886*W+76.9*B+199)/5.0)*VDD^2*F
power_csn	((0.037*W+9.08*B+22.3)/5.0)*VDD^2*F
	Y = 32
power_add	((0.0406*W+150*B+206)/5.0)*VDD^2*F
power_csn	((0.0185*W+18.1*B+22.3)/5.0)*VDD^2*F

NOTES:

1. power_add : This is a normal mode power of memory. When CSN is low.
2. power_csn : This is a standby mode power of memory. When CSN is high.

3) Size Equation [Unit: μm]

Width 12.1*B*Y+464.6
Height 10.85*W/Y+380.75

STDM80 (Typical process, 3.3V, 25 ^{o}C)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 4
tacc	(2.51e-03*W+9.12e-02*S+2.02e-01*SL*0.019+8.47)
twen	(1.16e-03*W+6.54e-02*S+4.25+1.20e-04*W*S)
	Y = 8
tacc	(1.24e-03*W+9.22e-02*S+2.06e-01*SL*0.019+8.51)
twen	(5.83e-04*W+6.54e-02*S+4.25+6.04e-05*W*S)
	Y = 16
tacc	(6.18e-04*W+1.07e-01*S+1.94e-01*SL*0.019+8.61)
twen	(2.91e-04*W+6.54e-02*S+4.25+3.02e-05*W*S)
	Y = 32
tacc	(3.10e-04*W+1.05e-01*S+1.97e-01*SL*0.019+8.73)
twen	(1.45e-04*W+6.54e-02*S+4.25+1.51e-05*W*S)

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 4
power_add	((0.273*W+16.4*B+94.7)/3.3)*VDD^2*F
power_csn	((0.0951*W+1.5*B+18.2)/3.3)*VDD^2*F
	Y = 8
power_add	((0.153*W+27*B+94.5)/3.3)*VDD^2*F
power_csn	((0.0475*W+3.01*B+1.82)/3.3)*VDD^2*F
	Y = 16
power_add	((0.0594*W+51.8*B+130)/3.3)*VDD^2*F
power_csn	((0.0237*W+6.02*B+18.2)/3.3)*VDD^2*F
	Y = 32
power_add	((0.0253*W+105*B+138)/3.3)*VDD^2*F
power_csn	((0.0118*W+12*B+18.2)/3.3)*VDD^2*F

NOTES:

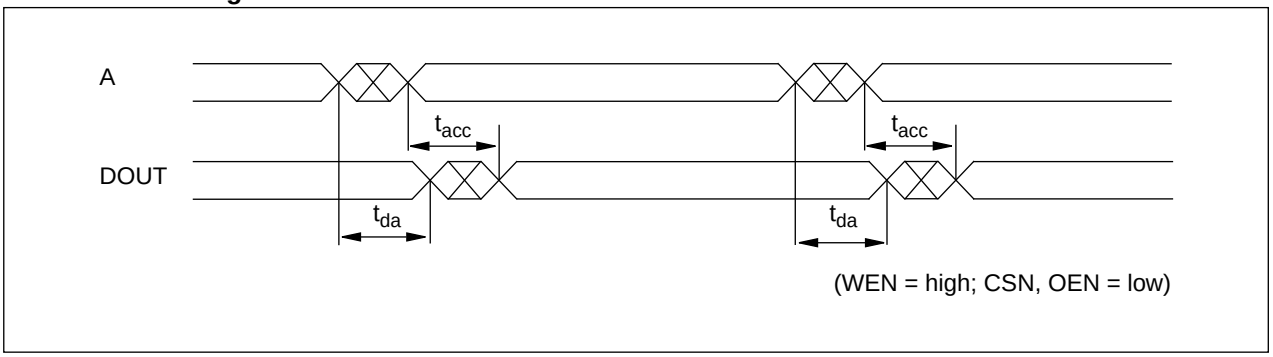
1. power_add : This is a normal mode power of memory. When CSN is low.
2. power_csn : This is a standby mode power of memory. When CSN is high.

3) Size Equation [Unit: μm]

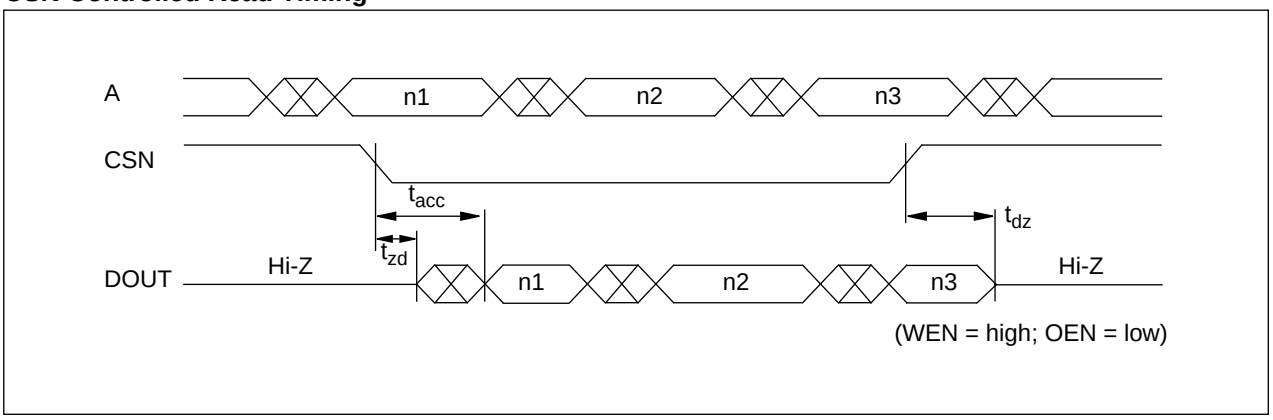
Width 12.1*B*Y+464.6
Height 10.85*W/Y+380.75

Timing Diagrams

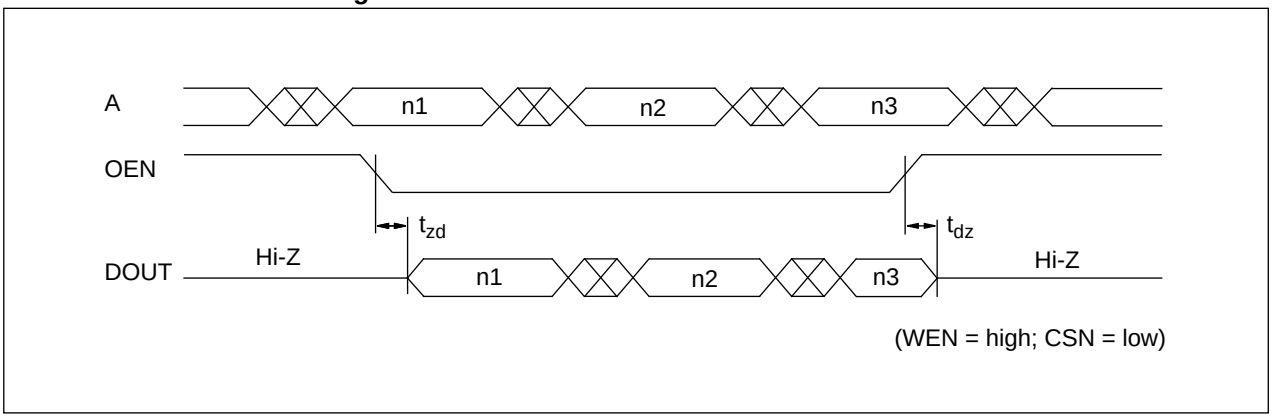
Basic Read Timing



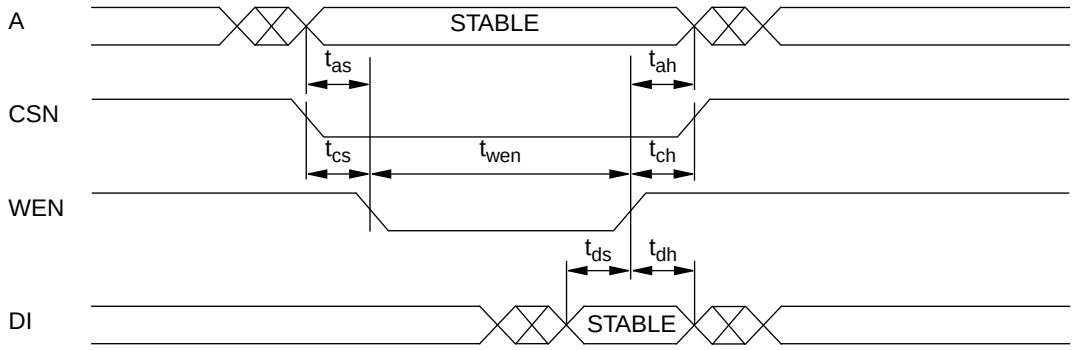
CSN Controlled Read Timing



OEN Controlled Read Timing

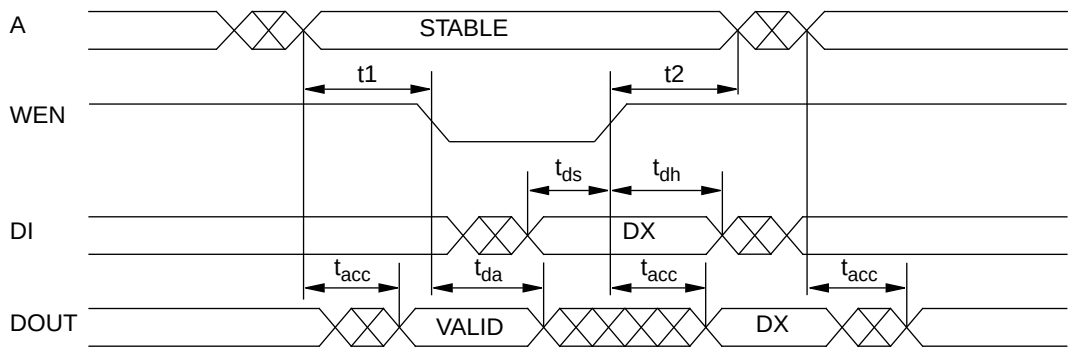


Basic Write Timing



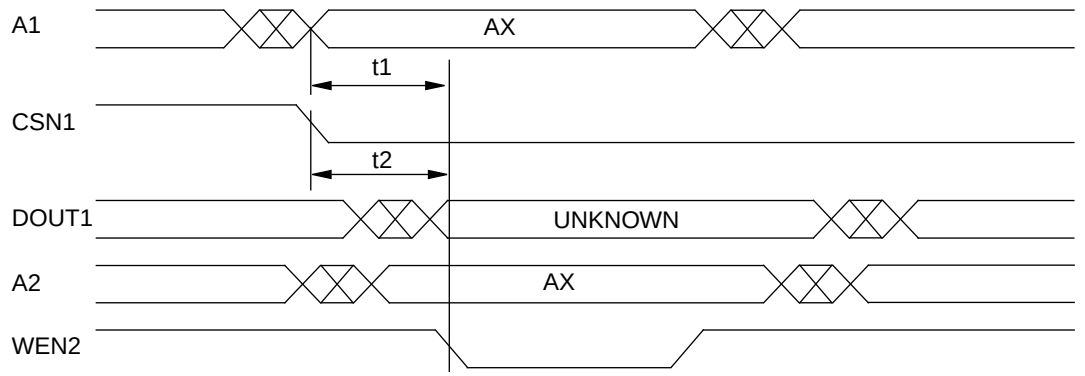
(OEN = Don't Care)

Read-Write-Read Timing (when t1, t2 > tacc)



(CSN, OEN = low)

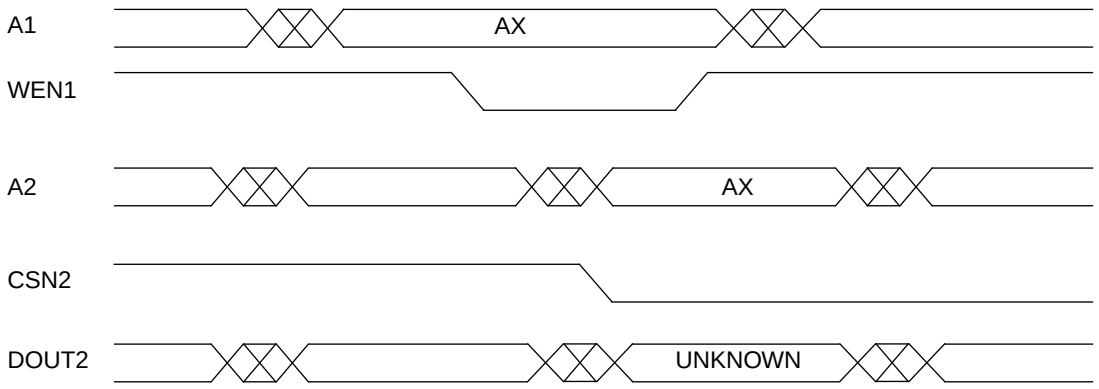
Read-Write Contention (when MIN (t1, t2) <= trwc)



(WEN = high; OEN1,CSN2 = low)

* If the smaller of t1 or t2 is smaller than or equal to Trwc, it is Read-Write Contention.
The read by port1 is invalid, the write by port2 is still valid.

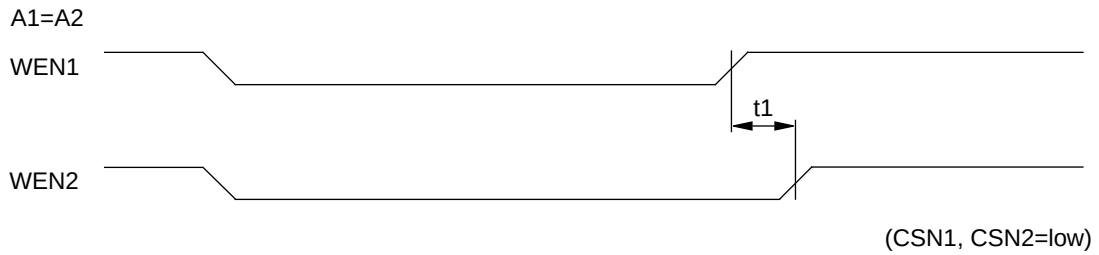
Write-Read Contention



(CSN1, OEN2=low; WEN2=high)

* If read access by port2 begins while WEN1 is low and the addresses of both ports are same, it is Write-Read Contention. The read by port2 is invalid, the write by port1 is still valid.

Write-Write Contention (when t1 <= twwc)



(CSN1, CSN2=low)

* If t1 is smaller than or equal to twwc, it is Write-Write Contention. The data stored at current address will be unpredictable. Regardless of the value of t1, read by port1 after WEN1 rise is invalid. It is a sort of Write-Read Contention.

Datapath Compilers 6

Contents

Overview 6-1

Datapath Compilers Information 6-3

Macro Cells

Adder/Subtracter 6-5

Arithmetic Logic Unit 6-7

Array Multiplier 6-10

Barrel Shifter 6-16

Carry-Select Adder 6-19

Comparator 6-21

Decrementer 6-23

Fast Multiplier 6-25

Incrementer 6-27

Incrementer/Decrementer 6-29

Normalizer 6-31

One Detector 6-33

Parity 6-35

Priority Encoder 6-37

Register File 6-39

Saturating Adder 6-49

Zero Detector 6-51

Logic Cells

AND-OR 6-53

AND-OR-INVERT 6-55

Buffer/Inverter 6-57

Bus Holder 6-59

D Flip-Flop 6-60

Full Adder 6-72

Latch 6-74

Multiplexer 6-82

NAND/AND 6-85

NOR/OR 6-87

OR-AND 6-89

OR-AND-INVERT 6-91

Tri-State Buffer/Inverter 6-93

XNOR/XOR 6-95

OVERVIEW

The datapath cell library is a set of high-level logic elements developed by Samsung ASIC. Datapath cells generate application-specific design libraries that can be used with the datapath place and route tool to construct complex datapaths. The blocks which are produced using datapath cells can then be globally routed using the chip level place and route tool like ArcCell.

Datapath compiler automatically places and routes circuits that have an inherently regular structure. Datapath compiler differs from a standard cell place and route tool in that it enables you to map regularity from a logical design into a layout. With datapath, you can create layouts that are as dense as custom layouts. A typical application of datapath is a multi-bit arithmetic logic function.

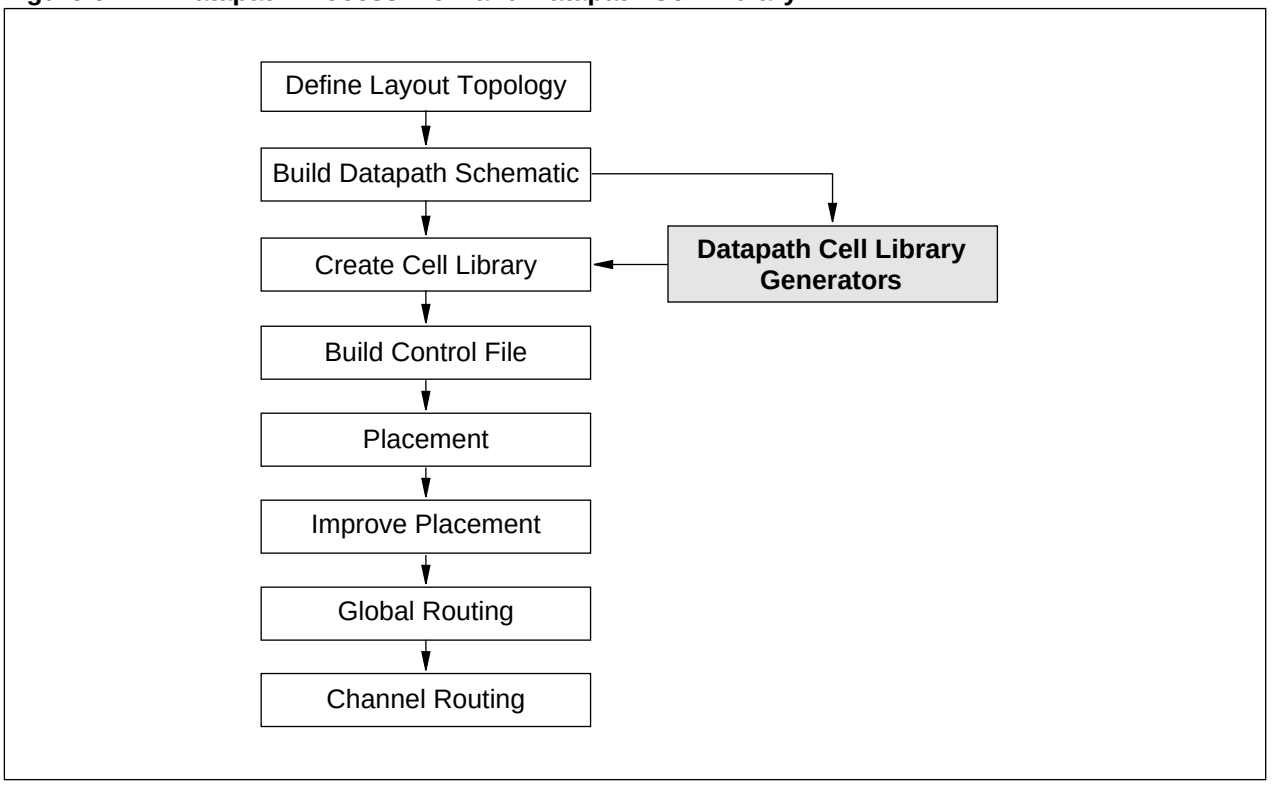
Datapath compiler enables you to:

- Generate schematics automatically according to the user-specific parameters
- Support functional models, test vectors and auto-characterized timing models
- Produce layouts that exhibit modularity and topological regularity
- Control the layout placement and density
- Perform over-the-cell routing and TLM maze routing with channel compaction
- Produce “cap” file and “wire delay” file for back-annotation process.

Datapath Process Flow

The datapath process flow begins the physical design portion of the IC design process. The logic design and circuit analysis have been completed and the next step is to produce a layout for the design. The figure 6-1 illustrates the recommended methodology for using datapath to create a layout for a design and illustrates how the datapath cell library fits into the datapath process flow.

Figure 6-1. Datapath Process Flow and Datapath Cell Library

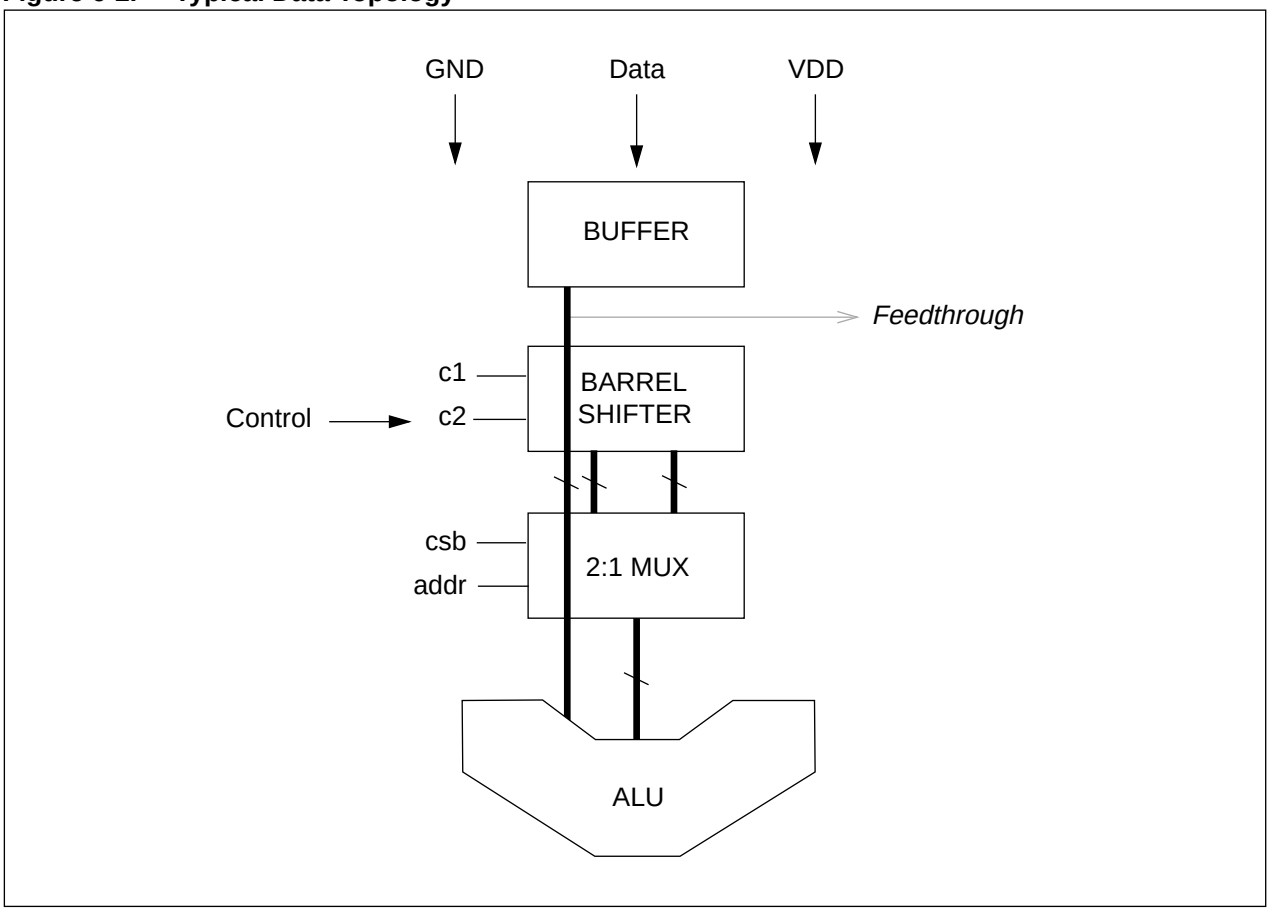


A datapath layout is a two-dimensional array of rows and columns with routing channels between the rows. The orientation of bits and words with respect to rows and columns defines the datapath layout topology.

Feedthrough terminals are the locations on a datapath cell where the datapath router can cross the row without connecting to the cell. Feedthroughs can be built into the cell (that is, the cell contains a vertical wire with a top and bottom terminal that is not connected internal to the cell), or they can be locations where there is sufficient room to route a wire vertically over the cell.

The figure 6-2 illustrates a typical datapath topology.

Figure 6-2. Typical Data Topology



DATAPATH COMPILERS INFORMATION

Macro Cells

Cell Name	Function	Bits	Features
adder	Adder/Subtracter	4 ~ 128	• Ripple/Carry-Bypass Scheme • 2's Complement Overflow Flag
addersat	Saturating Adder	4 ~ 128	• Ripple/Carry-Bypass Scheme • 2's Complement
alu	Arithmetic Logic Unit	4 ~ 128	• 2's Complement Overflow/Carry-Out Flag • 9 Arithmetic, 15 Logical Functions
bs	Barrel Shifter	4 ~ 128	• Transmission Gate Multiplexing Scheme • Bi-Directional Shift or Rotate • Fill Vacant Bits with Data
cmp	Comparator	4 ~ 128	• Less than or Equal Flag & Equal Flag • Greater than or Equal Flag & Equal Flag • Greater than & Equal Flag • Less than & Equal Flag • 2's Complement
csadder	Carry-Select Adder	4 ~ 128	• Double Carry-Select Algorithm • 2's Complement Overflow Flag
dec	Decrementer	4 ~ 128	• Ripple/Carry-Bypass Scheme
enc	Priority Encoder	4 ~ 128	• Detect from LSB/MSB
fmpy	Fast Multiplier	8 ~ 64	• Modified Wallace Tree Architecture • 2's Complement
inc	Incrementer	4 ~ 128	• Ripple/Carry-Bypass Scheme
incdec	Incrementer/Decrementer according to select signal	4 ~ 128	• Ripple/Carry-Bypass Scheme
mpy	Array Multiplier	6 ~ 64	• Supporting Accumulator and Pipes • 2's Complement Multiplication
norm	Normalizer	4 ~ 128	• Outputs Shift Amount and All0 Flag
oned	One Detector	4 ~ 128	• Generating One Flag
parity	Parity Generator	4 ~ 128	• Generating Parity Flag
regf	Register File	8 ~ 128	• Configurable Read (1 ~ 4)/Write (1 ~ 2) • Address Decoders on Either Side of Block
zerod	Zero Detector	4 ~ 128	• Generating Zero Flag

Logic Cells

Cell Name	Function	Bits	Features
ao	AND-OR	4 ~ 128	• Configurable 21 and 22 Types
aoi	AND-OR-INVERT	4 ~ 128	• Configurable 21 and 22 Types
buffer	Buffer/Inverter	4 ~ 128	• Buffers and Inverters
bushldr	Bus Holder	4 ~ 128	• Bus Holder
dff	D Flip-Flop	4 ~ 128	• Negative/Positive Edge Triggered • Scan Logic and Set/Reset Options • Tri-State and Normal Outputs
fadder	Full Adder	4 ~ 128	• Full Adder Array
latch	Transparent Latch	4 ~ 128	• High Input Enable • Scan Logic and Set/Reset Options • Tri-State and Normal Outputs
mux	Multiplexer	4 ~ 128	• Inverting/Non-Inverting • Configurable 2, 3, 4 and 8 Inputs
nand	NAND/AND	4 ~ 128	• Configurable 2, 3 and 4 Inputs
nor	NOR/OR	4 ~ 128	• Configurable 2, 3 and 4 Inputs
oa	OR-AND	4 ~ 128	• Configurable 21 and 22 Types
oai	OR-AND-INVERT	4 ~ 128	• Configurable 21 and 22 Types
tristate	Tri-State Buffer/Inverter	4 ~ 128	• Tri-State Buffers and Inverters
xor	Exclusive OR/NOR	4 ~ 128	• Configurable 2 and 3 Inputs

Features

- Two’s complement or unsigned magnitude operation
- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Simple ripple and sophisticated group bypass scheme
- Two’s complement overflow flag
- *n*-bit (4 to 128) Adder
- Three drive strength options for output

General Description

The Adder/Subtracter builds an *n*-bit wide Adder schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells.

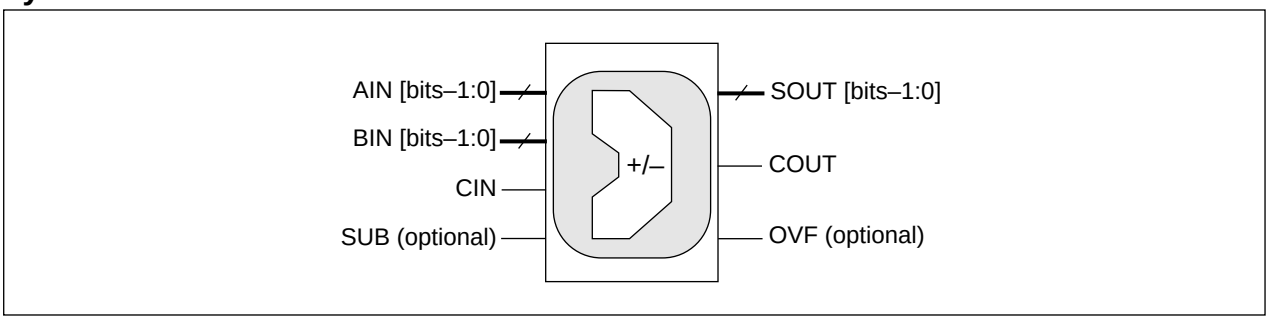
The Adder/Subtracter performs two’s complement addition/subtraction or unsigned magnitude addition. The overflow flag gets set if an overflow occurs while adding two positive or negative numbers. The overflow is ignored while doing unsigned magnitude operations.

Design Description

The Adder/Subtracter performs add/subtract function. An *n*-bit wide operand (AIN), an *n*-bit wide operand (BIN), a 1-bit wide input carry signal (CIN), an *n*-bit wide output bus (SOUT) and 1-bit wide output carry signal (COUT) serve as the I/O signals to the module.

The Adder/Subtracter can be built with two different carry chains allowing speed/area trade-offs. The ripple carry chain is high in density, but low in performance. The carry-bypass chain has a unique grouping of bits which creates a high performance design. This scheme is preferable for the addition of large data words to attain high speed.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
nopass	0: group bypass; 1: ripple adder	0/1
subtract	0: adder; 1: subtracter	0/1
cinlogic	0: CIN ← ~CIN; 1: CIN ← CIN	0/1
overflow	Overflow flag for signed operation	0/1
drv	Drive strength	1/2/4

Adder/Subtracter

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input
BIN [bits–1:0]		Data input
CIN		Carry-in
SUB		It specifies addition/subtraction (optional when the parameter subtract = 1).
SOUT[bits–1:0]	O	Result of addition/subtraction
COUT		It specifies the carry-out of two given numbers.
OVF		Overflow/underflow of signal addition/subtraction (optional when the parameter overflow = 1).

Function Table

Type	Function
Adder	If (cinlogic == 1), SOUT = AIN + BIN + CIN, else SOUT = AIN + BIN + ~CIN
Subtracter	If (cinlogic == 1), SOUT = AIN + ~BIN + CIN, else SOUT = AIN + ~BIN + ~CIN
Overflow	(~SOUT [bits–1]) • (AIN [bits–1] • BIN [bits–1]) + (SOUT [bits–1]) • (~AIN [bits–1]) • (~ BIN [bits–1])

Truth Table

Inputs			Outputs	
AIN	BIN	CIN	SOUT	COUT
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Pin Capacitance

Pin Name	Value (pF)	
	DP80	DPM80
AIN	0.049	0.048
BIN	0.039	0.039
CIN	0.095	0.092

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: nopass = 0, subtract = 0, cinlogic = 1, overflow = 1, drv =1

Library	Bit	Area (μm x μm)		Delay (ns)		Current (mA)
		Width	Height	T_{PLH}	T_{PHL}	
DP80	8	240.5	104.8	2.807	2.303	0.230
	16	451.7	103.4	3.247	2.811	0.439
	24	662.9	107.8	3.447	2.933	0.625
	32	874.1	108.9	3.719	3.501	0.825
DPM80	8	240.5	104.8	4.638	4.312	0.147
	16	451.7	103.4	5.218	4.922	0.279
	24	662.9	107.8	5.668	5.342	0.387
	32	874.1	108.9	5.896	5.620	0.524

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- High performance Arithmetic Logic Unit
- Two’s complement overflow flag
- *n*-bit (4 to 128) Adder used
- Carry-out flag
- Three drive strength options for output

General Description

The Arithmetic Logic Unit builds an *n*-bit wide Arithmetic Logic Unit schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells.

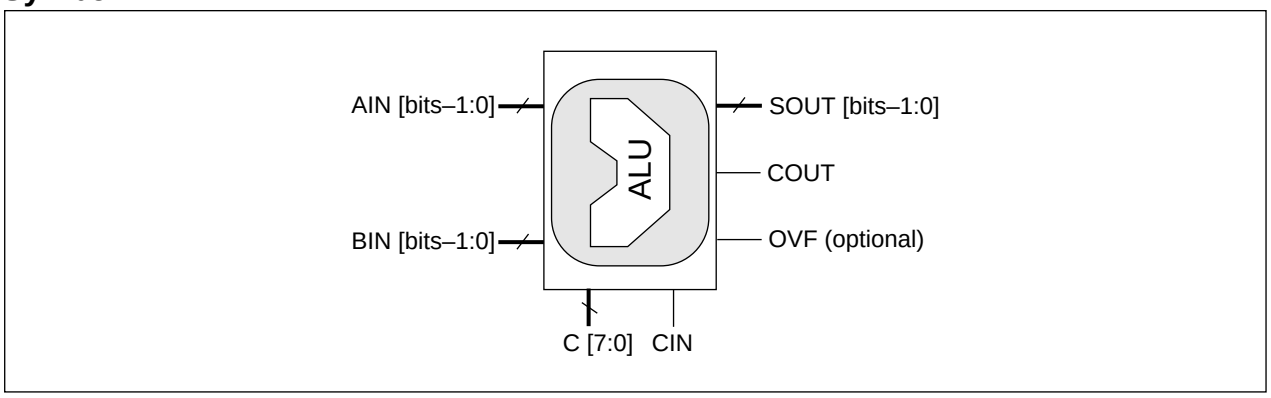
Design Description

The logic circuit produced by the generator performs 15 logical, 9 arithmetic operations. An *n*-bit wide operand (AIN), an *n*-bit wide operand (BIN), a 1-bit wide input carry signal(CIN), an *n*-bit wide output bus(SOUT) and 1-bit output carry signal(COUT) serve as the I/O signals to the module.

The Arithmetic Logic Unit is built with a carry-bypass chain. The carry-bypass chain has a unique grouping of bits which creates a high performance design. This scheme provides high performance for large data words arithmetic operations.

The overflow flag gets set if an overflow occurs while adding two positive or negative numbers. This flag is ignored for unsigned magnitude operations but is important when using the block in two’s complement arithmetic operations.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
overflow	Overflow flag for signed operation	0/1
drv	Drive strength	1/2/4

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input for arithmetic/logical operations
BIN [bits–1:0]		Data input for arithmetic/logical operations
C [7:0]		Operational code control inputs Refer to “opcode” in the function table below.
CIN		Carry-in for arithmetic operations It must be maintained to ‘0’ in a logical operation.
SOUT [bits–1:0]	O	Result of an arithmetic/logical operation
COUT		Carry-out of an arithmetic operation
OVF		Overflow/underflow of a signed addition (optional when the parameter overflow = 1)

Function Table

Logical	Opcode	Arithmetic	Opcode
0	0x00	a + b + CIN	0x76
~a & ~b	0x01	a + ~b + CIN	0xb9
~a & b	0x02	b + ~a + CIN	0xd9
~a	0x03	~a + CIN	0xf3
a & ~b	0x04	~b + CIN	0xf5
~b	0x05	a + CIN	0xfc
a ^ b	0x06	b + CIN	0xfa
~a | ~b	0x07	a – ~CIN	0x33
a & b	0x08	b – ~CIN	0x55
~(a ^ b)	0x09	**NOTE**: While the ALU is not active, it is preferable to keep the opcode to “0x00”. If C input has an improper code, which is not in the above table, it can cause the undesirable power consumption.	
pass b	0x0a		
~a | b	0x0b		
pass a	0x0c		
a | ~b	0x0d		
a | b	0x0e		

Pin Capacitance

Pin Name	Value (pF)	
	DP80	DPM80
AIN	0.045	0.044
BIN	0.091	0.089
CIN	0.069	0.068
C	0.375	0.366

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: overflow = 1, drv =1						
Library	**Bit**	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
		Width	**Height**	**T_{PLH}**	**T_{PHL}**	
DP80	8	240.9	159.2	2.901	2.563	0.155
	16	452.1	155.7	3.291	3.061	0.305
	24	663.3	157.4	3.551	3.213	0.445
	32	874.5	159.1	3.841	3.493	0.592
DPM80	8	240.9	159.2	4.400	4.158	0.155
	16	452.1	155.7	4.990	4.748	0.305
	24	663.3	157.4	5.436	5.218	0.445
	32	874.5	159.1	5.856	5.638	0.592

Array Multiplier

Features

- Functional model, test-vector, schematic and layout generators
- Timing model with auto-characterization
- High speed and density
- Two’s complement multiplication

General Description

The Array Multiplier can be optimized for multiple-targeted technologies. The Array Multiplier can build Multipliers from 6-bits to 64-bits with an accumulator, a configurable size of output buffer and a pipe.

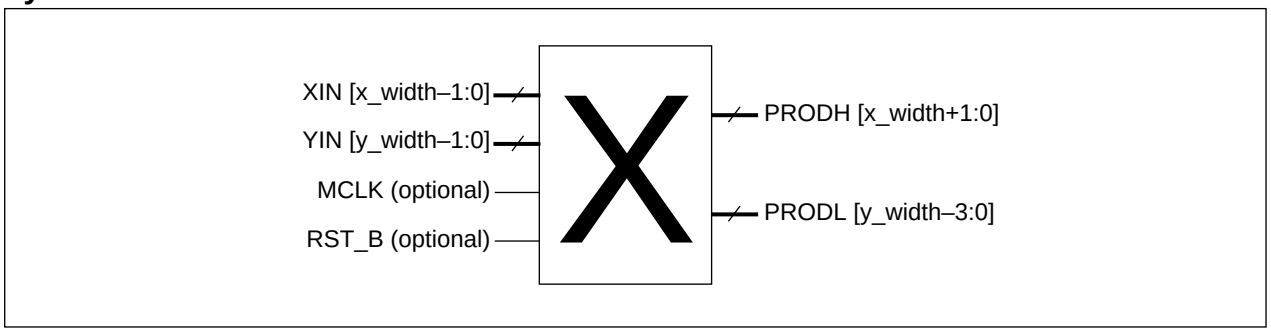
Design Description

The Array Multiplier uses the modified Booth’s algorithm to encode the multiplier bits by partitioning the bits into three bit groups, with one bit shared between groups and performing the desired operation as required by the algorithm. The use of the modified Booth’s algorithm reduces by half the number of partial products formed.

You can insert one pipeline stage, which increases the efficiency of the multiplier. The MSB adder used in the design is a fast group bypass adder and does not require pipes. The LSB adder is programmable to take pipes and is, therefore, the adder array. The clocks to the pipeline control how the internal data changes so that the data is always stable throughout the clock period and there is no hold problem.

The multiplier and the multiplicand are programmable in increments by the two bits from a minimum of 6 bits to a maximum of 64 bits.

Symbol



Parameter Description

Parameter Name	Description	Range
x_width*	Multiplicand bits (the x-input width)	6 to 64 even
y_width	Multiplier bits (the y-input width)	6 to 64 even
pipes	Pipeline stage	0/1
accum	0: none; n: (x_width+n) bit accumulator	0/1/2/3/4
obuff	1: 6x output buffer; 2: 12x output buffer	1/2

* x_width should be greater than or equal to y_width ($x \geq y$).

Pin Description

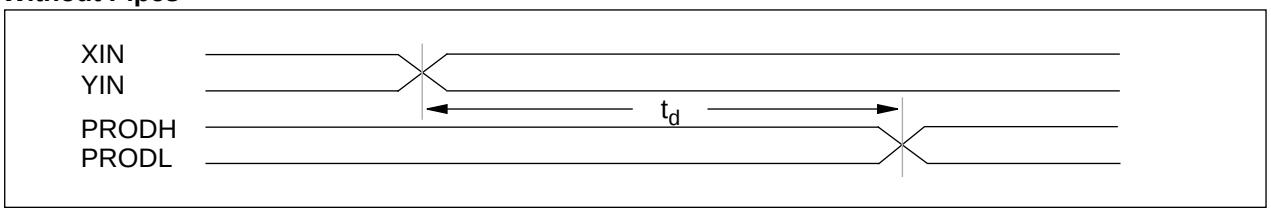
Pin Name	I/O	Description
XIN [x_width–1:0]	I	Data input – Multiplicand
YIN [y_width–1:0]		Data input – Multiplier
MCLK		Clock input to the latches used in the design (optional when pipes = 1 or accum ≥ 1)
RST_B		Input reset line for the latches (active high). If the multiplier has an accumulator, the reset lines ensure that the contents of the accumulator is zero before the first set of XIN * YIN arrives to the accumulator (optional when pipes = 1 or accum ≥ 1).
PRODH [x_width+1:0]	O	Data output lines from the MSB adder. The values of these lines together with the prodL values gives the output data (product).
PRODL [y_width–3:0]		Data output lines from the LSB adder

Pin Capacitance

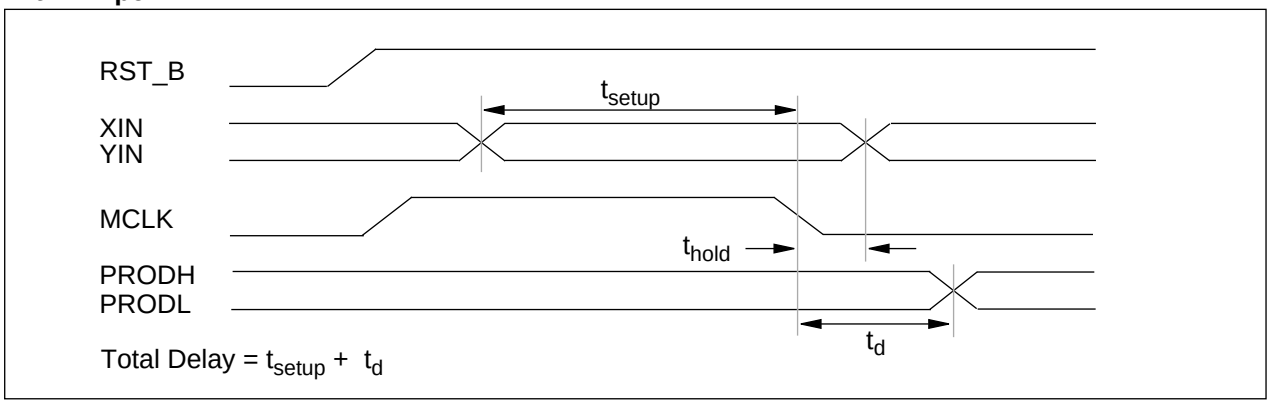
Pin Name	Value (pF)	
	DP80	DPM80
XIN	0.082	0.080
YIN	0.078	0.076

Timing Diagram

Without Pipes



With 1 Pipe



Timing Parameters (With 1 Pipe)

Symbol	Description	Inputs	Outputs
t_{setup}	Input stage delay – Setup time	XIN, YIN	–
t_{hold}	Input state delay – Hold time	XIN, YIN	–
t_d	Output state delay	–	PRODH, PRODL

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Without Pipes

Parameters: io_latch = 0, accum =0, obuff = 1, met_layer = 3, pipe=0						
Library	**Bit**	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
		Width	**Height**	**T_{PLH}**	**T_{PHL}**	
DP80	8 x 8	290.4	413.6	5.524	5.354	0.600
	16 x 8	501.6	413.6	5.553	5.582	–
	16 x 16	501.6	673.6	7.762	7.672	2.830
	24 x 8	765.6	413.6	5.893	5.693	–
	24 x 16	765.6	673.6	7.902	7.772	–
	24 x 24	765.6	967.6	10.022	9.892	4.791
	32 x 8	976.8	413.6	6.363	6.193	–
	32 x 16	976.8	673.6	8.062	7.912	–
	32 x 24	976.8	967.6	10.192	10.032	–
	32 x 32	976.8	1237.6	12.162	12.164	7.560
DPM80	8 x 8	290.4	413.6	8.604	8.492	0.364
	16 x 8	501.6	413.6	8.794	8.952	–
	16 x 16	501.6	673.6	11.654	11.762	1.627
	24 x 8	765.6	413.6	9.144	9.162	–
	24 x 16	765.6	673.6	11.854	12.062	–
	24 x 24	765.6	967.6	14.754	14.862	2.815
	32 x 8	976.8	413.6	9.714	9.732	–
	32 x 16	976.8	673.6	12.254	12.162	–
	32 x 24	976.8	967.6	15.154	15.062	–
	32 x 32	976.8	1237.6	18.054	17.962	4.468

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

With 1 Pipe

Parameters: io_latch = 0, accum =0, obuff = 1, met_layer = 3, pipe=1					
Library	**Bit**	**Area (μm x μm)**		**Delay (ns)**	
		Width	**Height**	**T_{PLH}**	**T_{PHL}**
DP80	8 x 8	290.4	531.5	5.230	5.080
	16 x 8	501.6	531.5	5.940	5.730
	16 x 16	501.6	826.7	6.740	6.530
	24 x 8	765.6	531.5	6.152	5.952
	24 x 16	765.6	826.7	6.952	6.752
	24 x 24	765.6	1163.2	7.822	7.672
	32 x 8	976.8	531.5	6.652	6.482
	32 x 16	976.8	826.7	7.452	7.282
	32 x 24	976.8	1163.2	8.322	8.142
	32 x 32	976.8	1469.8	9.232	9.082
DPM80	8 x 8	290.4	531.5	7.804	7.732
	16 x 8	501.6	531.5	8.904	8.762
	16 x 16	501.6	826.7	10.234	10.092
	24 x 8	765.6	531.5	9.326	9.214
	24 x 16	765.6	826.7	10.626	10.534
	24 x 24	765.6	1163.2	12.126	12.034
	32 x 8	976.8	531.5	10.066	10.074
	32 x 16	976.8	826.7	11.426	11.434
	32 x 24	976.8	1163.2	12.826	12.834
	32 x 32	976.8	1469.8	14.326	14.334

Timing Requirements

With 1 Pipe

Parameters: io_latch = 0, accum =0, obuff = 1, met_layer = 3, pipe=1			
Size	**Timing Field**	**Value (ns)**	
		DP80	**DPM80**
8X8	min_pulse_width_high MCLK	0.630	0.756
	min_pulse_width_low MCLK	0.661	1.050
	min_pulse_width_low RST_B	0.909	1.360
	hold_falling XIN MCLK	0.227	0.299
	hold_falling YIN MCLK	0.042	–0.040
	setup_falling XIN MCLK	2.720	3.710
	setup_falling YIN MCLK	3.170	4.520
16 x 8	min_pulse_width_high MCLK	0.913	1.140
	min_pulse_width_low MCLK	0.854	1.330
	min_pulse_width_low RST_B	1.360	2.010
	hold_falling XIN MCLK	0.321	0.462
	hold_falling YIN MCLK	0.042	–0.040
	setup_falling XIN MCLK	2.720	3.710
	setup_falling YIN MCLK	3.280	4.660
16 x 16	min_pulse_width_high MCLK	0.913	1.140
	min_pulse_width_low MCLK	0.854	1.330
	min_pulse_width_low RST_B	1.360	2.010
	hold_falling XIN MCLK	0.285	0.405
	hold_falling YIN MCLK	0.042	–0.040
	setup_falling XIN MCLK	3.490	4.890
	setup_falling YIN MCLK	4.000	5.740
24 x 8	min_pulse_width_high MCLK	0.744	0.951
	min_pulse_width_low MCLK	0.773	1.240
	min_pulse_width_low RST_B	1.130	1.760
	hold_falling XIN MCLK	0.320	0.465
	hold_falling YIN MCLK	0.042	–0.040
	setup_falling XIN MCLK	2.720	3.710
	setup_falling YIN MCLK	3.300	4.780
24 x 16	min_pulse_width_high MCLK	0.744	0.951
	min_pulse_width_low MCLK	0.773	1.240
	min_pulse_width_low RST_B	1.130	1.760
	hold_falling XIN MCLK	0.284	0.408
	hold_falling YIN MCLK	0.042	–0.040
	setup_falling XIN MCLK	3.490	4.890
	setup_falling YIN MCLK	4.020	5.860

Timing Requirements (Cont.)

With 1 Pipe (Cont.)

Parameters: io_latch = 0, accum =0, obuff = 1, met_layer = 3, pipe=1			
Size	**Timing Field**	**Value (ns)**	
		DP80	**DPM80**
24 x 24	min_pulse_width_high MCLK	0.744	0.951
	min_pulse_width_low MCLK	0.773	1.240
	min_pulse_width_low RST_B	1.130	1.760
	hold_falling XIN MCLK	0.248	0.351
	hold_falling YIN MCLK	0.042	–0.040
	setup_falling XIN MCLK	4.280	6.070
	setup_falling YIN MCLK	4.750	6.940
32 x 8	min_pulse_width_high MCLK	0.880	1.150
	min_pulse_width_low MCLK	0.869	1.390
	min_pulse_width_low RST_B	1.350	2.110
	hold_falling XIN MCLK	0.370	0.561
	hold_falling YIN MCLK	0.042	–0.040
	setup_falling XIN MCLK	2.720	3.710
	setup_falling YIN MCLK	3.410	4.890
32 x 16	min_pulse_width_high MCLK	0.880	1.150
	min_pulse_width_low MCLK	0.869	1.390
	min_pulse_width_low RST_B	1.350	2.110
	hold_falling XIN MCLK	0.334	0.504
	hold_falling YIN MCLK	0.042	–0.040
	setup_falling XIN MCLK	3.490	4.890
	setup_falling YIN MCLK	4.130	5.970
32 x 24	min_pulse_width_high MCLK	0.880	1.150
	min_pulse_width_low MCLK	0.869	1.390
	min_pulse_width_low RST_B	1.350	2.110
	hold_falling XIN MCLK	0.298	0.447
	hold_falling YIN MCLK	0.042	–0.040
	setup_falling XIN MCLK	4.280	6.070
	setup_falling YIN MCLK	4.860	7.060
32X32	min_pulse_width_high MCLK	0.880	1.150
	min_pulse_width_low MCLK	0.869	1.390
	min_pulse_width_low RST_B	1.350	2.110
	hold_falling XIN MCLK	0.262	0.390
	hold_falling YIN MCLK	0.042	–0.040
	setup_falling XIN MCLK	5.230	7.260
	setup_falling YIN MCLK	5.640	8.180

Barrel Shifter

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- High performance Barrel Shifter
- *n*-bit (4 to 128) Shifter
- Transmission gate multiplexing scheme
- Bi-directional shift, fill vacant bits with data, or rotates
- Three drive strength options for output

General Description

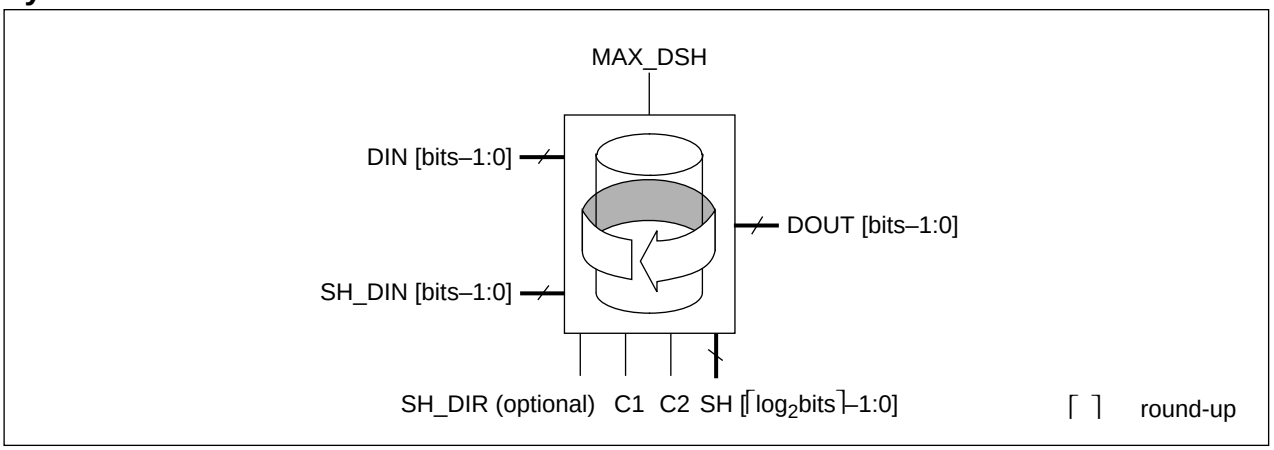
The Barrel Shifter builds an n-bit wide Barrel Shifter schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leafcells. The Barrel Shifter can shift and rotate input signals in either direction. The direction of the shift can be chosen between MSB(LEFT) and LSB(RIGHT) of the bit string. The Barrel Shifter supports both arithmetic and logical shift operations.

Design Description

The Barrel Shifter is constructed as a series of cascaded 2-to-1 and 4-to-1 multiplexers. In its largest configuration (128 bits), three rows of 4-to-1 and one row of 2-to-1 MUXs are used. The architecture is based on a left-shifter block, a right-shifter block, a fill block and a direction block.

Data can be shifted left or right; the vacant bits are padded with zeros during a left shift and can be padded with MSB of the shift data bus during a right shift. A shift data bus (SH_DIN) fills the vacant bits during a shift operation. During a right shift, the shift data bus fills the vacant bits with data from the LSB of the shift data bus; during a left shift, the shift data bus fills the vacant bits with data from the MSB of the shift data bus (essentially a circular shift).

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Direction of shift	LEFT/RIGHT/BOTH
drv	Drive strength	1/2/4

Pin Description

Pin Name	I/O	Description
DIN [bits–1:0]	I	Data input
SH_DIN [bits–1:0]		Shift data input
SH_DIR		Shift direction (Left/Right) (optional when the parameter type = BOTH)
C1, C2		Control signals
SH [$\lceil \log_2 bits \rceil$–1:0]		Shift amount (in binary)
MAX_DSH		It fills data output with filling information according to C1 and C2. It refreshes output with fill data.
DOUT [bits–1:0]	O	Data output

⌈ ⌉ round-up

Function Table

SH_DIR	C1	C2	DOUT
0	0	0	Shift right and fill with zeros
0	1	0	Shift right and fill with data bus (SH_DIN)
1	0	0	Shift left and fill with zeros
1	1	0	Shift left and fill with data bus (SH_DIN)
0	0	1	Shift right and fill with MSB
1	1	1	Left rotation
0	1	1	Right rotation

Pin Capacitance

Pin Name	Value (pF)	
	DP80	DPM80
C1	0.057	0.057
C2	0.083	0.081
DIN	0.268	0.250
MAX_DSH	0.073	0.072
SH	0.192	0.184
SH_DIN	0.043	0.042
SH_DIR	0.042	0.041

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: type = BOTH, drv = 1						
Library	**Bit**	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
		Width	**Height**	**T_{PLH}**	**T_{PHL}**	
DP80	8	264.0	295.0	3.251	2.344	0.116
	16	475.2	376.9	3.521	2.544	0.223
	24	686.4	481.1	4.111	2.954	0.438
	32	897.6	517.1	4.281	3.014	1.041
DPM80	8	264.0	295.0	4.856	2.356	0.068
	16	475.2	376.9	5.256	2.967	0.135
	24	686.4	481.1	6.076	3.896	0.261
	32	897.6	517.1	6.316	4.286	0.477

Features

- Two’s complement or unsigned magnitude operation
- Functional model, test vector, schematic, and layout generators
- Timing model with auto-characterization
- Sophisticated double carry-select algorithm
- Two’s complement overflow flag
- *n*-bit (4 to 128) Adder
- Three drive strength options for output

General Description

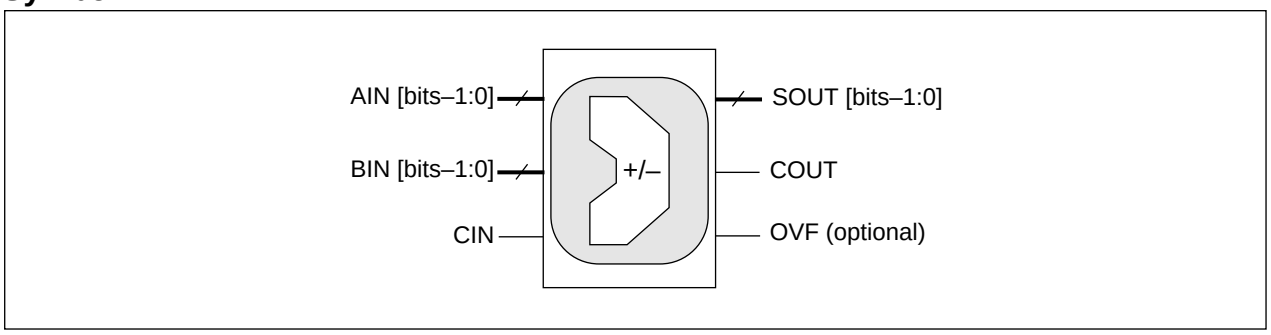
The Carry-Select Adder performs two’s complement addition or unsigned magnitude operation. The high performance Carry-Select Adder design can have layout leaf cells optimized for multiple-targeted technologies. The overflow flag gets set if an overflow occurs while adding two positive or negative numbers. The overflow is ignored for unsigned magnitude operations.

Design Description

The Carry-Select Adder performs high speed binary addition by using a sophisticated double carry-select algorithm with group delay equalization for carry propagation. The outer carry-select scheme is used to provide a short path between the low order inputs and the high order outputs. The internal carry-select schemes are placed within these blocks to reduce their block propagation delays. The sizes of the carry-select blocks increase along the carry propagation tree to produce a fast addition. An *n*-bit wide operand (AIN), an *n*-bit wide operand (BIN), a 1-bit wide input carry signal (CIN), and an *n*-bit wide output bus (SOUT) and 1-bit output carry signal (COUT) serve as the I/O signals to the module. The generated layout is constrained to four rows of cells for minimal area consumption.

This fast Carry-Select Adder is configured for your highest performance applications and outperforms normal Carry-Select Adders by modulating the size of the groups to equalize carry propagation delay, and by providing a second level of carry-select scheme.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of Carry-Select Adder instance to be generated	Any string
bits	Number of bits in the input data bus	4 to 128
overflow	It determines whether overflow output is present; 0: no overflow; 1: overflow	0/1
drv	Drive strength	1/2/4

Carry-Select Adder

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Input data word
BIN [bits–1:0]		Input data word
CIN		Carry-in
SOUT [bits–1:0]	O	Sum output (AIN + BIN + CIN)
COUT		Carry-out
OVF		Overflow output occurs during a signed addition (optional when the parameter overflow = 1).

Function Table

Type	Function
Adder	AIN + BIN + CIN
Overflow	(~SOUT [bits–1]) • (AIN [bits–1] • BIN [bits–1]) + (SOUT [bits–1]) • (~AIN [bits–1]) • (~BIN [bits–1])

Truth Table

Inputs			Outputs	
AIN	BIN	CIN	SOUT	COUT
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Pin Capacitance

Pin Name	Value (pF)	
	DP80	DPM80
AIN	0.077	0.076
BIN	0.071	0.071
CIN	0.061	0.059

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: overflow = 0, drv = 1						
Library	Bit	Area (µm x µm)		Delay (ns)		Current (mA)
		Width	Height	T_{PLH}	T_{PHL}	
DP80	8	240.5	146.8	2.232	2.046	0.427
	16	451.7	149.5	2.693	2.527	0.884
	24	662.9	151.3	3.085	2.857	1.352
	32	874.1	151.3	3.143	2.967	1.817
DPM80	8	240.5	146.8	3.388	3.082	0.216
	16	451.7	149.5	4.068	3.762	0.451
	24	662.9	151.3	4.571	4.289	0.694
	32	874.1	151.3	4.847	4.541	0.930

Features

- Functional model, test vector, schematic, and layout generators
- Timing model with auto-characterization
- Fast signed comparison
- Less than or equal and equal flags
- Greater than or equal and equal flags
- Greater than and equal flags
- Less than and equal flags
- *n*-bit (4 to 128) Comparator

General Description

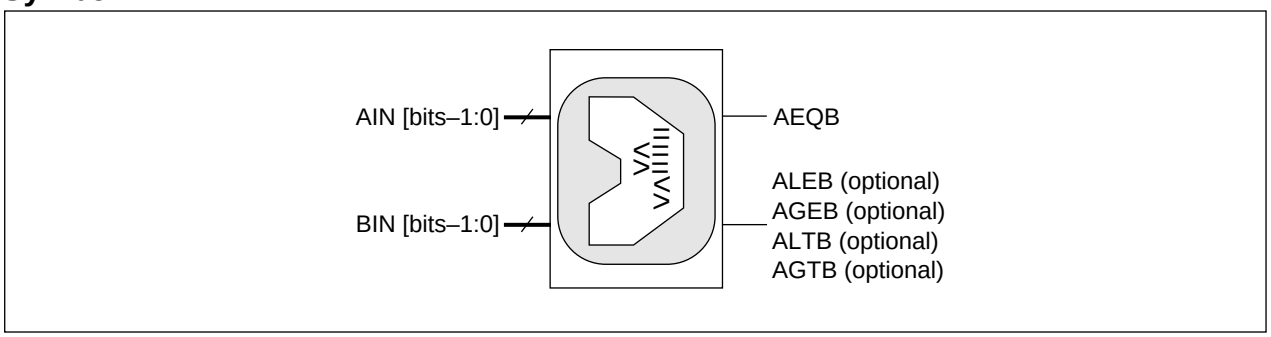
The Comparator builds an *n*-bit wide Comparator schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells. The Comparator supports signed comparisons.

Design Description

The logic circuit produced by the generator produces two different flags according to options.
In case of Greater than or Equal and Equal Flags (A ≥ B and A = B), two *n*-bit wide data operands (AIN, BIN) and two 1-bit wide outputs (AGEB, AEQB) serve as the I/O signals to the module. In case of Less than or Equal and Equal Flags (A ≤ B and A = B), two 1-bit wide outputs (ALEB, AEQB) serve as the I/O signals to the module. In case of Greater than and Equal Flags (A > B and A = B), two 1-bit wide outputs (AEQB, AGTB) serve as the I/O signals to the module. In case of Less than and Equal Flags (A < B and A = B), two 1-bit wide outputs (ALTB and AEQB) serve as the I/O signals to the module.

The Comparator is built with a unique carry-bypass chain. The carry-bypass chain has a unique grouping of bits which modulates the group sizes to minimize carry propagation delay, which creates a high performance design. This scheme is optimized for the comparison of large data words to attain high speed.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Type of flags to be generated – 0: LE, 1: GE, 2: LT, 3: GT	0/1/2/3
drv	Drive Strength	1/2/4

Comparator

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input bus A
BIN [bits–1:0]		Data input bus B
AEQB	O	Equality flag (A = B) that specifies the signed equality of input busses
ALEB (optional)		Less than or Equal to flag (A ≤ B)
AGEB (optional)		Greater than or Equal to flag (A ≥ B)
ALTB (optional)		Less than flag (A < B)
AGTB (optional)		Greater than flag (A > B)

Function Table

Type	Function
AEQB (equal)	==
ALEB (less than or equal)	<=
AGEB (greater than or equal)	>=
ALTB (less than)	<
AGTB (greater than)	>

Pin Capacitance

Pin Name	Value (pF)	
	DP80	DPM80
AIN	0.072	0.072
BIN	0.075	0.075

Truth Table

Inputs		Outputs				
AIN	BIN	AEQB	ALEB	AGEB	AGTB	ALTB
0	0	1	1	1	0	0
0	1	0	1	0	0	1
1	0	0	0	1	1	0
1	1	1	1	1	0	0

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: type = 1, drv = 1						
Library	Bit	Area (μm x μm)		Delay (ns)		Current (mA)
		Width	Height	T_{PLH}	T_{PHL}	
DP80	8	213.2	105.3	2.651	2.433	0.099
	16	424.4	108.7	2.439	1.831	0.184
	24	635.6	112.3	2.671	2.453	0.248
	32	846.8	110.7	3.109	2.051	0.340
DPM80	8	213.2	105.3	4.878	4.586	0.058
	16	424.4	108.7	4.714	4.378	0.107
	24	635.6	112.3	4.898	4.606	0.143
	32	846.8	110.7	5.504	5.178	0.195

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Simple ripple and sophisticated carry-bypass scheme
- *n*-bit (4 to 128) Decrementer
- Buffered carry path
- Three drive strengths on output

General Description

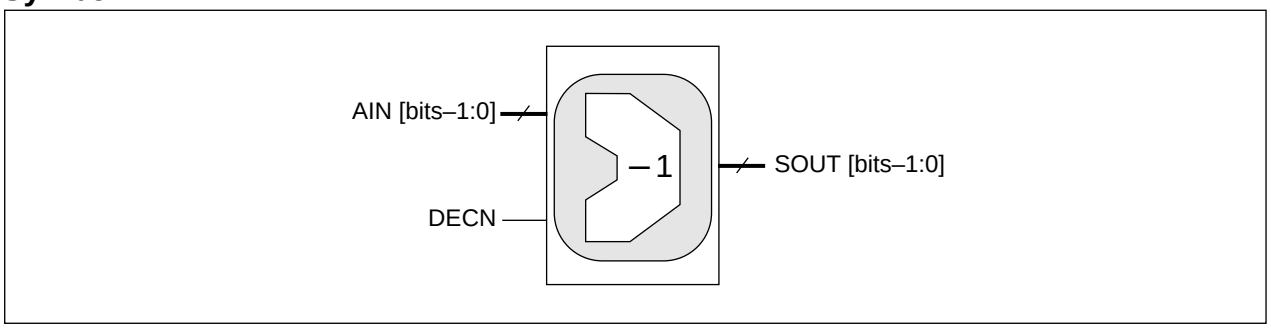
The Decrementer builds an *n*-bit wide Decrementer schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells. The Decrementer supports signed decrements.

Design Description

The logic circuit produced by the generator performs decrement functions. An *n*-bit wide operand (AIN), a 1-bit wide input carry signal (DECN), and an *n*-bit wide output bus (SOUT) serve as the I/O signals to the module.

The Decrementer is built with a unique carry-bypass chain. The carry-bypass chain has a unique grouping of bits which modulates the group sizes to minimize delay which creates a high performance design. This scheme is optimized for the decrement of large data words to attain high speed.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
nopass	0: group bypass; 1: ripple adder	0/1
drv	Drive strength	1/2/4

Decrementer

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input
DECN		Decrement signal which is active low
SOUT [bits–1:0]	O	Data output – Result of decrementer

Function Table

Type	Function
Decrementer	AIN – 1

Truth Table

Inputs		Output
AIN	**DECN**	**SOUT**
0	1	0
1	1	1
0	0	1
1	0	0

Pin Capacitance

Pin Name	Value (pF)	
	DP80	**DPM80**
AIN	0.023	0.023
DECN	0.095	0.092

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: nopass = 0, drv = 1						
Library	**Bit**	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
		Width	**Height**	**T_{PLH}**	**T_{PHL}**	
DP80	8	213.2	94.5	2.449	2.165	0.095
	16	424.4	96.7	2.825	2.207	0.207
	24	635.6	99.8	3.027	2.809	0.240
	32	846.8	99.8	3.225	2.607	0.315
DPM80	8	213.2	94.5	3.890	3.574	0.061
	16	424.4	96.7	4.473	4.157	0.125
	24	635.6	99.8	4.747	4.475	0.156
	32	846.8	99.8	5.063	4.737	0.203

Features

- Functional model, test vector, schematic and layout generator
- Timing model with auto-characterization
- Fastest architecture for large multipliers
- Supports two’s complement multiplication
- Three drive strength options for output

General Description

The Fast Multiplier can be optimized for multiple-targeted technologies. The Fast Multiplier can build Multipliers from 8-bits to 64-bits. There are output buffers which can be varied to three drive strengths.

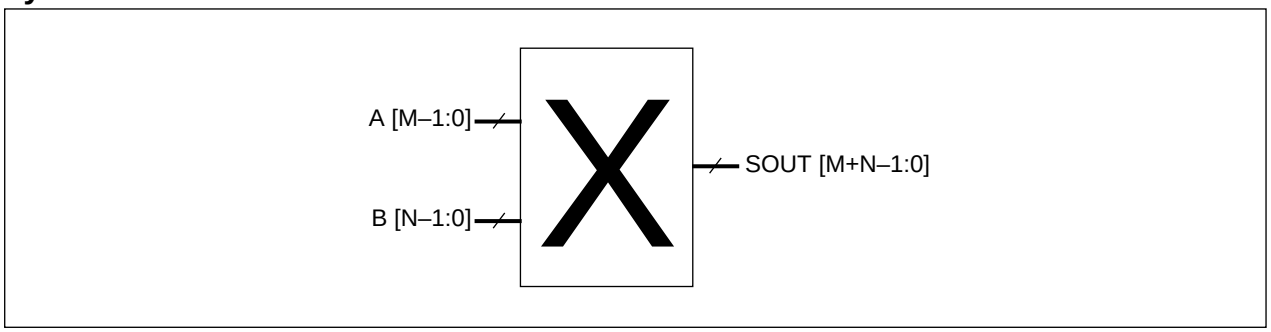
Design Description

The Fast Multiplier is based on a modified Wallace tree architecture, using the Baugh-Wooley algorithm to sum partial products for signed multiplication.

The traditional Wallace tree depends on a Carry Save Adder (CSA) which reduces three partial products to two redundant outputs (Sum, Carry). The modified Wallace tree architecture is based on a 4-2 Carry Save Adder (CSA42). The CSA42 reduces four partial products to two redundant outputs. This architecture reduces the number of partial products by two at each stage of the Wallace tree so that the core of a 32 x 32 multiplication can be achieved in four CSA42 delays.

The final sum (MSB) is generated by adding the final two redundant products from the multiplier core (Sum, Carry). The MSB adder uses a double carry select architecture to generate the final sum.

Symbol



Parameter Description

Parameter Name	Description	Range
M	Multiplicand bits (x-input width)	Refer to the note.
N	Multiplier bits (y-input width)	Refer to the note.
drv	1x/2x/4x output drive strength	1/2/4

NOTES: If M >= N, M = N, N+1, N+2, ..., 126 where N = 8, 12, 16, 20, 24, 32, 40 and 64
If M <= N, N = M, M+1, M+2, ..., 126 where M = 8, 12, 16, 20, 24, 32, 40 and 64

Fast Multiplier

Pin Description

Pin Name	I/O	Description
A [M–1:0]	I	Data input – Multiplicand
B [N–1:0]		Data input – Multiplier
SOUT [M+N–1:0]	O	Data output – Result

Pin Capacitance

Pin Name	Value (pF)	
	DP80	DPM80
A	0.040	0.039
B	0.040	0.039

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: drv = 1						
Library	N x M	Area (μm x μm)		Delay (ns)		Current (mA)
		Width	Height	T_{PLH}	T_{PHL}	
DP80	8 x 8	689.0	485.8	4.807	4.417	0.981
	8 x 16	900.2	484.7	5.987	5.577	–
	8 x 24	689.0	485.8	6.177	5.777	–
	8 x 32	900.2	484.7	6.377	5.967	–
	16 x 16	689.0	485.8	6.517	6.127	8.073
	16 x 24	900.2	484.7	7.297	6.907	–
	16 x 32	689.0	485.8	7.227	6.837	–
	24 x 24	900.2	484.7	7.717	7.327	8.946
	24 x 32	689.0	485.8	7.897	7.507	–
	32 x 32	900.2	484.7	8.557	8.157	15.442
DPM80	8 x 8	689.0	485.8	7.378	6.956	0.648
	8 x 16	900.2	484.7	8.928	8.456	–
	8 x 24	689.0	485.8	9.468	8.996	–
	8 x 32	900.2	484.7	9.808	9.336	–
	16 x 16	689.0	485.8	9.878	9.396	5.260
	16 x 24	900.2	484.7	11.058	10.586	–
	16 x 32	689.0	485.8	11.058	10.576	–
	24 x 24	900.2	484.7	11.738	11.306	5.920
	24 x 32	689.0	485.8	12.138	11.606	–
	32 x 32	900.2	484.7	13.238	12.806	10.147

Features

- Functional model, test vector, schematic, and layout generators
- Timing model with auto-characterization
- Simple ripple and sophisticated carry-bypass scheme
- *n*-bit (4 to 128) Incrementer
- Buffered carry path
- Three drive strengths on output

General Description

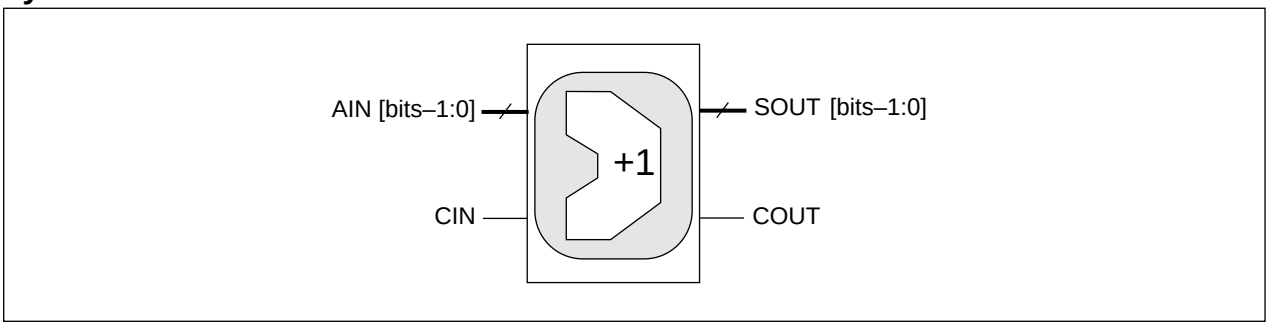
The Incrementer builds an *n*-bit wide Incrementer schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells. The Incrementer supports signed increments.

Design Description

The logic circuit produced by the generator performs increment functions. An *n*-bit wide operand (AIN), a 1-bit wide input carry signal (CIN), and an *n*-bit wide output bus (SOUT) and 1-bit output carry signal (COUT) serve as the I/O signals to the module.

The Incrementer can be built with two different carry chains allowing speed/area trade-offs. The ripple carry chain is high in density and low in performance. The carry-bypass chain has a unique grouping of bits which creates a high performance design. This scheme is preferable for the increment of high order bits to attain high performance.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
nopass	0: group bypass; 1: ripple adder	0/1
drv	Drive strength	1/2/4

Incrementer

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input
CIN		Carry-in increment signal
SOUT [bits–1:0]	O	Output data bus – Result of incrementer
COUT		Carry-out signal

Function Table

Type	Function
Incrementer	AIN + CIN

Truth Table

Inputs		Output
AIN	**CIN**	**SOUT**
0	0	0
1	0	1
0	1	1
1	1	0

Pin Capacitance

Pin Name	Bit	Value (pF)	
		DP80	DPM80
AIN	8/16/24/32	0.143	0.139
CIN	8/16/24/32	0.109	0.106

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: nopass = 0, drv = 1						
Library	**Bit**	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
		Width	**Height**	**T_{PLH}**	**T_{PHL}**	
DP80	8	213.2	88.7	2.087	1.479	0.085
	16	424.4	94.9	2.155	1.861	0.154
	24	635.6	92.3	2.426	2.208	0.222
	32	846.8	92.5	2.514	1.897	0.291
DPM80	8	213.2	88.7	3.180	2.884	0.053
	16	424.4	94.9	3.500	3.194	0.097
	24	635.6	92.3	3.774	3.502	0.140
	32	846.8	92.5	4.090	3.774	0.185

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Simple ripple and sophisticated carry-bypass scheme
- *n*-bit (4 to 128) Incrementer/Decrementer
- Buffered carry path
- Three Multiple drive strengths options for output

General Description

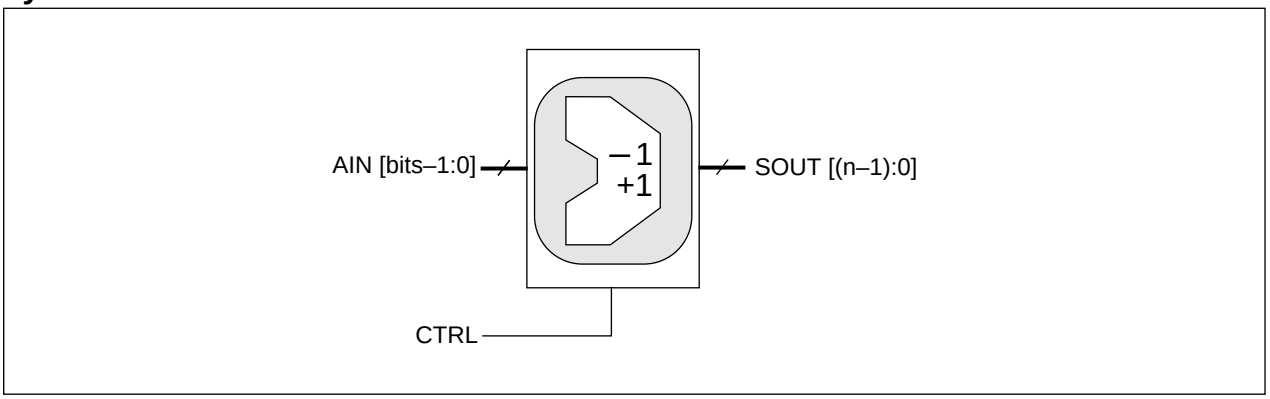
The Incrementer/Decrementer builds an *n*-bit wide Incrementer/Decrementer schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells. The Incrementer/Decrementer supports signed decrements.

Design Description

The logic circuit produced by the generator performs increment or decrement function by control signal. An *n*-bit wide operand (AIN), a 1-bit wide input control signal (CTRL), and an *n*-bit wide output bus (SOUT) serve as the I/O signals to the module.

The Incrementer/Decrementer is built with a unique carry-bypass chain. The carry-bypass chain has a unique grouping of bits which modulates the group sizes to minimize carry propagation delay, which creates a high performance design. This scheme is optimized for the incrementer/decrementer of large data words to attain high speed.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
nopass	0: group bypass; 1: ripple adder	0/1
drv	Drive strength	1/2/4

Incrementer/Decrementer

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input
CTRL	I	Decrement signal which is active low, Increment signal which is active high
SOUT [bits–1:0]	O	Data output – Result of Incrementer or Decrementer

Function Table

Type	Function
Decrementer	AIN–1
Incrementer	AIN+1

Truth Table

Inputs		Output
AIN	**CTRL**	**SOUT**
0	1	1
1	1	0
0	0	1
1	0	0

Pin Capacitance

Pin Name	Value (pF)	
	DP80	**DPM80**
AIN	0.053	0.052
CTRL	0.821	0.800

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: nopass = 0, drv = 1						
Library	**Bit**	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
		Width	**Height**	**T_{PLH}**	**T_{PHL}**	
DP80	8	213.2	100.6	2.784	2.500	0.05
	16	424.4	107.5	3.169	2.875	0.08
	24	635.6	106.1	3.381	3.153	0.08
	32	846.8	106.3	3.569	3.275	0.11
DPM80	8	213.2	100.6	4.184	3.888	0.03
	16	424.4	107.5	4.621	4.305	0.05
	24	635.6	106.1	4.895	4.623	0.06
	32	846.8	106.3	5.211	4.895	0.08

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- *n*-bit (4 to 128) Normalizer
- High performance
- Outputs shift amount
- Three drive strength options for output

General Description

The Normalizer detects the number of leading zero's in the input data word, and outputs the data word so the left-most "1" appears in the MSB position, along with the shifted amount. If no "1" is detected in the data input, the ALL0 flag is set. The Normalizer is a high performance datapath function which can build normalizers between 4-128 bits in 1 bit increments.

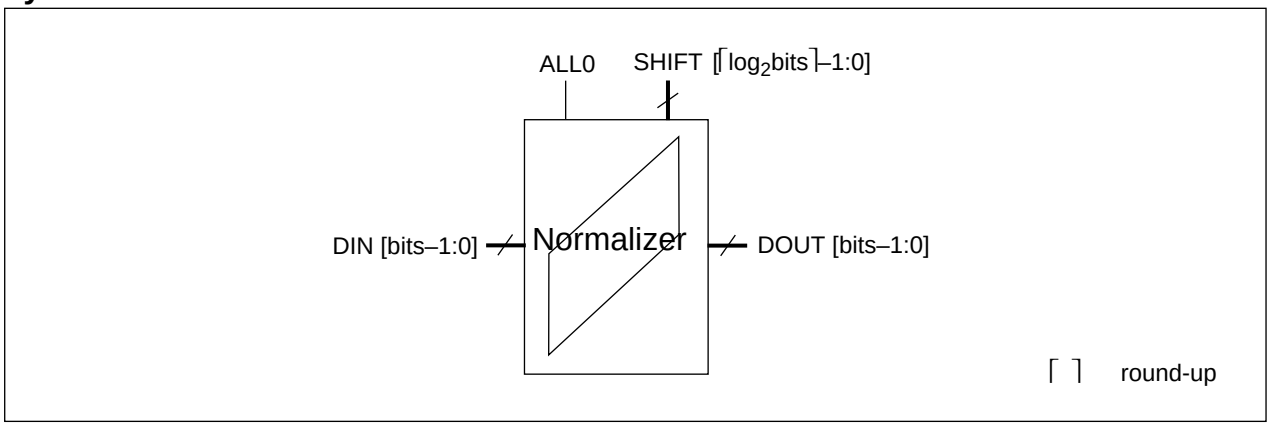
Design Description

The Normalizer is built from 2 sub-functions, an Priority Encoder, and a Left Shifter. The Priority Encoder detects the left-most "1" from the data input word and outputs the amount to be shifted. Then the amount is passed into the Left Shifter block and the leading "1" is shifted to the MSB position with the LSB filled with "0".

The priority encoder uses a parallel technique to calculate the high and low output address bits to speed up the leading "1" detection. A binary tree is used to determine the address of the high order bits, while a multiplexer tree is used to propagate the values of the low order bits.

The Left Shifter is constructed as a series of cascaded 2-to-1 and 4-to-1 multiplexers. In its largest configuration (128 bits), three rows of 4-to-1 and one row of 2-to-1 MUXs are used.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
drv	Drive strength	1/2/4

Normalizer

Pin Description

Pin Name	I/O	Description
DIN [bits–1:0]	I	Data input
ALL0	O	Output flag that zeros all bits on the data input bus
SHIFT [$\lceil \log_2 bits \rceil$–1:0]		Data output – Encoded address of the leading 1 bit
DOUT [bits–1:0]		Normalized data output

⌈ ⌉ round-up

Pin Capacitance

Pin Name	Bit	Value (pF)	
		DP80	DPM80
DIN	8/24/32	0.184	0.172
	16	0.322	0.296

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: drv = 1						
Library	Bit	Area (μm x μm)		Delay (ns)		Current (mA)
		Width	Height	T_{PLH}	T_{PHL}	
DP80	8	266.5	177.5	1.759	1.660	0.114
	16	477.7	205.0	2.080	1.980	0.226
	24	688.9	262.6	2.250	2.300	0.384
	32	900.1	297.6	2.400	2.300	0.507
DPM80	8	266.5	177.5	2.586	2.504	0.068
	16	477.7	205.0	3.036	2.964	0.136
	24	688.9	262.6	3.246	3.414	0.230
	32	900.1	297.6	3.486	3.414	0.307

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Fast datapath one flag
- *n*-bit (4 to 128) one Detector
- Three drive strength options for output

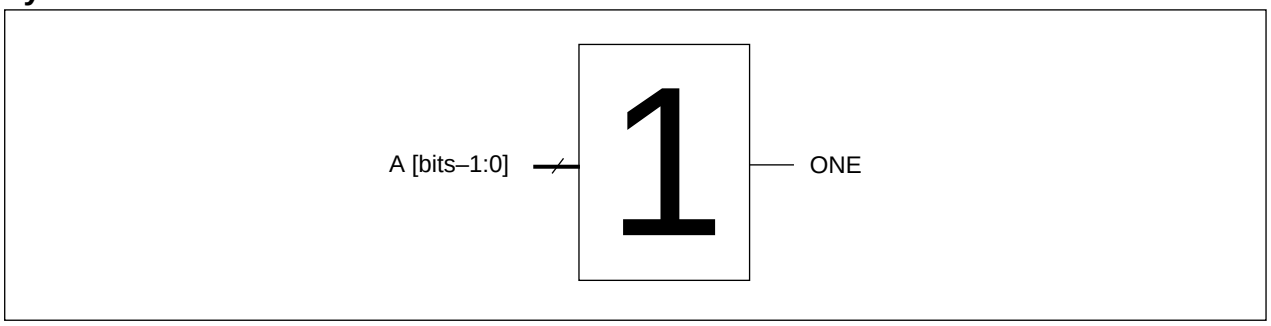
General Description

The One Detector builds an *n*-bit wide schematic that is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells. The One Detector detects “0” in the inputs and if there is no “0”, it sets ONE to “1.”

Design Description

The One Detector performs deciding whether the input is one or not. An *n*-bit wide operand (AIN) and a 1-bit wide one flag (ONE) serve as the I/O signals to the module. The One Detector can be built with simple AND gates.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
drv	Drive strength	1/2/4

One Detector

Pin Description

Pin Name	I/O	Description
A [bits–1:0]	I	Data input
ONE	O	It specifies whether all the bits in the input A are “0” or “1”.

Truth Table

A	ONE
All 1	1
Any 0	0

Pin Capacitance

Pin Name	Value (pF)	
	DP80	DPM80
A	0.036	0.035

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: drv = 1						
Library	Bit	Area (μm x μm)		Delay (ns)		Current (mA)
		Width	Height	T_{PLH}	T_{PHL}	
DP80	8	213.3	61.3	1.672	1.037	0.030
	16	424.5	64.6	1.950	1.186	0.032
	24	662.0	68.0	2.210	1.355	0.068
	32	846.9	71.4	2.230	1.335	0.065
DPM80	8	213.3	61.3	2.477	1.580	0.030
	16	424.5	64.6	2.907	1.786	0.032
	24	662.0	68.0	3.287	1.986	0.068
	32	846.9	71.4	3.327	1.986	0.065

Features

- Functional model, test-vector, schematic and layout generators
- Timing model with auto-characterization
- *n*-bit (4 to 128) Parity
- High speed and density
- Three drive strength options for output

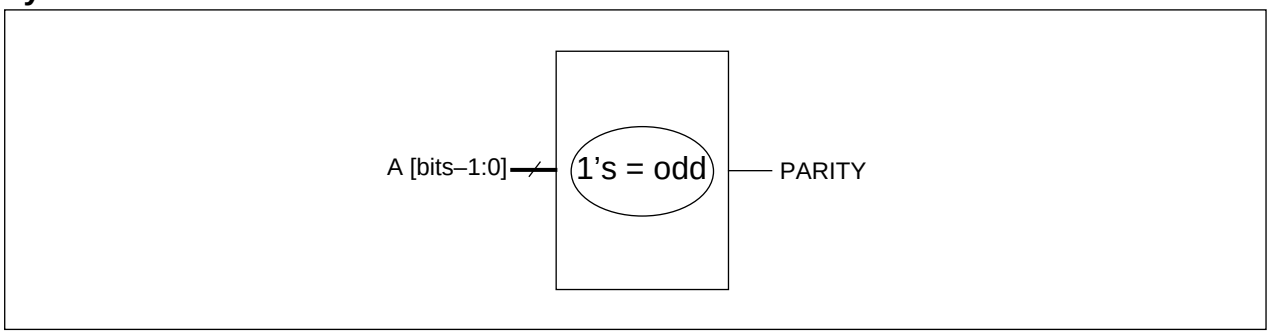
General Description

The Parity builds an n-bit wide Parity schematic. The Parity calculates the parity value of the specified input bits by performing the XOR function across all inputs. The design is optimized for multiple targeted technologies.

Design Description

The Parity uses a binary tree architecture for high speed calculations of the parity value. To minimize the area of the implementation, the layout cells used in the parity are placed in a single datapath row. It enables different drive strengths to be specified for the output.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of Parity generator to be created	Any string
bits	Number of bits in the input data bus	4 to 128
drv	Drive strength	1/2/4

Parity

Pin Description

Pin Name	I/O	Description
A [bits–1:0]	I	Data input bus for Parity generation
PARITY	O	Output parity value for inputs (odd parity)

Pin Capacitance

Pin Name	Value (pF)	
	DP80	DPM80
A	0.033	0.034

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: drv = 1						
Library	Bit	Area (μm x μm)		Delay (ns)		Current (mA)
		Width	Height	T_{PLH}	T_{PHL}	
DP80	8	188.3	58.5	1.444	1.180	0.030
	16	399.5	64.2	1.803	1.459	0.032
	24	635.6	67.4	2.000	1.385	0.068
	32	821.9	71.1	2.000	1.736	0.065
DPM80	8	188.3	58.5	2.203	1.963	0.018
	16	399.5	64.2	2.655	2.413	0.015
	24	635.6	67.4	3.105	2.789	0.037
	32	821.9	71.1	3.105	2.863	0.032

Features

- Functional Model, test-vectors, schematics and layout generators
- Timing model with auto characterization
- High speed and density
- *n*-bit (4 to 128) Priority Encoder

General Description

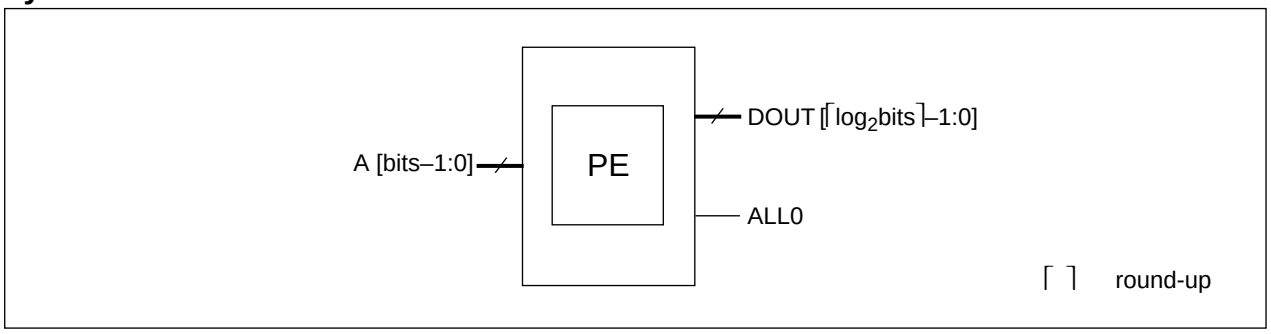
The Priority Encoder builds an n-bit wide schematic that is used to drive the datapath placement and routing tool in combination with technology-specific layout leafcells. The Priority Encoder detects the leading “1” on data bus.

Design Description

The priority encoder uses a parallel processing technique to calculate the high and low output address bits to speed up the leading “1” detection. A binary tree is used to determine the address of the high order bits, while a multiplexer tree is used to propagate the values of the low order bits.

This design supports a wide range of input data width with a narrow delay time spectrum. It can create either a leftmost one or a rightmost one Priority Encoder.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of Priority Encoder to be created	Any string
bits	Number of bits in the input data bus	4 to 128
type	0: detect from MSB; 1: detect from LSB	0/1
drv	Drive strength	1/2/4

Priority Encoder

Pin Description

Pin Name	I/O	Description
A [bits–1:0]	I	Data input bus for the leading one detection
DOUT [$\lceil \log_2 bits \rceil$–1:0]	O	Data output – Encoded address of the leading 1 bit
ALL0		Output flag that zeros all bits on the data input bus

⌈ ⌉ round-up

Pin Capacitance

Pin Name	Value (pF)	
	DP80	DPM80
A	0.064	0.062

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: type = 0, drv = 1						
Library	Bit	Area (μm x μm)		Delay (ns)		Current (mA)
		Width	Height	T_{PLH}	T_{PHL}	
DP80	8	213.2	91.7	1.612	1.940	0.030
	16	424.4	99.6	1.934	2.260	0.057
	24	635.6	109.8	2.104	2.590	0.068
	32	846.8	118.4	2.264	2.590	0.207
DPM80	8	213.2	91.7	2.648	2.664	0.018
	16	424.4	99.6	3.108	3.124	0.030
	24	635.6	109.8	3.308	3.574	0.037
	32	846.8	118.4	3.558	3,574	0.124

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Configurable read/write ports for macro block
- Address decoders on either side of the datapath block
- *n*-bit (4 to 128) Register File

General Description

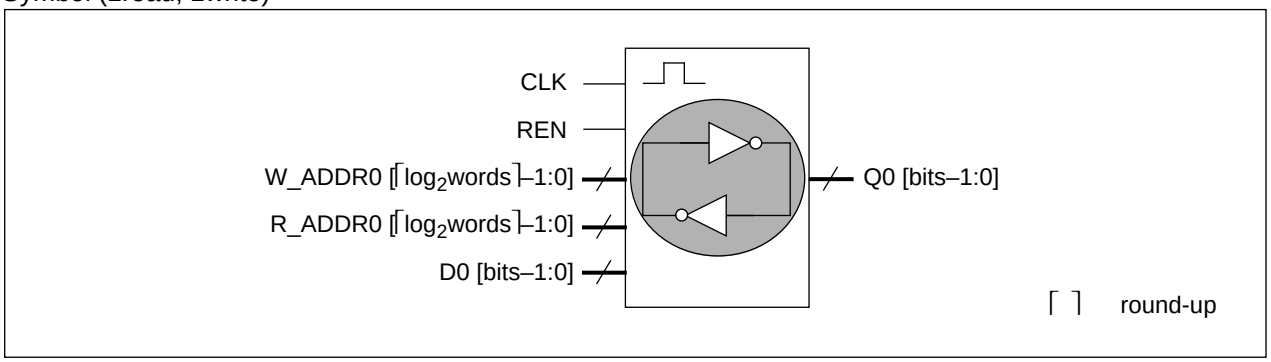
The Register File is optimized for multiple-targeted technologies. The Register File can be built with one to four read ports and with one to two write ports. The maximum number of words is 128 and there can be up to 128 bits per word.

Design Description

The Register File can be used as a stand-alone module or as part of a datapath block. To allow some flexibility, it allows you to place the control block to the right or left side of the register block.

All read and write ports are independent. The read ports always output data; data will be changed after the read address has been changed. The write ports are enabled by REN and data is latched into the memory location on the falling edge of the clock.

Symbol (1read, 1write)



Parameter Description

Parameter Name	Description	Range
words	Number of words in the Register File	8 to 128
bits	Number of bits per word	8 to 128
writes	Number of write ports	1/2
reads	Number of read ports	1/2/3/4
control	Where to place control with respect to memory	LEFT/RIGHT

Pin Description

Pin Name	I/O	Description
CLK (When # (write port) = 1.) CLK [1:0] (When # (write port) = 2.)	I	Clock signal (active-high) for each write port. When the clock is high, data pass into the decoded memory location and is latched on the falling clock edge.
REN (When # (write port) = 1.) REN [1:0] (When # (write port) = 2.)		Register enable signal (active-low) for each write port. A high state prevents a write operation to the write port; a low state allows a write operation.
W_ADDR0 [$\lceil \log_2 words \rceil$–1:0]		Data input – Write address bus There is one address bus for each write port and there can be from 1 to 2 write ports.
R_ADDR0 [$\lceil \log_2 words \rceil$–1:0]		Data input – Read address bus There is one address bus for each read port and there can be from 1 to 4 read ports.
D0 <0>...D0 [bits–1:0]		Input – Word values written into the write port location during the write operation. There is one input bus for each write port.
Q0 <0>...Q0 [bits–1:0]	O	Output data previously written into the register file Data are present at all times and its value depends on the read address. There is one output bus for each read port.

⌈ ⌉ round-up

Pin Capacitance

Library	Word	Pin Name					
		CLK	D0	REN	R_ADDR0	R_ADDR1	W_ADDR0
DP80	8	0.176	0.033	0.064	0.032	0.032	0.033
	16	0.255	0.033	0.064	0.032	0.032	0.033
	24	0.334	0.033	0.064	0.032	0.032	0.033
	32	0.390	0.033	0.064	0.032	0.032	0.033
DPM80	8	0.173	0.032	0.062	0.031	0.031	0.032
	16	0.250	0.032	0.062	0.031	0.031	0.032
	24	0.327	0.032	0.062	0.031	0.031	0.032
	32	0.381	0.032	0.062	0.031	0.031	0.032

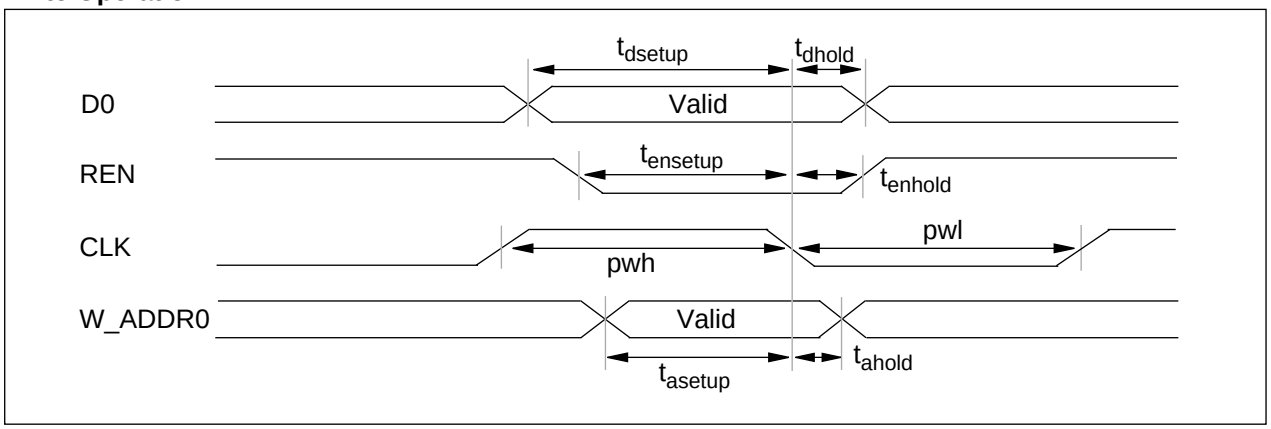
Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

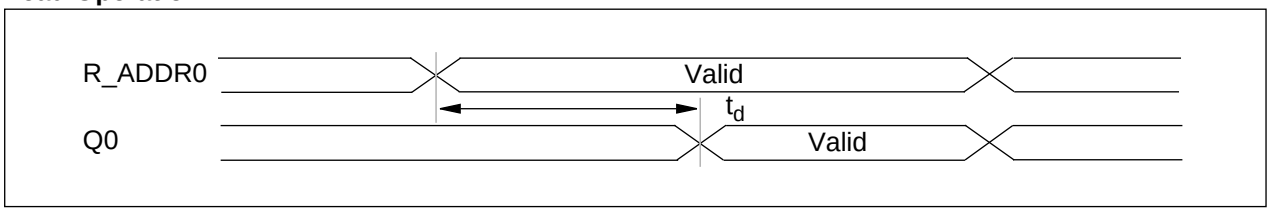
Parameters: read = 1, write = 2, control = LEFT					
Library	**Words x Bit**	**Area (μm x μm)**		**Delay (ns)**	
		Width	**Height**	**T_{PLH}**	**T_{PHL}**
DP80	8 x 8	237.6	343.2	2.490	2.070
	8 x 16	448.8	343.2	2.570	2.160
	8 x 24	660.0	343.2	2.650	2.260
	8 x 32	871.2	343.2	2.730	2.360
	16 x 8	237.6	549.9	2.900	2.460
	16 x 16	448.8	549.9	2.980	2.560
	16 x 24	660.0	549.9	3.060	2.650
	16 x 32	871.2	549.9	3.140	2.750
	24 x 8	237.6	740.5	3.051	2.601
	24 x 16	448.8	740.5	3.131	2.701
	24 x 24	660.0	740.5	3.211	2.801
	24 x 32	871.2	740.5	3.291	2.891
	32 x 8	237.6	924.1	3.361	2.901
	32 x 16	448.8	924.1	3.441	3.001
	32 x 24	660.0	924.1	3.521	3.091
	32 x 32	871.2	924.1	3.601	3.191
DPM80	8 x 8	237.6	343.2	3.735	3.201
	8 x 16	448.8	343.2	3.915	3.351
	8 x 24	660.0	343.2	4.085	3.511
	8 x 32	871.2	343.2	4.255	3.661
	16 x 8	237.6	549.9	4.436	3.882
	16 x 16	448.8	549.9	4.596	4.042
	16 x 24	660.0	549.9	4.756	4.192
	16 x 32	871.2	549.9	4.916	4.342
	24 x 8	237.6	740.5	4.896	4.282
	24 x 16	448.8	740.5	5.056	4.432
	24 x 24	660.0	740.5	5.226	4.592
	24 x 32	871.2	740.5	5.386	4.742
	32 x 8	237.6	924.1	5.496	4.812
	32 x 16	448.8	924.1	5.656	4.962
	32 x 24	660.0	924.1	5.816	5.122
	32 x 32	871.2	924.1	5.976	5.272

Timing Diagram

Write Operation



Read Operation



NOTE: Not allowed to read and write in the same location at the same time.

Timing Parameters

Symbol	Description	Input	Output
t_{dsetup}	Input data setup time	D0	–
t_{dhold}	Input data hold time	D0	–
$t_{ensetup}$	REN setup time	REN	–
t_{enhold}	REN hold time	REN	–
t_{asetup}	W_ADDR setup time	W_ADDR	–
t_{ahold}	W_ADDR hold time	W_ADDR	–
pwh	CLK pulse width high	CLK	–
pwl	CLK pulse width low	CLK	–
t_d	Read access time	R_ADDR	Q0

Timing Requirements

Parameters: read = 1, write = 2, control = LEFT			
Words x Bit	**Timing Field**	**Value (ns)**	
		DP80	**DPM80**
8 x 8	min_pulse_width_high CLK	0.576	0.686
	min_pulse_width_low CLK	0.333	0.801
	hold_rising D0 REN	0.100	0.237
	hold_falling D0 CLK	0.136	0.273
	hold_rising REN CLK	–0.472	–0.741
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.339	0.345
	setup_falling D0 CLK	0.364	0.347
	setup_rising REN CLK	0.970	1.430
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100
8 x 16	min_pulse_width_high CLK	0.698	0.874
	min_pulse_width_low CLK	0.469	1.010
	hold_rising D0 REN	0.146	0.325
	hold_falling D0 CLK	0.182	0.374
	hold_rising REN CLK	–0.488	–0.788
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.293	0.257
	setup_falling D0 CLK	0.318	0.246
	setup_rising REN CLK	0.987	1.450
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100
8 x 24	min_pulse_width_high CLK	0.820	1.060
	min_pulse_width_low CLK	0.605	1.210
	hold_rising D0 REN	0.192	0.414
	hold_falling D0 CLK	0.228	0.476
	hold_rising REN CLK	–0.503	–0.836
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.247	0.169
	setup_falling D0 CLK	0.272	0.144
	setup_rising REN CLK	1.000	1.470
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100

Timing Requirements (Cont.)

Parameters: read = 1, write = 2, control = LEFT			
Words x Bit	**Timing Field**	**Value (ns)**	
		DP80	**DPM80**
8 x 32	min_pulse_width_high CLK	0.941	1.250
	min_pulse_width_low CLK	0.741	1.420
	hold_rising D0 REN	0.238	0.502
	hold_falling D0 CLK	0.274	0.577
	hold_rising REN CLK	–0.519	–0.883
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.201	0.080
	setup_falling D0 CLK	0.226	0.043
	setup_rising REN CLK	1.020	1.490
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100
16 x 8	min_pulse_width_high CLK	0.576	0.686
	min_pulse_width_low CLK	0.333	0.801
	hold_rising D0 REN	0.100	0.237
	hold_falling D0 CLK	0.136	0.273
	hold_rising REN CLK	–0.726	–1.170
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.339	0.345
	setup_falling D0 CLK	0.364	0.347
	setup_rising REN CLK	1.360	1.940
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100
16 x 16	min_pulse_width_high CLK	0.698	0.874
	min_pulse_width_low CLK	0.469	1.010
	hold_rising D0 REN	0.146	0.325
	hold_falling D0 CLK	0.182	0.374
	hold_rising REN CLK	–0.742	–1.220
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.293	0.257
	setup_falling D0 CLK	0.318	0.246
	setup_rising REN CLK	1.380	1.960
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100

Timing Requirements (Cont.)

Parameters: read = 1, write = 2, control = LEFT			
Words x Bit	**Timing Field**	**Value (ns)**	
		DP80	**DPM80**
16 x 24	min_pulse_width_high CLK	0.820	1.060
	min_pulse_width_low CLK	0.605	1.210
	hold_rising D0 REN	0.192	0.414
	hold_falling D0 CLK	0.228	0.476
	hold_rising REN CLK	–0.757	–1.270
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.247	0.169
	setup_falling D0 CLK	0.272	0.144
	setup_rising REN CLK	1.400	1.980
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100
16 x 32	min_pulse_width_high CLK	0.941	1.250
	min_pulse_width_low CLK	0.741	1.420
	hold_rising D0 REN	0.238	0.502
	hold_falling D0 CLK	0.274	0.577
	hold_rising REN CLK	–0.773	–1.310
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.201	0.080
	setup_falling D0 CLK	0.226	0.043
	setup_rising REN CLK	1.410	2.000
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100
24 x 8	min_pulse_width_high CLK	0.576	0.686
	min_pulse_width_low CLK	0.333	0.801
	hold_rising D0 REN	0.100	0.237
	hold_falling D0 CLK	0.136	0.273
	hold_rising REN CLK	–0.953	–1.600
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.339	0.345
	setup_falling D0 CLK	0.364	0.347
	setup_rising REN CLK	1.760	2.450
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100

Timing Requirements (Cont.)

Parameters: read = 1, write = 2, control = LEFT			
Words x Bit	**Timing Field**	**Value (ns)**	
		DP80	**DPM80**
24 x 16	min_pulse_width_high CLK	0.698	0.874
	min_pulse_width_low CLK	0.469	1.010
	hold_rising D0 REN	0.146	0.325
	hold_falling D0 CLK	0.182	0.374
	hold_rising REN CLK	–0.961	–1.650
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.293	0.257
	setup_falling D0 CLK	0.318	0.246
	setup_rising REN CLK	1.770	2.470
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100
24 x 24	min_pulse_width_high CLK	0.820	1.060
	min_pulse_width_low CLK	0.605	1.210
	hold_rising D0 REN	0.192	0.414
	hold_falling D0 CLK	0.228	0.476
	hold_rising REN CLK	–0.969	–1.700
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.247	0.169
	setup_falling D0 CLK	0.272	0.144
	setup_rising REN CLK	1.790	2.500
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100
24 x 32	min_pulse_width_high CLK	0.941	1.250
	min_pulse_width_low CLK	0.741	1.420
	hold_rising D0 REN	0.238	0.502
	hold_falling D0 CLK	0.274	0.577
	hold_rising REN CLK	–0.977	–1.740
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.201	0.080
	setup_falling D0 CLK	0.226	0.043
	setup_rising REN CLK	1.810	2.550
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100

Timing Requirements (Cont.)

Parameters: read = 1, write = 2, control = LEFT			
Words x Bit	**Timing Field**	**Value (ns)**	
		DP80	**DPM80**
32 x 8	min_pulse_width_high CLK	0.576	0.686
	min_pulse_width_low CLK	0.333	0.801
	hold_rising D0 REN	0.100	0.237
	hold_falling D0 CLK	0.136	0.273
	hold_rising REN CLK	–1.130	–2.030
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.339	0.345
	setup_falling D0 CLK	0.364	0.347
	setup_rising REN CLK	2.150	3.010
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100
32 x 16	min_pulse_width_high CLK	0.698	0.874
	min_pulse_width_low CLK	0.469	1.010
	hold_rising D0 REN	0.146	0.325
	hold_falling D0 CLK	0.182	0.374
	hold_rising REN CLK	–1.140	–2.080
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.293	0.257
	setup_falling D0 CLK	0.318	0.246
	setup_rising REN CLK	2.170	3.060
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100
32 x 24	min_pulse_width_high CLK	0.820	1.060
	min_pulse_width_low CLK	0.605	1.210
	hold_rising D0 REN	0.192	0.414
	hold_falling D0 CLK	0.228	0.476
	hold_rising REN CLK	–1.150	–2.130
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.247	0.169
	setup_falling D0 CLK	0.272	0.144
	setup_rising REN CLK	2.180	3.110
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100

Timing Requirements (Cont.)

Parameters: read = 1, write = 2, control = LEFT			
Words x Bit	**Timing Field**	**Value (ns)**	
		DP80	**DPM80**
32 x 32	min_pulse_width_high CLK	0.941	1.250
	min_pulse_width_low CLK	0.741	1.420
	hold_rising D0 REN	0.238	0.502
	hold_falling D0 CLK	0.274	0.577
	hold_rising REN CLK	–1.150	–2.180
	hold_falling REN CLK	–0.200	–0.200
	hold_falling W_ADDR0 CLK	–0.200	–0.200
	setup_rising D0 REN	0.201	0.080
	setup_falling D0 CLK	0.226	0.043
	setup_rising REN CLK	2.200	3.160
	setup_falling REN CLK	0.800	1.100
	setup_falling W_ADDR0 CLK	0.800	1.100

Features

- Functional model, test vector, schematic, and layout generators
- Timing model with auto-characterization
- High performance saturation scheme
- Two's complement overflow flag
- *n*-bit (4 to 128) Saturating Adder
- Three drive strength options for output

General Description

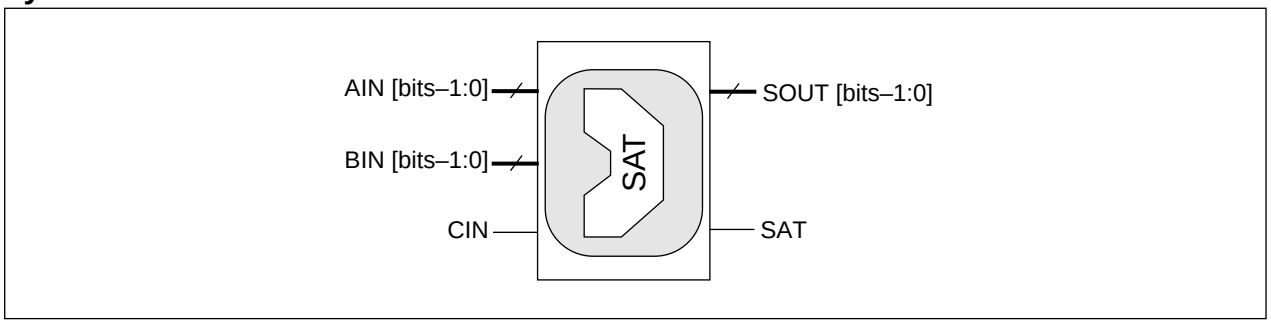
The Saturating Adder builds an *n*-bit wide adder schematic that is used to drive the datapath place and route tool in combination with technology-specific layout leaf cells. The saturate flag saturates the output to the largest positive number on an overflow or to the smallest negative number on an underflow.

Design Description

The Saturating Adder performs addition functions. An *n*-bit wide operand (AIN), an *n*-bit wide operand (BIN), a 1-bit wide input carry signal (CIN), and an *n*-bit wide output bus (SOUT) and a 1-bit saturation flag (SAT) serve as the I/O signals to the module.

The Saturating Adder can be built with two different carry chains allowing speed/area trade-offs. The ripple carry chain is high in density, with lower performance. The carry-bypass chain has a unique grouping of bits which creates a high performance design. This scheme is preferable for the addition of large data words to attain high speed.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
nopass	0: group bypass; 1: ripple adder	0/1
drv	Drive strength	1/2/4

Saturating Adder

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input
BIN [bits–1:0]		Data input
CIN		Carry-in
SAT	O	Saturate flag
SOUT		Output result of addition

Function Table

Type	Function

SOUT	AIN + BIN + CIN
	If (AIN and BIN have positive values, and SAT output becomes 1),
	then SOUT [bits–2:0] = 1, SOUT [bits–1] = 0.
	If (AIN and BIN have negative values, and SAT output becomes 1),
	then SOUT [bits–2:0] = 0, SOUT [bits–1] = 1.

SAT	If the result of two positive numbers addition is negative value or the result of two negative numbers addition is positive, then SAT is “1.”

Truth Table

Inputs			Outputs	
AIN	**BIN**	**CIN**	**SOUT**	**SAT**
0	0	0	0	0
0	0	0	1	1
0	1	0	0	0
1	1	0	1	0
0	0	1	1	0
1	0	1	0	0
0	1	1	0	1
1	1	1	1	0

Pin Capacitance

Pin Name	Value (pF)	
	DP80	**DPM80**
AIN	0.049	0.048
BIN	0.039	0.039
CIN	0.095	0.092

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: nopass = 0, drv = 1						
Library	**Bit**	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
		Width	**Height**	**T_{PLH}**	**T_{PHL}**	
DP80	8	266.4	134.9	3.685	3.395	0.313
	16	477.6	135.1	4.265	3.965	0.599
	24	688.8	138.2	4.595	4.285	0.872
	32	900.0	137.4	5.015	4.685	1.148
DPM80	8	266.4	134.9	5.944	5.406	0.203
	16	477.6	135.1	6.804	6.266	0.388
	24	688.8	138.2	7.484	6.936	0.563
	32	900.0	137.4	8.034	7.496	0.737

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Fast datapath zero flag
- *n*-bit (4 to 128) zero Detector
- Three drive strength options for output

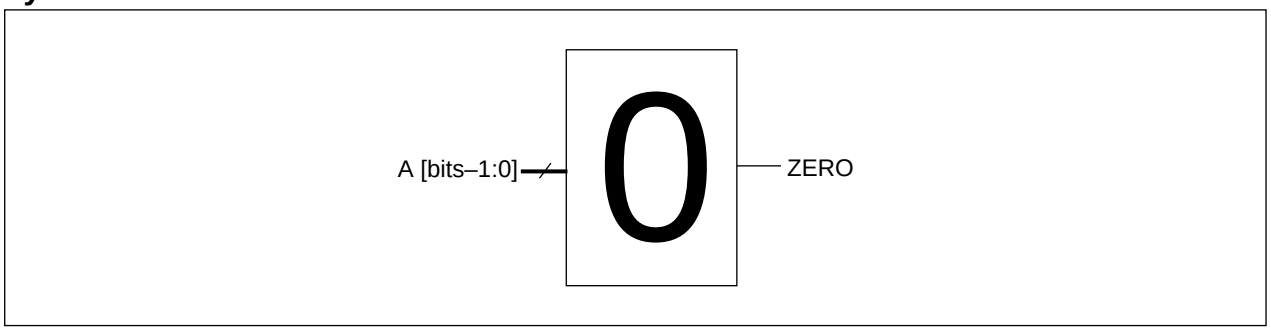
General Description

The Zero Detector builds an *n*-bit wide schematic that is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells. The Zero Detector detects “1” in the inputs and if there is no “1”, it sets ZERO to “1.”

Design Description

The Zero Detector performs deciding whether the input is zero or not. An *n*-bit wide operand (AIN) and a 1-bit wide zero flag (ZERO) serve as the I/O signals to the module. The Zero Detector can be built with simple OR gates.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
drv	Drive strength	1/2/4

Zero Detector

Pin Description

Pin Name	I/O	Description
A [bits–1:0]	I	Data input
ZERO	O	It specifies whether all the bits in the input A are 0 or 1.

Truth Table

A	ZERO
All 0	1
Any 1	0

Pin Capacitance

Pin Name	Value (pF)	
	DP80	DPM80
A	0.023	0.023

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: drv = 1						
Library	Bit	Area (μm x μm)		Delay (ns)		Current (mA)
		Width	Height	T_{PLH}	T_{PHL}	
DP80	8	213.3	59.6	1.468	1.054	0.030
	16	424.5	61.6	1.633	1.242	0.032
	24	662.0	65.1	1.797	1.416	0.068
	32	846.9	68.4	1.797	1.430	0.065
DPM80	8	213.3	59.6	2.214	1.522	0.030
	16	424.5	61.6	2.524	1.770	0.032
	24	662.0	65.1	2.814	2.010	0.068
	32	846.9	68.4	2.814	2.030	0.065

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for types 21 and 22
- Two drive strength options for output

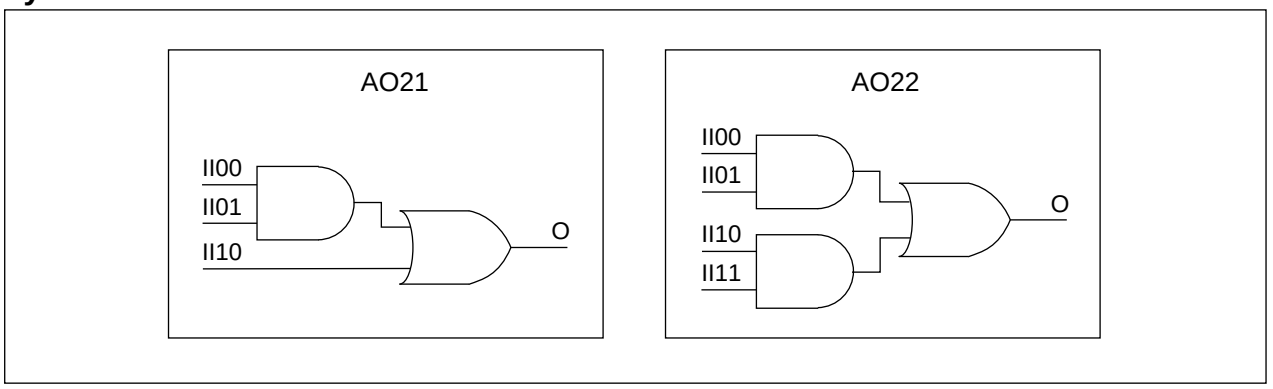
General Description

The high performance datapath AND-OR design can be optimized for multiple-targeted technologies. The generator can build AND-OR gates ranging from 4-bits to 128-bits for two different configurations (21 and 22) and two different drive strengths.

Design Description

The AND-OR design has schematic and layout generators that can build a variety of AND-OR gates. You have an option to build the different kinds of structure configurations by setting the “type” parameter to 21/22 depending on your application.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Configuration type	21/22
drv	Drive strength	1/2

Pin Description

AO22		
Pin Name	**I/O**	**Description**
II00 [bits–1:0]	I	Data input
II01 [bits–1:0]		Data input
II10 [bits–1:0]		Data input
II11 [bits–1:0]		Data input
O	O	Data output

Truth Table

AO21			
Inputs			**Output**
II00	**II01**	**II10**	**O**
x	x	1	1
x	0	0	0
0	x	0	0
1	1	0	1

AO22				
Inputs				**Output**
II00	**II01**	**II10**	**II11**	**O**
x	0	x	0	0
0	x	x	0	0
x	0	0	x	0
0	x	0	x	0
1	1	x	x	1
x	x	1	1	1

Pin Capacitance

AO21		
Pin Name	**Value (pF)**	
	DP80	**DPM80**
II10	0.023	0.023
II01	0.024	0.023
II00	0.024	0.023

AO22		
Pin Name	**Value (pF)**	
	DP80	**DPM80**
II11	0.024	0.023
II10	0.023	0.022
II01	0.024	0.024
II00	0.024	0.023

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	**Bit**	**Area (μm x μm)**		**Delay (ns)**			
		Width	**Height**	**DP80**		**DPM80**	
				T_{PLH}	**T_{PHL}**	**T_{PLH}**	**T_{PHL}**
AO21	8/16/24/32	26.4 x bits	54.7	0.923	0.816	1.367	1.285
AO22	8/16/24/32	26.4 x bits	54.7	1.043	0.792	1.489	1.277

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for types 21 and 22
- Two drive strength options for output

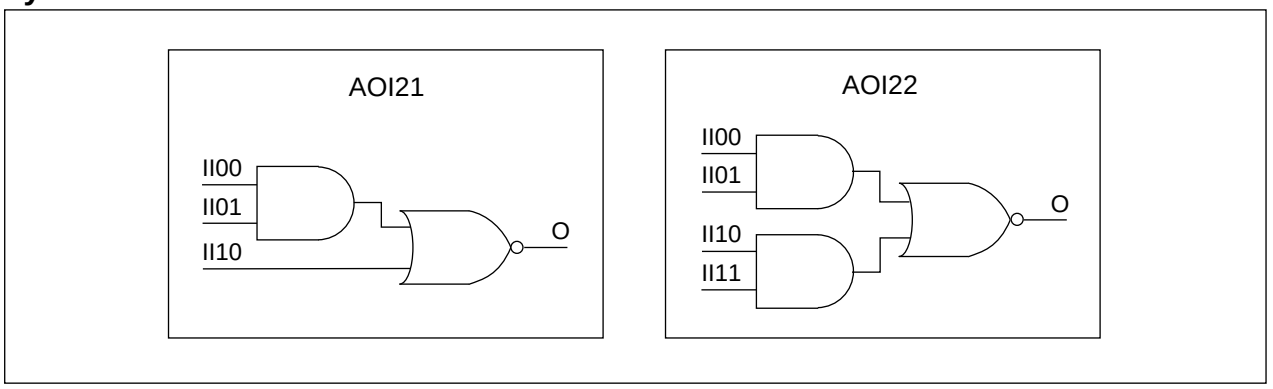
General Description

The high performance datapath AND-OR-INVERT design can be optimized for multiple-targeted technologies. The generator can build AND-OR-INVERT gates ranging from 4-bits to 128-bits for two different configurations (21 and 22) and two different drive strengths.

Design Description

The AND-OR-INVERT design has schematic and layout generators that can build a variety of AND-OR-INVERT gates. You have an option to build the different kinds of AND-OR-INVERT structure configurations by setting the “type” parameter to 21/22 depending on your application.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Configuration type	21/22
drv	Drive strength	1/2

Pin Description

AOI22		
Pin Name	**I/O**	**Description**
II00 [bits–1:0]	I	Data input
II01 [bits–1:0]		Data input
II10 [bits–1:0]		Data input
II11 [bits–1:0]		Data input
O	O	Data output

Truth Table

AOI21			
Inputs			**Output**
II00	**II01**	**II10**	**O**
x	x	1	0
x	0	0	1
0	x	0	1
1	1	0	0

AOI22				
Inputs				**Output**
II00	**II01**	**II10**	**II11**	**O**
x	0	x	0	1
0	x	x	0	1
x	0	0	x	1
0	x	0	x	1
1	1	x	x	0
x	x	1	1	0

Pin Capacitance

AOI21		
Pin Name	**Value (pF)**	
	DP80	**DPM80**
II10	0.023	0.023
II01	0.024	0.024
II00	0.024	0.024

AOI22		
Pin Name	**Value (pF)**	
	DP80	**DPM80**
II11	0.024	0.024
II10	0.023	0.022
II01	0.025	0.025
II00	0.024	0.024

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	**Bit**	**Area (μm x μm)**		**Delay (ns)**			
		Width	**Height**	**DP80**		**DPM80**	
				T_{PLH}	**T_{PHL}**	**T_{PLH}**	**T_{PHL}**
AOI21	8/16/24/32	26.4 x bits	54.5	1.213	0.738	1.715	1.051
AOI22	8/16/24/32	26.4 x bits	58.4	1.213	0.858	1.735	1.193

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for Buffer/Inverter design
- Four drive strength options for output

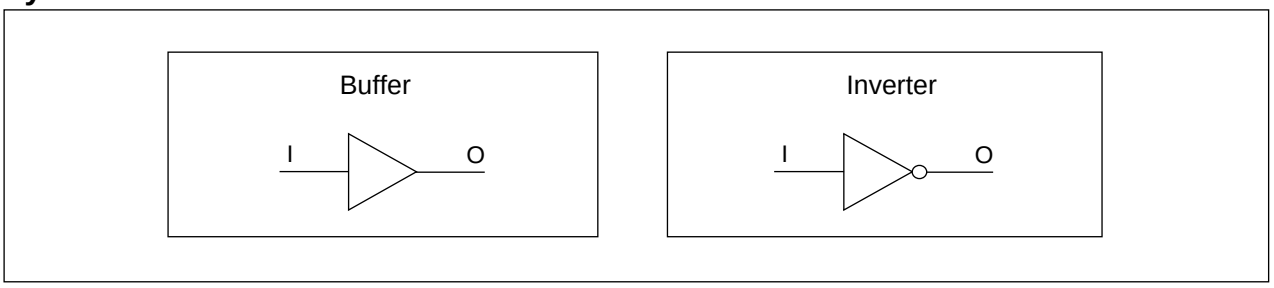
General Description

The high performance Buffer/Inverter design is optimized for multiple-targeted technologies. The generator design has the capability to build Buffers/Inverters ranging from 4-bits to 128-bits for various drive strength configurations.

Design Description

The Buffer/Inverter design has schematic and layout generators that can build a variety of Buffers and Inverters. You have an option to select either Buffer or Inverter by setting the “type” parameter to 1 or 0 respectively. The design supports four different drive strength options (1X, 2X, 4X and 8X).

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Type of a cell to be generated; 0: Inverter; 1: Buffer	0/1
drv	Drive strength	1/2/4/8

Buffer/Inverter

Pin Description

Pin Name	Description
I [bits–1:0]	Input
O [bits–1:0]	Output

Truth Table

Buffer	
I	**O**
0	0
1	1

Inverter	
I	**O**
0	1
1	0

Pin Capacitance

Pin Name	Value (pF)			
	Buffer		Inverter	
	DP80	DPM80	DP80	DPM80
I	0.023	0.022	0.031	0.030

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (µm x µm)		Delay (ns)			
		Width	Height	DP80		DPM80	
				T_{PLH}	T_{PHL}	T_{PLH}	T_{PHL}
Buffer	8/16/24/32	26.4 x bits	55.7	0.843	0.642	1.249	0.943
Inverter	8/16/24/32	26.4 x bits	53.6	0.913	0.521	1.314	0.789

Features

- Variable word width of 4 to 128 bits

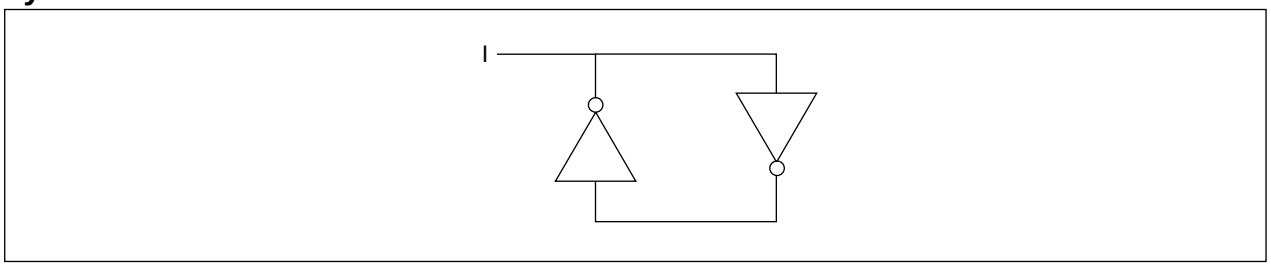
General Description

The high performance datapath Bus Holder design can be optimized for multiple-targeted technologies. The generator can build Bus Holders ranging from 4-bits to 128-bits.

Design Description

The Bus Holder design has schematic and layout generators that can build a variety of Bus Holders. The primary function of the Bus Holder is to hold the previous state, when the drivers on a bus go tri-stated.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128

Pin Description

Pin Name	Description
I [bits–1:0]	Data input

Pin Capacitance

Pin Name	Value (pF)	
	DP80	DPM80
I	0.055	0.054

D Flip-Flop

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Separate load enable line
- Scan logic, set, reset and tri-stated output with enable high input options
- Clock edge specification option
- Tri-stated, normal and inverted outputs
- Two drive strength options for output

General Description

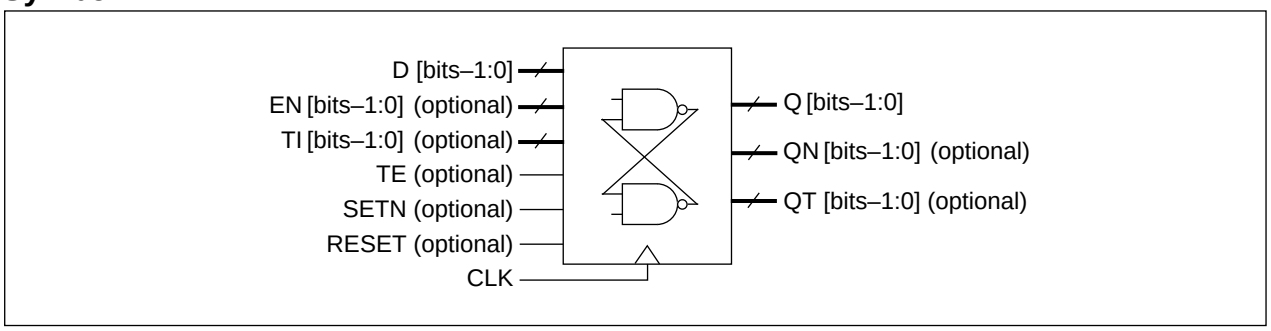
The high performance D Flip-Flop design can be optimized for multiple-targeted technologies. The generator can build D flip-flops ranging from 4-bits to 128-bits, with scan logic, set, reset and tri-stated output with enable high input options. The clock edge specification can also be controlled by users, either positive or negative edged. This generator supports a tri-state output and two different drive strengths.

Design Description

The D Flip-Flop design has schematic and layout generators that can build a variety of D flip-flops depending on the parameters set. The design supports scan inputs with test enable input. You can also have set, reset input along with the scan inputs, and tri-stated output with enable high input.

The clock edge can be specified by setting the clk parameter to 0 or 1 (negative clk or positive clk respectively). Both Q (normal data out), QN (inverted data out) and QT (tri-state data output) are available.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
scan	Scan inputs – 0: no scan; 1: scan	0/1
set	Set – 0: no; 1: set	0/1
rst	Reset – 0: no; 1: reset	0/1
tri	Tri-stated output with enable high input	0/1
q	Normal data output	0/1
qn	Inverted data output	0/1
clk	Clock edge spec. – 0: negative clk; 1: positive clk	0/1
drv	Drive strength	1/4

Pin Description

Pin Name	I/O	Description
D [bits–1:0]	I	Data input
EN [bits–1:0]		Enable input (optional when tri = 1)
TI [bits–1:0]		Test input (optional when scan = 1)
TE		Test enable input (optional when scan = 1)
SETN		Set input (optional when set = 1)
RESET		Reset input (optional when rst = 1)
CLK		Clock input (positive- or negative-edge)
Q [bits–1:0]	O	Normal data output
QN [bits–1:0]		Inverted data output (optional when qn = 1)
QT [bits–1:0]		Tri-stated data output (optional when tri = 1)

Truth Table

Positive edge trigger (clk = 1)									
Inputs							Outputs		
D	**CLK**	**EN**	**SETN**	**RESET**	**TI**	**TE**	**Q (n+1)**	**QN (n+1)**	**QT (n+1)**
x	x	0	x	x	x	x	x	x	Hi-Z
x	x	1	0	0	x	x	1	0	1
x	x	1	0	1	x	x	1	0	1
x	x	1	1	1	x	x	0	1	0
D	↓	1	1	0	x	0	Q (n)	QN (n)	QT (n)
D	↑	1	1	0	x	0	D	~D	D
x	↓	1	1	0	D	1	Q (n)	QN (n)	QT (n)
x	↑	1	1	0	D	1	D	~D	D

Negative edge trigger (clk = 0)									
Inputs							Outputs		
D	**CLK**	**EN**	**SETN**	**RESET**	**TI**	**TE**	**Q (n+1)**	**QN (n+1)**	**QT (n+1)**
x	x	0	x	x	x	x	x	x	Hi-Z
x	x	1	0	0	x	x	1	0	1
x	x	1	0	1	x	x	1	0	1
x	x	1	1	1	x	x	0	1	0
D	↑	1	1	0	x	0	Q (n)	QN (n)	QT (n)
D	↓	1	1	0	x	0	D	~D	D
x	↑	1	1	0	D	1	Q (n)	QN (n)	QT (n)
x	↓	1	1	0	D	1	D	~D	D

Pin Capacitance

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan = 0, clk = 0, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.031	0.031
(Parameters: qn = 1, q = 1, tri = 0, rst = 0, set = 0, scan = 0, clk = 0, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.031	0.031
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 0, clk = 0, drv = 1)			
CLK	8	0.272	0.264
	16	0.544	0.528
	24	0.816	0.792
	32	1.088	1.056
D	8/16/24/32	0.031	0.031
EN	8/16/24/32	0.023	0.023
QT	8/16/24/32	0.027	0.028
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 0, scan = 0, clk = 0, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.031	0.031
RESET	8	0.424	0.416
	16	0.848	0.832
	24	1.272	1.248
	32	1.696	1.664

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst =1, set = 0, scan = 0, clk = 0, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.512
	24	0.792	0.768
	32	1.056	1.024
D	8/16/24/32	0.031	0.030
EN	8/16/24/32	0.023	0.022
RESET	8	0.408	0.400
	16	0.816	0.800
	24	1.224	1.200
	32	1.632	1.600
QT	8/16/24/32	0.027	0.028
(Parameters: qn = 0, q = 1, tri = 0, rst = 1, set = 1, scan = 0, clk = 0, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.031	0.031
RESET	8	0.416	0.416
	16	0.832	0.832
	24	1.248	1.248
	32	1.664	1.664
SETN	8	0.416	0.408
	16	0.832	0.816
	24	1.248	1.224
	32	1.664	1.632

Pin Capacitance (Cont.)

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 1, q = 1, tri = 0, rst =1, set = 1, scan = 0, clk = 0, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.031	0.030
RESET	8	0.424	0.408
	16	0.848	0.832
	24	1.272	1.248
	32	1.696	1.664
SETN	8	0.424	0.408
	16	0.848	0.832
	24	1.272	1.224
	32	1.696	1.632
(Parameters: qn = 0, q = 1, tri = 1, rst =1, set = 1, scan = 0, clk = 0, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.031	0.030
EN	8/16/24/32	0.023	0.023
RESET	8	0.416	0.392
	16	0.832	0.784
	24	1.248	1.176
	32	1.664	1.568
SETN	8	0.400	0.400
	16	0.800	0.800
	24	1.200	1.200
	32	1.600	1.600
QT	8/16/24/32	0.027	0.029

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst =1, set = 1, scan = 1, clk = 0, drv = 1)			
CLK	8	0.272	0.264
	16	0.544	0.528
	24	0.816	0.792
	32	1.088	1.056
D	8/16/24/32	0.051	0.049
EN	8/16/24/32	0.023	0.023
TE	8	0.192	0.192
	16	0.384	0.384
	24	0.576	0.576
	32	0.768	0.768
TI	8/16/24/32	0.052	0.050
QT	8/16/24/32	0.026	0.028
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 1, clk = 0, drv = 1)			
CLK	8	0.272	0.264
	16	0.544	0.528
	24	0.816	0.792
	32	1.088	1.056
D	8/16/24/32	0.053	0.051
EN	8/16/24/32	0.023	0.023
RESET	8	0.424	0.416
	16	0.848	0.832
	24	1.272	1.248
	32	1.696	1.664
SETN	8	0.416	0.408
	16	0.832	0.816
	24	1.248	1.224
	32	1.664	1.632
TE	8	0.192	0.200
	16	0.384	0.400
	24	0.576	0.600
	32	0.768	0.800
TI	8/16/24/32	0.052	0.050
QT	8/16/24/32	0.027	0.029

Pin Capacitance (Cont.)

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 1, q = 1, tri = 0, rst =0, set = 0, scan = 0, clk = 1, drv = 1)			
CLK	8	0.264	0.256
	16	0.528	0.512
	24	0.792	0.768
	32	1.056	1.024
D	8/16/24/32	0.031	0.030
(Parameters: qn = 0, q = 1, tri = 1, rst =0, set = 0, scan = 0, clk = 1, drv = 1)			
CLK	8	0.264	0.256
	16	0.528	0.512
	24	0.792	0.768
	32	1.056	1.024
D	8/16/24/32	0.031	0.030
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 0, clk = 1, drv = 1)			
CLK	8	0.264	0.256
	16	0.528	0.512
	24	0.792	0.768
	32	1.056	1.024
D	8/16/24/32	0.031	0.030
EN	8/16/24/32	0.023	0.023
QT	8/16/24/32	0.027	0.028
(Parameters: qn = 1, q = 1, tri = 0, rst 01, set = 0, scan = 0, clk = 1, drv = 1)			
CLK	8	0.264	0.256
	16	0.528	0.512
	24	0.792	0.768
	32	1.056	1.024
D	8/16/24/32	0.031	0.030
RESET	8	0.416	0.392
	16	0.832	0.784
	24	1.248	1.176
	32	1.664	1.568

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst =1, set = 0, scan = 0, clk = 1, drv = 1)			
CLK	8	0.264	0.256
	16	0.528	0.512
	24	0.792	0.768
	32	1.056	1.024
D	8/16/24/32	0.031	0.030
EN	8/16/24/32	0.023	0.022
RESET	8	0.400	0.392
	16	0.800	0.784
	24	1.200	1.176
	32	1.600	1.568
QT	8/16/24/32	0.027	0.028
(Parameters: qn = 1, q = 1, tri = 0, rst =1, set = 1, scan = 0, clk = 1, drv = 1)			
CLK	8	0.264	0.256
	16	0.528	0.512
	24	0.792	0.768
	32	1.056	1.024
D	8/16/24/32	0.031	0.030
RESET	8	40.8	0.400
	16	0.816	0.800
	24	1.224	1.200
	32	1.632	1.600
SETN	8	0.408	0.400
	16	0.816	0.800
	24	1.224	1.200
	32	1.632	1.600

Pin Capacitance (Cont.)

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 0, rst = 1, set = 1, scan = 0, clk = 1, drv = 1)			
CLK	8	0.264	0.256
	16	0.528	0.512
	24	0.792	0.768
	32	1.056	1.024
D	8/16/24/32	0.031	0.030
RESET	8	0.416	0.392
	16	0.832	0.784
	24	1.248	1.176
	32	1.664	1.568
SETN	8	0.408	0.400
	16	0.816	0.800
	24	1.224	1.200
	32	1.632	1.600
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 0, clk = 1, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.031	0.030
EN	8/16/24/32	0.023	0.023
RESET	8	0.408	0.416
	16	0.816	0.832
	24	1.224	1.248
	32	1.632	1.664
SETN	8	0.408	0.400
	16	0.816	0.800
	24	1.224	1.200
	32	1.632	1.600
QT	8/16/24/32	0.027	0.029

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 1, clk = 1, drv = 1)			
CLK	8	0.256	0.256
	16	0.512	0.512
	24	0.768	0.768
	32	1.024	1.024
D	8/16/24/32	0.052	0.051
EN	8/16/24/32	0.023	0.023
TE	8	0.192	0.200
	16	0.384	0.400
	24	0.576	0.600
	32	0.768	0.800
TI	8/16/24/32	0.024	0.025
QT	8/16/24/32	0.027	0.028
(Parameters: qn = 0, q = 1, tri = 1, rst =1, set = 1, scan = 1, clk = 1, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.052	0.050
EN	8/16/24/32	0.023	0.023
RESET	8	0.416	0.408
	16	0.832	0.816
	24	1.248	1.224
	32	1.664	1.632
SETN	8	0.408	0.400
	16	0.816	0.800
	24	1.224	1.200
	32	1,632	1.600
TE	8	0.192	0.200
	16	0.384	0.400
	24	0.576	0.600
	32	0.768	0.800
TI	8/16/24/32	0.024	0.025
QT	8/16/24/32	0.027	0.029

D Flip-Flop

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bits	Parameters		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan = 0, clk = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	73.6	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.200	0.400
		hold_falling D CLK	0.200	0.200
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.277	1.774
		T_{PHL}	1.138	1.508
(Parameters: qn = 1, q = 1, tri = 0, rst = 0, set = 0, scan = 0, clk = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	77.8	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.200	0.400
		hold_falling D CLK	0.200	0.200
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.327	1.837
		T_{PHL}	1.168	1.543
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 0, clk = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	88.3	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.250	0.350
		hold_falling D CLK	0.200	0.200
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.903	2.964
		T_{PHL}	1.383	1.940
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 0, scan = 0, clk = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	84.1	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.200	0.400
		min_pulse_width_high RESET	0.250	0.350
		hold_falling D CLK	0.200	0.200
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.397	1.985
		T_{PHL}	1.158	1.519

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bits	Parameters		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 0, scan = 0, clk = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	92.5	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.250	0.350
		min_pulse_width_high RESET	0.250	0.350
		hold_falling D CLK	0.200	0.200
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.963	3.013
		T_{PHL}	1.383	1.949
(Parameters: qn = 0, q = 1, tri = 0, rst = 1, set = 1, scan = 0, clk = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
	Delay (ns)	Height	79.9	
		min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.200	0.400
		min_pulse_width_high RESET	0.250	0.350
		min_pulse_width_low SETN	0.200	0.400
		hold_falling D CLK	0.200	0.200
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.337	1.869
		T_{PHL}	1.158	1.525
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 1, scan = 0, clk = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	84.1	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.200	0.400
		min_pulse_width_high RESET	0.250	0.350
		min_pulse_width_low SETN	0.200	0.400
		hold_falling D CLK	0.200	0.200
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.407	1.983
		T_{PH}	1.208	1.597

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bits	Parameters		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 0, clk = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	92.5	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.250	0.350
		min_pulse_width_high RESET	0.250	0.350
		min_pulse_width_low SETN	0.250	0.350
		hold_falling D CLK	0.100	0.100
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.973	3.059
		T_{PHL}	1.423	1.994
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 1, clk = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	94.6	
	Delay (ns)	min_pulse_width_high CLK	0.400	0.350
		min_pulse_width_low CLK	0.250	0.350
		hold_falling D CLK	0.100	0.100
		hold_falling TI CLK	0.100	0.100
		setup_falling D CLK	0.600	0.700
		setup_falling TI CLK	0.600	0.700
		T_{PLH}	1.903	2.927
		T_{PHL}	1.383	1.953
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 1, clk = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	100.5	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.250	0.300
		min_pulse_width_high RESET	0.250	0.350
		min_pulse_width_low SETN	0.250	0.300
		hold_falling D CLK	0.100	0.000
		hold_falling TI CLK	0.100	0.000
		setup_falling D CLK	0.600	0.800
		setup_falling TI CLK	0.600	0.700
		T_{PLH}	1.973	3.067
		T_{PHL}	1.423	2.013

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bits	Parameters		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan = 0, clk = 1, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	73.6	
	Delay (ns)	min_pulse_width_high CLK	0.200	0.300
		min_pulse_width_low CLK	0.250	0.350
		hold_falling D CLK	–0.100	–0.100
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.167	1.726
		T_{PHL}	0.858	1.254
(Parameters: qn = 1, q = 1, tri = 0, rst = 0, set = 0, scan = 0, clk = 1, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	77.8	
	Delay (ns)	min_pulse_width_high CLK	0.200	0.300
		min_pulse_width_low CLK	0.250	0.350
		hold_falling D CLK	–0.100	–0.100
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.217	1.767
		T_{PHL}	0.989	1.283
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 0, clk = 1, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	88.3	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.250	0.350
		hold_falling D CLK	–0.100	–0.100
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.823	2.897
		T_{PHL}	1.143	1.689
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 0, scan = 0, clk = 1, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	84.1	
	Delay (ns)	min_pulse_width_high CLK	0.200	0.300
		min_pulse_width_low CLK	0.400	0.350
		min_pulse_width_high RESET	0.200	0.300
		hold_falling D CLK	–0.100	–0.100
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.297	1.913
		T_{PHL}	0.933	1.406

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bits	Parameters		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 0, scan = 0, clk = 1, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	92.5	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.250	0.350
		min_pulse_width_high RESET	0.250	0.350
		hold_falling D CLK	–0.100	–0.100
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.853	2.942
		T_{PHL}	1.113	1.627
(Parameters: qn = 0, q = 1, tri = 0, rst = 1, set = 1, scan =0, clk = 1, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	79.9	
	Delay (ns)	min_pulse_width_high CLK	0.200	0.300
		min_pulse_width_low CLK	0.250	0.400
		min_pulse_width_high RESET	0.200	0.300
		min_pulse_width_low SETN	0.350	0.400
		hold_falling D CLK	–0.100	–0.100
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.237	1.831
		T_{PHL}	0.898	1.315
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 1, scan = 0, clk = 1, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	84.1	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.300
		min_pulse_width_low CLK	0.300	0.400
		min_pulse_width_high RESET	0.250	0.300
		min_pulse_width_low SETN	0.300	0.400
		hold_rising D CLK	–0.100	–0.100
		T_{PLH}	1.297	0.000
		T_{PHL}	0.938	0.000

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bits	Parameters		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 0, clk = 1, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	92.5	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.250	0.350
		min_pulse_width_high RESET	0.250	0.350
		min_pulse_width_low SETN	0.250	0.350
		hold_rising D CLK	–0.100	–0.100
		setup_rising D CLK	0.500	0.600
		T_{PLH}	1.863	2.946
		T_{PHL}	1.153	1.691
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 1, clk = 1, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	94.6	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.250	0.350
		hold_falling D CLK	–0.100	–0.200
		hold_rising TI CLK	–0.100	–0.200
		setup_rising D CLK	0.500	0.700
		setup_falling TI CLK	0.500	0.700
		T_{PLH}	1.823	2.907
		T_{PHL}	1.143	1.683
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 1, clk = 1, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	100.5	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_low CLK	0.250	0.350
		min_pulse_width_high RESET	0.250	0.350
		min_pulse_width_low SETN	0.250	0.350
		hold_falling D CLK	–0.100	–0.200
		hold_rising TI CLK	–0.100	–0.300
		setup_rising D CLK	0.500	0.700
		setup_falling TI CLK	0.500	0.700
		T_{PLH}	1.863	2.946
		T_{PHL}	1.153	1.683

Full Adder

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Two drive strength options for output

General Description

The high performance datapath Full Adder design can be optimized for multiple-targeted technologies. This generator can build Full Adders ranging from 4-bits to 128-bits, supporting two different drive strengths.

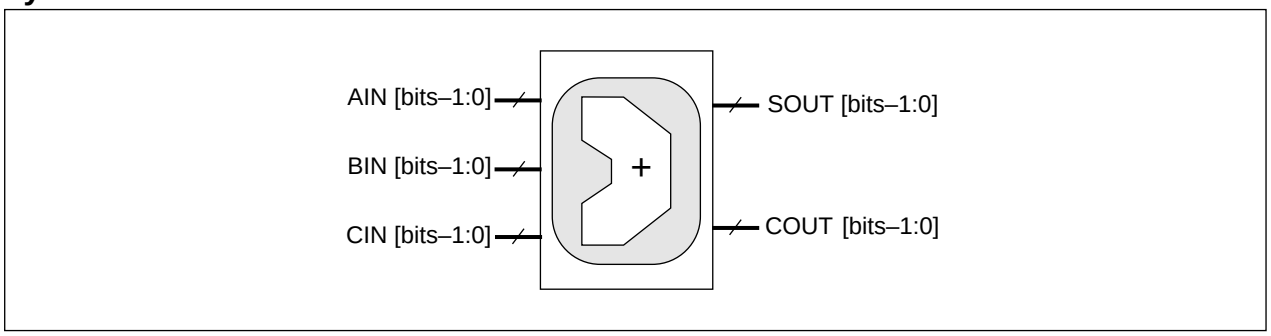
Design Description

The Full Adder design has schematic and layout generators that can build a variety of Full Adders. The design supports two different drive strengths (1X and 2X).

The sum output is expressed as: **SOUT = AIN ⊕ BIN ⊕ CIN**

The carry output is expressed as: **COUT = {(AIN | BIN) & CIN} | (AIN & BIN)**

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
drv	Drive strength	1/2

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Input AIN
BIN [bits–1:0]		Input BIN
CIN [bits–1:0]		Carry-in CIN
SOUT [bits–1:0]	O	Sum output
COUT [bits–1:0]		Carry output

Truth Table

Inputs			Outputs	
AIN	BIN	CIN	SOUT	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Pin Capacitance

Pin Name	Value (pF)	
	DP80	DPM80
AIN	0.056	0.056
BIN	0.072	0.065
CIN	0.067	0.064

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Area (μm x μm)		Delay (ns)			
	Width	Height	DP80		DPM80	
			T_{PLH}	T_{PHL}	T_{PLH}	T_{PHL}
8/16/24/32	26.4 x bits	75.7	1.287	0.936	1.817	1.448

Latch

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Separate load enable line
- Scan logic, set, reset and tri-stated output with enable high input options
- Tri-stated, normal and inverted output
- Two drive strength options for output

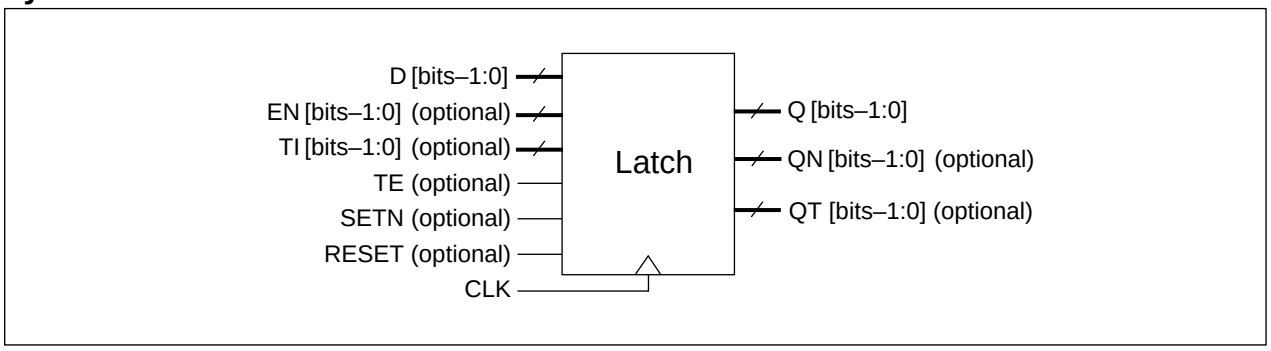
General Description

The high performance Latch design can be optimized for multiple-targeted technologies. The generator can build Latches ranging from 4-bits to 128-bits, with scan logic and set, reset and tri-stated output with enable high input options.This generator supports two different drive strengths.

Design Description

The Latch design has schematic and layout generators that can build a variety of Latches depending on the parameters set. The design supports scan inputs with test enable input. You can also have set or reset input, and tri-stated output with enable high input.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
scan	Scan inputs – 0: no scan; 1: scan	0/1
set	Set – 0: no; 1: set	0/1
rst	Reset – 0: no; 1: reset	0/1
tri	Tri-stated output with enable high input	0/1
q	Normal data output	0/1
qn	Inverted data output	0/1
drv	Drive strength	1/4

Pin Description

Pin Name	I/O	Description
D [bits–1:0]	I	Data input
EN [bits–1:0]		Enable input (optional when tri = 1)
TI [bits–1:0]		Test input (optional when scan = 1)
TE		Test enable input (optional when scan = 1)
SETN		Set input (optional when set = 1)
RESET		Reset input (optional when rst = 1)
CLK		Clock input
Q [bits–1:0]	O	Normal data output
QN [bits–1:0]		Inverted data output (optional when qn = 1)
QT [bits–1:0]		Tri-stated data output (optional when tri = 1)

Truth Table

Inputs							Outputs		
D	**CLK**	**EN**	**SETN**	**RESET**	**TI**	**TE**	**Q (n+1)**	**QN (n+1)**	**QT (n+1)**
x	x	0	x	x	x	x	x	x	HI-Z
x	x	1	0	0	x	x	1	0	1
x	x	1	0	1	x	x	1	0	1
x	x	1	1	1	x	x	0	1	0
D	0	1	1	0	x	0	Q (n)	QN (n)	QT (n)
D	1	1	1	0	x	0	D	~D	D
x	0	1	1	0	D	1	Q (n)	QN (n)	QT (n)
x	1	1	1	0	D	1	D	~D	D

Pin Capacitance

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan = 0, drv = 1)			
CLK	8	0.264	0.256
	16	0.528	0.512
	24	0.792	0.768
	32	1.056	1.024
D	8/16/24/32	0.032	0.031
(Parameters: qn = 1, q = 1, tri = 0, rst =0, set = 0, scan = 0, drv = 1)			
CLK	8	0.256	0.256
	16	0.512	0.512
	24	0.768	0.768
	32	1.024	1.024
D	8/16/24/32	0.032	0.031

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 0, q = 0, tri = 1, rst =0, set = 0, scan = 0, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.512
	24	0.792	0.768
	32	1.056	1.024
D	8/16/24/32	0.032	0.031
EN	8/16/24/32	0.023	0.022
QT	8/16/24/32	0.029	0.029

Pin Capacitance (Cont.)

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst =0, set = 0, scan = 0, drv = 1)			
CLK	8	0.264	0.256
	16	0.528	0.512
	24	0.792	0.768
	32	1.056	1.024
D	8/16/24/32	0.032	0.031
EN	8/16/24/32	0.023	0.022
QT	8/16/24/32	0.029	0.029
(Parameters: qn = 0, q = 1, tri = 0, rst = 1, set = 0, scan = 0, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.032	0.031
RESET	8	0.248	0.240
	16	0.496	0.480
	24	0.744	0.720
	32	0.992	0.960
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 0, scan = 0, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.032	0.031
RESET	8	0.248	0.240
	16	0.496	0.480
	24	0.744	0.720
	32	0.992	0.960

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 0, q = 0, tri = 1, rst = 1, set = 0, scan = 0, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.032	0.031
EN	8/16/24/32	0.023	0.022
RESET	8	0.248	0.248
	16	0.496	0.496
	24	0.744	0.744
	32	0.992	0.992
QT	8/16/24/32	0.028	0.029
(Parameters: qn = 0, q = 1, tri =1, rst =1, set = 0, scan = 0, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.032	0.031
EN	8/16/24/32	0.023	0.023
RESET	8	0.256	0.240
	16	0.512	0.480
	24	0.768	0.720
	32	1.024	0.960
QT	8/16/24/32	0.028	0.029
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan = 1, drv = 1)			
CLK	8	0.264	0.264
	16	0.528	0.528
	24	0.792	0.792
	32	1.056	1.056
D	8/16/24/32	0.053	0.051
TE	8	0.192	0.192
	16	0.384	0.384
	24	0.576	0.576
	32	0.768	0.768
TI	8/16/24/32	0.053	0.052

Pin Capacitance (Cont.)

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 1, drv = 1)			
CLK	8	0.264	0.256
	16	0.528	0.512
	24	0.792	0.768
	32	1.056	1.024
D	8/16/24/32	0.052	0.050
EN	8/16/24/32	0.023	0.023
TE	8	0.240	0.232
	16	0.480	0.464
	24	0.720	0.696
	32	0.960	0.928
TI	8/16/24/32	0.051	0.050
QT	8/16/24/32	0.029	0.030
(Parameters: qn = 0, q = 1, tri =1, rst =1, set = 1, scan = 0, drv = 1)			
CLK	8	0.272	0.264
	16	0.544	0.528
	24	0.816	0.792
	32	1.088	1.056
D	8/16/24/32	0.033	0.032
EN	8/16/24/32	0.023	0.022
RESET	8	0.256	0.256
	16	0.512	0.512
	24	0.768	0.768
	32	1.024	1.024
SETN	8	0.256	0.248
	16	0.512	0.496
	24	0.768	0.744
	32	1.024	0.992
QT	8/16/24/32	0.027	0.029

Pin Name	Bit	Value (pF)	
		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 1, drv = 1)			
CLK	8	0.272	0.264
	16	0.544	0.528
	24	0.816	0.792
	32	1.088	1.056
D	8/16/24/32	0.046	0.045
EN	8/16/24/32	0.023	0.022
RESET	8	0.248	0.256
	16	0.496	0.512
	24	0.744	0.768
	32	0.992	1.024
SETN	8	0.248	0.248
	16	0.496	0.496
	24	0.744	0.744
	32	0.992	0.992
TE	8	0.232	0.232
	16	0.464	0.464
	24	0.696	0.696
	32	0.928	0.928
TI	8/16/24/32	0.046	0.044
QT	8/16/24/32	0.027	0.029

Latch

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bits	Parameters		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan =0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	64.6	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		hold_falling D CLK	0.200	0.100
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.127	1.694
		T_{PHL}	0.932	1.237
(Parameters: qn = 1, q = 1, tri = 0, rst = 0, set = 0, scan = 0, drv = 1)				
8/16/24/3	Area (µm x µm)	Width	26.4 x bits	
		Height	69.4	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		hold_falling D CLK	0.100	0.100
		setup_falling D CLK	0.500	0.700
		T_{PLH}	1.197	1.743
		T_{PHL}	0.972	1.279
(Parameters: qn = 0, q = 0, tri = 1, rst = 0, set = 0, scan = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	75.7	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		hold_falling D CLK	0.200	0.100
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.723	2,759
		T_{PHL}	1.083	1.605
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	82.0	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		hold_falling D CLK	0.100	0.100
		setup_falling D CLK	0.500	0.700
		T_{PLH}	1.743	2.791
		T_{PHL}	1.113	1.617

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bits	Parameters		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 0, rst = 1, set = 0, scan =0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	67.3	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_high RESET	0.250	0.350
		hold_falling D CLK	0.100	0.100
		setup_falling D CLK	0.500	0.600
		T_{PLH}	1.197	1.777
		T_{PHL}	0.998	1.384
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 0, scan = 0, drv = 1)				
8/16/24/3	Area (µm x µm)	Width	26.4 x bits	
		Height	71.5	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_high RESET	0.250	0.350
		hold_rising D CLK	–1.300	–1.600
		setup_rising D CLK	1.600	2.000
		T_{PLH}	1.247	1.865
		T_{PHL}	0.942	1.352
(Parameters: qn = 0, q = 0, tri = 1, rst = 1, set = 0, scan = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
	Delay (ns)	Height	77.8	
		min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_high RESET	0.250	0.350
		hold_rising D CLK	–1.500	–1.900
		setup_rising D CLK	1.600	2.000
		T_{PLH}	1.793	2.861
		T_{PHL}	1.093	1.639
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 0, scan = 0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	82.0	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_high RESET	0.250	0.350
		hold_rising D CLK	–1.500	–1.900
		setup_rising D CLK	1.700	2.000
		T_{PLH}	1.823	2.918
		T_{PHL}	1.153	1.736

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bits	Parameters		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan =0, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	82.2	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_high RESET	0.250	0.350
		min_pulse_width_low SETN	0.250	0.350
		hold_rising D CLK	–1.600	–1.900
		setup_rising D CLK	1.700	2.100
		T_{PLH}	1.803	2.867
		T_{PHL}	1.361	1.851
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan = 1, drv = 1)				
8/16/24/3	Area (µm x µm)	Width	26.4 x bits	
		Height	71.0	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		hold_rising D CLK	–1.500	–2.000
		hold_rising TI CLK	–1.500	–2.000
		setup_rising D CLK	1.600	2.100
		setup_rising TI CLK	1.600	2.000
		T_{PLH}	1.237	1.880
		T_{PHL}	1.146	1.732
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 1, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	88.3	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		hold_rising D CLK	–1.600	–2.000
		hold_rising TI CLK	–1.500	–2.000
		setup_rising D CLK	1.700	2.100
		setup_rising TI CLK	1.700	2.100
		T_{PLH}	1.873	3.051
		T_{PHL}	1.361	1.873

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bits	Parameters		DP80	DPM80
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan =1, drv = 1)				
8/16/24/32	Area (µm x µm)	Width	26.4 x bits	
		Height	93.8	
	Delay (ns)	min_pulse_width_high CLK	0.250	0.350
		min_pulse_width_high RESET	0.250	0.350
		min_pulse_width_low SETN	0.250	0.350
		hold_rising D CLK	–1.600	–2.000
		hold_rising TI CLK	–1.600	–2.000
		setup_rising D CLK	1.700	2.200
		setup_rising TI CLK	1.700	2.200
		T_{PLH}	1.907	3.112
		T_{PHL}	1.391	1.931

Multiplexer

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for 2:1 to 8:1 multiplexing inputs with a variable number of bits
- Inverting and non-inverting options
- Configurable select inputs according to decoding and non-decoding options
- Three drive strength options for output

General Description

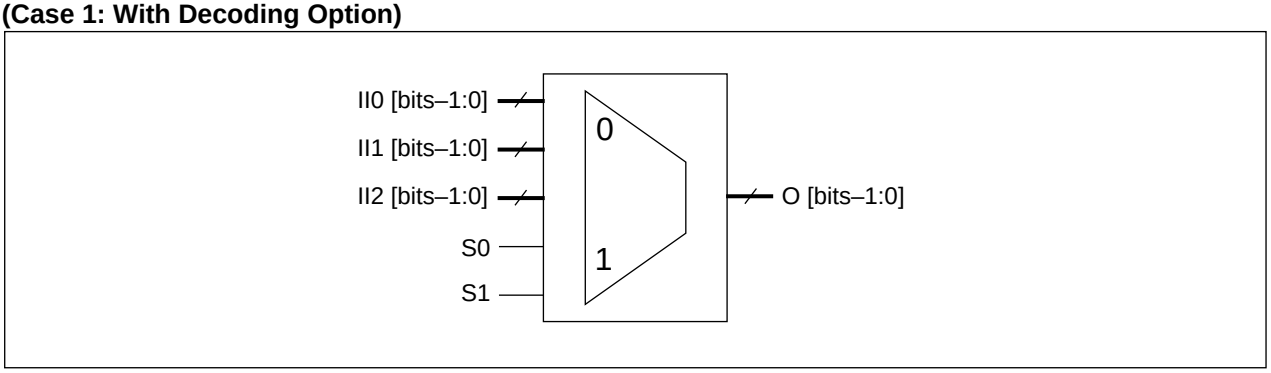
The multiplexer is optimized for multiple-targeted technologies. The generator n has the capability to build 2:1, 3:1, 4:1 and 8:1 multiplexer configurations from 4 to 128 bits range, with inverting and non-inverting, decoding and non-decoding options and three different drive strength capability.

Design Description

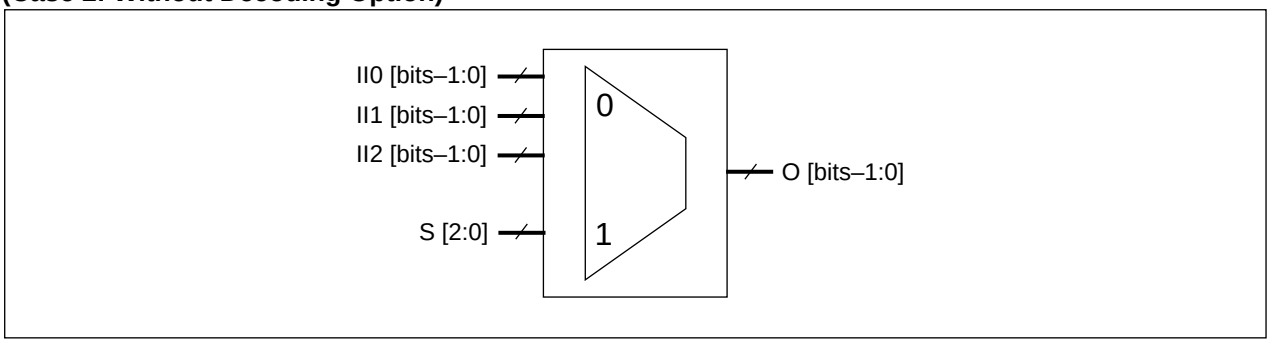
The Multiplexer has schematic and layout generators that can build a variety of multiplexers. You have options to select among two types of output buffering (inverting and non-inverting), two types of select inputs (decoding and non-decoding), three different sizes of output buffers, variable number of bits (4 to 128), and inputs ranging from 2 to 8.

Symbol (In case of 3:1 MUX)

(Case 1: With Decoding Option)



(Case 2: Without Decoding Option)



Pin Description

(Case 1)

Pin Name	I/O	Description
II0/II1/II2 [bits–1:0]	I	Data input
S0, S1		Select lines
O	O	Data output – The Multiplexer generator can produce an inverted or non-inverted output.

(Case 2)

Pin Name	I/O	Description
II0/II1/II2 [bits–1:0]	I	Data input
S [$\lceil \log_2 ins \rceil$–1:0]		Select lines
O	O	Data output – The Multiplexer generator can produce an inverted or non-inverted output.

$\lceil \ \rceil$ round-up

Truth Table

(Case 1)

Non-Inverted Output					
Inputs					Output
II0	II1	II2	S0	S1	O
1	0	0	0	0	1
0	1	0	0	1	1
0	0	1	1	x	1

Inverted Output					
Inputs					Output
II0	II1	II2	S0	S1	O
1	0	0	0	0	0
0	1	0	0	1	0
0	0	1	1	x	0

(Case 2)

Non-Inverted Output						
Inputs						Output
II0	II1	II2	S[0]	S[1]	S[2]	O
1	0	0	1	0	0	1
0	1	0	0	1	0	1
0	0	1	0	0	1	1

Inverted Output						
Inputs						Output
II0	II1	II2	S[0]	S[1]	S[2]	O
1	0	0	1	0	0	0
0	1	0	0	1	0	0
0	0	1	0	0	1	0

Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
ins	Number of inputs	2/3/4/8
type	Output buffering: inverting or non-inverting	0/1
sel	Select controlling: decoding of non-decoding	0/1
drv	Drive strengths	1/2/4

Pin Capacitance

3-1 MUX With Decoding Option			
Pin Name	Bit	Value (pF)	
		DP80	DPM80
II2	8/16/24/32	0.052	0.050
II1	8/16/24/32	0.053	0.050
II0	8/16/24/32	0.052	0.050
S1	8/16/24/32	0.030	0.029
S0	8/16/24/32	0.030	0.029

3-1 MUX Without Decoding Option			
Pin Name	Bit	Value (pF)	
		DP80	DPM80
II2	8/16/24/32	0.052	0.050
II1	8/16/24/32	0.053	0.050
II0	8/16/24/32	0.052	0.050
S	8	0.184	0.192
	16	0.368	0.384
	24	0.552	0.576
	32	0.736	0.768

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Area (µm x µm)		Delay (ns)			
	Width	Height	DP80		DPM80	
			T_{PLH}	T_{PHL}	T_{PLH}	T_{PHL}
3-1 MUX With Decoding Option						
8	26.4 x bits	71.5	1.564	1.276	2.292	1.765
16			1.704	1.402	2.572	2.036
24			1.843	1.528	2.842	2.316
32			1.980	1.653	3.122	2.596
3-1 MUX Without Decoding Option						
8/16/24/32	26.4 x bits	65.2	0.897	0.588	1.431	0.911

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for 2, 3 and 4 inputs
- Three drive strength options for input

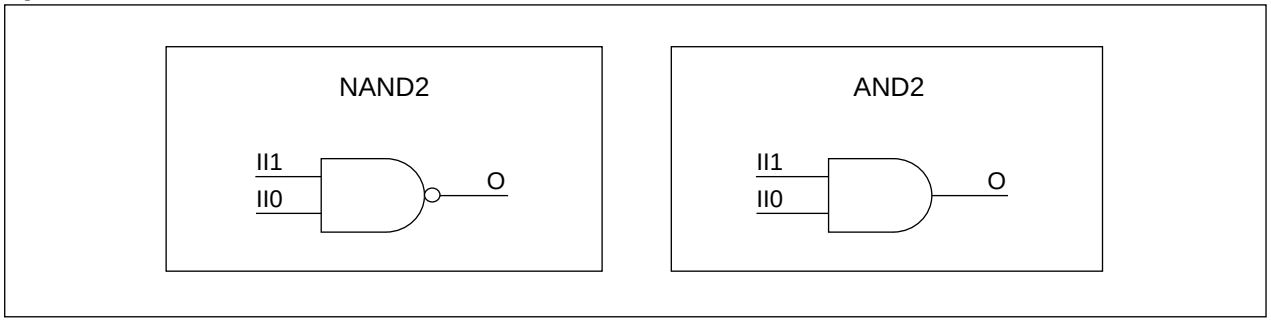
General Description

The high performance datapath NAND/AND design can be optimized for multiple-targeted technologies. This generator can build NAND/AND gates ranging from 4-bits to 128-bits for 2, 3 and 4 input configurations, supporting three different drive strengths.

Design Description

The NAND/AND design has schematic and layout generators that can build a variety of NAND and AND gates. You have an option to select either NAND or AND by setting the "type" parameter to 0 or 1 respectively. The design supports three different drive strengths (1X, 2X and 4X) and is also configured to build 2, 3 and 4-input gates.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
ins	Number of inputs	2/3/4
type	0: NAND; 1: AND	0/1
drv	Drive strength	1/2/4

NAND/AND

Pin Description

Pin Name	I/O	Description
II0 [bits–1:0]	I	Input pin – 2, 3, 4 input NAND/AND
II1 [bits–1:0]		Input pin – 2, 3, 4 input NAND/AND
II2 [bits–1:0]		Input pin – 3, 4 input NAND/AND
II3 [bits–1:0]		Input pin – 4 input NAND/AND
O	O	Output pin

Truth Table

NAND2		
Inputs		Output
II0	II1	O
0	0	1
0	1	1
1	0	1
1	1	0

AND2		
Inputs		Output
II0	II1	O
0	0	0
0	1	0
1	0	0
1	1	1

Pin Capacitance

Pin Name	Value (pF)			
	NAND4		AND4	
	DP80	DPM80	DP80	DPM80
II3	0.034	0.033	0.031	0.031
II2	0.034	0.033	0.031	0.030
II1	0.033	0.032	0.031	0.030
II0	0.031	0.030	0.031	0.030

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (μm x μm)		Delay (ns)			
		Width	Height	DP80		DPM80	
				T_{PLH}	T_{PHL}	T_{PLH}	T_{PHL}
NAND4	8/16/24/32	26.4 x bits	59.6	0.963	1.111	1.381	1.773
AND4	8/16/24/32	26.4 x bits	59.0	1.053	0.758	1.503	1.048

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for 2, 3 and 4 inputs
- Three drive strength options for output

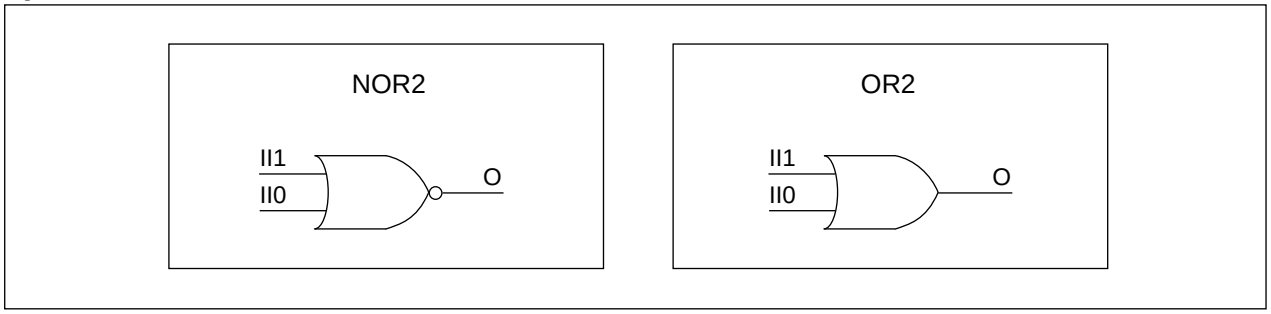
General Description

The high performance datapath NOR/OR design can be optimized for multiple-targeted technologies. This generator can build NOR/OR gates ranging from 4-bits to 128-bits for 2, 3 and 4 input configurations, supporting three different drive strengths.

Design Description

The NOR/OR design has schematic and layout generators that can build a variety of NOR and OR gates. You have an option to select either NOR or OR by setting the "type" parameter to 0 or 1 respectively. The design supports three different drive strengths (1X, 2X and 4X) and is also configured to build 2, 3 and 4-input gates.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
ins	Number of inputs	2/3/4
type	0: NOR; 1: OR	0/1
drv	Drive strength	1/2/4

Pin Description

Pin Name	I/O	Description
II0 [bits–1:0]	I	Input pin – 2-, 3-, 4-input NOR/OR
II1 [bits–1:0]		Input pin – 2-, 3-, 4-input NOR/OR
II2 [bits–1:0]		Input pin – 3-, 4-input NOR/OR
II3 [bits–1:0]		Input pin – 4-input NOR/OR
O	O	Output pin

Truth Table

NOR2		
Inputs		Output
II0	II1	O
0	0	1
0	1	0
1	0	0
1	1	0

OR2		
Inputs		Output
II0	II1	O
0	0	0
0	1	1
1	0	1
1	1	1

Pin Capacitance

Pin Name	Value (pF)			
	NOR4		OR4	
	DP80	DPM80	DP80	DPM80
II3	0.035	0.034	0.027	0.027
II2	0.036	0.035	0.028	0.028
II1	0.037	0.036	0.030	0.029
II0	0.037	0.036	0.029	0.028

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (μm x μm)		Delay (ns)			
		Width	Height	DP80		DPM80	
				T_{PLH}	T_{PHL}	T_{PLH}	T_{PHL}
NOR4	8/16/24/32	26.4 x bits	58.9	1.909	0.561	3.048	0.816
OR4	8/16/24/32	26.4 x bits	58.9	1.023	0.860	1.466	1.470

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for types 21 and 22
- Two drive strength options for output

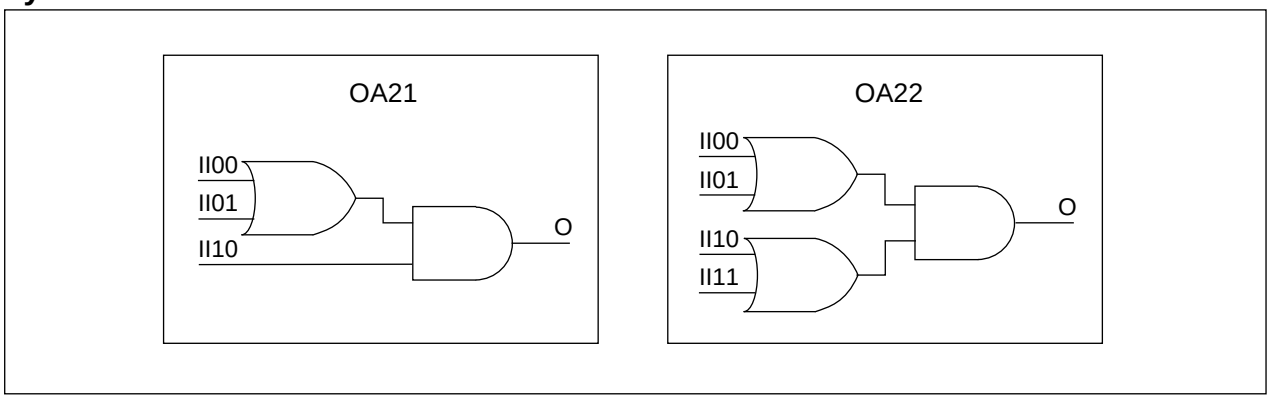
General Description

The high performance datapath OR-AND design can be optimized for multiple-targeted technologies. This generator can build OR-AND gates ranging from 4-bits to 128-bits for two different configurations (21 and 22) and two different drive strengths (1X and 2X).

Design Description

The OR-AND design has schematic and layout generators that can build a variety of OR-AND gates. You have an option to build the different kinds of OA structure configurations by setting the "type" parameter to 21 or 22 depending on your application.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Configuration type	21/22
drv	Drive strength	1/2

Pin Description

OA22		
Pin Name	**I/O**	**Description**
II00 [bits–1:0]	I	Data input
II01 [bits–1:0]		Data input
II10 [bits–1:0]		Data input
II11 [bits–1:0]		Data input
O	O	Data output

Truth Table

OA21			
Inputs			**Output**
II00	**II01**	**II10**	**O**
1	x	1	1
x	1	1	1
x	x	0	0
0	0	x	0

OA22				
Inputs				**Output**
II00	**II01**	**II10**	**II11**	**0**
1	x	1	x	1
x	1	1	x	1
1	x	x	1	1
x	1	x	1	1
0	0	x	x	0
x	x	0	0	0

Pin Capacitance

OA21		
Pin Name	**Value (pF)**	
	DP80	**DPM80**
II10	0.033	0.032
II01	0.031	0.031
II00	0.032	0.031

OA22		
Pin Name	**Value (pF)**	
	DP80	**DPM80**
II11	0.031	0.031
II10	0.034	0.033
II01	0.031	0.030
II00	0.032	0.031

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	**Bit**	**Area (μm x μm)**		**Delay (ns)**			
		Width	**Height**	**DP80**		**DPM80**	
				T_{PLH}	**T_{PHL}**	**T_{PLH}**	**T_{PHL}**
OA21	8/16/24/32	26.4 x bits	56.8	0.913	0.732	1.337	1.079
OA22	8/16/24/32	26.4 x bits	58.9	0.928	0.881	1.317	1.487

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for types 21 and 22
- Two drive strength options for output

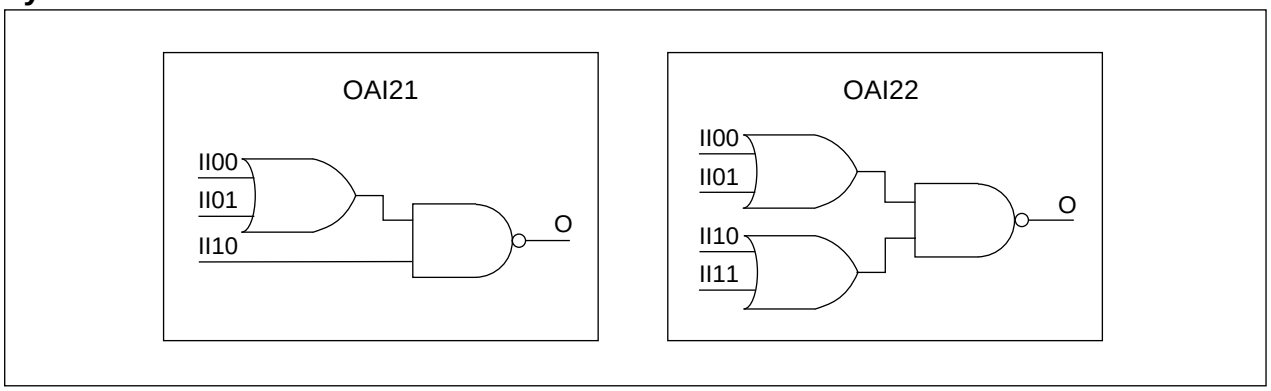
General Description

The high performance datapath OR-AND-INVERT design can be optimized for multiple-targeted technologies. This generator can build OR-AND-INVERT gates ranging from 4-bits to 128-bits for two different configurations (21 and 22) and two different drive strengths (1X and 2X).

Design Description

The OR-AND-INVERT design has schematic and layout generators that can build a variety of OR-AND-INVERT gates. You have an option to build the different kinds of OAI structure configurations by setting the "type" parameter to 21 or 22 depending on your application.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Configuration type	21/22
drv	Drive strength	1/2

Pin Description

OAI22		
Pin Name	**I/O**	**Description**
II00 [bits–1:0]	I	Data input
II01 [bits–1:0]		Data input
II10 [bits–1:0]		Data input
II11 [bits–1:0]		Data input
O	O	Data output

Truth Table

OAI21			
Inputs			**Output**
II00	**II01**	**II10**	**O**
1	x	1	0
x	1	1	1
x	x	0	1
0	0	x	1

OAI22				
Inputs				**Output**
II00	**II01**	**II10**	**II11**	**O**
1	x	1	x	0
x	1	1	x	0
1	x	x	1	0
x	1	x	1	0
0	0	x	x	1
x	x	0	0	1

Pin Capacitance

OAI21		
Pin Name	**Value (pF)**	
	DP80	**DPM80**
II10	0.024	0.024
II01	0.025	0.025
II00	0.025	0.024

OAI22		
Pin Name	**Value (pF)**	
	DP80	**DPM80**
II11	0.023	0.023
II10	0.022	0.022
II01	0.023	0.023
II00	0.024	0.024

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	**Bit**	**Area (μm x μm)**		**Delay (ns)**			
		Width	**Height**	**DP80**		**DPM80**	
				T_{PLH}	**T_{PHL}**	**T_{PLH}**	**T_{PHL}**
OAI21	8/16/24/32	26.4 x bits	54.5	1.163	0.778	1.671	1.109
OAI22	8/16/24/32	26.4 x bits	58.4	1.283	0.758	1.825	1.103

Features

- Technology-independent generator
- Variable word width of 4 to 128 bits
- Configurable for tri-state buffer/inverter design
- Four drive strength options for output

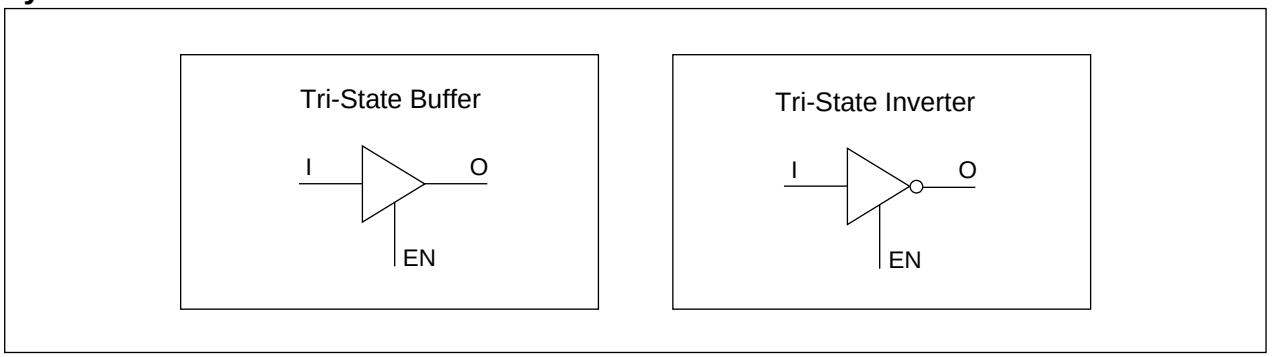
General Description

The high performance Tri-State Buffer/Inverter design is optimized for multiple-targeted technologies. The generator design has the capability to build tri-state buffers/inverters ranging from 4-bits to 128-bits for various drive strength configurations.

Design Description

The Tri-State Buffer/Inverter design has schematic and layout generators that can build a variety of tri-state buffers and inverters. You have an option to select either Tri-State Buffer or a Tri-State Inverter by setting the "type" parameter to 1 or 0 respectively. The design supports 4 different drive strength options (1X, 2X, 4X, 8X) for the tri-state buffer and 2 drive strength options (1X and 2X) for the tri-state inverter.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	0: Tri-State Inverter; 1: Tri-State Buffer	0/1
drv	Drive strength	1/2/4/8

NOTE: For type = 0, only 1X and 2X supported.

Tri-State Buffer/Inverter

Pin Description

Pin Name	Description
I [bits–1:0]	Input
EN [bits–1:0]	High enable
O [bits–1:0]	Output

Truth Table

Tri-State Buffer		
Inputs		Output
I	EN	O
x	0	Hi-Z
0	1	0
1	1	1

Tri-State Inverter		
Inputs		Output
I	EN	O
x	0	Hi-Z
0	1	1
1	1	0

Pin Capacitance

Pin Name	Value (pF)			
	Tri-State Buffer		Tri-State Inverter	
	DP80	DPM80	DP80	DPM80
EN	0.049	0.047	0.034	0.033
I	0.050	0.049	0.049	0.048
O	0.026	0.027	0.059	0.058

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Area (µm x µm)		Delay (ns)			
	Width	Height	DP80		DPM80	
			T_{PLH}	T_{PHL}	T_{PLH}	T_{PHL}
Tri-State Buffer						
8/16/24/32	26.4 x bits	63.7	0.831	0.773	1.238	1.027
Tri-State Inverter						
8/16/24/32	26.4 x bits	61.0	0.884	0.525	1.286	0.773

Features

- Technology-independent generator
- Variable word width of 4 to 128 bits
- Configurable for 2 and 3 inputs
- Configurable for XNOR/XOR design
- Three drive strength options for output

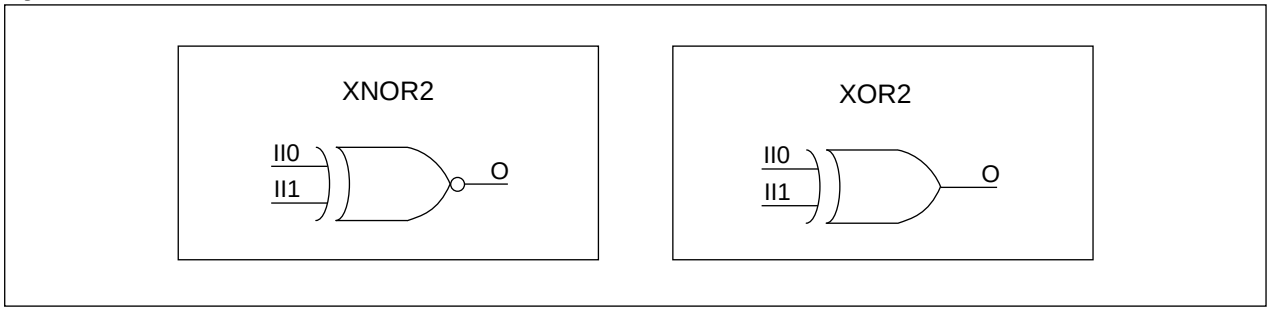
General Description

The high performance datapath XNOR/XOR design can be optimized for multiple targeted technologies. The generator can build XNOR/XOR gates ranging from 4-bits to 128-bits for 2 and 3 input configurations, supporting three different drive strengths.

Design Description

The XNOR/XOR design has schematic and layout generators that can build a variety of XNOR and XOR gates. You have an option to select either XNOR or XOR by setting the “type” parameter to 0 or 1 respectively. The design supports three different drive strengths (1X, 2X and 4X) and is also configured to build 2- and 3-input gates.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
ins	Number of inputs	2/3
type	0: XNOR; 1: XOR	0/1
drv	Drive strength	1/2/4

NOTE: When ins = 3, only drv = 1 and 2 are supported.

XNOR/XOR

Pin Description

Pin Name	I/O	Description
II0 [bits–1:0]	I	Input pin – 2-, 3-input XNOR/XOR
II1 [bits–1:0]		Input pin – 2-, 3-input XNOR/XOR
II2 [bits–1:0]		Input pin – 3-input XNOR/XOR
O	O	Output pin

Truth Table

XNOR2		
Inputs		Output
II0	II1	O
0	0	1
0	1	0
1	0	0
1	1	1

XOR2		
Inputs		Output
II0	II1	O
0	0	0
0	1	1
1	0	1
1	1	0

Pin Capacitance

Pin Name	Value (pF)			
	XNOR3		XOR3	
	DP80	DPM80	DP80	DPM80
II2	0.027	0.027	0.027	0.027
II1	0.030	0.030	0.030	0.030
II0	0.035	0.034	0.035	0.034

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (μm x μm)		Delay (ns)			
		Width	Height	DP80		DPM80	
				T_{PLH}	T_{PHL}	T_{PLH}	T_{PHL}
XNOR3	8/16/24/32	26.4 x bits	65.2	1.315	0.965	1.892	1.468
XOR3	8/16/24/32	26.4 x bits	65.2	1.008	0.885	1.497	1.415

JTAG Boundary Scans 7

Contents

Overview 7-1
Boundary Scan Architecture 7-2
Boundary Scan Register Macrocells 7-4
- JTBI1 7-5
- JTCK 7-12
- JTIN1 7-14
- JTINT1 7-18
- JTOUT1 7-24

JTAG Tap Controller Macrofunction 7-28
Instruction Register/Decoder Macrofunction 7-31
Implementation of IEEE P1149.1/JTAG 7-32
System Clock Considerations 7-32

OVERVIEW

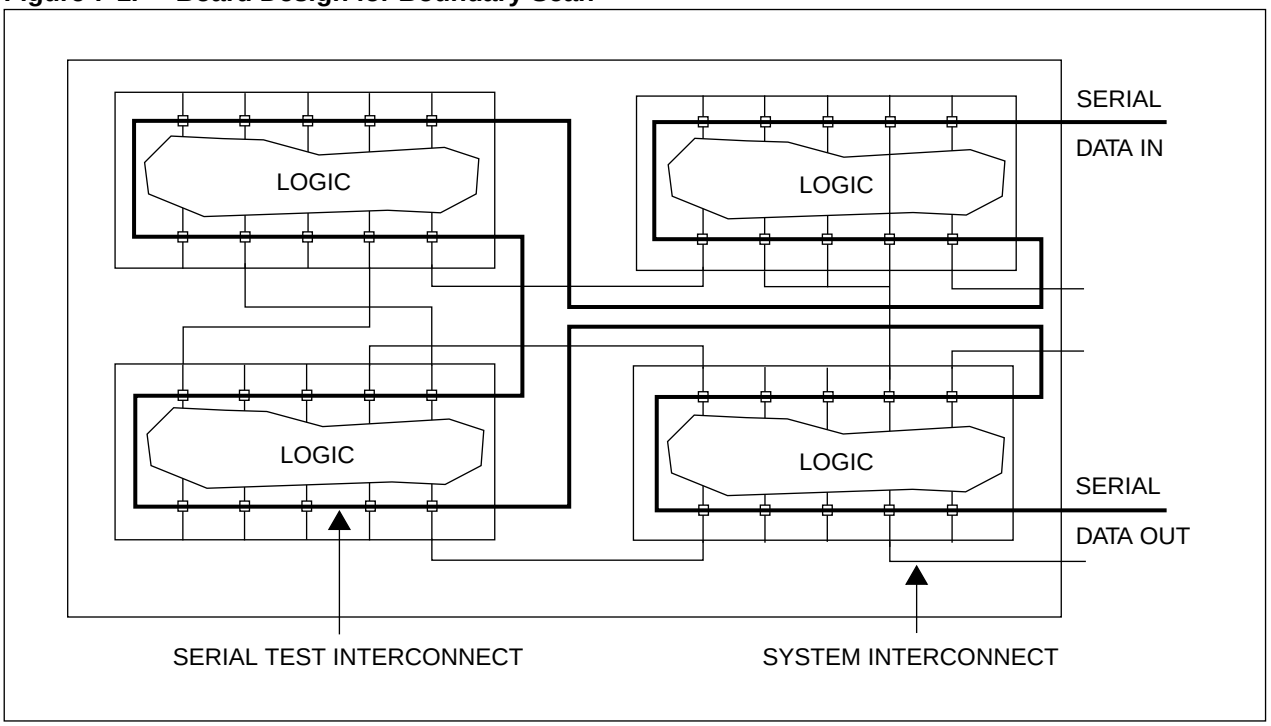
A board test is typically achieved by using in-circuit test techniques. However, in-circuit test techniques demonstrate significant limitations for Surface Mount Technology (SMT) and Fine Pitch Technology (FPT) boards. The pin and pad spacings getting tighter make it difficult to test boards with traditional methods economically and reliably.

A boundary scan design reduces the cost of a function test. A boundary scan design circuitry allows boards to be tested using the equivalent in-circuit test technique without bed-of-nails fixture. In recognition of the increasing acceptance of the boundary scan test, IEEE and JTAG (Joint Test Action Group) developed IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std 1149.1).

A boundary scan technique requires to place a boundary scan cell adjacent to each component pin so that signals at component boundaries can be controlled and observed using scan testing principles. Each boundary scan cell for a given component is able to capture data from an input pin or from its internal logic, and to drive its internal logic or an output pin. Boundary scan cells for the pins of a given component are interconnected so as to form a shift-register chain around the border of the design, known as a boundary scan register. Boundary scan registers for individual components can be connected in series to form a single path through the complete design as shown in the figure 9-1. Alternatively, a board design can contain several independent boundary scan paths that allow individual components to be tested as well as the interconnections between components.

To test component interconnections, test data are first shifted into all boundary scan register cells associated with component output test pins. Test data are then loaded into parallel inputs of boundary scan cells associated with input pins through the component interconnections, and data captured in these cells are shifted out from the boundary cells for evaluation. For an individual component test, a boundary scan register is used to isolate on-chip system logic from stimuli received from surrounding components. An actual test can be performed through the boundary scan path or the built-in self-test hardware.

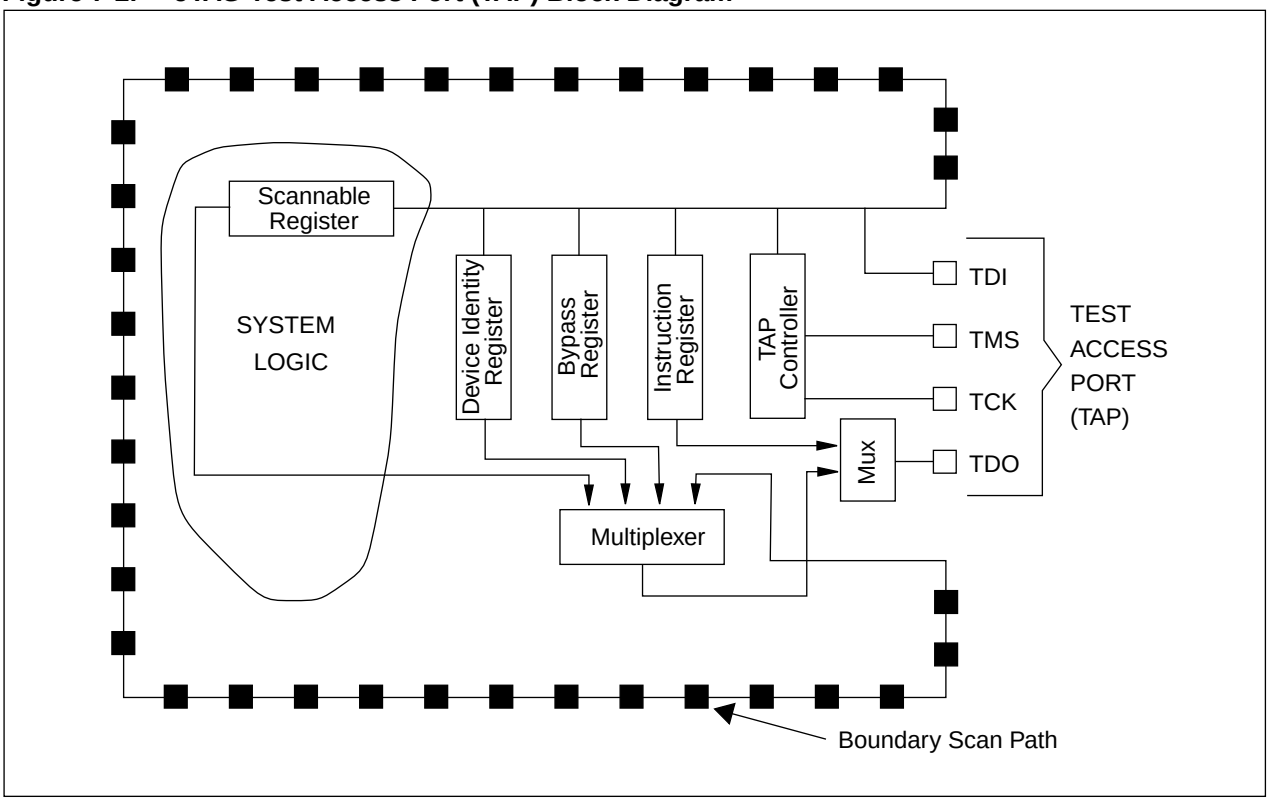
Figure 7-1. Board Design for Boundary Scan



BOUNDARY SCAN ARCHITECTURE

A boundary scan architecture contains TAP (Test Access Port), TAP controller, instruction register and a group of test data registers. The instruction and test data registers are separate shift-register-based paths connected in parallel with a common serial data input and a common serial data output which are connected to TAP, TDI and TDO signals. TAP controller selects the alternative instruction and test data register paths between TDI and TDO. The schematic view of the top level design of the test logic architecture is shown in the figure 9-2.

Figure 7-2. JTAG Test Access Port (TAP) Block Diagram



Boundary Scan Functional Block Descriptions

TAP (Test Access Port)

TAP is a general-purpose port that can provide with an access to many test support functions built into a component, including the test logic. It includes three inputs (TCK; Test Clock Signal, TMS; Test Mode Signal and TDI; Test Data Input) and one output (TDO; Test Data Output) required by the test logic. An optional fourth input (TRSTN; Test Reset) is provided for the asynchronous initialization of the test logic. The values applied at TMS and TDI pins are sampled on the rising edge of TCK, and the value placed on TDO pin changes on the falling edge of TCK.

TAP Controller

TAP controller receives TCK, interprets the signals on TMS, and generates clock and control signals for both instruction and test data registers and for other parts of the test circuitries as required.

Instruction Register/Instruction Decoder

Test instructions are shifted into and held by the instruction register. Test instructions include a selection of tests to be performed or the test data register to be accessed. A basic 3-bit instruction register and its instruction decoder are provided as macrofunctions in the library.

Test Data Registers

Data registers include a bypass register, a boundary scan register, a device identification register and other design specific registers. Only the bypass- and boundary scan registers are mandatory; the rest are optional.

Bypass register:	The bypass register provides a single-bit serial connection through the circuit when none of the other test data registers is selected. It can be used to allow test data to flow through a given device to the other components in a product without affecting a normal operation.
Boundary scan register:	The boundary scan register detects typical production defects in board interconnects, such as opens, shorts, etc. It also allows an access to component inputs and outputs when you test their logic or sample flow-through signals. Special boundary scan register macrocells are provided for this purpose. These special registers is discussed in the next section of next pages.
Design-specific test data register:	These optional registers may be provided to allow an access to design-specific test support features in the integrated circuit, such as self-test, scan test.
Device identification register:	This is an optional test data register that allows the manufacturer part number and variant of a components to be identified. The 32-bit identification register is partitioned into four fields:

Device version identifier	1st field	The first four bits beginning from MSB
Device part number	2nd field	16 bits
Manufacturer's JEDEC number	3rd field	11 bits
LSB	4th field	1 bit —tied in High

The ASIC designer is free to fill the version and part number in any manner as long as the total twenty bits are used.

SEC's JEDEC code:	78 decimal = 1001110 Continuation field (4 bits) = 0000
Contents of device identification register:	XXXX XXXXXXXXXXXXXXX 0000 1001110 1 Users can define these two fields.

BOUNDARY SCAN REGISTER MACROCELLS

The boundary scan register allows testing of circuitry external to the integrated circuit and provides for defined conditions to be established at the periphery of the on-chip system logic while it is tested itself. It also permits signals flowing through system pins to be sampled and examined without interfering with the operation of the on-chip system logic. The boundary scan register has four capabilities:

Capture: Loads data into the boundary scan register in parallel on the rising edge of TCK. It does not affect the output until Update is executed.

Shift: Shifts data from one boundary scan register to the next register towards the serial data output pin on the rising edge of TCK.

Update: Loads data in the boundary scan register into the parallel data output pin on the falling edge of TCK when EXTEST or INTEST instruction is selected.

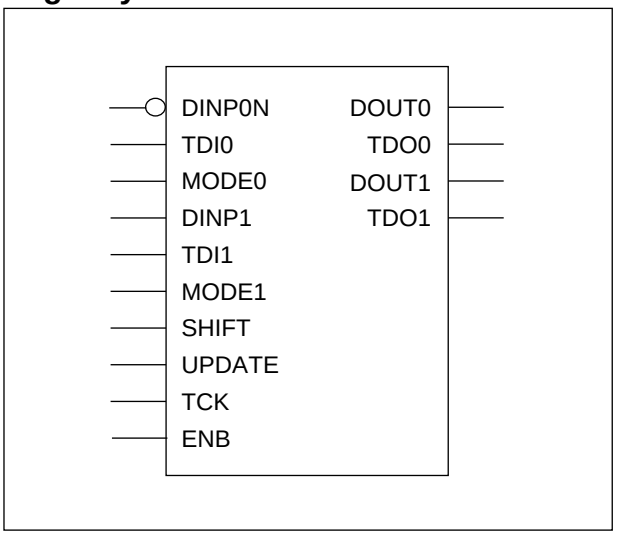
Set: Sets the parallel output pin.

SEC supports five types of boundary scan registers. Four of them, JTCK, JTBI1, JTIN1 and JTOUT1 are to be implemented around the periphery of the die next to I/O cells. For this reason, two I/O pads at each corner, that is, the total of eight I/O pads for the entire chip are not scannable. An implementation is automatically performed during a placement to achieve the most optimum placement with a minimum performance penalty. The fifth cell, JTINT1, is to be placed in the core area of the die for tri-state I/O control. Applications for each type of boundary scan register cell are summarized as follows.

Cell List

Cell Name	Function Description	Page
JTBI1	Bi-directional I/O Boundary Scan Cell	7-5
JTCK	Special Input (such as Clock Input) Boundary Scan Cell	7-12
JTIN1	Input Boundary Scan Cell	7-14
JTINT1	Tri-State I/O Control Boundary Scan Cell	7-18
JTOUT1	Output Boundary Scan Cell	7-24

Logic Symbol



Cell Data

Input Loading (SL)		
	STD80	**STDM80**
DINP0N	0	4
TDI0	2	1
MODE0	1	1
DINP1	2	3
TDI1	2	1
MODE1	1	1
SHIFT	2	2
UPDATE	3	2
TCK	1	1
ENB	0	0
Gate Count		
22		

Pin Description

Pin name	I/O	Description
DINP0N	I	Parallel Data Input Active Low for the Input Part of the Bi-Directional Pin
TDI0	I	Serial Test Data Input for Input Part of the Bi-Directional Pin
MODE0	I	Mode Select for Input Part—Low for Data Input and High for Internal Register Data Value
DINP1	I	Parallel Data Input Active Low for the Output Part of the Bi-Directional Pin
TDI1	I	Serial Test Data Input for Input Part of the Bi-Directional Pin
MODE1	I	Mode Select for Output Part—Low for Data Input and High for Internal Register Data Value
SHIFT	I	Active High Shift Control Input
UPDATE	I	Update Latch Input—Low for Update
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable
DOUT0	O	Parallel Data Output for Input Part of the Bi-Directional Pin
TDO0	O	Serial Test Data Output for Input Part of the Bi-Directional Pin
DOUT1	O	Parallel Data Output for Output Part of the Bi-Directional Pin
TDO1	O	Serial Test Data Output for Output Part of the Bi-Directional Pin

JTBI1

Bi-directional I/O Scan Cell with Capture, Shift and Update

Truth Table

DINP0N	TDI0	MODE0	SHIFT	UPDATE	TCK	ENB	OUTPUT
							DOUT0
0	X	0	X	X	X	X	1
1	X	0	X	X	X	X	0
X	X	1	X	X	X	X	LatchQN
							TDO0
X	X	X	X	X	↗	0	TDO0o
0	X	0	0	X	↗	1	1
1	X	0	0	X	↗	1	0
X	X	1	0	X	↗	1	LatchQN
X	0	X	1	X	↗	1	0
X	1	X	1	X	↗	1	1
X	X	X	X	X	0	X	TDO0o
X	X	X	X	X	1	X	TDO0o
X	X	X	X	X	↘	X	TDO0o
							LatchQN
X	X	X	X	0	X	X	TDO0
X	X	X	X	1	X	X	LatchQNo

DINP1	TDI1	MODE1	SHIFT	UPDATE	TCK	ENB	OUTPUT
							DOUT1
0	X	0	X	X	X	X	0
1	X	0	X	X	X	X	1
X	X	1	X	X	X	X	LatchQ
							TDO1
X	X	X	X	X	↗	0	TDO1o
0	X	X	0	X	↗	1	0
1	X	X	0	X	↗	1	1
X	0	X	1	X	↗	1	0
X	1	X	1	X	↗	1	1
X	X	X	X	X	0	X	TDO1o
X	X	X	X	X	1	X	TDO1o
X	X	X	X	X	↘	X	TDO1o
							LatchQ
X	X	X	X	0	X	X	TDO1
X	X	X	X	1	X	X	LatchQo

NOTES:

1. Outputs are defined in separate truth tables. In addition, the internal states known as “LatchQ” and “LatchQN” are defined as the output of the latch in the logic diagram.
2. JTBI1 has a similar truth table to JTIN1 and JTOUT1 macrocells without SETN input. It has similar delays to JTIN1 and JTOUT1.

Timing Requirements

(Typical process, 25°C, 5V, 3.3V)

Parameter	Symbol	Value (ns)	
		STD80	STDM80
Input Setup Time (TDI0 to TCK)	t_{SU}	0.46	0.60
Input Hold Time (TDI0 to TCK)	t_{HD}	0.41	0.41
Input Setup Time (TDI0 to ENB)	t_{SU}	0.46	0.57
Input Hold Time (TDI0 to ENB)	t_{HD}	0.38	0.41
Input Setup Time (TDI1 to TCK)	t_{SU}	0.46	0.60
Input Hold Time (TDI1 to TCK)	t_{HD}	0.41	0.41
Input Setup Time (TDI1 to ENB)	t_{SU}	0.46	0.57
Input Hold Time (TDI1 to ENB)	t_{HD}	0.38	0.41
Input Setup Time (DINP0N to TCK)	t_{SU}	0.74	1.01
Input Hold Time (DINP0N to TCK)	t_{HD}	0.33	0.33
Input Setup Time (DINP0N to ENB)	t_{SU}	0.74	1.01
Input Hold Time (DINP0N to ENB)	t_{HD}	0.33	0.33
Input Setup Time (DINP1 to TCK)	t_{SU}	0.46	0.60
Input Hold Time (DINP1 to TCK)	t_{HD}	0.41	0.41
Input Setup Time (DINP1 to ENB)	t_{SU}	0.49	0.60
Input Hold Time (DINP1 to ENB)	t_{HD}	0.38	0.41
Input Setup Time (SHIFT to TCK)	t_{SU}	0.60	0.76
Input Hold Time (SHIFT to TCK)	t_{HD}	0.52	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.60	0.74
Input Hold Time (SHIFT to ENB)	t_{HD}	0.74	0.33
Input Setup Time (MODE0 to TCK)	t_{SU}	0.82	1.15
Input Hold Time (MODE0 to TCK)	t_{HD}	0.33	0.33
Input Setup Time (MODE0 to ENB)	t_{SU}	0.82	1.12
Input Hold Time (MODE0 to ENB)	t_{HD}	0.33	0.33

JTBI1

Bi-directional I/O Scan Cell with Capture, Shift and Update

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 JTBI1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO0	t_{PLH}	0.94	0.88 + 0.030*SL	0.90 + 0.024*SL	0.90 + 0.024*SL
	t_{PHL}	0.81	0.73 + 0.043*SL	0.74 + 0.038*SL	0.74 + 0.037*SL
	t_R	0.22	0.14 + 0.041*SL	0.12 + 0.048*SL	0.09 + 0.052*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.067*SL	0.08 + 0.069*SL
ENB to TDO0	t_{PLH}	0.93	0.93 + 0.003*SL	0.87 + 0.029*SL	0.92 + 0.024*SL
	t_{PHL}	0.80	0.73 + 0.032*SL	0.71 + 0.042*SL	0.76 + 0.037*SL
	t_R	0.21	0.14 + 0.038*SL	0.11 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.24	0.12 + 0.063*SL	0.11 + 0.067*SL	0.08 + 0.069*SL
TCK to TDO1	t_{PLH}	0.92	0.86 + 0.028*SL	0.87 + 0.024*SL	0.87 + 0.024*SL
	t_{PHL}	0.78	0.70 + 0.041*SL	0.71 + 0.037*SL	0.71 + 0.037*SL
	t_R	0.20	0.13 + 0.039*SL	0.11 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.09 + 0.068*SL	0.09 + 0.069*SL
ENB to TDO1	t_{PLH}	0.90	0.90 + -0.001*SL	0.84 + 0.029*SL	0.89 + 0.024*SL
	t_{PHL}	0.79	0.65 + 0.070*SL	0.72 + 0.038*SL	0.73 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.10 + 0.066*SL	0.10 + 0.068*SL	0.08 + 0.069*SL
DINP0N to DOUT0	t_{PLH}	0.18	0.14 + 0.021*SL	0.14 + 0.018*SL	0.20 + 0.012*SL
	t_{PHL}	0.23	0.15 + 0.043*SL	0.20 + 0.018*SL	0.20 + 0.018*SL
	t_R	0.23	0.19 + 0.018*SL	0.19 + 0.019*SL	0.12 + 0.026*SL
	t_F	0.27	0.12 + 0.074*SL	0.23 + 0.026*SL	0.15 + 0.033*SL
MODE0 to DOUT0	t_{PLH}	0.34	0.27 + 0.034*SL	0.32 + 0.011*SL	0.31 + 0.012*SL
	t_{PHL}	0.47	0.40 + 0.034*SL	0.42 + 0.025*SL	0.48 + 0.018*SL
	t_R	0.16	0.13 + 0.014*SL	0.11 + 0.024*SL	0.09 + 0.026*SL
	t_F	0.29	0.22 + 0.038*SL	0.23 + 0.033*SL	0.23 + 0.033*SL
UPDATE to DOUT0	t_{PLH}	0.62	0.58 + 0.021*SL	0.59 + 0.016*SL	0.62 + 0.012*SL
	t_{PHL}	0.87	0.80 + 0.034*SL	0.82 + 0.028*SL	0.92 + 0.018*SL
	t_R	0.20	0.15 + 0.025*SL	0.15 + 0.024*SL	0.14 + 0.026*SL
	t_F	0.35	0.27 + 0.041*SL	0.29 + 0.029*SL	0.25 + 0.033*SL
TCK to DOUT0	t_{PLH}	1.42	1.38 + 0.019*SL	1.39 + 0.015*SL	1.42 + 0.012*SL
	t_{PHL}	1.38	1.31 + 0.033*SL	1.33 + 0.024*SL	1.39 + 0.018*SL
	t_R	0.20	0.16 + 0.024*SL	0.15 + 0.025*SL	0.15 + 0.025*SL
	t_F	0.33	0.25 + 0.037*SL	0.27 + 0.031*SL	0.25 + 0.033*SL
ENB to DOUT0	t_{PLH}	1.44	1.40 + 0.018*SL	1.41 + 0.015*SL	1.44 + 0.012*SL
	t_{PHL}	1.39	1.33 + 0.033*SL	1.34 + 0.024*SL	1.40 + 0.018*SL
	t_R	0.20	0.16 + 0.019*SL	0.15 + 0.024*SL	0.14 + 0.026*SL
	t_F	0.33	0.25 + 0.036*SL	0.27 + 0.031*SL	0.25 + 0.033*SL
DINP1 to DOUT1	t_{PLH}	0.31	0.25 + 0.030*SL	0.26 + 0.025*SL	0.28 + 0.024*SL
	t_{PHL}	0.40	0.31 + 0.044*SL	0.32 + 0.041*SL	0.36 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.049*SL	0.09 + 0.052*SL
	t_F	0.27	0.14 + 0.068*SL	0.14 + 0.066*SL	0.11 + 0.069*SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 JTBI1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
MODE1 to DOUT1	t_{PLH}	0.38	0.32 + 0.031*SL	0.33 + 0.025*SL	0.34 + 0.024*SL
	t_{PHL}	0.37	0.28 + 0.044*SL	0.29 + 0.041*SL	0.34 + 0.037*SL
	t_R	0.29	0.05 + 0.120*SL	0.23 + 0.038*SL	0.10 + 0.052*SL
	t_F	0.26	0.13 + 0.066*SL	0.13 + 0.067*SL	0.11 + 0.069*SL
UPDATE to DOUT1	t_{PLH}	0.78	0.68 + 0.048*SL	0.73 + 0.025*SL	0.75 + 0.024*SL
	t_{PHL}	0.71	0.62 + 0.045*SL	0.63 + 0.042*SL	0.68 + 0.037*SL
	t_R	0.22	0.14 + 0.043*SL	0.12 + 0.050*SL	0.10 + 0.052*SL
	t_F	0.27	0.15 + 0.064*SL	0.14 + 0.065*SL	0.11 + 0.069*SL
TCK to DOUT1	t_{PLH}	1.57	1.51 + 0.029*SL	1.52 + 0.024*SL	1.52 + 0.024*SL
	t_{PHL}	1.38	1.29 + 0.044*SL	1.30 + 0.039*SL	1.32 + 0.037*SL
	t_R	0.22	0.13 + 0.048*SL	0.12 + 0.050*SL	0.11 + 0.052*SL
	t_F	0.27	0.14 + 0.064*SL	0.13 + 0.068*SL	0.12 + 0.069*SL
ENB to DOUT1	t_{PLH}	1.58	1.52 + 0.028*SL	1.53 + 0.025*SL	1.54 + 0.024*SL
	t_{PHL}	1.39	1.30 + 0.047*SL	1.32 + 0.039*SL	1.33 + 0.037*SL
	t_R	0.22	0.13 + 0.044*SL	0.12 + 0.049*SL	0.10 + 0.052*SL
	t_F	0.28	0.13 + 0.070*SL	0.14 + 0.066*SL	0.11 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

JTBI1

Bi-directional I/O Scan Cell with Capture, Shift and Update

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 JTBI1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO0	t_{PLH}	1.41	1.33 + 0.040*SL	1.34 + 0.035*SL	1.35 + 0.034*SL
	t_{PHL}	1.19	1.09 + 0.053*SL	1.11 + 0.046*SL	1.11 + 0.046*SL
	t_R	0.30	0.18 + 0.058*SL	0.15 + 0.069*SL	0.14 + 0.070*SL
	t_F	0.31	0.15 + 0.081*SL	0.16 + 0.079*SL	0.12 + 0.085*SL
ENB to TDO0	t_{PLH}	1.39	1.29 + 0.048*SL	1.33 + 0.035*SL	1.34 + 0.034*SL
	t_{PHL}	1.17	1.06 + 0.053*SL	1.08 + 0.046*SL	1.09 + 0.045*SL
	t_R	0.29	0.17 + 0.063*SL	0.15 + 0.069*SL	0.14 + 0.071*SL
	t_F	0.31	0.15 + 0.080*SL	0.15 + 0.080*SL	0.15 + 0.081*SL
TCK to TDO1	t_{PLH}	1.36	1.27 + 0.045*SL	1.31 + 0.035*SL	1.31 + 0.034*SL
	t_{PHL}	1.14	1.04 + 0.052*SL	1.06 + 0.045*SL	1.07 + 0.045*SL
	t_R	0.29	0.17 + 0.061*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.079*SL	0.12 + 0.083*SL
ENB to TDO1	t_{PLH}	1.36	1.28 + 0.038*SL	1.29 + 0.034*SL	1.30 + 0.034*SL
	t_{PHL}	1.12	1.02 + 0.051*SL	1.04 + 0.045*SL	1.05 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.080*SL	0.12 + 0.083*SL
DINP0N to DOUT0	t_{PLH}	0.26	0.22 + 0.020*SL	0.22 + 0.019*SL	0.23 + 0.017*SL
	t_{PHL}	0.31	0.21 + 0.049*SL	0.27 + 0.030*SL	0.31 + 0.025*SL
	t_R	0.22	0.15 + 0.033*SL	0.15 + 0.035*SL	0.17 + 0.031*SL
	t_F	0.26	0.11 + 0.075*SL	0.24 + 0.033*SL	0.19 + 0.039*SL
MODE0 to DOUT0	t_{PLH}	0.37	0.30 + 0.032*SL	0.33 + 0.022*SL	0.35 + 0.020*SL
	t_{PHL}	0.51	0.43 + 0.038*SL	0.46 + 0.029*SL	0.50 + 0.024*SL
	t_R	0.24	0.17 + 0.034*SL	0.16 + 0.035*SL	0.17 + 0.034*SL
	t_F	0.26	0.17 + 0.044*SL	0.18 + 0.041*SL	0.22 + 0.036*SL
UPDATE to DOUT0	t_{PLH}	0.85	0.77 + 0.041*SL	0.83 + 0.023*SL	0.89 + 0.015*SL
	t_{PHL}	1.27	1.18 + 0.047*SL	1.21 + 0.036*SL	1.26 + 0.030*SL
	t_R	0.25	0.18 + 0.036*SL	0.17 + 0.040*SL	0.23 + 0.032*SL
	t_F	0.44	0.35 + 0.048*SL	0.36 + 0.043*SL	0.41 + 0.037*SL
TCK to DOUT0	t_{PLH}	2.13	2.08 + 0.026*SL	2.09 + 0.022*SL	2.11 + 0.019*SL
	t_{PHL}	2.06	1.97 + 0.045*SL	1.99 + 0.036*SL	2.04 + 0.030*SL
	t_R	0.25	0.18 + 0.038*SL	0.18 + 0.036*SL	0.19 + 0.034*SL
	t_F	0.44	0.34 + 0.048*SL	0.36 + 0.042*SL	0.37 + 0.040*SL
ENB to DOUT0	t_{PLH}	2.12	2.07 + 0.026*SL	2.08 + 0.022*SL	2.10 + 0.019*SL
	t_{PHL}	2.04	1.95 + 0.045*SL	1.98 + 0.036*SL	2.02 + 0.030*SL
	t_R	0.25	0.18 + 0.037*SL	0.18 + 0.036*SL	0.15 + 0.040*SL
	t_F	0.44	0.35 + 0.049*SL	0.36 + 0.044*SL	0.40 + 0.038*SL
DINP1 to DOUT1	t_{PLH}	0.41	0.33 + 0.040*SL	0.35 + 0.035*SL	0.38 + 0.031*SL
	t_{PHL}	0.55	0.43 + 0.057*SL	0.46 + 0.049*SL	0.48 + 0.046*SL
	t_R	0.29	0.16 + 0.067*SL	0.14 + 0.073*SL	0.14 + 0.072*SL
	t_F	0.34	0.18 + 0.082*SL	0.19 + 0.080*SL	0.17 + 0.081*SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 JTBI1

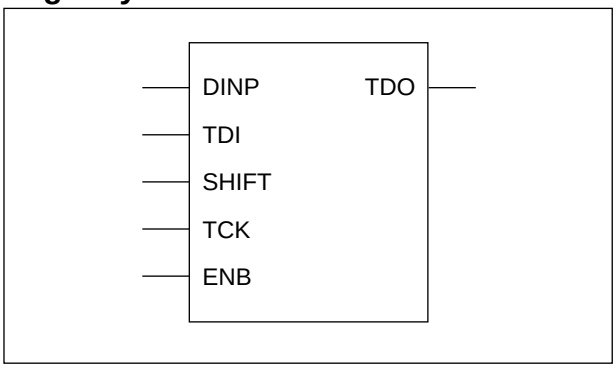
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
MODE1 to DOUT1	t_{PLH}	0.34	0.28 + 0.032*SL	0.25 + 0.041*SL	0.31 + 0.033*SL
	t_{PHL}	0.51	0.40 + 0.054*SL	0.40 + 0.055*SL	0.50 + 0.040*SL
	t_R	0.29	0.15 + 0.071*SL	0.16 + 0.068*SL	0.14 + 0.071*SL
	t_F	0.35	0.17 + 0.085*SL	0.19 + 0.081*SL	0.19 + 0.081*SL
UPDATE to DOUT1	t_{PLH}	1.11	1.02 + 0.042*SL	1.04 + 0.035*SL	1.05 + 0.034*SL
	t_{PHL}	1.02	0.91 + 0.058*SL	0.91 + 0.055*SL	1.01 + 0.041*SL
	t_R	0.30	0.16 + 0.069*SL	0.17 + 0.067*SL	0.14 + 0.070*SL
	t_F	0.36	0.20 + 0.081*SL	0.18 + 0.084*SL	0.23 + 0.077*SL
TCK to DOUT1	t_{PLH}	2.33	2.25 + 0.041*SL	2.26 + 0.035*SL	2.28 + 0.033*SL
	t_{PHL}	2.07	1.95 + 0.062*SL	1.99 + 0.047*SL	2.00 + 0.046*SL
	t_R	0.31	0.16 + 0.074*SL	0.17 + 0.071*SL	0.22 + 0.064*SL
	t_F	0.37	0.20 + 0.085*SL	0.21 + 0.082*SL	0.26 + 0.076*SL
ENB to DOUT1	t_{PLH}	2.32	2.24 + 0.040*SL	2.25 + 0.035*SL	2.25 + 0.034*SL
	t_{PHL}	2.05	1.93 + 0.057*SL	1.96 + 0.050*SL	1.98 + 0.046*SL
	t_R	0.30	0.17 + 0.065*SL	0.16 + 0.070*SL	0.16 + 0.070*SL
	t_F	0.38	0.18 + 0.097*SL	0.24 + 0.078*SL	0.24 + 0.078*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

JTCK

Special Input Scan Cell with Capture and Shift

Logic Symbol



Cell Data

Input Loading (SL)		
	STD80	**STDM80**
DINP	1	1
TDI	1	0
SHIFT	1	1
TCK	1	1
ENB	1	0
Gate Count		
7		

General Description

JTCK is a special input boundary scan cell for clock pad. It has capture and shift capabilities only. JTCK doesn't have update and set capabilities, but has clock enable capability.

Pin Description

Pin name	I/O	Description
DINP	I	Parallel System Data Input
TDI	I	Serial Test Data Input
SHIFT	I	Active High Shift Control Input
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable Input
TDO	O	Serial Test Data Output

Truth Table

DINP	TDI	SHIFT	TCK	ENB	TDO
X	X	X	↑	0	TDOo
0	X	0	↑	1	0
1	X	0	↑	1	1
X	0	1	↑	1	0
X	1	1	↑	1	1
X	X	X	0	X	TDOo
X	X	X	1	X	TDOo
X	X	X	↓	X	TDOo

Timing Requirements

(Typical process, 25°C, 5V, 3.3V)

Parameter	Symbol	Value (ns)	
		STD80	STDM80
Input Setup Time (TDI to TCK)	t_{SU}	0.74	1.07
Input Hold Time (TDI to TCK)	t_{HD}	0.74	0.33
Input Setup Time (TDI to ENB)	t_{SU}	0.74	1.04
Input Hold Time (TDI to ENB)	t_{HD}	0.33	0.33
Input Setup Time (DINP to TCK)	t_{SU}	0.66	0.96
Input Hold Time (DINP to TCK)	t_{HD}	0.33	0.33
Input Setup Time (DINP to ENB)	t_{SU}	0.66	0.93
Input Hold Time (DINP to ENB)	t_{HD}	0.33	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.60	0.79
Input Hold Time (SHIFT to TCK)	t_{HD}	0.33	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.63	0.79
Input Hold Time (SHIFT to ENB)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 JTCK

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.64	0.58 + 0.029*SL	0.59 + 0.024*SL	0.60 + 0.024*SL
	t_{PHL}	0.72	0.64 + 0.041*SL	0.64 + 0.038*SL	0.65 + 0.037*SL
	t_R	0.20	0.11 + 0.046*SL	0.10 + 0.049*SL	0.08 + 0.052*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
ENB to TDO	t_{PLH}	0.64	0.58 + 0.029*SL	0.59 + 0.024*SL	0.60 + 0.024*SL
	t_{PHL}	0.70	0.62 + 0.041*SL	0.62 + 0.038*SL	0.63 + 0.037*SL
	t_R	0.20	0.11 + 0.047*SL	0.10 + 0.052*SL	0.10 + 0.052*SL
	t_F	0.23	0.10 + 0.064*SL	0.10 + 0.067*SL	0.07 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 JTCK

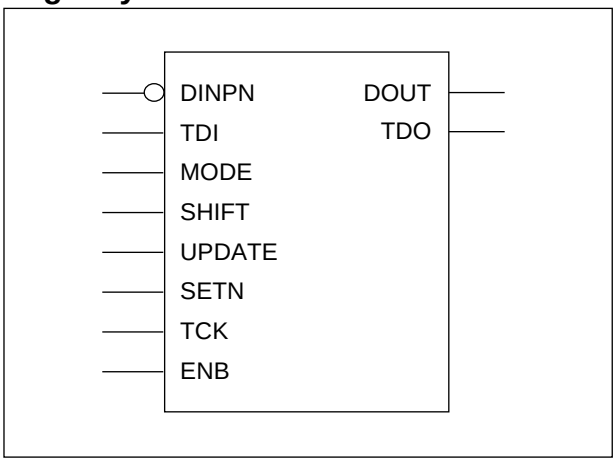
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.90	0.83 + 0.038*SL	0.81 + 0.043*SL	0.88 + 0.033*SL
	t_{PHL}	1.04	0.94 + 0.051*SL	0.96 + 0.045*SL	0.96 + 0.045*SL
	t_R	0.28	0.15 + 0.067*SL	0.11 + 0.079*SL	0.18 + 0.069*SL
	t_F	0.30	0.15 + 0.078*SL	0.15 + 0.078*SL	0.11 + 0.084*SL
ENB to TDO	t_{PLH}	0.91	0.84 + 0.037*SL	0.84 + 0.035*SL	0.83 + 0.037*SL
	t_{PHL}	1.05	0.95 + 0.051*SL	0.97 + 0.045*SL	0.98 + 0.044*SL
	t_R	0.28	0.15 + 0.065*SL	0.15 + 0.068*SL	0.12 + 0.072*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.082*SL	0.16 + 0.079*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

JTIN1

Input Scan Cell with Capture, Shift, Update and Set

Logic Symbol



Cell Data

Input Loading (SL)		
	STD80	**STDM80**
DINPN	1	4
TDI	0	1
MODE	1	1
SHIFT	1	1
UPDATE	1	1
SETN	0	0
TCK	1	1
ENB	0	0
Gate Count		
13		

Pin Description

Pin name	I/O	Description
DINPN	I	Parallel Data Input Active Low
TDI	I	Serial Test Data Input
MODE	I	Mode Select Input—Low for Data Input and High for Internal Register Data Value
SHIFT	I	Active High Shift Control Input
UPDATE	I	Update Latch Input—Low for Update
SETN	I	Active Low Set Input
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable Input
DOUT	O	Parallel Data Output
TDO	O	Serial Test Data Output

Truth Table

DINPN	TDI	MODE	SHIFT	UPDATE	TCK	ENB	OUTPUT
							DOUT
0	X	0	X	X	X	X	1
1	X	0	X	X	X	X	0
X	X	1	X	X	X	X	LatchQ
							TDO
X	X	X	X	X	↑	0	TDOo
0	X	0	0	X	↑	1	1
1	X	0	0	X	↑	1	0
X	X	1	0	X	↑	1	LatchQ
X	0	X	1	X	↑	1	0
X	1	X	1	X	↑	1	1
X	X	X	X	X	0	X	TDOo
X	X	X	X	X	1	X	TDOo
X	X	X	X	X	↓	X	TDOo
							LatchQ
X	X	X	X	0	X	X	0
X	X	X	X	1	0	X	TDO
X	X	X	X	1	1	X	LatchQo

NOTE: Outputs are defined in separate truth tables. In addition, an internal state known as “LatchQ” is defined as the output of the latch in the logic diagram.

Timing Requirements

(Typical process, 25°C, 5V, 3.3V)

Parameter	Symbol	Value (ns)	
		STD80	STDM80
Input Setup Time (TDI to TCK)	t_{SU}	0.52	0.66
Input Hold Time (TDI to TCK)	t_{HD}	0.33	0.33
Input Setup Time (TDI to ENB)	t_{SU}	0.52	0.66
Input Hold Time (TDI to ENB)	t_{HD}	0.33	0.33
Input Setup Time (DINPN to TCK)	t_{SU}	0.82	1.12
Input Hold Time (DINPN to TCK)	t_{HD}	0.33	0.33
Input Setup Time (DINPN to ENB)	t_{SU}	0.82	1.12
Input Hold Time (DINPN to ENB)	t_{HD}	0.33	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.60	0.79
Input Hold Time (SHIFT to TCK)	t_{HD}	0.33	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.63	0.79
Input Hold Time (SHIFT to ENB)	t_{HD}	0.33	0.33
Input Setup Time (MODE to TCK)	t_{SU}	0.87	1.20
Input Hold Time (MODE to TCK)	t_{HD}	0.33	0.33
Input Setup Time (MODE to ENB)	t_{SU}	0.87	1.20
Input Hold Time (MODE to ENB)	t_{HD}	0.33	0.33
Input Hold Time (SETN to UPDATE)	t_{HD}		0.33
Recovery Time (SETN)	t_{RC}	0.33	0.49

JTIN1

Input Scan Cell with Capture, Shift, Update and Set

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 JTIN1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.64	0.59 + 0.023*SL	0.59 + 0.025*SL	0.60 + 0.024*SL
	t_{PHL}	0.72	0.64 + 0.041*SL	0.64 + 0.038*SL	0.65 + 0.037*SL
	t_R	0.20	0.11 + 0.048*SL	0.11 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
ENB to TDO	t_{PLH}	0.66	0.60 + 0.029*SL	0.61 + 0.024*SL	0.62 + 0.024*SL
	t_{PHL}	0.72	0.63 + 0.042*SL	0.64 + 0.038*SL	0.65 + 0.037*SL
	t_R	0.20	0.11 + 0.046*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.10 + 0.068*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
DINPN to DOUT	t_{PLH}	0.18	0.14 + 0.021*SL	0.14 + 0.018*SL	0.33 + -0.001*SL
	t_{PHL}	0.25	0.20 + 0.023*SL	0.20 + 0.021*SL	0.43 + -0.002*SL
	t_R	0.23	0.19 + 0.019*SL	0.19 + 0.021*SL	0.41 + -0.002*SL
	t_F	0.27	0.20 + 0.034*SL	0.22 + 0.028*SL	0.51 + -0.002*SL
MODE to DOUT	t_{PLH}	0.33	0.29 + 0.018*SL	0.30 + 0.013*SL	0.44 + -0.001*SL
	t_{PHL}	0.40	0.34 + 0.026*SL	0.35 + 0.021*SL	0.58 + -0.002*SL
	t_R	0.16	0.13 + 0.017*SL	0.11 + 0.025*SL	0.38 + -0.002*SL
	t_F	0.19	0.12 + 0.034*SL	0.13 + 0.032*SL	0.47 + -0.003*SL
UPDATE to DOUT	t_{PLH}	0.77	0.75 + 0.011*SL	0.74 + 0.015*SL	0.90 + -0.001*SL
	t_{PHL}	0.82	0.75 + 0.039*SL	0.78 + 0.022*SL	1.01 + -0.002*SL
	t_R	0.19	0.15 + 0.024*SL	0.14 + 0.025*SL	0.41 + -0.002*SL
	t_F	0.26	0.19 + 0.034*SL	0.20 + 0.032*SL	0.54 + -0.003*SL
SETN to DOUT	t_{PLH}	0.57	0.53 + 0.021*SL	0.55 + 0.015*SL	0.70 + -0.001*SL
	t_{PHL}	0.61	0.56 + 0.029*SL	0.57 + 0.023*SL	0.81 + -0.002*SL
	t_R	0.20	0.14 + 0.028*SL	0.15 + 0.026*SL	0.43 + -0.002*SL
	t_F	0.26	0.19 + 0.035*SL	0.20 + 0.031*SL	0.53 + -0.003*SL
TCK to DOUT	t_{PLH}	1.34	1.31 + 0.013*SL	1.31 + 0.016*SL	1.48 + -0.001*SL
	t_{PHL}	1.41	1.35 + 0.029*SL	1.37 + 0.023*SL	1.61 + -0.002*SL
	t_R	0.20	0.15 + 0.024*SL	0.15 + 0.024*SL	0.41 + -0.002*SL
	t_F	0.26	0.18 + 0.039*SL	0.20 + 0.032*SL	0.54 + -0.003*SL
ENB to DOUT	t_{PLH}	1.36	1.32 + 0.019*SL	1.33 + 0.015*SL	1.49 + -0.001*SL
	t_{PHL}	1.41	1.35 + 0.027*SL	1.36 + 0.023*SL	1.61 + -0.002*SL
	t_R	0.19	0.14 + 0.025*SL	0.15 + 0.024*SL	0.40 + -0.002*SL
	t_F	0.27	0.18 + 0.043*SL	0.21 + 0.030*SL	0.53 + -0.003*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 JTIN1

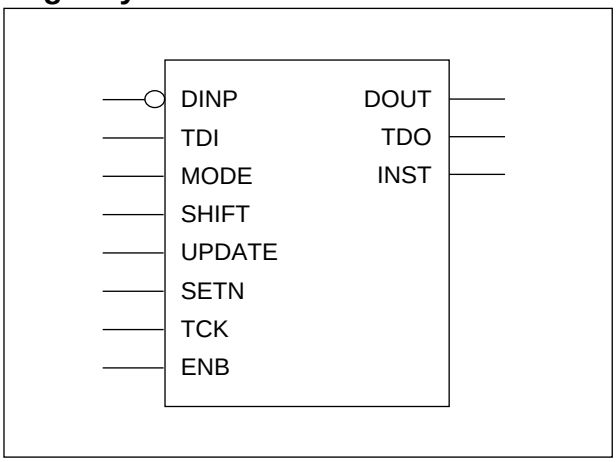
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.90	0.82 + 0.038*SL	0.83 + 0.035*SL	0.84 + 0.034*SL
	t_{PHL}	1.03	0.93 + 0.051*SL	0.95 + 0.046*SL	0.96 + 0.044*SL
	t_R	0.29	0.16 + 0.063*SL	0.15 + 0.068*SL	0.13 + 0.071*SL
	t_F	0.30	0.14 + 0.081*SL	0.14 + 0.080*SL	0.13 + 0.081*SL
ENB to TDO	t_{PLH}	0.94	0.85 + 0.045*SL	0.89 + 0.031*SL	0.87 + 0.033*SL
	t_{PHL}	1.00	0.90 + 0.051*SL	0.92 + 0.046*SL	0.92 + 0.045*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.068*SL	0.12 + 0.071*SL
	t_F	0.30	0.14 + 0.081*SL	0.15 + 0.079*SL	0.13 + 0.081*SL
DINPN to DOUT	t_{PLH}	0.26	0.21 + 0.022*SL	0.22 + 0.018*SL	0.52 + -0.023*SL
	t_{PHL}	0.33	0.26 + 0.033*SL	0.28 + 0.027*SL	0.76 + -0.041*SL
	t_R	0.22	0.14 + 0.037*SL	0.15 + 0.036*SL	0.77 + -0.052*SL
	t_F	0.29	0.19 + 0.052*SL	0.23 + 0.040*SL	0.95 + -0.063*SL
MODE to DOUT	t_{PLH}	0.45	0.41 + 0.023*SL	0.42 + 0.019*SL	0.77 + -0.030*SL
	t_{PHL}	0.53	0.46 + 0.035*SL	0.48 + 0.029*SL	1.01 + -0.046*SL
	t_R	0.20	0.13 + 0.033*SL	0.12 + 0.036*SL	0.71 + -0.048*SL
	t_F	0.26	0.18 + 0.042*SL	0.19 + 0.038*SL	0.86 + -0.057*SL
UPDATE to DOUT	t_{PLH}	1.09	1.01 + 0.038*SL	1.06 + 0.022*SL	1.50 + -0.040*SL
	t_{PHL}	1.18	1.10 + 0.040*SL	1.12 + 0.033*SL	1.71 + -0.052*SL
	t_R	0.25	0.19 + 0.029*SL	0.17 + 0.036*SL	0.76 + -0.048*SL
	t_F	0.35	0.25 + 0.052*SL	0.27 + 0.043*SL	1.04 + -0.066*SL
SETN to DOUT	t_{PLH}	0.76	0.71 + 0.027*SL	0.72 + 0.023*SL	1.14 + -0.036*SL
	t_{PHL}	0.84	0.76 + 0.040*SL	0.78 + 0.033*SL	1.38 + -0.052*SL
	t_R	0.25	0.17 + 0.039*SL	0.17 + 0.037*SL	0.80 + -0.053*SL
	t_F	0.35	0.26 + 0.047*SL	0.26 + 0.047*SL	1.06 + -0.067*SL
TCK to DOUT	t_{PLH}	1.93	1.88 + 0.024*SL	1.89 + 0.023*SL	2.30 + -0.037*SL
	t_{PHL}	2.11	2.03 + 0.039*SL	2.05 + 0.032*SL	2.65 + -0.052*SL
	t_R	0.24	0.17 + 0.034*SL	0.17 + 0.036*SL	0.78 + -0.051*SL
	t_F	0.34	0.25 + 0.049*SL	0.27 + 0.041*SL	0.99 + -0.061*SL
ENB to DOUT	t_{PLH}	1.97	1.90 + 0.032*SL	1.95 + 0.019*SL	2.33 + -0.036*SL
	t_{PHL}	2.08	2.00 + 0.040*SL	2.02 + 0.032*SL	2.63 + -0.055*SL
	t_R	0.24	0.17 + 0.036*SL	0.16 + 0.038*SL	0.80 + -0.052*SL
	t_F	0.35	0.25 + 0.048*SL	0.27 + 0.041*SL	1.00 + -0.061*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 7, *Group3 : 7 < SL

JTINT1

Tri-State I/O Control Scan Cell with Capture, Shift, Update and Set

Logic Symbol



Cell Data

Input Loading (SL)		
	STD80	**STDM80**
DINP	3	3
TDI	0	1
MODE	1	1
SHIFT	1	1
UPDATE	1	1
SETN	0	0
TCK	1	1
ENB	0	0
Gate Count		
13		

Pin Description

Pin name	I/O	Description
DINP	I	Parallel Data Input Active Low
TDI	I	Serial Test Data Input
MODE	I	Mode Select Input—Low for Data Input and High for Internal Register Data Value
SHIFT	I	Active High Shift Control Input
UPDATE	I	Update Latch Input—Low for Update
SETN	I	Active Low Set Input
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable Input
DOUT	O	Parallel Data Output
TDO	O	Serial Test Data Output
INST	O	Updated Instruction Output

Truth Table

DINP	TDI	MODE	SHIFT	UPDATE	SETN	TCK	ENB	OUTPUT
								DOUT
0	X	0	X	X	X	X	X	0
1	X	0	X	X	X	X	X	1
X	X	1	X	X	X	X	X	INST
								TDO
X	X	X	X	X	X	↗	0	TDOo
0	X	X	0	X	X	↗	1	0
1	X	X	0	X	X	↗	1	1
X	0	X	1	X	X	↗	1	0
X	1	X	1	X	X	↗	1	1
X	X	X	X	X	X	0	X	TDOo
X	X	X	X	X	X	1	X	TDOo
X	X	X	X	X	X	↘	X	TDOo
								INST
X	X	X	X	X	0	X	X	1
X	X	X	X	0	1	X	X	TDO
X	X	X	X	1	1	X	X	INSTo

NOTE: Outputs are defined in separate truth tables.

Timing Requirements

(Typical process, 25°C, 5V, 3.3V)

Parameter	Symbol	Value (ns)	
		STD80	STDM80
Input Setup Time (TDI to TCK)	t_{SU}	0.52	0.66
Input Hold Time (TDI to TCK)	t_{HD}	0.33	0.33
Input Setup Time (TDI to ENB)	t_{SU}	0.52	0.66
Input Hold Time (TDI to ENB)	t_{HD}	0.33	0.33
Input Setup Time (DINPN to TCK)	t_{SU}	0.52	0.66
Input Hold Time (DINPN to TCK)	t_{HD}	0.33	0.33
Input Setup Time (DINPN to ENB)	t_{SU}	0.52	0.66
Input Hold Time (DINPN to ENB)	t_{HD}	0.33	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.60	0.79
Input Hold Time (SHIFT to TCK)	t_{HD}	0.33	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.63	0.79
Input Hold Time (SHIFT to ENB)	t_{HD}	0.33	0.33
Input Hold Time (SETN to UPDATE)	t_{HD}		0.33
Recovery Time (SETN)	t_{RC}	0.33	0.49

JTINT1

Tri-State I/O Control Scan Cell with Capture, Shift, Update and Set

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 JTINT1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.64	0.58 + 0.031*SL	0.60 + 0.024*SL	0.59 + 0.024*SL
	t_{PHL}	0.72	0.63 + 0.044*SL	0.65 + 0.038*SL	0.65 + 0.037*SL
	t_R	0.20	0.12 + 0.040*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.10 + 0.066*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
ENB to TDO	t_{PLH}	0.66	0.56 + 0.052*SL	0.63 + 0.020*SL	0.59 + 0.024*SL
	t_{PHL}	0.74	0.61 + 0.062*SL	0.67 + 0.035*SL	0.65 + 0.037*SL
	t_R	0.20	0.12 + 0.038*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.10 + 0.068*SL	0.10 + 0.067*SL	0.07 + 0.069*SL
DINP to DOUT	t_{PLH}	0.32	0.28 + 0.018*SL	0.29 + 0.015*SL	0.32 + 0.012*SL
	t_{PHL}	0.41	0.35 + 0.026*SL	0.37 + 0.021*SL	0.39 + 0.018*SL
	t_R	0.19	0.14 + 0.029*SL	0.15 + 0.022*SL	0.12 + 0.026*SL
	t_F	0.22	0.15 + 0.033*SL	0.15 + 0.032*SL	0.14 + 0.034*SL
MODE to DOUT	t_{PLH}	0.36	0.32 + 0.023*SL	0.34 + 0.015*SL	0.36 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.028*SL	0.32 + 0.022*SL	0.36 + 0.018*SL
	t_R	0.20	0.15 + 0.023*SL	0.16 + 0.022*SL	0.12 + 0.026*SL
	t_F	0.21	0.14 + 0.033*SL	0.14 + 0.032*SL	0.13 + 0.034*SL
UPDATE to DOUT	t_{PLH}	0.79	0.75 + 0.021*SL	0.77 + 0.012*SL	0.77 + 0.012*SL
	t_{PHL}	0.80	0.77 + 0.015*SL	0.75 + 0.023*SL	0.80 + 0.018*SL
	t_R	0.19	0.14 + 0.027*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.22	0.16 + 0.034*SL	0.16 + 0.031*SL	0.14 + 0.033*SL
SETN to DOUT	t_{PLH}	0.55	0.51 + 0.021*SL	0.52 + 0.016*SL	0.56 + 0.012*SL
	t_{PHL}	0.59	0.54 + 0.029*SL	0.55 + 0.022*SL	0.59 + 0.018*SL
	t_R	0.19	0.14 + 0.026*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.22	0.16 + 0.034*SL	0.16 + 0.033*SL	0.15 + 0.033*SL
TCK to DOUT	t_{PLH}	1.35	1.31 + 0.020*SL	1.32 + 0.014*SL	1.34 + 0.012*SL
	t_{PHL}	1.39	1.34 + 0.025*SL	1.35 + 0.021*SL	1.38 + 0.018*SL
	t_R	0.19	0.16 + 0.017*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.22	0.16 + 0.034*SL	0.16 + 0.032*SL	0.15 + 0.033*SL
ENB to DOUT	t_{PLH}	1.35	1.31 + 0.018*SL	1.32 + 0.014*SL	1.35 + 0.012*SL
	t_{PHL}	1.41	1.36 + 0.026*SL	1.37 + 0.021*SL	1.40 + 0.018*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.22	0.16 + 0.033*SL	0.16 + 0.033*SL	0.15 + 0.033*SL
UPDATE to INST	t_{PLH}	0.69	0.64 + 0.026*SL	0.65 + 0.021*SL	0.62 + 0.024*SL
	t_{PHL}	0.70	0.62 + 0.040*SL	0.63 + 0.036*SL	0.62 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.09 + 0.050*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.063*SL	0.09 + 0.068*SL	0.09 + 0.069*SL
SETN to INST	t_{PLH}	0.48	0.42 + 0.027*SL	0.43 + 0.024*SL	0.43 + 0.024*SL
	t_{PHL}	0.48	0.40 + 0.040*SL	0.41 + 0.038*SL	0.42 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.11 + 0.060*SL	0.09 + 0.068*SL	0.09 + 0.069*SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 JTINT1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to INST	t_{PLH}	1.26	1.20 + 0.028*SL	1.21 + 0.023*SL	1.20 + 0.024*SL
	t_{PHL}	1.29	1.21 + 0.042*SL	1.22 + 0.038*SL	1.23 + 0.037*SL
	t_R	0.20	0.11 + 0.044*SL	0.10 + 0.050*SL	0.08 + 0.052*SL
	t_F	0.23	0.11 + 0.060*SL	0.10 + 0.068*SL	0.08 + 0.069*SL
ENB to INST	t_{PLH}	1.27	1.18 + 0.047*SL	1.24 + 0.020*SL	1.20 + 0.024*SL
	t_{PHL}	1.31	1.18 + 0.063*SL	1.24 + 0.038*SL	1.25 + 0.037*SL
	t_R	0.20	0.11 + 0.045*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.24	0.10 + 0.067*SL	0.10 + 0.068*SL	0.09 + 0.069*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 JTINT1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.93	0.83 + 0.048*SL	0.87 + 0.034*SL	0.87 + 0.034*SL
	t_{PHL}	1.04	0.93 + 0.051*SL	0.95 + 0.046*SL	0.96 + 0.044*SL
	t_R	0.28	0.16 + 0.063*SL	0.14 + 0.069*SL	0.12 + 0.071*SL
	t_F	0.30	0.14 + 0.080*SL	0.14 + 0.081*SL	0.13 + 0.082*SL
ENB to TDO	t_{PLH}	0.95	0.87 + 0.037*SL	0.88 + 0.035*SL	0.95 + 0.025*SL
	t_{PHL}	1.05	0.95 + 0.051*SL	0.96 + 0.046*SL	1.00 + 0.041*SL
	t_R	0.28	0.14 + 0.069*SL	0.14 + 0.069*SL	0.13 + 0.071*SL
	t_F	0.31	0.16 + 0.075*SL	0.15 + 0.079*SL	0.12 + 0.082*SL
DINP to DOUT	t_{PLH}	0.41	0.37 + 0.020*SL	0.37 + 0.021*SL	0.37 + 0.021*SL
	t_{PHL}	0.55	0.48 + 0.035*SL	0.50 + 0.029*SL	0.53 + 0.025*SL
	t_R	0.23	0.16 + 0.037*SL	0.16 + 0.035*SL	0.17 + 0.033*SL
	t_F	0.28	0.20 + 0.042*SL	0.20 + 0.041*SL	0.23 + 0.037*SL
MODE to DOUT	t_{PLH}	0.51	0.46 + 0.027*SL	0.49 + 0.016*SL	0.45 + 0.023*SL
	t_{PHL}	0.51	0.43 + 0.036*SL	0.45 + 0.030*SL	0.45 + 0.030*SL
	t_R	0.25	0.20 + 0.024*SL	0.16 + 0.036*SL	0.18 + 0.033*SL
	t_F	0.29	0.20 + 0.045*SL	0.23 + 0.038*SL	0.21 + 0.040*SL
UPDATE to DOUT	t_{PLH}	1.10	1.03 + 0.037*SL	1.09 + 0.017*SL	1.07 + 0.019*SL
	t_{PHL}	1.16	1.11 + 0.027*SL	1.10 + 0.030*SL	1.12 + 0.026*SL
	t_R	0.24	0.17 + 0.035*SL	0.16 + 0.037*SL	0.19 + 0.034*SL
	t_F	0.30	0.21 + 0.045*SL	0.23 + 0.039*SL	0.20 + 0.043*SL
SETN to DOUT	t_{PLH}	0.79	0.74 + 0.028*SL	0.76 + 0.022*SL	0.77 + 0.020*SL
	t_{PHL}	0.84	0.77 + 0.037*SL	0.79 + 0.031*SL	0.83 + 0.025*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.035*SL	0.19 + 0.032*SL
	t_F	0.30	0.21 + 0.043*SL	0.21 + 0.044*SL	0.23 + 0.040*SL
TCK to DOUT	t_{PLH}	1.95	1.90 + 0.024*SL	1.91 + 0.022*SL	1.93 + 0.019*SL
	t_{PHL}	2.06	1.98 + 0.037*SL	2.00 + 0.030*SL	2.03 + 0.025*SL
	t_R	0.24	0.17 + 0.035*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_F	0.30	0.21 + 0.046*SL	0.22 + 0.041*SL	0.20 + 0.045*SL
ENB to DOUT	t_{PLH}	1.99	1.93 + 0.032*SL	1.97 + 0.018*SL	1.97 + 0.018*SL
	t_{PHL}	2.10	2.03 + 0.036*SL	2.05 + 0.029*SL	2.06 + 0.027*SL
	t_R	0.24	0.17 + 0.037*SL	0.13 + 0.048*SL	0.29 + 0.025*SL
	t_F	0.30	0.21 + 0.044*SL	0.21 + 0.045*SL	0.26 + 0.038*SL
UPDATE to INST	t_{PLH}	0.96	0.86 + 0.048*SL	0.90 + 0.035*SL	0.94 + 0.029*SL
	t_{PHL}	0.98	0.86 + 0.060*SL	0.92 + 0.042*SL	0.91 + 0.044*SL
	t_R	0.27	0.14 + 0.066*SL	0.13 + 0.069*SL	0.08 + 0.077*SL
	t_F	0.31	0.15 + 0.081*SL	0.15 + 0.079*SL	0.13 + 0.082*SL
SETN to INST	t_{PLH}	0.65	0.58 + 0.038*SL	0.59 + 0.034*SL	0.59 + 0.033*SL
	t_{PHL}	0.65	0.55 + 0.050*SL	0.59 + 0.037*SL	0.48 + 0.052*SL
	t_R	0.28	0.14 + 0.074*SL	0.16 + 0.067*SL	0.11 + 0.074*SL
	t_F	0.33	0.14 + 0.095*SL	0.21 + 0.074*SL	0.15 + 0.082*SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 JTINT1

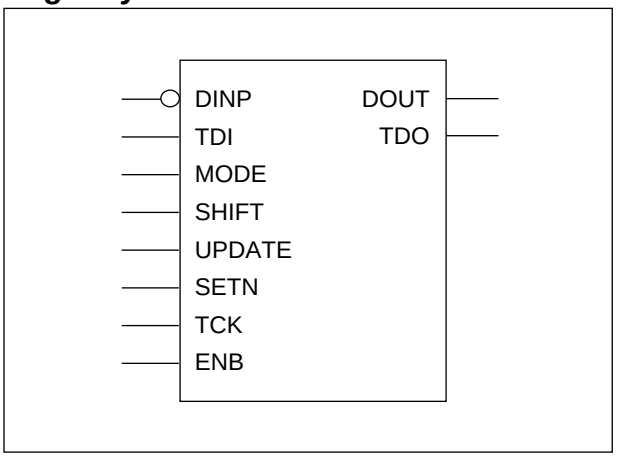
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to INST	t_{PLH}	1.83	1.74 + 0.045*SL	1.78 + 0.034*SL	1.77 + 0.035*SL
	t_{PHL}	1.89	1.76 + 0.066*SL	1.82 + 0.044*SL	1.82 + 0.044*SL
	t_R	0.28	0.14 + 0.067*SL	0.13 + 0.071*SL	0.11 + 0.074*SL
	t_F	0.31	0.14 + 0.084*SL	0.16 + 0.077*SL	0.12 + 0.083*SL
ENB to INST	t_{PLH}	1.86	1.79 + 0.035*SL	1.79 + 0.033*SL	1.84 + 0.027*SL
	t_{PHL}	1.92	1.82 + 0.050*SL	1.83 + 0.046*SL	1.84 + 0.045*SL
	t_R	0.28	0.14 + 0.069*SL	0.14 + 0.070*SL	0.10 + 0.075*SL
	t_F	0.31	0.15 + 0.077*SL	0.13 + 0.084*SL	0.17 + 0.079*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

JTOUT1

Output Scan Cell with Capture, Shift, Update and Set

Logic Symbol



Cell Data

Input Loading (SL)		
	STD80	**STDM80**
DINP	3	3
TDI	0	1
MODE	1	1
SHIFT	1	1
UPDATE	1	1
SETN	0	0
TCK	1	1
ENB	0	0
Gate Count		
12		

Pin Description

Pin name	I/O	Description
DINP	I	Parallel Data Input Active Low
TDI	I	Serial Test Data Input
MODE	I	Mode Select Input—Low for Data Input and High for Internal Register Data Value
SHIFT	I	Active High Shift Control Input
UPDATE	I	Update Latch Input—Low for Update
SETN	I	Active Low Set Input
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable Input
DOUT	O	Parallel Data Output
TDO	O	Serial Test Data Output

Truth Table

DINP	TDI	MODE	SHIFT	UPDATE	SETN	TCK	ENB	OUTPUT
								DOUT
0	X	0	X	X	X	X	X	0
1	X	0	X	X	X	X	X	1
X	X	1	X	X	X	X	X	LatchQ
								TDO
X	X	X	X	X	X	↑	0	TDOo
0	X	X	0	X	X	↑	1	0
1	X	X	0	X	X	↑	1	1
X	0	X	1	X	X	↑	1	0
X	1	X	1	X	X	↑	1	1
X	X	X	X	X	X	0	X	TDOo
X	X	X	X	X	X	1	X	TDOo
X	X	X	X	X	X	↓	X	TDOo
								LatchQ
X	X	X	X	X	0	X	X	1
X	X	X	X	0	1	X	X	TDO
X	X	X	X	1	1	X	X	LatchQo

NOTE: Outputs are defined in separate truth tables. In addition, an internal state known as “LatchQ” is defined as the output of the latch in the logic diagram.

Timing Requirements

(Typical process, 25°C, 5V, 3.3V)

Parameter	Symbol	Value (ns)	
		STD80	STDM80
Input Setup Time (TDI to TCK)	t_{SU}	0.52	0.66
Input Hold Time (TDI to TCK)	t_{HD}	0.33	0.33
Input Setup Time (TDI to ENB)	t_{SU}	0.52	0.66
Input Hold Time (TDI to ENB)	t_{HD}	0.33	0.33
Input Setup Time (DINP to TCK)	t_{SU}	0.52	0.66
Input Hold Time (DINP to TCK)	t_{HD}	0.33	0.33
Input Setup Time (DINP to ENB)	t_{SU}	0.52	0.66
Input Hold Time (DINP to ENB)	t_{HD}	0.33	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.60	0.79
Input Hold Time (SHIFT to TCK)	t_{HD}	0.33	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.63	0.79
Input Hold Time (SHIFT to ENB)	t_{HD}	0.33	0.33
Input Hold Time (SETN to UPDATE)	t_{HD}		0.33
Recovery Time (SETN)	t_{RC}	0.33	0.49

JTOUT1

Output Scan Cell with Capture, Shift, Update and Set

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.44ns, SL: Standard Load)

STD80 JTOUT1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.64	0.58 + 0.028*SL	0.59 + 0.025*SL	0.59 + 0.024*SL
	t_{PHL}	0.71	0.63 + 0.041*SL	0.64 + 0.038*SL	0.65 + 0.037*SL
	t_R	0.20	0.11 + 0.043*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.23	0.10 + 0.067*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
ENB to TDO	t_{PLH}	0.64	0.58 + 0.028*SL	0.59 + 0.024*SL	0.59 + 0.024*SL
	t_{PHL}	0.71	0.63 + 0.040*SL	0.64 + 0.037*SL	0.64 + 0.037*SL
	t_R	0.20	0.12 + 0.039*SL	0.10 + 0.049*SL	0.07 + 0.052*SL
	t_F	0.24	0.10 + 0.067*SL	0.10 + 0.067*SL	0.08 + 0.069*SL
DINP to DOUT	t_{PLH}	0.32	0.28 + 0.018*SL	0.29 + 0.015*SL	0.32 + 0.012*SL
	t_{PHL}	0.41	0.35 + 0.026*SL	0.37 + 0.021*SL	0.39 + 0.018*SL
	t_R	0.19	0.14 + 0.029*SL	0.15 + 0.022*SL	0.12 + 0.026*SL
	t_F	0.22	0.15 + 0.033*SL	0.15 + 0.032*SL	0.14 + 0.034*SL
MODE to DOUT	t_{PLH}	0.36	0.32 + 0.023*SL	0.34 + 0.015*SL	0.36 + 0.012*SL
	t_{PHL}	0.36	0.31 + 0.028*SL	0.32 + 0.022*SL	0.36 + 0.018*SL
	t_R	0.20	0.15 + 0.023*SL	0.16 + 0.022*SL	0.12 + 0.026*SL
	t_F	0.21	0.14 + 0.033*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
UPDATE to DOUT	t_{PLH}	0.77	0.71 + 0.030*SL	0.74 + 0.014*SL	0.76 + 0.012*SL
	t_{PHL}	0.76	0.73 + 0.019*SL	0.72 + 0.023*SL	0.77 + 0.018*SL
	t_R	0.20	0.15 + 0.027*SL	0.16 + 0.023*SL	0.13 + 0.026*SL
	t_F	0.23	0.16 + 0.034*SL	0.16 + 0.032*SL	0.15 + 0.033*SL
SETN to DOUT	t_{PLH}	0.54	0.50 + 0.021*SL	0.51 + 0.016*SL	0.55 + 0.012*SL
	t_{PHL}	0.58	0.50 + 0.039*SL	0.54 + 0.022*SL	0.58 + 0.018*SL
	t_R	0.19	0.14 + 0.026*SL	0.15 + 0.023*SL	0.12 + 0.026*SL
	t_F	0.23	0.16 + 0.038*SL	0.17 + 0.031*SL	0.15 + 0.033*SL
TCK to DOUT	t_{PLH}	1.33	1.29 + 0.019*SL	1.30 + 0.015*SL	1.33 + 0.012*SL
	t_{PHL}	1.37	1.32 + 0.028*SL	1.33 + 0.021*SL	1.36 + 0.018*SL
	t_R	0.19	0.16 + 0.018*SL	0.14 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.23	0.16 + 0.034*SL	0.17 + 0.032*SL	0.15 + 0.033*SL
ENB to DOUT	t_{PLH}	1.33	1.29 + 0.018*SL	1.30 + 0.015*SL	1.33 + 0.012*SL
	t_{PHL}	1.37	1.32 + 0.026*SL	1.33 + 0.021*SL	1.36 + 0.018*SL
	t_R	0.19	0.15 + 0.021*SL	0.14 + 0.024*SL	0.13 + 0.026*SL
	t_F	0.22	0.16 + 0.032*SL	0.16 + 0.032*SL	0.15 + 0.033*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.39ns, SL: Standard Load)

STDM80 JTOUT1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.90	0.82 + 0.038*SL	0.83 + 0.035*SL	0.84 + 0.034*SL
	t_{PHL}	1.01	0.90 + 0.051*SL	0.92 + 0.046*SL	0.93 + 0.044*SL
	t_R	0.29	0.16 + 0.063*SL	0.15 + 0.068*SL	0.13 + 0.071*SL
	t_F	0.31	0.16 + 0.076*SL	0.15 + 0.079*SL	0.10 + 0.085*SL
ENB to TDO	t_{PLH}	0.93	0.86 + 0.038*SL	0.87 + 0.035*SL	0.87 + 0.033*SL
	t_{PHL}	1.05	0.95 + 0.051*SL	0.96 + 0.046*SL	0.97 + 0.044*SL
	t_R	0.28	0.15 + 0.066*SL	0.14 + 0.068*SL	0.12 + 0.072*SL
	t_F	0.31	0.16 + 0.075*SL	0.15 + 0.079*SL	0.12 + 0.082*SL
DINP to DOUT	t_{PLH}	0.41	0.37 + 0.020*SL	0.37 + 0.021*SL	0.37 + 0.021*SL
	t_{PHL}	0.55	0.48 + 0.035*SL	0.50 + 0.029*SL	0.53 + 0.025*SL
	t_R	0.23	0.16 + 0.037*SL	0.16 + 0.035*SL	0.17 + 0.033*SL
	t_F	0.28	0.20 + 0.042*SL	0.20 + 0.041*SL	0.23 + 0.037*SL
MODE to DOUT	t_{PLH}	0.49	0.42 + 0.032*SL	0.44 + 0.026*SL	0.49 + 0.019*SL
	t_{PHL}	0.51	0.43 + 0.036*SL	0.44 + 0.035*SL	0.50 + 0.026*SL
	t_R	0.26	0.22 + 0.021*SL	0.19 + 0.031*SL	0.17 + 0.034*SL
	t_F	0.29	0.20 + 0.045*SL	0.22 + 0.038*SL	0.21 + 0.040*SL
UPDATE to DOUT	t_{PLH}	1.07	1.04 + 0.017*SL	1.03 + 0.022*SL	1.04 + 0.020*SL
	t_{PHL}	1.13	1.04 + 0.044*SL	1.09 + 0.029*SL	1.12 + 0.024*SL
	t_R	0.24	0.17 + 0.033*SL	0.17 + 0.034*SL	0.16 + 0.035*SL
	t_F	0.30	0.21 + 0.042*SL	0.20 + 0.045*SL	0.27 + 0.036*SL
SETN to DOUT	t_{PLH}	0.75	0.70 + 0.027*SL	0.71 + 0.023*SL	0.71 + 0.023*SL
	t_{PHL}	0.83	0.76 + 0.035*SL	0.77 + 0.032*SL	0.82 + 0.024*SL
	t_R	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.15 + 0.037*SL
	t_F	0.30	0.20 + 0.049*SL	0.22 + 0.043*SL	0.25 + 0.039*SL
TCK to DOUT	t_{PLH}	1.92	1.87 + 0.024*SL	1.88 + 0.022*SL	1.90 + 0.019*SL
	t_{PHL}	2.02	1.94 + 0.041*SL	1.98 + 0.028*SL	1.98 + 0.028*SL
	t_R	0.24	0.18 + 0.029*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_F	0.30	0.21 + 0.043*SL	0.22 + 0.041*SL	0.22 + 0.042*SL
ENB to DOUT	t_{PLH}	1.95	1.90 + 0.026*SL	1.92 + 0.021*SL	1.93 + 0.019*SL
	t_{PHL}	2.06	2.00 + 0.030*SL	1.99 + 0.033*SL	2.05 + 0.025*SL
	t_R	0.24	0.17 + 0.035*SL	0.16 + 0.036*SL	0.17 + 0.035*SL
	t_F	0.32	0.19 + 0.063*SL	0.28 + 0.035*SL	0.25 + 0.038*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 7, *Group3 : 7 < SL

JTAG TAP CONTROLLER MACROFUNCTION

TAP controller macrofunction consists of instruction register and data register scan paths, a bypass register, multiplexers and a 16-state finite state machine. The bypass register and instruction register are JTAG devices. TAP controller uses the largest available internal buffers (IVD8) to drive data register control signals.

Instruction register/decoder are external to TAP controller since the register length and instruction codes vary from one ASIC design to another. The instruction register consists of three JTINT1 macrocells. The instruction decoder is used to implement a minimum TAP configuration with a boundary scan register and an optional identification register.

TAP Controller Input Pin Description

Name	Mandatory	Description
BPSEL		Bypass select
DREGDI		Data register scan path data-in
IREGDI		Instruction register scan path data-in
TCK	•	Test clock
TDI	•	Test data input to the bypass register
TMS	•	Test mode select controlling state transitions of a finite state machine
TRSTN		Test reset input

TAP Controller Output Pin Description

Name	Mandatory	Description
DRE		Data register enable control output
IRE		Instruction register enable control output
RSTO		Reset output
SHFDR		Data register shift control output
SHFIR		Instruction register shift control output
TDO	•	Test data output
TDOE		TDO tri-state enable output
UPDATEDR		Data register update control output
UPDATEIR		Instruction register update control output

The bulleted pins (TCK, TDI, TMS and TDO) are mandatory pins associated with the IEEE P1149.1 standard test bus interface. TRSTN is an optional test reset input. It is possible to implement TAP without the test reset input indicated in the IEEE P1149.1 standard by setting TRSTN pin to high logic state. Alternatively, if a power-on reset capability is desired, TRSTN pin should be set to active low and connected to the power-on reset circuitry.

The 16 states of the finite state machine, diagrammed in the figure 9-3, also comply with the proposed IEEE P1149.1 standard. State transitions occur on the rising edge of TCK and are controlled by TMS. To ensure stable state transitions, TMS transitions occur on the falling edges of TCK. Capture, shift or update of test data take place on the next rising edge of TCK after the state transition or on each subsequent rising edge of TCK if no state transition occurs.

Figure 7-3. TAP Controller I/O Pin-Out Diagram

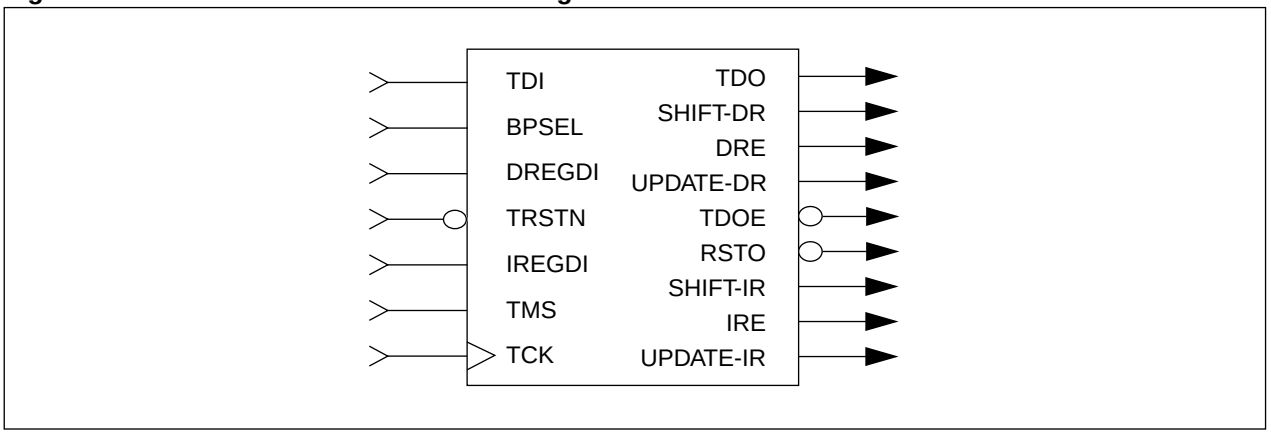
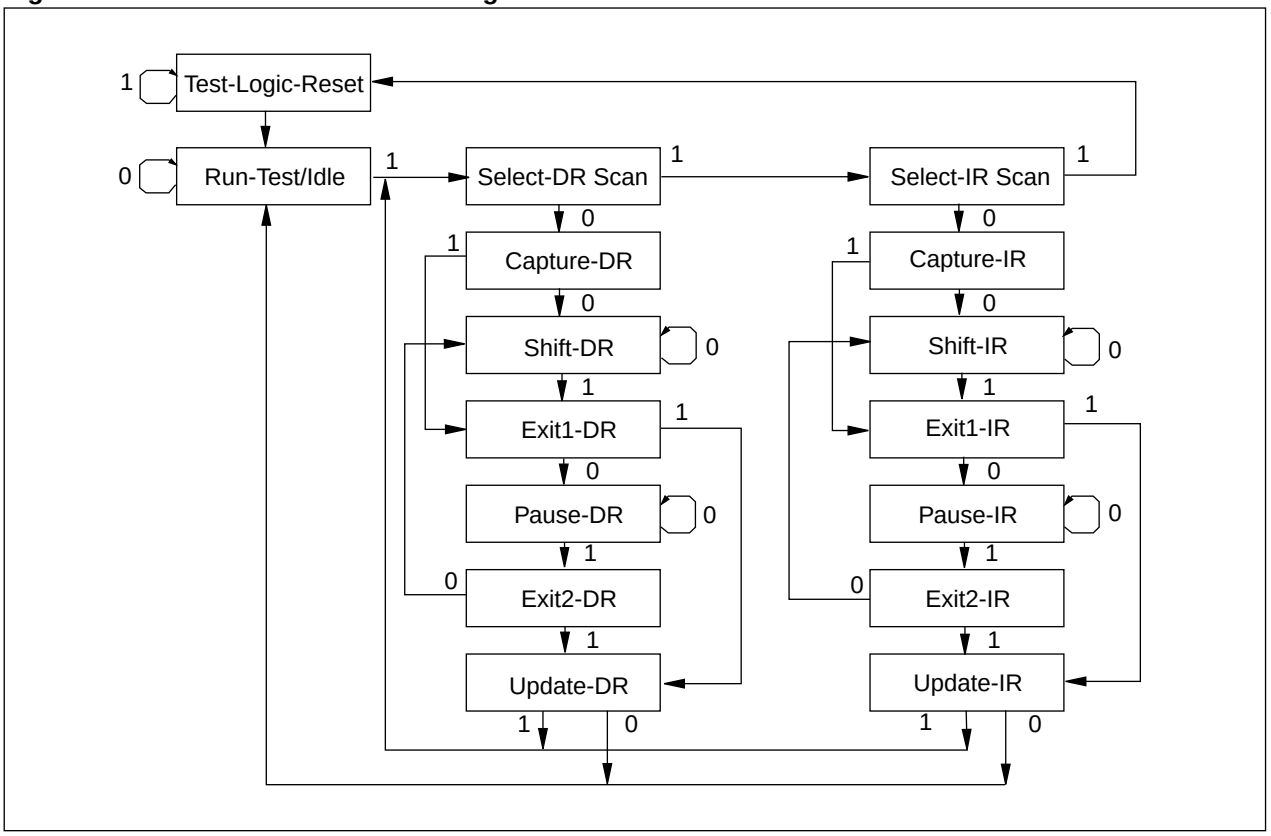


Figure 7-4. TAP Controller State Diagram



Behavior of TAP Controller States

Test-Logic-Reset

An initialization of the instruction register disables the test logic, allowing the on-chip system logic to operate normally. Irrespective of its original state, TAP controller reverts to Test-Logic-Reset when TMS is maintained high for five rising edges of TCK.

Run-Test/Idle

Idles in the state between scan operations or self-tests.

Capture-DR

Loads data parallelly into test data registers selected by the current instruction on the rising edge of TCK.

Shift-DR

Shifts data in the test data register between TDI and TDO one stage towards its serial output on each rising edge of TCK.

Pause-DR

Temporarily halts test data register shifts in the serial path between TDI and TDO.

Update-DR

Latches the data from the shift register path to the parallel output of test data registers on the falling edge of TCK.

Capture-IR

The shift-register contained in the instruction register loads a pattern of fixed logic value on the rising edge of TCK. It is possible to load design-specific data into shift-register stages that are not set to fixed values.

Shift-IR

Shifts data contained in the shift-register of the instruction register between TDI and TDO one stage towards its serial output on each rising edge of TCK.

Pause-IR

Temporarily halts shifting of the instruction register.

Update-IR

Latches the instruction shifted into the instruction register to the parallel output from the shift register path on the falling edge of TCK.

Select-DR-Scan, Select-IR-Scan, Exit1-DR, Exit2-DR, Exit1-IR, Exit2-IR

They are temporary controller states.

State Assignments for TAP Controller

Table 7-1. State Assignments

Controller State	State [3:0]	Controller State	State [3:0]
Exit2-DR	0	Exit2-IR	8
Exit1-DR	1	Exit1-IR	9
Shift-DR	2	Shift-IR	A
Pause-DR	3	Pause-IR	B
Select-IR Scan	4	Run-Test/Idle	C
Update-DR	5	Update-IR	D
Capture-DR	6	Capture-IR	E
Select-DR-Scan	7	Test-Logic-Reset	F

The bypass circuitry captures a low state during the data capture state of the finite state machine data cycle, as required by the proposed IEEE 1149.1 standard.

INSTRUCTION REGISTER/DECODER MACROFUNCTION

Instruction Register Macrofunction

The instruction register provides eight instructions in a minimum 3-bit device. These 3 bits are sufficient for operations of boundary scan cells and an instruction register, and three other operations such as the internal scan chains. Devices requiring more than eight instructions need a customer-specific design.

The instruction register allows an instruction to be shifted into the design. The instruction defines the test to be performed or the test data register to access or both. If a device identification register is present, the output register must be initialized to IDCODE instruction when TAP controller is in the Test-Logic-Reset state. Alternatively, it may be initialized to the bypass instruction. To support a fault isolation at the board-level, a constant binary ‘01’ pattern is loaded into the least significant bits of the instruction register when it is in the Capture-IR state.

Instruction Decoder Macrofunction

The instruction decoder operates with the instruction register to provide boundary scan control. Designs requiring other options need a customer-specific design.

Instruction Decoder Input Pin Description:

Name	Description
INST (2:0)	Instruction register input

Instruction Decoder Output Pin Description:

Name	Description
0_Mode	Boundary scan output mode control
I_Mode	Boundary scan input mode control

The instruction decoder has the following truth table.

INST(2)	INST(1)	INST(0)	I_Mode	0_Mode
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

IMPLEMENTATION OF IEEE P1149.1/JTAG

The following design procedures should be followed for ASIC implementation of IEEE P1149.1/JTAG using SEC boundary scan cells:

1. Allocate four (optionally five) package pins for testing.
2. Generate a bonding diagram, including provision for the corner pads that cannot be used for boundary scan I/Os.
3. Configure the top level device symbol with the same pin-out sequence as the packaged device.
4. Select appropriate boundary scan macrocells, JTBI1, JTCK, JTIN1 and JTOUT1, for the boundary-scan I/O pads. JTCK and JTIN1 must be associated with inputs; JTOUT1 with outputs and JTBI1 with bi-directional inputs and outputs.
5. ASIC clock inputs generally use JTCK macrocell, but it may be used for other critical inputs where performance considerations dominate. JTOUT1 macrocells are used for each output pin and JTBI1 macrocells are used by bi-directional pins.
6. JTAG inputs (TDI, TCK, TMS), output (TDO) and optional TRSTN are connected to TAP controller. The boundary scan register and the instruction register are connected to TDI and TCK inputs. Inputs, TDI, TMS and TRSTN should have input pull-up resistors.
7. To start the boundary scan chain sequence, connect any TDI input to JTBI1, JTCK, JTIN1, or JTOUT1 macrocells. The chain sequence proceeds to each adjacent macrocell I/O pad until terminated. TDO output of the final macrocell is connected to DREGDI input of TAP controller. Similarly, the terminal TDO output of the instruction register is connected to IREGDI of TAP controller.
8. Instruction register and data register control signals are connected to the instruction register and boundary scan registers, and INST signal lines from the instruction register are connected to the instruction decoder which supplies the control signals BPSEL, I_Mode and O_Mode for TAP controller and the boundary scan register. I_Mode is connected to JTIN1 macrocells and O_Mode is connected to JTOUT1 macrocells. I_Mode, O_Mode and MODE1 are also connected to the appropriate inputs of JTBI1 macrocells.
9. I_MODE output is connected to a IVD8 macrocell and TN inputs of the bi-directional and tri-state output buffers associated with the respective I/O pads. Other buffers may be required if there are a large number of bi-directional or tri-state pads.
10. If the design requires internal tri-state enable control signals, an additional JTINT1 macrocell is needed for each enable. Internal enable macrocells should be connected to TAP controller RSTO signal and O_MODE control line. JTIN1 macrocell is used for external tri-state enable input signals and should be connected to TAP controller RSTO signal and I_MODE control line.
11. Generate the test patterns to test JTAG portion of the design.

SYSTEM CLOCK CONSIDERATIONS

Test and system clocks must be synchronized carefully. All phases of the system clock should be gated on and off at a central point within the system. When TMS input is high, TCK can run continuously and test modes is disabled.