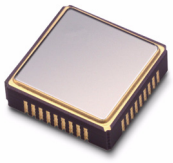
GENERAL DESCRIPTION



The M906-01 is a PLL (Phase Locked Loop) based clock generator that uses an internal VCSO (Voltage Controlled SAW Oscillator) to produce a very low jitter output clock. It is ideal for Gigabit Ethernet. The output clock (frequency of 156.25 or 187.50MHz for example) is provided from six LVPECL clock output pairs. (Specify frequency at time of order.) The accuracy of the output frequency is assured by the internal PLL, which phase-locks the internal VCSO to the reference input frequency (25 or 30MHz for example). The input reference can either be an external crystal, utilizing the internal crystal oscillator, or a stable external clock source such as a packaged crystal oscillator.

FEATURES

- **Output clock frequency from 125MHz to 190MHz (Consult factory for frequency availability)**
- **Six identical LVPECL output pairs**
- **Integrated SAW (surface acoustic wave) delay line**
- **Low jitter 0.7ps RMS (over 12kHz-20MHz)**
- **Ideal for Gigabit Ethernet clock reference**
- **Output-to-output skew < 100ps**
- **External XTAL or LVCMOS reference input**
- **Selectable external feed-through clock input**
- **STOP clock control (Logic 1 stops output clocks)**
- **Industrial temperature grade available**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

PIN ASSIGNMENT (9 x 9 mm SMT)

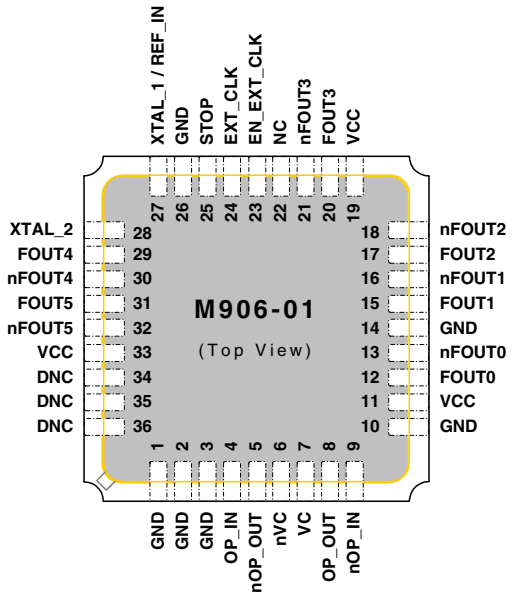


Figure 1: Pin Assignment

Example Output Frequency Configurations

Ref Clock Frequency (MHz)	PLL Ratio	Output Frequency [1] (MHz)	Application
20	25/4	156.25	GbE
25		156.25	10GbE
30		187.50	12GbE

Table 1: Example Output Frequency Configurations

Note 1:Specify output clock frequency at time of order

SIMPLIFIED BLOCK DIAGRAM

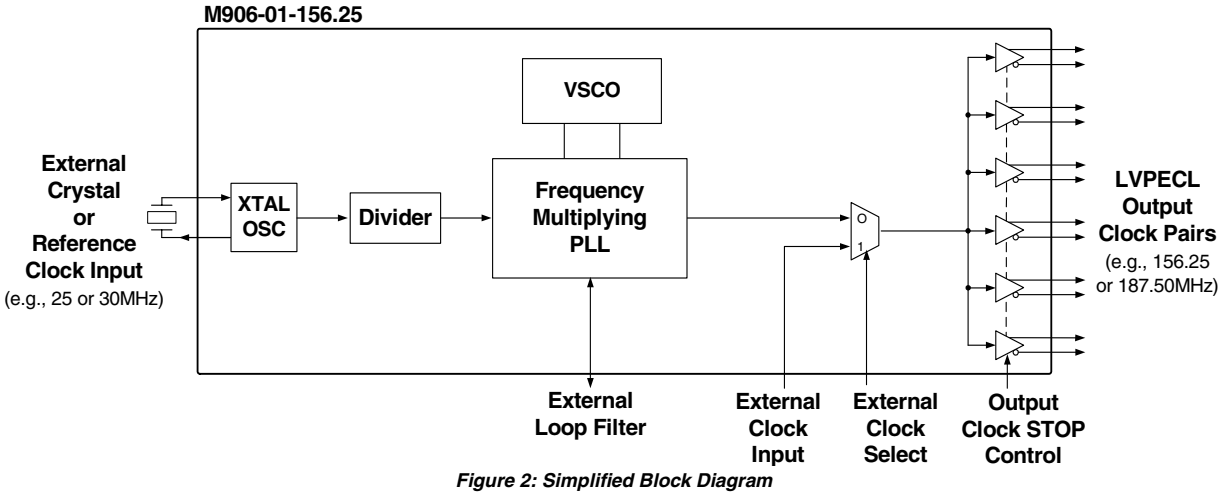


Figure 2: Simplified Block Diagram

DETAILED BLOCK DIAGRAM

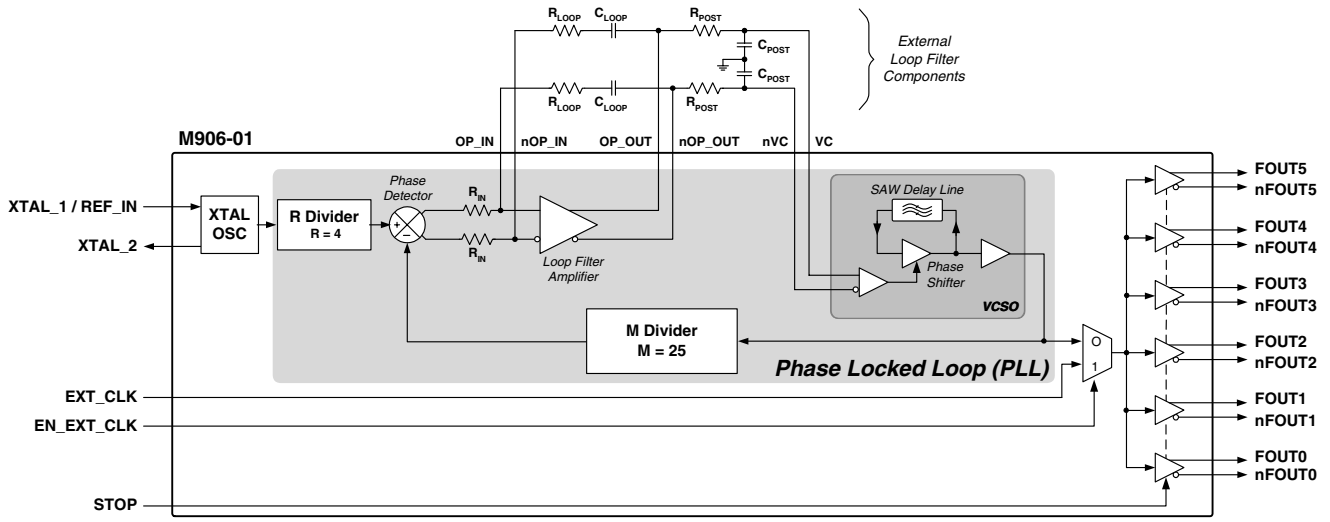


Figure 3: Detailed Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 4, External Loop Filter, on pg. 3.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12 13	FOUT0 nFOUT0	Output	No internal terminator	Clock output pairs, differential LVPECL output (156.25 MHz for the **M906-01-156.2500**)
15 16	FOUT1 nFOUT1			
17 18	FOUT2 nFOUT2			
20 21	FOUT3 nFOUT3			
29 30	FOUT4 nFOUT4			
31 32	FOUT5 nFOUT5			
23	EN_EXT_CLK	Input	Internal pull-down resistor[1]	Logic 1 enables the EXT_CLK input. Use Logic 0 for normal operation.
24	EXT_CLK	Input		External clock feed-through: 0 to 200 MHz
25	STOP	Input	Internal pull-down resistor[1]	Logic 1 stops clock outputs. Use Logic 0 for normal operation.
27	XTAL_1 / REF_IN	Input	Internal pull-down resistor[1]	External crystal connection. Also accepts LVCMOS/LVTTL compatible clock source.
28	XTAL_2	Input		External crystal connection. Leave unconnected when driving pin 27 with external clock reference.
34, 35, 36	DNC			Do Not Connect.

Table 2: Pin Descriptions

Note 1: For typical value of internal pull-down resistor, see **DC Characteristics**, **Pull-down** on pg. 5 for typical value.

FUNCTIONAL DESCRIPTION

The M906-01 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to an input reference clock.

The M906-01 combines the flexibility of a VCSO (Voltage Controlled SAW Oscillator) with the stability of a crystal oscillator.

Input Reference

The input reference can either be an external, discrete crystal device or a stable external clock source such as a packaged crystal oscillator:

- If an external crystal is used with the on-chip crystal oscillator circuit (XTAL OSC), the external crystal should be a parallel-resonant, fundamental mode crystal. Apply it to the XTAL_1 / REF_IN and XTAL_2 input pins. External crystal load capacitors are also required.
- If an external LVCMOS/LVTTL clock source is used, apply it to the XTAL_1 / REF_IN input pin.

In either case, the reference clock is supplied to the phase detector of the PLL. The M906-01 includes a reference divider that divides the input reference frequency by a fixed value “R” and provides the result to the phase detector.

The EX_CLK pin is available for a clock feed-through mode for testing. See “External Clock Feed-through” on pg. 4.

The PLL

The PLL (Phase Locked Loop) includes the phase detector, the VCSO, a feedback divider (labeled “M Divider”), and a reference divider (“R Divider”).

The feedback divider divides the VCSO output frequency by a fixed value “M” to match the reference frequency provided to the phase detector by the reference divider.

By controlling the frequency and phase of the VCSO, the phase detector precisely locks the frequency and phase of the feedback divider output to that of the reference divider output. This creates an output frequency that is a multiple of the reference frequency (which is output from the VCSO).

The relationship between the VCSO output frequency, the M Divider, the R Divider and the input reference frequency is defined as follows:

$$Fvcso = Fxtal \times \frac{M}{R}$$

For the **M906-01-156.2500** *(see* “Ordering Information” *on pg. 6):*

- VCSO output frequency = 156.25MHz
- Input reference frequency = 25MHz
- M=25
- R= 4

Therefore, for the **M906-01-156.2500**:

$$156.25MHz = 25MHz \times \frac{25}{4}$$

The product of the input crystal frequency and $\frac{M}{R}$ falls within the lock range of the VCSO.

External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M906-01 requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 4).

Due to the differential signal path design, the implementation requires two identical complementary RC filters as shown here.

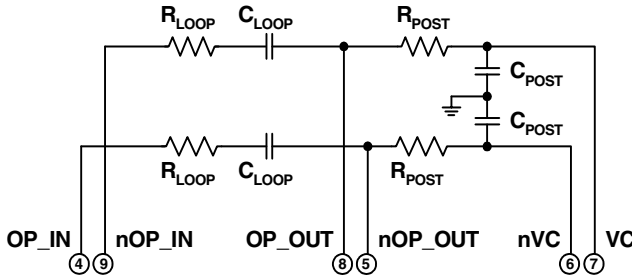


Figure 4: External Loop Filter

External Loop Filter Component Values

PLL Bandwidth	Damping Factor	R loop	C loop	R post	C post
500Hz	2.1	1.5kΩ	4.00µF	50kΩ	3300pF
1.5kHz	3.3	4.7kΩ	1.00µF	50kΩ	1500pF
6.4kHz	4.4	20.0kΩ	0.10µF	20kΩ	470pF
10.6kHz [1]	4.2	33.0kΩ	0.033µF	20kΩ	470pF

Table 3: External Loop Filter Component Values

Note 1: Recommended for most applications

External Clock Feed-through

The EXT_CLK pin provides an input for an external single-ended clock that directly drives the LVPECL clock outputs. In application, this may be used for system debugging and performance evaluation.

1. Set pin EN_EXT_CLK to Logic 1.
2. Apply an external LVCMOS/LVTTL clock source to the EXT_CLK input pin.

Due to the fact that EXT_CLK bypasses the PLL, any frequency between DC and 200MHz can be used.

STOP Clock

The STOP pin puts the output clock into a static condition.

Logic 1 Output clocks are static
Logic 0 Output clocks enabled for normal operation

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 4: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature					
		Commercial	0		+70	°C
		Industrial	-40		+85	°C

Table 5: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial)[1], T_A = -40 °C to +85 °C (industrial)[1], Output Frequency=156.25MHz[1], LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
	I_{CC}	Power Supply Current			350		mA
Logic Inputs	V_{IH}	Input High Voltage	EN_EXT_CLK, EXT_CLK, STOP	2		V_{CC} +0.3	V
	V_{IL}	Input Low Voltage		-0.3		0.8	V
	I_{IH}	Input High Current				150	µA
	I_{IL}	Input Low Current		-5.0			µA
Reference Clock Input	V_{IH}	Input High Voltage	XTAL_1 / REF_IN (XTAL_2 disconnected)	(V_{CC}/2) +0.5		V_{CC} +0.3	V
	V_{IL}	Input Low Voltage		-0.3		(V_{CC}/2) +0.5	V
	I_{IH}	Input High Current				150	µA
	I_{IL}	Input Low Current		-5.0			µA
All Inputs	C_{IN}	Input Capacitance, All Inputs	EN_EXT_CLK, EXT_CLK, STOP, XTAL_1 / REF_IN			4	pF
Pull-down	$R_{pulldown}$	Internal Pull-down Resistor	EN_EXT_CLK, STOP		51		kΩ
Differential Output	V_{OH}	Output High Voltage	FOUT, nFOUT (0-5)	V_{CC} -1.4		V_{CC} -1.0	V
	V_{OL}	Output Low Voltage		V_{CC} -2.0		V_{CC} -1.7	V
	V_{P-P}	Peak to Peak Output Voltage		0.6		0.85	V

Table 6: DC Characteristics

Note 1: See Ordering Information on pg. 6

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial)[1], T_A = -40 °C to +85 °C (industrial)[1], Output Frequency=156.25MHz[1], LVPECL outputs terminated with 50Ω to V_{CC} - 2V

Symbol	Parameter		Min	Typ	Max	Unit	Test Conditions
F_{OUT}	Output Frequency Range		125	156.25	190	MHz	
F_{IN}	Nominal Input Frequency, XTAL_1 / REF_IN			25		MHz	
APR	VCSO Pull-Range		±100	±150		ppm	
Φn	Single Side Band Phase Noise @156.25MHz	1kHz Offset		-100		dBc/Hz	
		10kHz Offset		-110		dBc/Hz	
		100kHz Offset		-134		dBc/Hz	
J(t)	Jitter (rms)			0.7	1.0	ps	12kHz to 20MHz
t_{DC}	Output Duty Cycle, High Time		45	50	55	%	
t_R	Output Rise Time	FOUT, nFOUT (0-1)	350	450	550	ps	20% to 80%
t_F	Output Fall Time	FOUT, nFOUT (0-1)	350	450	550	ps	20% to 80%
t_S	Output Skew	Between Any Pair			100	ps	
	EXT_CLK Frequency	EXT_CLK	0		200	MHz	

Table 7: AC Characteristics

Note 1: See Ordering Information on pg. 6

DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:

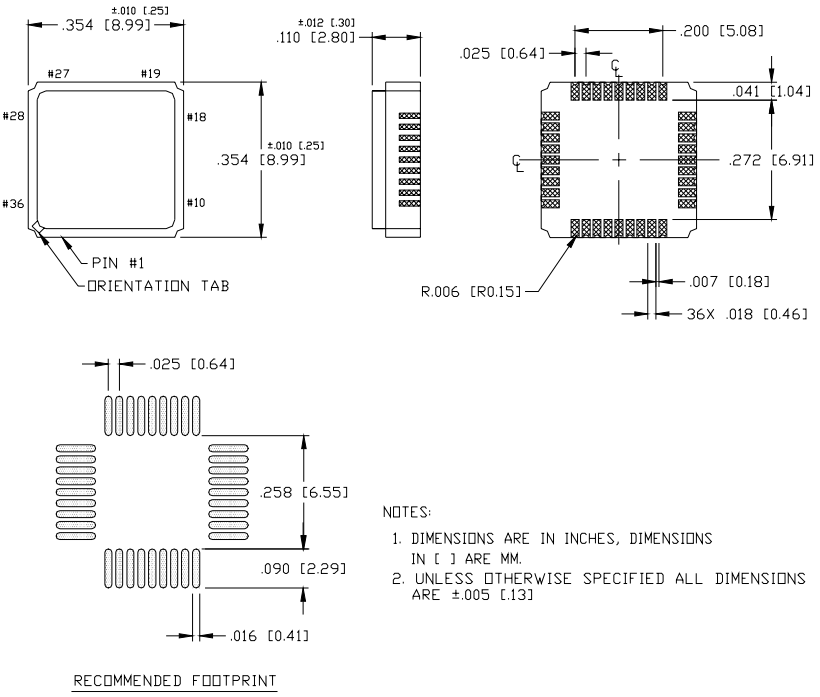


Figure 5: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

Part Numbering Scheme

Part Number: **M906-01-xxx.xxxx**

Device Number

Temperature
"-" = 0 to +70 °C (commercial)
I = - 40 to +85 °C (industrial)

Output Frequency (MHz)
See Table 8, right. Consult ICS for other frequencies.

Figure 6: Part Numbering Scheme

Example Part Numbers

Output Freq. (MHz)	Temperature	Order Part Number
156.25	commercial	**M906-01-156.2500**
	industrial	**M906-01I156.2500**
156.25	commercial	**M906-01-156.2500**
	industrial	**M906-01I156.2500**
187.50	commercial	**M906-01-187.5000**
	industrial	**M906-01I187.5000**

Table 8: Example Part Numbers

Consult factory for frequency availability.