LXT305

T1/E1 Integrated Short Haul Transceiver with Transmit Jitter Attenuation

General Description

The LXT305 is a fully integrated transceiver for both North American 1.544 MHz (T1), and European 2.048 MHz (E1) applications. Transmit pulse shapes (T1 or E1) are selectable for various line lengths and cable types.

The LXT305 provides transmit jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface. It is especially well suited for applications involving T1 and higher rates such as M13 mux, SONET, etc. A variety of diagnostic features including transmit and receive monitoring are incorporated. Clock inputs may be derived from an on-chip crystal oscillator or digital inputs.

The LXT305, an advanced double-poly, double-metal CMOS device, requires only a single 5-volt power supply.

Applications

- SONET Equipment
- M13 Multiplexers
- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Compatible with most popular PCM framers including the LXP2180A and LXP2181A
- Line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV
- Selectable slicer levels (T1/E1) improve SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Local and remote loopback functions
- Transmit Driver Performance Monitor (DPM) output
- Receive monitor with Loss of Signal (LOS) output
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Pin and functional compatibility with Crystal CS61535
- Replaces CS61534
- Transmit jitter attenuation starting at 3 Hz
- Microprocessor controllable
- Available in 28 pin DIP and PLCC

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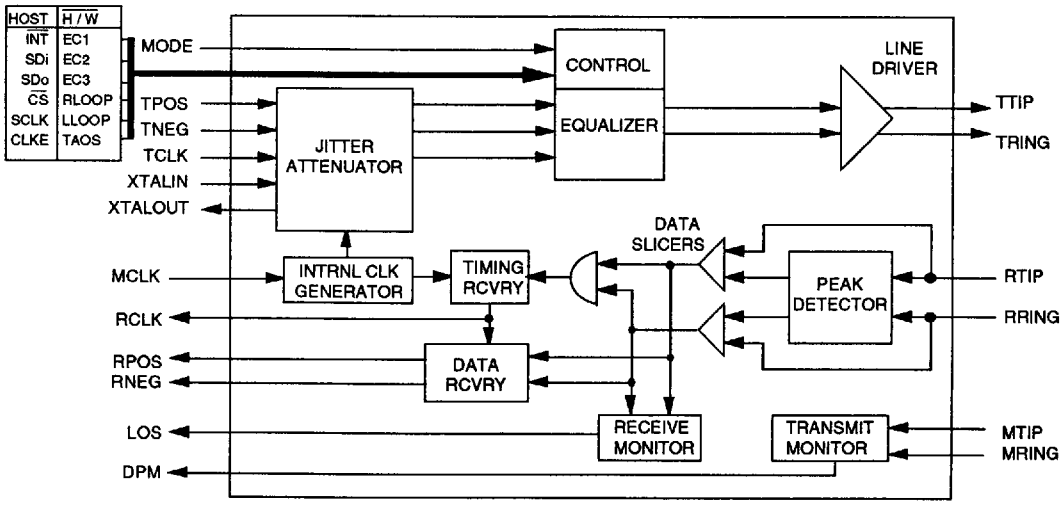
Figure 1: LXT305 Block Diagram



Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin [1]	V_{IN}	RGND - 0.3	RV+ + 0.3	V
Input current, any pin [2]	I_{IN}	-10	10	mA
Ambient operating temperature	T_A	-40	85	°C
Storage temperature	T_{STG}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation not guaranteed at these extremes.
[1] Excluding RTIP and RRING which must stay within -6V to RV + 0.3V.
[2] Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100mA.

Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
DC supply [3]	RV+, TV+	4.75	5.0	5.25	V	
Ambient operating temperature	T_A	-40	25	85	°C	
Total power dissipation [4]	P_D	-	620	–	mW	100% ones density & maximum line length @ 5.25 V

[3] TV+ must not exceed RV+ by more than 0.3 V.
[4] Power dissipation while driving 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Digital Characteristics (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

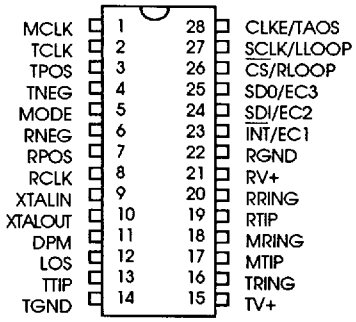
Parameter	Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage [5,6] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	–	V	
Low level input voltage [5,6] (pins 1-5, 10, 23-28)	V_{IL}	–	–	0.8	V	
High level output voltage [5,6] (pins 6-8, 11, 12, 23, 25)	V_{OH}	2.4	–	–	V	I_{OUT}=- 400 µA
Low level output voltage [5,6] (pins 6-8, 11, 12, 23, 25)	V_{OL}	–	–	0.4	V	I_{OUT}=1.6mA
Input leakage current	I_{LL}	-10	–	+10	µA	
Three-state leakage current [5] (pin 25)	I_{3L}	-10	–	+10	µA	

[5] Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.
[6] Output drivers will output CMOS logic levels into CMOS loads.

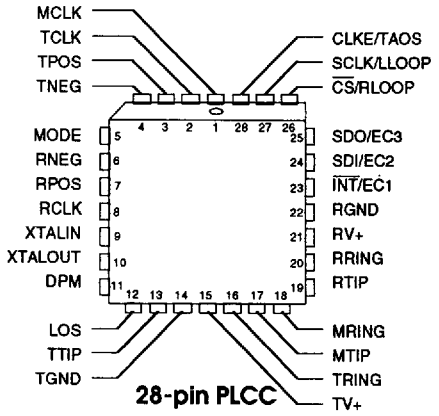
Analog Specifications (T_A = -40° to 85°C, V+ = 5.0 V ±5%, GND = 0 V)

Parameter		Min	Typ	Max	Units	Test Conditions
AMI Output Pulse Amplitudes	T1	2.4	3.0	3.6	V	measured at the DSX
	E1	2.7	3.0	3.3	V	measured at line side
Recommended Output Load at TTIP and TRING		–	25	–	Ω	
Jitter added by the transmitter [7]	10Hz - 8kHz	–	–	0.01	UI	
	8kHz - 40 kHz	–	–	0.025	UI	
	10Hz - 40 kHz	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Sensitivity below DSX	(0dB = 2.4V)	13.6	–	–	dB	
		500	–	–	mV	
Loss of Signal threshold		–	0.3	–	V	
Data decision threshold	T1	63	70	77	%peak	
	E1	43	50	57	% peak	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance	10kHz - 100kHz	0.4	–	–	UI	
Jitter attenuation curve corner frequency [8]		–	3	–	Hz	

[7] Input signal to TCLK is jitter-free.
[8] Circuit attenuates jitter at 20 dB/decade above the corner frequency.



28-pin DIP



28-pin PLCC

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Pin Descriptions

Pin #	Sym	I/O	Name	Description
1	MCLK	I	Master Clock	A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
2	TCLK	I	Transmit Clock	Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. Except during remote loopback, the transmitter remains powered down if TCLK is not supplied.
3	TPOS	I	Transmit Positive Data	Input for positive pulse to be transmitted on the twisted-pair line.
4	TNEG	I	Transmit Negative Data	Input for negative pulse to be transmitted on the twisted-pair line.
5	MODE	I	Mode Select	Setting MODE to logic 1 puts the LXT305 in the Host mode. In the Host mode, the serial interface is used to control the LXT305 and determine its status. Setting MODE to logic 0 puts the LXT305 in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
6	RNEG	O	Receive Negative Data	Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). In the Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware mode both outputs are stable and valid on the rising edge of RCLK.
7	RPOS	O	Receive Positive Data	
8	RCLK	O	Recovered Clock	This is the clock recovered from the signal received at RTIP and RRING.

Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
9	XTALIN	I	Crystal Input	An external crystal operating at four times the bit rate (6.176 MHz for T1, 8.192 MHz for E1 applications) with an 18.7pF load is required to enable the jitter attenuation function of the LXT305. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
10	XTALOUT	O	Crystal Output	
11	DPM	O	Driver Performance Monitor	DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains at logic 1 until a signal is detected.
12	LOS	O	Loss Of Signal	LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when a mark is received.
13	TTIP	O	Transmit Tip	Differential Driver Outputs. These outputs are designed to drive a 25 Ω load. The transmitter will drive 100 Ω shielded twisted-pair cable through a 2:1 step-up transformer without additional components. To drive 75Ω coaxial cable, two 2.2 Ω resistors are required in series with the transformer.
16	TRING	O	Transmit Ring	
14	TGND	-	Transmit Ground	Ground return for the transmit drivers power supply TV+.
15	TV+	I	Transmit Power Supply	+5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3V.
17	MTIP	I	Monitor Tip	These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another LXT305 on the board. *Host mode only:* To prevent false interrupts in the host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-level voltage. The monitor clock can range from 100kHz to the TCLK frequency.
18	MRING	I	Monitor Ring	
19	RTIP	I	Receive Tip	The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
20	RRING	I	Receive Ring	
21	RV+	I	Receive Power Supply	+5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	-	Receive Ground	Ground return for power supply RV+.

Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
23	$\overline{INT}$	O	Interrupt *(Host Mode)*	This LXT305 Host mode output goes low to flag the host processor when LOS or DPM go active. $\overline{INT}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the respective register bit (LOS and/or DPM.)
	EC1	I	Equalizer Control 1 *(H/W Mode)*	The signal applied at this pin in the LXT305 Hardware mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
24	SDI	I	Serial Data In *(Host Mode)*	The serial data input stream is applied to this pin when the LXT305 operates in the Host mode. SDI is sampled on the rising edge of SCLK.
	EC2	I	Equalizer Control 2 *(H/W Mode)*	The signal applied at this pin in the LXT305 Hardware mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
25	SDO	O	Serial Data Out *(Host Mode)*	The serial data from the on-chip register is output on this pin in the LXT305 Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is high.
	EC3	I	Equalizer Control 3 *(H/W Mode)*	The signal applied at this pin in the LXT305 Hardware mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
26	$\overline{CS}$	I	Chip Select *(Host Mode)*	This input is used to access the serial interface in the LXT305 Host mode. For each read or write operation, $\overline{CS}$ must transition from high to low, and remain low.
	RLOOP	I	Remote Loopback *(H/W Mode)*	This input controls loopback functions in the LXT305 Hardware mode. Setting RLOOP to a logic 1 enables the Remote Loopback mode. Setting both RLOOP and LLOOP causes a Reset .
27	SCLK	I	Serial Clock *(Host Mode)*	This clock is used in the LXT305 Host mode to write data to or read data from the serial interface registers.
	LLOOP	I	Local Loopback *(H/W Mode)*	This input controls loopback functions in the LXT305 Hardware mode. Setting LLOOP to a logic 1 enables the Local Loopback Mode.
28	CLKE	I	Clock Edge *(Host Mode)*	Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	I	Transmit All Ones *(H/W Mode)*	When set to a logic 1, TAOS causes the LXT305 (Hardware mode) to transmit a continuous stream of marks at the MCLK frequency.

Functional Description

The LXT305 is a fully integrated PCM transceiver for both 1.544 MHz (T1) and 2.048 MHz (E1) applications which allows full-duplex transmission of digital data over existing twisted-pair installations.

Figure 1 is a simplified block diagram of the LXT305. The LXT305 transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

Transmitter

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). If TCLK is not supplied, the transmitter remains powered down (except during remote loopback). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 1. Refer to Table 2 and Figure 2 for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode.

Pulses can be shaped for either 1.544 or 2.048 MHz applications. 1.544 MHz pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The LXT305 also matches FCC and ECSA specifications for CSU applications. 2.048 MHz pulses can drive either coaxial or shielded twisted-pair lines using appropriate resistors in line with the output transformer.

Jitter Attenuation

Jitter attenuation of the LXT305 transmit outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 3 for crystal specifications. The ES is a 32 x 2-bit register. Transmit data is clocked into the ES with the transmit clock (TCLK) signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the transmit path.

Driver Performance Monitor

The transceiver incorporates a Driver Performance Monitor (DPM) connected in parallel with TTIP and TRING at the output transformer. The DPM output level goes high upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

Line Code

The LXT305 transmits data as a 50% AMI line code as shown in Figure 3. Power consumption is reduced by activating the AMI line driver only to transmit a mark. The output driver is disabled during transmission of a space.

Table 1: Equalizer Control Inputs

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Frequency
0	1	1	0 - 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
1	0	0	133 - 266 ft ABAM	1.2 dB		
1	0	1	266 - 399 ft ABAM	1.8 dB		
1	1	0	399 - 533 ft ABAM	2.4 dB		
1	1	1	533 - 655 ft ABAM	3.0 dB		
0	0	0	CCITT Recommendation G.703		E1	2.048 MHz
0	1	0	FCC Part 68, Option A		CSU (DS-1)	1.544 MHz

[1] Line length from transceiver to DSX-1 cross-connect point.
[2] Maximum cable loss at 772 kHz.

Table 2: LXT305 Master Clock and Transmit Timing Characteristics (See Figure 2)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	T1	MCLK	-	1.544	-	MHz
	E1	MCLK	-	2.048	-	MHz
Master clock tolerance		MCLKt	-	±100	-	ppm
Master clock duty cycle		MCLKd	40	-	60	%
Crystal frequency	T1	fc	-	6.176	-	MHz
	E1	fc	-	8.192	-	MHz
Transmit clock frequency	T1	TCLK	-	1.544	-	MHz
	E1	TCLK	-	2.048	-	MHz
Transmit clock tolerance		TCLKt	-	-	±50	ppm
Transmit clock duty cycle		TCLKd	10	-	90	%
TPOS/TNEG to TCLK setup time		t_{SUT}	25	-	-	ns
TCLK to TPOS/TNEG Hold time		t_{HT}	25	-	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 2: LXT305 Transmit Clock Timing Diagram

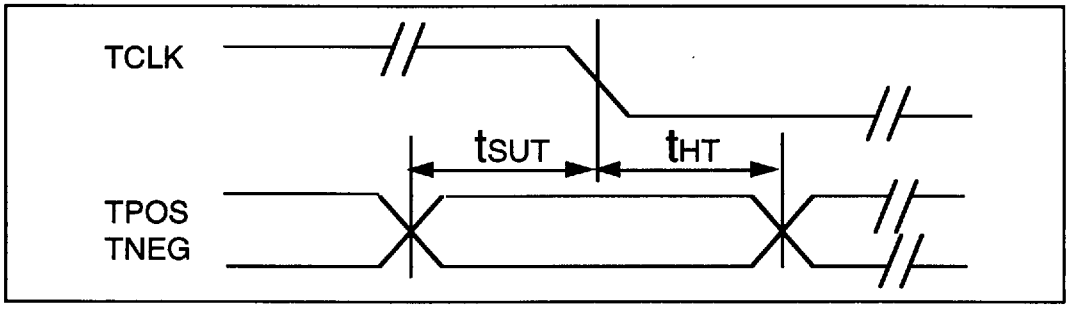
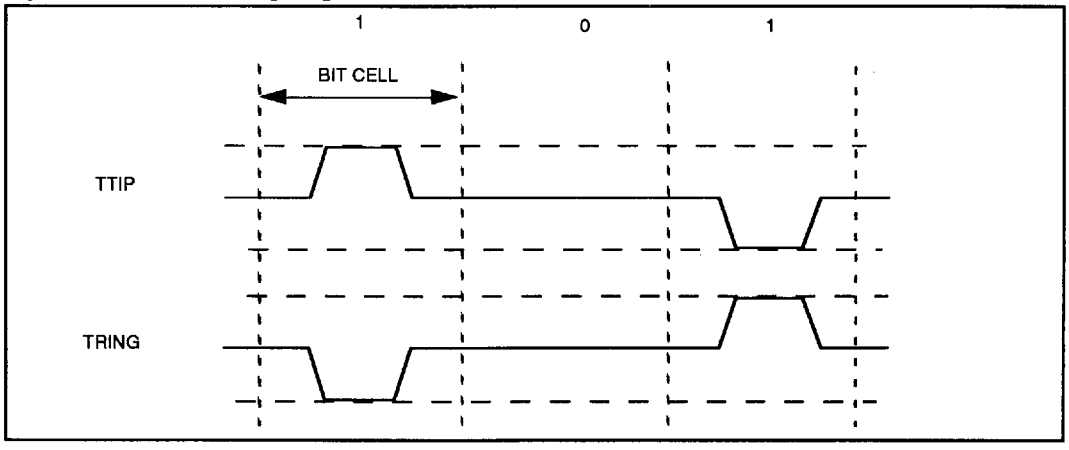


Figure 3: 50% AMI Coding Diagram



Receiver

The signal is received from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 4 and Figure 4 for LXT305 receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For T1 applications (determined by Equalizer Control inputs EC1 - EC3 ≠ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000) the threshold is set to 50 %.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum cable length is 1500 feet of ABAM cable (approximately 6 dB). Regardless of received signal level, the peak detectors are held above a minimum level of .3 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros (spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and the RCLK output is replaced with the MCLK. The LOS output is reset when a mark is received.

Operating Modes

The LXT305 transceiver can be controlled by a microprocessor through the serial interface (Host mode), or through hard-wired pins (Hardware mode). The mode of operation is set by the MODE pin logic level. The transceivers can also be commanded to operate in one of several diagnostic modes.

Table 3: LXT305 Crystal Specifications (External)

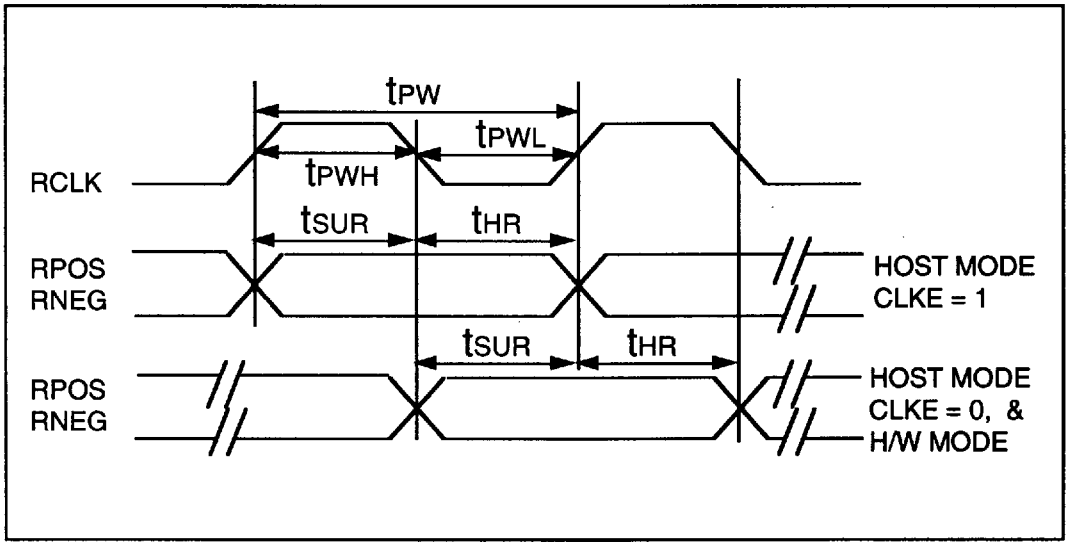
Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical

Table 4: LXT305 Receive Characteristics (See Figure 4)

Parameter		Sym	Min	Typ[1]	Max	Units
Receive slicer threshold	T1	RST	65	70	75	%
	E1	RST	45	50	55	%
Receive clock duty cycle [2]	T1	RCLKd	40	50	60	%
	E1	RCLKd	40	50	60	%
Receive clock pulse width [2]	T1	t_{PW}	594	648	702	ns
	E1	t_{PW}	447	488	529	ns
Receive clock pulse width high	T1	t_{PWH}	-	324	-	ns
	E1	t_{PWH}	-	244	-	ns
Receive clock pulse width low	T1	t_{PWL}	270	324	378	ns
	E1	t_{PWL}	203	244	285	ns
RPOS / RNEG to RCLK rising setup time	T1	t_{SUR}	50	270	-	ns
	E1	t_{SUR}	50	203	-	ns
RCLK rising to RPOS / RNEG hold time	T1	t_{HR}	50	270	-	ns
	E1	t_{HR}	50	203	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
[2] RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz, 0.2 UI clock displacement for 2.048 MHz.)

Figure 4: LXT305 Receive Clock Timing Diagram



Host Mode Operation

To allow a host microprocessor to access and control the LXT305 through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte.

The Host mode provides a latched Interrupt output ($\overline{INT}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as follows:

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

The LXT305 serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The LXT305 contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select ($\overline{CS}$) input to transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 5 lists serial data output bit combinations for each status. Serial data structure is shown in Figure 5 and I/O timing characteristics are shown in Table 6, and Figures 6 and 7.

Hardware Mode Operation

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK.

To operate in Hardware mode, MODE must be set to 0. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host mode.

Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. MCLK provides the receiver reference. The crystal oscillator provides the transmitter reference. If the LXT305 crystal oscillator is grounded, MCLK is used as the transmitter reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and then begins calibration.

Table 5: LXT305 Serial Data Output Bits (See Figure 5)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	Local Loopback active
0	1	1	TAOS and Local Loopback active
1	0	0	Remote Loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred

Figure 5: LXT305 Serial Interface Data Structure

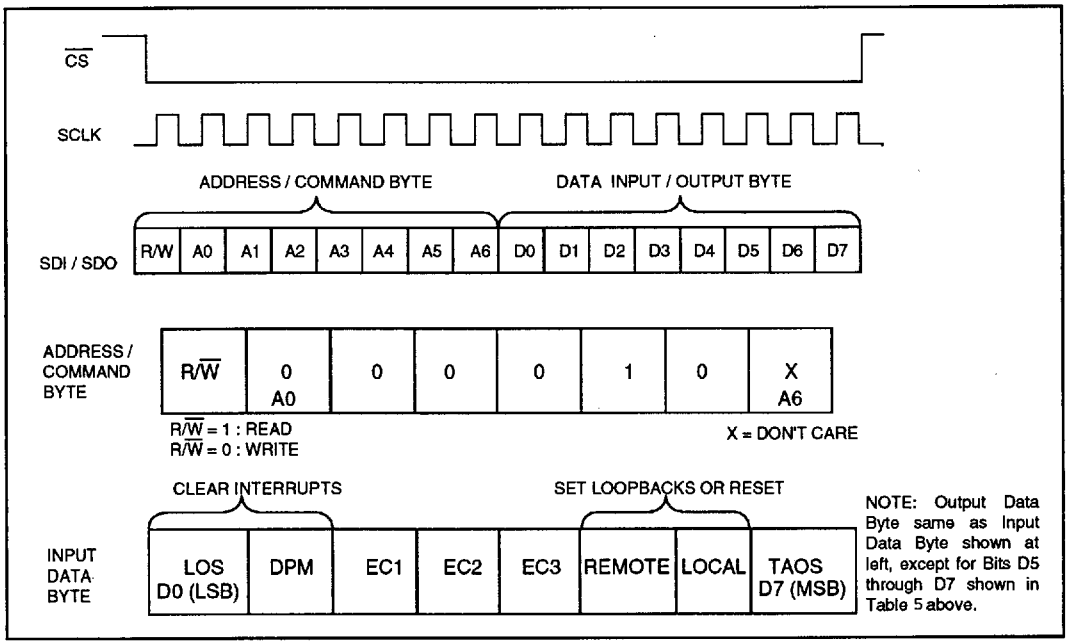


Table 6: LXT305 Serial I/O Timing Characteristics (See Figures 6 and 7)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	t_{DC}	50	-	-	ns	
SCLK to SDI hold time	t_{CDH}	50	-	-	ns	
SCLK low time	t_{CL}	240	-	-	ns	
SCLK high time	t_{CH}	240	-	-	ns	
SCLK rise and fall time	t_R, t_F	-	-	50	ns	
CS to SCLK setup time	t_{CC}	50	-	-	ns	
SCLK to CS hold time	t_{CCH}	50	-	-	ns	
CS inactive time	t_{CWH}	250	-	-	ns	
SCLK to SDO valid	t_{CDV}	-	-	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	-	100	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 6: LXT305 Serial Data Input Timing Diagram

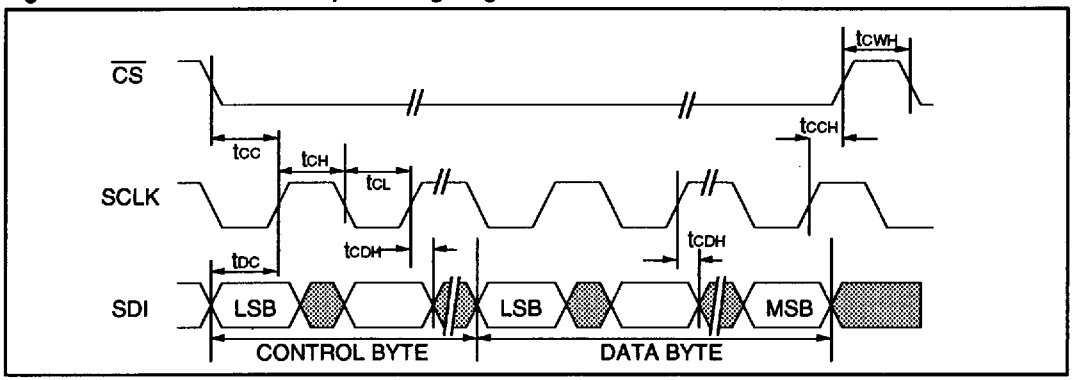
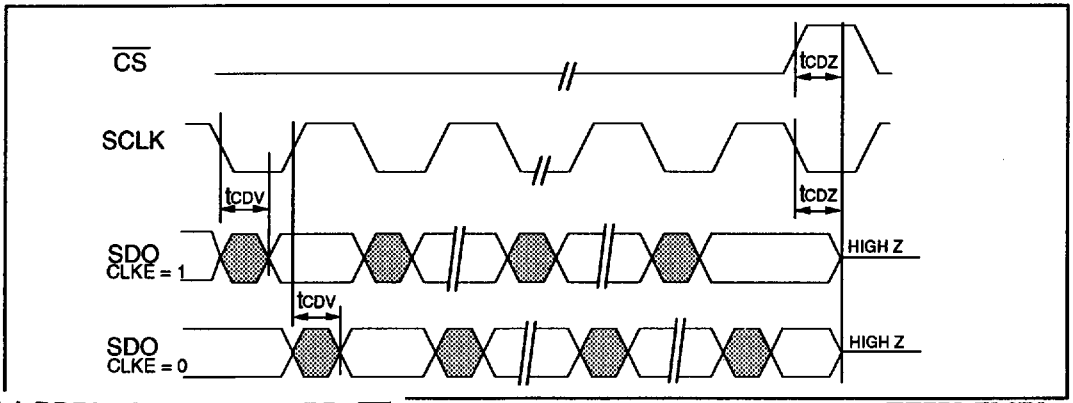


Figure 7: LXT305 Serial Data Output Timing Diagram



Diagnostic Mode Operation

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1's at the TCLK frequency when TAOS is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback. During TAOS, the transmitter is locked to MCLK.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK.) The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs will be transmitted normally. (A stream of 1's will be transmitted if the TAOS command is active.)

Power Requirements

The LXT305 is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3V of each other, and decoupled to their respective grounds separately, as shown in Figure 8. Isolation between the transmit and receive circuits is provided internally. Except during remote loopback, the transmitter powers down if TCLK is not supplied.

Applications

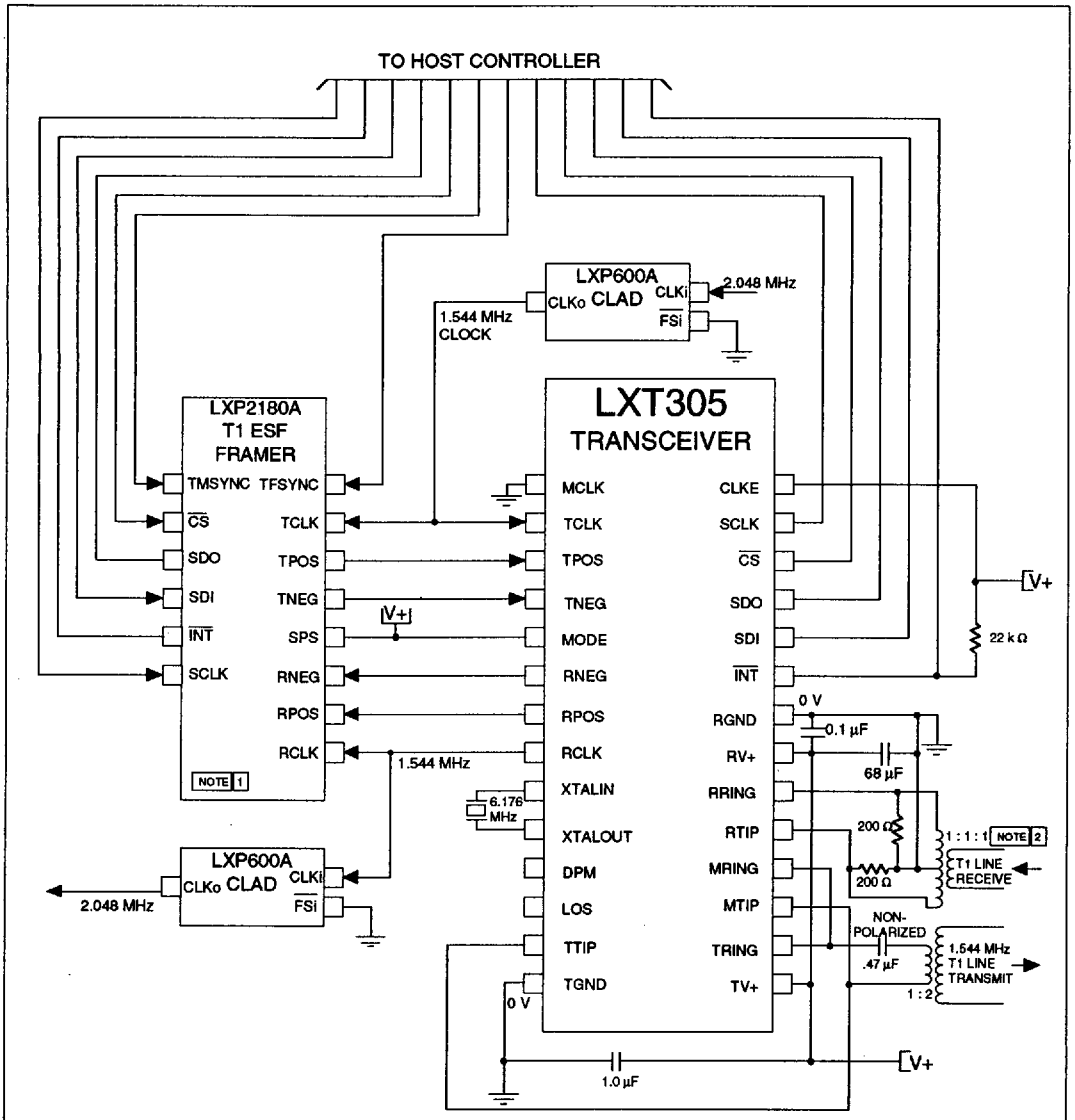
1.544 MHz DSX-1 Interface Applications

Figure 8 is a typical 1.544 MHz DSX-1 application. The LXT305 is shown in the Host mode with the LXP2180A T1/ESF Framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. An LXP600A Clock Adapter (CLAD) provides the 2.048 MHz system backplane clock, locked to the recovered 1.544 MHz clock signal. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68µF and 0.1 µF on the receive side.)

2.048 MHz E1 Interface Applications

Figure 9 is a typical 2.048 MHz E1 application. The LXT305 is shown in Hardware mode with the LXP2181A E1/CRC4 Framer. Resistors are installed in line with the transmit transformer for loading a 75 Ω coaxial cable. The in-line resistors are not required for transmission on 100 Ω shielded twisted-pair lines. As in the DSX-1 application Figure 8, this configuration is illustrated with a crystal in place to enable the LXT305 Jitter Attenuation Loop, and a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function.

Figure 8: Typical LXT305 1.544 MHz T1 Application (Host Mode)



NOTE 1 IN ADDITION TO THE LXP2180A, THE LXT305 IS COMPATIBLE WITH A WIDE VARIETY OF DIGITAL FRAMING AND SIGNALING DEVICES, INCLUDING THE LXP2181A, DS2180A, MT8976, AND R8070.

NOTE 2 WHEN LXT305 IS CONNECTED TO THE CROSS-CONNECT FRAME THROUGH A LOW LEVEL MONITOR JACK, RECEIVE TRANSFORMER SHOULD BE 1 : 2 : 2 TO BOOST THE INPUT SIGNAL.

Figure 9: Typical LXT305 2.048 MHz E1 Application (Hardware Mode)