12.0 Electrical and Timing Specifications

Table 12. Recommended Operating Conditions

Parameter	Symbol	150 MHz		170 MHz		220 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Power Supply	VDD, DACVDD, PLLVDD	3.0	3.6	3.0	3.6	3.0	3.6	Volts
Case Temperature	T_C	0	100	0	100	0	100	°C
DAC Output Load	R_L	37.5	50	37.5	50	37.5	50	W
Reference Voltage	V_{REF}	1.204	1.266	1.204	1.266	1.204	1.266	Volts

Table 13. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Power Supply	VDD, DACVDD, PLLVDD	-0.5	3.8	Volts
Signal Pin Voltage		-0.5	5.5	Volts
DAC Output Short Circuit Duration	t_s		∞	seconds
Case Temperature	T_C	0	145	°C
Soldering Temperature (5 seconds, 0.25 in. from case)	T_{SOL}		260	°C
Vapor Phase Soldering Temperature (1 minute)	$T_{V,SOL}$		220	°C

Table 14. DC Characteristics

Parameter	Symbol	Min.	Typical	Max.	Units
DAC Outputs					
Resolution		8	8	8	Bits
Integral Linearity Error	ILE			3/4	LSB
Differential Linearity Error	DLE			3/4	LSB
Grey Scale Error				5	% Grey Scale
Monotonicity		Guaranteed	Guaranteed	Guaranteed	
Coding					Binary
CMOS Digital Inputs					
Input High Voltage (V_{DD} = 3.3 V)	V_{IH}	2.0		5.5	Volts
Input Low Voltage	V_{IL}	-0.5		0.8	Volts
Input High Current (V_{IH} = 2.4V)	I_{IH}			20	µA
Input Low Current (V_{IL} = 0.0V)	I_{IL}	-20			µA
Input Capacitance (f=1 MHz, V_{IN} = 2.4V)	C_{IN}		4	8	pF
Digital Outputs					
Output High Voltage (I_{OH} = -12 mA)	V_{OH}	2.4			Volts
Output Low Voltage (I_{OL} = 6 mA)	V_{OL}			0.4	Volts
Hi-Z Current (0 ≤ V ≤ 3.6 V)	I_{OZ}	-20		20	µA
Analog Outputs					
DAC Inaccuracy				7	%
DAC-to-DAC Mismatch				5	%
Output Compliance	V_{OC}	-0.5		1.2	Volts

Table 15. AC Characteristics

Parameter	Symbol	Spec.	150 MHz	170 MHz	220 MHz	Units
RS[2:0] Setup	t_1	min	10	10	10	ns
RS[2:0] Hold	t_2	min	10	10	10	ns
$\overline{RD}$, $\overline{WR}$ Low	t_3	min	50	50	50	ns
$\overline{RD}$, $\overline{WR}$ High	t_4	min	6 × pclk	6 × pclk	6 × pclk	ns
$\overline{RD}$ Low to Data Bus Driven	t_5	min	2	2	2	ns
$\overline{RD}$ Low to Data Bus Valid	t_6	max	40	40	40	ns
$\overline{RD}$ High to Data Bus 3-Stated	t_7	max	20	20	20	ns
Data Bus Hold from $\overline{RD}$ High	t_8	min	2	2	2	ns
Write Data Setup	t_9	min	10	10	10	ns
Write Data Hold	t_{10}	min	10	10	10	ns
LCLK, SCLK Low	t_{11}	min	4	4	4	ns
LCLK, SCLK High	t_{12}	min	4	4	4	ns
LCLK, SCLK Cycle	t_{13}					
16:1 MUX Mode		max	9.38	10.6	13.75	MHz
8:1 MUX Mode		max	18.75	21.25	27.5	MHz
4:1 MUX Mode		max	37.5	42.5	55	MHz
2:1 MUX Mode		max	75	85	100	MHz
1:1 MUX Mode		max	100	100	100	MHz
16:1 MUX Mode		min	106.67	94.12	72.7	ns
8:1 MUX Mode		min	53.33	47.06	36.4	ns
4:1 MUX Mode		min	26.67	23.53	18.2	ns
2:1 MUX Mode		min	13.33	11.77	10	ns
1:1 MUX Mode		min	10	10	10	ns
PIX[63:0] Setup	t_{14}	min	1	1	1	ns
PIX[63:0] Hold	t_{15}					
1:1 MUX Mode		min	4	4	4	ns
Not 1:1 MUX Mode		min	2	2	2	ns
VGA[7:0], $\overline{BLANK}$, $\overline{BORDER}$ $\overline{HSYNCIN}$, $\overline{VCSYNCIN}$ Setup(1)	t_{16}	min	3	3	3	ns
VGA[7:0], $\overline{BLANK}$, $\overline{BORDER}$ $\overline{HSYNCIN}$, $\overline{VCSYNCIN}$ Hold(1)	t_{17}	min	3	3	3	ns
SCLK to LCLK skew (T=SCLK cycle time)	t_{18}	min	-2	-2	-2	ns
		max	T-8	T-8	T-8	ns
Supply Current (2)		typ(3)	450	450	650	mA
		max(4)	650	716	890	mA

Notes:

1. Setup and hold times for $\overline{VCSYNCIN}$ are only for when this signal is used as composite sync in. For usage as vertical sync in, there is no setup or hold time.
2. Supply current is the total of I_{VDD}, I_{VDDDAC} and I_{VDDPLL}.
3. Typical power dissipation is for VDD, VDDDAC, VDDPLL = 3.3 V, TA = 20 °C, with typical pixel patterns such as displayed with graphical user interfaces, and
   150 and 170 MHz parts running at 135 MHz (e.g,. for 1280 x 1024 screen)
   220 MHz part running at 216 MHz (e.g,. for 1600 x 1280 screen)
4. Maximum power dissipation is for VDD, VDDDAC, VDDPLL = 3.6 V, TA = 0 °C, with alternating full black/full white pixels running at the maximum specified frequency (150/170/220 MHz)

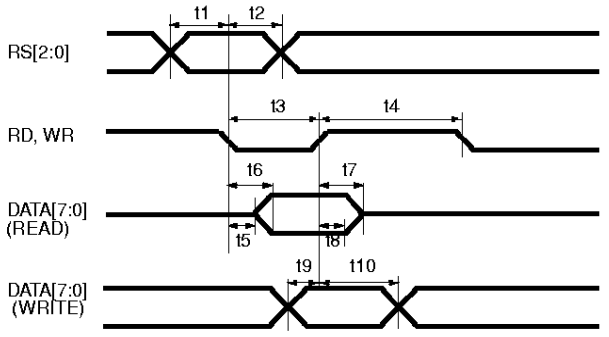

Figure 3. Microprocessor Interface Timing

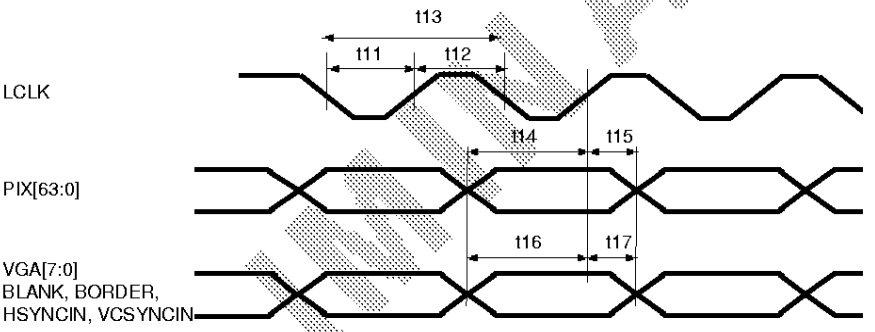

Figure 4. Pixel Data and Video Control Interface Timing

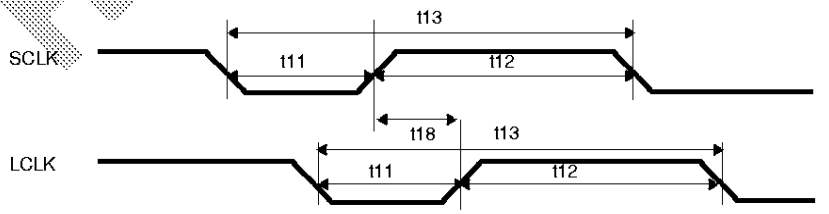

Figure 5. SCLK and LCLK Timing