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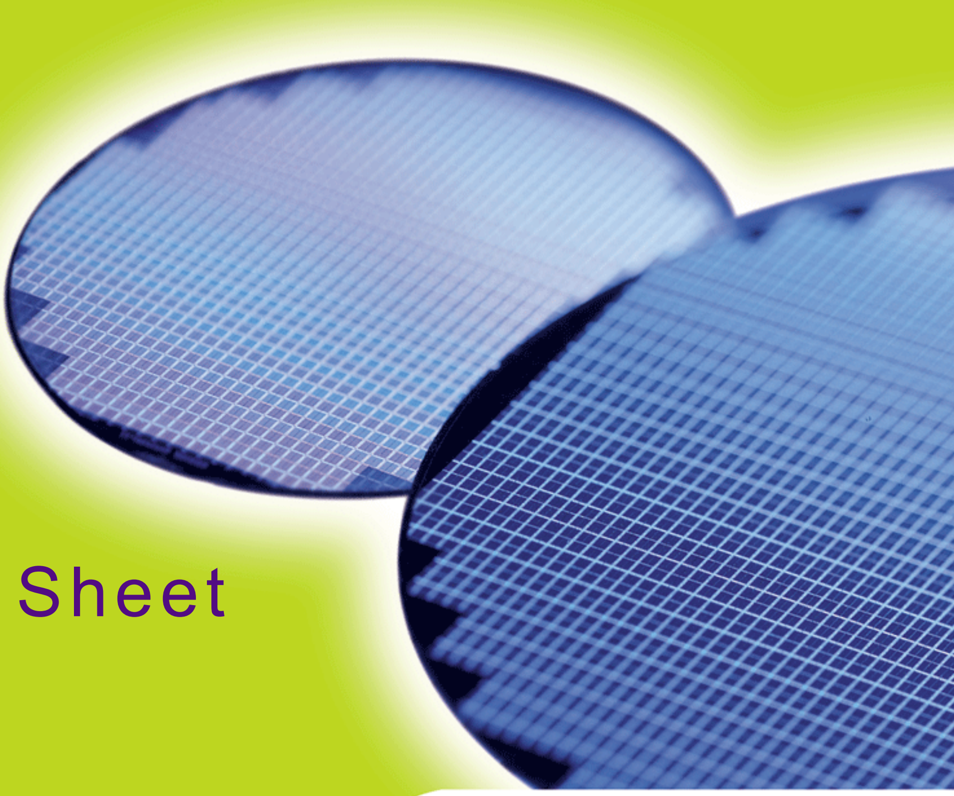
HYS64T128022HM–3S–A
HYS64T128022HM–3.7–A

214-Pin Micro-DIMM-DDR2-SDRAM Modules
MDIMM
DDR2 SDRAM
RoHS Compliant



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1 Overview

This chapter gives an overview of the 1.8 V 214-Pin Micro-DIMM-DDR2-SDRAM Module product family and describes its main characteristics.

1.1 Features

- 214-Pin PC2-5300 and PC2-4200 DDR2 SDRAM memory modules.
- 128M × 64 module organization, and 2 × 64M × 8 chip organization
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Two 512Mbit DDR2 SDRAM dies in a common P-TFBGA-63 package (dual-die)
- Programmable CAS Latencies (3, 4 and 5), Burst Length (8 & 4) and Burst Type
- Burst Refresh, Distributed Refresh and Self Refresh
- All inputs and outputs SSTL_1.8 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E^2PROM
- MDIMM Dimensions (nominal):
  30 mm high, 54.0 mm wide
- 2-piece type Mezzanine Socket with 0,4 mm contact centers
- RoHS Compliant Products[1]

TABLE 1
Performance Table

Product Type Speed Code			**–3S**	**–3.7**	**Unit**
Speed Grade			**PC2–5300 5–5–5**	**PC2–4200 4–4–4**	**—**
Max. Clock Frequency	@CL5	f_{CK5}	333	266	MHz
	@CL4	f_{CK4}	266	266	MHz
	@CL3	f_{CK3}	200	200	MHz
Min. RAS-CAS-Delay		t_{RCD}	15	15	ns
Min. Row Precharge Time		t_{RP}	15	15	ns
Min. Row Active Time		t_{RAS}	45	45	ns
Min. Row Cycle Time		t_{RC}	60	60	ns

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[1] RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

1.2 Description

The QIMONDA HYS64T128022HM–[3S/3.7]–A module family are Unbuffered Micro-DIMM modules “MDIMMs” with 30 mm height based on DDR2 technology. DIMMs are available as non-ECC modules in 128M × 64 (1GB) organization and density, intended for mounting into 214-pin mezzanine connector sockets.

The memory array is designed with 512-Mbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.

TABLE 2
Ordering Informationfor RoHS Compliant Products

Product Type1)	Compliance Code2)	Description	SDRAM Technology
PC2-5300			
HYS64T128022HM–3S–A	1GB 2R×8 PC2–5300M–555–12–ZZ	2 rank, Non-ECC	2 × 512 Mbit (×8))
PC2–4200			
HYS64T128022HM–3.7–A	1GB 2R×8 PC2–4200M–444–12–ZZ	2 rank, Non-ECC	2 × 512 Mbit (×8))

1) All Product Type numbers end with a place code, designating the silicon die revision. Example: HYS64T128022HM–3.7–A, indicating Rev. “A” dies are used for DDR2 SDRAM components. For all QIMONDA DDR2 module and component nomenclature see Chapter 6 of this data sheet.

2) The Compliance Code is printed on the module label and describes the speed grade, for example “PC2–4200M–444–12–ZZ”, where 4200M means Unbuffered Micro-DIMM modules with 4.26 GB/sec Module Bandwidth and “444-11” means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.2 and produced on the Raw Card “Z”.

TABLE 3
Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/columns bits	Raw Card
1 GByte	128M ×64	2	Non-ECC	16	14/2/10	ZZ

TABLE 4
Components on Modules

Product Type[1]	DRAM Components[1]	DRAM Density	DRAM Organisation	Note[2]
HYS64T128022HM	HYB18T512802AF	2× 512 Mbit	2 × 64M ×8	

1) Green Product

2) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

2 Pin Configuration

The pin configuration of the DDR2 SDRAM Micro-DIMM is listed by function in **Table 5** (214 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 6** and **Table 7** respectively. The pin numbering is depicted in **Figure 1**.

TABLE 5
Pin Configuration of MDIMM

Ball No.	Name	Pin Type	Buffer Type	Function
Clock Signals				
122	CK0	I	SSTL	**Clock Signal CK 1:0, Complementary Clock Signal CK 1:0**
194	CK1	I	SSTL	
123	$\overline{\text{CK0}}$	I	SSTL	
195	$\overline{\text{CK1}}$	I	SSTL	
43	CKE0	I	SSTL	**Clock Enables 1:0** *Note: 2-rank module*
147	CKE1	I	SSTL	
	NC	NC		**Not Connected** *Note: 1-rank module*
Control Signals				
165	$\overline{\text{S0}}$	I	SSTL	**Chip Select Rank 1:0** *Note: 2-rank module.*
62	$\overline{\text{S1}}$	I	SSTL	
	NC	NC		**Not Connected** *Note: 1-rank module*
163	$\overline{\text{RAS}}$	I		**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
60	$\overline{\text{CAS}}$	I	SSTL	
56	$\overline{\text{WE}}$	I	SSTL	
Address Signals				
55	BA0	I	SSTL	**Bank Address Bus 1:0**
162	BA1	I	SSTL	
46	BA2	I	SSTL	**Bank Address Bus 2** *Note: Greater than 512Mb DDR2 SDRAMS*
	NC	NC	–	**Not Connected** *Note: Less than 1Gb DDR2 SDRAMS*

Ball No.	Name	Pin Type	Buffer Type	Function
161	A0	I	SSTL	**Address Inputs 12:0, Address Input 10/Autoprecharge**
159	A1	I	SSTL	
52	A2	I	SSTL	
158	A3	I	SSTL	
51	A4	I	SSTL	
50	A5	I	SSTL	
157	A6	I	SSTL	
48	A7	I	SSTL	
155	A8	I	SSTL	
154	A9	I	SSTL	
54	A10	I	SSTL	
	AP	I	SSTL	
47	A11	I	SSTL	
153	A12	I	SSTL	
167	A13	I	SSTL	**Address Input 13** *Note: Modules based on ×4/×8 component*
	NC	NC	–	**Not Connected** *Note: Modules based on ×16 component*
Data Signals				
3	DQ0	I/O	SSTL	**Data Bus 0:38** *Note: Data Input/Output pins*
4	DQ1	I/O	SSTL	
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
109	DQ4	I/O	SSTL	
110	DQ5	I/O	SSTL	
114	DQ6	I/O	SSTL	
115	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
13	DQ9	I/O	SSTL	**Data Bus 0:38** *Note: Data Input/Output pins*
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
117	DQ12	I/O	SSTL	
118	DQ13	I/O	SSTL	
125	DQ14	I/O	SSTL	
126	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
128	DQ20	I/O	SSTL	
129	DQ21	I/O	SSTL	
133	DQ22	I/O	SSTL	
134	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
38	DQ26	I/O	SSTL	
39	DQ27	I/O	SSTL	
136	DQ28	I/O	SSTL	
137	DQ29	I/O	SSTL	
142	DQ30	I/O	SSTL	
143	DQ31	I/O	SSTL	
67	DQ32	I/O	SSTL	
68	DQ33	I/O	SSTL	
73	DQ34	I/O	SSTL	
74	DQ35	I/O	SSTL	
174	DQ36	I/O	SSTL	
175	DQ37	I/O	SSTL	
179	DQ38	I/O	SSTL	
180	DQ39	I/O	SSTL	**Data Bus 39:57**
76	DQ40	I/O	SSTL	
77	DQ41	I/O	SSTL	
81	DQ42	I/O	SSTL	
82	DQ43	I/O	SSTL	
182	DQ44	I/O	SSTL	
183	DQ45	I/O	SSTL	
188	DQ46	I/O	SSTL	
189	DQ47	I/O	SSTL	
84	DQ48	I/O	SSTL	

Ball No.	**Name**	**Pin Type**	**Buffer Type**	**Function**
85	DQ49	I/O	SSTL	**Data Bus 39:57**
92	DQ50	I/O	SSTL	
93	DQ51	I/O	SSTL	
191	DQ52	I/O	SSTL	
192	DQ53	I/O	SSTL	
200	DQ54	I/O	SSTL	
201	DQ55	I/O	SSTL	
95	DQ56	I/O	SSTL	
96	DQ57	I/O	SSTL	
101	DQ58	I/O	SSTL	
102	DQ59	I/O	SSTL	
203	DQ60	I/O	SSTL	
204	DQ61	I/O	SSTL	
208	DQ62	I/O	SSTL	
209	DQ63	I/O	SSTL	
7	DQS0	I/O	SSTL	**Data Strobes 7:0**
6	$\overline{\text{DQS0}}$	I/O	SSTL	
19	DQS1	I/O	SSTL	
18	$\overline{\text{DQS1}}$	I/O	SSTL	
28	DQS2	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
140	DQS3	I/O	SSTL	
139	$\overline{\text{DQS3}}$	I/O	SSTL	
71	DQS4	I/O	SSTL	
70	$\overline{\text{DQS4}}$	I/O	SSTL	
186	DQS5	I/O	SSTL	
185	$\overline{\text{DQS5}}$	I/O	SSTL	
198	DQS6	I/O	SSTL	
197	$\overline{\text{DQS6}}$	I/O	SSTL	
99	DQS7	I/O	SSTL	
98	$\overline{\text{DQS7}}$	I/O	SSTL	
112	DM0	I	SSTL	**Data Masks 7:0** *Note: ×8 based module*
120	DM1	I	SSTL	
131	DM2	I	SSTL	
36	DM3	I	SSTL	
177	DM4	I	SSTL	
79	DM5	I	SSTL	
90	DM6	I	SSTL	
206	DM7	I	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
EEPROM				
105	SCL	I	CMOS	**Serial Bus Clock**
104	SDA	I/O	OD	**Serial Bus Data**
211	SA0	I	CMOS	**Serial Address Select Bus 1:0**
213	SA1	I	CMOS	
Power Supplies				
1	V_{REF}	AI	–	**I/O Reference Voltage**
42, 45, 49, 53, 57, 61, 64, 146, 149, 152, 156, 160, 164, 168, 171	V_{DD}	PWR	–	**Power Supply**
107	V_{DDSPD}	PWR	–	**EEPROM Power Supply**
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 37, 40, 66, 69, 72, 75, 78, 80, 83, 86, 89, 91, 94, 97, 100, 103, 108, 111, 113, 116, 119, 121, 124, 127, 130, 132, 135, 138, 141, 144, 173, 176, 178, 181, 184, 187, 190, 193, 196, 205, 199, 202, 207, 210	V_{SS}	GND	–	**Ground Plane**
Other Pins				
166	ODT0	I	SSTL	**On-Die Termination Control 1:0** *Note: 2-rank module*
63	ODT1	I	SSTL	**On-Die Termination Control 1:0** *Note: 2-rank module*
	NC			**Not Connected** *Note: 1-rank module*
15, 16, 41, 44, 46, 58, 59, 65, 87, 88, 106, 145, 148, 150, 151, 167, 169, 170, 172, 212, 214	NC	NC		**Not connected**

TABLE 6
Abbreviations for Pin Type

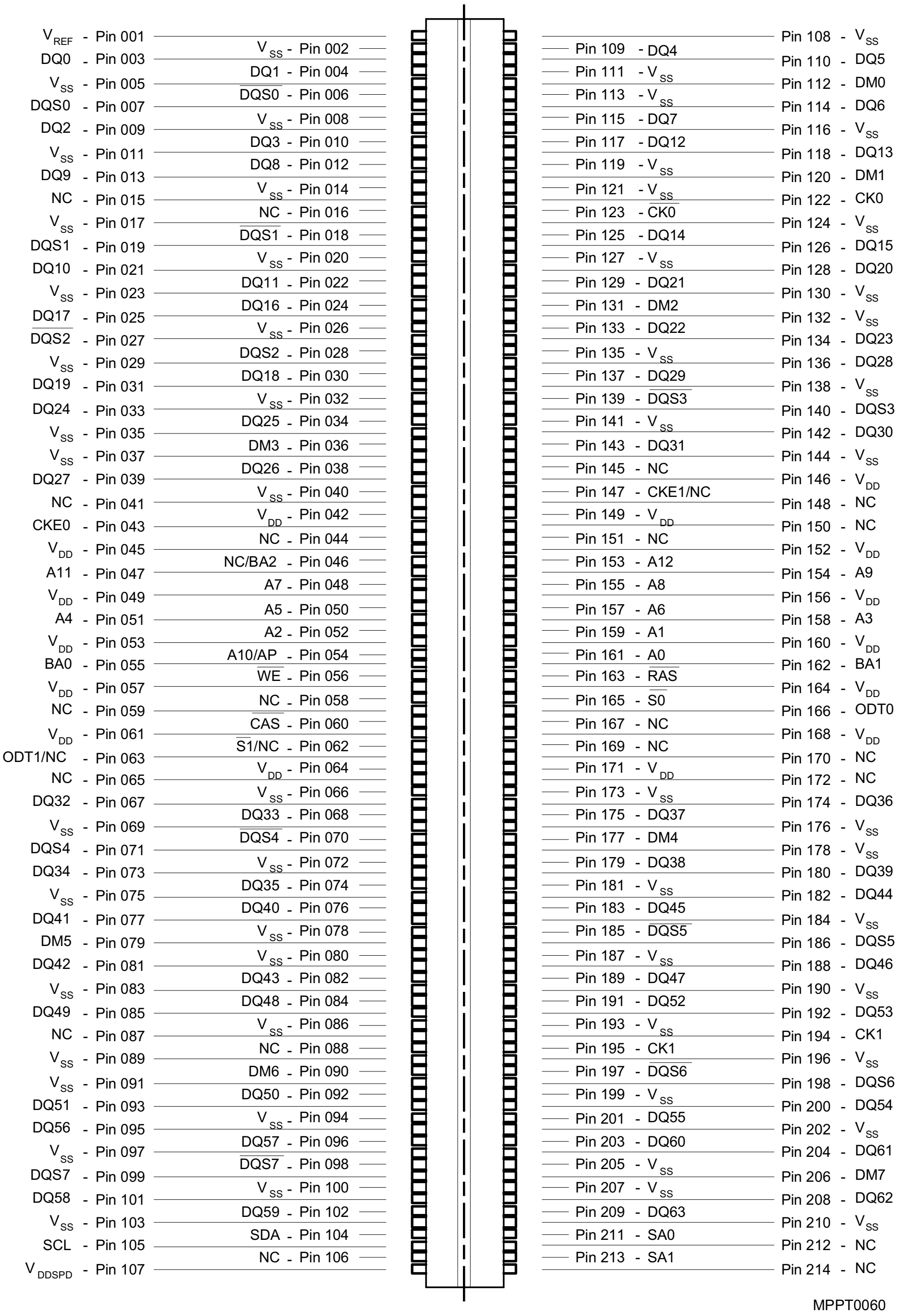
Abbreviation	**Description**
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 7
Abbreviations for Buffer Type

Abbreviation	**Description**
SSTL	Serial Stub Terminated Logic (SSTL_18)
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

FIGURE 1

Pin Configuration for Two-Piece Mezzanine Socket on MDIMM (214 pins)



3 Electrical Characteristics

This chapter lists the electrical characteristics.

3.1 Absolute Maximum Ratings

Caution is needed not to exceed absolute maximum ratings of the DRAM device listed in **Table 8** at any time.

TABLE 8
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–1.0	+2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.5	+2.3	V	1)2)
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	–0.5	+2.3	V	1)2)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.5	+2.3	V	1)
T_{STG}	Storage Temperature	–55	+100	°C	1)2)

1) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

Attention:** **Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 9
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{OPER}	Operating Temperature	0	95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3) Above 85 °C the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs
4) When operating this product in the 85 °C to 95 °C TCASE temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%

3.2 DC Operating Conditions

This chapter contains the DC operating conditions tables.

TABLE 10
Operating Conditions

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	0	+65	°C	
DRAM Case Temperature	T_{CASE}	0	+95	°C	1)2)3)4)
Storage Temperature	T_{STG}	– 50	+100	°C	
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	

1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.
2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported
3) Above 85 °C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs
4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%.
5) Up to 3000 m.

TABLE 11
Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	
DC Input Logic High	$V_{IH(DC)}$	$V_{REF} + 0.125$	—	$V_{DDQ} + 0.3$	V	
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	—	$V_{REF} - 0.125$	V	
In / Output Leakage Current	I_L	– 5	—	5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2) Peak to AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise in V_{DDQ}.
3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin

3.3 Timing Characteristics

This chapter describes the AC characteristics.

3.3.1 Speed Grade Definitions

This chapter contains the Speed Grade Definition tables.

TABLE 12
Speed Grade Definition Speed Bins for DDR2–667D

Speed Grade			**DDR2–667D**		**Unit**	**Note**
QAG Sort Name			**–3S**			
CAS-RCD-RP latencies			**5–5–5**		t_{CK}	
Parameter		**Symbol**	**Min.**	**Max.**	**—**	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0)

2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode

3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.

4) The output timing reference voltage level is V_{TT}.

5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

TABLE 13
Speed Grade Definition Speed Bins for DDR2–533C

Speed Grade			**DDR2–533C**		**Unit**	**Note**
QAG Sort Name			**–3.7**			
CAS-RCD-RP latencies			**4–4–4**		t_{CK}	
Parameter		**Symbol**	**Min.**	**Max.**	**—**	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3.75	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	ns	1)2)3)4)

Speed Grade		**DDR2–533C**		**Unit**	**Note**
QAG Sort Name		**–3.7**			
CAS-RCD-RP latencies		**4–4–4**		t_{CK}	
Parameter	**Symbol**	**Min.**	**Max.**	**—**	
RAS-CAS-Delay	t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time	t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{\text{CK}}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0)

2) The CK/$\overline{\text{CK}}$ input reference level (for timing reference to CK/$\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross. The DQS / $\overline{\text{DQS}}$, RDQS / $\overline{\text{RDQS}}$, input reference level is the crosspoint when in differential strobe mode.

3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.

4) The output timing reference voltage level is V_{TT}.

5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

3.3.2 Component AC Timing Parameters

This chapter contains the AC Timing Parameters.

TABLE 14
DRAM Component Timing Parameter by Speed Grade - DDR2–667

Parameter	**Symbol**	**DDR2–667**		**Unit**	**Note** 1)2)3)4)5)6)7)8)
		Min.	**Max.**		
DQ output access time from CK / $\overline{\text{CK}}$	t_{AC}	–450	+450	ps	9)
CAS to CAS command delay	t_{CCD}	2	—	nCK	
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock period	$t_{CK.AVG}$	3000	8000	ps	
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	—	nCK	12)
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{nRP}	—	nCK	13)14)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + $t_{CK .AVG}$ + t_{IH}	—	ns	
DQ and DM input hold time	$t_{DH.BASE}$	175	—	ps	19)20)15)
DQ and DM input pulse width for each input	t_{DIPW}	0.35	—	$t_{CK.AVG}$	
DQS output access time from CK / $\overline{\text{CK}}$	t_{DQSCK}	–400	+400	ps	9)
DQS input high pulse width	t_{DQSH}	0.35	—	$t_{CK.AVG}$	
DQS input low pulse width	t_{DQSL}	0.35	—	$t_{CK.AVG}$	
DQS-DQ skew for DQS & associated DQ signals	t_{DQSQ}	—	240	ps	16)
DQS latching rising transition to associated clock edges	t_{DQSS}	– 0.25	+ 0.25	$t_{CK.AVG}$	17)
DQ and DM input setup time	$t_{DS.BASE}$	100	—	ps	18)19)20)
DQS falling edge hold time from CK	t_{DSH}	0.2	—	$t_{CK.AVG}$	17)

Parameter	**Symbol**	**DDR2–667**		**Unit**	**Note** 1)2)3)4)5)6)7)8)
		Min.	**Max.**		
DQS falling edge to CK setup time	t_{DSS}	0.2	—	$t_{\text{CK.AVG}}$	17)
CK half pulse width	t_{HP}	Min($t_{\text{CH.ABS}}$, $t_{\text{CL.ABS}}$)	—	ps	21)
Data-out high-impedance time from CK / $\overline{\text{CK}}$	t_{HZ}	—	$t_{\text{AC.MAX}}$	ps	9)22)
Address and control input hold time	$t_{\text{IH.BASE}}$	275	—	ps	25)23)
Control & address input pulse width for each input	t_{IPW}	0.6	—	$t_{\text{CK.AVG}}$	
Address and control input setup time	$t_{\text{IS.BASE}}$	200	—	ps	24)25)
DQ low impedance time from CK/$\overline{\text{CK}}$	$t_{\text{LZ.DQ}}$	2 × $t_{\text{AC.MIN}}$	$t_{\text{AC.MAX}}$	ps	9)22)
DQS/$\overline{\text{DQS}}$ low-impedance time from CK / $\overline{\text{CK}}$	$t_{\text{LZ.DQS}}$	$t_{\text{AC.MIN}}$	$t_{\text{AC.MAX}}$	ps	9)22)
MRS command to ODT update delay	t_{MOD}	0	12	ns	1)
Mode register set command cycle time	t_{MRD}	2	—	nCK	
OCD drive mode output delay	t_{OIT}	0	12	ns	1)
DQ/DQS output hold time from DQS	t_{QH}	$t_{\text{HP}} - t_{\text{QHS}}$	—	ps	26)
DQ hold skew factor	t_{QHS}	—	340	ps	27)
Read preamble	t_{RPRE}	0.9	1.1	$t_{\text{CK.AVG}}$	28)29)
Read postamble	t_{RPST}	0.4	0.6	$t_{\text{CK.AVG}}$	28)30)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	1)
Write preamble	t_{WPRE}	0.35	—	$t_{\text{CK.AVG}}$	
Write postamble	t_{WPST}	0.4	0.6	$t_{\text{CK.AVG}}$	
Write recovery time	t_{WR}	15	—	ns	1)
Internal write to read command delay	t_{WTR}	7.5	—	ns	1)31)
Exit power down to read command	t_{XARD}	2	—	nCK	
Exit active power-down mode to read command (slow exit, lower power)	t_{XARDS}	7 – AL	—	nCK	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	nCK	
Exit self-refresh to a non-read command	t_{XSNR}	t_{RFC} +10	—	ns	1)
Exit self-refresh to read command	t_{XSRD}	200	—	nCK	
Write command to DQS associated clock edges	WL	RL–1		nCK	

1) For details and notes see the relevant Qimonda component data sheet

2) V_{DDQ} = 1.8 V ± 0.1V; V_{DD} = 1.8 V ± 0.1 V. See notes 5)6)7)8)

3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

4) Timings are guaranteed with CK/$\overline{\text{CK}}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.

5) The CK / $\overline{\text{CK}}$ input reference level (for timing reference to CK / $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross. The DQS / $\overline{\text{DQS}}$, RDQS / $\overline{\text{RDQS}}$, input reference level is the crosspoint when in differential strobe mode.

6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.

7) The output timing reference voltage level is V_{TT}.

8) New units, '$t_{\text{CK.AVG}}$' and 'nCK', are introduced in DDR2–667 and DDR2–800. Unit '$t_{\text{CK.AVG}}$' represents the actual $t_{\text{CK.AVG}}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2–400 and DDR2–533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 x $t_{\text{CK.AVG}}$ + $t_{\text{ERR.2PER(Min)}}$.

9) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{\text{ERR(6-10per)}}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{\text{ERR(6-10PER).MIN}}$ = – 272 ps and $t_{\text{ERR(6- 10PER).MAX}}$ = + 293 ps, then $t_{\text{DQSCK.MIN(DERATED)}}$ = $t_{\text{DQSCK.MIN}}$ – $t_{\text{ERR(6-10PER).MAX}}$ = – 400 ps – 293 ps = – 693 ps and $t_{\text{DQSCK.MAX(DERATED)}}$ = $t_{\text{DQSCK.MAX}}$ – $t_{\text{ERR(6-10PER).MIN}}$ = 400 ps + 272 ps = + 672 ps. Similarly, $t_{\text{LZ.DQ}}$ for DDR2–667 derates to $t_{\text{LZ.DQ.MIN(DERATED)}}$ = - 900 ps – 293 ps = – 1193 ps and $t_{\text{LZ.DQ.MAX(DERATED)}}$ = 450 ps + 272 ps = + 722 ps. (Caution on the MIN/MAX usage!)

10) Input clock jitter spec parameter. These parameters are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2–667 and DDR2–800 only. The jitter specified is a random jitter meeting a Gaussian distribution.

11) These parameters are specified per their average values, however it is understood that the relationship between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations).

12) $t_{\text{CKE.MIN}}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.

13) DAL = WR + RU{t_{RP}(ns) / t_{CK}(ns)}, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For t_{RP}, if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period. Example: For DDR2–533 at t_{CK} = 3.75 ns with t_{WR} programmed to 4 clocks. t_{DAL} = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.

14) $t_{\text{DAL.nCK}}$ = WR [nCK] + $t_{\text{nRP.nCK}}$ = WR + RU{t_{RP} [ps] / $t_{\text{CK.AVG}}$[ps] }, where WR is the value programmed in the EMR.

15) Input waveform timing t_{DH} with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{\text{IH.DC}}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{\text{IL.DC}}$ level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{\text{IL.DC.MAX}}$ and $V_{\text{IH.DC.MIN}}$. See **Figure 3**.

16) t_{DQSQ}: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.

17) These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{\text{DQS}}$) crossing to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{\text{JIT.PER}}$, $t_{\text{JIT.CC}}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

18) Input waveform timing t_{DS} with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{\text{IH.AC}}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{\text{IL.AC}}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{\text{il(DC)MAX}}$ and $V_{\text{ih(DC)MIN}}$. See **Figure 3**.

19) If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

20) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS / $\overline{\text{DQS}}$) crossing.

21) t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for t_{QH} calculation is determined by the following equation; t_{HP} = MIN ($t_{\text{CH.ABS}}$, $t_{\text{CL.ABS}}$), where, $t_{\text{CH.ABS}}$ is the minimum of the actual instantaneous clock high time; $t_{\text{CL.ABS}}$ is the minimum of the actual instantaneous clock low time.

22) t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}) .

23) Input waveform timing is referenced from the input signal crossing at the $V_{\text{IL.DC}}$ level for a rising signal and $V_{\text{IH.DC}}$ for a falling signal applied to the device under test. See **Figure 4**.

24) Input waveform timing is referenced from the input signal crossing at the $V_{\text{IH.AC}}$ level for a rising signal and $V_{\text{IL.AC}}$ for a falling signal applied to the device under test. See **Figure 4**.

25) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{\text{JIT.PER}}$, $t_{\text{JIT.CC}}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

26) t_{QH} = t_{HP} – t_{QHS}, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.} Examples: 1) If the system provides t_{HP} of 1315 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 975 ps minimum. 2) If the system provides t_{HP} of 1420 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 1080 ps minimum.

27) t_{QHS} accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.

28) t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). **Figure 2** shows a method to calculate these points when the device is no longer driving (t_{RPST}), or begins driving (t_{RPRE}) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

29) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.PER}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.PER.MIN}$ = – 72 ps and $t_{JIT.PER.MAX}$ = + 93 ps, then $t_{RPRE.MIN(DERATED)} = t_{RPRE.MIN} + t_{JIT.PER.MIN}$ = 0.9 x $t_{CK.AVG}$ – 72 ps = + 2178 ps and $t_{RPRE.MAX(DERATED)} = t_{RPRE.MAX} + t_{JIT.PER.MAX}$ = 1.1 x $t_{CK.AVG}$ + 93 ps = + 2843 ps. (Caution on the MIN/MAX usage!).

30) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.DUTY}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.DUTY.MIN}$ = – 72 ps and $t_{JIT.DUTY.MAX}$ = + 93 ps, then $t_{RPST.MIN(DERATED)} = t_{RPST.MIN} + t_{JIT.DUTY.MIN}$ = 0.4 x $t_{CK.AVG}$ – 72 ps = + 928 ps and $t_{RPST.MAX(DERATED)} = t_{RPST.MAX} + t_{JIT.DUTY.MAX}$ = 0.6 x $t_{CK.AVG}$ + 93 ps = + 1592 ps. (Caution on the MIN/MAX usage!).

31) t_{WTR} is at lease two clocks (2 x t_{CK}) independent of operation frequency.

FIGURE 2
Method for calculating transitions and endpoint

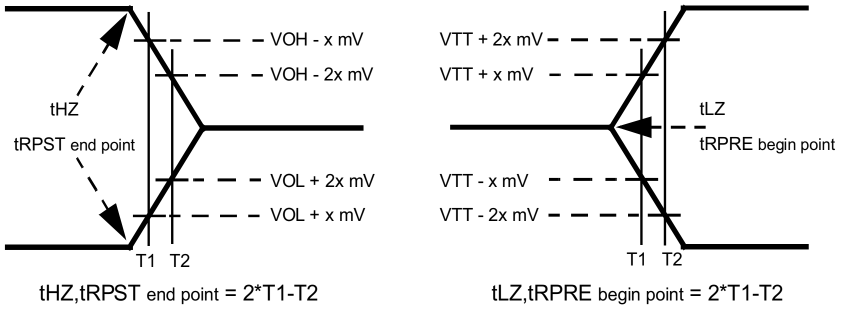


FIGURE 3
Differential input waveform timing - t_{DS} and t_{DS}

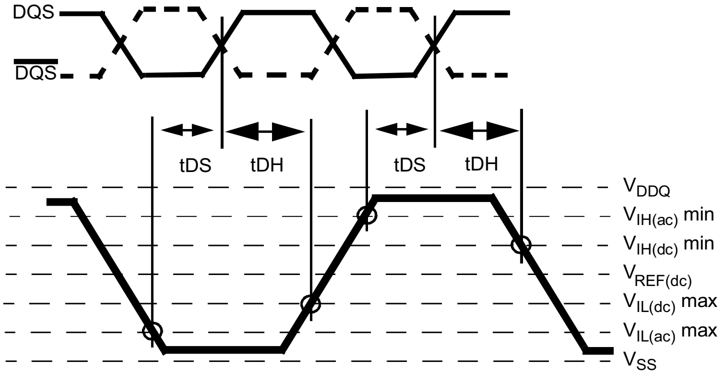


FIGURE 4
Differential input waveform timing - t_{IS} and t_{IH}

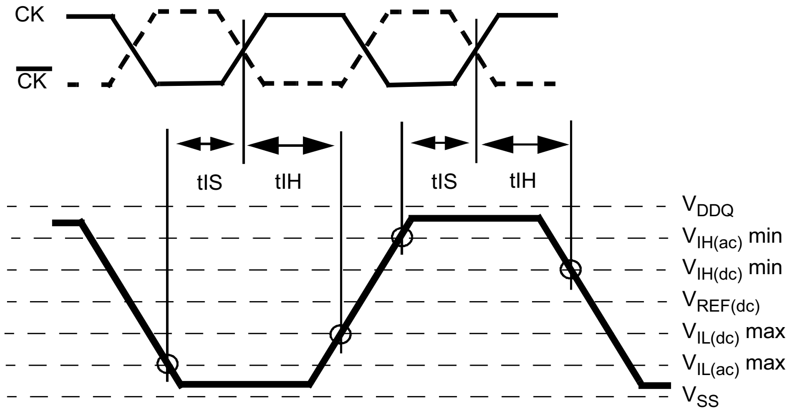


TABLE 15
DRAM Component Timing Parameter by Speed Grade - DDR2–533

Parameter	Symbol	DDR2–533		Unit	Note 1)2)3)4)5)6)7)
		Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	t_{AC}	–500	+500	ps	
$\overline{\text{CAS}}$ A to $\overline{\text{CAS}}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{\text{CK}}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{\text{CK}}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	8)18)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	9)
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	225	—	ps	10)
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	11)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{\text{CK}}$	t_{DQSCK}	–450	+450	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	ps	11)
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	ps	11)
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	11)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. ($t_{CL,}$ t_{CH})			12)
Data-out high-impedance time from CK / $\overline{\text{CK}}$	t_{HZ}	—	$t_{AC.MAX}$	ps	13)
Address and control input hold time	t_{IH}(base)	375	—	ps	11)
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	250	—	ps	11)
DQ low-impedance time from CK / $\overline{\text{CK}}$	$t_{LZ(DQ)}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
DQS low-impedance from CK / $\overline{\text{CK}}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—		
Data hold skew factor	t_{QHS}	—	400	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	14)15)

Parameter	**Symbol**	**DDR2–533**		**Unit**	**Note** 1)2)3)4)5)6)7)
		Min.	**Max.**		
Average periodic refresh Interval	t_{REFI}	—	3.9	µs	16)18)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	17)
Precharge-All (4 banks) command period	t_{RP}	$t_{RP} + 1t_{CK}$	—	ns	
Precharge-All (8 banks) command period	t_{RP}	$15 + 1t_{CK}$	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	14)
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	14)
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	14)18)
Active bank A to Active bank B command period	t_{RRD}	10	—	ns	16)22)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.25	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	19)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	20)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	21)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	21)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}	—	t_{CK}	22)

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ±0.1 V. See notes 5)6)7)8)
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS/ $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
10) For timing definition, refer to the Component data sheet.
11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
12) MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).

13) The t_{HZ}, t_{RPST} and t_{LZ}, t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving ($t_{HZ,}$ t_{RPST}), or begins driving ($t_{LZ,}$ t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions.These parameters are verified by design and characterization, but not subject to production test.

14) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.

15) 0 °C≤ $T_{CASE} \leq$ 85 °C

16) 85 °C $<$ $T_{CASE} \leq$ 95 °C

17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.

18) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See **Table 2 “Ordering Informationfor RoHS Compliant Products” on Page 4**.

19) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

20) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.

21) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MR, A12 = “0”) a fast power-down exit timing t_{XARD} can be used. In “low active power-down mode” (MR, A12 =”1”) a slow power-down exit timing t_{XARDS} has to be satisfied.

22) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.

3.3.3 ODT AC Electrical Characteristics

This chapter contains the ODT AC electrical characteristic tables.

TABLE 16

ODT AC Character. and Operating Conditions for DDR2-667

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	nCK	1)
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7 ns	ns	1)2)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	1)
t_{AOFD}	ODT turn-off delay	2.5	2.5	nCK	1)
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	1)3)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	1)
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	nCK	1)
t_{AXPD}	ODT Power Down Exit Latency	8	—	nCK	1)

1) New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2-667 and DDR2-800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 × $t_{CK.AVG}$+ $t_{EPR.2PER(MIN)}$.

2) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted differently per speed bin. For DDR2-667/800, t_{AOND} is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

3) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-667/800,if $t_{CK.AVG}$ = 3 ns is assumed, t_{AOFD}= 1.5 ns (0.5 × 3 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edge.

TABLE 17

ODT AC Character. and Operating Conditions for DDR2-533

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 1 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted differently per speed bin. For DDR2-400/533, t_{AOND} is 10 ns (= 2 x 5 ns) after the clock edge that registered a first ODT HIGH if t_{CK} = 5 ns.

2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-400/533, t_{AOFD} is 12.5 ns (= 2.5 x 5 ns) after the clock edge that registered a first ODT HIGH if t_{CK} = 5 ns.

3.4 I_{DD} Specifications and Conditions

This chapter describes the I_{DD} Specifications and Conditions.

TABLE 18
I_{DD} Measurement Conditions

Parameter	**Symbol**	**Note** 1)2)3)4)5)
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}	
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = CL_{MIN}; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}	6)
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD2N}	
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}	
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}	
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$	
Operating Current - Burst Read All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CKMIN}$; $t_{RAS} = t_{RASMAX}$; $t_{RP} = t_{RPMIN}$; CKE is HIGH, CS is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; I_{OUT} = 0mA.	I_{DD4R}	6)
Operating Current - Burst Write All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}	
Burst Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}	

Parameter	Symbol	Note 1)2)3)4)5)
Distributed Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}	
Self-Refresh Current CKE $\leq$ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}	
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}	6)

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
3) Definitions for I_{DD} see **Table 19**
4) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P}
5) For details and notes see the relevant Qimonda component data sheet
6) I_{DD1}, I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled (I_{OUT} = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

TABLE 19
Definitions for I_{DD}

Parameter	Description
LOW	$V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	Inputs are stable at a HIGH or LOW level
FLOATING	Inputs are $V_{REF} = V_{DDQ}$ /2
SWITCHING	Inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes

TABLE 20
I_{DD} Specification for HYS64T128022HM–[3S/3.7]–A

Product Type	**HYS64T128022HM–3S–A**	**HYS64T128022HM–3.7–A**	**Unit**	**Note**[1]
Organization	**1 GB**	**1 GB**		
	×**64**	×**64**		
	2 Ranks	**2 Ranks**		
	–3S	**–3.7**		
Symbol	**Max.**	**Max.**		
I_{DD0}	608	552	mA	[2]
I_{DD1}	720	632	mA	[2]
I_{DD2N}	800	640	mA	[3]
I_{DD2P}	80	64	mA	[3]
I_{DD2Q}	640	480	mA	[3]
I_{DD3N}	800	640	mA	[3]
$I_{DD3P\_0 \text{ (fast)}}$	304	256	mA	[3][4]
$I_{DD3P\_1 \text{ (slow)}}$	96	80	mA	[3][5]
I_{DD4R}	1080	752	mA	[2]
I_{DD4W}	1160	792	mA	[2]
I_{DD5B}	1160	1072	mA	[2]
I_{DD5D}	96	96	mA	[3][6]
I_{DD6}	80	64	mA	[3][6]
I_{DD7}	1216	1155	mA	[2]

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled
2) The other rank is in I_{DD2P} Precharge Power-Down Current mode
3) Both ranks are in the same I_{DD}current mode
4) Fast: MRS(12)=0
5) Slow: MRS(12)=1
6) IDD5D and I_{DD6} values are for $0°C \leq T_{Case} \leq 85°C$

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

TABLE 21
SPD codes for HYS64T128022HM–[3S/3.7]–A

Product Type		**HYS64T128022HM–3S–A**	**HYS64T128022HM–3.7–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×64**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–5300M–555**	**PC2–4200M–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0E	0E
4	Number of Column Addresses	0A	0A
5	DIMM Rank and Stacking Information	71	71
6	Data Width	40	40
7	Not used	00	00
8	Interface Voltage Level	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	3D
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	50
11	Error Correction Support (non-ECC, ECC)	00	00
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	08	08
14	Error Checking SDRAM Width	00	00
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	04	04
18	Supported CAS Latencies	38	38
19	DIMM Mechanical Characteristics	00	00
20	DIMM Type Information	08	08
21	DIMM Attributes	00	00
22	Component Attributes	03	03
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D

Product Type		**HYS64T128022HM–3S–A**	**HYS64T128022HM–3.7–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×64**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–5300M–555**	**PC2–4200M–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D
31	Module Density per Rank	80	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	37
34	$t_{DS.MIN}$ [ns]	10	10
35	$t_{DH.MIN}$ [ns]	17	22
36	$t_{WR.MIN}$ [ns]	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E
39	Analysis Characteristics	00	00
40	t_{RC} and t_{RFC} Extension	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69
43	$t_{CK.MAX}$ [ns]	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	1E
45	$t_{QHS.MAX}$ [ns]	22	28
46	PLL Relock Time	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	53	51
48	Psi(T-A) DRAM	78	78
49	ΔT_0 (DT0)	4B	3F
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	39	2E
51	ΔT_{2P} (DT2P)	26	1E
52	ΔT_{3N} (DT3N)	26	1E
53	$\Delta T_{3P.fast}$ (DT3P fast)	2B	24
54	$\Delta T_{3P.slow}$ (DT3P slow)	1B	17
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	4A	34
56	ΔT_{5B} (DT5B)	20	1E

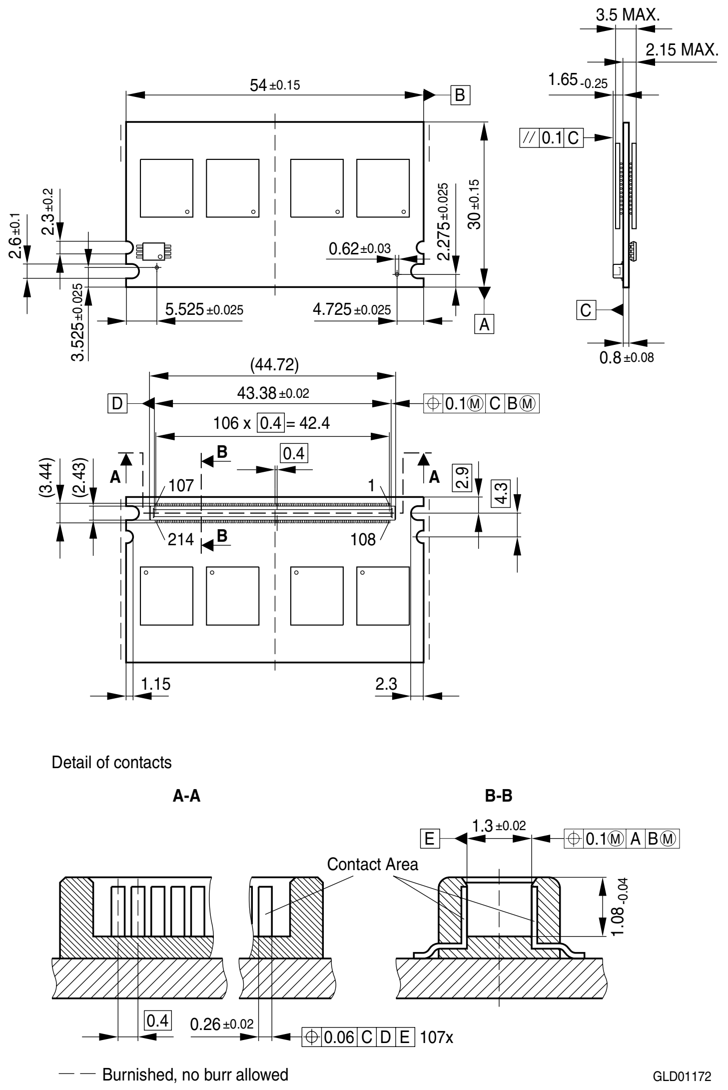
Product Type		**HYS64T128022HM–3S–A**	**HYS64T128022HM–3.7–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×64**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–5300M–555**	**PC2–4200M–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**
57	ΔT_7 (DT7)	22	20
58	Psi(ca) PLL	00	00
59	Psi(ca) REG	00	00
60	ΔT_{PLL} (DTPLL)	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00
62	SPD Revision	12	12
63	Checksum of Bytes 0-62	F4	EA
64	Manufacturer’s JEDEC ID Code (1)	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00
72	Module Manufacturer Location	xx	xx
73	Product Type, Char 1	36	36
74	Product Type, Char 2	34	34
75	Product Type, Char 3	54	54
76	Product Type, Char 4	31	31
77	Product Type, Char 5	32	32
78	Product Type, Char 6	38	38
79	Product Type, Char 7	30	30
80	Product Type, Char 8	32	32
81	Product Type, Char 9	32	32
82	Product Type, Char 10	48	48
83	Product Type, Char 11	4D	4D
84	Product Type, Char 12	33	33
85	Product Type, Char 13	53	2E
86	Product Type, Char 14	41	37
87	Product Type, Char 15	20	41
88	Product Type, Char 16	20	20
89	Product Type, Char 17	20	20

Product Type		**HYS64T128022HM–3S–A**	**HYS64T128022HM–3.7–A**
Organization		**1 GByte**	**1 GByte**
		×**64**	×**64**
		2 Ranks (×**8)**	**2 Ranks (**×**8)**
Label Code		**PC2–5300M–555**	**PC2–4200M–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**
90	Product Type, Char 18	20	20
91	Module Revision Code	2x	3x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95 - 98	Module Serial Number	xx	xx
99 - 127	Not used	00	00
128 - 255	Blank for customer use	FF	FF

5 Package Outlines

This chapter contains the package outlines of the products.

FIGURE 5
Package Outline L-DIM-214-04



Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

6 Product Type Nomenclature

Qimonda’s nomenclature uses simple coding combined with some proprietary coding. **Table 22** provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 23** and for components in **Table 24**.

TABLE 22
Nomenclature Fields and Examples

Example for	**Field Number**										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Micro-DIMM	HYS	64	T	64/128	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512/1G	16		0	A	C	–5	

TABLE 23
DDR2 DIMM Nomenclature

Field	**Description**	**Values**	**Coding**
1	Qimonda Module Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
		F	**F**ully Buffered

Field	Description	Values	Coding
10	Speed Grade	–2.5F	PC2–6400 5–5–5
		–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

TABLE 24
DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	Qimonda Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–25F	DDR2-800 5-5-5
		–2.5	DDR2-800 6-6-6
		–3	DDR2-667 4-4-4
		–3S	DDR2-667 5-5-5
		–3.7	DDR2-533 4-4-4
		–5	DDR2-400 3-3-3

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