ADVANCED INFORMATION

DESCRIPTION:

The DPD16ML36PL5 and the DPD16ML36PW5 are the Low Profile 16 Meg x 36 Dynamic RAM module in the family of ***SuperSIMM***™ modules that utilize the new and innovative space saving TSOP stacking technology. The module is constructed of eight dynamic RAM stacks surface mounted on an industry standard 72-pin SIMM and ZIP substrates and, with eight stacks consisting of four 16 Meg x 1 Dynamic RAM's.

The DPD16ML36PL5/DPD16ML36PW5 provides for a compatible upgrade path from lower density JEDEC compatible modules. The module features high speed access times, common data inputs and outputs, Fully Buffered Address and Write Enable, $\overline{RAS}$, $\overline{CAS}$ and power decoupling capacitors.

FEATURES:

- Access Times:
  70, 80, 100ns (max.)
- Single 5V (±5%) Supply
- Common Data Inputs and Outputs
- Fast Page Mode Capability
- 4096 Cycles / 64 ms
- 3 variations of Refresh:
  - $\overline{RAS}$ only Refresh
  - $\overline{CAS}$ before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Packages Available:
  Industry Standard 72-Pin SIMM
  Industry Standard 72-Pin ZIP

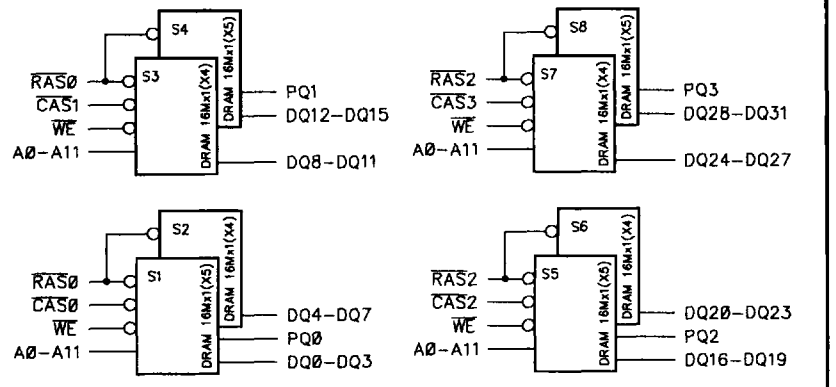
PIN NAMES	
A0 - A11	Row Address: A0 - A11 Column Address: A0 - A11 Refresh Address: A0 - A11
DQ0 - DQ31	Data In / Data Out
PQ0 - PQ3	Parity Data In / Data Out
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobes
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Enables
$\overline{WE}$	Read / Write Enable
V_{DD}	Power Supply (+5V)
V_{SS}	Ground
PD1 - PD4	Presence Detect Pin
N.C.	No Connect

PIN-OUT DIAGRAM

TOP VIEW

INDEX	→		1	VSS
DQ0	2		3	DQ16
DQ1	4		5	DQ17
DQ2	6		7	DQ18
DQ3	8		9	DQ19
VDD	10		11	N.C.
A0	12		13	A1
A2	14		15	A3
A4	16		17	A5
A6	18		19	A10
DQ4	20		21	DQ20
DQ5	22		23	DQ21
DQ6	24		25	DQ22
DQ7	26		27	DQ23
A7	28		29	A11
VDD	30		31	A8
A9	32		33	N.C.
$\overline{RAS2}$	34		35	PQ2
PQ0	36			
			37	PQ1
PQ3	38		39	VSS
$\overline{CAS0}$	40		41	$\overline{CAS2}$
$\overline{CAS3}$	42		43	$\overline{CAS1}$
$\overline{RAS0}$	44		45	N.C.
N.C.	46		47	$\overline{WE}$
N.C.	48		49	DQ8
DQ24	50		51	DQ9
DQ25	52		53	DQ10
DQ26	54		55	DQ11
DQ27	56		57	DQ12
DQ28	58		59	VDD
DQ29	60		61	DQ13
DQ30	62		63	DQ14
DQ31	64		65	DQ15
PD2	66		67	PD1
PD4	68		69	PD3
N.C.	70		71	N.C.
VSS	72			

FUNCTIONAL BLOCK DIAGRAM



ADVANCED INFORMATION

ABSOLUTE MAXIMUM RATINGS			
Symbol	Parameter	Value	Units
T_{STC}	Storage Temperature	-55 to +150	°C
$V_{I/O}$	Voltage on Any Pin	-1.0 to +7.0	V
V_{DD}	V_{DD} Supply Voltage	-1.0 to +7.0	V
I_{OUT}	Output Current	50	mA

CAPACITANCE: t_A = 25°C, f = 1MHz				
Symbol	Parameter	Max	Unit	Condition
C_{ADR}	Address Input	30	pF	V_{IN} = 0V
C_{CAS}	$\overline{CAS}$ Input	80		
C_{RAS}	$\overline{RAS}$ Input	145		
C_{WE}	Write Enable	30		
$C_{I/O}$	Data Input/Output	30		

PRESENCE DETECT PINS			
PIN	70ns	80ns	100ns
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	OPEN	OPEN	OPEN
PD3	V_{SS}	OPEN	V_{SS}
PD4	OPEN	V_{SS}	V_{SS}

OUTPUT LOAD		
Load	CL	Parameters Measured
1	100pF	except t_{CLZ}
2	5pF	t_{CLZ}

RECOMMENDED OPERATING CONDITIONS					
Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IL}	Input Low Voltage	-1.0		0.8	V
V_{IH}	Input High Voltage	2.4		V_{DD}+1.0	V
T_A	Operating Temperature	0	+25	+70	°C

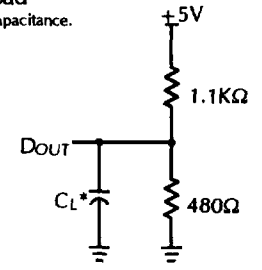
NOTE: All voltages referenced to V_{SS}.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns *
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

* Transition measured between 0.8V and 2.2V.

Figure 1. Output Load

** Including Scope and Jig Capacitance.



DC OPERATING CHARACTERISTICS									
Symbol	Characteristic	Conditions	70ns		80ns		100ns		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	$\overline{CAS}$	-90	90	-90	90	-90	90	µA
		$\overline{RAS}$	-180	180	-180	180	-180	180	µA
		A0 - A11, $\overline{WE}$	-20	20	-20	20	-20	20	
I_{OUT}	Output Leakage Current		-10	10	-10	10	-10	10	µA
I_{CC1}	Operating Current	$\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC} = min.		3240		2880		2560	mA
I_{CC2}	Standby Current	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{IH}		72		72		72	mA
I_{CC3}	$\overline{RAS}$ - Only Refresh Current	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @ t_{RC} = min.		3240		2880		2560	mA
I_{CC4}	FAST-PAGE-MODE Current	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC} = min.		2880		2520		2360	mA
I_{CC5}	Standby Current	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{DD} -0.2V		36		36		36	mA
I_{CC6}	$\overline{CAS}$ - Before - $\overline{RAS}$ Refresh Current	$\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = min.		3240		2880		2560	mA
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -5mA	2.4		2.4		2.4		V

ADVANCED INFORMATION

A.C. OPERATING AND CHARACTERISTICS (V_{DD} = 5.0V±10%, T_A = 0°C to 70°C)

No.	Symbol	Parameter	60ns		70ns		80ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Random Read or Write Cycle Time	110		130		150		ns
2	t_{RAC}	Access Time from $\overline{RAS}$ [3, 4, 9]		60		70		80	ns
3	t_{CAC}	Access Time from $\overline{CAS}$ [3, 4, 9]		15		20		20	ns
4	t_{AA}	Access Time from Column Address [3, 9]		35		40		45	ns
5	t_{CLZ}	$\overline{CAS}$ to Output in LOW-Z [3]	0		0		0		ns
6	t_{OFF}	Output Buffer Turn-Off Delay Time [6]	0	15	0	20	0	20	ns
7	t_T	Transition Time (Rise and Fall) [2]	3	50	3	50	3	50	ns
8	t_{RP}	$\overline{RAS}$ Precharge Time	40		50		60		ns
9	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns
10	t_{RSH}	$\overline{RAS}$ Hold Time	15		20		20		ns
11	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns
12	t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	20	10,000	ns
13	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time [4]	20	45	20	50	20	60	ns
14	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time [9]	15	30	15	35	15	40	ns
15	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns
16	t_{ASR}	Row Address Setup Time	0		0		0		ns
17	t_{RAH}	Row Address Hold Time	10		10		10		ns
18	t_{ASC}	Column Address Setup Time	0		0		0		ns
19	t_{CAH}	Column Address Hold Time	10		15		15		ns
20	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$ [12]	50		55		60		ns
21	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		ns
22	t_{RCS}	Read Command Setup Time	0		0		0		ns
23	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$ [7]	0		0		0		ns
24	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns
25	t_{WCH}	Write Command Hold Time	10		15		15		ns
26	t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$ [12]	55		60		60		ns
27	t_{WP}	Write Command Pulse Width	10		15		15		ns
28	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	55		20		20		ns
29	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		20		ns
30	t_{DS}	Data-In Setup Time [8]	0		0		0		ns
31	t_{DH}	Data-In Hold Time [8]	10		15		15		ns
32	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$ [12]	55		60		60		ns
33	t_{REF}	Refresh Period		64		64		64	ms
34	t_{WCS}	Write Command Setup Time	0		0		0		ns
35	t_{CSR}	$\overline{CAS}$ Setup Time (C-B-R Refresh)	10		10		10		ns

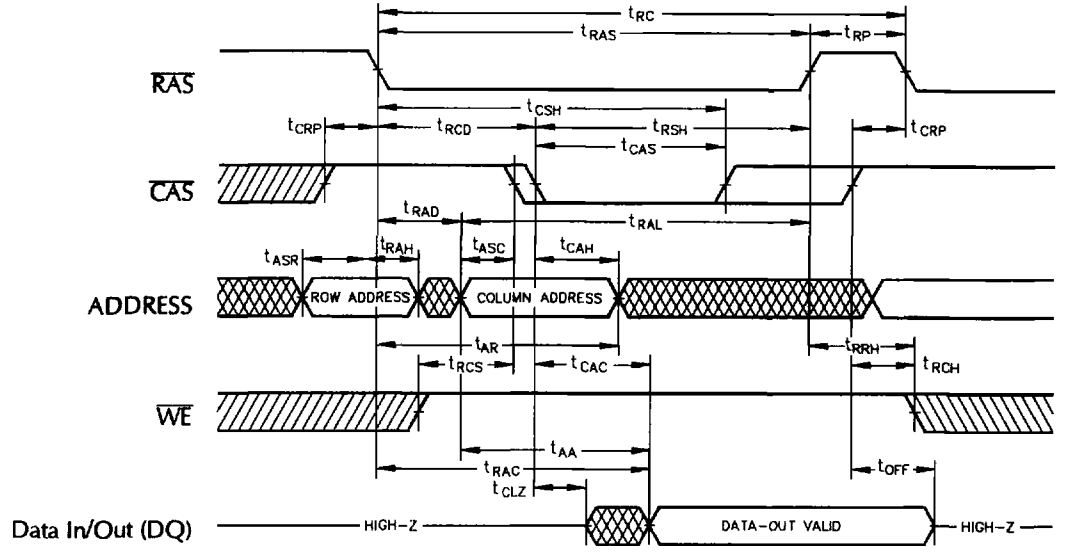
A.C. OPERATING AND CHARACTERISTICS (V_{DD} = 5.0V±10%, T_A = 0°C to 70°C) (Continued)

No.	Symbol	Parameter	60ns		70ns		80ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
36	t_{CHR}	$\overline{CAS}$ Hold Time (C-B-R Refresh)	15		15		15		ns
37	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Percharge Time	5		5		5		ns
38	t_{CPA}	Access Time from $\overline{CAS}$ Precharge [3]		35		40		45	ns
39	t_{PC}	FAST - PAGE - MODE Cycle Time	40		45		50		ns
40	t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Cycle)	10		10		10		ns
41	t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Cycle)	60	200,000	70	200,000	80	200,000	ns
42	t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35		40		45		
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (C-B-R Refresh)	10		10		10		ns
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time (C-B-R Refresh)	10		10		10		ns
45	t_{RASS}	$\overline{RAS}$ Pulse Width (C-B-R Refresh) [11]	100		100		100		µs
46	t_{RPS}	$\overline{RAS}$ Precharge Time (C-B-R Refresh) [11]	110		130		150		ns
47	t_{CHS}	$\overline{CAS}$ Hold Time (C-B-R Refresh) [11]	-50		-50		-50		ns

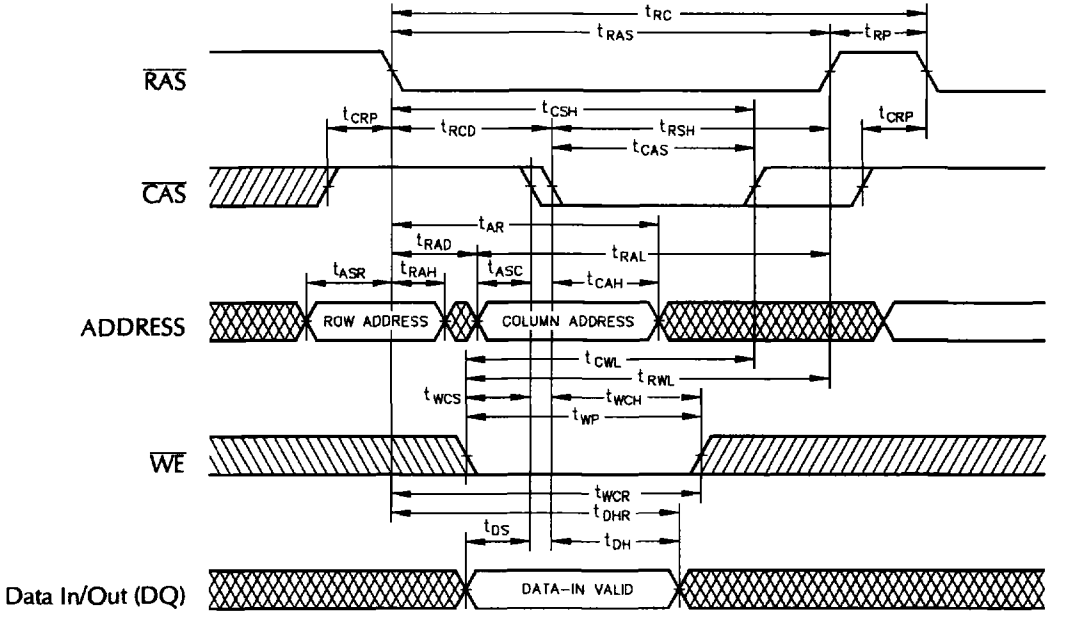
NOTES:

1. An initial pause of 200µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper operation is assured.
2. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.) and are assumes to be 5ns for all inputs.
3. Measured with the load equivalent to (2) two TTL loads and 100pF.
4. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) and can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that t_{RCD} 6≥ t_{RCD} (max.).
6. This parameter defines the time at which the output achieves the open circuit conditions and is not referenced to V_{OL} or V_{OH}.
7. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
8. These parameters are referenced to the $\overline{CAS}$ leading edge in EARLY-WRITE cycles and to the $\overline{WE}$ leading edge in READ-MODIFY-WRITE cycles
9. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. If t_{RAD} is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled exclusively by t_{AA}.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not a reference to output voltage level.
11. 4096 cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
12. t_{AR}, t_{WCR}, and t_{DHR} are references to t_{RAD} (max.).

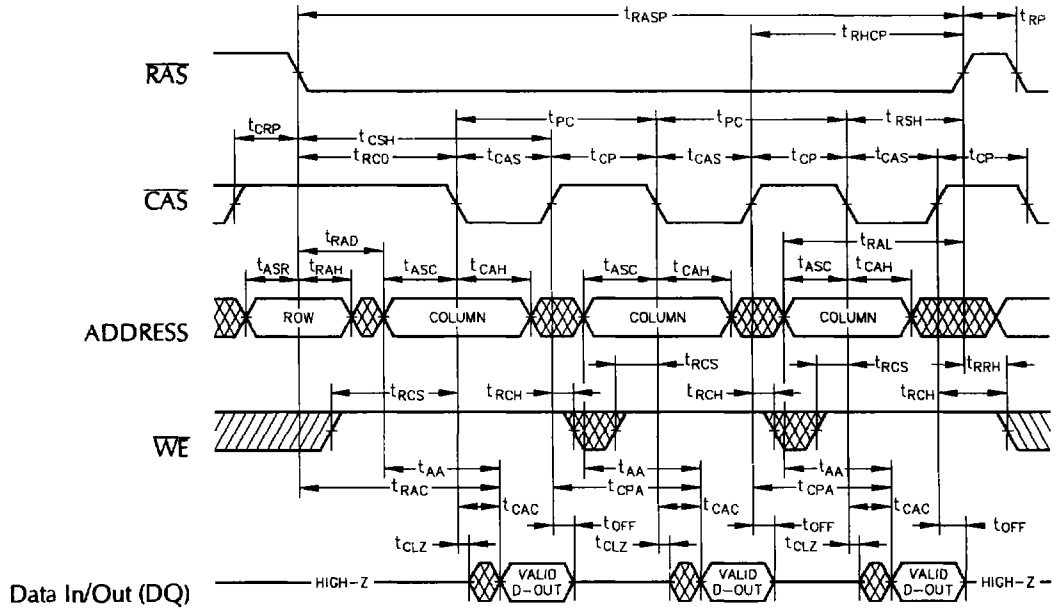
READ CYCLE



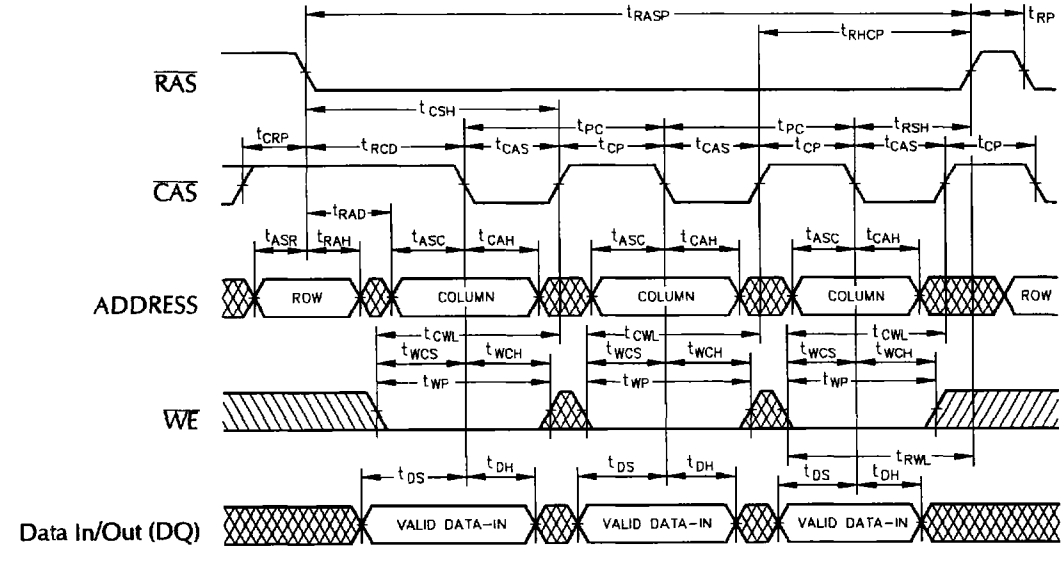
EARLY - WRITE CYCLE



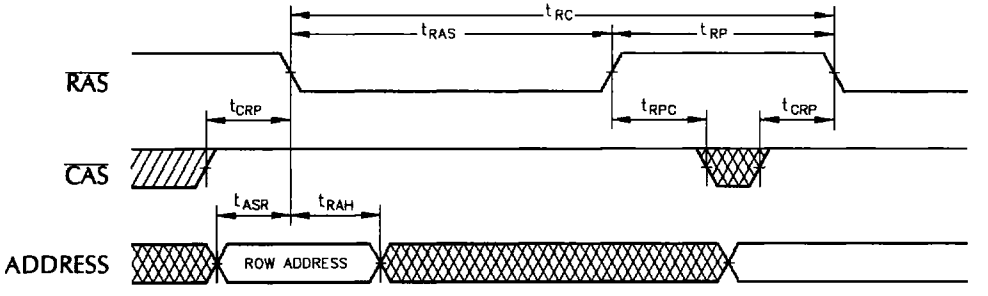
FAST - PAGE MODE READ CYCLE



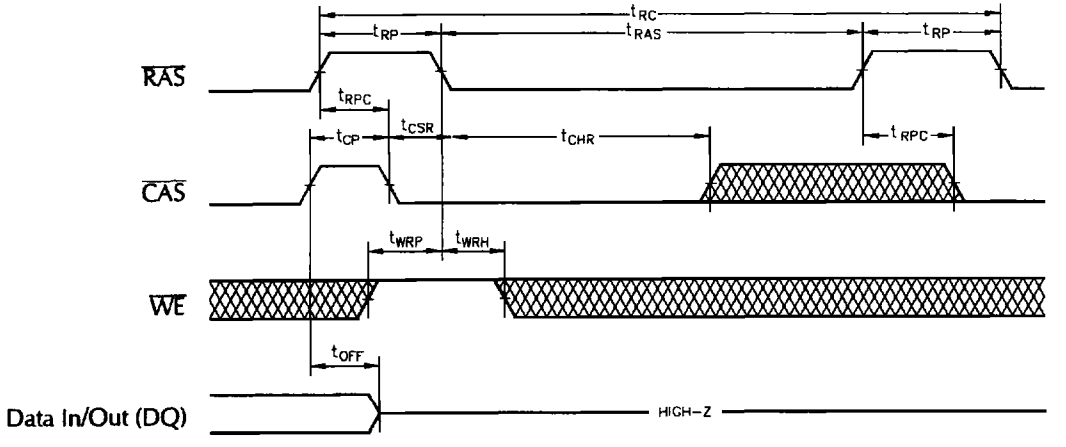
FAST - PAGE MODE EARLY WRITE CYCLE



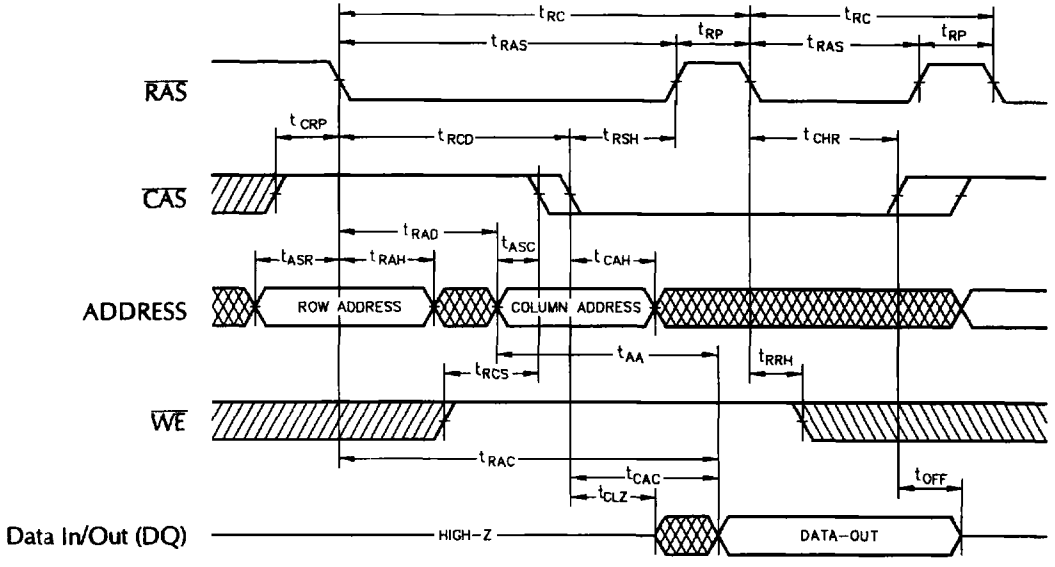
RAS - ONLY REFRESH CYCLE: WE, D_{IN} = Don't Care: D_{OUT} = Open



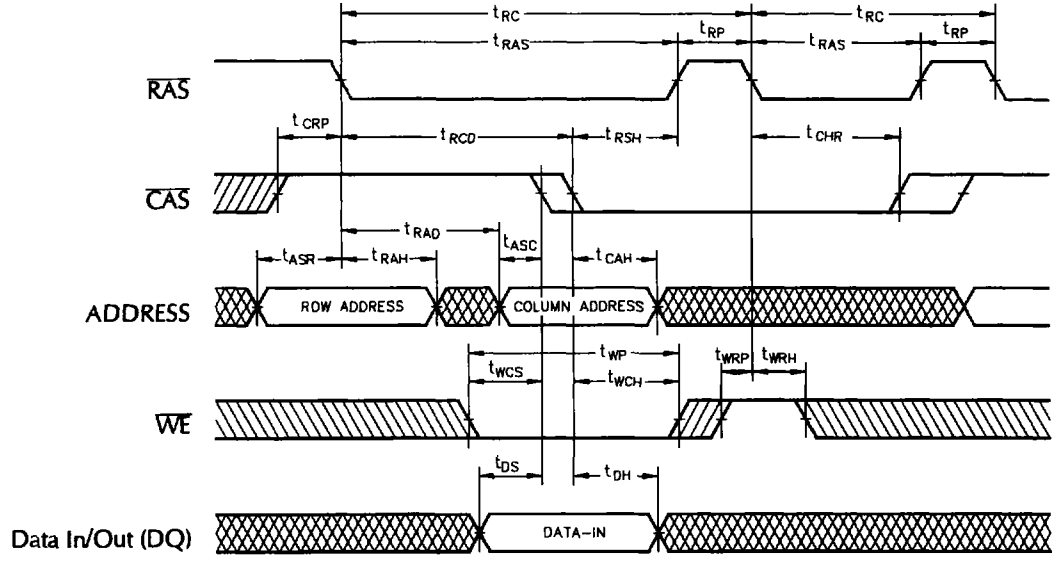
CAS - BEFORE RAS REFRESH CYCLE: Address = Don't Care



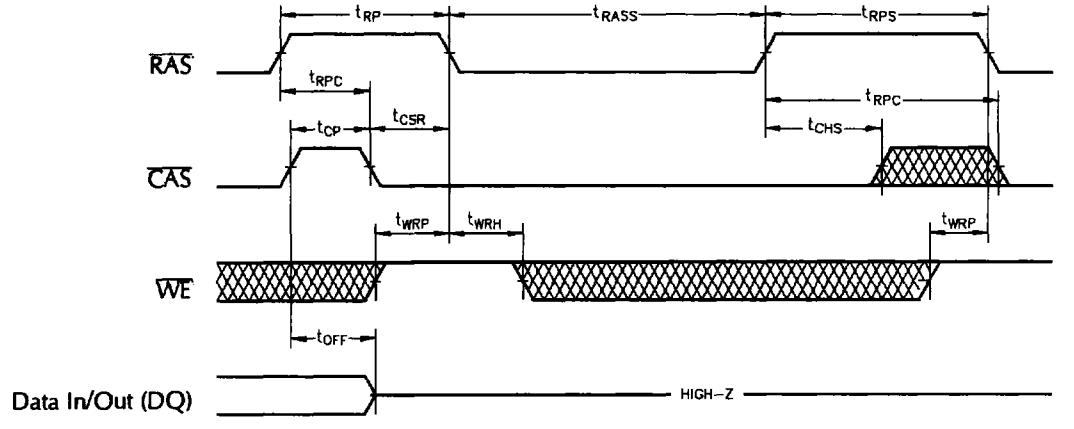
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE): D_{OUT} = Open



CAS - BEFORE RAS SELF REFRESH CYCLE: Address = Don't Care



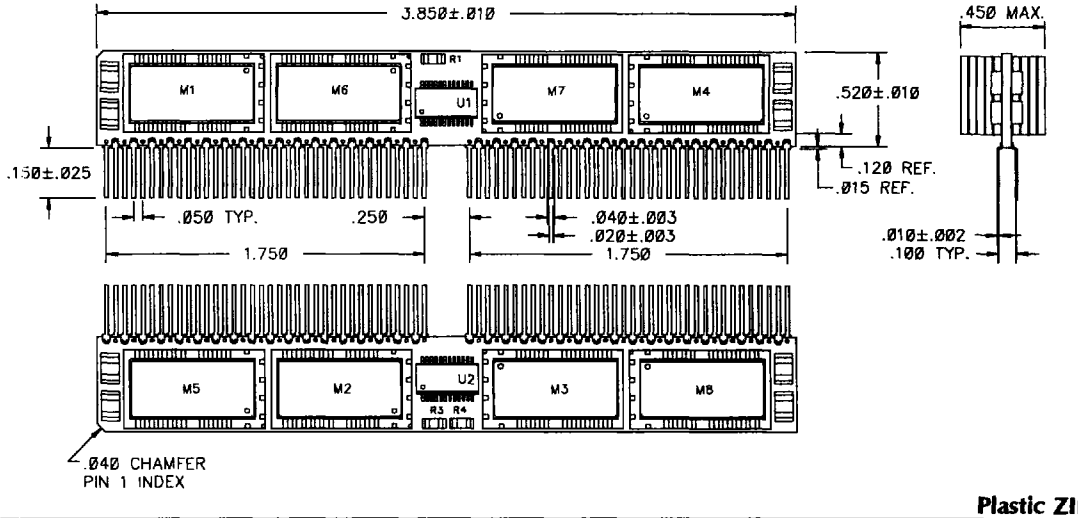
ORDERING INFORMATION

DP D 16M L 36 P W5 – XX C

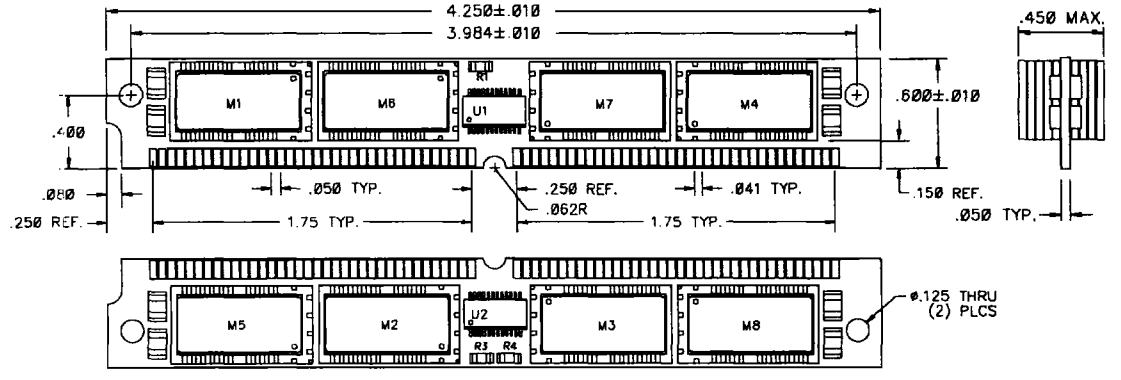
PREFIX | TYPE | MEMORY DEPTH | DESIG | MEMORY WIDTH | DESIG | PACKAGE | SPEED | GRADE

- C COMMERCIAL Ø°C to +7Ø°C
- 7Ø 7Øns
- 8Ø 8Øns
- 1Ø 1ØØns
- L 72-PIN Plastic ZIP / TSOP STACKING
- W 72-PIN SuperSIMM / TSOP STACKING
- 16 MEGABIT BASED
- LOW PROFILE MODULE WITH SUPPORT LOGIC
- CMOS DRAM

MECHANICAL DRAWING



Plastic ZIP



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