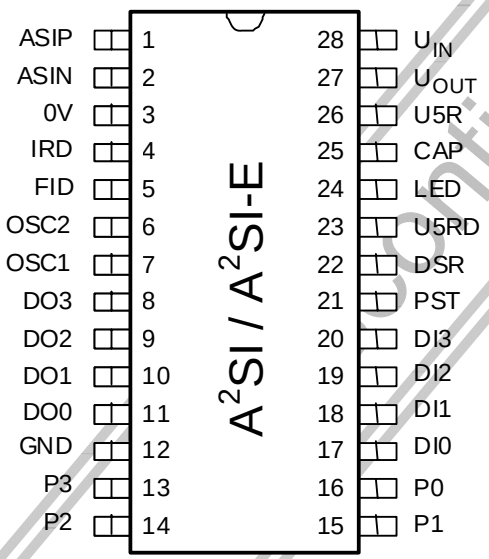
A²SI / A²SI-E

Universal Actuator-Sensor Interface IC

Datasheet

Features

- AS-i Complete Specification V2.11 compliant
- Integrated EEPROM
- Additional addressing channel using an opto-electronic interface
- Extended address mode operation as programmable option (up to 62 slaves)
- High impedance AS-i line input, additional pins for further impedance optimizations
- DC voltage output, approximately 24 volts, not stabilized
- 5 volt DC voltage output, stabilized, CMOS logic can be supplied directly (e.g. µC)
- LED status indicator output (compliant with the standard indication recommendation)
- Integrated watchdog



Description

A²SI is a monolithic CMOS integrated circuit certified for AS-i (Actuator Sensor-interface) networks. AS-i networks are intended for industrial automation.

The main advantage of AS-i solutions is that actuators and sensors are connected using a two-wire unshielded cable that is easy to install. This cable transports both power and information/data.

AS-i network communication is based on the master-slave principle. The network can be extended (to cable lengths greater than 100m) by using the A²SI in the repeater mode configuration.

AS-i is a standard for the automation industry based on IEC 62026-2 and EN 50295.

The device is available in a 28-pin SSOP package (A²SI) or SOP package (A²SI-E), respectively.

Application Support

Configuration of the chip is handled through programming of the on-chip E²PROM. ZMD provides special tools to ease product evaluation and selection of different operation modes.

AS-Interface Programmer 2.0 USB

(Ordering Code: 3600100145)

Evaluation board equipped with A²SI can be ordered from Bihl+Wiedemann GmbH

(www.bihl-wiedemann.de)

Further application support is available through e-mail hotline under asi@zmd.de

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0 READ THIS FIRST

0.1 Important Notice

Products sold by ZMD are covered exclusively by the warranty, patent indemnification and other provisions appearing in ZMD standard "Terms of Sale". ZMD makes no warranty (express, statutory, implied and/or by description), including without limitation any warranties of merchantability and/or fitness for a particular purpose, regarding the information set forth in the Materials pertaining to ZMD products, or regarding the freedom of any products described in the Materials from patent and/or other infringement. ZMD reserves the right to discontinue production and change specifications and prices of its products at any time and without notice. ZMD products are intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment, are specifically not recommended without additional mutually agreed upon processing by ZMD for such applications.

ZMD reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

0.2 References

[1] AS-Interface Complete Specification Version 3.0, dated 16.09.2004

0.3 IC Revision History

Revision	Date	Technical Changes	Note
A	September 1999	First by AMI marketed silicon version	IC Revision A did not have a revision code marking. ICs without a Revision Code are equivalent to Revision A.
B	January 2002	First by ZMD marketed silicon version	

C	August 2002	UART *(Telegram Checker)*	The telegram reception under worst case capacitive and worst case inductive network conditions was improved in response to suggestions of the technical committee of the AS-International Association.	The replacement of A²SI Revision B with Revision C neither has any impact to required external components nor requires a change of the external circuitry. The CAP-Pin of an IC of Revision C shall be connected to a series of one capacitor and one resistor, in the same manner like on Revision B. Suggested values are C=4.7nF, R=430…680 Ohms. See the Data Sheet and the Application Notes for more detailed information.
		UART *(Master Mode)*	The digital MAN-code communication channel does now support a more cost effective two-wire data transfer between the A²SI and the master control logic. It is not necessary to rely on the additional 'Receive_Strobe' signal, which is supplied at the parameter port P2 in Master Mode to verify the correctness of the MAN output signal at the LED port. The MAN signal is now distinctively disturbed if an erroneous telegram was detected at the AS-i input. This allows to spare at least one opto coupler in between the A²SI and the master control.	
		Main State Machine Slave Mode *(Communication Watchdog)*	If running, the communication watchdog will now become turned off as soon as the volatile slave address register is changed to zero (0x0). This occurs after the reception of a Delete_Address call or at a reset of the A²SI. In all previous revisions, a running communication watchdog could only be turned off by a reset of the A²SI (reception of Reset_ Slave call or external reset). In case the watchdog was running and a master did not submit a Reset_Slave call prior to an address assignment, the write access to the non-volatile E²PROM memory could have been interrupted. Because a data corruption is likely in such an event, the A²SI resumed to the fail save state of slave address zero (0x0) and did not respond to the newly assigned address until the address assignment call was repeated.	
		Oscillator	The loop gain of the oscillator was increased to support a broader variety of 8MHz crystals.	
		Effected part of the A²SI	Description of modification	
		Infrared input channel *(Slave Mode)*	It appeared the infrared input channel (IRD) was sensitive against coupled noise in some application circuits. In order to make the photo current input more robust for a broad variety of designs, the analog receiver circuit had been changed. This resulted in a much better performance in terms of noise sensitivity but required a slightly lower signal sensitivity as well. See the updated Data Sheet for more information.	
C	November 2008	The production of the A²SI device will discontinue in 2009. Please use the ASI4U device (http://www.zmd.biz/pdf/ASI4U%20Datasheet_Rev.1.7.pdf) in order to replace the A²SI in existing applications.		

1 General Device Specification

1.1 Absolute Maximum Ratings (Non Operating)

Any stress above the listed Absolute Maximum Ratings may cause permanent damage to the device. The given conditions represent a stress rating only. Functional operation of the device at those conditions or at any other stress above the Operational Limits is not implied. Exposure to maximum rating conditions for extended times may effect device performance, functionality, and reliability

Table 1: Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
V_{0V} ,V_{GND}	Voltage reference	0	0	V	
V_{ASIP}	Positive AS-i supply voltage	-0.3	40	V	
V_{ASIN}	Negative AS-i supply voltage	-0.3	20	V	1
$V_{ASIP-ASIN}$	Voltage difference from ASIP to ASIN (V_{ASIP} - V_{ASIN})	-0.3	40	V	2
V_{ASIPP}	AS-i supply pulse voltage, voltage difference between pins ASIP and ASIN (from ASIP to ASIN)		50	V	3
V_{UIN}	Aux. power supply input voltage	-0.3	40	V	
V_{UINPV}	Aux. power supply input voltage pulse		50	V	3
$V_{inputs1}$	Voltage at pins DI3 - DI0, DO3 - DO0, P3 - P0, DSR, PST, LED, FID, U_{OUT}	-0.3	V_{UIN} + 0.3	V	$V_{inputs1}$ ≤ 40V
$V_{inputs2}$	Voltage at pins OSC1, OSC2, IRD, CAP, U5R, U5RD	-0.3	7	V	
I_{in}	Input current into any pin except supply pins	-25	25	mA	
H	Humidity non-condensing				4
V_{HBM1}	Electrostatic discharge – human body model (HBM1)	4000		V	5
V_{HBM2}	Electrostatic discharge – human body model (HBM2)	2000		V	6
V_{EDM}	Electrostatic discharge – equipment discharge model (EDM)	400		V	7
θ_{STG}	Storage temperature	-55	125	°C	
P_{tot}	Total power dissipation		0.85/1.11	W	8, 9

1 ASIN-pin shall be shorted to 0V-pin on PCB.

2 Reverse polarity protection has to be performed externally.

3 Pulse with ≤ 50µs, repetition rate ≤ 0.5 Hz.

4 Level 4 according to JEDEC-020A is guaranteed

5 HBM1: C = 100pF charged to VHBM1 with resistor R = 1.5kΩ in series, valid for ASIP-ASIN only.

6 HBM2: C = 100pF charged to VHBM2 with resistor R = 1.5kΩ in series, valid for all pins except ASIP-ASIN.

7 EDM: C = 200pF charged to VEDM with no resistor in series, valid for ASIP-ASIN only.

8 P_{tot} = 0.85 W for A^2SI, 1.11 W for A^2SI-E

9 At maximum operating temperature, the allowed total power dissipation depends on the additional thermal resistance from case to ambient and on the operation ambient temperature (see Figure 1 for A^2SI, see Figure 2 for A^2SI-E).

CAUTION: ELECTROSTATIC SENSITIVE DEVICE Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to high-energy electrostatic discharge.

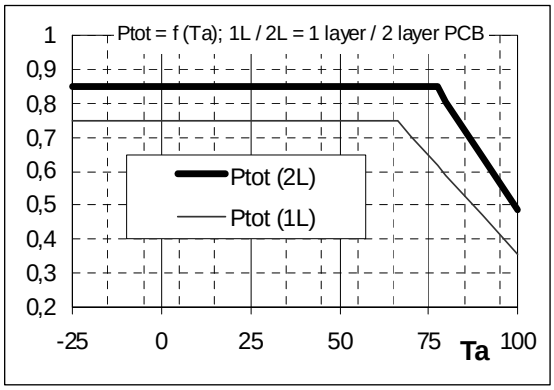


Figure 2: Maximum Power Dissipation for A²SI, PTOT = f(Ambient Temperature)

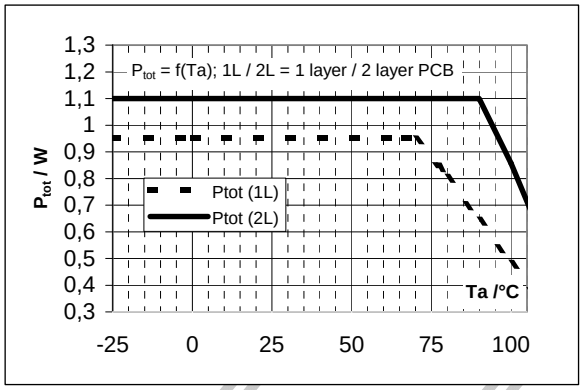


Figure 1: Maximum Power Dissipation for A²SI-E, PTOT = f(Ambient Temperature)

1.2 Operating Conditions

Table 2: Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
V_{UIN}	Positive supply voltage	16	33.1	V	1
V_{ASIN}	Negative AS-i supply voltage	0	0	V	2
V_{0V}, V_{GND}	Negative supply voltage	0	0	V	
I_{ASI}	Supply current at V_{ASI} = 30V		9	mA	3
I_{CL1}	Max. output sink current at pins DO3 - DO0, DSR		10	mA	
I_{CL2}	Max. output sink current at pins P0 - P3, PST		10	mA	
θ_{amb}	Ambient temperature range, operating range	-25	85/105	°C	4

1 DC voltage

2 ASIN shall be shorted with 0V to ensure proper functionality of transmitter circuit.

3 fc = 8.000 MHz, no load at any pin without reaction of the circuit, ASIP is short-cut to UIN and ASIN to 0V respectively.

4 θ_{amb} -25°C to 85°C for A²SI, -25°C to 105°C for A²SI-E

Table 3: Chrystal Frequency

Symbol	Parameter	Nom.	Unit	Note
f_c	Crystal frequency	8.000	MHz	

1.3 EMC Behavior

The IC fulfills the requirements defined in AS-Interface Complete Specification V2.11 [1] and related test requirements AS-Interface Slave ICs.
The above specified behavior is correct by design and has to be proven while IC characterization.

1.4 Quality Standards

The quality of the IC will be ensured according to the ZMD quality standards. ZMD is a qualified supplier according to ISO/TS 16949:2002 and ISO 14001:2004.
The following reference documents apply for the development process:

- Management Regulation: 0410 Product Development procedure
- Process Specification: 1.5µm CMOS-Technology

Functional device parameters are valid for device operating conditions specified in chapter 1.2 at page 3. Production device tests are performed within the recommended ranges of V_{LTGP} - V_{LTGN}, θamb = + 25°C (+ 85/105°C and - 25°C on sample base only) unless otherwise stated.

1.5 Humidity Class

Level 4 according to JEDEC-020D is guaranteed.

1.6 Package Pin Assignment

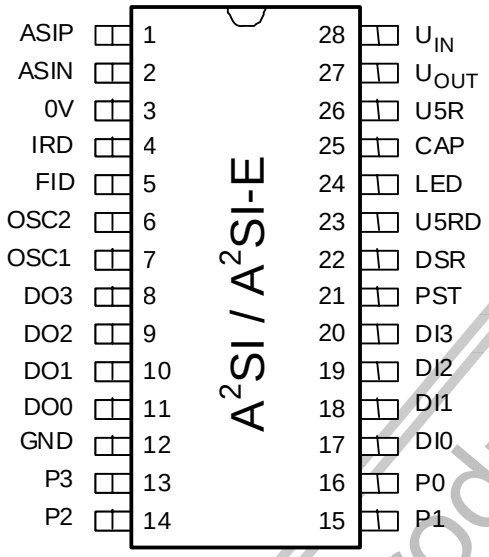


Figure 3: Pin Configuration, 28-Pin SSOP

Table 4: Pin Description

PIN #	Name	Type	Description
1	ASIP	INOUT	To be connected to the AS-i-line ASI+ via reverse polarity protection diode
2	ASIN	INOUT	To be connected to the AS-i-line ASI-
3	0V	SUPPLY	Common 0V for all ports except ASIP/ASIN (to be connected to ASI- line)
4	IRD	IN	Addressing channel input
5	FID	IN	Input peripheral fault indication
6	OSC2	INOUT	Crystal oscillator (8 MHz x-tal)
7	OSC1	IN	Crystal oscillator / external clock input
8	DO3	OUT	Output of data D3
9	DO2	OUT	Output of data D2
10	DO1	OUT	Output of data D1
11	DO0	OUT	Output of data D0
12	GND	SUPPLY	Digital IO ground, must be connected to pin 0V
13	P3	I/O	Input/output of parameter P3
14	P2	I/O	Input/output of parameter P2 / receive strobe in ”Master Mode”
15	P1	I/O	Input/output of parameter P1 / power fail in ”Master Mode”
16	P0	I/O	Input/output of parameter P0 / data clock in ”Master Mode”
17	DI0	IN	Input of data D0
18	DI1	IN	Input of data D1
19	DI2	IN	Input of data D2
20	DI3	IN	Input of data D3
21	PST	OUT	Parameter strobe output
22	DSR	I/O	Data strobe output/reset input
23	U5RD	SUPPLY	Digital 5V supply input, should be connected to U5R
24	LED	OUT	Output LED "AS-i-Diagnosis" / addressing channel output
25	CAP	IN/OUT	For connection of external RC components
26	U5R	OUT	Internal 5V supply that might be used to supply external circuits as well
27	U_{OUT}	OUT	Supply of external circuitry (e.g. sensor, actuator, etc.), approx. V_{UIN} minus 7 volt
28	U_{IN}	SUPPLY	Input of the power supply block (usually to be connected to the AS-i-line ASI+ via reverse polarity protection diode)

2 Basic Functional Description

2.1 Functional Block Diagram

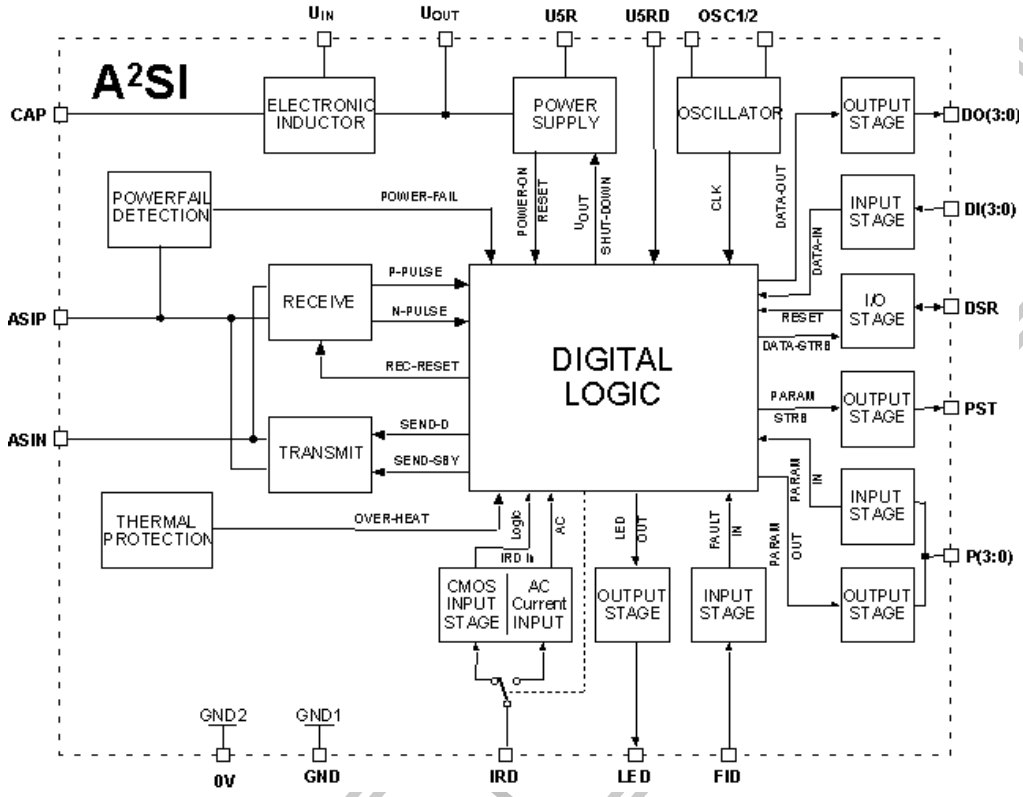


Figure 4: Block Diagram

Following device functions are associated with the different blocks of the IC:

Power Supply An on-chip electronic inductor provides a de-coupled voltage at pin U_{OUT} and the power supply regulates the internal 5V operating voltage. The de-coupling circuit (electronic coil) is connected between U_{IN} and U_{OUT} pins and guarantees a high impedance seen at U_{IN}. An external capacitor and resistor are required to allow a low-pass filter with a very high time constant. This high time-constant value is necessary to maximize the input impedance. The de-coupling circuit limits the current that can be drawn from U_{OUT}. The power supply will shut down the de-coupling circuit in case of an overload condition to prevent a total malfunction of the complete AS-i line. The regulated 5 volt supply voltage is connected to pin U5R. Two external capacitors are necessary to cope with fast internal and external load changes (spikes). Current drawn from pin U5R (up to 4 mA) has to be subtracted from the total load current. The power supply circuit dissipates the major amount of power.

The total power dissipation shall not exceed the specified values of Fehler! Verweisquelle konnte nicht gefunden werden.. The ground reference voltage for both UOUT and U5R is defined by the 0V pin. This pin must be connected to ASI- (ref. Fehler! Verweisquelle konnte nicht gefunden werden.).

Transmitter The transmitter draws a modulated current between ASIP and ASIN pins to generate the communication signals. The shape of the current corresponds to the integral of a sin²-function. The transmitter uses a current DAC and a high current driver. In order to activate high current drive capability, a small current will be turned on automatically prior to each transmission (slave mode only). The current will be ramped up slowly to avoid false voltage pulses on the AS-I line. The amount of circuitry between ASI+ and ASI- pins is minimized to allow high impedance values. When the transmitter is turned on, the receiver is turned off to

reduce power consumption.

Receiver

The receiver detects signals on the AS-i line and delivers the appropriate pulses to the digital logic. The DC value of the input signal is removed and the AC signal is band-pass filtered. The digital output signals are extracted from the $\sin^2$-shaped input pulses by a set of comparators. The maximum voltage of the first negative pulse determines the threshold level for all following pulses. The maximum value is digitally filtered to guarantee stable conditions (burst spikes have no effect). This approach combines a fast adaptation to changing signal amplitudes with a high detection safety. The receiver delivers positive (P-PULSE) and negative (N-PULSE) pulses to the IC's logic. The logic resets the comparators after receiving the REC-RESET signal. When the receiver is turned on, the transmitter is turned off to reduce power consumption.

Digital Logic

The digital logic block performs analysis of the received signal, controls reaction of the IC, transmits slave response, switches I/O-ports, and controls the internal EEPROM. Its principal function is described in detail in section 3.1.

Protection Circuitry

The device has several protection cells that prevent disruption and malfunction of the complete AS-i line.

The thermal detection shuts down the power supply in case of over-heating condition (silicon temperature > 140°C typically for more than 2 seconds) and when U_{OUT} is shorted to GND for more than 2 seconds. The device can only be reactivated by a power-on reset. An over-heating condition can occur by overloading any output pin. Therefore, the circuit monitors the operating conditions of the power supply (effectively monitors U_{OUT}) and measures the temperature of the silicon.

Power Fail Detection

The power-fail detector consists of a comparator that generates a logic signal in case the power supply drops below $22V_{DC}$ (Power-Fail) for a time of more than t_{Loff} (0.8 ± 0.1 ms). The power fail signal will be presented at pin P1 in master mode only.

Power-fail detection monitors the value of the ASIP voltage. It will activate a logic signal if power fails for more than 1ms. The device is then buffered by the external capacitor at U_{OUT} and the internal circuitry will be reset when U5R supply voltage fails

Infrared Diode Input

The photo current input can be used as an alternative communication pin in slave mode. The IRD circuitry will be turned off when the communication has been switched to AS-i line. In Slave mode the logic sets IRD input to photo-detector mode and disables CMOS mode. In this photo-detector mode, signals of an external photo diode are amplified. In CMOS mode (master/repeater mode only), input signals have to be CMOS levels between 0V and V_{U5R}

3 Operational Modes

3.1 Description of Digital Logic

The digital logic is structured in four parts:

1) the UART, which analyses the incoming signal from the AS-i line and ensures correct timing of output signals;
2) the STATE MACHINE, which controls the reaction of the IC;
3) the PORTS, which contain registers and digital I/O's;
4) and finally the E²PROM, which contains the non-volatile data of the A^2SI circuit.

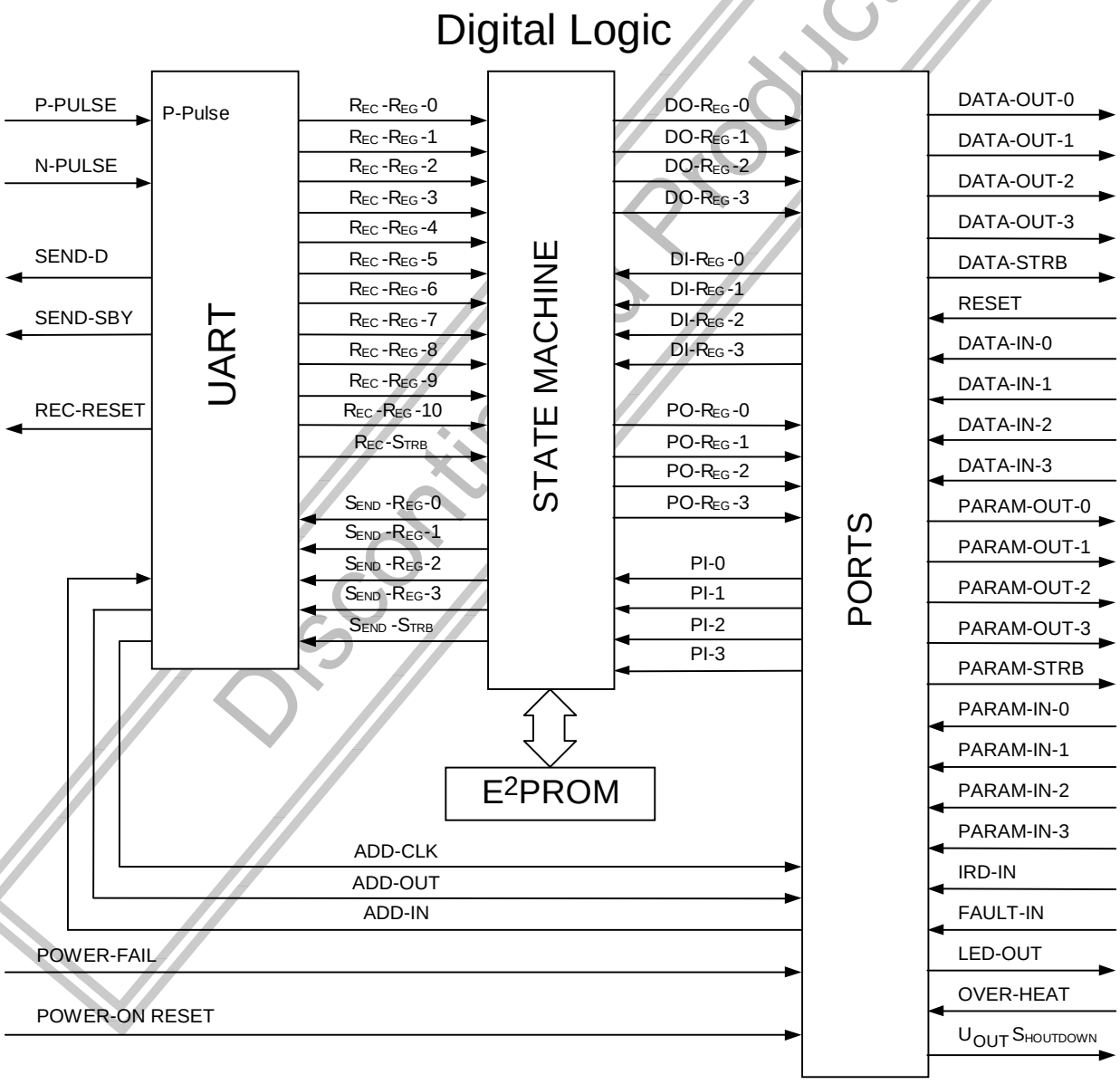


Figure 5: Digital Logic

3.2 Master/Repeater-Mode

3.2.1 IRD Input (CMOS Input)

The IC sends signals retrieved from pin IRD to AS-i line as an AS-i telegram. The input signal is Manchester-coded and active low. A falling edge of the IRD signal, which is conducted to ADD-IN, starts the receiving process and triggers the *Activity-Checker*. *Receive-Muxer* selects pin IRD as input for the receive data

The IRD signal is connected with *Send-Muxer* to SEND-D via ADD-IN. The IRD signal is latched every 500 ns as long as there is activity on the input pin. If there is a high level on the IRD input longer then 7.0 µs, *Activity-Checke*r will recognize this as no activity and *Receive-Muxer* is returning to idle state. The information on pin IRD is transported to pin SEND-D with a delay of 2.0 µs up to 2.5 µs. The sender is always in non-standby mode. The SEND-SBY signal is constant low and there is no generation of ADD-CLK.

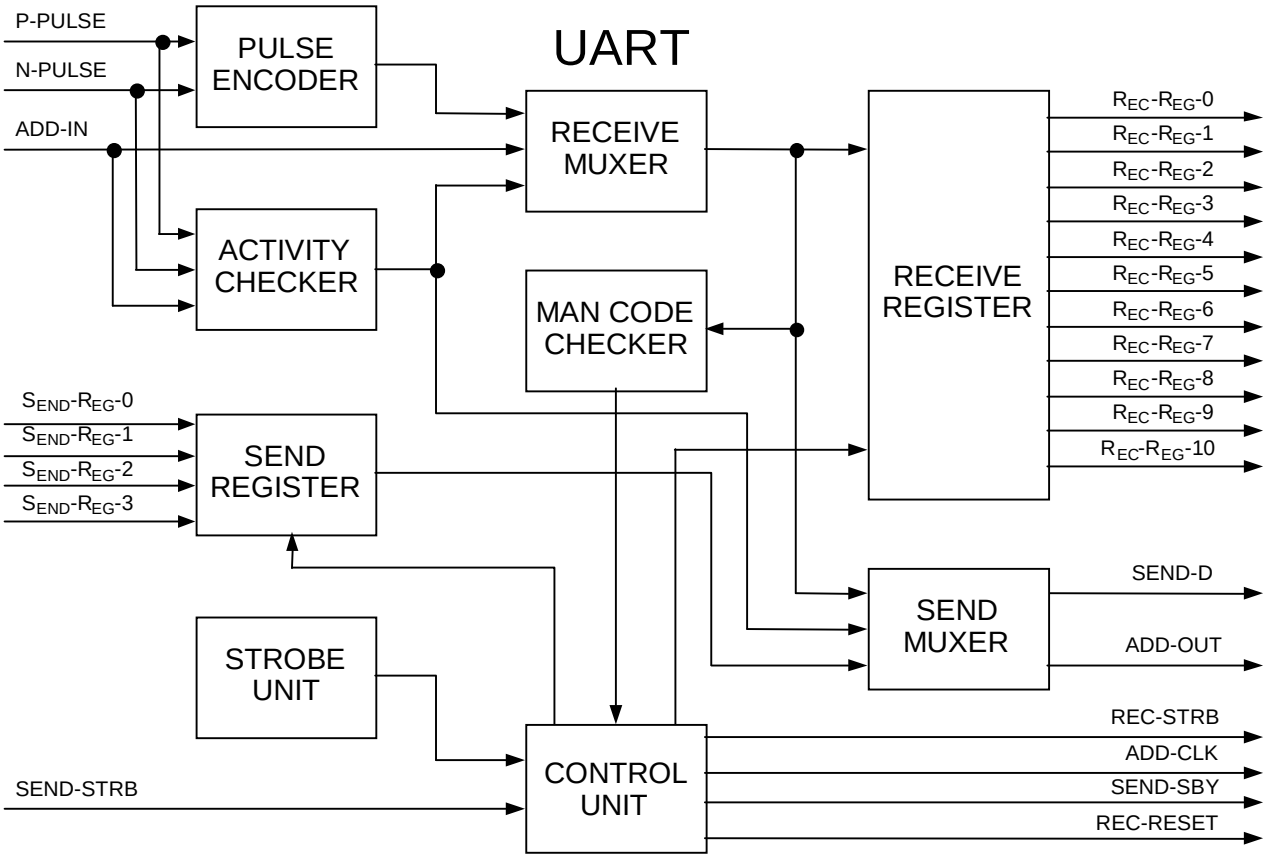


Figure 6: UART Block Diagram

3.2.2 AS-i Input

A signal on the AS-i-line generates signals at the receiver output that are pulse coded with a minimal pulse width of 750 ns up to 875 ns. A pulse on the AS-i line starts the receiver and triggers the *Activity-Checker* through N-PULSE or P-PULSE. The *Receive-Muxer* selects AS-i-line pins as input for the receive data. The N-PULSE and P-PULSE signals are latched every 250 ns as long as there is activity on the input pins. If there is a pulse distance on the AS-i-line inputs longer then 7.0 µs, the receiver will recognize this as no activity and the *Receive-Muxer* is going to the idle state.

The *Pulse-Encoder* is used to convert the active high pulse-coded signal to a active low Manchester-II-coded (MAN) signal. It will also check the pulse stream for timing and pulse errors (e.g. alternation error). In Master/Repeater mode the *Pulse-Encoder* additionally resynchronizes an error-free MAN telegram into a proper 3 µs time base. This is to eliminate the pulse jitter of the transformed AS-i telegram. The synchronized MAN signal is sent to ADD-OUT through the *Send-Muxer.* ADD-OUT is connected to LED-OUT on a higher hierarchy level. All in all, information on the AS-i-line pins is transported to pin LED-OUT with a delay of 2.5 µs up to 3.0 µs. In Master/Repeater mode the sender is never in standby mode, hence SEND-SBY signal is always low.

A generation of ADD-CLK is provided to simplify external processing of Manchester-coded data. The rising edge of the ADD-CLK signal is in the middle of the second half of the Manchester data assuring that correct binary data can be clocked into a shift register. The ADD-CLK starts with a rising edge 2.0 µs after the falling edge of the start bit at ADD-OUT with a period of 6.0 µs and a ratio of 1:1. The last rising edge of the ADD-CLK signal occurs 2.0 µs after the falling edge of the end bit at ADD-OUT.

If the received signal in the Master Mode is a valid slave answer with start bit, four (4) data bits, parity, and end bit and if a pause is following with a length greater than 6.0 µs, the UART generates the active high REC-STRB signal with a pulse width of 500 ns. The REC-STRB signal is connected to the P2 Parameter Output in this mode. It appears 10.0 to 10.5 µs after the rising edge of the end bit on AS-i-line.

3.2.3 Ports

Functional assignments of some IC ports depend on the operational mode of the IC. Thus, these ports perform multiple functions that are related to a particular mode of the IC.

In Master Mode, following signals and ports are connected:

Table 5: Pin Configuration in Master/Slave Function

PIN	Slave Function	Master	Repeater
P0	Parameter output port bit 0	REC-CLK	REC-CLK
P1	Parameter output port bit 1	POWER-FAIL	-
P2	Parameter output port bit 2	REC-STRB	-
LED	LED Fault indicator output/addressing channel output	MAN-OUT	MAN-OUT
IRD	Addressing channel input	MAN-IN	MAN-IN

3.3 Slave Mode

After IC-reset, *Receive-Muxer* is watching the two input channels (AS-i-line and IRD pin) depending on a multiplex select signal MPX. MPX has a frequency of about 1.0 kHz. If MPX is low, the *Receive-Muxer* selects the AS-i-line and vice versa if it is high, it selects the IRD pin as data input. The channel, from which a valid master call is received first, will be locked until the next IC-reset occurs.

3.3.1 IRD Input Mode (Photo Diode Input)

The photo diode current on the IRD input is Manchester-coded and low active (ref. 4.2 Addressing Channel Input IRD). A low level of the IRD signal starts the receiver and triggers the *Activity-Checker*. The *Control-Unit* is enabling the *Receive-Register* and the received information is clocked every 6 µs into the *Receive-Register*. If there is a high level on the IRD input longer then 7.0 µs, the *Control-Unit* will recognize this as no activity and the *Receive-Register* will be disabled. If the received information is a correct master call with *Start-Bit*, eleven *Data-Bits*, *Parity-Bit*, *End-Bit*, and following pause of either greater than 6.0 µs (Synchronous Mode) or 18.0 µs (Asynchronous Mode), the UART generates the internal active high REC-STRB signal with a pulse width of 500 ns.

If the received telegram contained an error, the *Control-Unit* will not generate the REC-STRB signal but go to its asynchronous state waiting for a pause at the IRD input. After a pause was detected, the UART is ready to receive the next telegram from the IRD input.

If a REC-STRB signal is generated, it occurs 9.5 µs up to 10.0 µs (Synchronous Mode) or 21.0 µs up to 21.5 µs (Asynchronous Mode), respectively, after the rising edge of the *End-Bit* on the IRD pin signal. If the slave was in asynchronous state, it now transforms to synchronous state. The *Rec-Muxer* is locked to the IRD input until the next IC-reset. After the generation of a REC-STRB signal the *Control-Unit* is waiting for about 6.0 µs for the SEND-STRB to be generated by the *Main-State-Machine*.

If the *Control-Unit* receives the active high SEND-STRB signal, it starts the transmission of the *Send-Register* data. Therefore, the *Send-Register* data will be converted to an active low Manchester II-coded (MAN) signal which is sent to the LED-OUT pin via ADD-OUT. The first falling edge of the MAN signal occurs 11.75 µs (Synchronous Mode) or 12.25 µs (Asynchronous Mode) after the rising edge of the REC-STRB signal. Hence, the delay from the rising edge of the *End-Bit* of the master call (IRD input) to the first falling edge of the slave response (LED output) is 21.25 to 21.75 µs (Synchronous Mode) or 33.25 to 33.75 µs (Asynchronous Mode). After the pause was detected, the UART is ready to receive the next telegram from the IRD input.

In case the *Control-Unit* will not receive a SEND-STRB signal within the given time frame (for instance, if this slave was not addressed), it will check for activity on the IRD input. Otherwise, it will just wait for the end of the response time (60 µs). In both cases the *Control-Unit* stays synchronous. Once a slave pause was detected, the UART is ready to receive the next telegram from the IRD input

3.3.2 AS-i Input Mode

A signal on the AS-i-line generates two pulse-coded signals (N-PULSE, P-PULSE) at the receiver output with a minimum pulse width of 750 to 875 ns. A pulse on the AS-i line starts the receiver and triggers the *Activity-Checker* through N-PULSE or P-PULSE.

The *Pulse-Encoder* is used to convert the active high pulse coded signal to an active low Manchester-II-coded (MAN) signal. It will also check the pulse stream for timing and pulse errors (e.g. alternation error). The *Control-Unit* enables the *Receive-Register* so that the received information can be clocked in every 6 µs. If there is a pulse distance on the AS-i-line input longer than 7.0 µs, the *Control-Unit* recognizes this as no activity and disables the *Receive-Register*.

If the received information is a correct master call with Start-Bit, eleven Data-Bits, Parity-Bit, End-Bit, and following pause of either greater than 6.0 µs (Synchronous Mode) or 18.0 µs (Asynchronous Mode), the UART generates the internal active high REC-STRB signal. If the received telegram contained an error, the Control-Unit will not generate the REC-STRB signal but go to its asynchronous state waiting for a pause at the AS-i line input. After a pause was detected the UART is ready to receive the next telegram from the AS-i line input.

If a REC-STRB signal is generated, it occurs 10.0 to 10.5 µs (Synchronous Mode) or 21.5 to 22 µs (Asynchronous Mode), respectively, after the rising edge (receiver comparator switching point) of the End-Bit on the AS-i line input. If the slave was in asynchronous state, it now transforms to synchronous state. The Rec-Muxer is locked to the AS-i line input until the next IC-reset. After the generation of a REC-STRB signal the Control-Unit is waiting for about 6.0 µs for the SEND-STRB to be generated by the Main-State-Machine.

If the Control-Unit receives the active high SEND-STRB signal (pulse width 500 ns), it starts the transmission of the Send-Register data. Therefore, the Send-Register data will be converted to an active low Manchester II-coded (MAN) signal which is sent to the AS-i line transmitter via SEND-D. The first falling edge of the MAN signal occurs 11.75 µs (Synchronous Mode) or 12.25 µs (Asynchronous Mode) after the rising edge of the REC-STRB signal.

Hence, the delay from the rising edge of the End-Bit of the master call (AS-i input) to the first falling edge of the slave response (AS-i output) is 21.75 to 22.25 µs (Synchronous Mode) or 33.75 to 34.25 µs (Asynchronous Mode).

The SEND-SBY will always be set low 0.5 µs after the rising edge of REC-STRB. This is to turn on the transmitter and let it settle at its operation point. The small offset current, which is required to operate the transmitter, will be ramped up slowly to avoid any false voltage pulses on the AS-i line.

If all data is sent, the Control-Unit sets the sender in standby mode (SEND-SBY is high) and checks for a slave pause on the AS-i line input. After the pause was detected, the UART is ready to receive the next telegram from the AS-i line input.

In case the Control-Unit will not receive a SEND-STRB signal within the given time frame (for instance, if this slave was not addressed), it will check for activity on the AS-i line. If any activity is detected in a time frame of about 60 µs (another slave is transmitting data), the Control-Unit will wait for the next pause (slave pause). Otherwise, it will just wait for the end of the response time (60 µs). In both cases the Control-Unit stays synchronus. Once a slave pause was detected, the UART is ready to receive the next telegram from the AS-i line input.

3.3.3 Ports

Although the A²SI can still store the AS-i Slave IO-Configuration Code it does not decode the value to configure the direction of the Data-Port signals. The A²SI rather has distinctive Data-Out and Data-In ports which do always work in parallel.

If bi-directional Data I/O is desired on top of a single Data-Port only (for backwards compatibility), the Data-Out pins and the Data-In pins need to be shorted on the circuit board respectively and the non-volatile Multiplex flag has to be set TRUE.

In that case the output ports will switch to high impedance state for a certain time following the rising edge of the Data-Strobe and allow the input data to be put on the Data-Port.

The input data will be read inverted if the non-volatile Invert_Data_In flag is TRUE. This feature will simplify the circuitry for NPN-inputs.

Note: The Multiplex and the Invert_Data_In flags are Configuration flags which are stored in the Firmware region of the internal E²PROM. For a complete overview of the E²PROM content please see the A²SI Application Notes.

The parameter port is always in bi-directional mode. The input data is the result of a wired-AND between the open drain output drivers and the application drivers.

3.3.4 Watchdog

Compliant to the AS-i Complete Specification, the IC contains an independent watchdog which is generally enabled by setting Watchdog_Active flag in the E²PROM to TRUE.

The watchdog will be activated for any slave address uneven to zero (0) after the reception of a Write_Parameter Request at the particular Slave Address. It will be deactivated by any circuit Reset and after the reception of a Delete_Address Request.

When activated, the Watchdog will be reset by every Write_Parameter and Data_Exchange Request received by the Slave. If no such request was received by the particular Slave within 40ms, a Hardware Reset will be performed and all Data and Parameter Outputs are switched inactive.

3.3.5 LED Output

An active FID (logic high) signal causes a flashing status LED (frequency approx. 2Hz) and Bit 1 of the AS-i Slave Status-Register (S1) is set as well. If FID is not active (logic low), S1 is cleared. In that case the status LED operation depends on the Data-Exchange-Disable flag.

The Data-Exchange-Disable is set to TRUE by each Reset of the A²SI. It becomes cleared (set to FALSE) after the first reception of a Write_Parameter Request.

If the Data-Exchange-Disable flag is set, no data exchange can be performed through the Data Ports which is indicated by a steady-on LED.

Note: An active FID has priority and will cause a flashing LED even if the Data-Exchange-Disable flag is set.

If the UART has selected the IRD input channel, the LED output is again overwritten by the Addressing Channel output. In this mode the LED pin does not operate as indicator LED output and periphery failures or status information can not be signaled.

3.3.6 Overtemp shutdown

The A²SI continuously observes its silicon die temperature. If the temperature rises above 140°C the IC will be put into shut-down and stay there until the next power-on reset occurs.

3.3.7 State Machine

The so-called Main-State-Machine performs the central control of the A2SI IC in terms of operation mode selection, EEPROM access control, processing of master requests and the control of the IC ports. The Main-State-Machine interfaces with the UART through the Receive- and the Send-Register as well as certain strobe signals.

To avoid the situation in which a slave IC gets locked in a not allowed state (i.e by emission of strong electromagnetic radiation) and thereby would jeopardize the entire system, all prohibited states of the state machine will lead to a RESET which is comparable to the AS-i call ”Reset Slave (RES)”.

3.3.8 Summary of Master Calls

Table 6: A²SI Master Calls and Related Save Responses

		Master Request														Slave Response						
Instruction	**MNE**	**ST**	**CB**	**A4**	**A3**	**A2**	**A1**	**A0**	**I4**	**I3**	**I2**	**I1**	**I0**	**PB**	**EB**	**SB**	**I3**	**I2**	**I1**	**I0**	**PB**	**EB**
Data Exchange	DEXG	0	0	A4	A3	A2	A1	A0	0	D3 ~Sel	D2	D1	D0	PB	1	0	D3 E3	D2 E2	D1 E1	D0 E0	PB	1
Write Parameter	WPAR	0	0	A4	A3	A2	A1	A0	1	P3 ~Sel	P2	P1	P0	PB	1	0	P3 I3	P2 I2	P1 I1	P0 I0	PB	1
Address Assignment	ADRA	0	0	0	0	0	0	0	A4	A3	A2	A1	A0	PB	1	0	0	1	1	0	PB	1
Write Extented ID Code-1	WID1	0	1	0	0	0	0	0	0	ID3	ID2	ID1	ID0	PB	1	0	0	0	0	0	PB	1
Delete Address	DELA	0	1	A4	A3	A2	A1	A0	0	0 Sel	0	0	0	PB	1	0	0	0	0	0	PB	1
Reset Slave	RES	0	1	A4	A3	A2	A1	A0	1	1 ~Sel	1	0	0	PB	1	0	0	1	1	0	PB	1
Read IO Configuration	RDIO	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	0	0	PB	1	0	IO3	IO2	IO1	IO0	PB	1
Read ID Code	RDID	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	0	1	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read ID Code-1	RID1	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	1	0	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read ID Code-2	RID2	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	1	1	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read Status	RDST	0	1	A4	A3	A2	A1	A0	1	1 ~Sel	1	1	0	PB	1	0	S3	S2	S1	S0	PB	1
Broadcast (Reset)	BR01	0	1	1	1	1	1	1	1	0	1	0	1	PB	1	--- no slave response ---						
Enter Program Mode	PRGM	0	1	0	0	0	0	0	1	1	1	0	1	PB	1	--- no slave response ---						

Note: In extended address mode the "Select Bit" defines whether the A-Slave or B-Slave is being addressed. Dependent on the type of master call the I3 bit carries the select bit information (Sel) or the inverted select bit information (~Sel).

3.4 Program Mode

Provided that the non-volatile configuration flag, *Program-Mode-Disable*, has not been set, the device can be transferred in program mode by utilizing the “Enter Program Mode” call.

Please refer to the A²SI Application Notes [4] for details of the programming process.

AS-i Complete Specification compliance note:

In order to ensure full compliance with the AS-i Complete Specification, the *Program-Mode-Disable* flag must be set in the final manufacturing and configuration process before an AS-i slave device is being delivered to field application users.

4 DC and AC Characteristics

All parameters are valid for the recommended range of V_{ASIP} - V_{ASIN}, V_{UIN} - V_{0V}, and θamb. The devices are tested within the recommended range of V_{ASIP} - V_{ASIN}, V_{IN} - V_{0V}, θamb = +25°C (+ 85°C and - 25°C for A^2SI or + 105°C and - 25°C for A^2SI-E on sample base only) unless otherwise stated. Unused input pins shall be connected to a suitable potential within the application circuit because there are no internal pull-up/down resistors. It is recommended to connect these pins either to 0V or via resistor to U_{OUT} or U5R respectively.

With an external LOW signal at the data strobe pin *DSR* (pull-down open drain driver) for more than 44µs, the IC will execute its reset procedure. During power on procedure all data and parameter ports will stay on high-impedance state.

If the IC has been put in its initialization procedure by an external reset via DSR, the LED pin should not be toggled externally to avoid that the IC control logic transfers to test mode.

4.1 Digital Input and Output Pins

Table 7: Input/Output Voltage and Current

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
Pins DI0 - DI3, P0 - P3, DSR, FID, PST					
V_{IL}	Voltage range for input ”low” level, not P0 – P3	0	2.5	V	
V_{IL}	Voltage range for input ”low” level, only P0 – P3	0	2.4	V	
V_{ICH}	Voltage range for input ”high” level	3.5	V_{UOUT}	V	
V_{HYST}	Hysteresis for switching level	0.25		V	1
I_{IL}	Current range for input ”low” level	-20	-5	µA	
I_{ICH}	Current range for input ”high” level	-10	10	µA	V_O = 5V
I_{IHV}	Current range for high voltage input		2	mA	V_O = 30V
Pins DO0 - DO3, P0 - P3, DSR, PST					
V_{OL1}	Voltage range for output ”low” level	0	1	V	I_{OL1} = 10mA
V_{OL2}	Voltage range for output ”low” level	0	0.4	V	I_{OL2} = 2mA
I_{OH}	Output leakage current	-10	10	µA	V_{OH} = 4.5V
CDL	Capacitance at pin DSR		10	pF	2
Pin LED					
V_{OL}	Voltage range for output ”low” level	0	1	V	I_{OL1} = 10mA 3
I_{OH}	Output leakage current	-10	30	µA	V_{OH} = 40V 4

1 Switching level approximately 3V, i.e. 3V ± VHYST.

2 For higher capacitive load an external pull-up resistor connected to UOUT is necessary to reach VIH ≥ 3.5V at DSR in less than 35 µs after the beginning of a DSR = Low pulse, otherwise a reset will be executed.

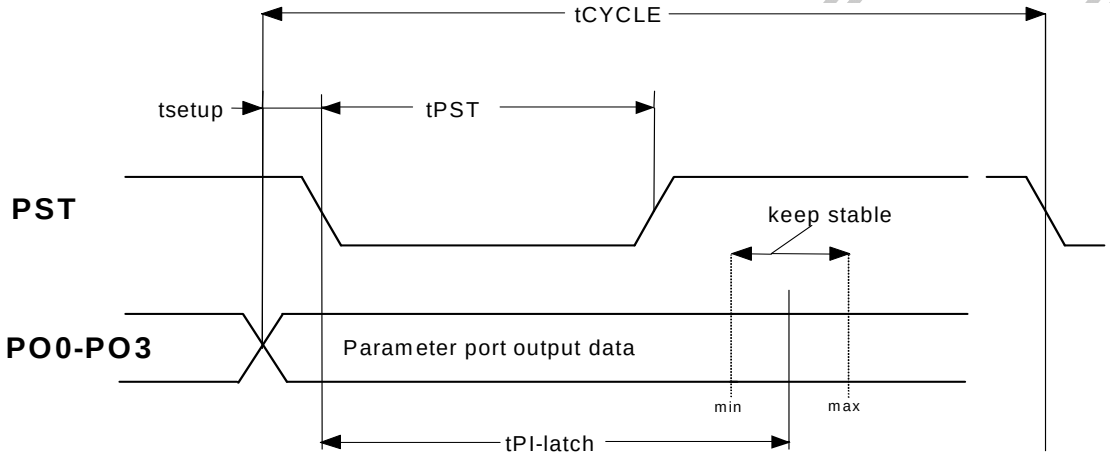
3 The output driver sends a “low” (LED on).

4 The output driver sends a “high” (equivalent to tri-state, LED off).

Table 8: Timing Parameter Port

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
t_{setup}	Valid output data; P0 - P3 to PST-H/L	0.1	0.5	µs	Figure 7
t_{PST}	PST pulse width	5	6	µs	
$t_{PI\text{-}latch}$	PST-H/L to parameter input latch	11	13.5	µs	1
t_{CYCLE}	Next cycle	150		µs	

1 The parameter input data must be stable within the period that is defined by minimum and maximum $t_{PI\text{-}latch}$.



parameter input value (PIx) = parameter output value (POx) wired AND with external signal source value

Figure 7: Timing Diagram Parameter Port P0 - P3

Table 9: Timing Data Port Outputs

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
t_{setup}	Valid output data; DO0 - DO3 to DSR-H/L	0.1	0.5	µs	Figure 8
t_{hold}	Valid output data; DO0 - DO3 to DSR-L/H	0.1	0.5	µs	
t_{DSTR}	DSR pulse width	5	6	µs	
$t_{DI\text{-}latch}$	DSR-H/L to data input latch	11	13.5	µs	1
t_{CYCLE}	Next cycle	150		µs	

1 The data input must be stable within the period that is defined by minimum and maximum of $t_{DI\text{-}latch}$.

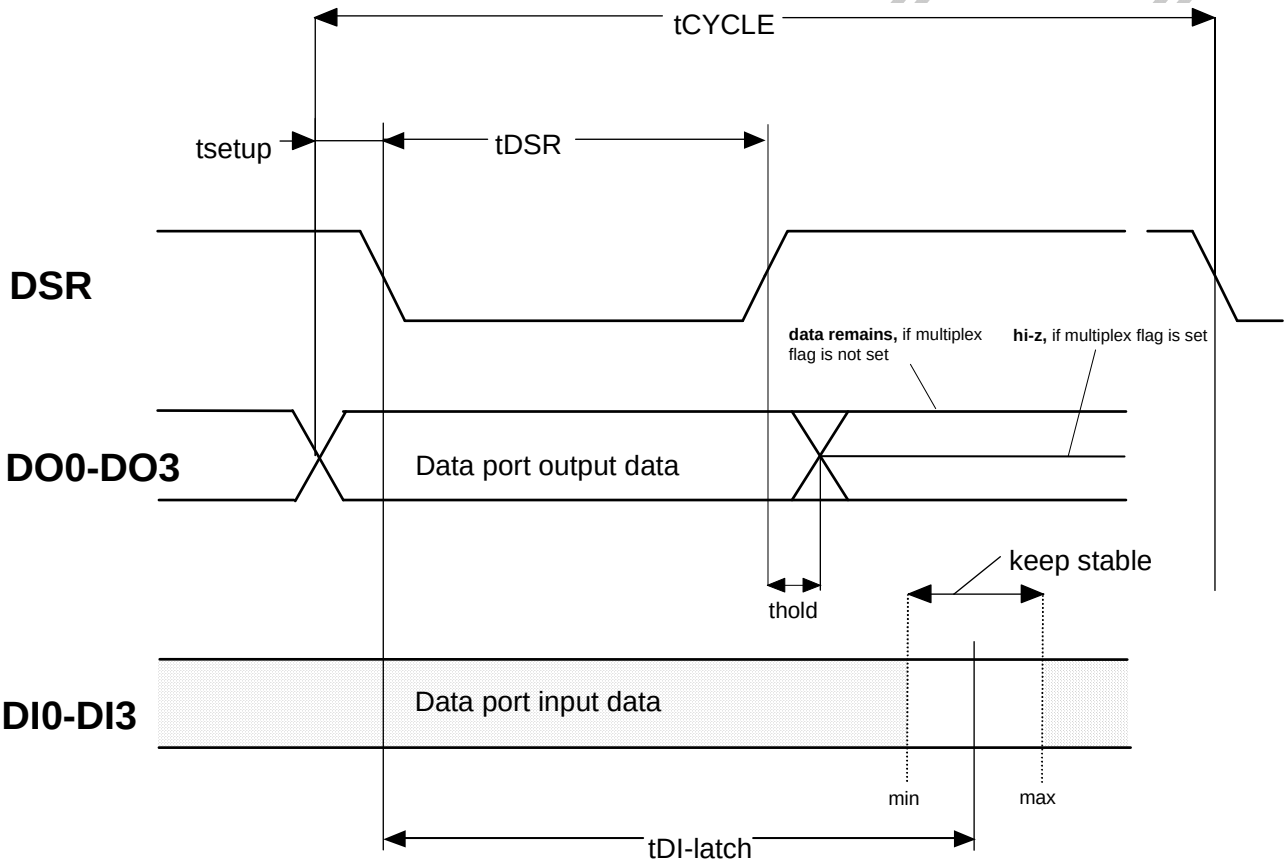


Figure 8: Timing Diagram Data Port DO0 - DO3

Table 10: Timing Reset Signal

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
t_{ALM1}	Ext. DSR (no reset)		35	µs	Figure 9
t_{ALM2}	Ext. DSR to DO0 - DO3 Hi-Z		44	µs	
t_{RESET1}	Reset time after DSR = external L ->H transition		2	ms	

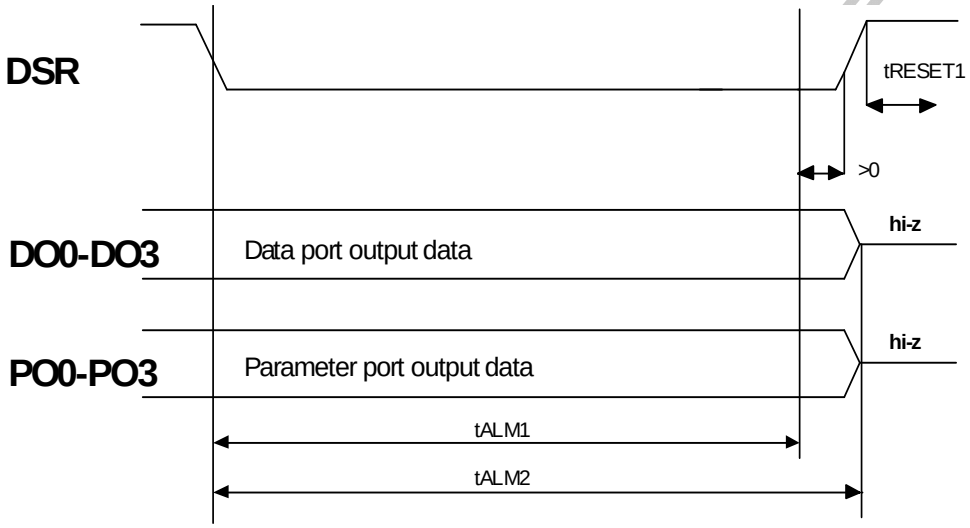


Figure 9: Timing Diagram External Reset via DSR

4.2 Addressing Channel Input IRD

The addressing channel input IRD is a dedicated photo-diode input. The photo-diode can be connected to the pins IRD and 0V directly. The IRD input is a AC current input. A valid signal at the current input has to have a certain amplitude (range) and should not exceed a certain offset value. A logic "low" at the IRD input will be detected, if the present signal value drops below I_{IRDO}, and a "high" will be detected, if its present value is greater than $I_{IRDO} + I_{IRDA}$.

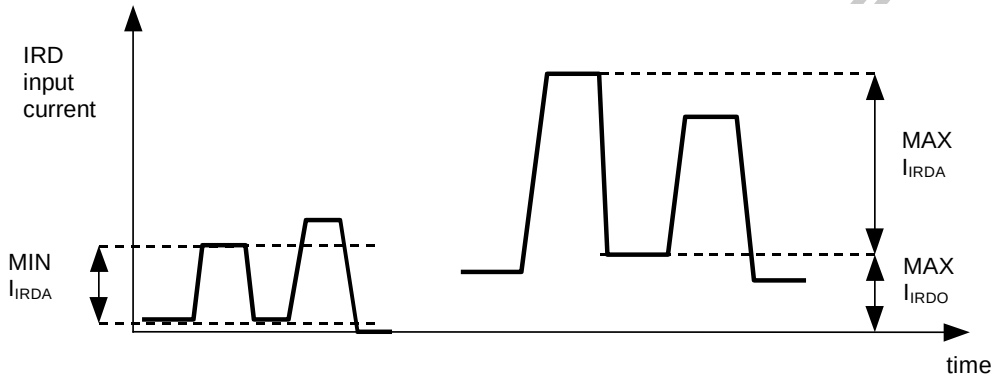


Figure 10: Photo Current Waveform

Table 11: AC Current Amplitude of IR Diode Input in Slave Mode

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
I_{IRDO}	Input current offset		10	μA_{PP}	
I_{IRDA}	Input current amplitude	10	100	μA_{PP}	IC Revision A&B
I_{IRDA}	Input current amplitude	25	100	μA_{PP}	IC Revision C

Table 12: Digital Input IRD in Master/Repeater Mode

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
V_{IL}	Voltage range for input ”low” level	0	2.5	V	
V_{ICH}	Voltage range for input ”high” level	3.5	V_{U5R}	V	
T_r /T_f	Rise/fall time		100	ns	1

1 In order to avoid jittery on the AS-i line, the rise/fall time of the IRD input signal should be as low as possible.

4.3 Fault Indication Input, FID

The fault indication input FID is a digital input dedicated for a periphery fault messaging signal. The S1 status bit is equivalent to the FID input signal. A FID transition will occur at S1 with a certain delay, because a synchronizer circuit is put in between.

4.4 Voltage Outputs

Table 13: Properties of Voltage Output Pins U_{OUT} and U5R

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
V_{UOUT}	U_{OUT} output supply voltage	V_{UIN}- $V_{DROPmax}$	V_{UIN}- $V_{DROPmin}$	V	I_{UOUT} = 30mA
V_{UOUTp}	U_{OUT} output voltage pulse deviation		1.5	V	1
t_{UOUTp}	U_{OUT} output voltage pulse deviation width		2	ms	1
V_{DROP}	Voltage drop from pin U_{IN} to pin U_{OUT}	6.5	7.7	V	V_{UIN} > 22V
V_{U5R}	5V supply voltage	4.5	5.5	V	
I_{UOUT}	U_{OUT} output supply current	0	30	mA	I_{U5R} = 0 mA, 2
I_{5V}	U5R output supply current	0	4	mA	I_{UOUT} < 26 mA
I_o	Total voltage output current I_{UOUT} + I_{5V}		30	mA	
I_{UOUTS}	Short circuit output current	50		mA	
C_{LUOUT}	Load capacitance at U_{OUT}	10	470	µF	
C_{L5V}	Load capacitance at U5R	1		µF	

1 COUT = 10 µF, output current switches from 0 to 30 mA and vice versa.
2 11.0V < VOUT < 27.6V.

4.5 AS-i Bus Load

The following parameters are determined with short-cut between the pins ASIP and UIN and the pins ASIN and 0V, respectively.

Table 14: AS-i Bus Interface Properties (Pins ASIP/ASIN and U_{IN})

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
V_{UIN}	Input AS-i voltage at U_{IN}	$V_{UOUTmin}$+ $V_{DROPmax}$	$V_{UOUTmax}$ + $V_{DROPmin}$	V	1
I_{LIN}	Input current limit at U_{IN}		56	mA	
V_{SIG}	Input signal voltage difference between ASIP and ASIN	3	8	V_{PP}	
I_{SIG}	Modulated output peak current from ASIP to ASIN	55	68	mA_P	
C_{Zener}	Parasitic capacitance of the external over-voltage protection diode (zener diode)		20	pF	2
R_{IN1}	Equivalent resistor of the device	16		kΩ	2, 3
L_{IN1}	Equivalent inductor of the device	18		mH	2, 3
C_{IN1}	Equivalent capacitor of the device		30	pF	2, 3
R_{IN2}	Equivalent resistor of the device	16		kΩ	2, 3
L_{IN2}	Equivalent inductor of the device	12	18	mH	2, 3
C_{IN2}	Equivalent capacitor of the device		15 + (L-12mH)* 2.5pF/mH	pF	2, 3

1 DC Parameter

2 The equivalent circuit of a slave (which is calculated from the impedance of the device and the paralleled external over-voltage protection diode (zener diode)) has to satisfy the Complete AS-i-Specification v.2.1 concerning the requirements for the extended address range.

3 Subtracting the maximum parasitic capacitance of the external over voltage protection diode (20pF) either the triple R_{IN1}, L_{IN1} and C_{IN1} or the triple R_{IN2}, L_{IN2} and C_{IN2} has to be committed by the device to fulfill the Complete AS-i-Specification v2.1.

4.6 Input Impedance Control

Table 15: CAP Pin

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
R_{CAP}	External filter resistor	0	2.2	kΩ	1
C_{CAP}	External filter capacitor	4.7	100	nF	1, 2

1 Recommended values for optimal impedance are: R_{CAP} = 1.2 kΩ and C_{CAP} = 10 nF(IC Revision A)

R_{CAP} = 430 – 680 Ω and C_{CAP} = 4.7 nF(IC Revision B and C) See chapter **Fehler! Verweisquelle konnte nicht gefunden werden.**, Package Marking, for details on how to distinguish different IC versions.

2 The de-coupling capacitor and serial resistor define internal low-pass filter time constant; lower values decrease the impedance but improve the turn-on time. Higher values do not improve the impedance but do increase the turn-on time. The turn-on time also depends on the load capacitor at UOUT. After connecting the slave to the power the capacitor is charged with the maximum current IUOUT. The impedance will increase when the voltage allows the analog circuitry to fully operate.

4.7 Oscillator

Table 16: Oscillator Pins (OSC1 and OSC2)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
C_{OSC}	External parasitic capacitor at oscillator pins OSC1, OSC2	0	5	pF	
V_{IL}	Input ”low” voltage	0	1.5	V	1
V_{ICH}	Input ”high” voltage	3.5	V_{U5R}	V	

1 For external clock applied to OSC1 only.

5 Development Information Data

Table 17: Information Data

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTE
V_{LSIGon}	Receiver comparator threshold level (see Figure 11)	45	50	%	Related to amplitude of 1st pulse
t_{reset1}	Reset time after Master Call „Reset AS-i-Slave“ or DSR = external L ->H transition		2	ms	1
t_{reset2}	Reset time after power on		30	ms	2
t_{reset3}	Reset time after power on with high capacitive load		1000	ms	3
$V_{ASIP-PF}$	V_{ASIP} voltage to detect power fail (master mode only)	21.5	23.5	V	
t_{Loff}	Power supply break down time (master mode only)	0.7	0.9	ms	4
V_{POR1F}	V_{U5R} voltage to trigger internal reset procedure, falling voltage	3.0	4.0	V	1
V_{POR1R}	V_{U5R} voltage to trigger INIT procedure, rising voltage	2.5	3.5	V	1
t_{Low}	Power-on reset pulse width	4	6	µs	
T_{Shut}	Chip temperature for thermal shut down (overheating)	125	160	°C	

Conditions: Asynchronous mode, reset to default comparator level at „line pause“.

1 Guaranteed by design only.

2 ‘Power_on’ starts latest at V_{UIN} = 18V, external capacitor at pin U_{OUT} = 10µF.

3 C_{UOUT} = 470µF, treset3 is guaranteed by design only.

4 C_{UOUT} > 10µF, no power fail generated at V_{ASIP} < $V_{ASIP-PF}$ for t < t_{Loff} (in master mode only).

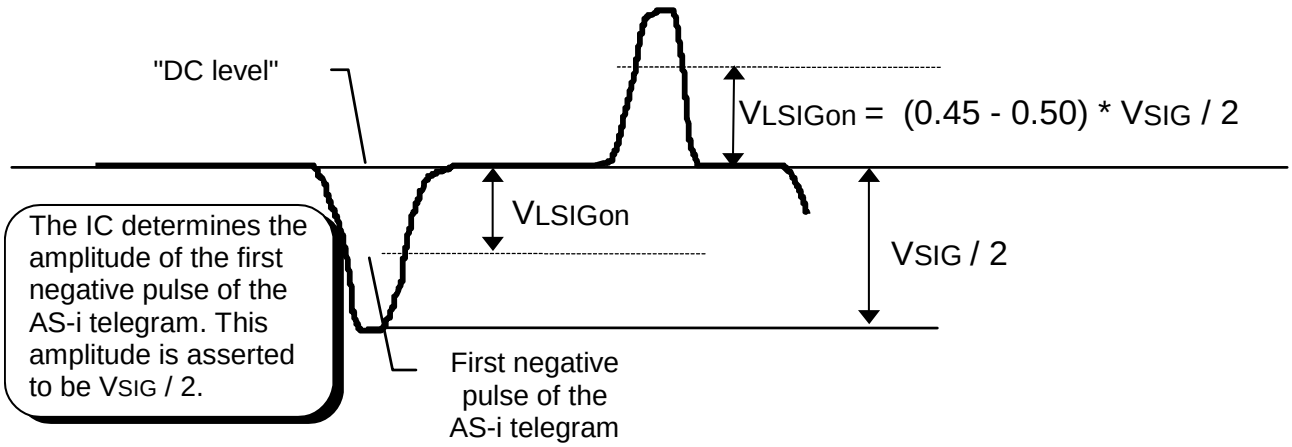


Figure 11: Receiver Comparator Set Up

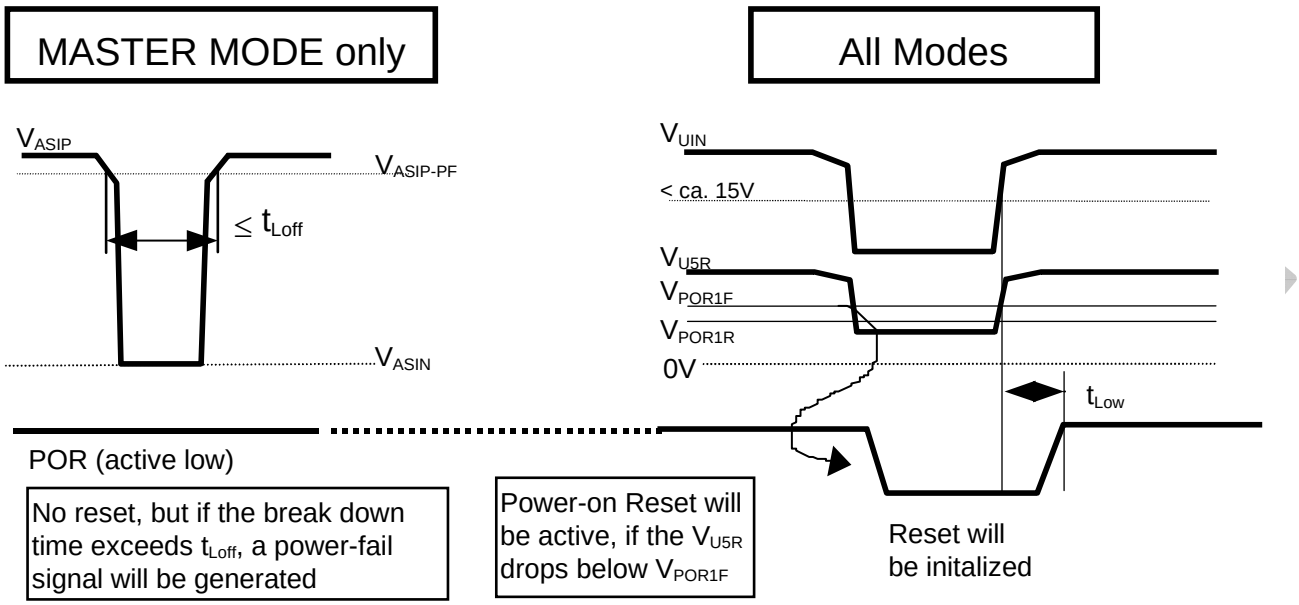


Figure 12: Power-Fail Generation (in Master Mode) and Reset Behavior (All Modes)

6 Application Circuits

The following figures show typical application cases of the A^2SI IC. In Figure 13 you can find a typical application circuit for A^2SI in slave operation mode. Figure 14 shows an application circuit in which the A^2SI is replacing an ASI3+ circuit. Finally, Figure 15 shows how the A^2SI circuit can be used to perform the analog/digital interface between the AS-i-line and the master electronics. Furthermore this figure shows that the IC can be used in repeater applications as well.

6.1 EMC Precautions

Precaution must be taken to avoid radio frequency interference. It is recommended to keep input lines as short as possible and to connect unused inputs to U_{OUT} through a pull-up resistor. Furthermore, the supply pins should be de-coupled with ceramic capacitors (10 to 100 nF) in addition to the normal de-coupling capacitors. Also, it is recommended to connect a pull-up resistor from DSR (pin 22) to U_{OUT} or U5R in order to avoid unintentional reset under difficult EMC conditions.

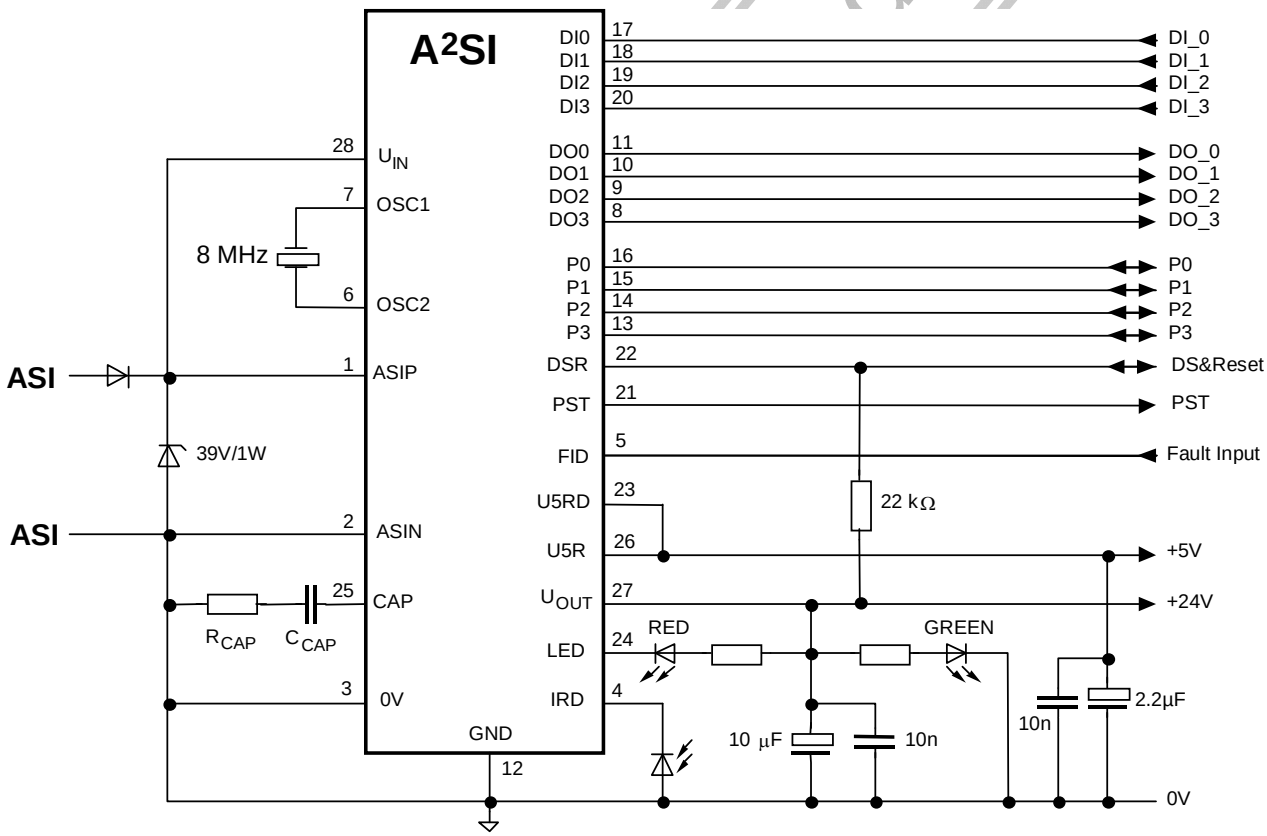


Figure 13: Typical Application, Slave Mode

Note: Figure 13 and Figure 14 show all digital (data and parameter) ports without the application specific connections. For correct function, it is important to consider that all output drivers are open drain stages and hence each port must be connected with an appropriate pull-up resistor.

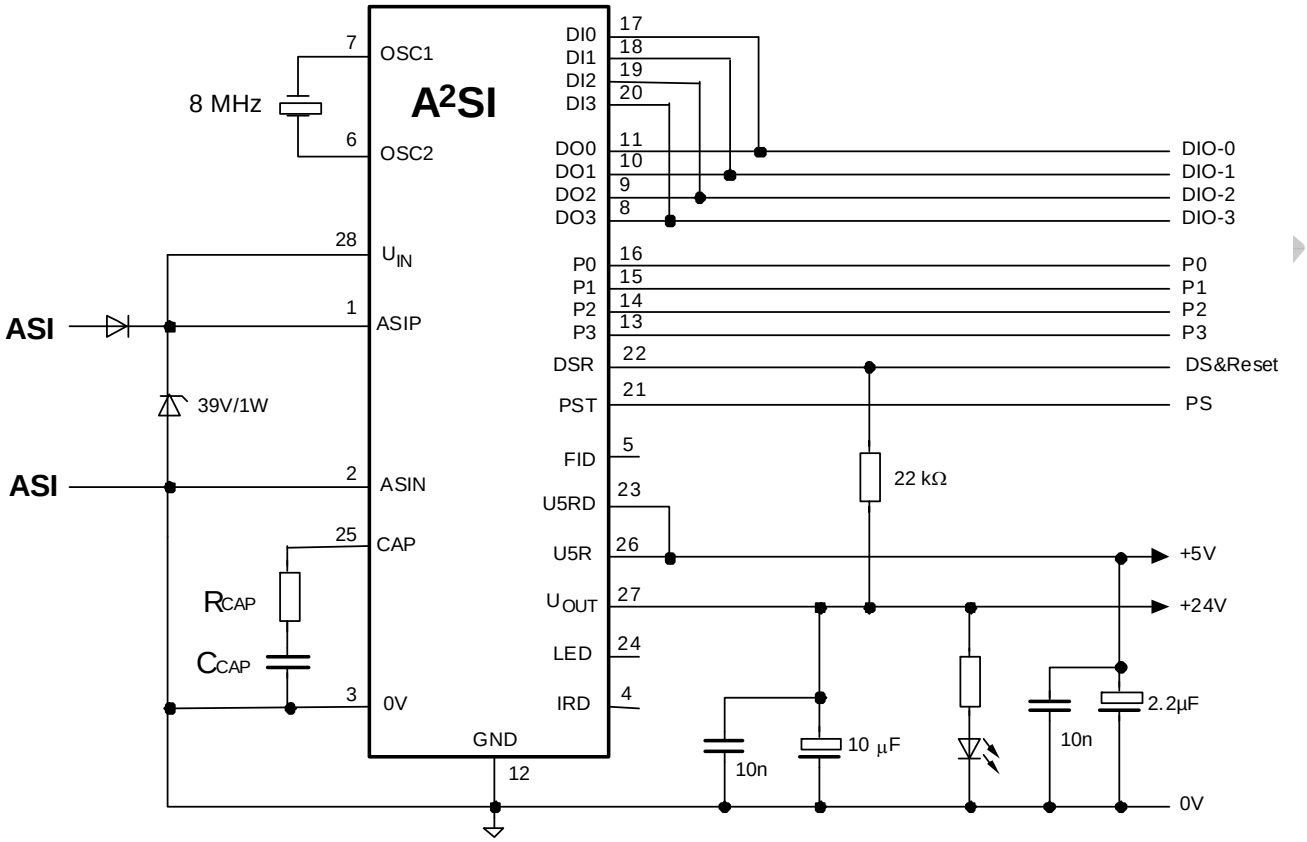


Figure 14: Typical ASI3+ Compatible Application

Note: Depending on I/O-configuration, DO- and DI-ports are connected and Multiplex-Flag is set.

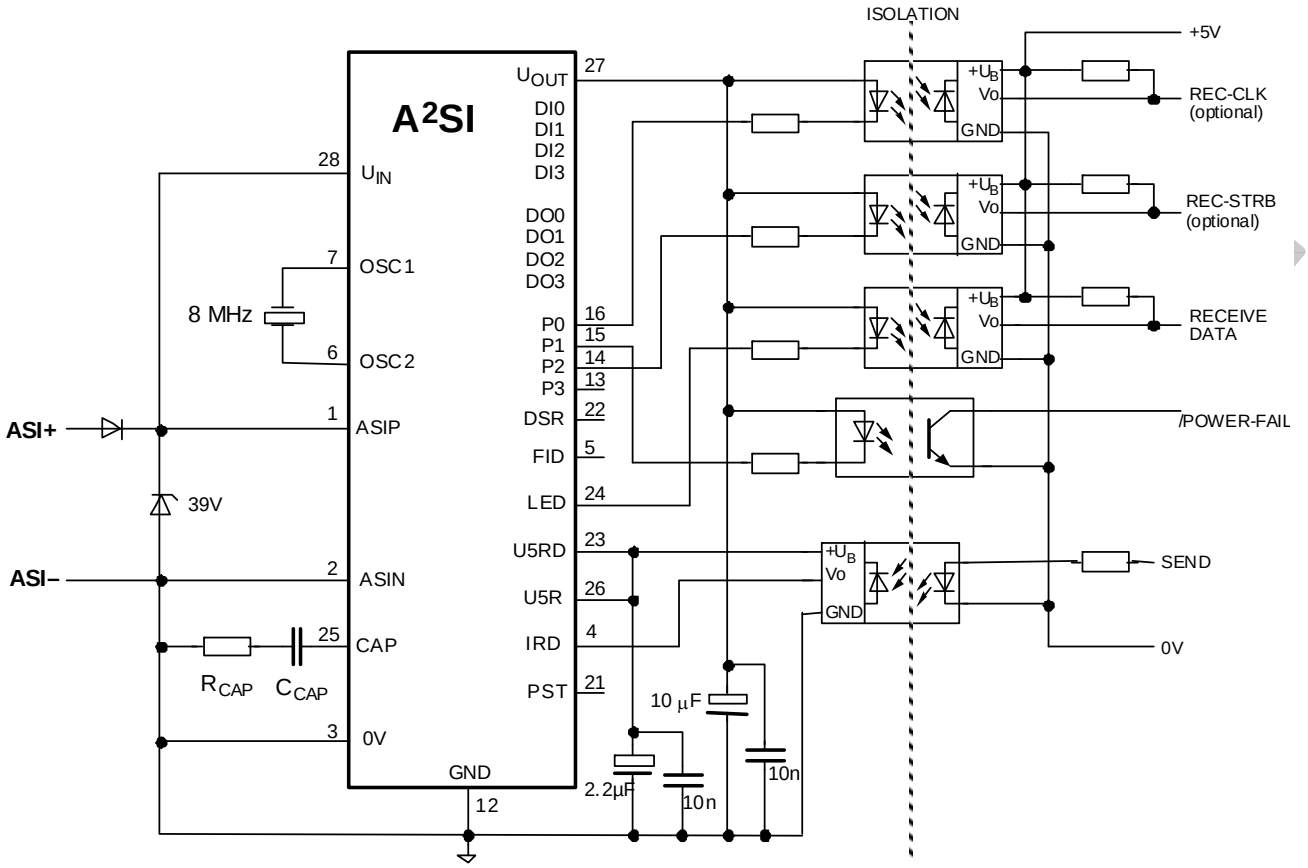


Figure 15: Master/Repeater Application

For further information see also A²SI Application Note.

7 Package Outline

7.1 A^2SI SSOP package

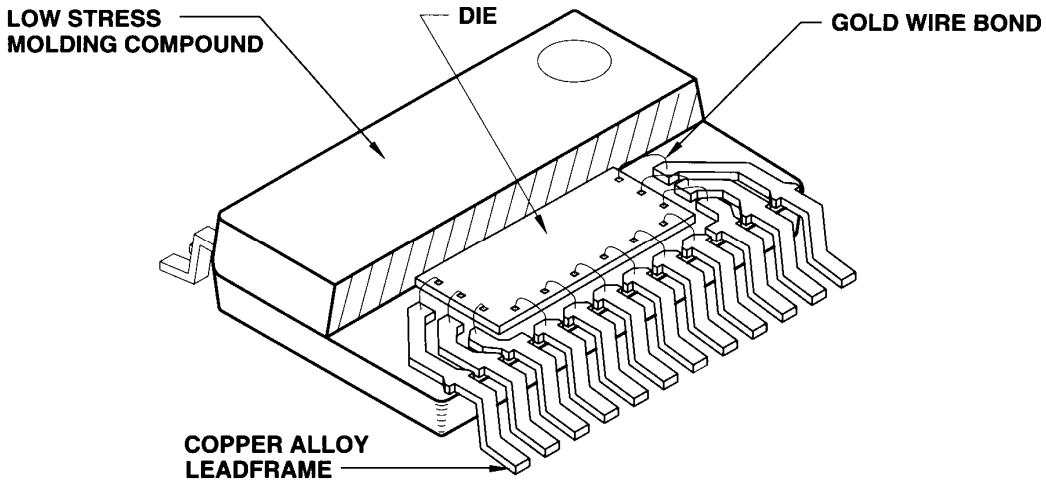


Figure 16: SSOP Package

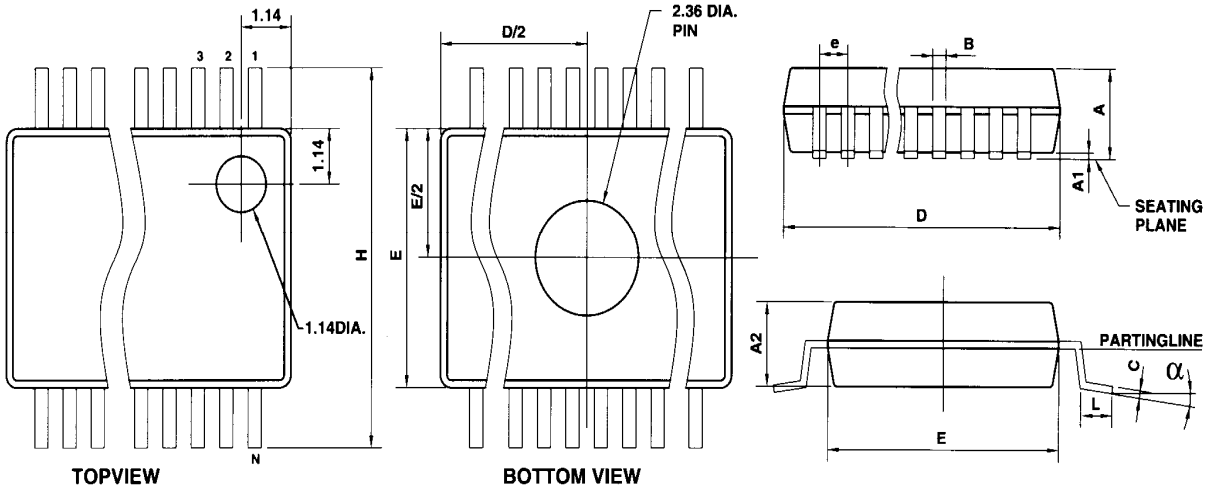


Figure 17: Package Dimensions

Table 18: Package Dimensions (mm)

Symbol	A	A1	A2	B	C	D	E	e	H	L	α
Nominal	1.86	0.13	1.73	0.30	0.15	10.20	5.30	0.65 BSC	7.80	0.75	4°
Maximum	1.99	0.21	1.78	0.38	0.20	10.33	5.38		7.90	0.95	8°
Minimum	1.73	0.05	1.68	0.25	0.13	10.07	5.20		7.65	0.55	0°

7.2 A^2SI-E SOP package

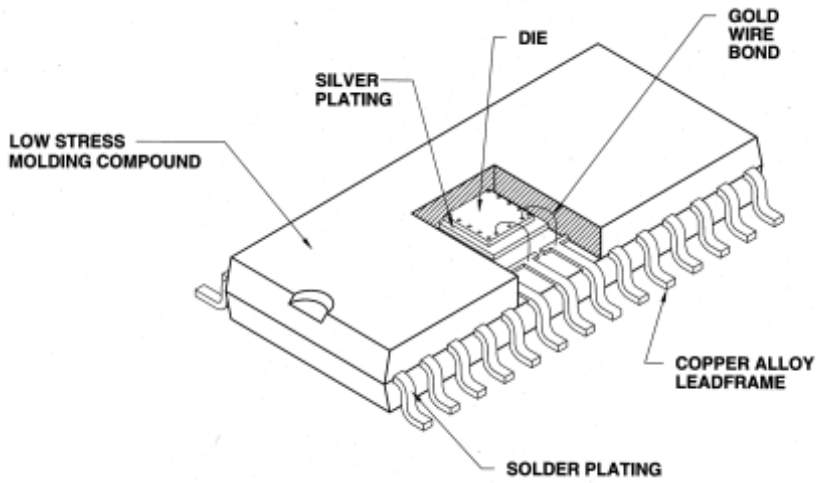


Figure 18: SOP Package

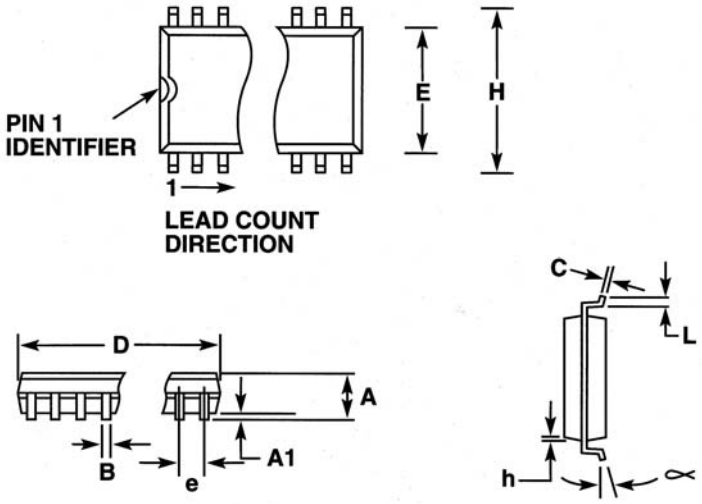


Figure 19: Package Dimensions

Table 19: Package Dimensions (mm)

Symbol	A	A1	B	C	e	D	E	L	H	h	α
Nominal					1,27					0,25 x 45°	
Maximum	2,35	0,10	0,33	0,23		17,70	7,40	0,41	10,01		0°
Minimum	2,65	0,30	0,51	0,32		18,10	7,60	1,27	10,64		8°

8 Package Marking

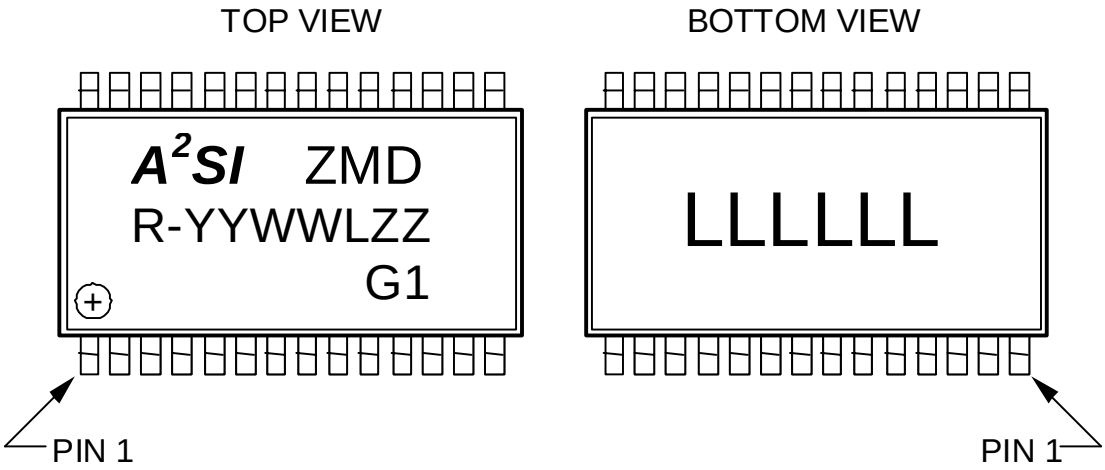


Figure 20: Package Marking

Top Marking:	A²SI / A²SI-E	Product name
	ZMD	Manufacturer
	R-	Revision code
	XXXX	Date code (year and week)
	Y	Assembly location
	ZZ	Traceability
Bottom Marking:	LLLLLL	ZMD Lot Number

The yellow dot indicating pre-programmed Master function is printed at the pin 1 marking ⊕.

Note: IC Revision A did not have a revision code marking. ICs without a Revision Code are equivalent to Revision A. Revision B shows “B-“, Revision C shows “C-“.

9 Ordering Information

Ordering Code	Package	RoHS Con-form	Temperature Range	Delivery	Variant	Min. Order Quantity (MOQ)	Remarks
A2SI-G1-ST Rev.C	SS0P28/ 5,3mm	Y	-25.. +85°C	Tube	Standard	705	(47 parts/tube)
A2SI-G1-SR Rev.C		Y	-25.. +85°C	Tape& Reel	Standard	1500	
A2SI-G1-SR-7 Rev.C		Y	-25.. +85°C	Tape& Reel	Standard	500	7 inch reel
A2SI-G1-MT Rev.C		Y	-25.. +85°C	Tube	Master	705	(47 parts/tube)
A2SI-G1-MR Rev.C		Y	-25.. +85°C	Tape& Reel	Master	1500	
A2SI-E-G1-ST Rev.C	SOP28/ 300mil	Y	-25..+105°C	Tube	Standard	540	(27 parts/tube)
A2SI-E-G1-SR Rev.C		Y	-25..+105°C	Tape& Reel	Standard	1000	
A2SI-E-G1-MT Rev.C		Y	-25..+105°C	Tube	Master	540	(27 parts/tube)
A2SI-E-G1-MR Rev.C		Y	-25..+105°C	Tape& Reel	Master	1000	

Example: A2SI-E-G1-SR-7 Rev.C

Package Type / Operating Temp. Range (optional)
None…SSOP28 / -25 to +85°C
E…SOP28 / -25 to +105°C

Design Revision
Rev.C…3rd design revision**

Package Material (optional)
G1…"green" plastic package with lead-free terminals - pure Sn
None…standard plastic package

Reel Diameter (optional, only for delivery form tape on reel)
None…standard reel diameter: 13"
7…reel diameter 7"

Delivery Form
T…in tube
R…in tape on reel

Device Type
S…Slave IC
M…Master IC*

10 Contact Information

10.1 ZMD Sales Contacts

ZMD AG
Grenzstrasse 28
01109 Dresden, Germany
Phone: +49 (0)351.8822.306
Fax: +49 (0)351.8822.337
E-mail: sales@zmd.de

ZMD Stuttgart Office
Nord-West-Ring 34
70974 Filderstadt - Bernhausen
Phone: +49 (0)711.674.517-0
Fax: +49 (0)711.674.517-99
E-mail: sales@zmd.de

ZMD America Inc.
201 Old Country Road, Ste 204
Melville, NY 11747
Phone: +1 (631) 549-2666
Fax: +1 (631) 549-2882
E-mail: sensors@zmda.com

Please also see www.zmd.biz for most current information on ZMD AS-Interface products and technical product support.

10.2 AS-International Association

Documentation and promotional materials as well as detailed technical specifications regarding the AS-Interface Bus Standard are available from:

AS-International Association:

Contact - Rolf Becker
Zum Taubengarten 52
D-63571 Gelnhausen
PO Box 1103 Zip (63551)
Phone: +49 6051 47 32 12
Fax: +49 6051 4732 82
E-mail: info@as-interface.net
Internet: www.as-interface.net

Refer to www.as-interface.net for contact information on local AS-Interface associations which provide special support within Europe, in the US and in Japan.

Notes: