

WD90C51

Laptop RAMDAC

T-52-33-45
Preliminary

December 08 1989

FEATURES:

- Personal System/2† Compatible
- PVGA1A and WD90C00 Compatible
- Bt471/478 & Bt476 Compatible
- Power Management Features
- On Chip Monitor Detection Logic
- Video Subsystem Cost Reduction
- Video Signal Output into 37.5 Ohms
- 256 X 18 Color Palette RAM
- Triple 6 Bit D/A Converters
- Programmable Pedestal (0 or 7.5 IRE)
- Asynchronous Microprocessor Interface
- Pixel Mask Register
- Up to 8 Bits Input Per Pixel
- RS-343/RS-170 Compatible Outputs
- 1.25 Micron CMOS Technology
- 44-Pin PLCC Package

DESCRIPTION:

The Western Digital WD90C51 was designed specifically for Personal System/2 compatible color graphics in a laptop computer environment. The WD90C51 integrates the functions of a color lookup table, digital to analog converters, bi-directional microprocessor interface, power saving features and PS/2 compatible monitor detection logic.

The WD90C51's 256 X 18 color lookup table has triple 6 bit video D/A converters. A pixel mask register and composite blank generation on the three channels are provided. Options supported by the WD90C51 include a programmable pedestal (0 or 7.5 IRE), and the use of an external voltage reference.

Without external buffering, the WD90C51 will generate RS-343A compatible video signals into a doubly-terminated 75 Ohm load, and RS-170 compatible video signals into a singly-terminated 75 Ohm load. Integral and differential linearity errors are a maximum of $\pm 1/4$ LSB.

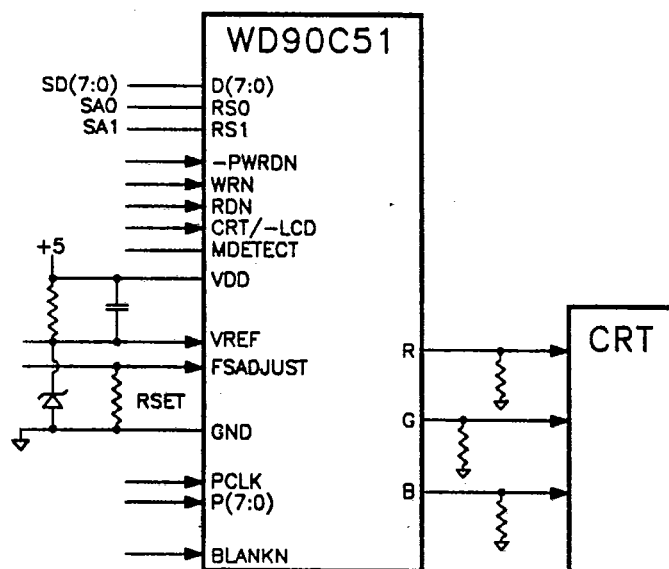


Figure 1. System Diagram

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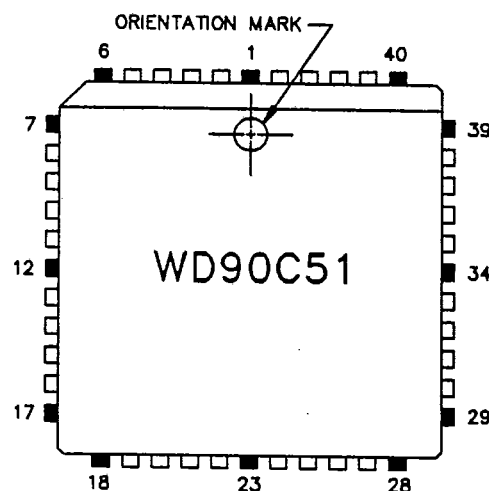
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T-62-33-45**SALES ORDER INFORMATION:****PACKAGE
TYPE**

44-PIN PLCC

**WESTERN DIGITAL
PART NO.**

WD90C51JM00

**44 PIN PLCC
(TOP VIEW)****Figure 2. Pin Diagram**

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	MDETECT	12	D4	23	SETUP	34	P2
2	N/C	13	D5	24	Analog GND	35	P3
3	Digital GND	14	D6	25	IOR	36	P4
4	Digital VDD	15	D7	26	IOG	37	P5
5	N/C	16	-WR	27	IOB	38	P6
6	-RD	17	RS0	28	FSADJUST	39	P7
7	-BLANK	18	RS1	29	N/C	40	PCLK
8	D0	19	N/C	30	N/C	41	CRT/-LCD
9	D1	20	-PWRDN	31	VREF	42	Digital GND
10	D2	21	Analog VDD	32	P0	43	Digital GND
11	D3	22	Analog VDD	33	P1	44	Digital GND

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SCOPE

The WD90C51 is a 1.2 micron CMOS device intended for use in a Personal System/2 compatible laptop system design providing high resolution color graphics.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, timing diagrams, package mechanical information and an applications section.

WD90C51 DESCRIPTION

The WD90C51 architecture consists of five major modules: the Address Register, the Pixel Mask Register, the color palette RAM, power down control, and the digital to analog converter with automatic power on reset. There are three major interfaces to the WD90C51: the MPU, the video memory, and the DAC interface.

WD90C51 MODULES

Address Register

The 8-bit Address Register is used to address the color palette RAM. It is designed for both RAM write mode ($RS1 = 0, RS0 = 0$) and RAM read mode ($RS1 = 1, RS0 = 1$), eliminating the need for external address multiplexers.

Pixel Mask Register

The 8-bit Pixel Mask Register, along with the pixel address bits P0 - P7, is used to generate the color palette RAM address. The register is independent of the pixel address and color value. Without altering the video memory and color palette RAM contents, the displayed color can be changed by programming only the Pixel Mask Register.

Color Palette RAM

There are three 256 x 6 color palette RAMs for the red, green and blue polygon. They provide color information to the triple 6-bit D/A converters. The WD90C51's color palette RAM memory cell is a custom design, power saving cell.

Power Down Control

The WD90C51 supports an intelligent power down control sequence. When -PWRDN input is low, the entire WD90C51 will enter the "IDLE" state; both the DAC and the color palette RAM will be turned off regardless of the CRT/LCD signal. When -PWRDN input is high in CRT mode, the WD90C51 will operate the same as the WD90C50 (the DAC and the color palette RAM are always enabled). In LCD mode, when -PWRDN input is high, the DAC is turned off. The color palette RAM will be enabled only when the MPU is accessing the WD90C51 because of the intelligent "MPU operation auto-detecting" circuit implemented in the WD90C51.

Automatic Power On Reset

The WD90C51 supports an "automatic power on reset" circuit that enables its DAC portion to initialize very quickly after power on. And, since the DAC is totally turned off in LCD mode, a triggered signal will also initialize the "reset operation" of the DAC during the mode change from LCD mode to CRT mode.

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WD90C51 INTERFACES

MPU INTERFACE

The RS1 and RS0 select inputs specify whether the MPU is accessing the Address Register, the color palette RAM, or the Pixel Mask Register, as shown in the table below.

RS1	RS0	REGISTER NAME
0	0	Address Register (RAM Write Mode)
1	1	Address Register (RAM Read Mode)
0	1	Color Palette RAM
1	0	Pixel Mask Register

The WD90C51 supports a bus interface allowing the MPU direct access to the color palette RAM. The MPU interface operates asynchronously to the pixel clock, so the MPU accesses to the color palette RAM may occur at any time without disturbing the display screen.

The MPU writes data to the color palette RAM by using RS1 and RS0 to select RAM write mode (RS1 = 0, RS0 = 0), and then writing the Address Register with the address of the color palette RAM location to be modified. The MPU then writes three successive cycles (red, green and blue) to the color palette RAM. During the three cycles, the write data are latched in the Data Input Registers. After the WRITE BLUE cycle, the color data (three bytes) are transferred from the Data Input Registers to the location on the color palette RAM given by the Address Register. At the end of the write cycles, the Address Register will increment by one to specify the address of the next location on the color palette RAM which can be modified when the MPU writes another sequence of red, green, and blue data.

The MPU reads color data from the color palette RAM by using RS1 and RS0 to select RAM read mode (RS1 = 1, RS0 = 1), and loading the Address Register with the address of the color palette RAM location to be read. When the MPU loads the Address Register, data will be read from the color palette RAM at the address given by the Address Register and will be latched in the Read Data Buffers. During the READ RED, READ GREEN and READ BLUE cycles, the data from the color palette RAM will be read directly from the Read Data Buffers by the MPU. After the READ BLUE cycle, the Address Register will increment by one to specify the address of the next location on the color palette RAM which can be read.

The MPU may read the Address Register at any time without modifying the Address Register contents or the current read/write mode. Care should be used in following the correct programming sequence for the Address Register, since when RAM write (or read) mode is programed, only the RAM write (or read) operation will be implemented.

The MPU may also access the Pixel Mask Register at any time since the WD90C51 design guarantees a flicker-free display whenever the MPU programs the Pixel Mask Register. The write strobe of the Pixel Mask Register need not be synchronized with PCLK. A logical "1" enables the pixel address bit and a logical "0" masks the pixel address bit. Since there is no external system RESET signal, care should be taken in following the correct programming sequence for the Pixel Mask Register. The register must be programed before the display is enabled. It is suggested that it be programed at the beginning of the WD90C51's initialization.

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VIDEO MEMORY INTERFACE

The Pixel Mask Register contents are bit-wised ANDed with the pixel address bits P0 - P7 to generate the color palette RAM address. It is suggested that P0 - P7 be synchronized with PCLK. The addressed location on the color palette RAM provides color information to the three D/A converters.

The -BLANK signal modifies the analog outputs to produce the output levels required for video applications. -BLANK is latched on the rising edge of PCLK for synchronization with the pixel color data. It should be synchronized with PCLK externally.

The WD90C51 analog outputs can drive a doubly-terminated 75 Ohm coaxial cable.

The SETUP signal specifies either a 0 IRE (SETUP = GND) or a 7.5 IRE (SETUP = VDD) blanking pedestal.

DAC INTERFACE

An external voltage reference should be used to provide power supply rejection and temperature compensation. For further information on the external voltage reference, refer to the applications section.

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The table below provides WD90C51 pin definitions for the 44-pin PLCC.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
PIXEL INTERFACE			
40	PCLK	I	PIXEL CLOCK: The rising edge of this signal latches P0-P7 and -BLANK. It is also used to control synchronization through the color look-up table to the D/A analog outputs. Typically, PCLK is the pixel clock rate of the video system.
7	-BLANK	I	COMPOSITE BLANK CONTROL: When -BLANK is a logical zero, the pixel inputs are ignored.
39	P7	I	PIXEL ADDRESS BIT 7 TO BIT 0: These inputs combined with the Pixel Mask Register will select, on a pixel basis, one of the 256 entries in the color palette RAM to provide color information to the DAC.
38	P6	I	
37	P5	I	
36	P4	I	
35	P3	I	
34	P2	I	
33	P1	I	
32	P0	I	
MICROPROCESSOR INTERFACE			
16	-WR	I	WRITE ENABLE: D7-D0 data are latched on the rising edge of -WR and RS1-RS0 are latched on the falling edge of -WR during an MPU write operation.
6	-RD	I	READ ENABLE: The color palette RAM and Pixel Mask Register can be read asynchronously by the MPU. RS1-RS0 are latched on the falling edge of -RD.
41	CRT/-LCD	I	LCD OR CRT SELECT: This active high input is used to control the internal power down mode. "0" is LCD mode, and "1" is CRT mode. In LCD mode, the DAC is turned off, and color palette RAM is enabled only during an MPU read or write operation. In CRT mode, the DAC and the color palette RAM are always enabled if -PWRDN input is high.
20	-PWRDN	I	POWER DOWN SELECT: This active low input is used to enable power down mode. The WD90C51 will enter the "IDLE" state if -PWRDN = "0". Both the DAC and the color palette RAM will be turned off regardless of the CRT/-LCD signal.

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PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
1	MDETECT	O	MONITOR DETECT: This active high signal is used to determine the monitor type, or if the monitor is connected by programming the color palette RAM with specific data.
15 14 13 12 11 10 9 8	D7 D6 D5 D4 D3 D2 D1 D0	I/O I/O I/O I/O I/O I/O I/O I/O	DATA BUS BIT 7 TO BIT 0: MPU data is transferred into and out of the RAMDAC over this eight bit data bus (bidirectional).
18 17	RS1 RS0	I I	REGISTER SELECT BIT 1 AND BIT 0: These bits specify whether the MPU is accessing the Address Register, the color palette RAM or the Pixel Mask Register.
ANALOG INTERFACE			
27 26 25	IOB IOG IOR	O O O	RED, GREEN AND BLUE CURRENT OUTPUTS: These high impedance current sources can directly drive a doubly-terminated 75-Ohm coaxial cable.
28	FSADJUST	O	FULL SCALE ADJUST CONTROL: A resistor (RSET) which is connected between this pin and analog ground controls the magnitude of the full scale video signal.
31	VREF	I	VOLTAGE REFERENCE INPUT: A 1.2 V reference will support this input. (LM385BZ-1.2, 1% tolerance).
23	SETUP	I	SETUP CONTROL INPUT: This signal is used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VDD) blanking pedestal. This selection could make BLACK and BLANK the same voltage level.
POWER, GROUND & NO-CONNECTS			
21, 22 24 4 3, 42, 43, 44 2, 5, 19, 29, 30	ANALOG VDD ANALOG GROUND DIGITAL VDD DIGITAL GROUND NO CONNECT	+5 V AGND +5 V GND N/C	

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T-62-33-45**ABSOLUTE MAXIMUM RATINGS**

Ambient temperature under bias	0°C to 70°C
Storage temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to V _{SS}	-0.3 to 7 Volts
Power dissipation	1.0 Watt

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating temperature range	0° to 70°C
Power supply voltage	4.75 to 5.25 Volts

D.C. CHARACTERISTICS**DIGITAL**

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS
V _{IL}	Input Low Voltage	GND -0.5	0.8	V	V _{DD} = 5V +/-10%
V _{IH}	Input High Voltage	2.0	V _{DD} +0.5	V	V _{DD} = 5V +/-10%
I _{IL}	Input Low Current	----	-1	uA	V _{IN} = 0.0V
I _{IH}	Input High Current	----	1	uA	V _{IN} = V _{CC}
V _{OL}	Output Low Voltage	----	0.4	V	I _{OL} = 4 mA
V _{OH}	Output High Voltage	2.4	----	V	I _{OH} = -4 mA
C _{IN}	Input Capacitance	----	10	pF	F _C = 1MHz
C _{OUT}	Output Capacitance	----	10	pF	F _C = 1MHz
I _{OZ}	3 State Current	----	50	uA	0V < V _{OUT} < V _{DD}

ANALOG

PARAMETER	MIN.	TYP	MAX	UNITS
Resolution (Each DAC)	----	6	----	Bits
Accuracy	----	----	----	----
Integral Linearity Error	----	----	1/4	LSB
Differential Linearity Error	----	----	1/4	LSB
Gray Scale Error	----	----	3.5 %	Full Scale
Monotonicity	Guaranteed			

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T-52-33-45**D.C. CHARACTERISTICS (Cont'd)****MAXIMUM CURRENT CONSUMPTION**

Mode PCLK Frequency	CRT 50 MHz	CRT 25 MHz	LCD 25 MHz	Power-Down 25 MHz
I _{dd} = Digital Supply Current (mA)	72	42	30	23
I _{aa} = Analog Supply Current (mA)	80	77	6	4

SETUP = V_{AA}

PARAMETER	MIN.	TYP	MAX	UNITS
Gray Scale Current Range	-----	-----	20.00	mA
White Level Relative to Blank	17.70	19.05	20.40	mA
White Level Relative to Black	16.74	17.62	18.50	mA
Black Level Relative to Blank	1.0	1.33	1.75	mA
Blank Level	6.5	7.62	8.80	mA
LSB Size	-----	279.68	-----	uA

SETUP = GND

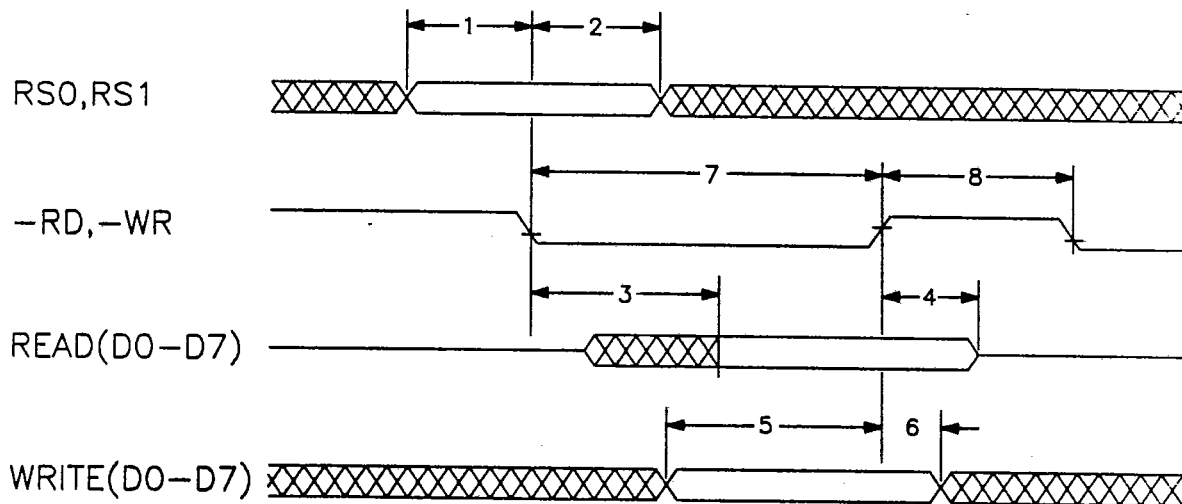
PARAMETER	MIN.	TYP	MAX	UNITS
Gray Scale Current Range	-----	-----	20.00	mA
White Level Relative to Blank	17.40	18.62	20.00	mA
White Level Relative to Black	17.40	18.62	20.00	mA
Black Level Relative to Blank	0	0	0	mA
Blank Level	6.90	8.05	9.2	mA
LSB Size	-----	295.56	-----	uA

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T-52-33-45**A. C. CHARACTERISTICS****MPU READ/WRITE TIMING DIAGRAM**

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS
1	RS0, RS1 Setup Time	10	----	----	ns
2	RS0, RS1 Hold Time	10	----	----	ns
3	-RD to Data Valid	----	----	40	ns
4	-RD Negated To Data Bus 3-States	5	----	----	ns
5	Write Data Setup Time	10	----	----	ns
6	Write Data Hold Time	10	----	----	ns
7	-RD, -WR Pulse Width Low	50	----	----	ns
8	-RD, -WR Pulse Width High	4 * PCLK	----	----	ns



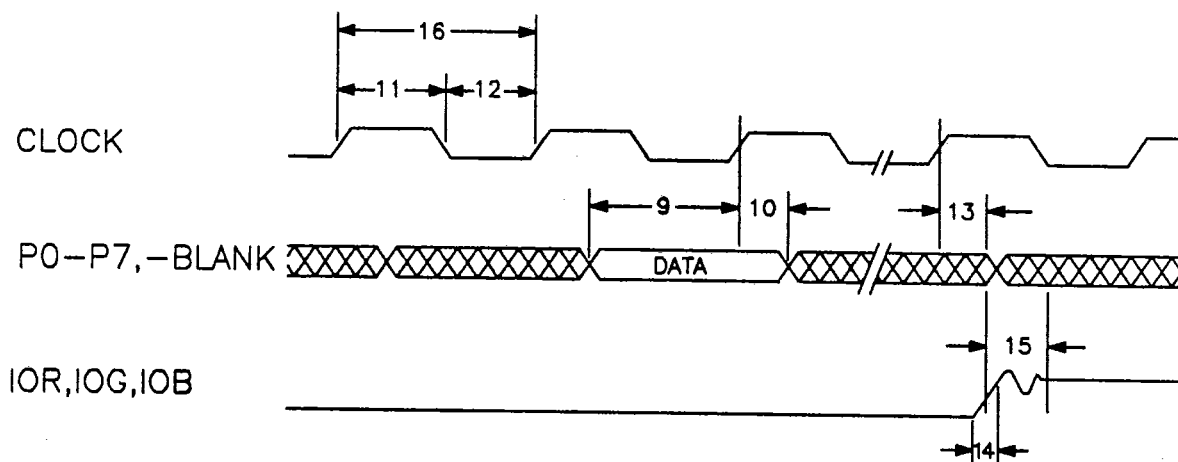
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A. C. CHARACTERISTICS (Cont'd)**VIDEO INPUT/OUTPUT TIMING DIAGRAM**

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS
11	Clock Pulse Width Low Time	6	----	----	ns
12	Clock Pulse Width High Time	6	----	----	ns
9	Pixel and -BLANK Setup Time	4	----	----	ns
10	Pixel and -BLANK Hold Time	4	----	----	ns
13	Analog Output Delay	----	----	30	ns
14	Analog Output Rise/Fall Time	----	2	----	ns
15	Analog Output Settling Time	----	15	----	ns
16	Clock Frequency	----	----	50	MHz



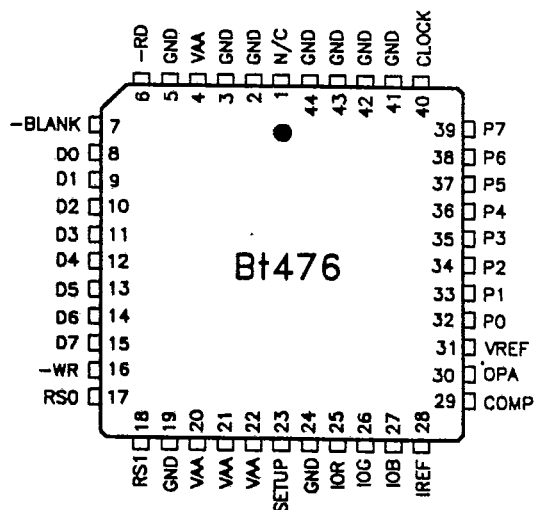
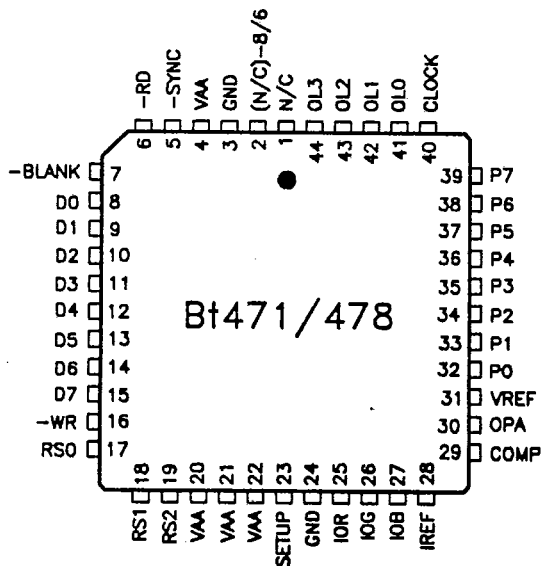
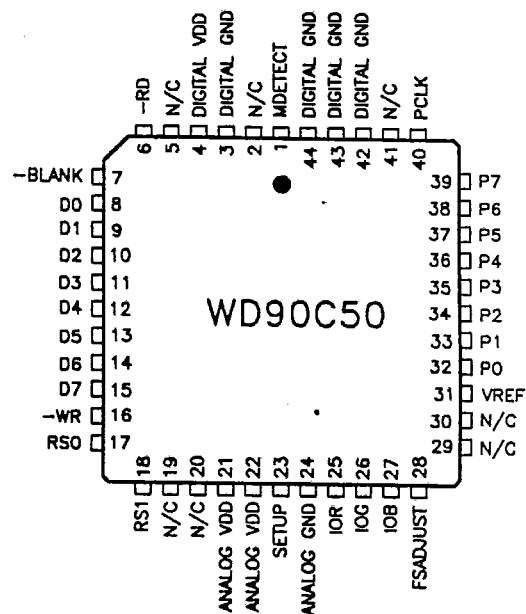
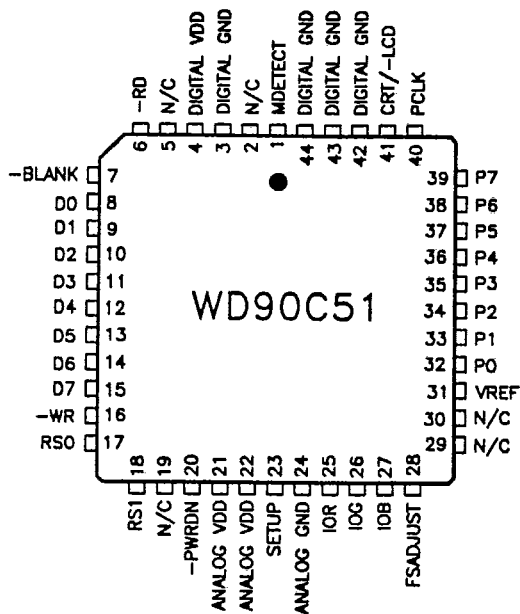
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APPLICATIONS

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WD90C50, Bt471/478 and Bt476 Pin-Compatibility



NOTES:

1. The WD90C51 is pin-compatible with WD90C50, and can easily replace Brooktree's Bt471/478 and Bt476 on a VGA board. Refer to the table on the following page.
2. The WD90C51 provides on chip monitor detection logic, reducing video subsystem cost.
3. In a typical application, WD90C51 functions the same as the WD90C50, Bt471/478 and Bt476. In addition, the WD90C51 supports intelligent power down control for power critical applications such as a laptop computer.
4. Note that the "RSET" resistor value necessary for the WD90C51 is different than for the Bt471/478 and Bt476 chips.

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APPLICATIONS (Cont'd)**T-52-33-45****WD90C50, Bt471/478, and Bt476 Pin-Compatibility**

<u>WD90C51</u>		<u>WD90C50</u>		<u>Bt471/478</u>		<u>Bt476</u>	
<u>PIN</u>	<u>SYMBOL</u>	<u>PIN</u>	<u>SYMBOL</u>	<u>PIN</u>	<u>SYMBOL</u>	<u>PIN</u>	<u>SYMBOL</u>
1	MDETECT	1	MDETECT	1	N/C	1	N/C
2	N/C	2	N/C	2	(N/C) -8/6	2	GND
3	Digital GND	3	Digital GND	3	GND	3	GND
4	Digital VDD	4	Digital VDD	4	V _{AA}	4	V _{AA}
5	N/C	5	N/C	5	-SYNC	5	GND
6	-RD	6	-RD	6	-RD	6	-RD
7	-BLANK	7	-BLANK	7	-BLANK	7	-BLANK
8	D0	8	D0	8	D0	8	D0
9	D1	9	D1	9	D1	9	D1
10	D2	10	D2	10	D2	10	D2
11	D3	11	D3	11	D3	11	D3
12	D4	12	D4	12	D4	12	D4
13	D5	13	D5	13	D5	13	D5
14	D6	14	D6	14	D6	14	D6
15	D7	15	D7	15	D7	15	D7
16	-WR	16	-WR	16	-WR	16	-WR
17	RS0	17	RS0	17	RS0	17	RS0
18	RS1	18	RS1	18	RS1	18	RS1
19	N/C	19	N/C	19	RS2	19	GND
20	-PWRDN	20	N/C	20	V _{AA}	20	V _{AA}
21	Analog VDD	21	Analog VDD	21	V _{AA}	21	V _{AA}
22	Analog VDD	22	Analog VDD	22	V _{AA}	22	V _{AA}
23	SETUP	23	SETUP	23	SETUP	23	SETUP
24	Analog GND	24	Analog GND	24	GND	24	GND
25	IOR	25	IOR	25	IOR	25	IOR
26	IOG	26	IOG	26	IOG	26	IOG
27	IOB	27	IOB	27	IOB	27	IOB
28	FSADJUST	28	FSADJUST	28	IREF	28	IREF
29	N/C	29	N/C	29	COMP	29	COMP
30	N/C	30	N/C	30	OPA	30	OPA
31	VREF	31	VREF	31	VREF	31	VREF
32	P0	32	P0	32	P0	32	P0
33	P1	33	P1	33	P1	33	P1
34	P2	34	P2	34	P2	34	P2
35	P3	35	P3	35	P3	35	P3
36	P4	36	P4	36	P4	36	P4
37	P5	37	P5	37	P5	37	P5
38	P6	38	P6	38	P6	38	P6
39	P7	39	P7	39	P7	39	P7
40	PCLK	40	PCLK	40	CLK	40	CLK
41	CRT/LCD	41	N/C	41	OL0	41	GND
42	Digital GND	42	Digital GND	42	OL1	42	GND
43	Digital GND	43	Digital GND	43	OL2	43	GND
44	Digital GND	44	Digital GND	44	OL3	44	GND

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APPLICATIONS (Cont'd)

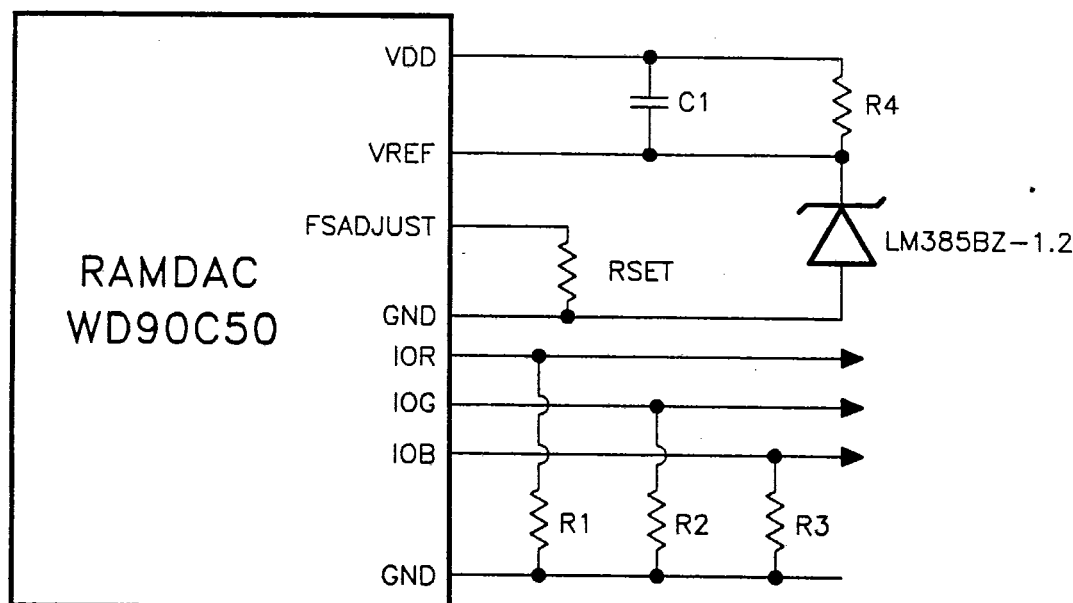
EXTERNAL VOLTAGE REFERENCE

An external voltage reference is used for DAC interface. The band-gap voltage regulator diode (LM385 - 1.2) is a simple, low cost regulator providing excellent power supply rejection and temperature compensation.

The RSET resistor controls the magnitude of the full scale video signal. This is defined as 1.0V full scale output into a 37.5-Ohm load. The relationship between RSET and full scale output current (= 26.67mA) is:

$$RSET \text{ (ohms)} = K * VREF (= 1.235 \text{ V}) / IOUT \text{ (mA)}$$

<u>BLACK TO BLANK RANGE (pedestal)</u>	<u>K</u>	<u>RSET (ohms)</u>
0 IRE	3.7898	175.49
7.5 IRE	4.0050	185.45



Notes:

1. C1 is a 0.1 uF Ceramic Capacitor.
2. R4 is a 1K-Ohm 5% Resistor.
3. RSET is a 174-Ohm or 187-Ohm 1% Metal-Film Resistor.
4. R1, R2, and R3 are 75-Ohm 1% Metal-Film Resistors.

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T-52-33-45**44-PIN PLCC**