# 512 Kbit / 1 Mbit / 2 Mbit (x8) Many-Time Programmable Flash
## SST27SF512 / SST27SF010 / SST27SF020

## FEATURES:

- **Organized as 64K x8 / 128K x8 / 256K x8**
- **4.5-5.5V Read Operation**
- **Superior Reliability**
  - Endurance: At least 1000 Cycles
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Current: 20 mA (typical)
  - Standby Current: 10 µA (typical)
- **Fast Read Access Time**
  - 70 ns

- **Fast Byte-Program Operation**
  - Byte-Program Time: 20 µs (typical)
  - Chip Program Time:
    1.4 seconds (typical) for SST27SF512
    2.8 seconds (typical) for SST27SF010
    5.6 seconds (typical) for SST27SF020
- **Electrical Erase Using Programmer**
  - Does not require UV source
  - Chip-Erase Time: 100 ms (typical)
- **TTL I/O Compatibility**
- **JEDEC Standard Byte-wide EPROM Pinouts**
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)
  - 32-pin PDIP for SST27SF010/020
- **All non-Pb (lead-free) devices are RoHS compliant**

## PRODUCT DESCRIPTION

The SST27SF512/010/020 are a 64K x8 / 128K x8 / 256K x8 CMOS, Many-Time Programmable (MTP) low cost flash, manufactured with SST's proprietary, high performance SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. These MTP devices can be electrically erased and programmed at least 1000 times using an external programmer with a 12V power supply. They have to be erased prior to programming. These devices conform to JEDEC standard pinouts for byte-wide memories.

Featuring high-performance Byte-Program, the SST27SF512/010/020 provide a Byte-Program time of 20 µs. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with an endurance of at least 1000 cycles. Data retention is rated at greater than 100 years.

The SST27SF512/010/020 are suited for applications that require infrequent writes and low power nonvolatile storage. These devices will improve flexibility, efficiency, and performance while matching the low cost in nonvolatile applications that currently use UV-EPROMs, OTPs, and mask ROMs.

To meet surface mount and conventional through hole requirements, the SST27SF512 are offered in 32-lead PLCC, 32-lead TSOP, and 28-pin PDIP packages. The SST27SF010/020 are offered in 32-pin PDIP, 32-lead PLCC, and 32-lead TSOP packages. See Figures 3, 4, and 5 for pin assignments.

## Device Operation

The SST27SF512/010/020 are a low cost flash solution that can be used to replace existing UV-EPROM, OTP, and mask ROM sockets. These devices are functionally (read and program) and pin compatible with industry standard EPROM products. In addition to EPROM functionality, these devices also support electrical Erase operation via an external programmer. They do not require a UV source to erase, and therefore the packages do not have a window.

## Read

The Read operation of the SST27SF512/010/020 is controlled by CE# and OE#. Both CE# and OE# have to be low for the system to obtain data from the outputs. Once the address is stable, the address access time is equal to the delay from CE# to output ($T_{CE}$). Data is available at the output after a delay of $T_{OE}$ from the falling edge of OE#, assuming that CE# pin has been low and the addresses have been stable for at least $T_{CE}$-$T_{OE}$. When the CE# pin is high, the chip is deselected and a typical standby current of 10 µA is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high.

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## Byte-Program Operation

The SST27SF512/010/020 are programmed by using an external programmer. The programming mode for SST27SF010/020 is activated by asserting 11.4-12V on $V_{PP}$ pin, $V_{DD}$ = 4.5-5.5V, $V_{IL}$ on CE# pin, and $V_{IH}$ on OE# pin. The programming mode for SST27SF512 is activated by asserting 11.4-12V on OE#/$V_{PP}$ pin, $V_{DD}$ = 4.5-5.5V, and $V_{IL}$ on CE# pin. These devices are programmed byte-by-byte with the desired data at the desired address using a single pulse (CE# pin low for SST27SF512 and PGM# pin low for SST27SF010/020) of 20 μs. Using the MTP programming algorithm, the Byte-Programming process continues byte-by-byte until the entire chip has been programmed.

## Chip-Erase Operation

The only way to change a data from a "0" to "1" is by electrical erase that changes every bit in the device to "1". Unlike traditional EPROMs, which use UV light to do the Chip-Erase, the SST27SF512/010/020 uses an electrical Chip-Erase operation. This saves a significant amount of time (about 30 minutes for each Erase operation). The entire chip can be erased in a single pulse of 100 ms (CE# pin low for SST27SF512 and PGM# pin for SST27SF010/020). In order to activate the Erase mode for SST27SF010/020, the 11.4-12V is applied to $V_{PP}$ and $A_9$ pins, $V_{DD}$ = 4.5-5.5V, $V_{IL}$ on CE# pin, and $V_{IH}$ on OE# pin. In order to activate Erase mode for SST27SF512, the 11.4-12V is applied to OE#/$V_{PP}$ and $A_9$ pins, $V_{DD}$ = 4.5-5.5V, and $V_{IL}$ on CE# pin. All other address and data pins are "don't care". The falling edge of CE# (PGM# for SST27SF010/020) will start the Chip-Erase operation. Once the chip has been erased, all bytes must be verified for FFH. Refer to Figures 13 and 14 for the flowcharts.

## Product Identification Mode

The Product Identification mode identifies the devices as the SST27SF512, SST27SF010 and SST27SF020 and manufacturer as SST. This mode may be accessed by the hardware method. To activate this mode for SST27SF010/020, the programming equipment must force $V_H$ (11.4-12V) on address $A_9$ with $V_{PP}$ pin at $V_{DD}$ (4.5-5.5V) or $V_{SS}$. To activate this mode for SST27SF512, the programming equipment must force $V_H$ (11.4-12V) on address $A_9$ with OE#/$V_{PP}$ pin at $V_{IL}$. Two identifier bytes may then be sequenced from the device outputs by toggling address line $A_0$. For details, see Tables 3 and 4 for hardware operation.

**TABLE  1: Product Identification**

|  | Address | Data |
| --- | --- | --- |
| Manufacturer's ID | 0000H | BFH |
| Device ID |  |  |
| SST27SF512 | 0001H | A4H |
| SST27SF010 | 0001H | A5H |
| SST27SF020 | 0001H | A6H |

T1.2  1152
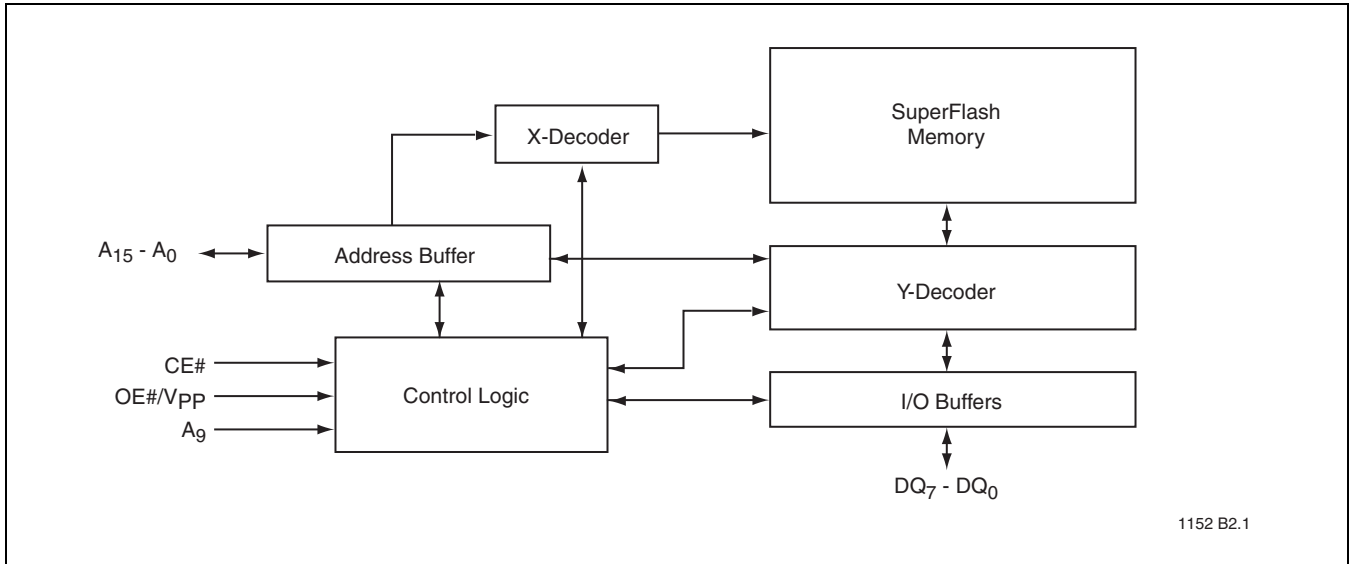
**FIGURE  1: Functional Block Diagram - SST27SF512**



$A_{MS} = A_{17}$ for SST27SF020, $A_{16}$ for SST27SF010
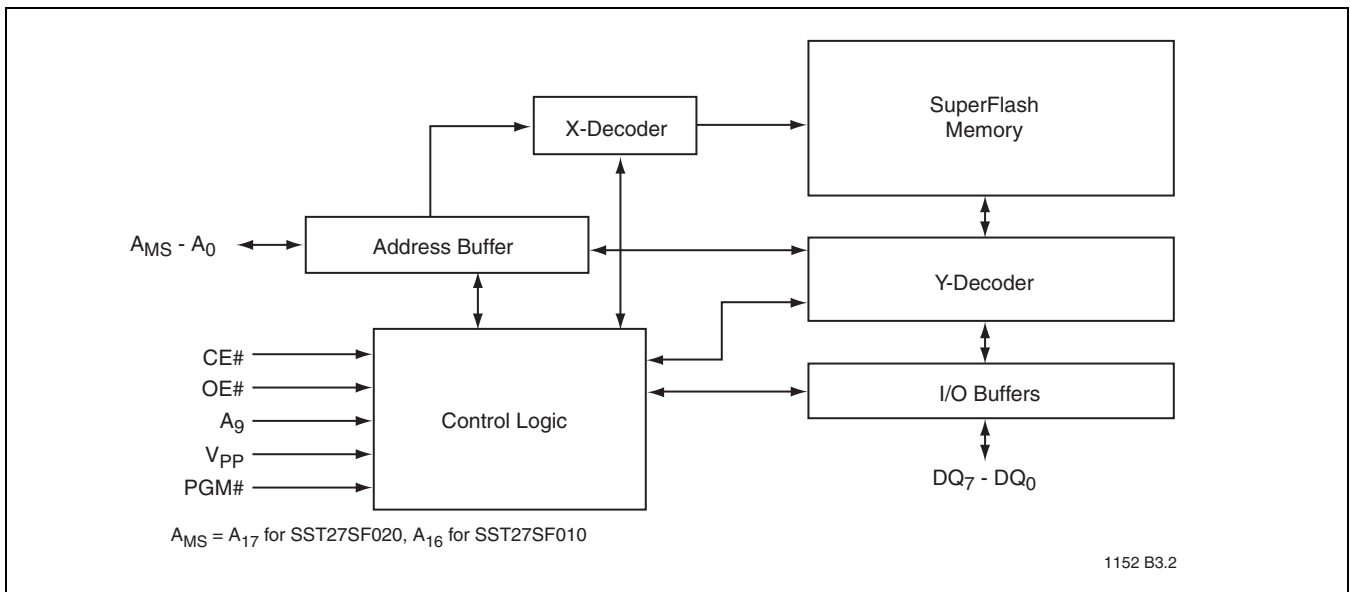
**FIGURE  2: Functional Block Diagram - SST27SF010/020**

S71152-12-000      9/08
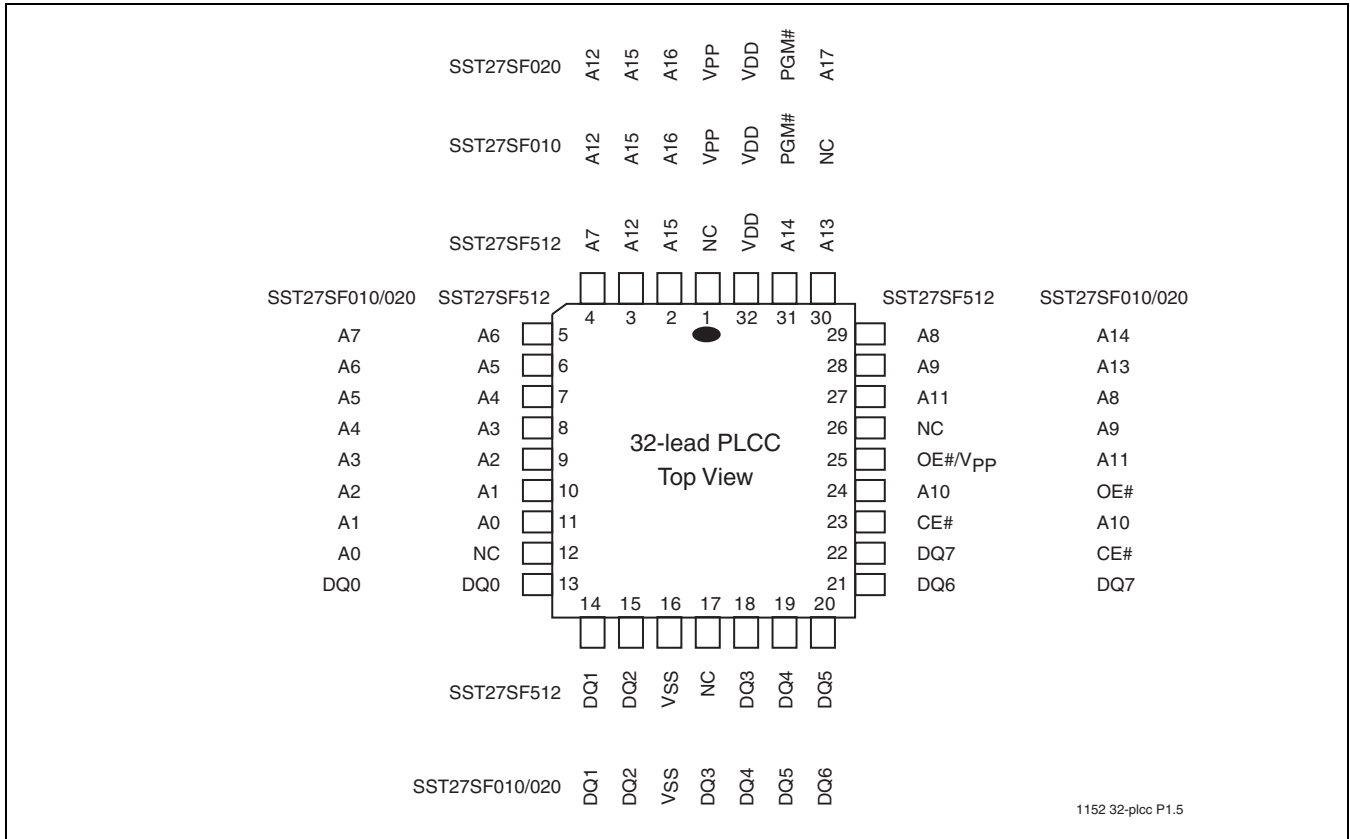
**FIGURE  3: Pin Assignments for 32-lead PLCC**
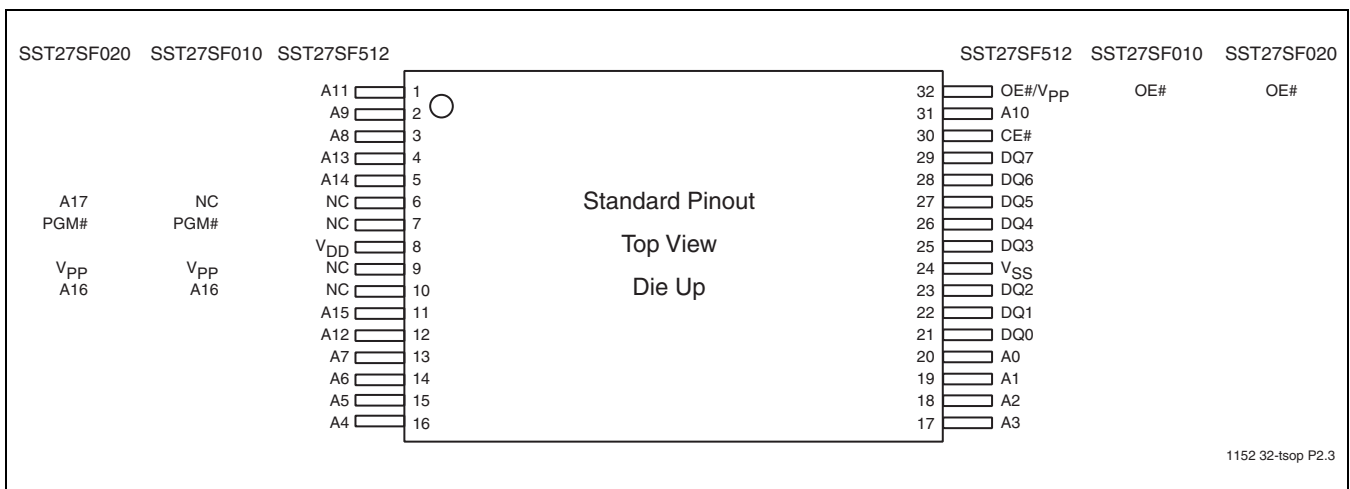


**FIGURE  4: Pin Assignments for 32-lead TSOP (8mm x 14mm)**

S71152-12-000        9/08
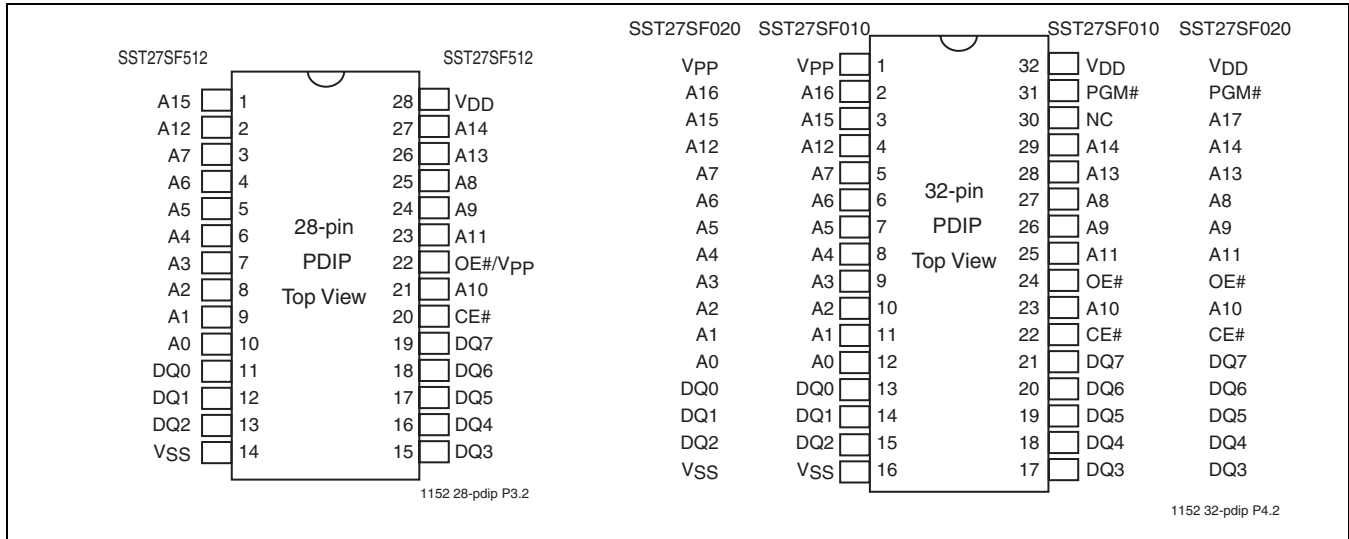
**FIGURE  5: Pin Assignments for 28-pin and 32-pin PDIP**

**TABLE  2: Pin Description**

| Symbol | Pin Name | Functions |
|---|---|---|
| $A_{MS}$[1]-$A_0$ | Address Inputs | To provide memory addresses |
| $DQ_7$-$DQ_0$ | Data Input/output | To output data during Read cycles and receive input data during Program cycles<br>The outputs are in tri-state when OE# or CE# is high. |
| CE# | Chip Enable | To activate the device when CE# is low |
| OE# | Output Enable | For SST27SF010/020, to gate the data output buffers during Read operation |
| OE#/$V_{PP}$ | Output Enable/$V_{PP}$ | For SST27SF512, to gate the data output buffers during Read operation and high voltage pin during Chip-Erase and programming operation |
| $V_{PP}$ | Power Supply for Program or Erase | For SST27SF010/020, high voltage pin during Chip-Erase and programming operation 11.4-12V |
| $V_{DD}$ | Power Supply | To provide 5.0V supply (4.5-5.5V) |
| $V_{SS}$ | Ground | |
| NC | No Connection | Unconnected pins. |

T2.4 1152

1. $A_{MS}$ = Most significant address
   $A_{MS}$ = $A_{15}$ for SST27SF512, $A_{16}$ for SST27SF010, and $A_{17}$ for SST27SF020

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**TABLE   3: Operation Modes Selection for SST27SF512**

| Mode | CE# | OE#/$V_{PP}$ | $A_9$ | DQ | Address |
|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $A_{IN}$ | $D_{OUT}$ | $A_{IN}$ |
| Output Disable | $V_{IL}$ | $V_{IH}$ | $X^1$ | High Z | X |
| Program | $V_{IL}$ | $V_{PPH}$ | $A_{IN}$ | $D_{IN}$ | $A_{IN}$ |
| Standby | $V_{IH}$ | X | X | High Z | X |
| Chip-Erase | $V_{IL}$ | $V_{PPH}$ | $V_H$ | High Z | X |
| Program/Erase Inhibit | $V_{IH}$ | $V_{PPH}$ | X | High Z | X |
| Product Identification | $V_{IL}$ | $V_{IL}$ | $V_H$ | Manufacturer's ID (BFH)<br>Device ID (A4H) | $A_{15}$-$A_1$=$V_{IL}$, $A_0$=$V_{IL}$<br>$A_{15}$-$A_1$=$V_{IL}$, $A_0$=$V_{IH}$ |

T3.2 1152

1. X can be $V_{IL}$ or $V_{IH,}$ but no other value.
**Note:** $V_{PPH}$ = 11.4-12V, $V_H$ = 11.4-12V

**TABLE   4: Operation Modes Selection for SST27SF010/020**

| Mode | CE# | OE# | PGM# | $A_9$ | $V_{PP}$ | DQ | Address |
|---|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $X^1$ | $A_{IN}$ | $V_{DD}$ or $V_{SS}$ | $D_{OUT}$ | $A_{IN}$ |
| Output Disable | $V_{IL}$ | $V_{IH}$ | X | X | $V_{DD}$ or $V_{SS}$ | High Z | $A_{IN}$ |
| Program | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $A_{IN}$ | $V_{PPH}$ | $D_{IN}$ | $A_{IN}$ |
| Standby | $V_{IH}$ | X | X | X | $V_{DD}$ or $V_{SS}$ | High Z | X |
| Chip-Erase | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_H$ | $V_{PPH}$ | High Z | X |
| Program/Erase Inhibit | $V_{IH}$ | X | X | X | $V_{PPH}$ | High Z | X |
| Product Identification | $V_{IL}$ | $V_{IL}$ | X | $V_H$ | $V_{DD}$ or $V_{SS}$ | Manufacturer's ID (BFH)<br>Device ID[2] | $A_{MS}^3$ - $A_1$=$V_{IL}$, $A_0$=$V_{IL}$<br>$A_{MS}^3$ - $A_1$=$V_{IL}$, $A_0$=$V_{IH}$ |

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1. X can be $V_{IL}$ or $V_{IH,}$ but no other value.
2. Device ID = A5H for SST27SF010 and A6H for SST27SF020
3. $A_{MS}$ = Most significant address
   $A_{MS}$ = $A_{16}$ for SST27SF010 and $A_{17}$ for SST27SF020
**Note:** $V_{PPH}$ = 11.4-12V, $V_H$ = 11.4-12V

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -55°C to +125°C

Storage Temperature  . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -65°C to +150°C

D. C. Voltage on Any Pin to Ground Potential . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .-0.5V to $V_{DD}$+0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential  . . . . . . . . . . . . . . . . . . . . . . . . . . . . .-2.0V to $V_{DD}$+2.0V

Voltage on $A_9$ and $V_{PP}$ Pin to Ground Potential  . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.5V to 14.0V

Package Power Dissipation Capability ($T_A$ = 25°C) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1.0W

Through Hole Lead Soldering Temperature (10 Seconds) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 300°C

Surface Mount Solder Reflow Temperature[1] . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 260°C for 10 seconds

Output Short Circuit Current[2] . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 100 mA

    1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions.
       Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
    2. Outputs shorted for no more than one second. No more than one output shorted at a time.

**OPERATING RANGE**

| Range | Ambient Temp | $V_{DD}$ | $V_{PP}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 4.5-5.5V | 11.4-12V |

**AC CONDITIONS OF TEST**

Input Rise/Fall Time . . . . . . . . . . . 10 ns

Output Load . . . . . . . . . . . . . . . . $C_L$ = 30 pF for 70 ns

See Figures 11 and 12

**TABLE 5: Read Mode DC Operating Characteristics for SST27SF512/010/020**
        $V_{DD}$ = 4.5-5.5V, $V_{PP}$=$V_{DD}$ or $V_{SS}$ ($T_A$ = 0°C to +70°C (Commercial))

| Symbol | Parameter | Limits Min | Limits Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $I_{DD}$ | $V_{DD}$ Read Current | | 30 | mA | Address input=$V_{ILT}$/$V_{IHT}$ at f=1/$T_{RC}$ Min $V_{DD}$=$V_{DD}$ Max CE#=OE#=$V_{IL}$, all I/Os open |
| $I_{PPR}$ | $V_{PP}$ Read Current | | 100 | µA | Address input=$V_{ILT}$/$V_{IHT}$ at f=1/$T_{RC}$ Min $V_{DD}$=$V_{DD}$ Max, $V_{PP}$=$V_{DD}$ CE#=OE#=$V_{IL}$, all I/Os open |
| $I_{SB1}$ | Standby $V_{DD}$ Current (TTL input) | | 3 | mA | CE#=$V_{IH}$, $V_{DD}$=$V_{DD}$ Max |
| $I_{SB2}$ | Standby $V_{DD}$ Current (CMOS input) | | 100 | µA | CE#=$V_{DD}$-0.3 $V_{DD}$=$V_{DD}$ Max |
| $I_{LI}$ | Input Leakage Current | | 1 | µA | $V_{IN}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $I_{LO}$ | Output Leakage Current | | 10 | µA | $V_{OUT}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $V_{IL}$ | Input Low Voltage | | 0.8 | V | $V_{DD}$=$V_{DD}$ Min |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{DD}$+0.5 | V | $V_{DD}$=$V_{DD}$ Max |
| $V_{OL}$ | Output Low Voltage | | 0.2 | V | $I_{OL}$=2.1 mA, $V_{DD}$=$V_{DD}$ Min |
| $V_{OH}$ | Output High Voltage | 2.4 | | V | $I_{OH}$=-400 µA, $V_{DD}$=$V_{DD}$ Min |
| $I_H$ | Supervoltage Current for $A_9$ | | 200 | µA | CE#=OE#=$V_{IL}$, $A_9$=$V_H$ Max |

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### TABLE 6: Program/Erase DC Operating Characteristics for SST27SF512
$V_{DD}$=4.5-5.5V, $V_{PP}$=$V_{PPH}$ ($T_A$=25°C±5°C)

| Symbol | Parameter | Limits | | | Test Conditions |
| | | Min | Max | Units | |
|---|---|---|---|---|---|
| $I_{DD}$ | $V_{DD}$ Erase or Program Current | | 30 | mA | CE#=$V_{IL}$, OE#/$V_{PP}$=11.4-12V, $V_{DD}$=$V_{DD}$ Max |
| $I_{PP}$ | $V_{PP}$ Erase or Program Current | | 3 | mA | CE#=$V_{IL}$, OE#/$V_{PP}$=11.4-12V, $V_{DD}$=$V_{DD}$ Max |
| $I_{LI}$ | Input Leakage Current | | 1 | μA | $V_{IN}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $I_{LO}$ | Output Leakage Current | | 10 | μA | $V_{OUT}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $V_H$ | Supervoltage for $A_9$ | 11.4 | 12 | V | CE#=OE#/$V_{PP}$=$V_{IL}$, |
| $I_H$ | Supervoltage Current for $A_9$ | | 200 | μA | CE#=OE#/$V_{PP}$=$V_{IL}$, $A_9$=$V_H$ Max |
| $V_{PPH}$ | High Voltage for OE#/$V_{PP}$ Pin | 11.4 | 12 | V | |

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### TABLE 7: Program/Erase DC Operating Characteristics for SST27SF010/020
$V_{DD}$=4.5-5.5V, $V_{PP}$=$V_{PPH}$ ($T_A$=25°C±5°C)

| Symbol | Parameter | Limits | | | Test Conditions |
| | | Min | Max | Units | |
|---|---|---|---|---|---|
| $I_{DD}$ | $V_{DD}$ Erase or Program Current | | 30 | mA | CE#=PGM#=$V_{IL}$, OE#=$V_{IH}$, $V_{PP}$=11.4-12V, $V_{DD}$=$V_{DD}$ Max |
| $I_{PP}$ | $V_{PP}$ Erase or Program Current | | 3 | mA | CE#=PGM#=$V_{IL}$, OE#=$V_{IH}$, $V_{PP}$=11.4-12V, $V_{DD}$=$V_{DD}$ Max |
| $I_{LI}$ | Input Leakage Current | | 1 | μA | $V_{IN}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $I_{LO}$ | Output Leakage Current | | 10 | μA | $V_{OUT}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $V_H$ | Supervoltage for $A_9$ | 11.4 | 12 | V | CE#=OE#=$V_{IL}$, |
| $I_H$ | Supervoltage Current for $A_9$ | | 200 | μA | CE#=OE#=$V_{IL}$, $A_9$=$V_H$ Max |
| $V_{PPH}$ | High Voltage for $V_{PP}$ Pin | 11.4 | 12 | V | |

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### TABLE 8: Recommended System Power-up Timings

| Symbol | Parameter | Minimum | Units |
|---|---|---|---|
| $T_{PU-READ}$[1] | Power-up to Read Operation | 100 | μs |
| $T_{PU-WRITE}$[1] | Power-up to Write Operation | 100 | μs |

T8.1  1152

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

### TABLE 9: Capacitance ($T_A$ = 25°C, f=1 Mhz, other pins open)

| Parameter | Description | Test Condition | Maximum |
|---|---|---|---|
| $C_{I/O}$[1] | I/O Pin Capacitance | $V_{I/O}$ = 0V | 12 pF |
| $C_{IN}$[1] | Input Capacitance | $V_{IN}$ = 0V | 6 pF |

T9.0  1152

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

### TABLE 10: Reliability Characteristics

| Symbol | Parameter | Minimum Specification | Units | Test Method |
|---|---|---|---|---|
| $N_{END}$[1] | Endurance | 1000 | Cycles | JEDEC Standard A117 |
| $T_{DR}$[1] | Data Retention | 100 | Years | JEDEC Standard A103 |

T10.3  1152

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

## AC CHARACTERISTICS

**TABLE 11: Read Cycle Timing Parameters $V_{DD}$ = 4.5-5.5V** ($T_A$ = 0°C to +70°C (Commercial))

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{RC}$ | Read Cycle Time | 70 | | ns |
| $T_{CE}$ | Chip Enable Access Time | | 70 | ns |
| $T_{AA}$ | Address Access Time | | 70 | ns |
| $T_{OE}$ | Output Enable Access Time | | 35 | ns |
| $T_{CLZ}$[1] | CE# Low to Active Output | 0 | | ns |
| $T_{OLZ}$[1] | OE# Low to Active Output | 0 | | ns |
| $T_{CHZ}$[1] | CE# High to High-Z Output | | 25 | ns |
| $T_{OHZ}$[1] | OE# High to High-Z Output | | 25 | ns |
| $T_{OH}$[1] | Output Hold from Address Change | 0 | | ns |

T11.3  1152

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 12: Program/Erase Cycle Timing Parameters for SST27SF512**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{AS}$ | Address Setup Time | 1 | | µs |
| $T_{AH}$ | Address Hold Time | 1 | | µs |
| $T_{PRT}$ | OE#/$V_{PP}$ Pulse Rise Time | 50 | | ns |
| $T_{VPS}$ | OE#/$V_{PP}$ Setup Time | 1 | | µs |
| $T_{VPH}$ | OE#/$V_{PP}$ Hold Time | 1 | | µs |
| $T_{PW}$ | CE# Program Pulse Width | 20 | 30 | µs |
| $T_{EW}$ | CE# Erase Pulse Width | 100 | 500 | ms |
| $T_{DS}$ | Data Setup Time | 1 | | µs |
| $T_{DH}$ | Data Hold Time | 1 | | µs |
| $T_{VR}$ | OE#/$V_{PP}$ and $A_9$ Recovery Time | 1 | | µs |
| $T_{ART}$ | $A_9$ Rise Time to 12V during Erase | 50 | | ns |
| $T_{A9S}$ | $A_9$ Setup Time during Erase | 1 | | µs |
| $T_{A9H}$ | $A_9$ Hold Time during Erase | 1 | | µs |

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**TABLE 13: Program/Erase Cycle Timing Parameters for SST27SF010/020**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{CES}$ | CE# Setup Time | 1 | | µs |
| $T_{CEH}$ | CE# Hold Time | 1 | | µs |
| $T_{AS}$ | Address Setup Time | 1 | | µs |
| $T_{AH}$ | Address Hold Time | 1 | | µs |
| $T_{PRT}$ | $V_{PP}$ Pulse Rise Time | 50 | | ns |
| $T_{VPS}$ | $V_{PP}$ Setup Time | 1 | | µs |
| $T_{VPH}$ | $V_{PP}$ Hold Time | 1 | | µs |
| $T_{PW}$ | PGM# Program Pulse Width | 20 | 30 | µs |
| $T_{EW}$ | PGM# Erase Pulse Width | 100 | 500 | ms |
| $T_{DS}$ | Data Setup Time | 1 | | µs |
| $T_{DH}$ | Data Hold Time | 1 | | µs |
| $T_{VR}$ | $A_9$ Recovery Time for Erase | 1 | | µs |
| $T_{ART}$ | $A_9$ Rise Time to 12V during Erase | 50 | | ns |
| $T_{A9S}$ | $A_9$ Setup Time during Erase | 1 | | µs |
| $T_{A9H}$ | $A_9$ Hold Time during Erase | 1 | | µs |

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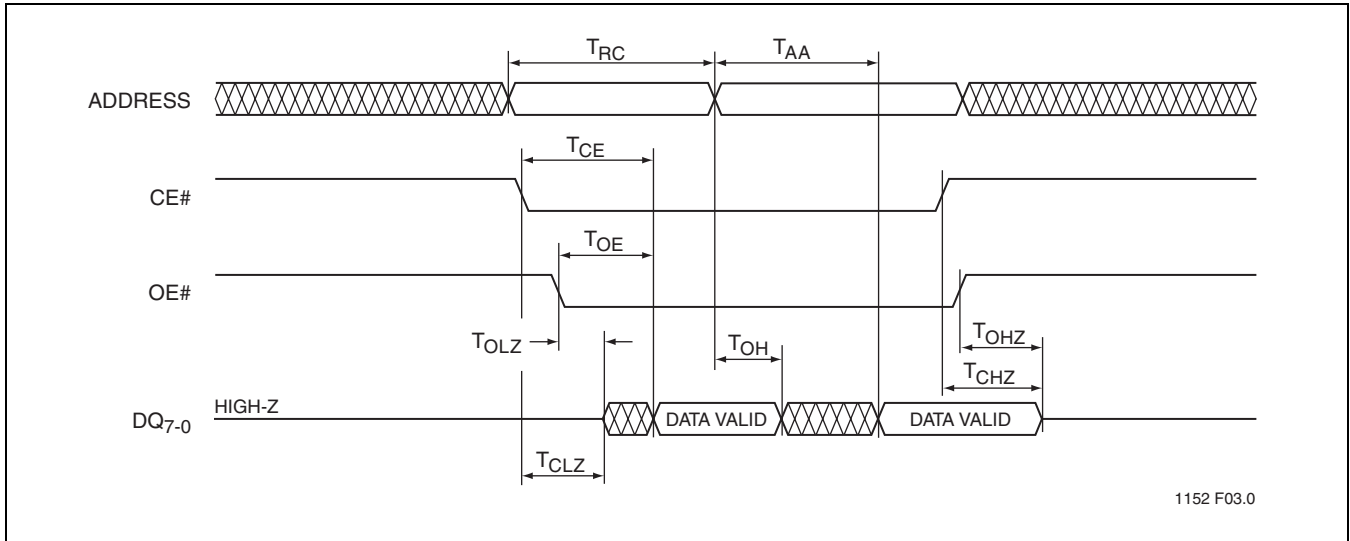
**FIGURE  6: Read Cycle Timing Diagram for SST27SF512/010/020**
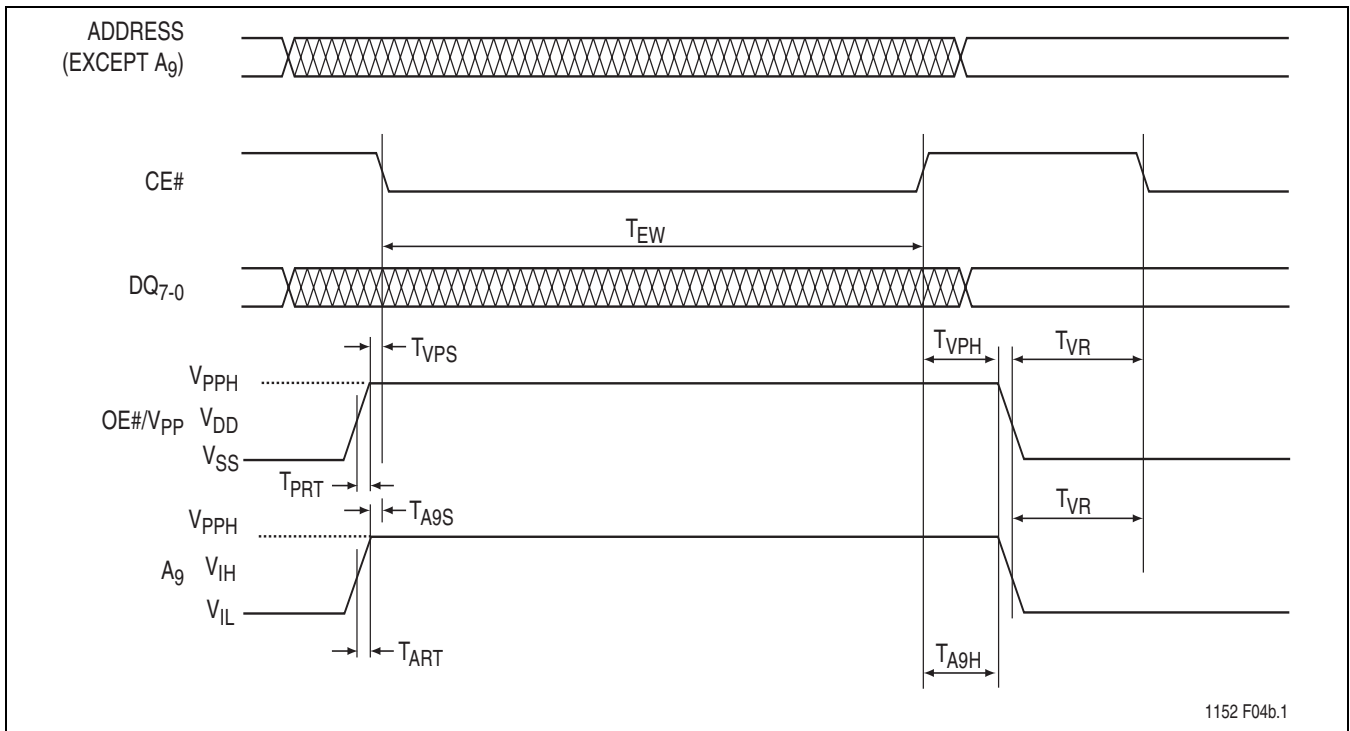


**FIGURE  7: Chip-Erase Timing Diagram for SST27SF512**
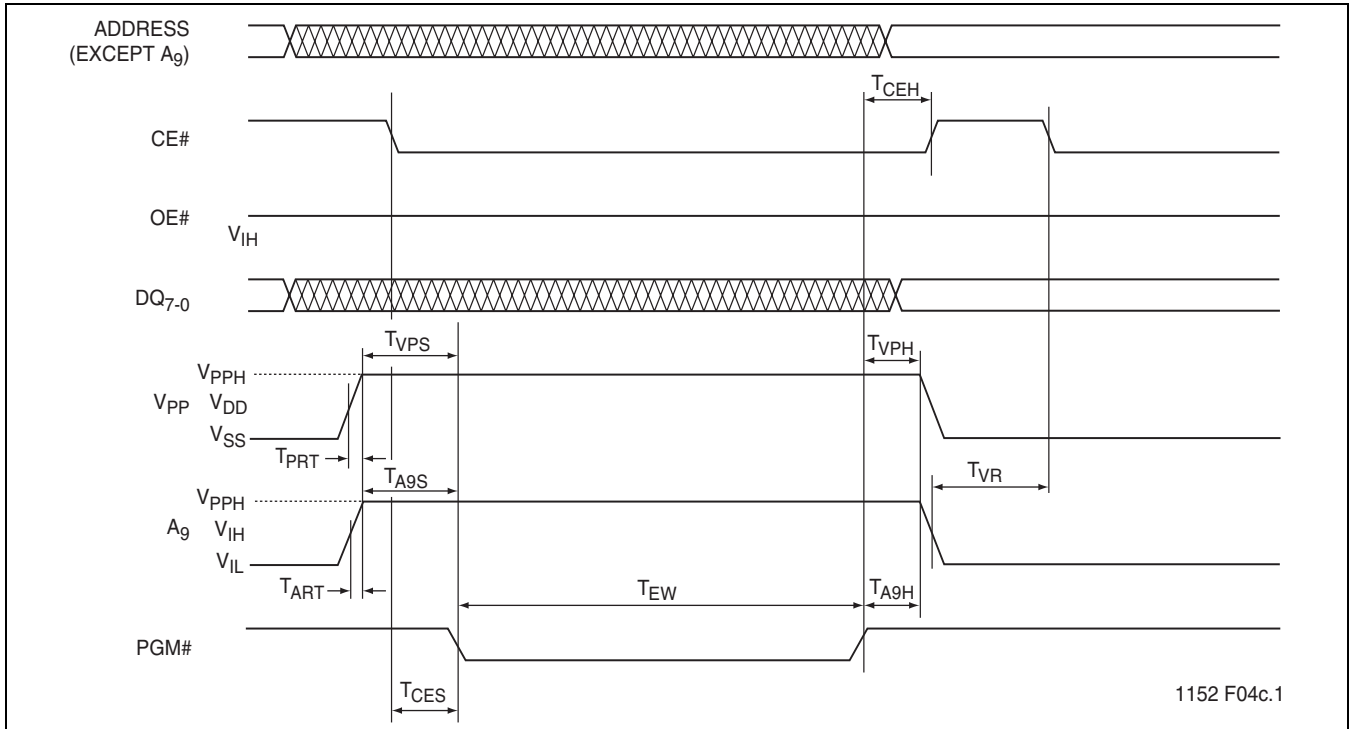
**FIGURE   8: Chip-Erase Timing Diagram for SST27SF010/020**
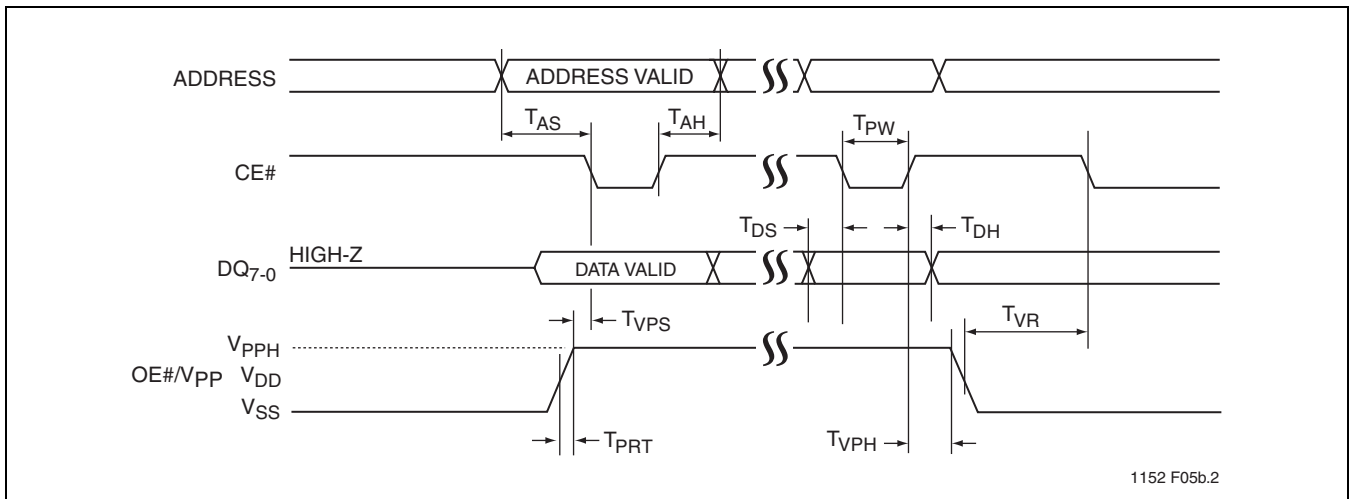


**FIGURE   9: Byte-Program Timing Diagram for SST27SF512**

S71152-12-000      9/08
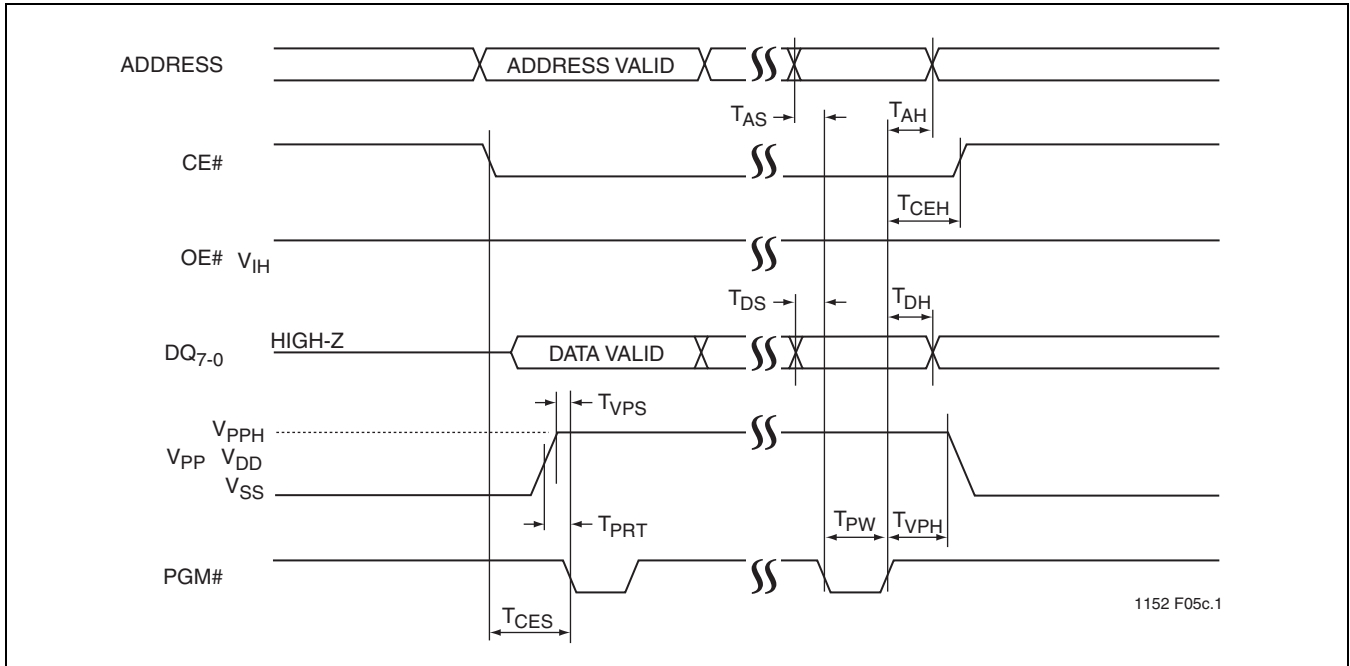
**FIGURE 10: Byte-Program Timing Diagram for SST27SF010/020**
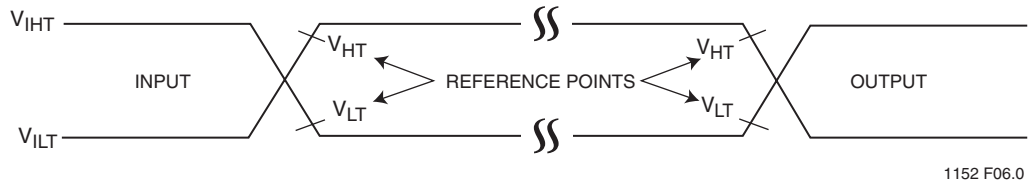
AC test inputs are driven at $V_{IHT}$ (2.4 V) for a logic "1" and $V_{ILT}$ (0.4 V) for a logic "0". Measurement reference points for inputs and outputs are $V_{HT}$ (2.0 V) and $V_{LT}$ (0.8 V). Input rise and fall times (10% ↔ 90%) are <10 ns.

**Note:** $V_{HT}$ - $V_{HIGH}$ Test
$V_{LT}$ - $V_{LOW}$ Test
$V_{IHT}$ - $V_{INPUT}$ HIGH Test
$V_{ILT}$ - $V_{INPUT}$ LOW Test

**FIGURE 11: AC Input/Output Reference Waveforms**
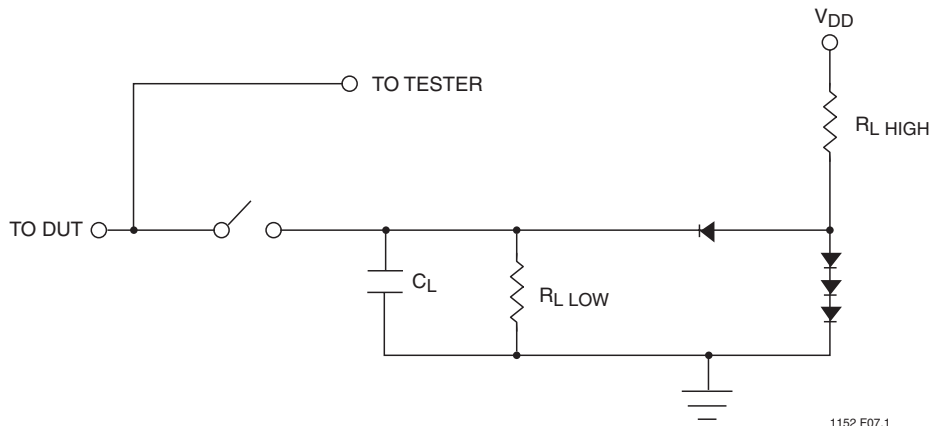


**FIGURE 12: A Test Load Example**

```
                          ┌─────────────────┐
                          │      Start       │
                          └─────────────────┘
                                   │
                          ┌─────────────────┐
                          │    A9 = VH       │
                          └─────────────────┘
                                   │
                          ┌─────────────────┐
                          │  OE#/VPP = VPPH  │
                          └─────────────────┘
                                   │
                          ┌─────────────────┐
                          │ Erase 100ms pulse│
                          │   (CE# = VIL)    │
                          └─────────────────┘
                                   │
                          ┌─────────────────────┐
                          │ OE#/VPP = VDD or VSS │
                          │  A9 = VIL or VIH     │
                          └─────────────────────┘
                                   │
                          ┌─────────────────┐
                          │ Wait for OE#/VPP and │
                          │  A9 Recovery Time   │
                          └─────────────────┘
                                   │
                          ┌─────────────────┐
                          │   Read Device    │
                          │ (CE# = OE# = VIL)│
                          └─────────────────┘
                                   │
                               ╱───────╲
                              ╱ Compare  ╲      No
                             ╱  All       ╲────────────┐
                             ╲  bytes to   ╱            │
                              ╲  FFH      ╱             │
                               ╲───────╱               │
                                  │ Yes                 │
                          ┌─────────────────┐   ┌─────────────────┐
                          │  Device Passed   │   │  Device Failed  │
                          └─────────────────┘   └─────────────────┘
```

$A_9 = V_H$

$OE\#/V_{PP} = V_{PPH}$

Erase 100ms pulse $(CE\# = V_{IL})$

$OE\#/V_{PP} = V_{DD}$ or $V_{SS}$
$A_9 = V_{IL}$ or $V_{IH}$

Wait for $OE\#/V_{PP}$ and $A_9$ Recovery Time

Read Device $(CE\# = OE\# = V_{IL})$
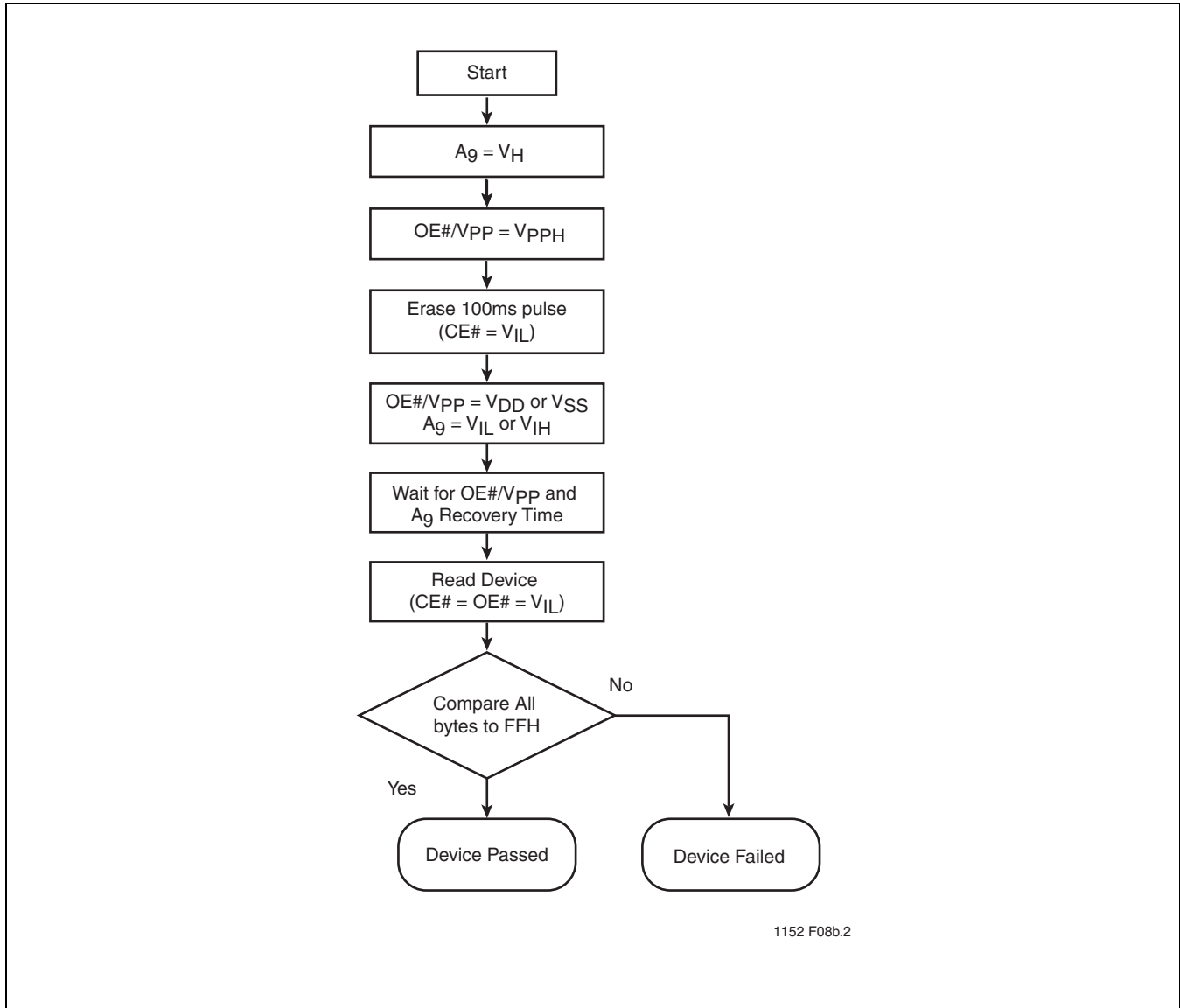
1152 F08b.2

**FIGURE 13:  Chip-Erase Algorithm for SST27SF512**
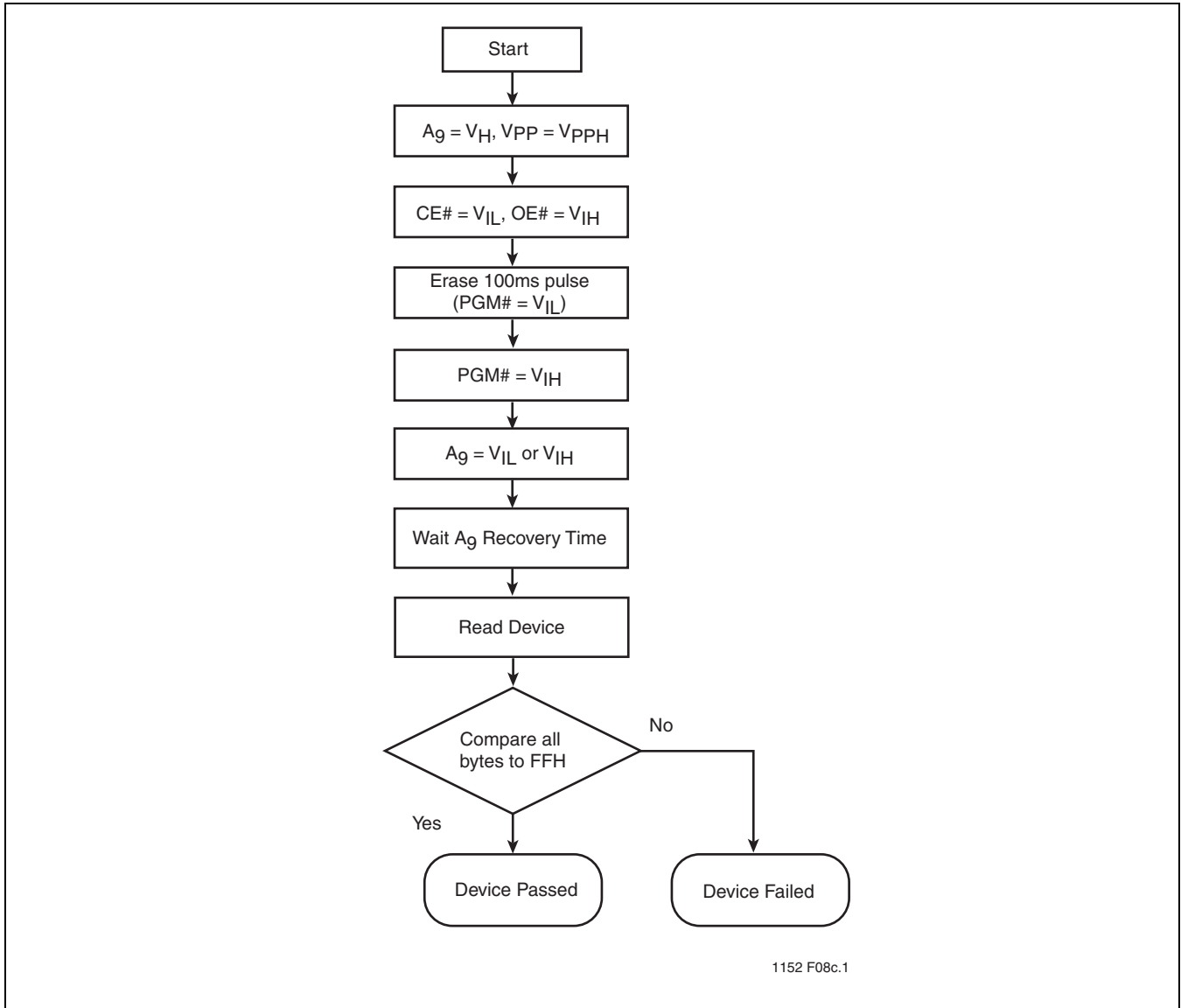
**FIGURE 14:  Chip-Erase Algorithm for SST27SF010/020**
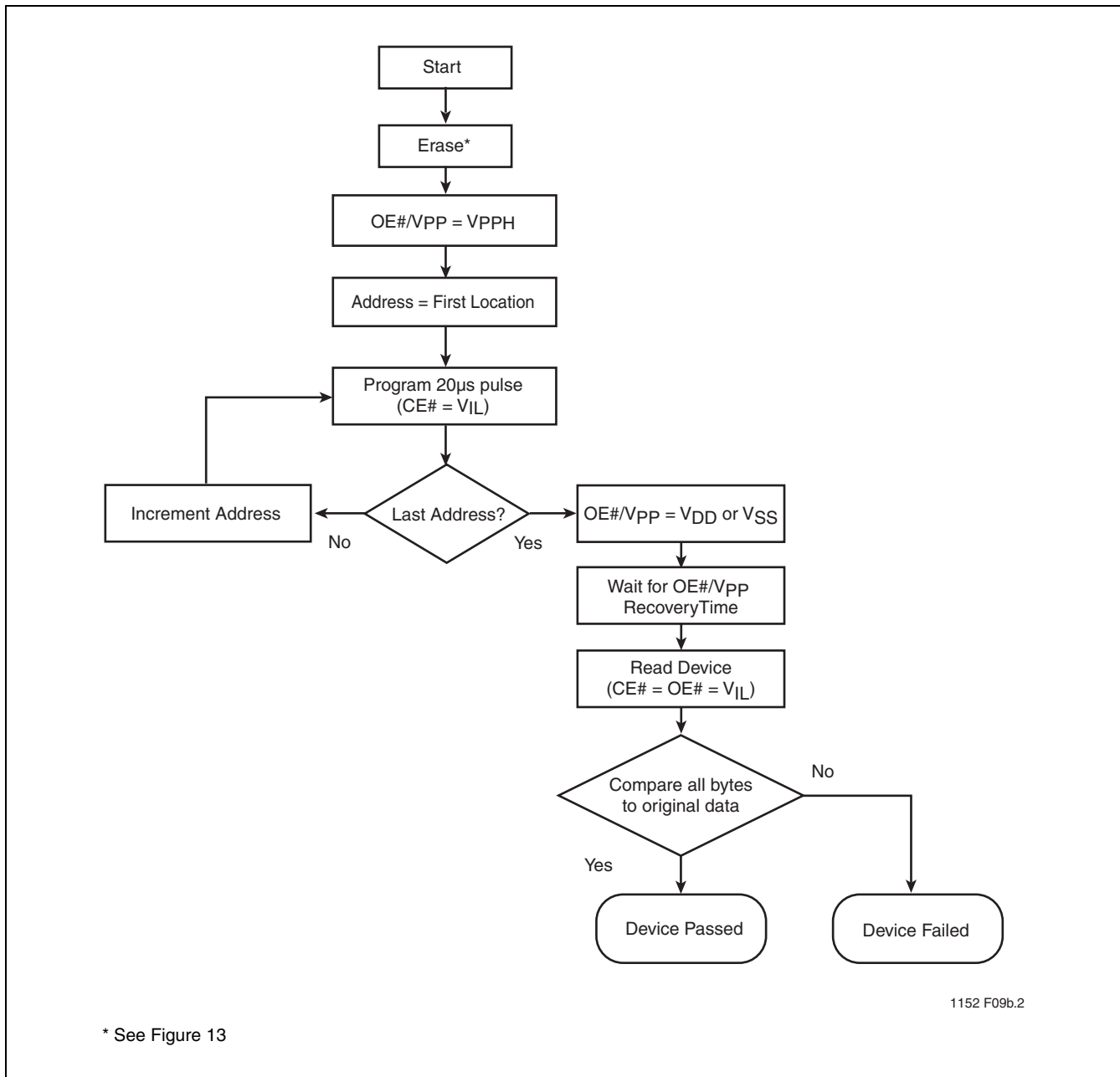
**FIGURE 15: Byte-Program Algorithm for SST27SF512**

Within the flowchart:

Start → Erase* → OE#/VPP = VPPH → Address = First Location → Program 20μs pulse (CE# = $V_{IL}$) → Last Address?

Last Address? — No → Increment Address (loops back to Program 20μs pulse)

Last Address? — Yes → OE#/VPP = $V_{DD}$ or $V_{SS}$ → Wait for OE#/VPP RecoveryTime → Read Device (CE# = OE# = $V_{IL}$) → Compare all bytes to original data

Compare all bytes to original data — Yes → Device Passed

Compare all bytes to original data — No → Device Failed

1152 F09b.2

* See Figure 13

```
                              ┌──────────┐
                              │  Start   │
                              └────┬─────┘
                          ┌────────┴────────┐
                          ┊     Erase*       ┊
                          └────────┬────────┘
                            ┌──────┴──────┐
                            │ VPP = VPPH  │
                            └──────┬──────┘
                        ┌──────────┴───────────┐
                        │ Address =  First Location │
                        └──────────┬───────────┘
                        ┌──────────┴───────────┐
                        │ CE# = VIL, OE# = VIH │
                        └──────────┬───────────┘
                        ┌──────────┴───────────┐
                        │  Program 20µs pulse  │
                        │     (PGM# = VIL)     │
                        └──────────┬───────────┘
                                   │
     ┌──────────────────┐     ╱────┴────╲
     │Increment Address │◄───╱ Last Address? ╲
     └──────────────────┘    ╲             ╱
              ▲            No  ╲─────┬────╱  Yes
              └───────────────┘      │
                                ┌────┴─────┐
                                │Read Device│
                                └────┬─────┘
                              ╱──────┴──────╲      No
                             ╱ Compare all bytes ╲──────┐
                             ╲ to original data  ╱      │
                              ╲────┬────────╱           │
                            Yes    │                    │
                            ┌──────┴──────┐     ┌────────┴──────┐
                            │Device Passed│     │ Device Failed │
                            └─────────────┘     └───────────────┘
```

1152 F09c.1

\* See Figure 14

**FIGURE 16: Byte-Program Algorithm for SST27SF010/020**

## PRODUCT ORDERING INFORMATION

```
SST   27   SF   020   -   70   -   3C   -   NH     E
XX    XX   XX   XXXX   -   XXX  -   XX   -   XXX    X
```

**Environmental Attribute**
E[1] = non-Pb

**Package Modifier**
H = 32 pins or leads

**Package Type**
N = PLCC
P = PDIP
W = TSOP (type 1, die up, 8mm x 14mm)

**Temperature Range**
C = Commercial = 0°C to +70°C

**Minimum Endurance**
3 = 1,000 cycles

**Read Access Speed**
70 = 70 ns

**Device Density - x8 Organization**
020 = 2 Mbit
010 = 1 Mbit
512 = 512 Kbit

**Voltage Range**
S = 4.5-5.5V

**Product Series**
27 = Many-Time Programmable Flash
OTP/EPROM replacement with
EPROM pinout

---
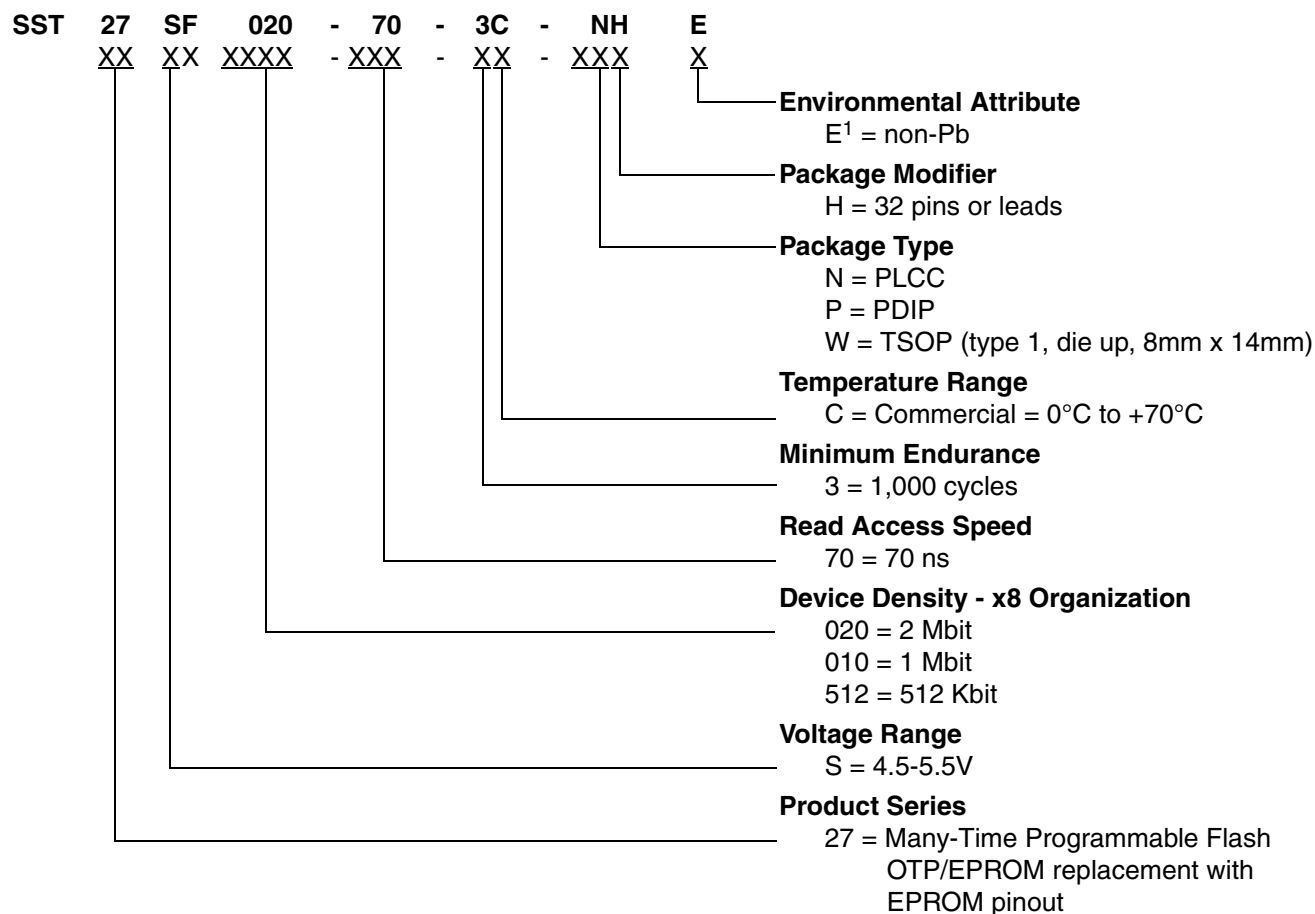
1. Environmental suffix "E" denotes non-Pb solder.
SST non-Pb solder devices are "RoHS Compliant".

**Valid combinations for SST27SF512**

SST27SF512-70-3C-NHE   SST27SF512-70-3C-WHE

**Valid combinations for SST27SF010**

SST27SF010-70-3C-NHE   SST27SF010-70-3C-WHE   SST27SF010-70-3C-PHE

**Valid combinations for SST27SF020**

SST27SF020-70-3C-NHE   SST27SF020-70-3C-WHE   SST27SF020-70-3C-PHE

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales
representative to confirm availability of valid combinations and to determine availability of new combinations.

## PACKAGING DIAGRAMS

TOP VIEW

SIDE VIEW

BOTTOM VIEW

Optional
Pin #1
Identifier

.495
.485
.453
.447

.048
.042

.020 R.
MAX.

.029
.023 x 30°

.112
.106

.040 R.
.030

2  1  32

.042
.048

.595
.585

.553
.547

.032
.026

.050
BSC

.021
.013

.400
BSC

.530
.490

.050
BSC

.015 Min.

.095
.075

.140
.125

.032
.026

Note:   1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
        2. All linear dimensions are in inches (max/min).
        3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
        4. Coplanarity: 4 mils.

32-plcc-NH-3
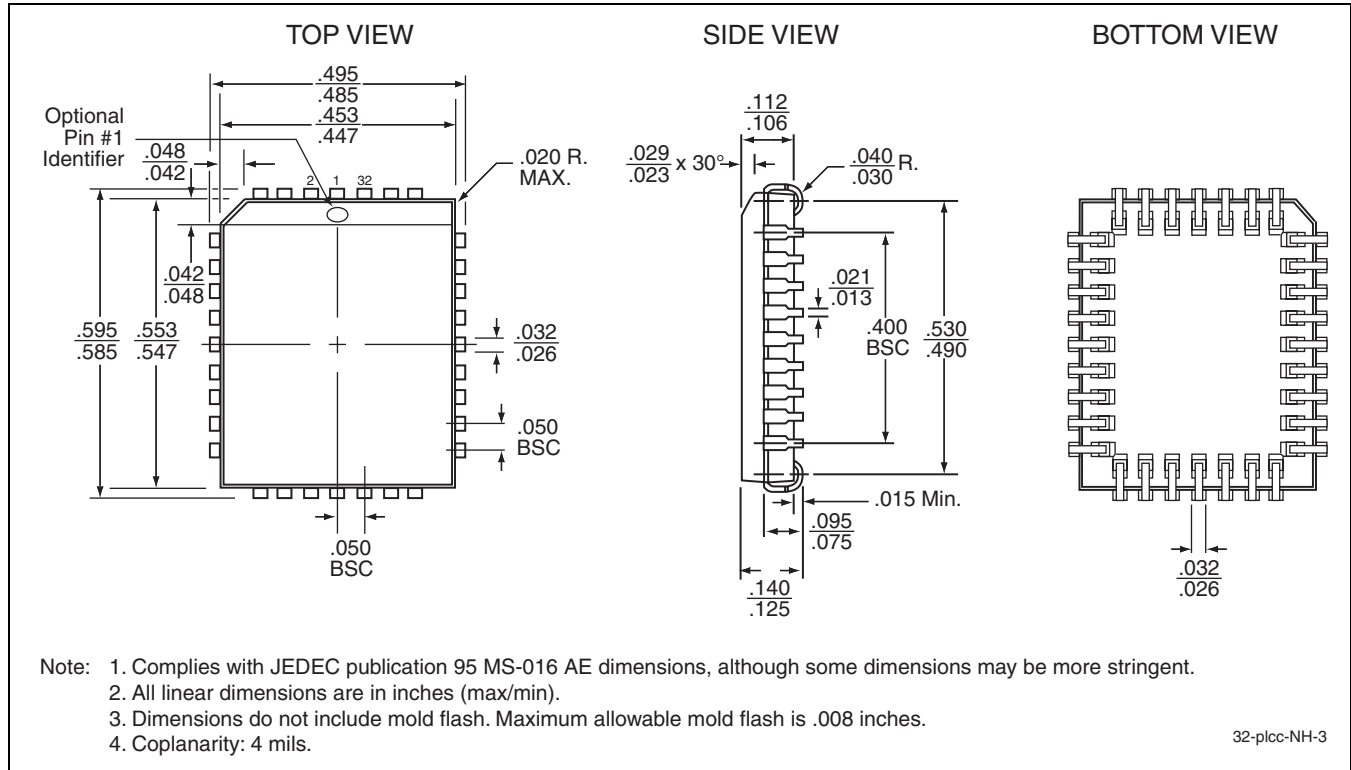
**FIGURE 17: 32-lead Plastic Lead Chip Carrier (PLCC)**
**SST Package Code: NH**

1.05
0.95

0.50
BSC

0.27
0.17

0.15
0.05

8.10
7.90

12.50
12.30

Pin # 1 Identifier

1.20
max.

0.70
0.50

14.20
13.80

DETAIL

0°- 5°

0.70
0.50

1mm

Note:    1. Complies with JEDEC publication 95 MO-142 BA dimensions,
             although some dimensions may be more stringent.
          2. All linear dimensions are in millimeters (max/min).
          3. Coplanarity: 0.1 mm
          4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

32-tsop-WH-7
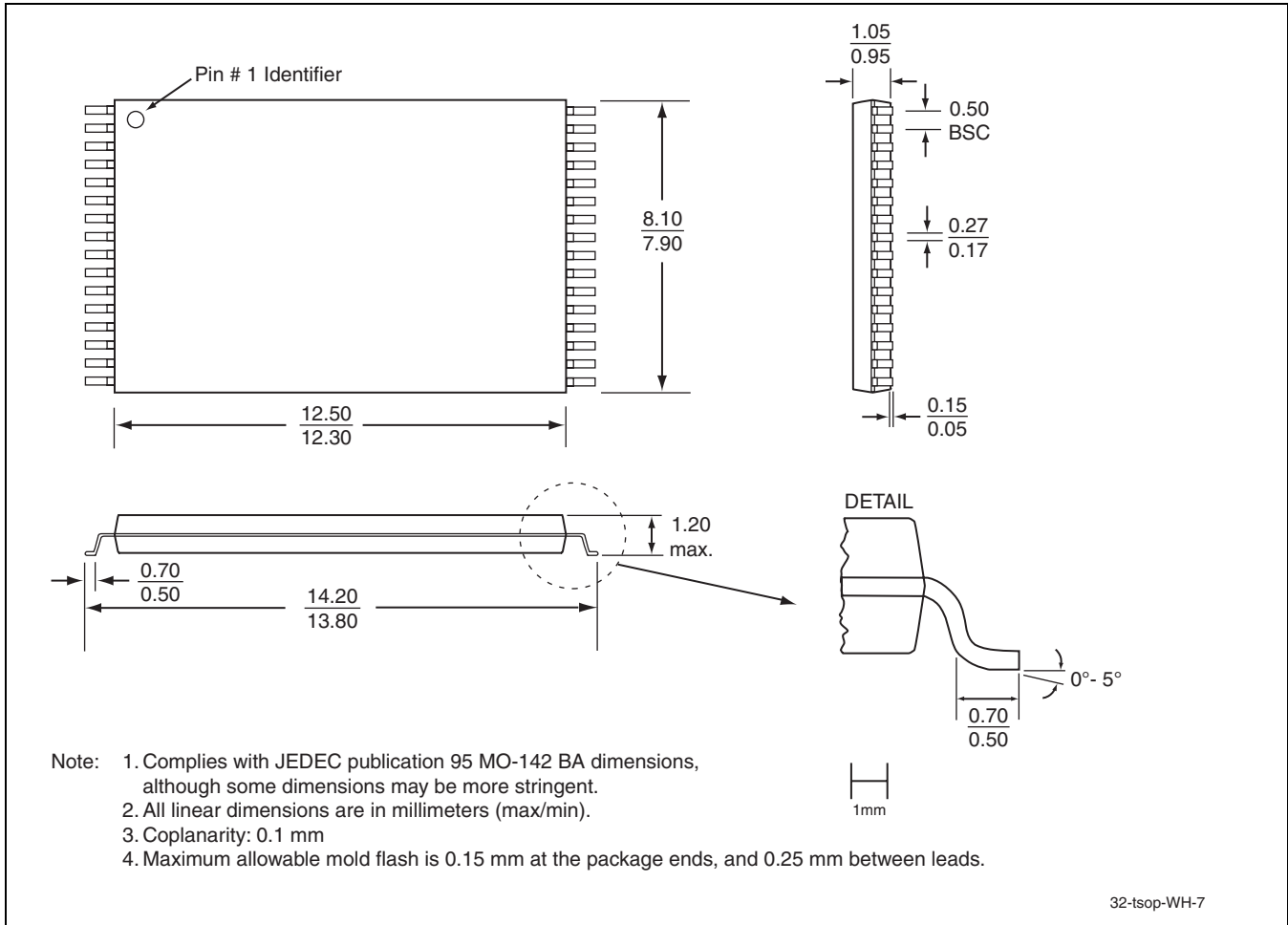
**FIGURE 18: 32-lead Thin Small Outline Package (TSOP) 8mm x 14mm**
            **SST Package Code: WH**

32

Pin #1 Identifier → 1

.075 / .065

1.655 / 1.645

Base Plane

Seating Plane

.050 / .015

.080 / .070

.065 / .045

.022 / .016

.100 BSC

.200 / .170

.150 / .120

.625 / .600

.550 / .530

7° 4 PLCS.

.012 / .008

.600 BSC

0° / 15°

Note:  1. Complies with JEDEC publication 95 MO-015 AP dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

32-pdip-PH-3
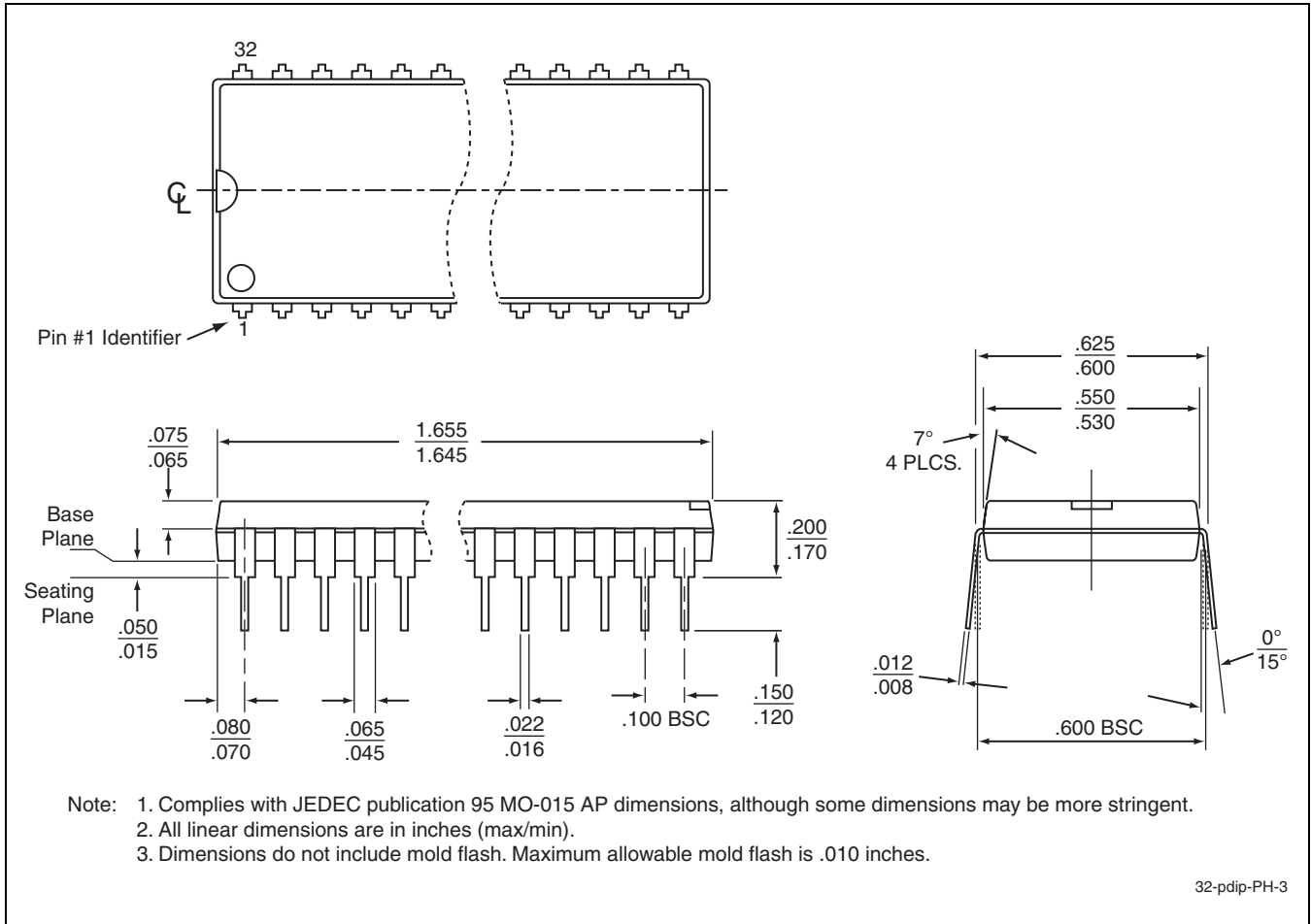
**FIGURE 19: 32-pin Plastic Dual In-line Pins (PDIP)**
**SST Package Code: PH**

**TABLE 14: Revision History**

| Number | Description | Date |
|:---:|:---|:---:|
| 02 | • 2002 Data Book | Feb 2002 |
| 03 | • Document Control Release (SST Internal): No technical changes | Apr 2002 |
| 04 | • Corrected $I_H$ Supervoltage Current for $A_9$ from 100 µA to 200 µA in Tables 5, 6, and 7 | Jul 2002 |
| 05 | • Corrected the Test Conditions for $I_{DD}$ and $I_{PPR}$ in Table 5 on page 7 | Sep 2003 |
| 06 | • Corrected the Max value for $I_{PP}$ from 1 mA to 3 mA (See Tables 6 and 7)<br>• Added MPNs for non-PB packages (See page 19) | Nov 2003 |
| 07 | • 2004 Data Book<br>• Corrected caption for Figure 7 from "Read Cycle" to "Chip-Erase" | Nov 2003 |
| 08 | • Removed 256 Kbit parts - refer to EOL Product Data Sheet S71152(02) | Apr 2004 |
| 09 | • Removed all 90 ns parts - refer to EOL Product Data Sheet S71152(03)<br>• Added RoHS compliance information on page 1 and in the "Product Ordering Information" on page 19<br>• Added the solder reflow temperature to the "Absolute Maximum Stress Ratings" on page 7. | Mar 2005 |
| 10 | • Removed obsolete Latch-up parameter from Table 10 on page 8 | May 2005 |
| 11 | • Corrected $V_{PP}$ voltage from 11.4-12.6V to 11.4-12V | Sep 2005 |
| 12 | • Removed leaded parts. See S71152(04)<br>• End-of-Life PG package and PG valid combination. See S71152(04) | Sep 2008 |

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