Q-TECH
CORPORATION

LEADLESS CHIP CARRIER
CRYSTAL CLOCK OSCILLATORS
1.8 to 15Vdc - 732.4Hz to 125MHz

Description

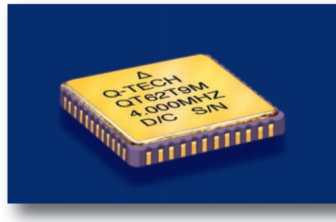
Q-Tech's Leadless Chip Carrier crystal oscillators consist of a source clock square wave generator, logic output buffers and/or logic divider stages, and a round AT high-precision quartz crystal built in a ceramic true SMD package.

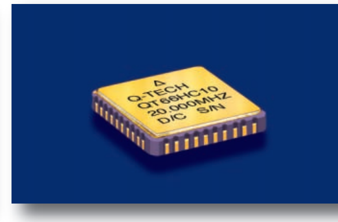
Features

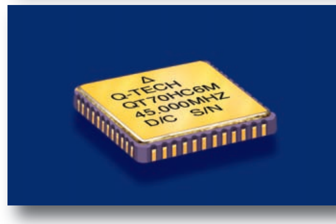
- Made in the USA
- ECCN: EAR99
- DFARS 252-225-7014 Compliant: Electronic Component Exemption
- USML Registration # M17677
- Wide frequency range from 732.4Hz to 125MHz
- Available as QPL MIL-PRF-55310/19 (QT66T), /20 (QT62T), and /29 (QT66HCD)
- Choice of packages and pin outs
- Choice of supply voltages
- Choice of output logic options (CMOS, ACMOS, HCMOS, LVHCMOS, TTL, ECL, PECL, and LVPECL)
- AT-Cut crystal
- True SMD hermetically sealed package
- Tight or custom symmetry available
- Low height available
- External tuning capacitor option
- Fundamental and third overtone designs
- Tristate function option D
- Four-point crystal mounts
- Custom design available tailors to meet customer's needs
- Q-Tech does not use pure lead or pure tin in its products
- RoHS compliant

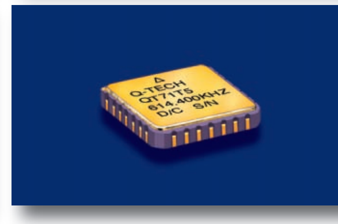
Applications

- Designed to meet today's requirements for all voltage applications
- Wide military clock applications
- Industrial controls
- Microcontroller driver









Ordering Information

QTXX — XX — D — XX — M — 60.000MHz

Model #

Output frequency

C	=	CMOS +5V to +15V *
AC	=	ACMOS +5V
HC	=	HCMOS +5V
T	=	TTL +5V
L	=	LVHCMOS + 3.3V
N	=	LVHCMOS + 2.5V
R	=	LVHCMOS + 1.8V
Z	=	Z output

Tristate Option D
(Left blank if no Tristate)

Screened to
MIL-PRF-55310,level B
(Left blank if no screening)

1	=	± 100ppm	at	0ºC	to	+70ºC
3**	=	± 5ppm	at	0ºC	to	+50ºC
4	=	± 50ppm	at	0ºC	to	+70ºC
5	=	± 25ppm	at	-20ºC	to	+70ºC
6	=	± 50ppm	at	-55ºC	to	+105ºC
9	=	± 50ppm	at	-55ºC	to	+125ºC
10	=	± 100ppm	at	-55ºC	to	+125ºC
11	=	± 50ppm	at	-40ºC	to	+85ºC
12	=	± 100ppm	at	-40ºC	to	+85ºC

(*) Please specify supply voltage when ordering CMOS
(**) Require an external capacitor

For frequency stability vs. temperature options not listed herein, please request a custom part number.

For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com

Package Information

- Package material (Header): 90% AL_2O_3 , (Metalization): Tungsten
- Lead finish: Gold Plated – 50µ ~ 80µ inches
  Nickel Underplate – 100µ ~ 250µ inches
- Cover: Kovar, Gold Plated – 60µ ~ 90µ inches
  Nickel Underplate – 50µ ~ 100µ inches
  With attached Preform – 80% Au, 20% Sn
- Package to lid attachment: Seam weld

Packaging Options

- Standard packaging in anti-static plastic tube
- Optional Tape and Reel

Other Options Available For An Additional Charge

- Solder Dip Sn/Pb 60/40%
- P. I. N. D. test
- J-leads attached

Specifications subject to change without prior notice.

Electrical Characteristics

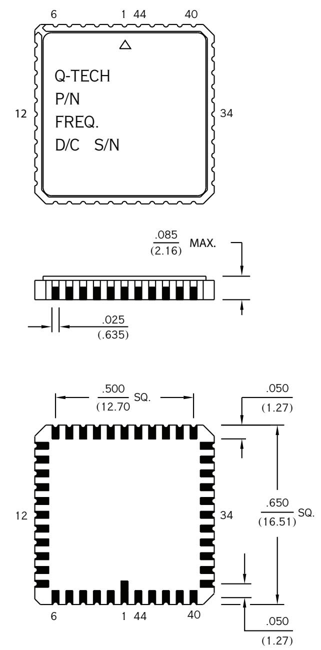
Parameters		C	AC	HC	T	L (*)
Output freq. range (Fo)	QT62, 70	**732.4Hz — 15MHz**	**732.4Hz — 85MHz**			**732.4Hz — 85MHz**
	QT66	**732.4Hz — 15MHz**	**732.4Hz — 85MHz**			**732.4Hz — 125MHz**
	QT71	**100kHz — 15MHz**	**100kHz — 85MHz**			**100kHz — 125MHz**
Supply voltage (Vdd)		5V ~ 15Vdc ± 10%	5.0Vdc ± 10%			3.3Vdc ± 10%
Freq. stability (ΔF/ΔT)		See Option codes				
Operating temp. (Topr)		See Option codes				
Storage temp. (Tsto)		-62ºC to + 125ºC				
Operating supply current (Idd) (No Load)		F and Vdd dependent 3 mA max. at 5V up to 5MHz 25 mA max. at 15V up to 15MHz	20 mA max. - 732.4Hz ~ < 16MHz 25 mA max. - 16MHz ~ < 40MHz 35 mA max. - 40MHz ~ < 60MHz 45 mA max. - 60MHz ~ 85MHz			3 mA max. - 732.4Hz ~ < 500kHz 6 mA max. - 500kHz ~ < 16MHz 10 mA max. - 16MHz ~ < 32MHz 20 mA max. - 32MHz ~ < 60MHz 30 mA max. - 60MHz ~ < 100MHz 40 mA max. - 100MHz ~ 125MHz
Symmetry (50% of ouput waveform or 1.4Vdc for TTL)		45/55% max. Fo < 4MHz 40/60% max. Fo ≥ 4MHz	45/55% max. Fo < 12MHz 40/60% max. Fo ≥ 12MHz			
Rise and Fall times (with typical load)		30ns max. (Measured from 10% to 90%)	15ns max. Fo < 15kHz 6ns max. Fo 15kHz ~ 39.999MHz 3ns max. Fo 40MHz ~ 160 MHz (Measured from 10% to 90% CMOS or from 0.8V to 2.0V TTL)			
Output Load		**15pF // 10kΩ**			**10TTL Fo < 20MHz** 6TTL Fo ≥ 20MHz	**15pF // 10kΩ**
Start-up time (Tstup)		10ms max.				
Output voltage (Voh/Vol)		0.9 x Vdd min.; 0.1 x Vdd max.			2.4V min.; 0.4V max.	0.9 x Vdd min.; 0.1 x Vdd max.
Output Current (Ioh/Iol)		± 1mA typ. at 5V ± 6.8mA typ. at 15V	± 24mA	±8 mA	-1.6mA / TTL +40µA / TTL	± 4mA .
Enable/Disable Tristate function Pin 1		Call for details	VIH ≥ 2.2V Oscillation; VIL ≤ 0.8V High Impedance			VIH ≥ 0.7 x Vdd Oscillation; VIL ≤ 0.3 x Vdd High Impedance
Jitter RMS 1σ (at 25ºC)		8ps typ. - < 40MHz 5ps typ. - ≥ 40MHz				15ps typ. - < 40MHz 8ps typ. - ≥ 40MHz
Aging (at 70ºC)		± 5ppm max. first year / ± 2ppm typ. per year thereafter				

(*) Available in 2.5Vdc (N) or 1.8Vdc (R)
Z Output logic can drive up to 200 pF load with typical 6ns rise & fall times (tr, tf)
ECL, PECL, LVPECL are available. Please contact Q-Tech for details.

Package Configuration Versus Pin Connections

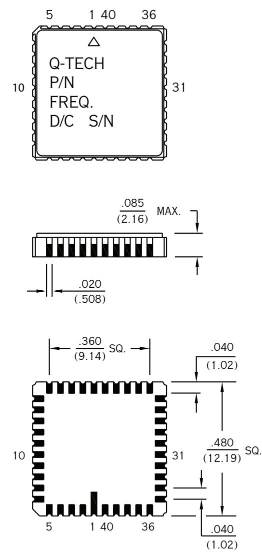
A

QT62



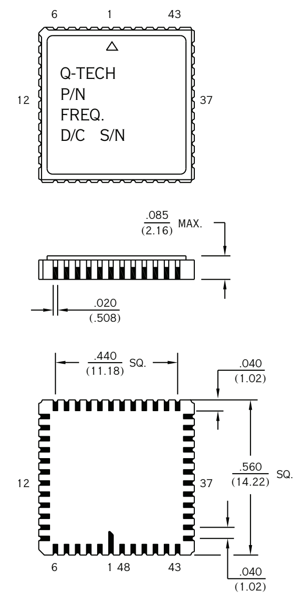
B

QT66



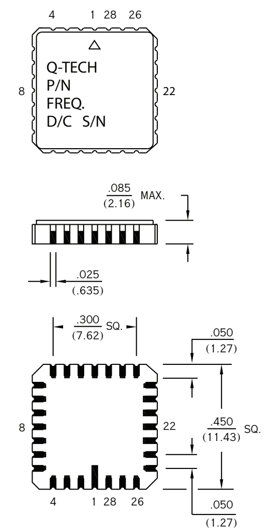
C

QT70



D

QT71

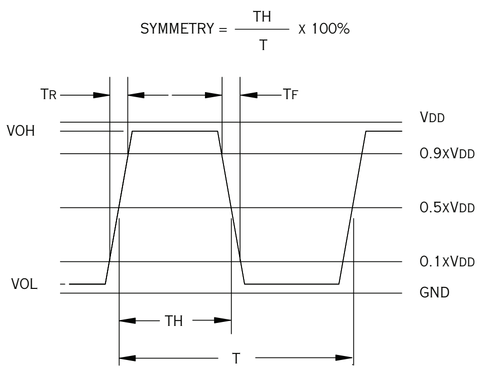


Dimensions are in inches (mm)

QT #	Conf	Vcc	GND	Case	Output	E/D	Equivalent MIL-PRF-55310 Configuration
QT62	A	6 & 12	34 & 40	34 & 40	42	41	/20 = QT62T
QT66	B	4 & 10	31 & 37	31 & 37	39	32	/19 = QT66T /29 = QT66HCD
QT70	C	5	44	44	47	N/A	N/A
QT71	D	4 & 8	22 & 26	22 & 26	28	27	N/A

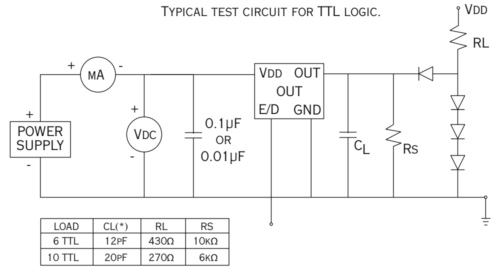
Please contact factory for pin connections on external capacitor (code 3).

Output Waveform (Typical)



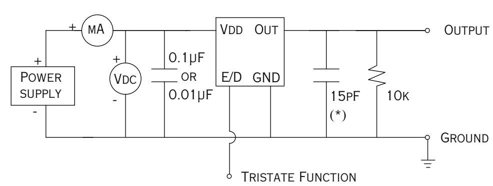
Test Circuit

Typical test circuit for TTL logic.



(*) CL includes the loading effect of the oscilloscope probe.

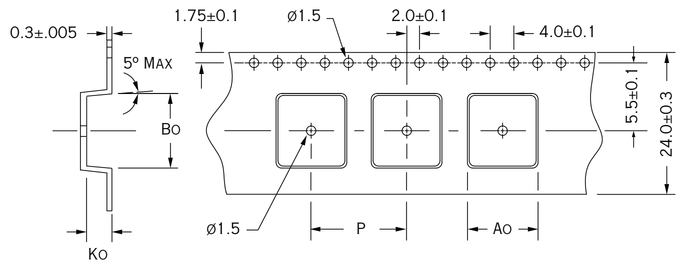
Typical test circuit for CMOS logic

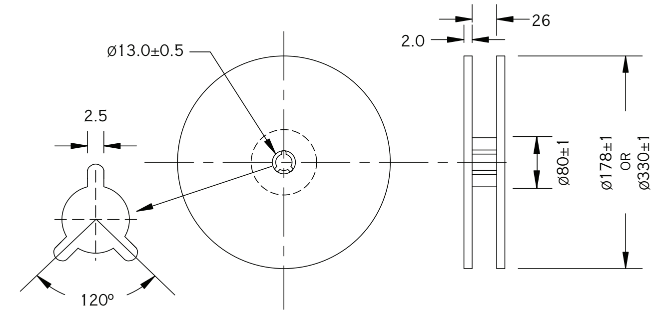


(*) CL includes probe and jig capacitance

The Tristate function on pin 1 has a built-in pull-up resistor typical 50kΩ, so it can be left floating or tied to Vdd without deteriorating the electrical performance.

Tape and Reel

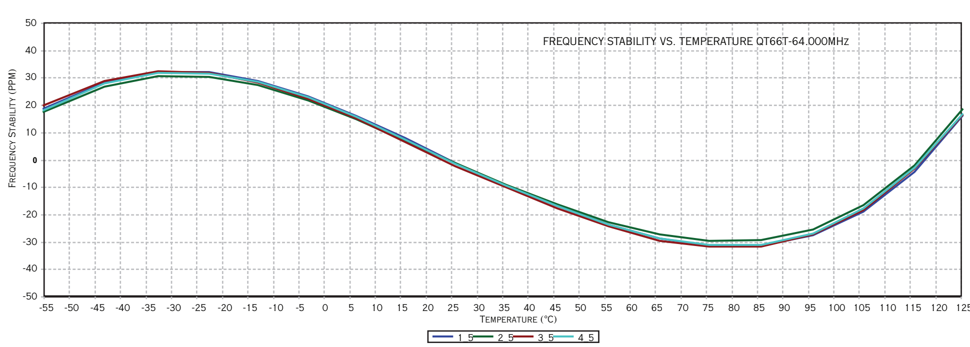




Dimensions are in mm. Tape is compliant to EIA-481-A.

QT#	P (mm)	Ao (mm)	Bo (mm)	Ko (mm)	Reel size (Diameter in mm)	Qty per reel (pcs)
QT62	20	17	17.30	2.70	178mm 330mm	100 600
QT66	16	12.57	12.57	2.54	178mm 330mm	280 1200
QT71	16	12.00	12.00	3.00	178mm 330mm	280 1200

Frequency vs. Temperature Curve



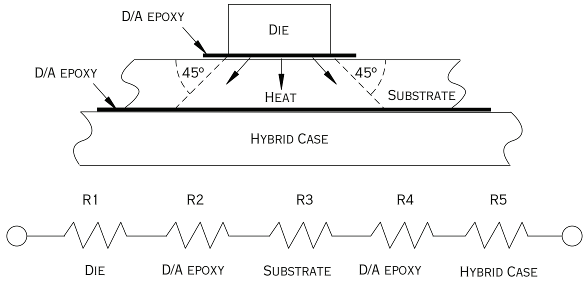
Thermal Characteristics

The heat transfer model in a hybrid package is described in figure 1.

Heat spreading occurs when heat flows into a material layer of increased cross-sectional area. It is adequate to assume that spreading occurs at a 45° angle.

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and hybrid case.

$$RT = R1 + R2 + R3 + R4 + R5$$



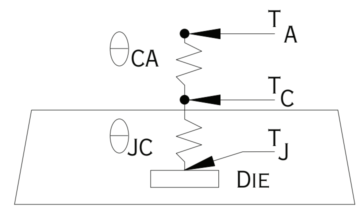
(Figure 1)

The total thermal resistance RT (see figure 2) between the heat source (die) to the hybrid case is the Theta Junction to Case (Theta JC) in°C/W.

- Theta junction to case (Theta JC) for this product is 30°C/W.
- Theta case to ambient (Theta CA) for this part is 100°C/W.
- Theta Junction to ambient (Theta JA) is 130°C/W.

Maximum power dissipation PD for this package at 25°C is:

- PD(max) = (TJ (max) – TA)/Theta JA
- With TJ = 175°C (Maximum junction temperature of die)
- PD(max) = (175 – 25)/130 = 1.15W



$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

(Figure 2)

Environmental Specifications

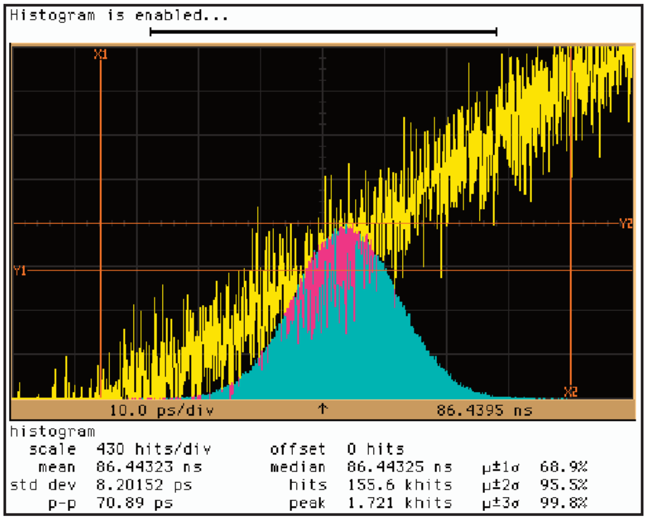
Q-Tech Standard Screening/QCI (MIL-PRF55310) is available for all of our Leadless Chip Carrier packages. Q-Tech can also customize screening and test procedures to meet your specific requirements. The Leadless Chip Carrier packages are designed and processed to exceed the following test conditions:

Environmental Test	Test Conditions
Temperature cycling	MIL-STD-883, Method 1010, Cond. B
Constant acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal Fine Leak	MIL-STD-883, Method 1014, Cond. A
Burn-in	160 hours, 125°C with load
Aging	30 days, 70°C, ± 1.5ppm max
Vibration sinusoidal	MIL-STD-202, Method 204, Cond. D
Shock, non operating	MIL-STD-202, Method 213, Cond. I
Thermal shock, non operating	MIL-STD-202, Method 107, Cond. B
Ambient pressure, non operating	MIL-STD-202, 105, Cond. C, 5 minutes dwell time minimum
Resistance to solder heat	MIL-STD-202, Method 210, Cond. B
Moisture resistance	MIL-STD-202, Method 106
Terminal strength	MIL-STD-202, Method 211, Cond. C
Resistance to solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208

Please contact Q-Tech for higher shock requirements

Period Jitter

As data rates increase, effects of jitter become critical with its budgets tighter. Jitter is the deviation of a timing event of a signal from its ideal position. Jitter is complex and is composed of both random and deterministic jitter components. Random jitter (RJ) is theoretically unbounded and Gaussian in distribution. Deterministic jitter (DJ) is bounded and does not follow any predictable distribution. DJ is also referred to as systematic jitter. A technique to measure period jitter (RMS) one standard deviation (1σ) and peak-to-peak jitter in time domain is to use a high sampling rate (>8G samples/s) digitizing oscilloscope. Figure shows an example of peak-to-peak jitter and RMS jitter (1σ) of a QT66T-24MHz, at 5.0Vdc.



RMS jitter (1σ): 8.20ps   Peak-to-peak jitter: 70.89ps

Phase Noise and Phase Jitter Integration

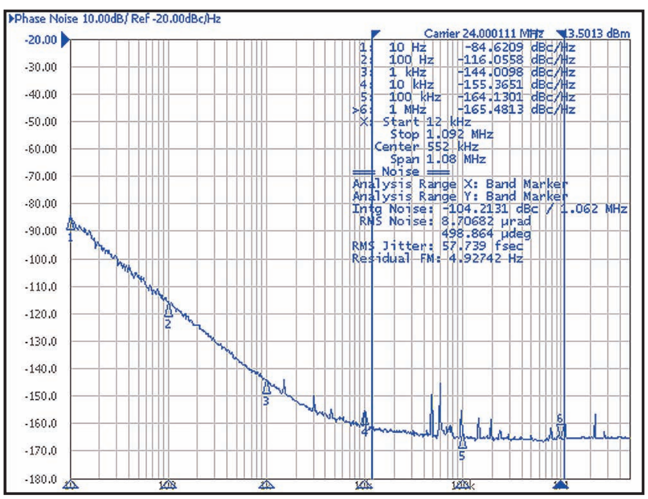
Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at an offset frequency from the carrier, e.g. 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, etc. Phase noise measurement is made with an Agilent E5052A Signal Source Analyzer (SSA) with built-in outstanding low-noise DC power supply source. The DC source is floated from the ground and isolated from external noise to ensure accuracy and repeatability.

In order to determine the total noise power over a certain frequency range (bandwidth), the time domain must be analyzed in the frequency domain, and then reconstructed in the time domain into an rms value with the unwanted frequencies excluded. This may be done by converting L(f) back to Sφ(f) over the bandwidth of interest, integrating and performing some calculations.

Symbol	Definition
$\int\mathcal{L}(f)$	Integrated single side band phase noise (dBc)
$S\varphi(f)=(180/\Pi)x\sqrt{2\int\mathcal{L}(f)df}$	Spectral density of phase modulation, also known as RMS phase error (in degrees)
RMS jitter = Sφ (f)/(fosc.360°)	Jitter(in seconds) due to phase noise. Note Sφ (f) in degrees.

The value of RMS jitter over the bandwidth of interest, e.g. 10kHz to 20MHz, 10Hz to 20MHz, represents 1 standard deviation of phase jitter contributed by the noise in that defined bandwidth.

Figure below shows a typical Phase Noise/Phase jitter of a QT66T10M, 5.0Vdc, 24MHz clock at offset frequencies 10Hz to 5MHz, and phase jitter integrated over the bandwidth of 12kHz to 1MHz.



QT66T10M, 5.0Vdc, 24MHz