M5M51288BKP,KJ,J-15,-20,-25,-20L,-25L
M5M51288BVP-20,-25,-20L,-25L

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51288BKP,KJ,J,VP are a family of 131072-word by 8-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high-speed application.

The M5M51288BKP,KJ,J,VP are offered in a 32-pin plastic dual-in-line package(DIP), 32-pin plastic small outline J-lead package(SOJ), 32-pin thin small outline package (TSOP).

These devices operate on a single 5V supply, and are directly TTL compatible. They include power down feature as well.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51288BKP,KJ,J - 15	15ns	190 mA	10mA
M5M51288BKP,KJ,J,VP - 20	20ns	170 mA	10mA
M5M51288BKP,KJ,J,VP - 20L			100 μA
M5M51288BKP,KJ,J,VP - 25	25ns	150 mA	10mA
M5M51288BKP,KJ,J,VP - 25L			100 μA

- Single +5V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by $\overline{S}_1$,S_2
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs

PACKAGE

M5M51288BKP ..... 32pin 300mil DIP
M5M51288BKJ ..... 32pin 300mil SOJ
M5M51288BJ ..... 32pin 400mil SOJ
M5M51288BVP ..... 32pin 8×20mm² TSOP(I)

APPLICATION

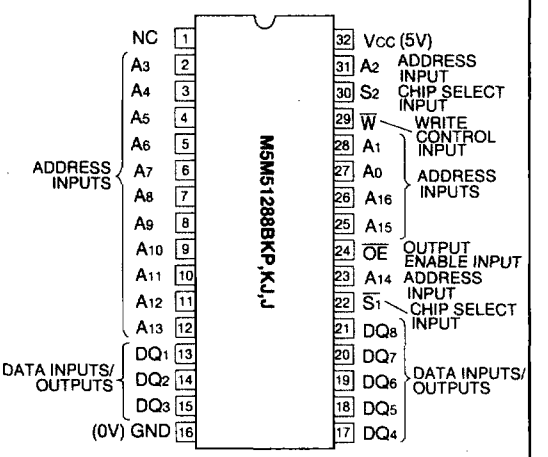
High speed memory units

FUNCTION

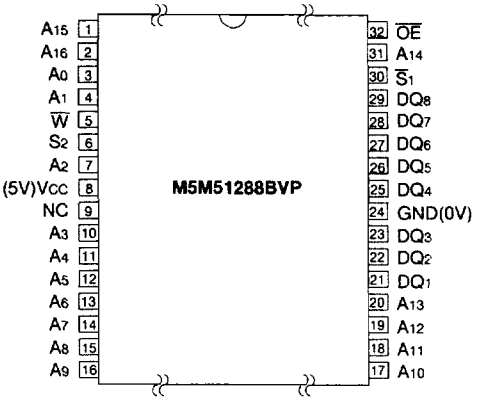
The operation mode of the M5M51288B series is determined by a combination of the device control inputs $\overline{S}_1$,S_2,$\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table shown in next page.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}_1$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}_1$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

PIN CONFIGURATION (TOP VIEW)



Outline 32P4Y(KP)
32P0J(KJ)
32P0K(J)



Outline 32P3H-E

NC : NO CONNECTION

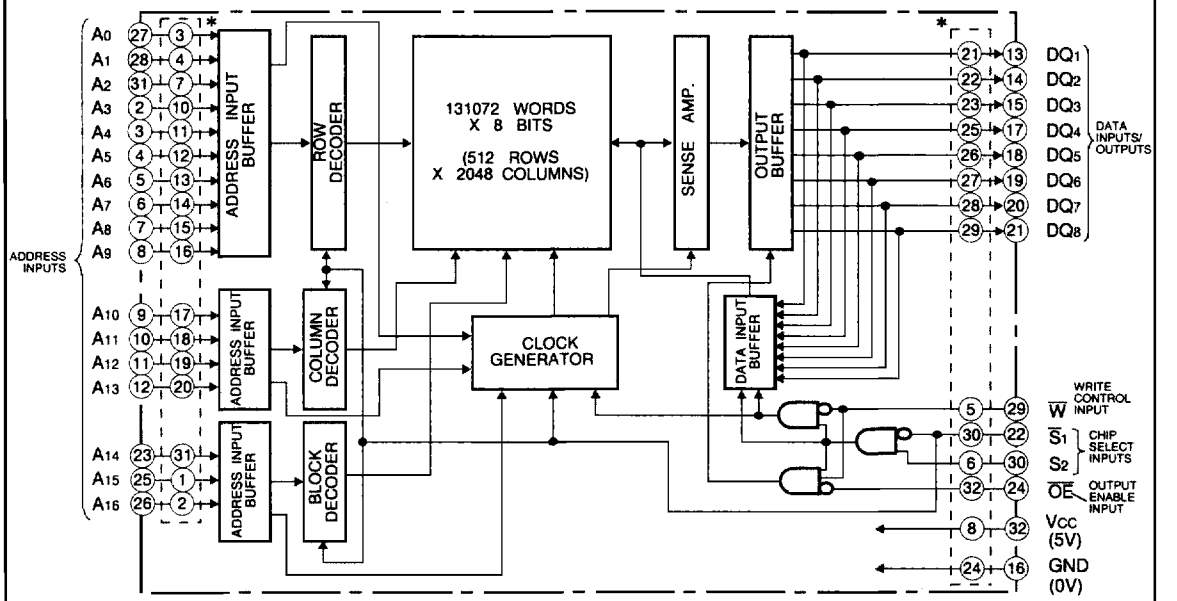
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}_1$ and S_2 are in an active state ($\overline{S}_1$=L,S_2=H)

When setting $\overline{S}_1$ at a high level or S_2 at a low level,the chip is in a non-selectable mode in which both reading and writing are disabled.In this mode,the output stage is in a high-impedance state,allowing OR -tie with other chips and memory expansion by $\overline{S}_1$ and S_2.

FUNCTION TABLE

$\overline{S}_1$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Active
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



* Pin numbers inside dotted line show those of TSOP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~Vcc+0.3	V
V_O	Output voltage		−3.5*~Vcc+0.3	V
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
$T_{stg(bias)}$	Storage temperature(bias)		−10~85	℃
T_{stg}	Storage temperature		−65~150	℃

*Pulse width≦20ns, in case of DC: −0.5V

DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage			−0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL}=8mA				0.4	V
I_I	Input current	V_I=0~Vcc				2	μA
| I_{OZ} |	Output current in off-state	$V_I(\overline{S1})=V_{IH}$, $V_{I/O}$=0~Vcc				10	μA
I_{CC1}	Active supply current (TTL level)	$V_I(\overline{S1})=V_{IL}$, other inputs=$V_{IH}$ or V_{IL}, Output-open(duty 100%)	AC (15ns cycle)			190	mA
			AC (20ns cycle)			170	
			AC (25ns cycle)			150	
			DC		70	85	
I_{CC2}	Stand-by supply current (TTL level)	$V_I(\overline{S1})=V_{IH}$	AC (15ns cycle)			60	mA
			AC (20/25ns cycle)			50	
			DC			35	
I_{CC3}	Stand-by current (MOS level)	$V_I(\overline{S1})\geqq$Vcc−0.2V, other inputs $V_I\leqq$0.2V or $V_I\geqq$Vcc−0.2V	-15,-20,-25		1	10	mA
			-20L,-25L		10	100	μA

*Pulse width≦20ns, in case of AC: −3.0V

CAPACITANCE (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			6	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc=5V, Ta=25℃
3: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3.0V, V_{IL} = 0V

Input rise and fall time ····· 3ns

Input timing reference levels ····· V_{IH} = 1.5V, V_{IL} = 1.5V

Output timing reference levels ····· V_{OH} = 1.5V, V_{OL} =1.5V

Output loads ····· Fig1, Fig2

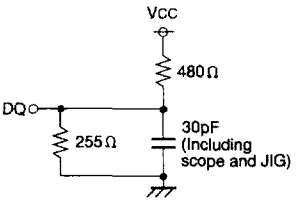


Fig.1 Output load

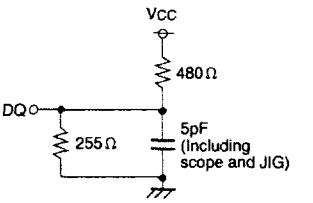


Fig.2 Output load for ten, tdis

(2) READ CYCLE

Symbol	Parameter	Limits						Unit
		M5M51288BKP,KJ,J -15		M5M51288BKP,KJ,J, VP-20, -20L		M5M51288BKP,KJ,J, VP-25, -25L		
		Min	Max	Min	Max	Min	Max	
tCR	Read cycle time	15		20		25		ns
ta(A)	Address access time		15		20		25	ns
ta(S1)	Chip select 1 access time		15		20		25	ns
ta(S2)	Chip select 2 access time		14		17		20	ns
ta(OE)	Output enable access time		8		10		13	ns
tdis(S1)	Output disable time after $\overline{S_1}$ high	0	7	0	7	0	8	ns
tdis(S2)	Output disable time after S_2 low	0	7	0	7	0	8	ns
tdis(OE)	Output disable time after $\overline{OE}$ high	0	7	0	7	0	8	ns
ten(S1)	Output enable time after $\overline{S_1}$ low	6		6		6		ns
ten(S2)	Output enable time after S_2 high	6		6		6		ns
ten(OE)	Output enable time after $\overline{OE}$ low	0		0		0		ns
tv(A)	Data valid time after address change	7		7		7		ns
tPU	Power-up time after chip selection	0		0		0		ns
tPD	Power-down time after chip selection		15		20		25	ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M51288BKP,KJ,J -15		M5M51288BKP,KJ,J, VP-20, -20L		M5M51288BKP,KJ,J, VP-25, -25L		
		Min	Max	Min	Max	Min	Max	
tCW	Write cycle time	15		20		25		ns
tw(W)	Write pulse width	12		15		20		ns
tsu(A)1	Address setup time ($\overline{W}$)	0		0		0		ns
tsu(A)2	Address setup time ($\overline{S_1}$, S_2)	0		0		0		ns
tsu(S1)	Chip select 1 setup time	12		15		20		ns
tsu(S2)	Chip select 2 setup time	12		15		20		ns
tsu(D)	Data setup time	8		12		15		ns
th(D)	Data hold time	0		0		0		ns
trec(W)	Write recovery time	0		0		0		ns
tdis(W)	Output disable time after $\overline{W}$ low	0	7	0	7	0	8	ns
tdis(OE)	Output disable time after $\overline{OE}$ high	0	7	0	7	0	8	ns
ten(W)	Output enable time after $\overline{W}$ high	0		0		0		ns
ten(OE)	Output enable time after $\overline{OE}$ low	0		0		0		ns
tsu(A-$\overline{W}$H)	Address to $\overline{W}$ high	12		15		20		ns

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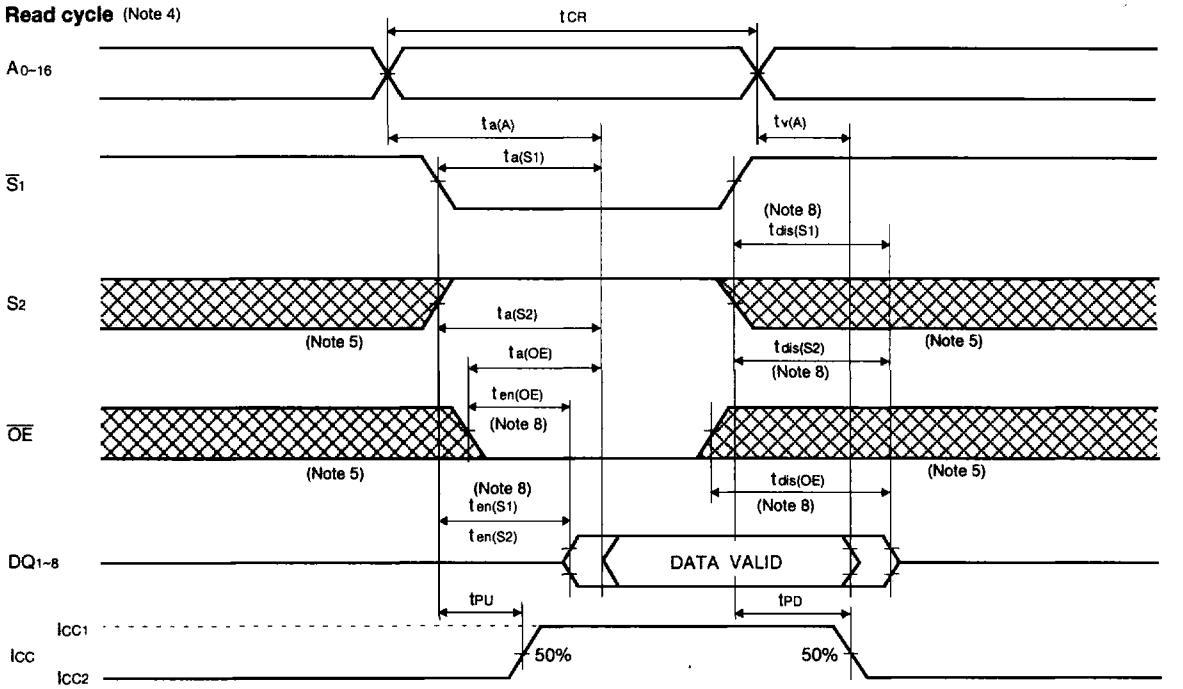
(4) TIMING DIAGRAMS

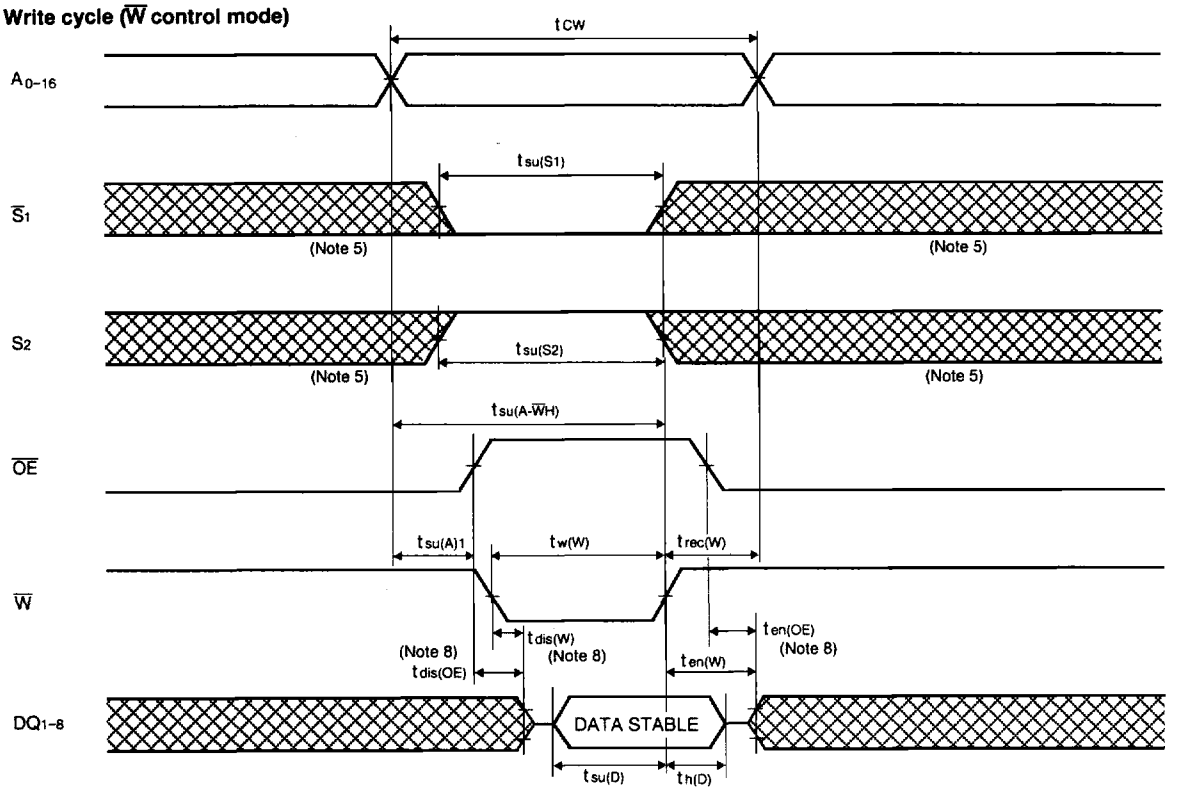
Read cycle (Note 4)



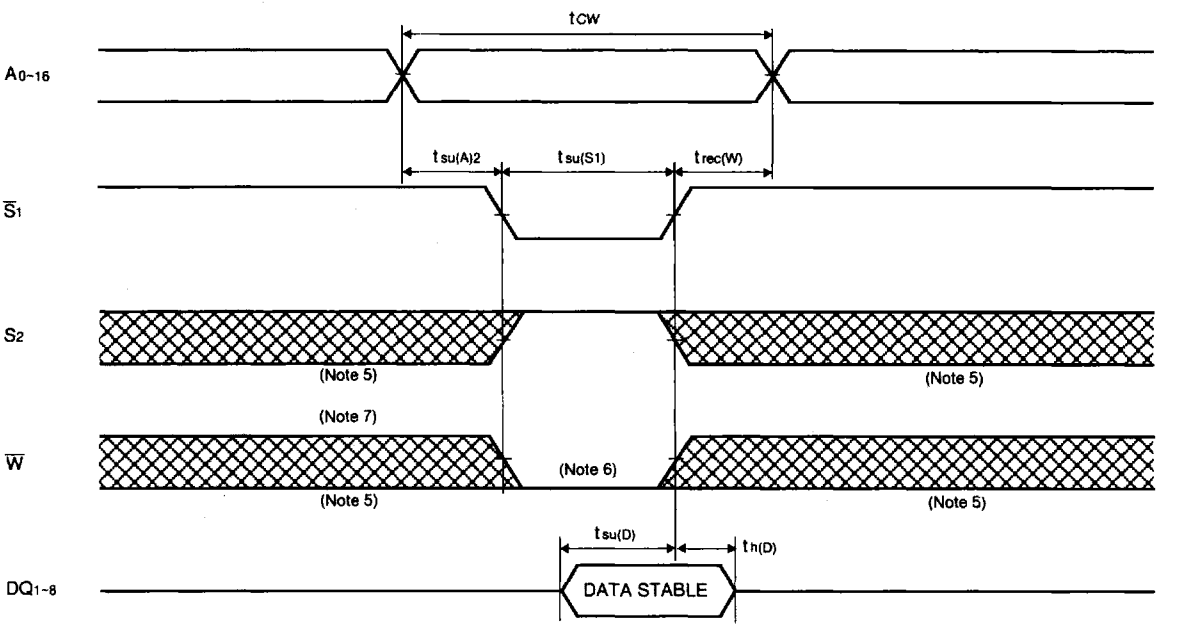
W=H

Note 4: Addresses and S1,S2 valid prior to OE transition low by (ta(A) - ta(OE)), (ta(S1) - ta(OE)), ta(S2) - ta(OE)).

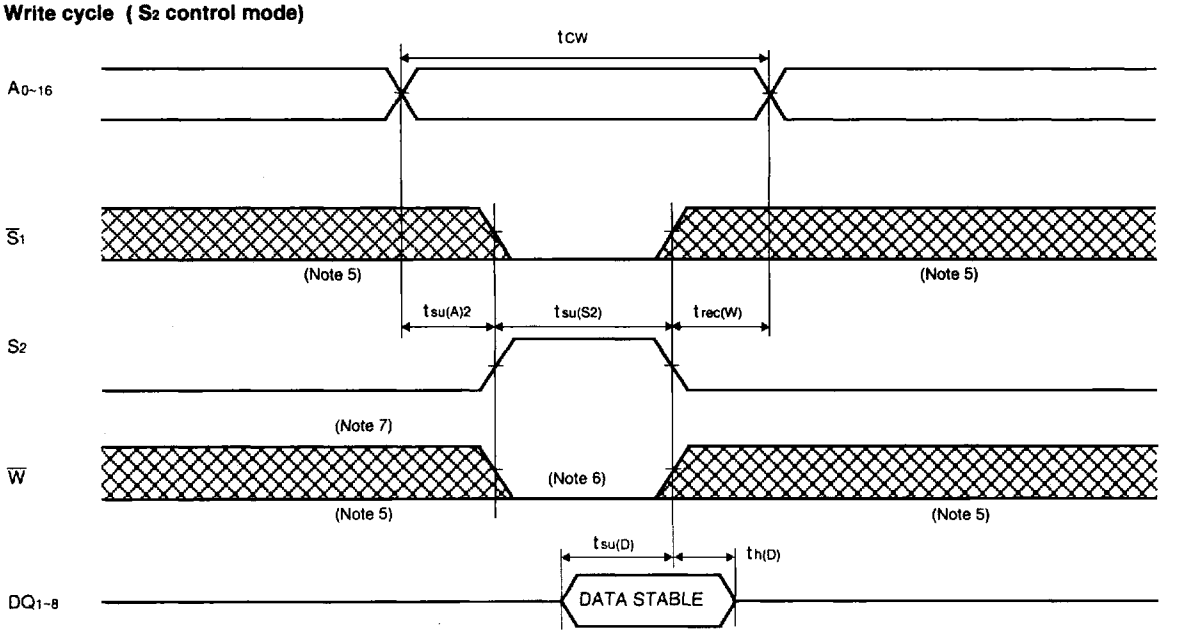
Write cycle (W control mode)



Write cycle ($\overline{S}_1$ control mode)



Write cycle (S_2 control mode)



Note 5: Hatching indicates the state is "don't care".
6: Writing is executed while S2 high overlaps $\overline{S}_1$ and $\overline{W}$ low.
7: When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S}_1$ or rising edge of S2, the outputs are maintained in the high impedance state.
8: Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.
9: ten, tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage	V_I ($\overline{S_1}$) ≧ Vcc − 0.2V V_I ≧ Vcc − 0.2V or 0V ≦ V_I ≦ 0.2V		2			V
V_I ($\overline{S_1}$)	Chip select input voltage			Vcc − 0.2			V
$t_{su\ (PD)}$	Power down setup time			0			ns
$t_{rec\ (PD)}$	Power down recovery time		-20L	20			ns
			-25L	25			
$I_{CC\ (PD)}$	Power down supply current	Vcc = 3.0V				50	μA
		Vcc = 5.5V				100	

Note 10 : This is only M5M51288BKP, KJ, J,VP-20L, -25L

TIMING WAVEFORM FOR POWER DOWN