LTM9005

IF Sampling Receiver Subsystem

FEATURES

- **Fully Integrated "RF-to-Bits" IF-Sampling Receiver Subsystem**
- **Wide RF Frequency Range: 400MHz to 3.8GHz**
- **140MHz Center Frequency Internal SAW Filter**
- **Low Power ADC with Up to 14-Bit Resolution, 125Msps Sample Rate**
- **16dB Cascaded NF, 17.7dBm Two-Tone IIP3**
- 1.2W Total Power Consumption
- 50Ω Single-Ended RF and LO Ports
- Continuous 20dB Attenuation Range
- Internal Bypass Capacitance, No External Components Required
- ADC Clock Duty Cycle Stabilizer
- Digital Output Supply Range: 0.5V to 3.6V
- 15mm × 22mm LGA package

APPLICATIONS

- Base Station Receivers
- Remote Radio Heads
- Communications Test Equipment

DESCRIPTION

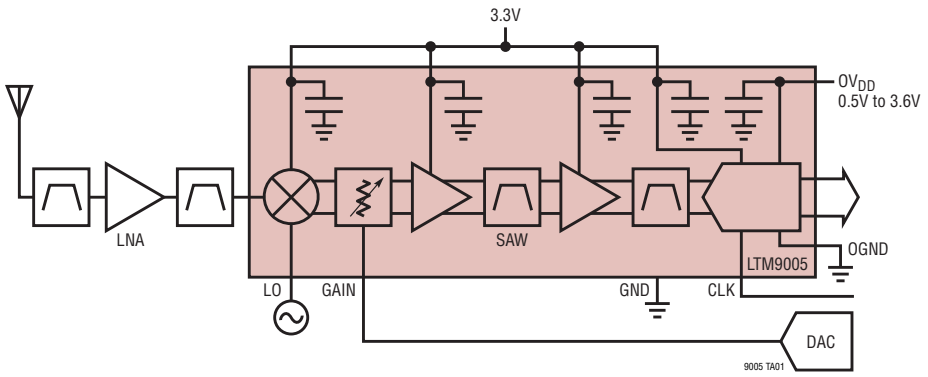
The LTM®9005 is an IF Sampling Receiver Subsystem for wireless base stations and communications test equipment. Utilizing an integrated System in a Package (SiP) technology, it includes a downconverting mixer, 140MHz SAW filter, two gain stages, a variable attenuator and analog-to-digital converter (ADC). The system is tuned for an Intermediate Frequency (IF) of 140MHz and a signal bandwidth of up to 60MHz; contact Linear Technology regarding customization. The high integration and small package allow for a very compact receiver.

The high signal level downconverting mixer is optimized for high linearity, wide dynamic range IF sampling applications. It includes a high speed differential LO buffer amplifier driving a double-balanced mixer. Broadband, integrated transformers on the RF and LO inputs provide single ended 50Ω interfaces. The RF and LO inputs are internally matched to 50Ω from 1.6GHz to 2.3GHz.

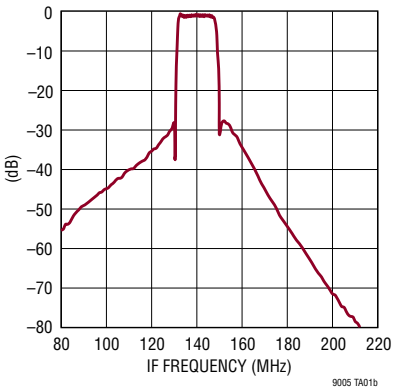
Versions are available with ADCs up to 14-bit resolution and 125Msps. A separate output supply allows the parallel output bus to drive 0.5V to 3.6V logic. A single-ended CLK input controls converter operation. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

TYPICAL APPLICATION

Simplified IF-Sampling Receiver



IF Frequency Response, 64k Point FFT, RF = 1.95GHz, LO = 1.81GHz



ABSOLUTE MAXIMUM RATINGS

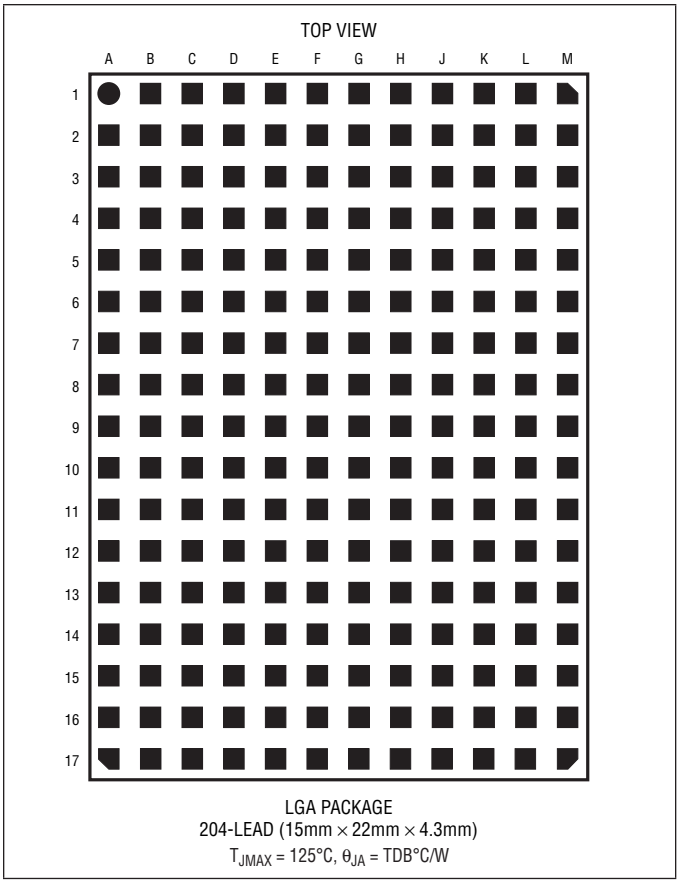
(Notes 1, 2)

Supply Voltage (V_{CC2}, V_{CC3}) ..... –0.3V to 3.6V
Supply Voltage (V_{CC1}, V_{DD}, OV_{DD})..... –0.3V to 4.0V
Digital Output Ground Voltage (OGND) ..... –0.3V to 1V
LO Input Power (380MHz to 4.2GHz).....10dBm
LO Input DC Voltage..... –1V to V_{CC1} + 1V
RF Input Power (400MHz to 3.8GHz) 12dBm
RF Input DC Voltage..... ±0.1V
EN Voltage .....–0.3V to V_{CC1} + 0.3V
AMP1SHDN Voltage.....–0.3V to V_{CC2} + 0.3V
AMP2SHDN Voltage.....–0.3V to V_{CC3} + 0.3V
GAIN Voltage.....–0.3V to V_{CC1} + 0.3V
GAIN Current.....20mA
Digital Input Voltage..... –0.3V to (V_{DD} + 0.3V)
Digital Output Voltage.....–0.3V to (OV_{DD} + 0.3V)
Operating Ambient Temperature Range
LTM9005C ..... 0°C to 70°C
LTM9005I .....–40°C to 85°C
Storage Temperature Range .....–45°C to 125°C
Maximum Junction Temperature ..... 125°C

CAUTION: Pins A8, A9, B8, B9, L8, L9, M8 and M9 and the RF and LO inputs are sensitive to electro-static discharge (ESD). It is very important that proper ESD precautions be observed when handling the LTM9005. Avoid ultrasonic exposure, the LTM9005 contains a hermetic cavity filter.

PIN CONFIGURATION

(See Pin Functions, Pin Configuration Table)



LGA PACKAGE
204-LEAD (15mm × 22mm × 4.3mm)
T_{JMAX} = 125°C, θ_{JA} = TDB°C/W

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM9005CV-AA#PBF	LTM9005V AA	204-Lead (15mm × 22mm × 4.3mm) LGA	0°C to 70°C
LTM9005IV-AA#PBF	LTM9005V AA	204-Lead (15mm × 22mm × 4.3mm) LGA	–40°C to 85°C
LTM9005CV-AB#PBF	LTM9005V AB	204-Lead (15mm × 22mm × 4.3mm) LGA	0°C to 70°C
LTM9005IV-AB#PBF	LTM9005V AB	204-Lead (15mm × 22mm × 4.3mm) LGA	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3). All specifications apply at maximum gain setting.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	RF Input Frequency Range	No External Matching (Midband) With External Matching (Low Band or High Band)		 400	1600 to 2300	 3800	MHz MHz
	LO Input Frequency Range	No External Matching With External Matching		 380	1000 to 4200	 5000	MHz MHz
	RF Input Return Loss	Z_O = 50Ω, 1600MHz to 2300MHz (No External Matching)			>12		dB
	LO Input Return Loss	Z_O = 50Ω, 1000MHz to 5000MHz (No External Matching)			>10		dB
	RF Input Power for –1dBFS	LTM9005-AA RF = 900MHz, LO = 760MHz RF = 1950MHz, LO = 1810MHz LTM9005-AB RF = 900MHz, LO = 760MHz RF = 1950MHz, LO = 1810MHz		 TBD TBD TBD TBD	 TBD –18.8 TBD –17.8	 TBD TBD TBD TBD	 dBm dBm dBm dBm
	LO Input Power	1200MHz to 4200MHz 380MHz to 1200MHz		–8 –5	–3 0	2 5	dBm dBm
	LO to RF Leakage	f_{LO} = 380MHz to 1600MHz f_{LO} = 1600MHz to 4000MHz			<–50 <–45		dBm dBm
	RF to LO Isolation	f_{RF} = 400MHz to 1700MHz f_{RF} = 1700MHz to 3800MHz			>50 >42		dB dB
	2Rf-2LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/2$)	900MHz: f_{RF} = 830MHz at TBD 1950MHz: f_{RF} = 1880MHz at –19dBm			TBD –71		dBc dBc
	3Rf-3LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/3$)	900MHz: f_{RF} = 807MHz at TBD 1950MHz: f_{RF} = 1857MHz at –19dBm			TBD –96		dBc dBc

FILTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Center Frequency	LTM9005-AA LTM9005-AB			140 140		MHz MHz
	Lower 1dB Bandedge	LTM9005-AA LTM9005-AB			132 130.8		MHz MHz
	Upper 1dB Bandedge	LTM9005-AA LTM9005-AB			148 149.2		MHz MHz
	Lower 3dB Bandedge	LTM9005-AA LTM9005-AB			131.5 130		MHz MHz
	Upper 3dB Bandedge	LTM9005-AA LTM9005-AB			148.5 150		MHz MHz
	Lower 35dB Stopband	LTM9005-AA LTM9005-AB			129 126.8		MHz MHz
	Upper 35dB Stopband	LTM9005-AA LTM9005-AB			151 153.2		MHz MHz
	Passband Flatness	133.6MHz – 146.4MHz, LTM9005-AA 130.8MHz – 149.2MHz, LTM9005-AB			0.6 0.8		dB dB
	Phase Linearity	133.6MHz – 146.4MHz, LTM9005-AA 130.8MHz – 149.2MHz, LTM9005-AB			10 TBD		deg deg
	Group Delay	133.6MHz – 146.4MHz, LTM9005-AA 130.8MHz – 149.2MHz, LTM9005-AB			60 115		ns ns
	Absolute Delay	LTM9005-AA LTM9005-AB			1 1		µs µs

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution (No Missing Codes)	LTM9005-Ax	●	14			Bits
	Integral Linearity Error (Note 4)	IF = 140MHz, LTM9005-Ax			±TBD		LSB
	Differential Linearity Error	IF = 140MHz, LTM9005-Ax			±TBD		LSB

GAIN CONTROL

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC1} = 3.3V, RF Input = –1dBFS.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Gain Adjustment Range				20		dB
	Forward Current Range		●	0		10	mA
	Response Time	10% to 90% Gain Current Step			TBD		µs
	Input Impedance	XX MHz, 0.1 < I_{GAIN} < 10mA			50		Ω
	Isolation to Output	RF Input = TBD dBm (Note 5)			TBD		dB
	Control Voltage	Maximum Gain Gain –20dB			3.3 2.55		V V

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3). All specifications apply at maximum gain setting.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio at –1dBFS, within the RF Passband	LTM9005-AA RF = 1950MHz, LO = 1810MHz LTM9005-AB RF = 1950MHz, LO = 1810MHz		TBD TBD	67.2 67	TBD TBD	dB dB
SFDR	Spurious Free Dynamic Range at –1dBFS 2nd or 3rd Harmonic	LTM9005-AA RF = 1950MHz, LO = 1810MHz LTM9005-AB RF = 1950MHz, LO = 1810MHz		TBD TBD	75 75	TBD TBD	dB dB
SFDR	Spurious Free Dynamic Range at –1dBFS 4th or Higher	LTM9005-AA RF = 1950MHz, LO = 1810MHz LTM9005-AB RF = 1950MHz, LO = 1810MHz		TBD TBD	93.5 93.5	TBD TBD	dB dB
S/(N+D)	Signal-to-Noise Plus Distortion Ratio at –1dBFS	LTM9005-AA RF = 1950MHz, LO = 1810MHz LTM9005-AB RF = 1950MHz, LO = 1810MHz		TBD TBD	60.5 62	TBD TBD	dB dB
IMD3	Intermodulation Distortion at –7dBFS per Tone	LTM9005-AA RF = 1950MHz, LO = 1810MHz LTM9005-AB RF = 1950MHz, LO = 1810MHz		TBD TBD	72.5 72.5	TBD TBD	dB dB

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Inputs (CLK, $\overline{OE}$, ADCSHDN)							
V_{IH}	High Level Input Voltage	V_{DD} = 3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 3V	●			0.8	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 6)			3		pF
Amplifier Shutdown (AMP1SHDN, AMP2SHDN)							
V_{IH}	High Level Input Voltage	V_{CC2} = V_{CC3} = 3V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{CC2} = V_{CC3} = 3V	●			0.8	V
I_{IH}	Input High Current	V_{CC2} = V_{CC3} = 3V, V_{IN} = 2V			1.3		µA
I_{IL}	Input Low Current	V_{CC2} = V_{CC3} = 3V, V_{IN} = 0.8V			0.1		µA
Mixer Enable (EN)							
V_{IH}	High Level Input Voltage	V_{CC1} = 3.3V	●	2.7			V
V_{IL}	Low Level Input Voltage	V_{CC1} = 3.3V	●			0.3	V
I_{IN}	Input Current	V_{IN} = 0V to V_{CC1}	●		53	90	µA
	Turn-ON Time				2.8		µs
	Turn-OFF Time				2.9		µs
Analog Inputs (Mode, SENSE)							
I_{MODE}	MODE Input Leakage		●	–3		3	µA
I_{SENSE}	SENSE Input Leakage	0V < SENSE < 1V	●	–3		3	µA
Logic Outputs							
OV_{DD} = 3V							
C_{OZ}	Hi-Z Output Capacitance	$\overline{OE}$ = 3V (Note 6)			3		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			50		mA
I_{SINK}	Output Sink Current	V_{OUT} = 3V			50		mA
V_{OH}	High Level Output Voltage	I_O = –10µA I_O = –200µA	 ●	 2.7	2.995 2.99		V V
V_{OL}	Low Level Output Voltage	I_O = 10µA I_O = 1.6mA	 ●		0.005 0.09	 0.4	V V
OV_{DD} = 2.5V							
V_{OH}	High Level Output Voltage	I_O = –200µA			2.49		V
V_{OL}	Low Level Output Voltage	I_O = 1.6mA			0.09		V
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	I_O = –200µA			1.79		V
V_{OL}	Low Level Output Voltage	I_O = 1.6mA			0.09		V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC1}	Mixer Supply Range		●	2.9	3.3	3.6	V
V_{CC2}	First Amplifier Supply Range		●	2.85	3.3	3.465	V
V_{CC3}	Second Amplifier Supply Range		●	2.85	3.3	3.465	V
V_{DD}	ADC Analog Supply Voltage		●	2.85	3.3	3.465	V
OV_{DD}	ADC Digital Output Supply Voltage		●	0.5	3.3	3.6	V
I_{CC1}	Mixer Supply Current	EN = 3V	●		82	92	mA
$I_{CC1(SHDN)}$	Mixer Shutdown Supply Current	EN = 0V	●			100	µA
I_{CC2}	First Amplifier Supply Current	AMP1SHDN = 0V	●		90	105	mA
$I_{CC2(SHDN)}$	First Amplifier Shutdown Supply Current	AMP1SHDN = 3V	●			3	mA
I_{CC3}	Second Amplifier Supply Current	AMP2SHDN = 0V	●		90	105	mA
$I_{CC3(SHDN)}$	Second Amplifier Shutdown Supply Current	AMP2SHDN = 3V	●			3	mA
I_{DD}	ADC Supply Current	ADCSHDN = 0V	●		132	156	mA
$P_{D(SHDN)}$	Power Dissipation in Shutdown	EN = 0V, AMP1SHDN = AMP2SHDN = ADCSHDN = 3V, $\overline{OE}$ = 3V, No RF, No LO, No CLK			TBD		mW
$P_{D(NAP)}$	ADC Nap Mode Power	EN = 0V, AMP1SHDN = AMP2SHDN = ADCSHDN = 3V, $\overline{OE}$ = 0V, No RF, No LO, No CLK			15		mW
$P_{D(TOTAL)}$	Total Power Dissipation	EN = 3V, AMP1SHDN = AMP2SHDN = ADCSHDN = 0V, $\overline{OE}$ = 0V, f_{SAMPLE} = MAX			1200		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency		●	1		125	MHz
t_L	CLK Low Time	Duty Cycle Stabilizer Off (Note 6) Duty Cycle Stabilizer On (Note 6)	● ●	3.8 3	4 4	500 500	ns ns
t_H	CLK High Time	Duty Cycle Stabilizer Off (Note 6) Duty Cycle Stabilizer On (Note 6)	● ●	3.8 3	4 4	500 500	ns ns
t_{AP}	Sample-and-Hold Aperture Delay	Figure 1 (Note 6, Note 7)			0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter	(Note 6, Note 7)			0.2		ps_{RMS}
t_D	CLK to DATA delay	C_L = 5pF (Note 6)	●	1.4	2.7	5.4	ns
	DATA Access Time After $\overline{OE}\downarrow$	C_L = 5pF (Note 6)	●		4.3	10	ns
	BUS Relinquish Time	(Note 6)	●		3.3	8.5	ns
	Pipeline Latency				5		Cycles

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: V_{CC1} = 3.3V, V_{CC2} = V_{CC3} = V_{DD} = 3V, AMP1SHDN = AMP2SHDN = ADCSHDN = 0V, EN = 3.3V, f_{SAMPLE} = 125MHz, RF input power = –10dBm.

Note 4: Integral nonlinearity is defined as the deviation of a code from a "best fit straight line" to the transfer curve. The deviation is measured from the center of the quantization band.

Note 5: Noise level superimposed on the GAIN pin at 140MHz required to generate spur above the noise floor.

Note 6: Guaranteed by design, not subject to test.

Note 7: Analog input measured at L8-L9 pads.

TIMING DIAGRAM

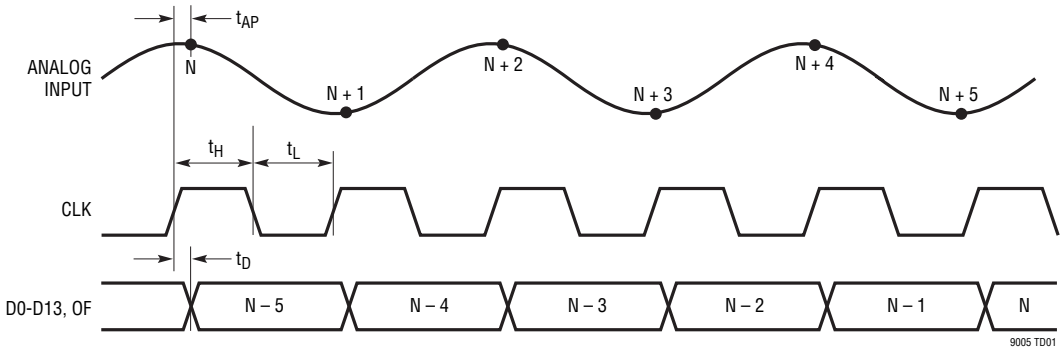
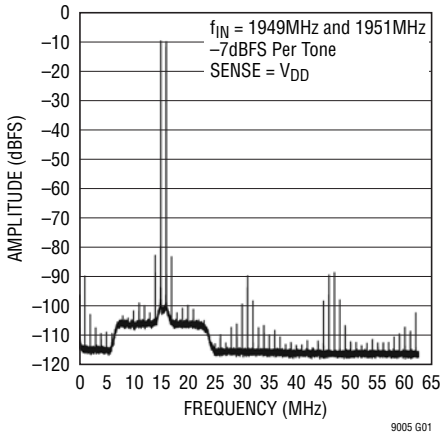


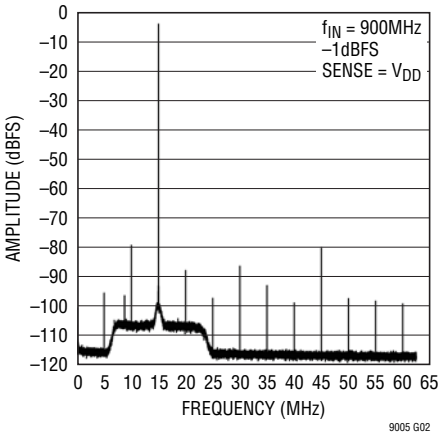
Figure 1. Digital Output Bus Timing

TYPICAL PERFORMANCE CHARACTERISTICS

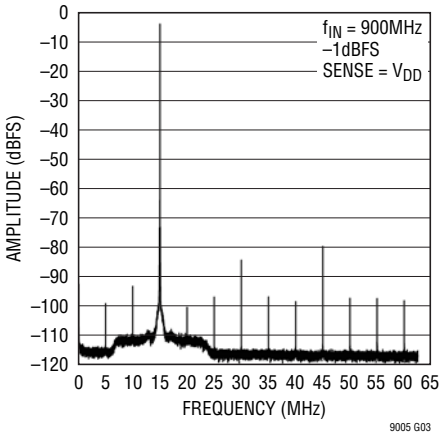
LTM9005-AA: 64K Point 2-Tone FFT



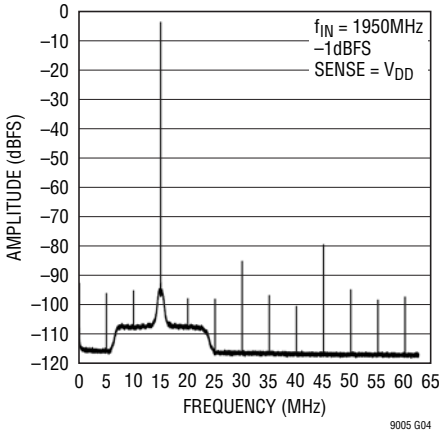
LTM9005: 64K Point FFT, Maximum Gain



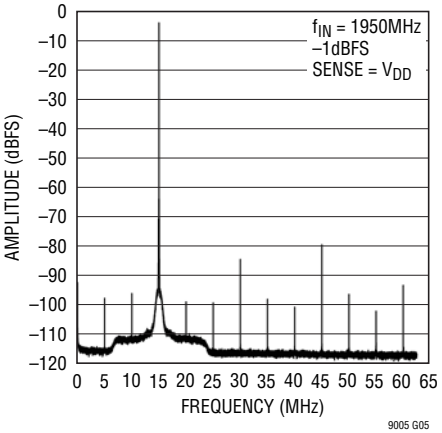
LTM9005: 64K Point FFT, Minimum Gain



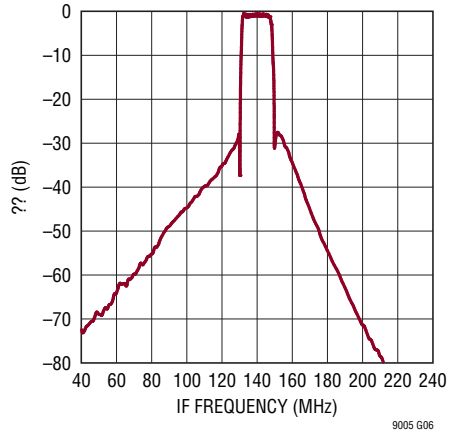
LTM9005: 64K Point FFT, Maximum Gain



LTM9005: 64K Point FFT, Minimum Gain

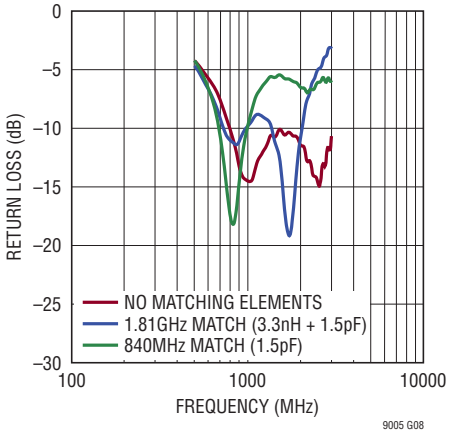


LTM9005: IF Frequency Response



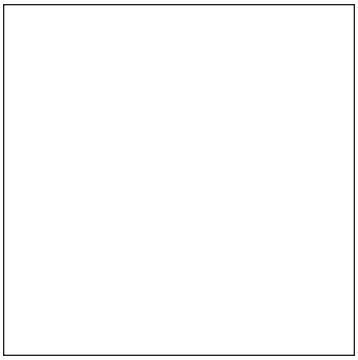
LTM9005: LO Port Impedance

LTM9005: LO Port Return Loss vs Frequency

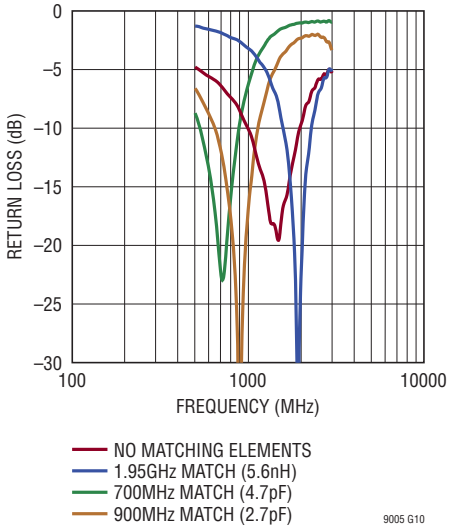


TYPICAL PERFORMANCE CHARACTERISTICS

LTM9005: RF Port Impedance



LTM9005: RF Port Return Loss vs Frequency



PIN FUNCTIONS

RF (Pin M3): Single-Ended Input for the RF Signal. This pin is internally connected to the primary side of the RF input transformer, which has low DC resistance to ground. If the RF source is not DC blocked, then a series blocking capacitor must be used. The RF input is internally matched from 1.6GHz to 2.3GHz. Operation down to 400MHz or up to 3.8GHz is possible with simple external matching.

LO (Pin M6): Single-Ended Input for the Local Oscillator Signal. This pin is internally connected to the primary side of the LO transformer, which is internally DC blocked. An external blocking capacitor is not required. The LO input is internally matched from 1GHz to 5GHz. Operation down to 380MHz is possible with simple external matching.

GAIN (Pin F1): Cathode of PIN Diode. Sinking current from GAIN attenuates the signal. The forward voltage is approximately 1V and the output impedance is 50Ω.

EN (Pin H1): Mixer Enable Pin. Connecting EN to V_{CC1} results in normal operation. Connecting EN to GND disables the mixer. The EN pin should not be left floating.

AMP1SHDN (Pin D4), AMP2SHDN (Pin L16): Amplifier Enable Pins. Connecting AMPSHDN to GND results in normal operation. Connecting AMP1SHDN to V_{CC2} disables the amplifier preceding the SAW filter and connecting AMP2SHDN to V_{CC3} disables the amplifier following the SAW filter. It is recommended to tie AMP1SHDN, AMP2SHDN and ADCSHDN together and control with 3V logic.

CLK (Pin A11): ADC Clock Input. The input sample starts on the positive edge.

ADCSHDN (Pin C13): ADC Shutdown Mode Selection Pin. Connecting ADCSHDN to GND and $\overline{OE}$ to GND results in normal operation with the ADC outputs enabled. Connecting ADCSHDN to GND and $\overline{OE}$ to V_{DD} results in normal operation with the outputs at high impedance. Connecting ADCSHDN to V_{DD} and $\overline{OE}$ to GND results in nap mode with the outputs at high impedance. Connecting ADCSHDN to V_{DD} and $\overline{OE}$ to V_{DD} results in sleep mode with the outputs at high impedance.

$\overline{OE}$ (Pin C12): Output Enable Pin. Refer to ADCSHDN pin function.

PIN FUNCTIONS

D0 – D13 (See Table for Pin Locations): Digital Outputs. D13 is the MSB.

OF (Pin G15): Over/Under Flow Output. High when an over or under flow has occurred.

MODE (Pin F15): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to GND selects offset binary output format and turns the clock duty cycle stabilizer off. 1/3 V_{DD} selects offset binary output format and turns the clock duty cycle stabilizer on. 2/3 V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer on. V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer off.

SENSE (Pin H12): Reference Programming Pin. Connecting SENSE to V_{DD} selects the internal reference and the default input range. Connecting SENSE to 1.5V selects the internal reference and a 3dB lower input range. An external reference greater than 0.5V and less than 1V applied to SENSE selects the external reference. A 1V external reference sets the input range equal to the default input range, a 0.5V external reference sets the input range 3dB lower and an external value between 0.5V and 1V sets the input range proportionally.

A8 (Pin A8): Test Pin Used During Manufacturing Only. Connect directly to B8. Keep this connection free from noise.

A9 (Pin A9): Test Pin Used During Manufacturing Only. Connect directly to B9. Keep this connection free from noise.

B8 (Pin B8): Test Pin Used During Manufacturing Only. Connect directly to A8. Keep this connection free from noise.

B9 (Pin B9): Test Pin Used During Manufacturing Only. Connect directly to A9. Keep this connection free from noise.

L8 (Pin L8): Test Pin Used During Manufacturing Only. Connect directly to M8. Keep this connection free from noise.

L9 (Pin L9): Test Pin Used During Manufacturing Only. Connect directly to M9. Keep this connection free from noise.

M8 (Pin M8): Test Pin Used During Manufacturing Only. Connect directly to L8. Keep this connection free from noise.

M9 (Pin M9): Test Pin Used During Manufacturing Only. Connect directly to L9. Keep this connection free from noise.

OGND (Pins A16, A17, B17, C16 and C17): Output Driver Ground.

OV_{DD} (Pins D16 and D17): Positive Supply for the Output Drivers. This supply is internally bypassed to GND. OV_{DD} can be 0.5V to 3.6V.

V_{CC1} (Pins K1 and K2): 3.3V Supply Voltage for Mixer. V_{CC1} is internally bypassed to GND.

V_{CC2} (Pins B1 and C1): 3.3V Supply Voltage for First Amplifier. V_{CC2} is internally bypassed to GND. Can operate at 3V if desired.

V_{CC3} (Pins M14 and M15): 3.3V Supply Voltage for Second Amplifier. V_{CC3} is internally bypassed to GND. Can operate at 3V if desired.

V_{DD} (Pins A13 and B13): 3.3V Supply Voltage for ADC. V_{DD} is internally bypassed to GND. Can operate at 3V if desired.

GND (See Table for Pin Locations): Module Ground.

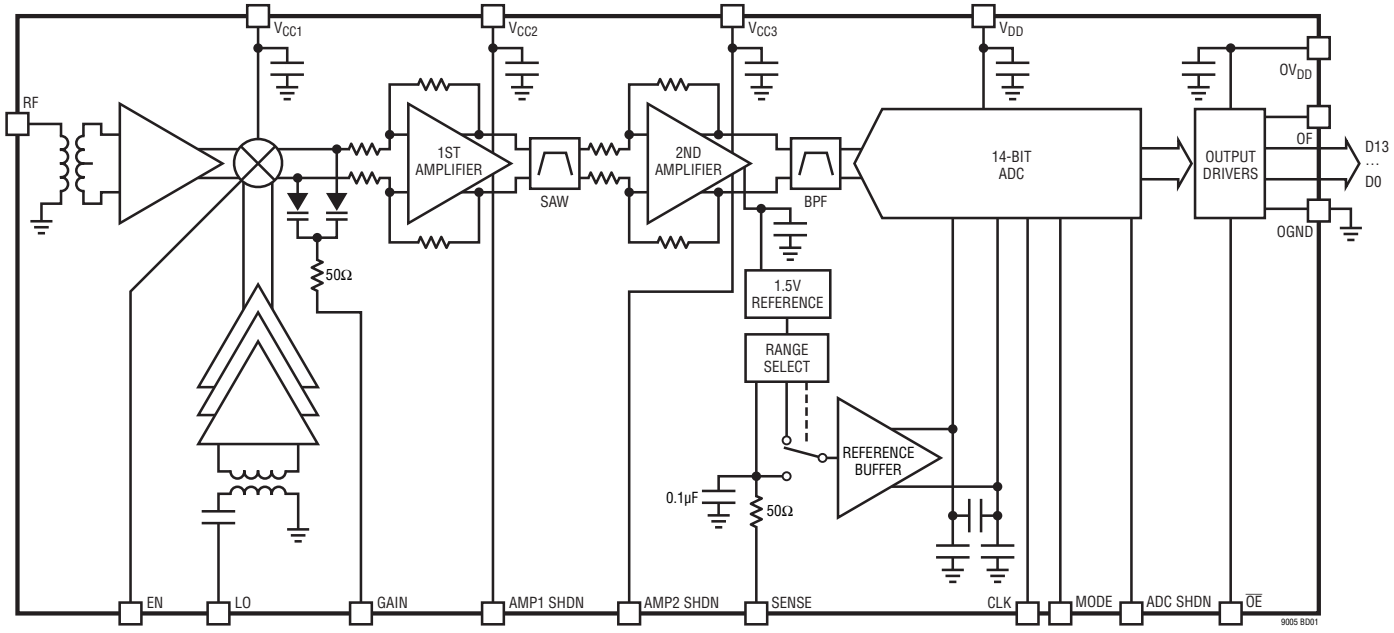
PIN FUNCTIONS

Pin Configuration

	A	B	C	D	E	F	G	H	J	K	L	M
1	GND	V_{CC2}	V_{CC2}	GND	GND	GAIN	GND	EN	GND	V_{CC1}	GND	GND
2	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{CC1}	GND	GND
3	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RF
4	GND	GND	GND	AMP1 SHDN	GND	GND	GND	GND	GND	GND	GND	GND
5	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
6	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	LO
7	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
8	A8	B8	GND	GND	GND	GND	GND	GND	GND	GND	L8	M8
9	A9	B9	GND	GND	GND	GND	GND	GND	GND	GND	L9	M9
10	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
11	CLK	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
12	GND	GND	$\overline{OE}$	GND	GND	GND	GND	SENSE	GND	GND	GND	GND
13	V_{DD}	V_{DD}	ADC SHDN	GND	GND	GND	GND	GND	GND	GND	GND	GND
14	D0	D2	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{CC3}
15	D1	D3	GND	GND	D5	MODE	OF	GND	GND	GND	GND	V_{CC3}
16	OGND	D4	OGND	OV_{DD}	D6	D9	D11	D13	GND	GND	AMP2 SHDN	GND
17	OGND	OGND	OGND	OV_{DD}	D7	D8	D10	D12	GND	GND	GND	GND

Top View of LGA Package (Looking Through Component)

BLOCK DIAGRAM



Simplified Block Diagram

OPERATION

DESCRIPTION

The LTM9005 is an integrated System in a Package (SiP) that includes a high-speed 14-bit A/D converter, two low-distortion fixed-gain amplifiers, a SAW filter, a continuously variable attenuator and an active mixer. The LTM9005 is designed for very compact IF sampling applications with RF input frequencies up to 3.8GHz. Typical applications include wireless base stations, remote radio heads and communications test instrumentation.

All of the supply bypassing and passive filtering has been included inside the LTM9005 making the total solution size extremely small. Furthermore, the tight coupling makes the performance more consistent and less dependent on board layout. Great care has been taken to protect sensitive signals from noise within the µModule package and isolate the RF section from the digital section.

The overall gain is optimized for the dynamic range of the ADC relative to the RF input level allowed by the mixer. The equivalent cascaded noise figure is 16dB. The RF input level for –1dBFs is typically –19dBm.

The following sections describe the operation of each functional element. The SiP technology allows the LTM9005 to be customized and this is described in the Semi-Custom Options section. The outline of the remaining sections follows the basic functional elements as shown in Figure 2.

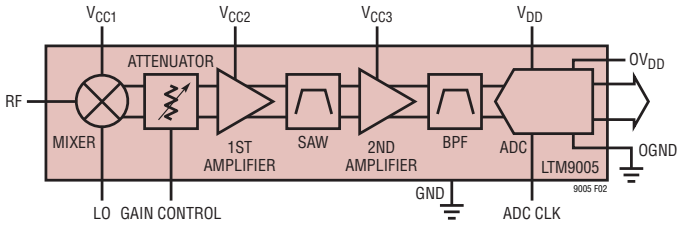


Figure 2. Basic Functional Elements

The Applications section describes the design considerations and recommendations for interfacing to the key ports and functions as well as board layout in the following order:

- RF Input Port
- LO Input Port
- ADC Clock Input Port
- GAIN Control Input
- SENSE and Reference Input
- Digital Outputs
- Shutdown Control
- Power Supplies
- Layout

SEMI-CUSTOM OPTIONS

The µModule construction affords a new level of flexibility in application-specific standard products. Standard mixed-signal, IF and RF components can be integrated regardless of their process technology and matched with passive components to a particular application. The LTM9005-AA, as the first example, is configured with a 14-bit ADC sampling at rates up to 125Msps. The total system gain is 22dB of which 20dB is variable. The IF is fixed by the SAW filter at 140MHz with 16MHz bandwidth. The RF range is matched for 1.6GHz to 2.3GHz with external matching required to achieve 400MHz to 3.8GHz.

However, other options are possible through Linear Technology's semi-custom development program. Linear Technology has in place a program to deliver other speed, resolution, RF/IF range, gain and filter configurations for nearly any specified application. ADC resolution and speed options range from 14-bits and 125Msps to 10-bits and 10Msps. The IF can be set from 70MHz to about 270MHz with bandwidths from a few MHz to about 60MHz. These semi-custom designs are based on existing ADCs, amplifiers, filters and mixers with appropriately modified matching networks. The final subsystem is then tested to the exact parameters defined for the application. The final result is a fully integrated, accurately tested and optimized solution in the same package. For more details on the semi-custom receiver subsystem program, contact Linear Technology.

OPERATION

Down-Converting Mixer

The mixer stage consists of a high linearity double-balanced mixer, RF buffer amplifier, high speed limiting LO buffer amplifier and bias/enable circuits. The RF and LO inputs are both single ended. Low side or high side LO injection can be used.

The RF input consists of an integrated transformer and a high linearity differential amplifier. The primary terminals of the transformer are connected to the RF input and ground. The secondary side of the transformer is internally connected to the amplifier's differential inputs.

The LO input consists of an integrated transformer and high speed limiting differential amplifiers. The amplifiers are designed to precisely drive the mixer for the highest linearity and the lowest noise figure.

Attenuator

A dual PIN diode with common-cathode connection is used for continuously variable attenuation. The anodes are connected to the outputs of the mixer and pulled up to V_{CC1} through 100nH inductors. The cathode includes a series 50Ω resistor to GAIN. See the GAIN Control Input section for applications information.

First and Second Amplifiers

The amplifiers used in the LTM9005 are low noise and low distortion fully differential ADC drivers. The amplifiers are fully differential amplifiers with on chip feedback resistors.

SAW Filter

A high selectivity, surface acoustic wave (SAW) filter is integrated in the LTM9005.

(Applications to provide additional text)

Band-Pass Filter

An L-C bandpass filter follows the second amplifier to prevent aliasing and to minimize the noise contribution of the second amplifier.

(Applications to provide additional text)

Analog to Digital Converter

The analog-to-digital converter (ADC) is a CMOS pipelined multistep converter. The converter has six pipelined ADC stages; a sampled analog input will result in a digitized value five cycles later (see Digital Output Bus Timing). The CLK input is single-ended. The ADC has two phases of operation, determined by the state of the CLK input pin.

Each pipelined stage contains an ADC, a reconstruction DAC and an interstage residue amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when the odd stages are outputting their residue, the even stages are acquiring that residue and visa versa.

When CLK is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors. At the instant that CLK transitions from low to high, the sampled input is held. While CLK is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H during this high phase of CLK. When CLK goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When CLK goes back high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third, fourth and fifth stages, resulting in a fifth stage residue that is sent to the sixth stage ADC for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffer.

APPLICATIONS INFORMATION

RF Input Port

The RF input is shown in Figure 3 and is internally matched from 1.6GHz to 2.3GHz, requiring no external components over this frequency range. The input return loss, shown in Figure 4, is typically 12dB at the band edges. The input match at the lower band edge can be optimized with a series 3.9pF capacitor at Pin M3, which improves the 1.6GHz return loss to greater than 25dB. Likewise, the 2.3GHz match can be improved to greater than 25dB with a series 1.5nH inductor. A series 2.7nH/2.2pF network will simultaneously optimize the lower and upper band edges and expand the RF input bandwidth to 1.2GHz to 2.5GHz. Measured RF input return losses for these three cases are also plotted in Figure 4.

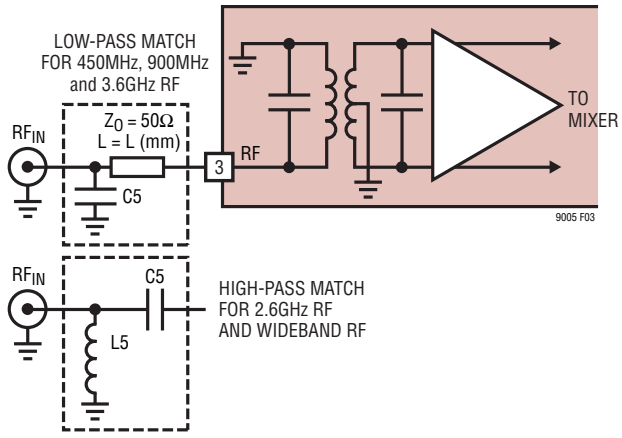


Figure 3. RF Input Schematic

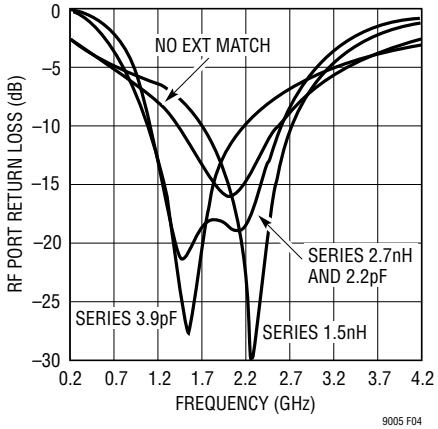


Figure 4. Series Reactance Matching

Alternatively, the input match can be shifted as low as 400MHz or up to 3800MHz by adding a shunt capacitor (C5) to the RF input. A 450MHz input match is realizedwith C5 = 12pF, located 6.5mm away from Pin M3 on a 50Ω input transmission line. A 900MHz input match requires C5 = 3.9pF, located at 1.7mm. A 3.6GHz input match is realized with C5 = 1pF, located at 2.9mm. This series transmission line/shunt capacitor matching topology allows the LTM9005 to be used for multiple frequency standards without circuit board layout modifications. The series transmission line can also be replaced with a series chip inductor for a more compact layout.

Input return losses for the 450MHz, 900MHz, 2.6GHz and 3.6GHz applications are plotted in Figure 5. The input return loss with no external matching is repeated in Figure 5 for comparison. The 2.6GHz RF input match uses the high-pass matching network shown in Figure 3 with C5 = 3.9pF and L5 = 3.6nH. The high-pass input matching network is also used to create a wideband or dual-band input match. For example, with C5 = 3.3pF and L5 = 10nH, the RF input is matched from 800MHz to 2.2GHz, with optimum matching in the 800MHz to 1.1GHz and 1.6GHz to 2.2GHz bands, simultaneously.

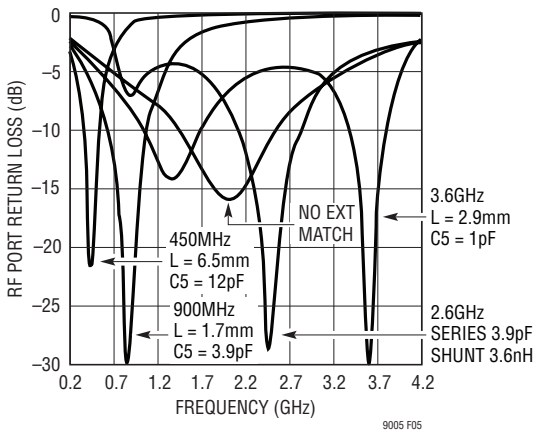


Figure 5. RF Input Return Loss with and Without Matching

APPLICATIONS INFORMATION

RF input impedance and S11 versus frequency (with no external matching) are listed in Table 1 and referenced to Pin M3. The S11 data can be used with a microwave circuit simulator to design custom matching networks and simulate board-level interfacing to the RF input filter.

Table 1 RF Input Impedance vs Frequency

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
50	4.6 + j2.3	0.832	174.7
300	9.1 + j11.2	0.706	153.8
450	12.0 + j14.5	0.639	145.8
600	14.7 + j17.4	0.588	138.7
900	20.5 + j23.3	0.506	123.4
1300	34.4 + j30.3	0.380	97.5
1700	59.6 + j23.8	0.299	55.8
1950	69.2 + j2.8	0.163	6.9
2200	59.2 – j18.1	0.184	–53.5
2450	41.5 – j24.5	0.274	–94.2
2700	28.3 – j21.3	0.374	–120.3
3000	19.0 – j13.5	0.481	–145.5
3300	13.9 – j5.1	0.568	–167.3
3600	10.8 + j3.4	0.645	171.9
3900	9.4 + j12.3	0.700	151.4

RF Input Overload

In the event of an overload condition at the RF input, (Applications to provide additional text following characterization).

LO Input Port

The LO input, shown in Figure 6, is internally matched from 1GHz to 5GHz. The input match can be shifted down, as low as 750MHz, with a single shunt capacitor (C4) on Pin M6. One example is plotted in Figure 7 where C4 = 2.7pF produces a 50MHz to 1GHz match.

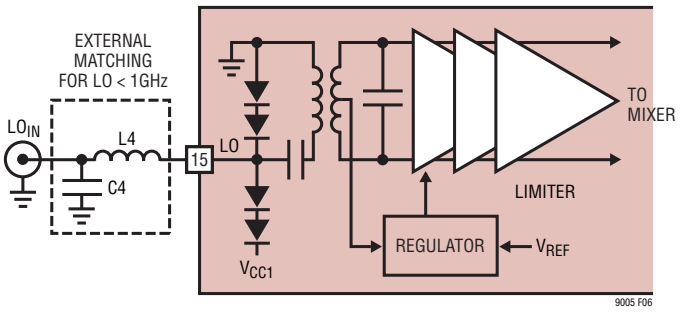


Figure 6. LO Input Schematic

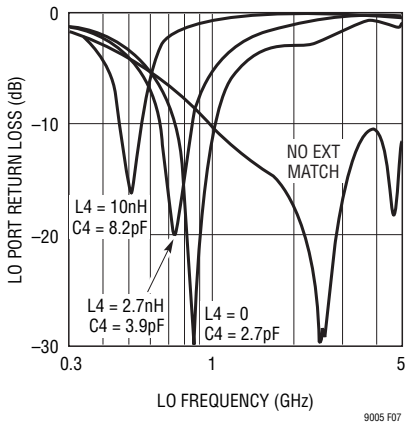


Figure 7. LO Input Return Loss

LO input matching below 750MHz requires the series inductor (L4)/shunt capacitor (C4) network shown in Figure 6. Two examples are plotted in Figure 7 where L4 = 2.7nH/C4 = 3.9pF produces a 650MHz to 830MHz match and L4 = 10nH/C4 = 8.2pF produces a 460MHz to 560MHz match.

The optimum LO drive is –3dBm for LO frequencies above 1.2GHz, although the amplifiers are designed to accommodate several dB of LO input power variation without significant mixer performance variation. Below 1.2GHz, 0dBm LO drive is recommended for optimum noise figure, although –3dBm will still deliver good conversion gain and linearity.

APPLICATIONS INFORMATION

Custom matching networks can be designed using the port impedance data listed in Table 2. This data is referenced to the LO pin with no external matching.

Table 2 LO Input Impedance vs Frequency

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
50	10.0 – j326	0.991	–17.4
300	80.5 – j41.9	0.820	–99.2
500	11.8 – j10.1	0.632	–155.9
700	18.8 + j10.9	0.474	151.8
900	35.0 + j27.4	0.350	100.8
1200	72.9 + j19.3	0.241	31.3
1500	70.0 – j12.6	0.196	–26.1
1800	55.0 – j17.0	0.167	–64.3
2200	47.8 – j9.7	0.102	–97.2
2600	53.6 – j1.9	0.039	–26.8
3000	66.7 + j0.7	0.143	2.1
3500	82.1 – j13.9	0.263	–17.4
4000	69.0 – j30.1	0.290	–43.5
4500	43.7 – j13.2	0.154	–107.5
5000	36.4 + j19.8	0.271	111.6

LO Input Overload

Text to come.

Reference Operation

The LTM9005 includes an internal voltage reference that is internally bypassed. An external reference can be used or the internal reference can be configured for two pin selectable input ranges. Tying the SENSE pin to V_{DD} selects the default range; tying the SENSE pin to 1.5V selects a 3dB lower range.

Other voltage ranges in-between the pin selectable ranges can be programmed. An external reference can be used by applying its output directly or through a resistive divider to SENSE. It is not recommended to drive the SENSE pin with a logic device. The SENSE pin should be tied to the appropriate level as close to the converter as possible. If the SENSE pin is driven externally, note that this pin is filtered internally with a 50Ω series resistor and a 0.1µF capacitor to ground.

ADC Clock Input

The CLK input can be driven directly with a CMOS or TTL level signal. A sinusoidal clock can also be used along with a low-jitter squaring circuit before the CLK pin (Figure 8).

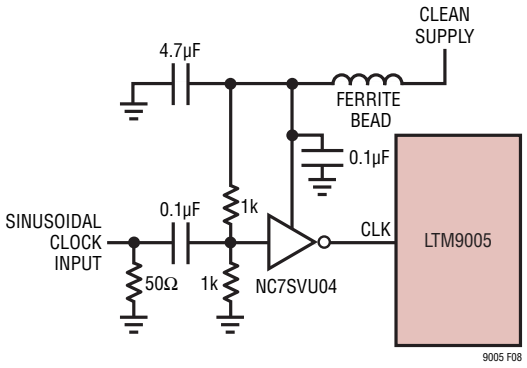


Figure 8. Sinusoidal Single-Ended CLK Driver

The noise performance of the ADC can depend on the clock signal quality as much as on the analog input. Any noise present on the CLK signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical, use as large an amplitude as possible. Also, if the ADC is clocked with a sinusoidal signal, filter the CLK signal to reduce wideband noise and distortion products generated by the source.

Figure 9 and Figure 10 show alternatives for converting a differential clock to the single-ended CLK input. The use of a transformer provides no incremental contribution

APPLICATIONS INFORMATION

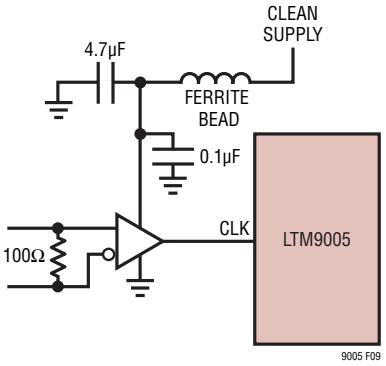


Figure 9. CLK Driver Using an LVDS or PECL to CMOS Converter

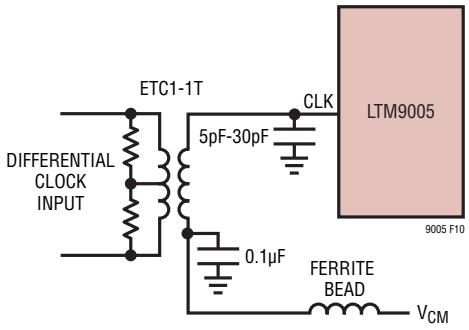


Figure 10. LVDS or PECL CLK Drive Using a Transformer

to phase noise. The LVDS or PECL to CMOS translators provide little degradation below 70MHz, but at 140MHz will degrade the SNR compared to the transformer solution. The nature of the received signals also has a large bearing on how much SNR degradation will be experienced. For high crest factor signals such as WCDMA or OFDM, the use of these translators will have a lesser impact.

The transformer in the example may be terminated with the appropriate termination for the signaling in use. The use of a transformer with a 1:4 impedance ratio may be desirable in cases where lower voltage differential signals are considered. The center tap may be bypassed to ground through a capacitor close to the ADC if the differential signals originate on a different plane. The use of a capacitor at the input may result in peaking, and depending on transmission line length may require a 10Ω to 20Ω series resistor to act as both a lowpass filter for high frequency noise that may be induced into the clock line by neighboring digital signals, as well as a damping mechanism for reflections.

Maximum and Minimum Conversion Rates

The maximum conversion rate for the ADC is 125Msps. The lower limit of the sample rate is determined by the droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTM9005 is 1Msps.

Clock Duty Cycle Stabilizer

An optional clock duty cycle stabilizer circuit ensures high performance even if the input clock has a non 50% duty cycle. Using the clock duty cycle stabilizer is recommended for most applications. To use the clock duty cycle stabilizer, the MODE pin should be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

This circuit uses the rising edge of the CLK pin to sample the analog input. The falling edge of CLK is ignored and the internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 40% to 60% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require a hundred clock cycles for the PLL to lock onto the input clock.

For applications where the sample rate needs to be changed quickly, the clock duty cycle stabilizer can be disabled. If the duty cycle stabilizer is disabled, care should be taken to make the sampling clock have a 50% (±5%) duty cycle.

GAIN Control Input

The total receiver gain is continuously adjustable using a PIN diode. Maximum gain is set by forcing GAIN to V_{CC1}.

APPLICATIONS INFORMATION

Minimum gain is achieved by sinking approximately 10mA from the GAIN pin. If the gain is to be adjusted as part of an active control loop then the circuit in Figure 11 can be used. See the Typical Performance Characteristics for the transfer function.

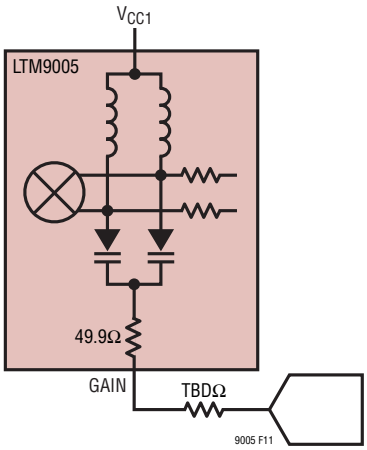


Figure 11. Automatic Gain Control Circuit

The DAC used to control GAIN will contribute a non-negligible amount of voltage noise. (Text to come—discuss further and provide noise analysis.)

In some applications it may be sufficient to permanently set the gain to a fixed level. This simplifies the circuitry as a fixed resistor to ground can be implemented.

DIGITAL OUTPUTS

Table 3 shows the relationship between the analog input voltage, the digital data bits, and the overflow bit.

Table 3. Output Codes vs Input Voltage, LTM9005-AA

INPUT (SENSE = V_{DD})	OF	D13 – D0 (OFFSET BINARY)	D13 – D0 (2'S COMPLEMENT)
Overvoltage	1	11 1111 1111 1111	01 1111 1111 1111
Maximum	0	11 1111 1111 1111	01 1111 1111 1111
	0	11 1111 1111 1110	01 1111 1111 1110
	0	10 0000 0000 0001	00 0000 0000 0001
	0	10 0000 0000 0000	00 0000 0000 0000
	0	01 1111 1111 1111	11 1111 1111 1111
	0	01 1111 1111 1110	11 1111 1111 1110
	0	00 0000 0000 0001	10 0000 0000 0001
Minimum	0	00 0000 0000 0000	10 0000 0000 0000
Undervoltage	1	00 0000 0000 0000	10 0000 0000 0000

Digital Output Modes

Figure 12 shows an equivalent circuit for a single output buffer. Each buffer is powered by OV_{DD} and OGND, isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

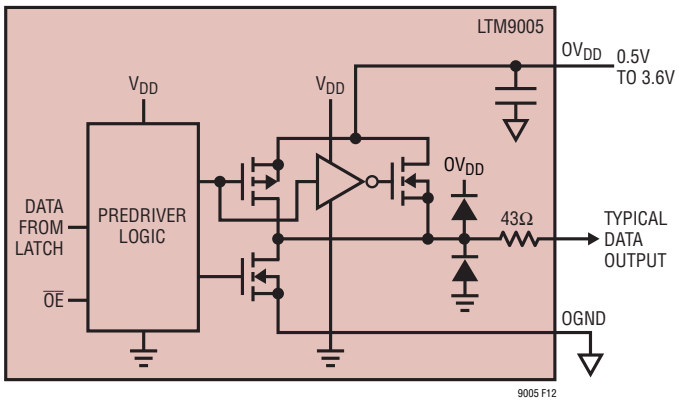


Figure 12. Digital Output Buffer

As with all high speed/high resolution converters the digital output loading can affect the performance. The digital outputs of the ADC should drive a minimal capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. For full speed operation, the capacitive load should be kept under 10pF.

Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

Data Format

Using the MODE pin, the ADC parallel digital output can be selected for offset binary or 2's complement format. Connecting MODE to GND or $1/3V_{DD}$ selects straight binary output format. Connecting MODE to $2/3V_{DD}$ or V_{DD} selects 2's complement output format. An external resistive divider can be used to set the $1/3V_{DD}$ or $2/3V_{DD}$ logic values. Table 5 shows the logic states for the MODE pin.

APPLICATIONS INFORMATION

Table 4. MODE Pin Function

MODE PIN	OUTPUT FORMAT	CLOCK DUTY CYCLE STABILIZER
0	Straight Binary	Off
$1/3V_{DD}$	Straight Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

Overflow Bit

When OF outputs a logic high the converter is either overranged or underranged.

Output Clock

The ADC has a delayed version of the CLK input available as a digital output, CLKOUT. The falling edge of the CLKOUT pin can be used to latch the digital output data.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied to the same supply that powers the logic being driven. For example, if the converter drives a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply.

OV_{DD} can be powered with any voltage from 500mV up to the V_{DD} of the part. OGND can be powered with any voltage from GND up to 1V and must be less than OV_{DD}. The logic outputs will swing between OGND and OV_{DD}.

Output Enable

The outputs may be disabled with the output enable pin, $\overline{OE}$. $\overline{OE}$ high disables all data outputs including OF. The data access and bus relinquish times are too slow to allow the outputs to be enabled and disabled during full speed operation. The output Hi-Z state is intended for use during long periods of inactivity.

Shutdown Modes

The LTM9005 provides several levels of shutdown. The mixer, both amplifiers and the ADC can all be shut down independently. Furthermore, the ADC may be placed in shutdown or nap modes to conserve power. Connecting ADCSHDN to GND results in normal operation. Connecting ADCSHDN to V_{DD} and $\overline{OE}$ to V_{DD} results in sleep mode, which powers down all circuitry including the reference and the ADC typically dissipates 1mW. When exiting sleep mode, it will take milliseconds for the output data to become valid because the reference capacitors have to recharge and stabilize. Connecting ADCSHDN to V_{DD} and $\overline{OE}$ to GND results in nap mode and the ADC typically dissipates 30mW. In nap mode, the on-chip reference circuit is kept on, so that recovery from nap mode is faster than that from sleep mode, typically taking 100 clock cycles. In both sleep and nap modes, all digital outputs are disabled and enter the Hi-Z state.

Amplifier Shutdown

When the ADC is in sleep or nap mode, it is recommended to shut down both the first and second amplifiers using their respective shutdown pins, AMP1SHDN and AMP2SHDN. Connecting AMPSHDN to GND results in normal operation. Connecting AMP1SHDN to V_{CC2} disables the amplifier preceding the SAW filter and connecting AMP2SHDN to V_{CC3} disables the amplifier following the SAW filter. It is recommended to tie AMP1SHDN, AMP2SHDN and ADCSHDN together and control with 3V logic.

Mixer Enable Interface

The mixer is enabled and shut down differently than the other functions in the LTM9005. The voltage necessary to turn on the mixer is 2.7V. To disable the mixer, the enable voltage must be less than 0.3V. If the EN pin is allowed to float, the mixer will tend to remain in its last operating state. Thus it is not recommended that the enable function be used in this manner. If the shutdown function is not required, then the EN pin should be connected directly to V_{CC1}.

Supply Sequencing

The V_{CC} pins provide the supplies to the mixer and both amplifiers. The V_{DD} pin provides the supply to the ADC. Each V_{CC} pin is brought out separately and internally bypassed. The mixer, both amplifiers and the ADC are separate integrated circuits within the LTM9005; however, there are no supply sequencing considerations beyond

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standard practice. It is recommended that all supply inputs use the same low noise, 3.3V supply, but the ADC and the amplifiers may be operated from a lower voltage level if desired. All three rails can operate from the same 3.3V linear regulator but place a ferrite bead between the supply pins. Separate linear regulators can be used without additional supply sequencing circuitry if they have common input supplies.

Grounding and Bypassing

The LTM9005 requires a printed circuit board with a clean unbroken ground plane; a multilayer board with an internal ground plane is recommended. The pinout of the LTM9005 has been optimized for a flow-through layout so that the interaction between inputs and digital outputs is minimized. The placement of critical pads allows for those signals to be routed on the top layer.

The ground planes within the LTM9005 are broken in to three areas: RF ground, IF ground and digital ground. The mixer (V_{CC1}) and first amplifier (V_{CC2}) return to RF ground. In Figure ?, this area is to the left of the line starting between pads M6 and M7 and ending between pads A10 and A11. The RF ground plane is bridged to the IF ground plane by the SAW filter. All GND pins can connect to the same ground plane. It is not necessary to break these ground planes on the circuit board but the pads are separated and available for use.

The second amplifier (V_{CC3}) and the analog portion of the ADC (V_{DD}) return to IF ground. All GND pads to the right of line described above are IF ground. The IF ground plane is bridged to the digital ground plane by the ADC die. The digital ground plane uses the OGND pads and extends under all of the digital output pads.

The LTM9005 is internally bypassed with the mixer (V_{CC1}), first amplifier (V_{CC2}), second amplifier (V_{CC3}) and ADC (V_{DD}) supplies returning to ground (GND). The digital output supply (OV_{DD}) is returned to OGND. Additional bypass capacitance is optional and may be required if power supply noise is significant.

Heat Transfer

Most of the heat generated by the LTM9005 is transferred through the bottom-side ground pads. For good electrical and thermal performance, it is critical that all ground pins are connected to a ground plane of sufficient area with as many vias as possible.

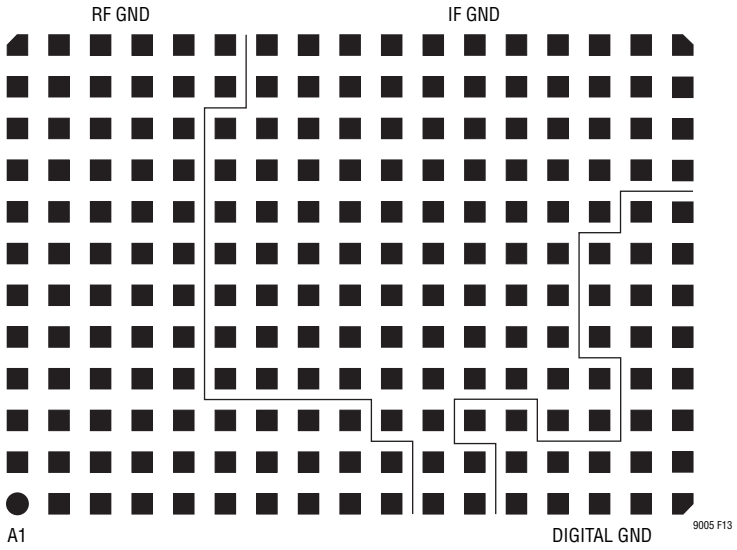

Figure 13

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Recommended Layout

The high integration of the LTM9005 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for ground. This helps to dissipate heat in the package through the board and also helps to shield sensitive on-board analog signals. Common ground (GND) and output ground (OGND) are electrically isolated on the LTM9005, but can be connected on the PCB underneath the part to provide a common return path.
- Use multiple ground vias. Using as many vias as possible helps to improve the thermal performance of the board and creates necessary barriers sepa-rating analog and digital traces on the board at high frequencies.
- Separate analog and digital traces as much as possible, using vias to create high-frequency barriers. This will reduce digital feedback that can reduce the signal-to-noise ratio (SNR) and dynamic range of the LTM9005.
- Connect pad A8 to B8 on the top layer with no other connections. These pads should not be connected to any other circuitry or ground. Keep these two pads free from noise. Connect A9 to B9, L8 to M8 and L9 to M9 in the same manner.

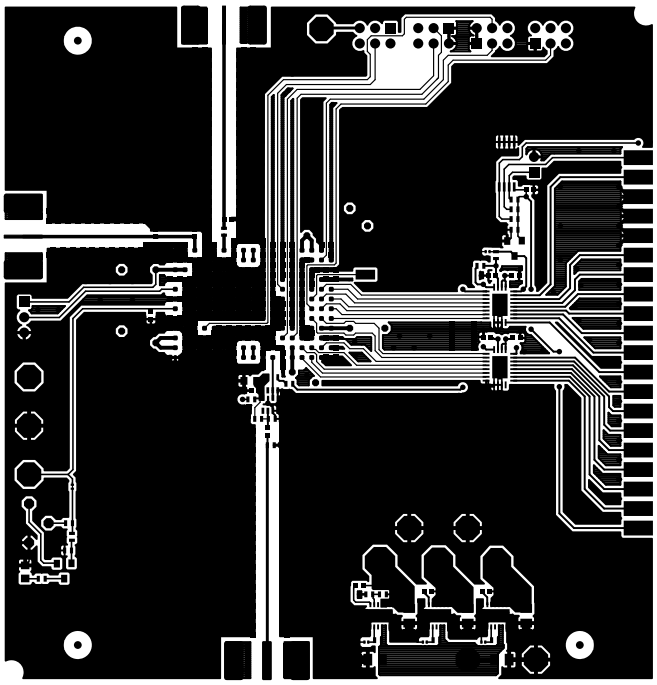
Figure # through ## give a good example of the recommended layout.

The quality of the paste print is an important factor in producing high yield assemblies. It is recommended to use a type 3 or 4 printing no-clean solder paste. The solder stencil design should follow the guidelines outlined in Application Note 100. Avoid ultrasonic cleaning.

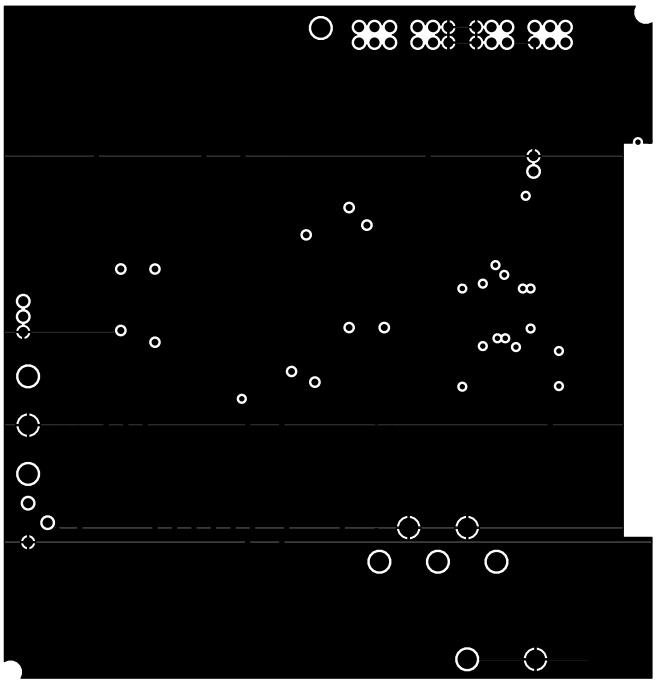
The LTM9005 employs gold-finished pads for use with Pb-based or tin-based solder paste. It is inherently Pb-free and complies with the JEDEC (e4) standard. The materials declaration is available online at http://www.linear.com/leadfree/mat_dec.jsp.

APPLICATIONS INFORMATION

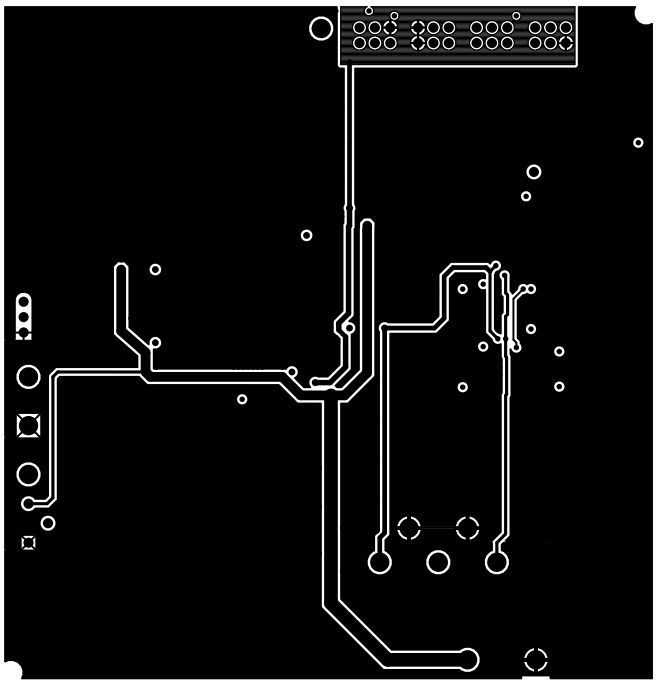
Layer 1



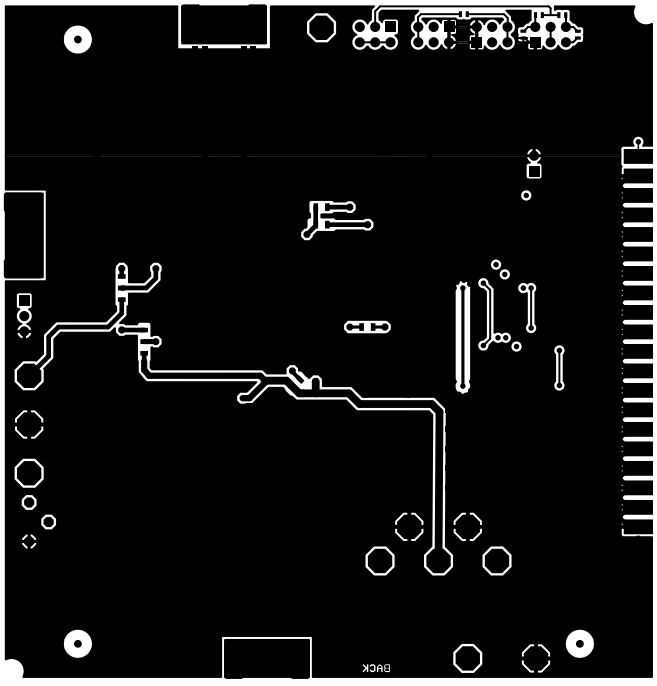
Layer 2



Layer 3

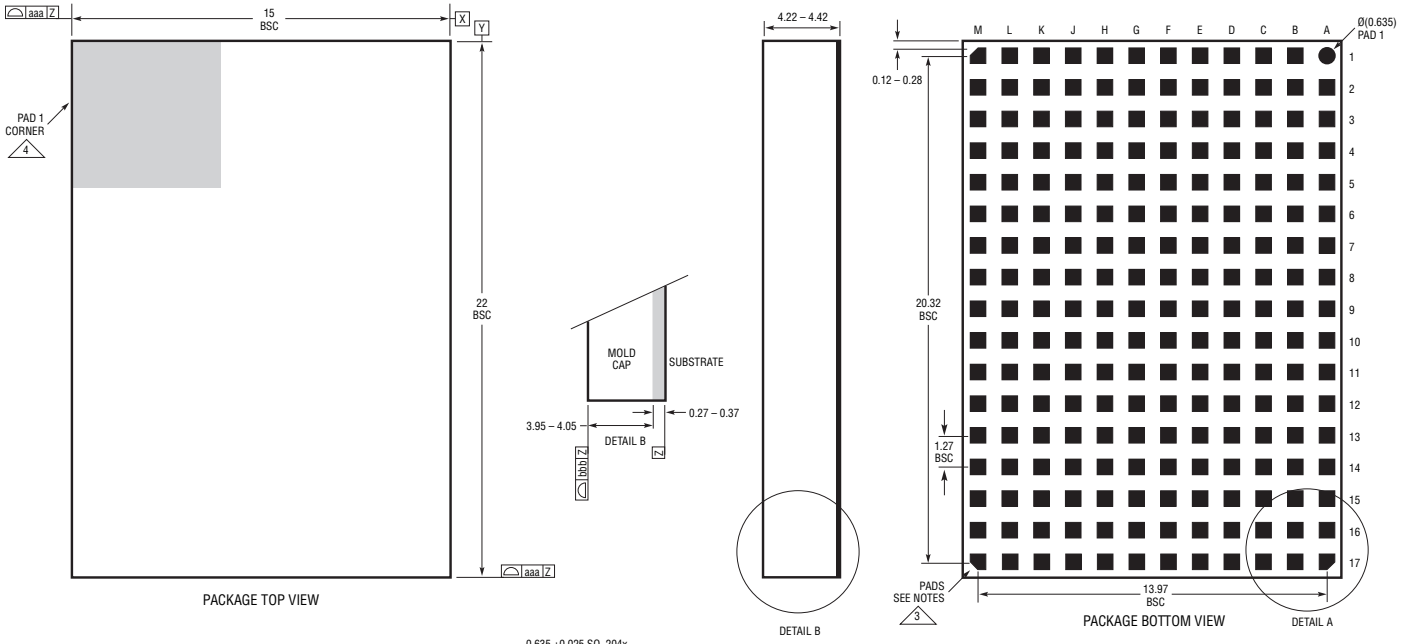


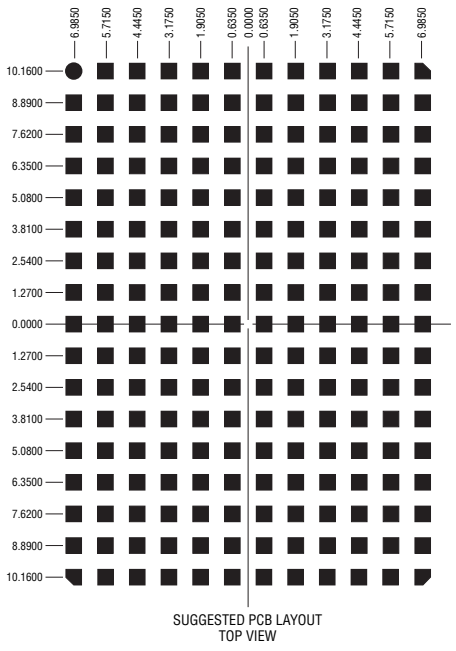
Layer 4

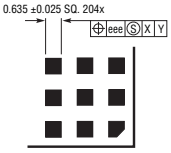


PACKAGE DESCRIPTION

LGA Package
204-Lead (22mm × 15mm × 4.32mm)
(Reference LTC DWG # 05-08-1841 Rev Ø)

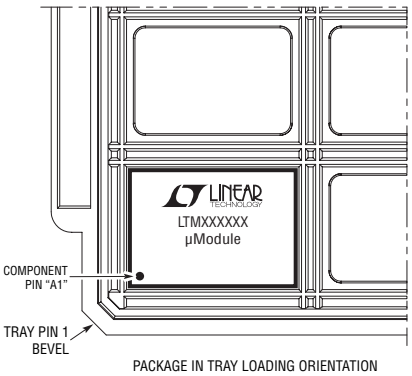






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 204

SYMBOL	TOLERANCE
aaa	0.15
bbb	0.10
eee	0.05



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2225	12-Bit, 10Msps ADC	60mW, 71dB SNR, 5mm × 5mm QFN
LTC2226	12-Bit, 25Msps ADC	75mW, 71dB SNR, 5mm × 5mm QFN
LTC2227	12-Bit, 40Msps ADC	125mW, 71dB SNR, 5mm × 5mm QFN
LTC2228	12-Bit, 65Msps ADC	210mW, 71dB SNR, 5mm × 5mm QFN
LTC2229	12-Bit, 80Msps ADC	230mW, 70.6dB SNR, 5mm × 5mm QFN
LTC2245	14-Bit, 10Msps ADC	60mW, 74.4dB SNR, 5mm × 5mm QFN
LTC2246	14-Bit, 25Msps ADC	75mW, 74dB SNR, 5mm × 5mm QFN
LTC2247	14-Bit, 40Msps ADC	125mW, 74dB SNR, 5mm × 5mm QFN
LTC2248	14-Bit, 65Msps ADC	210mW, 74dB SNR, 5mm × 5mm QFN
LTC2249	14-Bit, 80Msps ADC	230mW, 73dB SNR, 5mm × 5mm QFN
LTC2252	12-Bit, 105Msps, 3V ADC, Lowest Power	320mW, 70.2dB SNR, 32-Pin QFN Package
LTC2253	12-Bit, 125Msps ADC, 3V ADC, Lowest Power	395mW, 70.2dB SNR, 32-Pin QFN Package
LTC2254	14-Bit, 105Msps, 3V ADC, Lowest Power	320mW, 72.4dB SNR, 88dB SFDR, 32-Pin QFN Package
LTC2255	14-Bit, 125Msps ADC, 3V ADC, Lowest Power	395mW, 72.5dB SNR, 88dB SFDR, 32-Pin QFN Package
LT5527	400MHz to 3.7GHz, 5V High Signal Level Downconverting Mixer	23.5dBm IIP3 at 1.9GHz, NF = 12.5dB, Single-Ended RF and LO Ports
LT5557	800MHz to 2.7GHz High Linearity Direct Conversion Quadrature Demodulator	24.7dBm IIP3 at 1.9GHz, NF = 11.7dB, Single-Ended RF and LO Ports, 3.3V Supply
LTC6400-8/LTC6400-14/ LTC6400-20/LTC6400-26	Low Noise, Low Distortion Differential Amplifier for 300MHz IF, Fixed Gain of 8dB, 14dB, 20dB or 26dB	3V, 90mA, 39.5dBm OIP3 at 300MHz, 6dB NF
LTC6401-8/LTC6401-14/ LTC6401-20/LTC6401-26	Low Noise, Low Distortion Differential Amplifier for 140MHz IF, Fixed Gain of 8dB, 14dB, 20dB or 26dB	3V, 45mA, 45.5dBm OIP3 at 140MHz, 6dB NF
LTM9001	16-Bit, High-Speed Receiver Subsystem	µModule Receiver with ADC, Fixed Gain Amplifier and Anti-Alias Filter in 11.25mm × 11.25mm LGA
LTM9002	14-Bit, High-Speed Dual Receiver Subsystem	µModule Receiver with Dual ADC, Dual Amplifiers, Anti-Alias Filters and a Dual Trim DAC in 15mm × 11.25mm LGA

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