International
IOR Rectifier

3A Highly Integrated Sup*IR*Buck® Single-Input Voltage, Synchronous Buck Regulator

IR3823

FEATURES

- Single input voltage range from 5V to 21V
- Wide Input voltage range from 1.0V to 21V with external V_{CC} bias voltage
- Output voltage from 0.6V to 0.86% of PVin
- Enhanced line/load regulation with feedforward
- Programmable switching frequency up to 1.5MHz
- Three user selectable soft-start time options
- Thermally compensated current limit with robust hiccup mode over current protection
- Synchronization to an external clock
- Precise reference voltage (0.6V+/-0.6%)
- Open-drain PGood indication
- Output over voltage protection
- Enable Input with Under-Voltage Lockout (UVLO)
- V_{CC} Under-Voltage Lockout (UVLO)
- Enhanced Pre-bias start-up
- Integrated MOSFET drivers and Bootstrap Diode
- Thermal shut-down
- -40°C to 125°C operating junction temperature
- 3.5mm x 3.5mm PQFN package
- Lead-free, Halogen-free and RoHS6 Compliant

DESCRIPTION

The IR3823 SupIRBuck® is a 3A easy-to-use, fully integrated and highly efficient synchronous Buck regulator intended for Point-Of-Load (POL) applications.

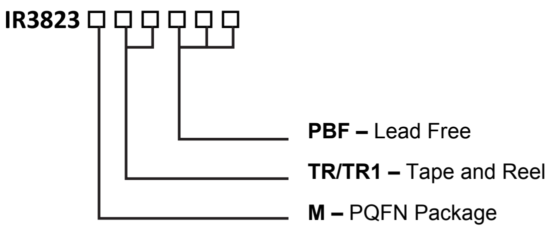
The IR3823 features programmable switching frequency from 300kHz to 1.5MHz, three selectable soft-start time options, and smooth synchronization to an external clock. The IR3823 uses voltage mode control employing a proprietary PWM modulator, allowing high control bandwidth and fast loop response with less output capacitors. The other important functions include thermally compensated over current protection, output over voltage protection and thermal shut-down, etc. The IR3823 is offered in a small 3.5mm x 3.5mm PQFN package with excellent thermal performance.

APPLICATIONS

- Computing Applications
- Set Top Box Applications
- Storage Applications
- Data Center Applications
- Telecom Applications
- Distributed Point of Load Power Architectures

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR3823	PQFN 3.5 mm x 3.5 mm	Tape and Reel	750	IR3823MTR1PBF
IR3823	PQFN 3.5 mm x 3.5 mm	Tape and Reel	4000	IR3823MTRPBF



BASIC APPLICATION

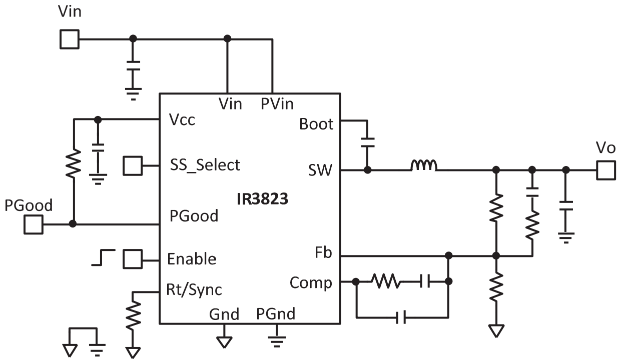

Vin
Vin
PVin
Vcc
Boot
SS_Select
SW
Vo
IR3823
PGood
PGood
Enable
Fb
Rt/Sync
Comp
Gnd
PGnd

Figure 1: IR3823 Basic Application Circuit

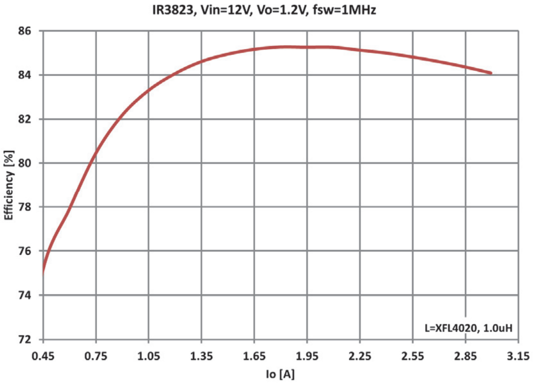


Figure 2: IR3823 Efficiency

PINOUT DIAGRAM

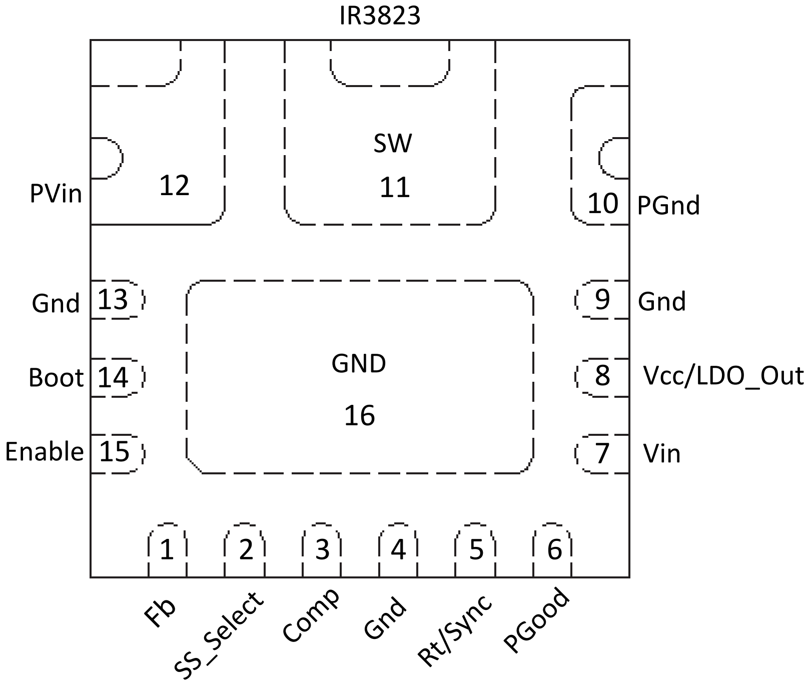

IR3823
PVin
12
SW
11
10
PGnd
Gnd
13
9
Gnd
Boot
14
GND
16
8
Vcc/LDO_Out
Enable
15
7
Vin
1
2
3
4
5
6
Fb
SS_Select
Comp
Gnd
Rt/Sync
PGood

Figure 3: 3.5mm x 3.5mm PQFN (Top View)

BLOCK DIAGRAM

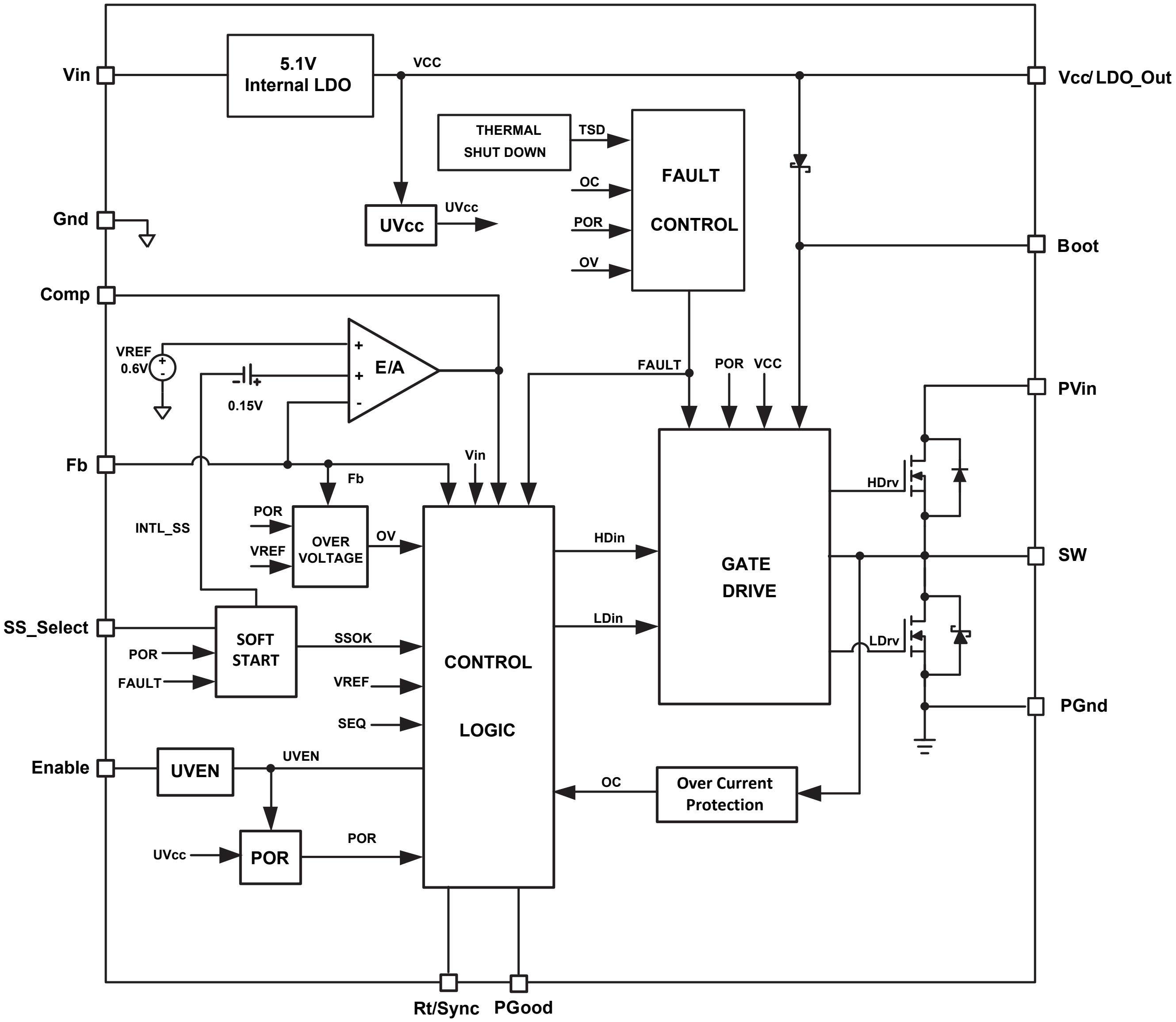

Vin
5.1V
Internal LDO
VCC
Vcc/LDO_Out
THERMAL
SHUT DOWN
TSD
FAULT
CONTROL
OC
POR
OV
Gnd
UVcc
UVcc
Boot
Comp
VREF
0.6V
0.15V
E/A
FAULT
POR
VCC
PVin
Fb
Vin
Fb
HDrv
INTL_SS
POR
VREF
OVER
VOLTAGE
OV
HDin
GATE
DRIVE
SW
SS_Select
SOFT
START
SSOK
LDin
LDrv
POR
FAULT
VREF
CONTROL
LOGIC
PGnd
SEQ
Enable
UVEN
UVEN
OC
Over Current
Protection
UVcc
POR
POR
Rt/Sync
PGood

Figure 4: Simplified Block Diagram

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	Fb	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
2	SS_Select	Soft start selection pin. Three user selectable soft start time is available: 1.5ms (SS_Select=Vcc), 3ms (SS_Select=Float), 6ms (SS_Select=Gnd)
3	Comp	Output of the error amplifier. The loop compensation network should be connected between Comp and Fb pin.
4,9,13, 16	Gnd	Analog ground for the internal reference and the control circuitry.
5	Rt/Sync	Multi-function pin to set the switching frequency. The internal oscillator frequency is set with a resistor between this pin and Gnd. Or synchronization to an external clock by connecting this pin to the external clock signal through a diode.
6	PGood	Open-drain power good indication pin. Connect a pull-up resistor from this pin to Vcc.
7	Vin	Input of the Internal LDO. A 1.0µFceramic capacitor should be connected between this pin and PGnd. If an external Vcc voltage is used, this pin should be shorted to Vcc pin.
8	Vcc/LDO_Out	Output of the internal LDO and optional input of an external biased supply voltage. A minimum 2.2µF ceramic capacitor is recommended between this pin and PGnd.
10	PGnd	Power Ground. This pin serves as a separated ground for the MOSFET drivers and should be connected to the system power ground plane.
11	SW	Switch node. Connect this pin to the output inductor.
12	PVin	Power stage input.
14	Boot	Supply voltage for the high-side driver. A 100nF ceramic capacitor should be connected between this pin and SW pin.
15	Enable	Enable pin to turn on/off the device. Connect this pin to PVin pin through a resistor divider to implement the input voltage UVLO.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond these listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PVin, Vin to PGnd (Note 3)	-0.3V to 25V
Vcc/LDO_Out to PGnd (Note 3)	-0.3V to 8V (Note 1)
Boot to PGnd (Note 3)	-0.3V to 33V
SW to PGnd (Note 3)	-0.3V to 25V (DC), -4V to 25V (AC, 100ns)
Boot to SW	-0.3V to V_{CC} + 0.3V (Note 2)
PGood, SS_Select to Gnd (Note 3)	-0.3V to V_{CC} + 0.3V (Note 2)
Other Input/Output Pins to Gnd (Note 3)	-0.3V to +3.9V
PGnd to Gnd	-0.3V to +0.3V
THERMAL INFORMATION	
Junction to Ambient Thermal Resistance Θ_{jA}	37.4 °C/W (Note 4)
Junction to PCB Thermal Resistance $\Theta_{j\text{-}PCB}$	10.1 °C/W
Junction to Case Top Thermal Resistance $\Theta_{j\text{-}CTop}$	120 °C/W
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C

Note 1: Vcc must not exceed 7.5V for Junction Temperature between -10°C and -40°C
Note 2: Must not exceed 8V
Note 3: PGnd pin and Gnd pin are connected together.
Note 4: Θ_{jA} is for the test in still air with IRDC3823 evaluation board. The IRDC3823 uses a 4-layer 2.6” x 2.2” FR4 PCB board. Each layer uses 2 oz. copper.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	MAX	UNITS
Input Voltage Range with External Vcc (Note 5, Note 7)	PV_{in}	1.0	21	V
Input Voltage Range with Internal LDO (Note 6, Note 7)	V_{in}, PV_{in}	5.5	21	
Supply Voltage Range (Note 6)	V_{CC}	4.5	7.5	
Supply Voltage Range (Note 6)	Boot to SW	4.5	7.5	
Output Voltage Range	V_0	0.6	0.86 x PV_{in}	
Output Current Range	I_0	0	3	A
Switching Frequency	F_S	300	1500	kHz
Operating Junction Temperature	T_J	-40	125	°C

Note 5: V_{in} is connected to V_{cc} to bypass the internal LDO.
Note 6: V_{in} is connected to PV_{in}. For single-rail applications with PV_{in}=V_{in}= 4.5V-5.5V, please refer to the application information in the section of Internal LDO and the section of Over Current Protection.
Note 7: Maximum SW node voltage should not exceed 25V.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specifications apply over, 5.5V < V_{in} = PV_{in} < 21V, 0°C < T_J < 125°C, SS_Select=Float. Typical values are specified at T_a = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Stage						
Power Losses	P_{LOSS}	PV_{in}= V_{in} = 12V, V_o = 1.2V, I_o = 3A, F_s = 1000kHz, L = 1.0uH, Note 8		0.6		W
Top Switch $R_{DS(ON)}$	$R_{DS(on)-T}$	V_{BOOT} -Vsw=5.1V,I_o = 3A, T_j = 25°C		40	52	mΩ
Bottom Switch $R_{DS(ON)}$	$R_{DS(on)-B}$	V_{cc} = 5.1V, I_o = 3A, T_j = 25°C		26	34	
Bootstrap Diode Forward Voltage	V_D	I(Boot) = 10mA	180	260	470	mV
SW Leakage Current	I_{SW}	V_{SW} = 0V, Enable = 0V, V_{FB}=1V			1	μA
		V_{SW} = 0V, Enable = High, V_{FB}=1V			1	μA
Dead Band Time	T_D	Note 8		12.5		ns
Supply Current						
Vin Supply Current (standby)	$I_{in(Standby)}$	EN = Low, No Switching V_{in}=21V, PV_{in}=0V			200	μA
Vin Supply Current (dynamic)	$I_{in(Dyn)}$	EN = High, F_{SW} =1000kHz, V_{in} = PV_{in} = 16V		10	12.5	mA

ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, these specifications apply over, 5.5V < V_{in} = PV_{in} < 21V, 0°C < T_J < 125°C, SS_Select=Float. Typical values are specified at T_a = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}/LDO_Out						
Output Voltage	V_{cc}	V_{in}(min) = 5.5V, I_o = 0-25mA C_{LOAD} = 2.2uF	4.75	5.1	5.4	V
LDO Dropout Voltage	V_{cc_drop}	V_{in}=4.7V, I_o=15mA, C_{LOAD}=2.2uF			0.4	V
Short Circuit Current	I_{short}	V_{in}=7.3V, PV_{in}=Float, V_{cc}=0V		70		mA
Oscillator						
Rt Voltage	V_{Rt}			1.0		V
Frequency Range	F_s	Rt = 80.6kΩ	270	300	330	kHz
		Rt = 23.2kΩ	900	1000	1100	
		Rt = 15kΩ	1350	1500	1650	
Ramp Amplitude	V_{ramp}	V_{in} = 5.5V, Vin slew rate max = 1V/µs, Note 8		0.825		V_{p-p}
		V_{in} = 12V, Vin slew rate max = 1V/µs, Note 8		1.80		
		V_{in} = 21V, Vin slew rate max = 1V/µs, Note 8		3.15		
		V_{in}=V_{cc}=5V, For external V_{cc} operation, Note 8		0.75		
Ramp Offset		Note 8		0.16		V
Minimum Pulse Width	$T_{min(ctrl)}$	Note 8			60	ns
Maximum Duty Cycle	D_{max}	F_s = 300kHz, V_{in} =PV_{in}= 12V	86			%
Fixed Off Time	T_{off}	Note 8		200	250	ns
Sync Frequency Range	F_{sync}		270		1650	kHz
Sync Pulse Duration	T_{sync}		100	200		ns
Sync Level Threshold	High		3.0			V
	Low				0.6	V
Error Amplifier						
Input Bias Current (V_{FB})	I_{FB}(E/A)		-1		+1	µA
Output Sink Current	I_{sink}(E/A)		0.4	0.85	1.2	mA
Output Source Current	I_{source}(E/A)		4	7.5	11	mA
Slew Rate	SR	Note 8	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	Note 8	20	30	40	MHz

ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, these specifications apply over, 5.5V < V_{in} = PV_{in} < 21V, 0°C < T_J < 125°C, SS_Select=Float. Typical values are specified at T_a = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier (Continued)						
DC Gain	Gain	Note 8	100	110	120	dB
Maximum Output Voltage	V_{max}(E/A)		1.7	2.0	2.3	V
Minimum Output Voltage	V_{min}(E/A)				100	mV
Reference Voltage (V_{REF})						
Feedback Voltage	V_{FB}			0.6		V
Accuracy		0°C < T_j < 70°C	-0.6		+0.6	%
		-40°C < T_j < 125°C ; Note 9	-1.2		+1.2	
Soft Start						
Soft Start Ramp Rate		SS_Select=V_{CC}	0.34	0.4	0.46	mV/µs
		SS_Select=Float	0.16	0.2	0.24	
		SS_Select=Gnd	0.085	0.1	0.115	
SS_Select Input Bias Current		SS_Select=Gnd		40	80	uA
Power Good						
Power Good Turn on Threshold	$VPG_{(on)}$	V_{FB} rising	85	90	95	% V_{REF}
Power Good Lower Turn off Threshold	$VPG_{(lower)}$	V_{FB} falling	80	85	90	% V_{REF}
Power Good Turn on Delay	$TPG_{(ON)\_D}$	V_{FB} rising, see $VPG_{(on)}$		2.56		ms
Power Good Upper Turn off Threshold	$VPG_{(upper)}$	V_{FB} rising	115	120	125	% V_{REF}
PGood Comparator Delay		V_{FB} < $VPG_{(lower)}$ or V_{FB} > $VPG_{(upper)}$	1	2	3.5	µs
PGood Voltage Low	PG(voltage)	I_{PGood} = -5mA			0.5	V
Under-Voltage Lockout						
V_{cc}-Start Threshold	V_{CC} UVLO Start	V_{cc} rising trip Level	3.9	4.1	4.3	V
V_{cc}-Stop Threshold	V_{CC} UVLO Stop	Vcc falling trip Level	3.6	3.8	4.0	V
Enable-Start-Threshold	Enable UVLO Start	ramping up	1.14	1.2	1.26	V
Enable-Stop-Threshold	Enable UVLO Stop	ramping down	0.95	1	1.05	
Enable Leakage Current	I_{EN_LK}	Enable = 3.3V			1	µA

ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, these specifications apply over, 5.5V < V_{in} = PV_{in} < 21V, 0°C < T_J < 125°C, SS_Select=Float. Typical values are specified at T_a = 25°C.

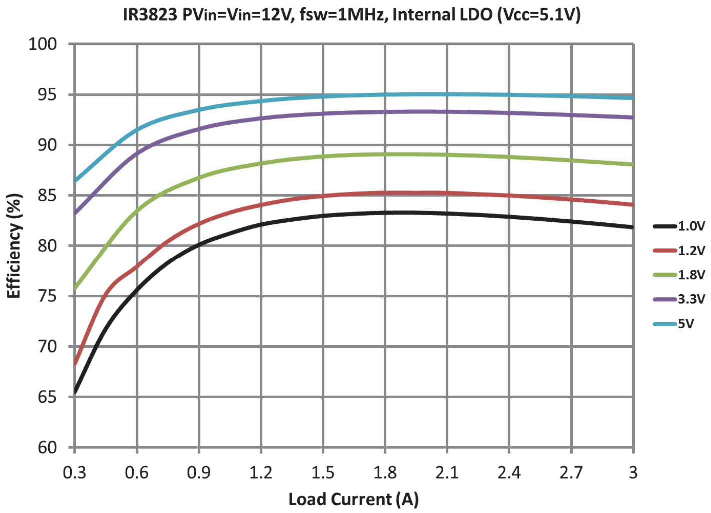
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Over-Voltage Protection						
OVP Trip Threshold	OVP_V_{th}	V_{FB} rising	115	120	125	% V_{REF}
OVP Comparator Delay	T_{OVP_D}		1	2	3.5	μs
Over-Current Protection						
Current Limit	I_{LIMIT}	T_j = 25°C, V_{CC}=5.1V	3.6	4.5	5.4	A
Hiccup Blanking Time	T_{BLK_Hiccup}	SS_Select = Vcc, Note 8		10		ms
		SS_Select = Float, Note 8		20		
		SS_Select = Gnd, Note 8		40		
Over-Temperature Protection						
Thermal Shutdown Threshold		Note 8		145		°C
Hysteresis		Note 8		20		

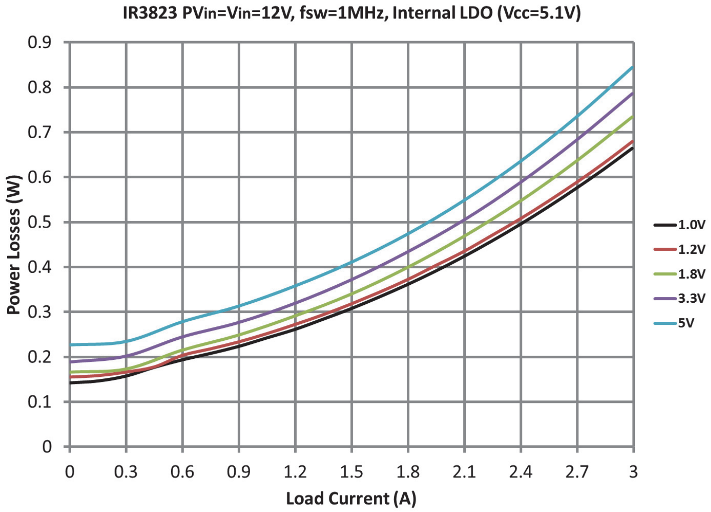
Note 8: Guaranteed by design, but not tested in production.
Note 9: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.

TYPICAL EFFICIENCY AND POWER LOSS CURVES

PV_{in} = V_{in}=12V, V_{CC}= Internal LDO, I_O = 0A-3A, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3823, the inductor losses and the losses of the input and output capacitors. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

VOUT (V)	F_S (kHz)	LOUT (µH)	P/N	DCR (mΩ)	SIZE (mm)
1.0	1000	1.0	XFL4020-102ME (Coilcraft)	10.8	4.0x4.0x2.1
1.2	1000	1.0	XFL4020-102ME (Coilcraft)	10.8	4.0x4.0x2.1
1.8	1000	1.2	PIMB053T-1R2MS-39 (Cyntec)	15	4.9x5.2x3.0
3.3	1000	2.2	XAL5030-222ME (Coilcraft)	13.2	5.28x5.48x3.1
5	1000	2.2	XAL5030-222ME (Coilcraft)	13.2	5.28x5.48x3.1





TYPICAL EFFICIENCY AND POWER LOSS CURVES

PV_{in} = 12V, V_{in}=V_{CC}= External 5V, I_O = 0A-3A, F_S = 1000 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3823, the inductor losses and the losses of the input and output capacitors. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

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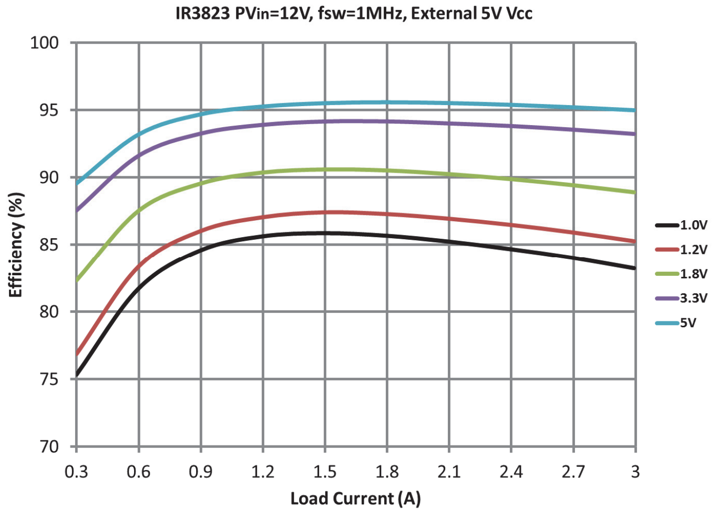

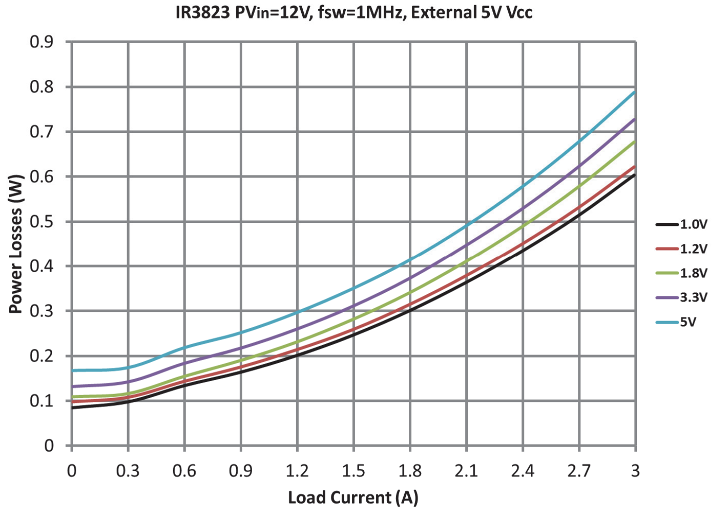

TYPICAL EFFICIENCY AND POWER LOSS CURVES

$PV_{in} = V_{in} = V_{CC} = 5V$, $I_O = 0A\text{-}3A$, $F_S = 1000$ kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of IR3823, the inductor losses and the losses of the input and output capacitors. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

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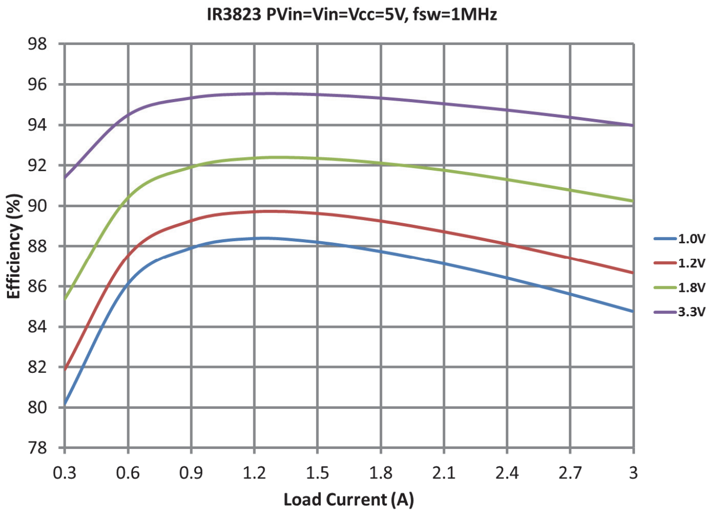
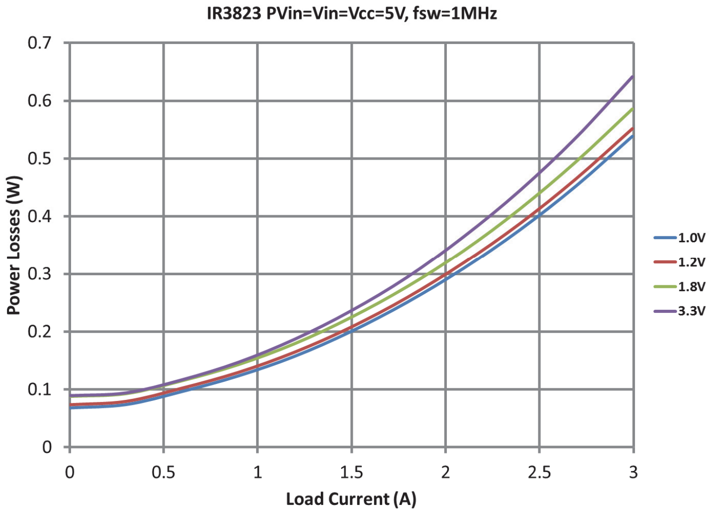
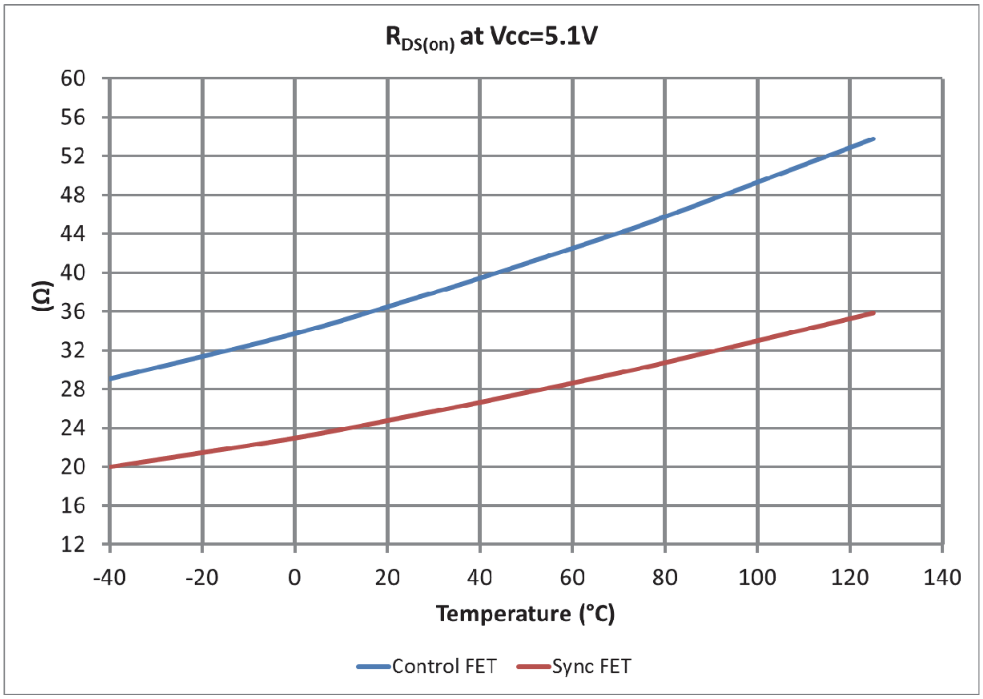
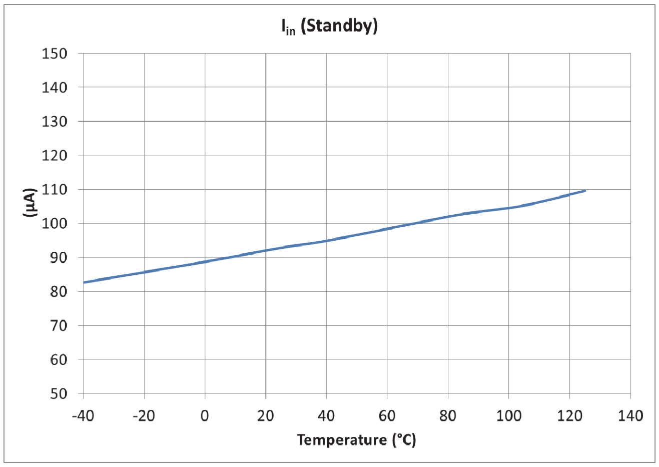


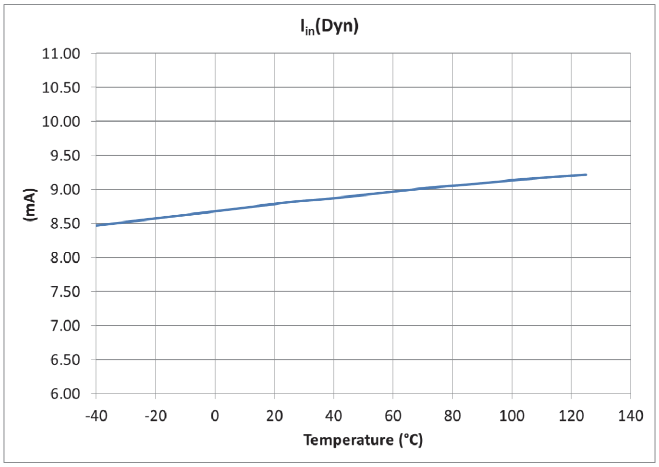


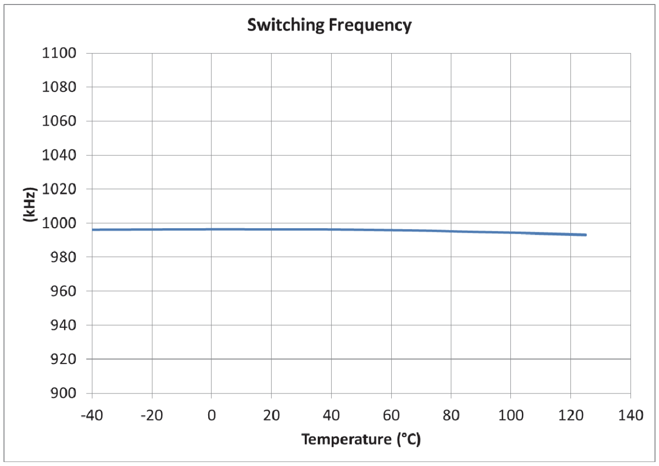
$R_{DS(ON)}$ OF MOSFETS OVER TEMPERATURE AT V_{CC}=5.1V

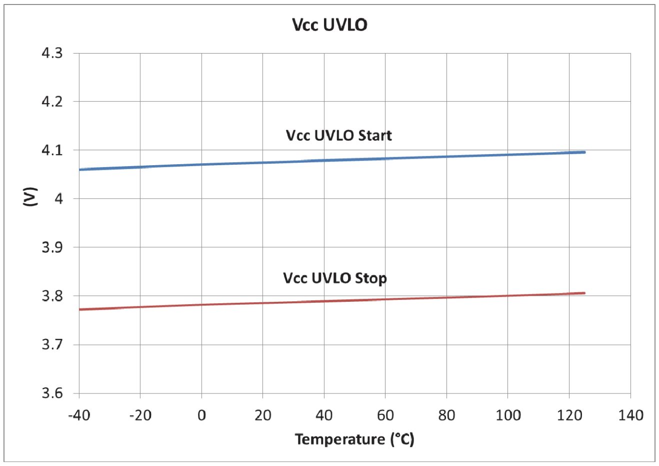


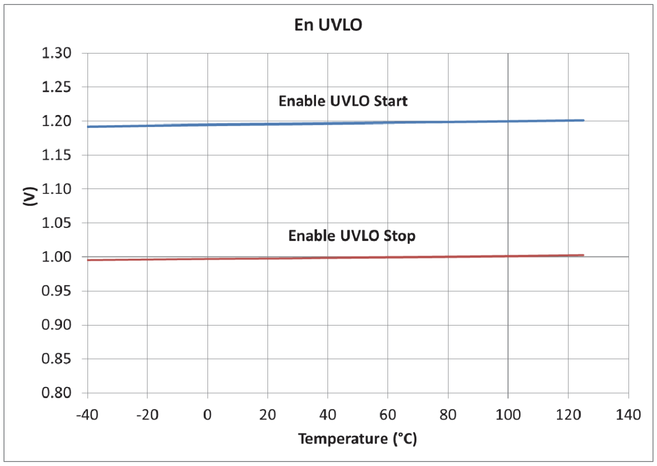
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

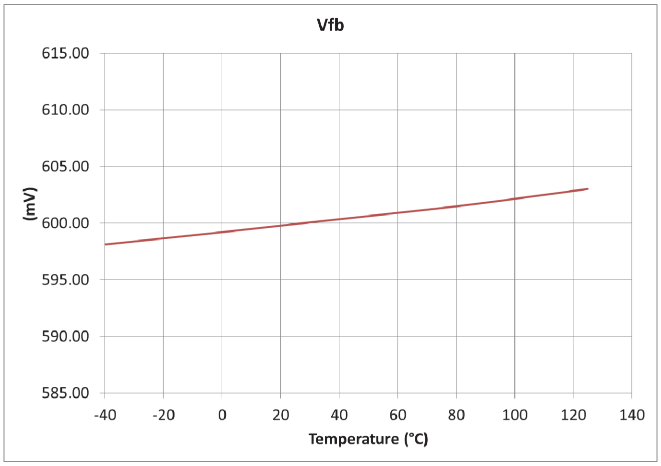




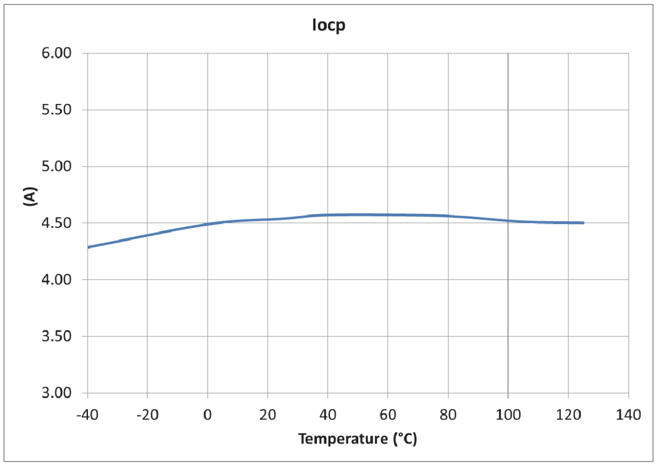


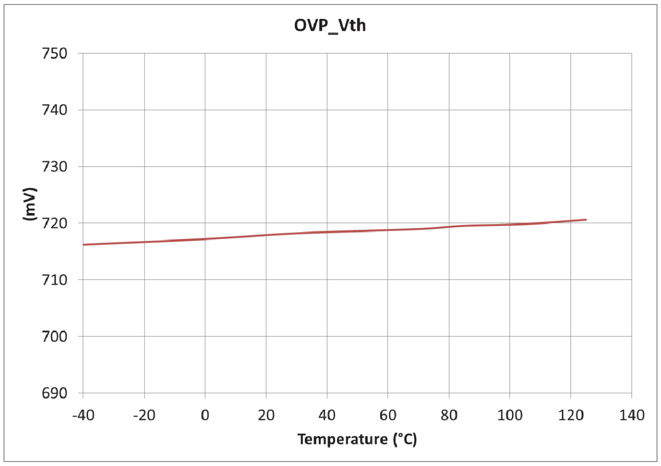


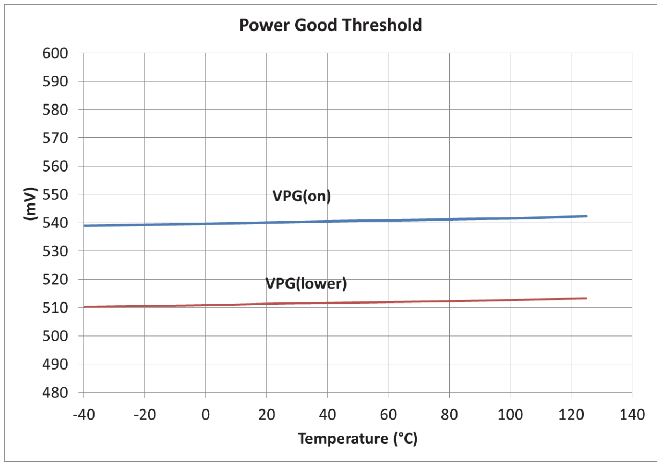


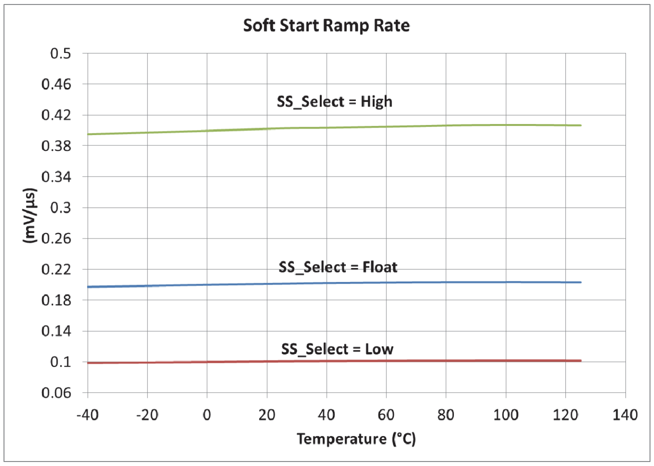


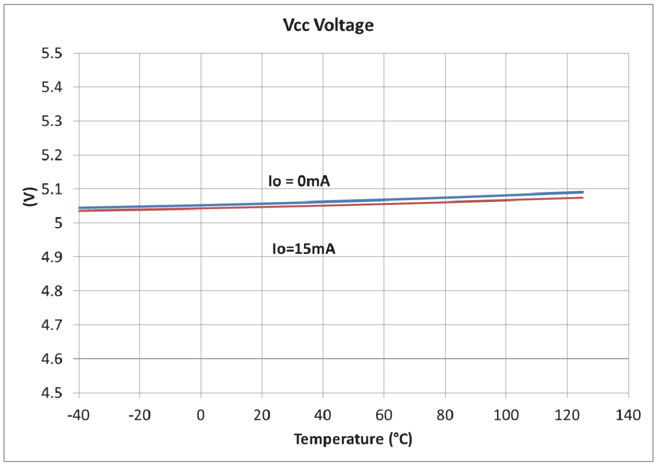
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)











THEORY OF OPERATION

DESCRIPTION

The IR3823 SupIRBuck® is a 3A easy-to-use, fully integrated and highly efficient synchronous Buck regulator intended for Point-Of-Load (POL) applications. It includes two IR HEXFETs with low $R_{DS(on)}$. The bottom FET has an integrated monolithic schottky diode in place of a conventional body diode.

The IR3823 provides precisely regulated output voltage programmed via two external resistors from 0.6V to $0.86 \times V_{in}$. It uses voltage mode control employing a proprietary PWM modulator with input voltage feedforward. That provides excellent noise immunity, easy loop compensation design, and good line transient response.

The IR3823 has an internal Low Dropout (LDO) Regulator, allowing single supply operation without resorting to an external bias supply voltage. To further improve the light load efficiency, the internal LDO can be bypassed by using an external bias supply. This mode allows the input bus voltage range extended down to 1.0V.

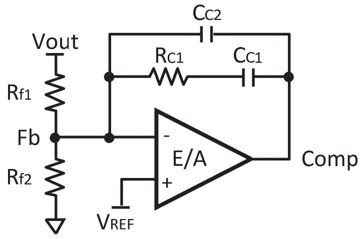
The IR3823 features programmable switching frequency from 300kHz to 1.5MHz, three selectable soft-start time, and smooth synchronization to an external clock. The other important functions include thermally compensated over current protection, output over voltage protection, pre-bias start-up, enable with input voltage monitoring, PGood output and thermal shut-down.

VOLTAGE LOOP COMPESNATION DESIGN

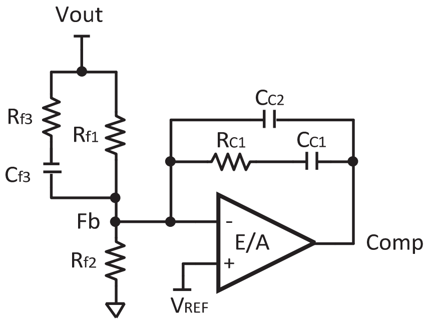
The IR3823 uses PWM voltage mode control. The output voltage of the POL, sensed by a resistor divider, is fed into an internal Error Amplifier (E/A). The output of the E/R is then compared to an internal ramp voltage to determine the pulse width of the gate signal for the control FET. The amplitude of the ramp voltage is proportional to V_{in} so that the bandwidth of the voltage loop remains almost constant for different input voltages. This feature is called input voltage feedfoward. It allows the feedback loop design independent of the input voltage. Please refer to the next section for more information.

A RC network has to be connected between the FB pin and the COMP pin to form a feedback compensator. The goal of the compensator design is to achieve a high control bandwidth with a phase margin of 45° or above. The high control bandwidth is beneficial for the loop dynamic response, which helps to reduce the number of output capacitors, the PCB size and the cost. A phase margin of 45° or higher is desired to ensure the system stability. For most applications, a gain margin of -10dB or higher is preferred to accommodate component variations and to eliminate jittering/noise. The proprietary PWM modulator in IR3823 significantly reduces the PWM jittering, allowing the control bandwidth in the range of 1/10th to 1/5th of the switching frequency.

Two types of compensators are commonly used: Type II (PI) and Type III (PID), as shown in Figure 5. The selection of the compensation type is dependent on the ESR of the output capacitors. Electrolytic capacitors have relatively higher ESR. If the ESR pole is located at the frequency lower than the cross-over frequency, F_C, the ESR pole will help to boost the phase margin. Thus a type II compensator can be used. For the output capacitors with lower ESR such as ceramic capacitors, type III compensation is often desired.



(a)



(b)

Figure 5: Loop Compensator (a) Type II, (b) Type III

Table 1 lists the compensation selection for different types of output capacitors.

For more detailed design guideline of voltage loop compensation, please refer to the application note AN-1162, "*Compensation Design Procedure for Buck Converter with Voltage-Mode Error-Amplifier*". SupBuck design tool is also available at www.irf.com providing the reference design based on user's design requirements.

TABLE 1 RECOMMENDED COMPENSATION TYPE

COMPENSATOR	LOCATION OF CROSS-OVER FREQUENCY	TYPE OF OUTPUT CAPACITORS
Type II (PI)	$F_{LC}<F_{ESR}<F_0<F_S/2$	Electrolytic, POS-CAP, SP-CAP
Type III-A (PID)	$F_{LC}<F_0<F_{ESR}<F_S/2$	POS-CAP, SP-CAP
Type III-B (PID)	$F_{LC}<F_0<F_S/2<F_{ESR}$	Ceramic

F_{LC} is the resonant frequency of the output LC filter. It is often referred to as double pole.

$$F_{LC}=\frac{1}{2\times\pi\sqrt{L_o\times C_o}}$$

F_{ESR} is the ESR zero of the output capacitor.

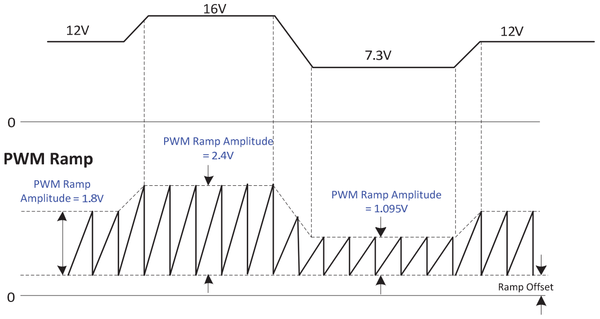
$$F_{ESR}=\frac{1}{2\pi\times ESR\times C_o}$$

F_0 is the cross-over frequency of the closed voltage loop and F_S is the switching frequency.

INPUT VOLTAGE FEEDFORWARD

Input voltage feedforward is an important feature, because it can keep the converter stable and preserve its load transient performance when V_{in} varies in a large range. In IR3823, feedforward function is enabled when V_{in} pin is connected to PV_{in} pin and V_{in}>5.5V. In this case, the internal low dropout (LDO) regulator is used. The PWM ramp amplitude (V_{ramp}) is proportionally changed with V_{in} to maintain the ratio V_{in}/V_{ramp} almost constant throughout V_{in} variation range (as shown in Figure 6). Thus, the control loop bandwidth and phase margin can be maintained constant. Feed-forward function can also minimize impact on output voltage from fast V_{in} change. The maximum V_{in} slew rate is within 1V/µs.

If an external bias voltage is used as V_{cc}, V_{in} pin should be connected to V_{cc}/LDO_out pin instead of PV_{in} pin. Then the feedforward function is disabled. The control loop compensation might need to be adjusted.



16V
12V
12V
7.3V
0
PWM Ramp Amplitude = 2.4V
PWM Ramp
PWM Ramp Amplitude = 1.8V
PWM Ramp Amplitude = 1.095V
Ramp Offset
0

Figure 6: Timing Diagram for Input Feedforward

UNDER-VOLTAGE LOCKOUT AND POR

The Under-Voltage Lockout (UVLO) circuit monitors the voltage of V_{CC}/LDO_Output pin and the Enable pin. It assures that the MOSFET driver outputs remain off whenever either of these two signals is below the set thresholds. Normal operation resumes once both V_{CC}/LDO_Output and En voltages rise above their thresholds.

The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram). When the POR is asserted, the soft start sequence starts (see soft start section).

ENABLE/EXTERNAL PVIN MONITOR

The IR3823 has an Enable function providing another level of flexibility for start-up. The Enable pin has a precise threshold, which is internally monitored by Under-Voltage Lockout (UVLO) circuit. If the voltage at Enable pin is below its UVLO threshold, both high-side and low-side FETs are off. When Enable pin is below its UVLO, Over-Voltage Protection (OVP) is disabled, and PGood stays low.

The Enable pin should not be left floating. A pull-down resistor in the range of several kilo ohms is recommended to connect between the Enable Pin and Gnd.

In addition to logical inputs, the Enable pin can be used to implement precise input voltage UVLO. As shown in Figure 7, the input of the Enable pin is derived from the PV_{in} voltage by a set of resistive divider, R1 and R2. By selecting different divider ratios, users can program the UVLO threshold voltage. The bus voltage UVLO is a very desirable feature. It prevents the IR3823 from regulating at PV_{in} lower than the desired voltage level. Figure 8 shows the start-up waveform with the input UVLO voltage set at 10V.

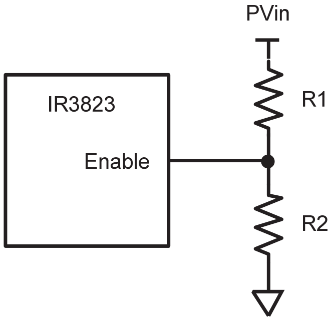


Figure 7: Implementation of Input Under-Voltage Lockout (UVLO) using Enable Pin

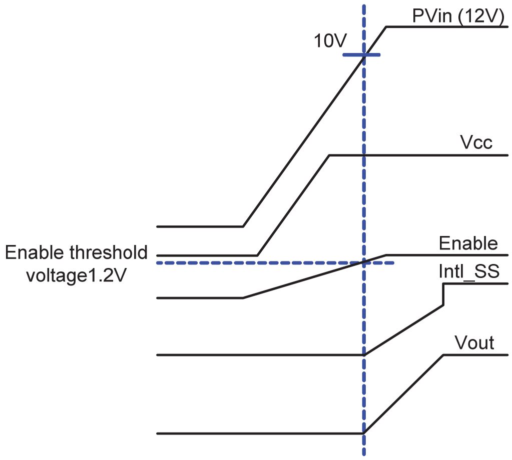


Figure 8: Illustration of start-up with PVin UVLO threshold voltage of 10V. The internal soft-start is used in this case.

INTERNAL LOW DROPOUT REGULATOR

The IR3823 has an internal Low Dropout Regulator (LDO), offering a V_{CC} voltage of 5.1V. The internal LDO is beneficial for single rail (supply) applications, where no external bias supplies will be needed. For these applications, V_{in} pin should be connected to PV_{in} and V_{CC}/LDO_Out pin is left floating as shown in Figure 9. 1.0µF and 2.2µF ceramic bypass capacitors should be placed close to V_{in} pin and V_{CC}/LDO_Out pin respectively.

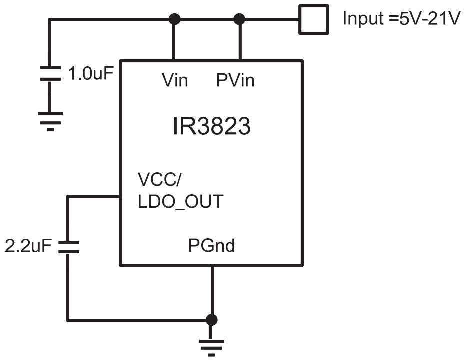


Figure 9: Internally Biased Single-Rail Configuration

When Vin drops below 5.5V, the internal LDO enters the dropout mode. Figure 10 shows the V_{CC}/LDO_Out voltage for V_{in}=PV_{in}=5V with switching frequency of 600kHz and 1500kHz respectively. Alternatively, if the input bus voltage, PV_{in}, is in the range of 4.5V to 7.5V, V_{CC}/LDO_Out pin can be directly connected to PV_{in} pin to bypass the internal LDO and therefore to avoid the voltage drop on the internal LDO. This configuration is illustrated in Figure 11.

Figure 12 shows the configuration using an external V_{CC} voltage. With this configuration, the input voltage range can be extended down to 1.0V. Please note that the input feedforward function is disabled for this configuration. The feedback compensation needs to be adjusted accordingly.

It should be noted as the V_{CC} voltage decreases, the efficiency and the over current limit will decrease due to the increase of $R_{DS(ON)}$. Please refer to the section of the over current protection for more information.

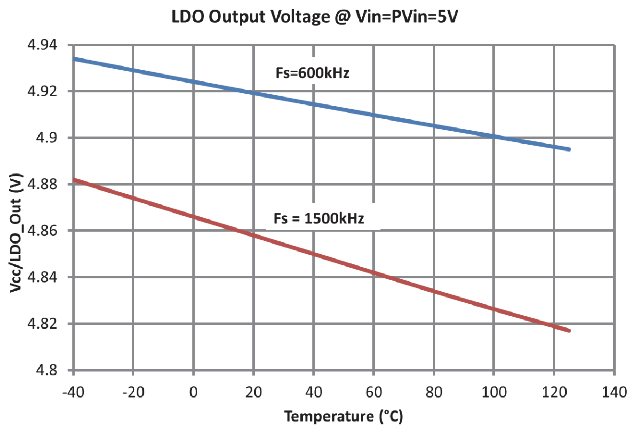


Figure 10: LDO Dropout Voltage at V_{in}=PV_{in}=5V

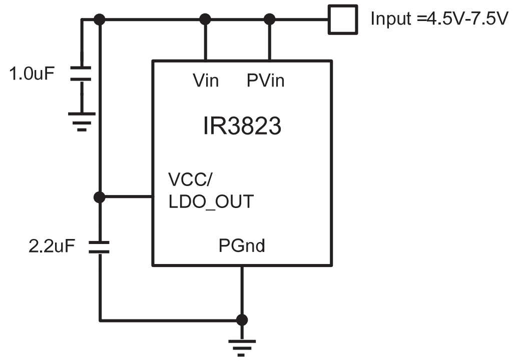

Input =4.5V-7.5V
1.0uF
Vin
PVin
IR3823
VCC/
LDO_OUT
2.2uF
PGnd

Figure 11: Single-Rail Configuration for 4.5V-7V inputs

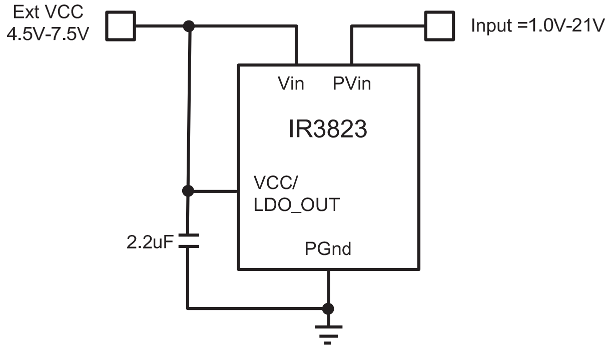

Ext VCC
4.5V-7.5V
Input =1.0V-21V
Vin
PVin
IR3823
VCC/
LDO_OUT
2.2uF
PGnd

Figure 12: Use External Bias Voltage

.

SOFT-START

The IR3823 has an internal digital soft-start circuit to control the output voltage rise time, and to limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and Vcc voltages rise above their UVLO thresholds and generate the Power On Ready (POR) signal. The slew rate of the internal soft-start can be adjusted externally with SS_Select pin, as shown in Table 2.

Table 2 User Selectable Soft-Start Time

SS_Select	Slew Rate (mV/ µs)	Soft-Start Time (ms)
Vcc	0.4	1.5
Float	0.2	3
Gnd	0.1	6

Figure 13 shows the waveforms during soft start. The corresponding soft-start time can be calculated as follows.

$$T_{ss} = \frac{0.75V - 0.15V}{SlewRate}$$

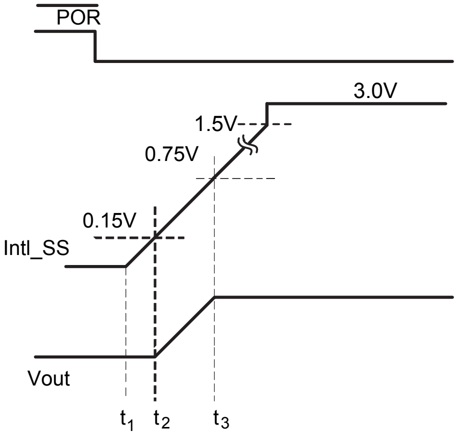

POR
3.0V
1.5V
0.75V
0.15V
Intl_SS
Vout
t_1
t_2
t_3

Figure 13: Theoretical start-up waveforms using internal soft-start

It should be noted that during the soft-start, the over-current protection (OCP) and over-voltage protection (OVP) is enabled to protect the device for any short circuit or over voltage condition.

PRE-BIAS START-UP

IR3823 is able to start up into a pre-charged output smoothly, which prevents oscillations and disturbances of the output voltage.

The output starts in an asynchronous fashion and keeps the synchronous MOSFET (Sync FET) off until the first gate signal for control MOSFET (Ctrl FET) is generated. Figure 14 shows a typical Pre-Bias condition at start up. The gate signal of the control FET is determined by the loop compensator. The sync FET always starts with a narrow pulse width (12.5% of a switching period) and gradually increases its duty cycle with a step of 12.5% until it reaches the steady state value. The number of these startup pulses for each step is 16 and it's internally programmed. Figure 15 shows the series of 16x8 startup pulses.

It should be noted that during pre-bias start up, PGood is not active until the first gate signal for control FET is generated. Please refer to Power Good Section for more information.

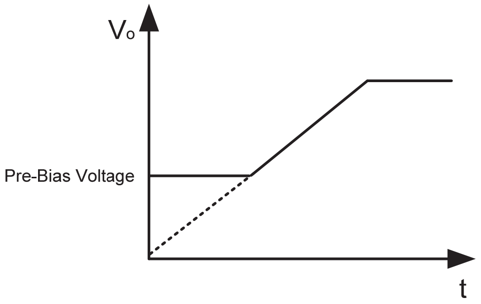


Figure 14: Pre-Bias start-up

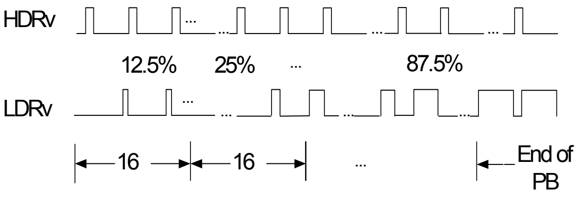


Figure 15: Pre-Bias startup pulses

SHUTDOWN

IR3823 can be shut down by pulling the Enable pin below its 1.0V threshold. Both the high side and the low side drivers will be pulled low.

OPERATING FREQUENCY

The switching frequency can be programmed between 300kHz – 1200kHz by connecting an external resistor from Rt pin to Gnd. Rt can be calculated as follows.

$$F_s = 19954 \times R_t^{-0.953}$$

Where F_S is in kHz, and Rt is in kΩ.

Table 3 shows the different oscillator frequency and its corresponding Rt for easy reference.

Table 3 Switching Frequency vs. R_t

R_t (kΩ)	F_S (kHz)
80.6	300
60.4	400
48.7	500
39.2	600
34	700
29.4	800
26.1	900
23.2	1000
21	1100
19.1	1200
17.4	1300
16.2	1400
15	1500

OVER CURRENT PROTECTION

The over current (OC) protection is performed by sensing current through the $R_{DS(on)}$ of the Synchronous MOSFET. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and any layout related noise issues. The current limit is pre-set internally and is compensated according to the IC temperature. So at different ambient temperature, the over-current trip threshold remains almost constant.

Detailed operation of OCP is explained as follows. Over Current Protection circuit senses the inductor current flowing through the Synchronous MOSFET closer to the valley point. OCP circuit samples this current for 40nsec typically after the rising edge of the PWM set pulse, which has a width of 12.5% of the switching period. The PWM pulse starts at the falling edge of the PWM set pulse. This makes valley current sense more robust as current is sensed close to the bottom of the inductor downward slope where transient and switching noise are lower and helps to prevent false tripping due to noise and transient. An OC condition is detected if the load current exceeds the threshold, the converter enters into hiccup mode. PGood will go low and the internal soft start signal will be pulled low. The converter goes into hiccup mode with some hiccup blanking time as shown in Figure 16. The convertor stays in this mode until the over load or short circuit is removed. With different SS_Select configurations, the hiccup blanking time is different. Please refer to the electrical table for details. The actual DC output current limit point will be greater than the valley point by an amount equal to approximately half of peak to peak inductor ripple current.

$$I_{OCP} = I_{LIMIT} + \frac{\Delta i}{2}$$

I_{OCP}= DC current limit hiccup point
I_{LIMIT}= Over current limit (Valley of Inductor Current)
Δi= Peak-to-peak inductor ripple current

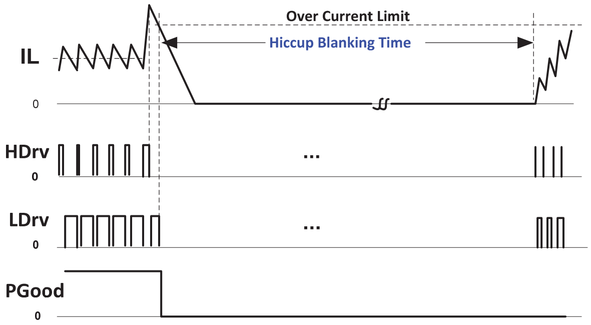


Figure 16: Timing Diagram for Hiccup OCP

Over current limit is affected by the V_{CC} voltage. For some single rail operations where V_{in} is 5V or less, the OCP limit will de-rated due to the drop of V_{CC} voltage. Figure 17 and Figure 18 show the over current limit for two single rail applications with $V_{in}=PV_{in}=5V$ and $V_{in}=PV_{in}=V_{CC}=4.5V$ respectively.

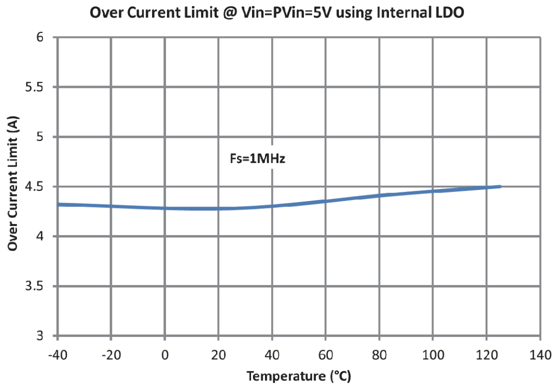


Figure 17:OCP Limit at $V_{in}=PV_{in}=5V$ using Internal LDO

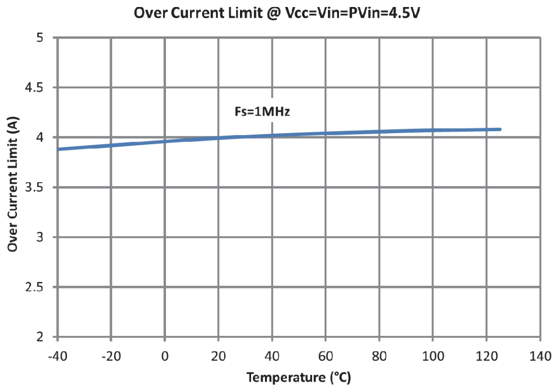


Figure 18: OCP Limit at $V_{in}=PV_{in}=V_{CC}=4.5V$

OVER-VOLTAGE PROTECTION (OVP)

Over-voltage protection in IR3823 is achieved by comparing FB pin voltage to a pre-set threshold. OVP threshold is set at 1.2×Vref. When FB pin voltage exceeds the over voltage threshold, an over voltage trip signal asserts after 2us (typ.) delay. Then the high side drive signal HDrv is turned off immediately, PGood flags low. The sync FET remains on to discharge the output capacitor. When the V_{FB} voltage drops below the threshold, the sync FET turns off to prevent the complete depletion of the output capacitor. After that, HDrv remains off until a reset is performed by cycling either V_{cc} or Enable. Figure 19 shows the timing diagram for over voltage protection. Please note that OVP comparator becomes active only when the IR3823 is enabled.

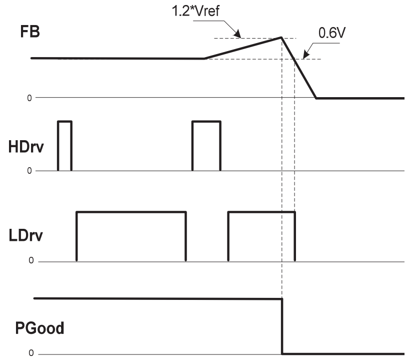


Figure 19: Timing Diagram for Over Voltage Protection

POWER GOOD OUTPUT

IR3823 continually monitors the output voltage via FB voltage. The FB voltage is an input to the window comparator with upper and lower threshold of 120% and 85% of the reference voltage respectively. PGood signal is high whenever FB voltage is within the PGood comparator window thresholds. For pre-biased start-up, PGood is not active until the first gate signal of the control FET is generated.

The PGood pin is open drain and it needs to be externally pulled high. High state indicates that output is in regulation.

In addition, PGood is also gated by other faults including over current and over temperature. When either of the faults occurs, PGood pin will be pulled low.

THERMAL SHUTDOWN

Temperature sensing is provided inside IR3823. The trip threshold is typically set to 145ºC. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs and resets the internal soft start.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the thermal shutdown threshold.

EXTERNAL SYNCHRONIZATION

IR3823 incorporates an internal phase lock loop (PLL) circuit which enables synchronization of the internal oscillator to an external clock. This function is important to avoid sub-harmonic oscillations due to beat frequency for embedded systems when multiple point-of-load (POL) regulators are used. A multi-function pin, Rt/Sync, is used to connect the external clock. If the external clock is present before the converter turns on, Rt/Sync pin can be connected to the external clock signal solely and no other resistor is needed. If the external clock is applied after the converter turns on, or the converter switching frequency needs to toggle between the external clock frequency and the internal free-running frequency, an external resistor from Rt/Sync pin to Gnd is required to set the free-running frequency.

When an external clock is applied to Rt/Sync pin after the converter runs in steady state with its free-running frequency, a transition from the free-running frequency to the external clock frequency will happen. This transition is to gradually make the actual switching frequency equal to the external clock frequency, no matter which one is higher. On the contrary, when the external clock signal is removed from Rt/Sync pin, the switching frequency is also changed to free-running gradually. In order to minimize the impact from these transitions to output voltage, a diode is recommended to add between the external clock and Rt/Sync pin, as shown in Figure 20. Figure 21 shows the timing diagram of these transitions.

An internal compensation circuit is used to change the PWM ramp slope according to the clock frequency applied on Rt/Sync pin. Thus, the effective amplitude of the PWM ramp (V_{ramp}), which is used in compensation loop calculation, has minor impact from the variation of the external synchronization signal.

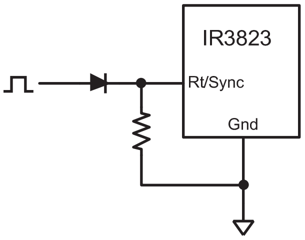


Figure 20: Configuration of External Synchronization

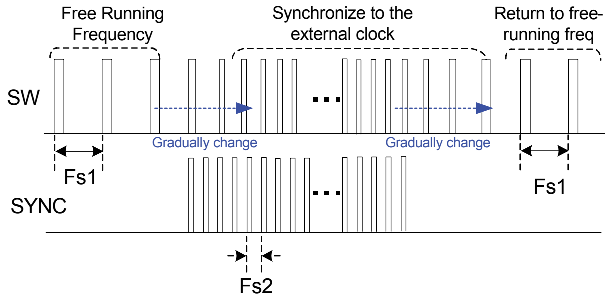


Figure 21: Timing Diagram for Synchronization to the External Clock (Fs1<Fs2 or Fs1>Fs2)

MINIMUM ON TIME CONSIDERATIONS

The minimum ON time is the shortest amount of time for which Ctrl FET may be reliably turned on, and this depends on the internal timing delays. For IR3823, the worst case minimum on-time is specified as 60ns.

Any design or application using IR3823 must ensure operation with a pulse width that is higher than this minimum on-time and preferably higher than 60ns. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{V_{in} \times F_s}$$

In any application that uses IR3823, the following condition must be satisfied:

$$t_{on(\min)} \le t_{on}$$

$$t_{on(\min)} \le \frac{V_{out}}{V_{in} \times F_s} \text{, therefore, } V_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}}$$

The minimum output voltage is limited by the reference voltage and hence $V_{out(min)}$ = 0.6V. Therefore,

$$V_{in} \times F_s \le \frac{V_{out(\min)}}{t_{on(\min)}} = \frac{0.6\text{V}}{60\text{ns}} = 10V/\mu s$$

Therefore, at the maximum recommended input voltage 21V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 476 kHz. Conversely, for operation at the maximum recommended operating frequency (1.65 MHz) and minimum output voltage (0.6V). The input voltage (PV_{in}) should not exceed 6V, otherwise pulse skipping will happen.

MAXIMUM DUTY RATIO

A certain off-time is specified for IR3823. This provides an upper limit on the operating duty ratio at any given switching frequency. The off-time remains at a relatively fixed ratio to switching period in low and mid frequency range, while in high frequency range this ratio increases, thus the lower the maximum duty ratio at which IR3823 can operate. Figure 22 shows a plot of the maximum duty ratio vs. the switching frequency.

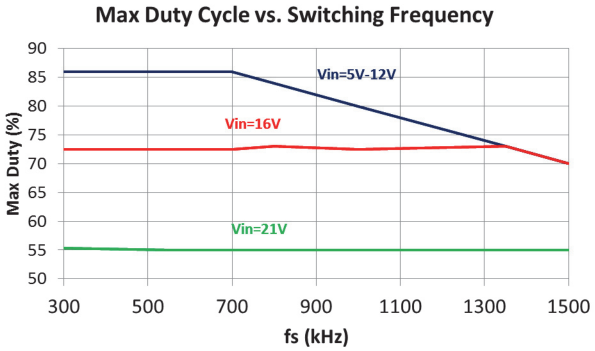


Figure 22: Maximum duty cycle vs. switching frequency.

DESIGN EXAMPLE

The following example is a typical application for IR3823. The application circuit is shown in Figure 26.

$PV_{in} = V_{in} = 12V\ (\pm 10\%)$

$V_o = 1.2V$

$I_o = 3A$

Peak-to-Peak Ripple Voltage = ±1% of V_o

$\Delta V_o = \pm\ 4\%$ of V_o (for 30% Load Transient)

$F_s = 1MHz$

EXTERNAL PVIN MONITOR (INPUT UVLO)

As explained in the section of Enable/External PV_{in} monitor, the input voltage, PV_{in}, can be monitored by connecting the Enable pin to PV_{in} through a set of resistor divider. When PV_{in} exceeds the desired voltage level such that the voltage at the Enable pin exceeds the Enable threshold, 1.2V, the IR3823 is turned on. The implementation of this function is shown in Figure 7.

For a typical Enable threshold of V_{EN} = 1.2 V

$$PV_{in(\min)} \times \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2$$

$$R_2 = R_1 \times \frac{V_{EN}}{PV_{in(\min)} - V_{EN}}$$

For the minimum input voltage $PV_{in\ (min)}$ = 9.2V, select R_1=49.9kΩ, and R_2=7.5kΩ.

SWITCHING FREQUENCY

For F_S = 1MHz, select Rt = 23.2 kΩ, from Table 3.

OUTPUT VOLTAGE SETTING

Output voltage is set by the reference voltage and the external voltage divider connected to the FB pin. The FB pin is the inverting input of the error amplifier, which is internally referenced to 0.6V. The divider ratio is set to provide 0.6V at the FB pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_{REF} \times (1 + \frac{R_{F1}}{R_{F2}})$$

R_{F1} and R_{F2} are the feedback resistor divider, as shown in Figure 23. For the selection of R_{F1} and R_{F2}, please see feedback compensation section.

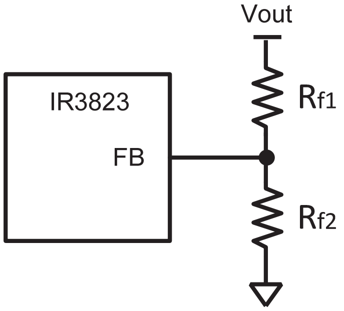


Figure 23: The output voltage is programmed through a set of feedback resistor divider

BOOTSTRAP CAPACITOR SELECTION

To drive the Control FET, it is necessary to supply a gate voltage at least 4V greater than the voltage at the SW pin, which is connected to the source of the Control FET. This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor, C1, as shown in Figure 24. The operation of the circuit is as follows: When the sync FET is turned on, the capacitor node connected to SW is pulled low. V_{CC} starts to charge C1 through the internal bootstrap didoe. The voltage, V_c, across the bootstrap capacitor C1 can be calculated as

$$V_C = V_{CC} - V_D$$

where V_D is the forward voltage drop of the bootstrap diode.

When the control FET turns on in the next cycle, the SW node voltage rises to the bus voltage, PV_{in}. The voltage at the Boot pin becomes:

$$V_{BOOT} = PV_{in} + V_{CC} - V_D$$

A good quality ceramic capacitor of 0.1µF with voltage rating of at least 25V is recommended for most applications.

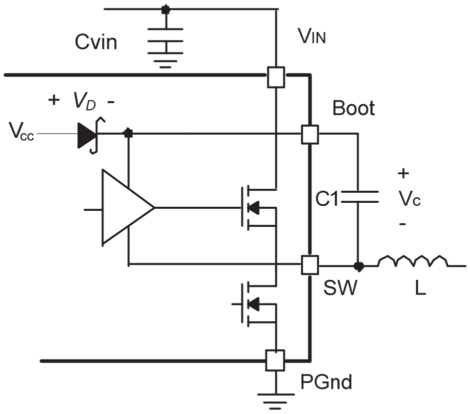


Figure 24: Bootstrap circuit to generate the supply voltage for the high-side driver voltage

INPUT CAPACITOR SELECTION

Good quality input capacitors are necessary to minimize the input ripple voltage and to supply the switch current during the on-time. The input capacitors should be selected based on the RMS value of the input ripple current and requirement of the input ripple voltage.

The RMS value of the input ripple current can be calculated as follows:

$$I_{RMS} = I_o \times \sqrt{D \times (1 - D)}$$

Where D is the duty cycle and I_o is the output current. For I_o=6A and D=0.1, I_{RMS}= 0.9A

The input voltage ripple is the result of the charging of the input capacitors and the voltage induced by ESR and ESL of the input capacitors.

Ceramic capacitors are recommended due to their high ripple current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency.

For this application, it is suggested to use two 10µF/25V ceramic capacitors, C3216X5R1E106M, from TDK. In addition, although not mandatory, a 1x100uF, 25V SMD capacitor EEE-1EA101XP from Panasonic may also be used as a bulk capacitor and is recommended if the input power supply is not located close to the converter.

INDUCTOR SELECTION

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor (Δi). The optimum point is usually found between 20% and 50% ripple of the output current.

The saturation current of the inductor is desired to be higher than the over current limit plus the inductor ripple current. An inductor with soft-saturation characteristic is recommended.

For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$PV_{in\max} - V_o = L \times \frac{\Delta i_{L\max}}{\Delta t}; \ \Delta t = \frac{D}{F_s}$$

$$L = (PV_{in\max} - V_o) \times \frac{V_o}{V_{in} \times \Delta i_{L\max} \times F_s}$$

Where:

PV_{inmax} = Maximum input voltage
V_0 = Output Voltage
Δi_{Lmax} = Maximum Inductor Peak-to-Peak Ripple Current
F_s = Switching Frequency
Δt = On time
D = Duty Cycle

Select $\Delta i_{Lmax} \approx 36\% \times I_o$, then the output inductor is calculated to be 1.0µH. Select L=1.0µH, XFL4020-102ME, from Coilcraft which provides a compact, low profile inductor suitable for this application.

OUTPUT CAPACITOR SELECTION

Output capacitors are usually selected to meet two specific requirements: (1) Output ripple voltage and

(2) load transient response. The load transient response is also greatly affected by the control bandwidth. So it is common practice to select the output capacitors to meet the requirements of the output ripple voltage first, and then design the control bandwidth to meet the transient load response. For some cases, even with the highest allowable control bandwidth, the resulting load transient response still cannot meet the requirement. The number of output capacitors then need to be increased.

The voltage ripple is attributed by the ripple current charging the output capacitors, and the voltage drop due to the Equivalent Series Resistance (ESR) and the Equivalent Series Inductance (ESL). Following lists the respective peak-to-peak ripple voltages:

$$\Delta V_{o(C)} = \frac{\Delta i_{L\max}}{8 \times C_o \times F_s}$$

$$\Delta V_{o(ESR)} = \Delta i_{L\max} \times ESR$$

$$\Delta V_{o(ESL)} = \left(\frac{PV_{in} - V_o}{L}\right) \times ESL$$

Where $\Delta i_{L\max}$ is maximum inductor peak-to-peak ripple current.

Good quality ceramic capacitors are recommended due to their low ESR, ESL and the small package size. It should be noted that the capacitance of ceramic capacitors are usually de-rated with the DC and AC biased voltage. It is important to use the de-rated capacitance value for the calculation of output ripple voltage as well as the voltage loop compensation design. The de-rated capacitance value may be obtained from the manufacturer's datasheets.

In this case, one 22uF ceramic capacitors, C2012X5R0J226M, from TDK are used to achieve ±12mV peak-to-peak ripple voltage requirement. The de-rated capacitance value with 1.2VDC bias and 10mVAC voltage is around 18uF each.

FEEDBACK COMPENSATION

For this design, the resonant frequency of the output LC filter, F_{LC}, is

$$\begin{aligned} F_{LC} &= \frac{1}{2 \times \pi \sqrt{L_o \times C_o}} \\ &= \frac{1}{2 \times \pi \sqrt{1.0 \times 10^{-6} \times 1 \times 18 \times 10^{-6}}} \\ &= 37.5\text{kHz} \end{aligned}$$

The equivalent ESR zero of the output capacitors, F_{ESR}, is.

$$\begin{aligned} F_{ESR} &= \frac{1}{2\pi \times ESR \times 1 \times C_o} \\ &= \frac{1}{2\pi \times 3 \times 10^{-3} \times 18 \times 10^{-6}} \\ &= 2.9 \times 10^3 \text{kHz} \end{aligned}$$

Designing crossover frequency at 1/5th of switching frequency gives F_0=200 kHz.

According to Table 1, Type III B compensation is selected for $F_{LC}<F_0<F_S/2<F_{ESR}$. Type III compensator is shown below for easy reference.

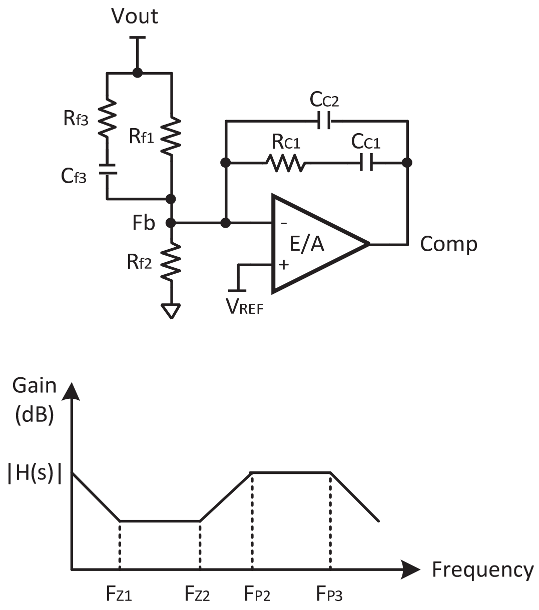


Figure 25: Type III compensation and its asymptotic gain plot

As can be seen from Figure 25, Type III compensator contains two zeros and three poles. They can be calculated as follows.

The zeros are:

$$F_{Z1} = \frac{1}{2\pi \times R_{C1} \times C_{C1}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{F3} \times (R_{F3} + R_{F1})}$$

The poles are:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_{F3} \times C_{F3}}$$

$$F_{P3} = \frac{1}{2\pi \times R_{C1} \times C_{C2}}$$

Please note that the order of the zeros and poles do not necessarily follow the location shown in Figure 25. It can vary with the design preference.

To archive the sufficient phase boost near the cross-over frequency, it is desired to place one zero and one pole as follows:

$$F_Z = F_0\sqrt{\frac{1-\sin\theta}{1+\sin\theta}} = 200\times 10^3\sqrt{\frac{1-\sin 70}{1+\sin 70}} = 35\text{kHz}$$

$$F_P = F_0\sqrt{\frac{1+\sin\theta}{1-\sin\theta}} = 200\times 10^3\sqrt{\frac{1+\sin 70}{1-\sin 70}} = 1134\text{kHz}$$

To compensate the phase lag of the pole at the origin and to provide extra phase boost, the other zero can be placed at one half of the first zero, i.e. $1/F_Z$ = 17.5 kHz.

The third pole is usually placed at one half of the switching frequency to damp the switching noise.

The selected compensation parameters are: R_{F1}=4.02kΩ, R_{F2}=4.02kΩ, R_{F3}=127Ω, C_{F3}=2200pF, R_{C1}=1.0kΩ, C_{C1}=4.7nF, C_{C2}=56pF. The resulting zeros and poles are listed in Table 4. Please note that one of high-frequency poles has been moved to 2843 kHz to increase the phase margin.

Table 4 Zeros and Poles of the Voltage Loop Compensator

Zeros		Poles		
34 kHz	17 kHz	0	570 kHz	2843 kHz

APPLICATION DIAGRAM

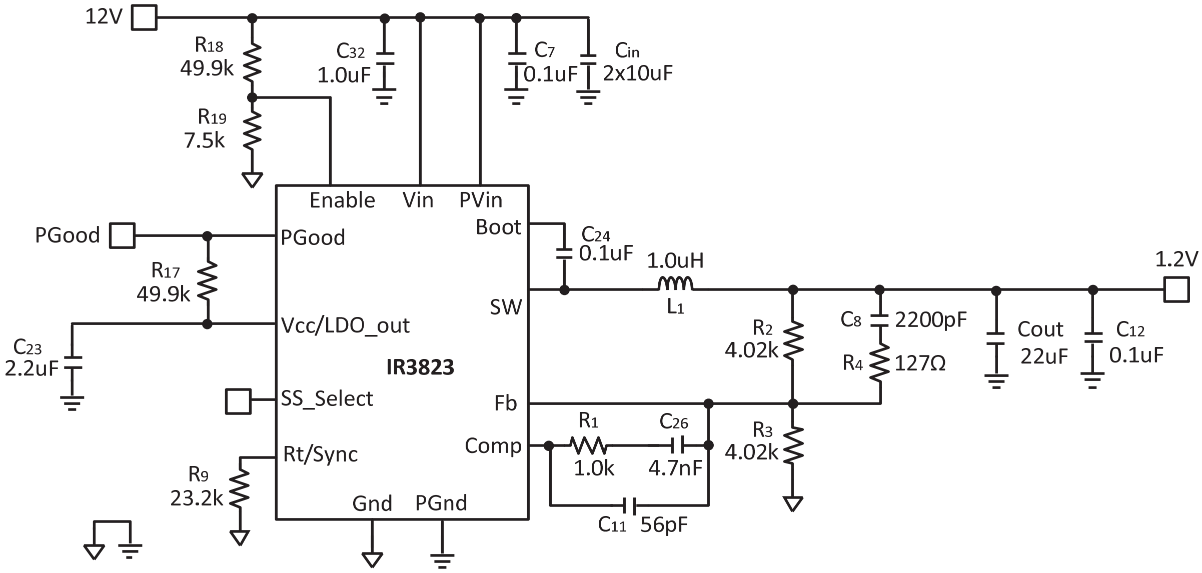

12V
R18
49.9k
R19
7.5k
C32
1.0uF
C7
0.1uF
Cin
2x10uF
Enable
Vin
PVin
Boot
PGood
PGood
R17
49.9k
C23
2.2uF
Vcc/LDO_out
IR3823
SS_Select
Rt/Sync
R9
23.2k
Gnd
PGnd
C24
0.1uF
1.0uH
L1
SW
1.2V
R2
4.02k
C8
2200pF
R4
127Ω
Cout
22uF
C12
0.1uF
Fb
Comp
R1
1.0k
C26
4.7nF
R3
4.02k
C11
56pF

Figure 26: Single Rail 3A POL Application Circuit: PV$_{in}$=V$_{in}$=12V, V$_{o}$=1.2V, Io=3A, f$_{sw}$=1MHz

SUGGESTED BILL OF MATERIALS

QTY	PART REFERENCE	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER
2	C$_{in}$	10uF	1206, 25V, X5R, 20%	TDK	C3216X5R1E106M
3	C7, C12, C24	0.1uF	0603, 25V, X7R, 10%	Murata	GRM188R71E104KA01B
1	C11	56pF	0603, 50V, NP0, 5%	TDK	C1608C0G1H560J080AA
1	C$_{out}$	22uF	0805, 6.3V, X5R, 20%	TDK	C2012X5R0J226M
1	C8	2200pF	0603,50V,X7R	Murata	GRM188R71H222KA01B
1	C23	2.2uF	0603, 16V, X5R, 20%	TDK	C1608X5R1C225M
1	C26	4700pF	0603, 50V 10% X7R	Murata	GRM188R71H472KA01D
1	C32	1.0uF	0603, 25V, X5R, 10%	Murata	GRM188R61E105KA12D
1	R1	1.0k	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF1001V
2	R2, R3	4.02k	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF4021V
1	R4	127	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF1270V
1	R9	23.2k	Thick Film, 0603,1/10W	Panasonic	ERJ-3EKF2322V
2	R17, R18	49.9k	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF4992V
1	R19	7.5k	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF7501V
1	L	1.0uH	SMD, 4.0mmx4.0mmx2.1mm, 10.8mΩ	Coilcraft	XFL4020-102ME
1	U1	IR3823	3A POL, PQFN 3.5mm x3.5mm	IR	IR3823

APPLICATION DIAGRAM

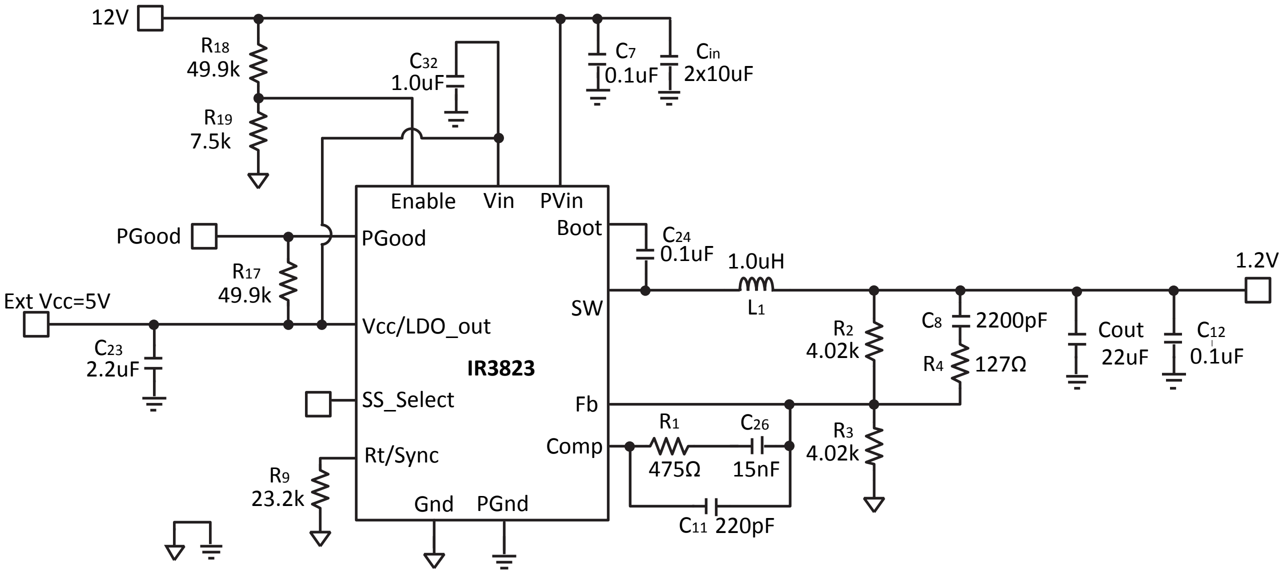

12V
R18
49.9k
R19
7.5k
C32
1.0uF
C7
0.1uF
Cin
2x10uF
Enable
Vin
PVin
PGood
Boot
C24
0.1uF
1.0uH
L1
1.2V
R17
49.9k
Ext Vcc=5V
Vcc/LDO_out
SW
R2
4.02k
C8
2200pF
R4
127Ω
Cout
22uF
C12
0.1uF
C23
2.2uF
IR3823
SS_Select
Fb
R1
475Ω
C26
15nF
R3
4.02k
Rt/Sync
Comp
R9
23.2k
Gnd
PGnd
C11 220pF

Figure 27: 3A POL Application Circuit with external 5V V_{CC}: $PV_{in}=V_{in}=12V$, $V_o=1.2V$, Io=3A, $f_{sw}=1MHz$. Please note that loop compensation is adjusted to consider the absence of the input voltage feedforward.

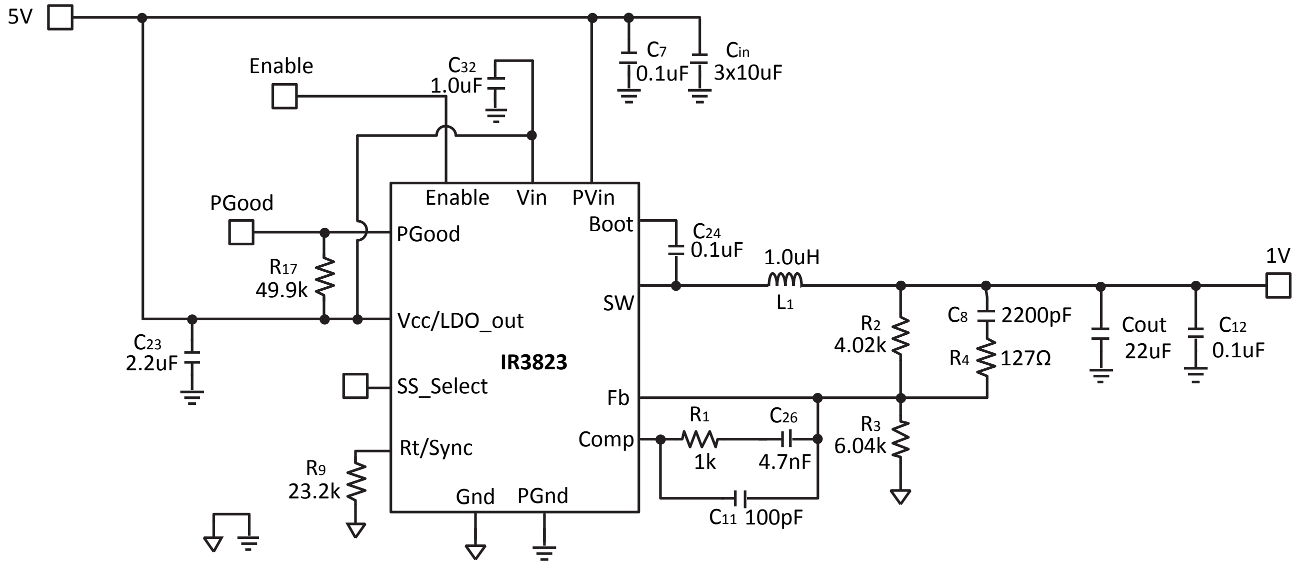
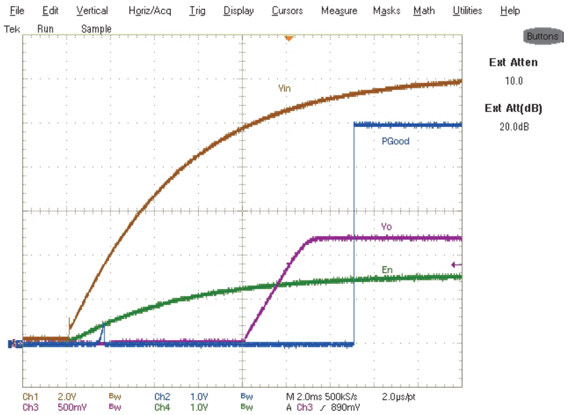

5V
Enable
C32
1.0uF
C7
0.1uF
Cin
3x10uF
Enable
Vin
PVin
PGood
PGood
Boot
C24
0.1uF
1.0uH
L1
1V
R17
49.9k
Vcc/LDO_out
SW
R2
4.02k
C8
2200pF
R4
127Ω
Cout
22uF
C12
0.1uF
C23
2.2uF
IR3823
SS_Select
Fb
R1
1k
C26
4.7nF
R3
6.04k
Rt/Sync
Comp
R9
23.2k
Gnd
PGnd
C11 100pF

Figure 28: Single Rail 3A POL Application Circuit: $PV_{in}=V_{in}=5V$, $V_o=1.0V$, Io=3A, $f_{sw}=1MHz$

TYPICAL OPERATING WAVEFORMS

V_{in} = 12V, V_0 = 1.2V, I_0 = 0-3A, Unless otherwise Specified, SS_Select = Float. Room Temperature, No Air Flow



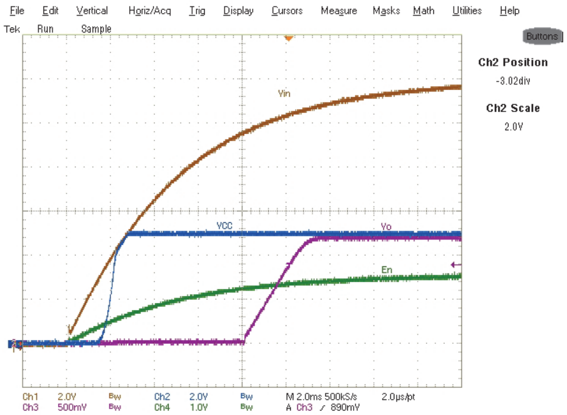
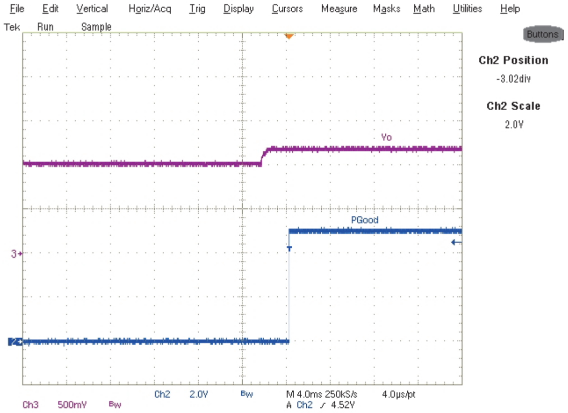


Figure 29: Start up at 3A Load with SS_Select pin floating. Ch_1:V_{in}, Ch_2: P_{Good}, Ch_3:V_o ,Ch_4: Enable

Figure 30: Start up at 3A Load with SS_Select pin floating. Ch_1:V_{in}, Ch_2: V_{cc}, Ch_3:V_o ,Ch_4: Enable



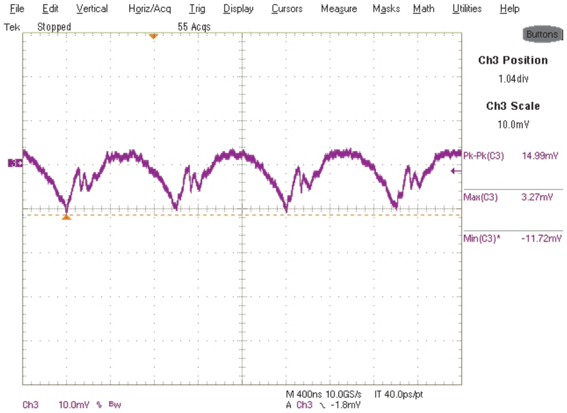
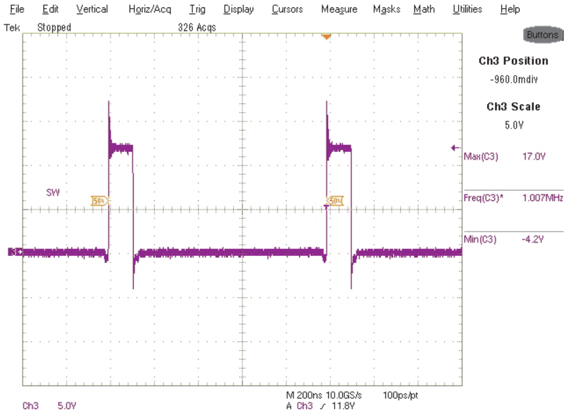


Figure 31: Start up with 1.06V Pre Bias, 0A Load Ch_3:V_o, Ch_2:P_{Good}

Figure 32: Output Voltage Ripple, 3A load Ch_3: V_{out}



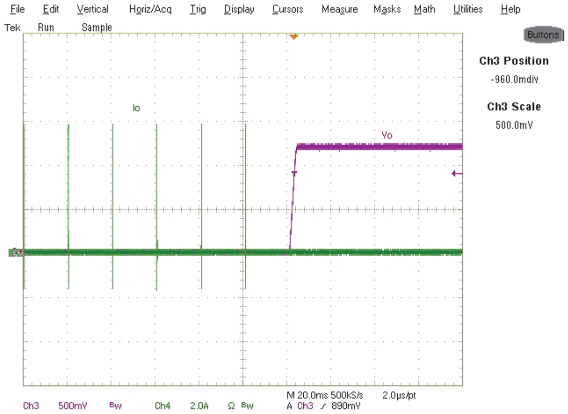
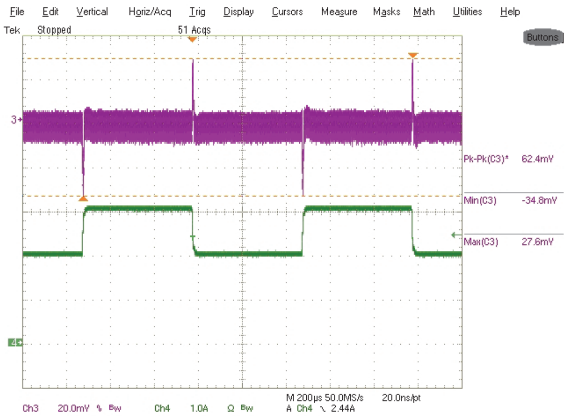


Figure 33: Inductor node at 3A load, Ch3: SW node

Figure 34: Short circuit (Hiccup) Recovery, Ch3:Vout , Ch4:Iout

TYPICAL OPERATING WAVEFORMS

V_{in} = 12V, V_0 = 1.2V, I_0 = 0-3A, Unless otherwise Specified, SS_Select = Float. Room Temperature, No Air Flow


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Masks Math Utilities Help
Tek Stopped
51 Acqs
Buttons
3
4
Pk-Pk(C3)* 62.4mV
Min(C3) -34.8mV
Max(C3) 27.6mV
Ch3 20.0mV Bw
Ch4 1.0A Ω Bw
M 200µs 50.0MS/s 20.0ns/pt
A Ch4 \ 2.44A

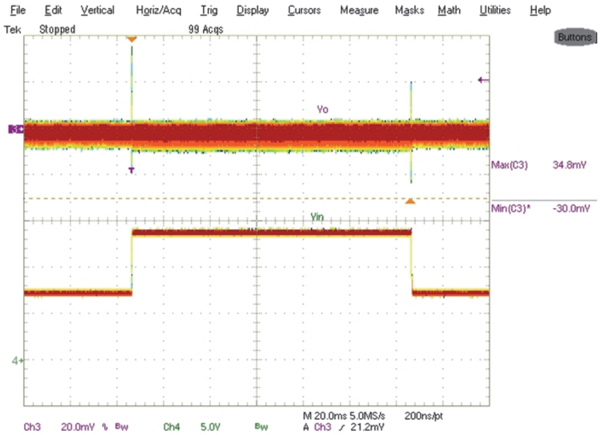
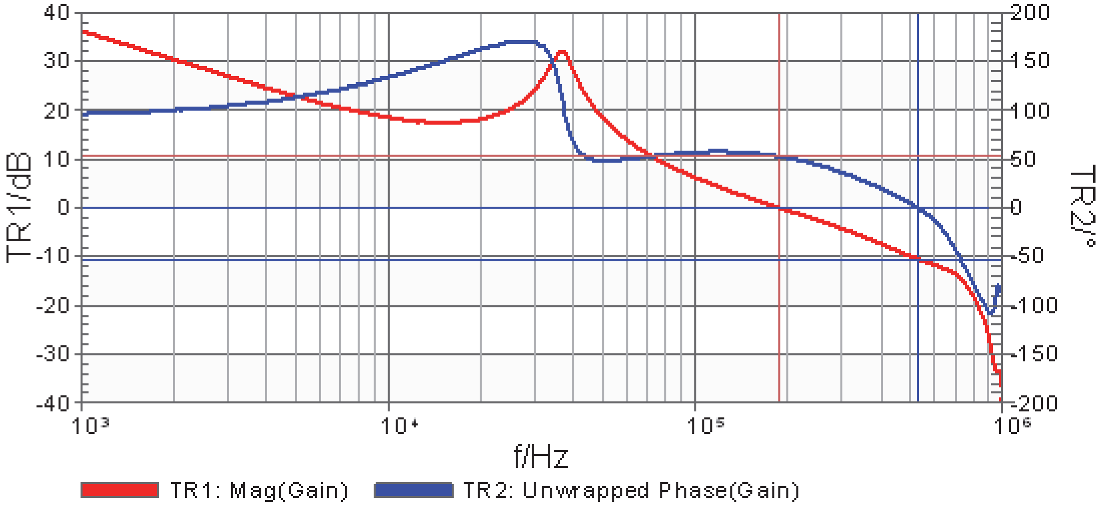

File Edit Vertical Horiz/Acq Trig Display Cursors Measure Masks Math Utilities Help
Tek Stopped
99 Acqs
Buttons
Vo
Vin
3
4
Max(C3) 34.8mV
Min(C3)* -30.0mV
Ch3 20.0mV Bw
Ch4 5.0V Bw
M 20.0ms 5.0MS/s 200ns/pt
A Ch3 / 21.2mV

Figure 35: Transient Response, 2A to 3A Step load Ch3:V_{out} Ch4-I_{out}

Figure 36: Feed Forward for V_{in} change from 7 to 14V and back to 7V. Ch3-V_{out}, Ch4-V_{in}



	Frequency	Trace1	Trace2
Cursor 1	188.366 kHz	0.000 dB	52.895 °
Cursor 2	528.174 kHz	-10.478 dB	-227.374 °

Figure 37: Bode Plot at 6A load, bandwidth = 188 kHz, and phase margin = 53 degrees and gain margin = -10dB

TYPICAL OPERATING WAVEFORMS

V_{in} = 12V, V_0 = 1.2V, I_0 = 0-3A, Unless otherwise Specified, SS_Select = Float. Room Temperature, No Air Flow

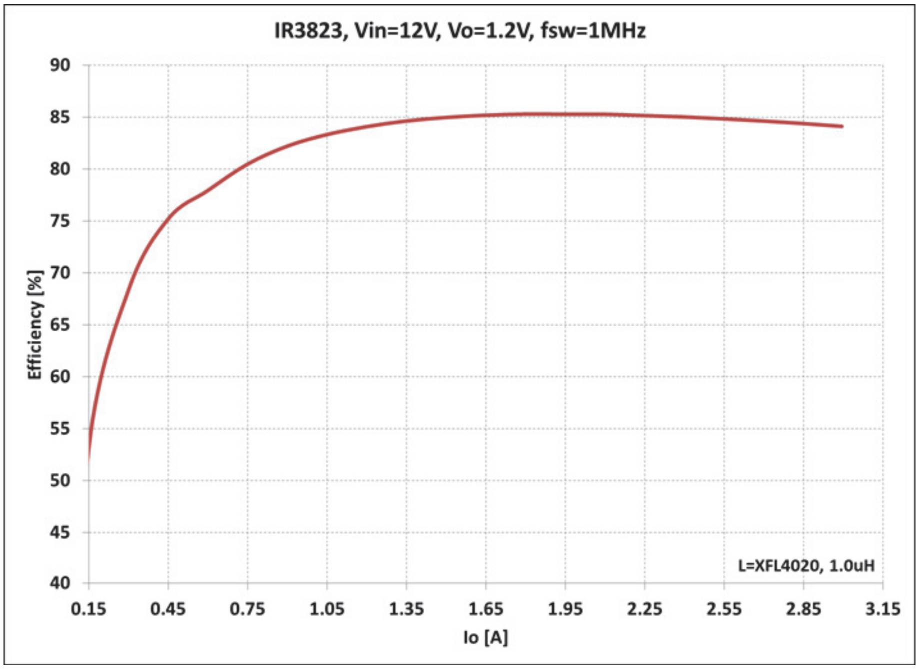


Figure 38: Efficiency vs. Load Current

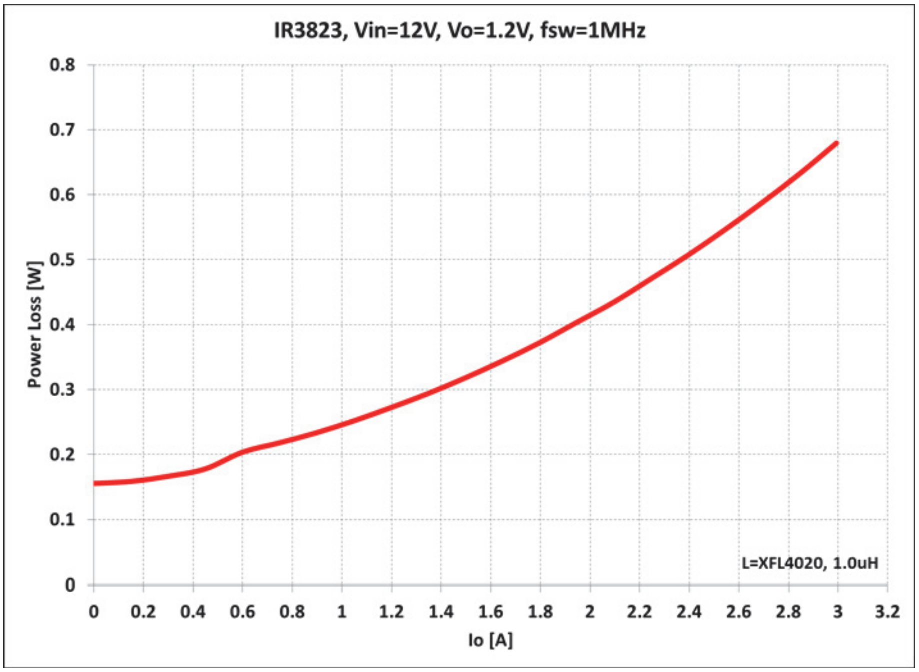


Figure 39: Power Loss vs. Load Current

TYPICAL OPERATING WAVEFORMS

V_{in} = 12V, V_0 = 1.2V, I_0 = 0-3A, Unless otherwise Specified, SS_Select = Float. Room Temperature, No Air Flow

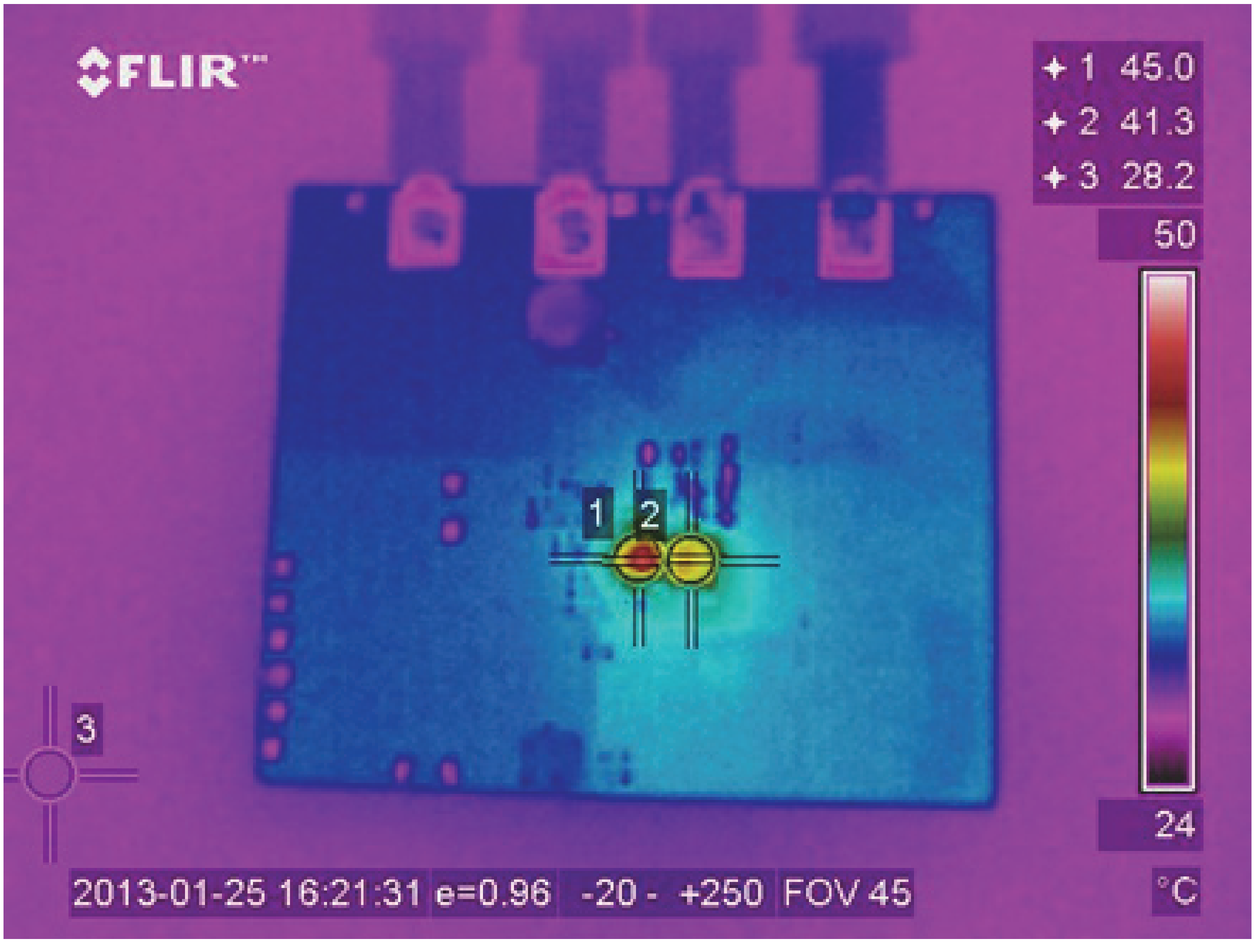

FLIR
1 45.0
2 41.3
3 28.2
50
24
°C
1
2
3
2013-01-25 16:21:31 e=0.96 -20 - +250 FOV 45

Figure 40: Thermal Image of the board at 3A load, IR3823=45°C, Inductor=41.3°C

LAYOUT RECOMMENDATIONS

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with worse than expected results.

Make the connections for the power components in the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

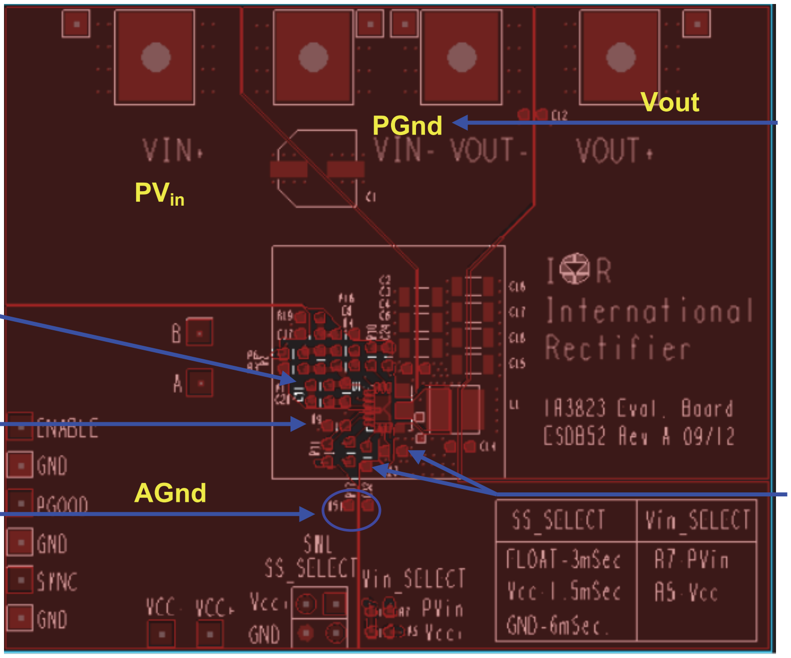
The inductor, output capacitors and the IR3823 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the PV_{in} pin of IR3823.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for V_{in} and V_{CC} should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

In a multilayer PCB use one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point. It is recommended to place all the compensation parts over the analog ground plane in top layer.

The Power QFN is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 4-layers PCB. To effectively remove heat from the device the exposed pad should be connected to the ground plane using via holes. Figure 41-Figure 44 illustrates the implementation of the layout guidelines outlined above, on the IRDC3823 4-layer demo board.



Allow enough copper & minimum ground length path between Input and Output

Compensation parts should be placed as close as possible to the Comp pin

SW node copper is kept only at the top layer to minimize the switching noise

Resistor Rt should be placed as close as possible to their pins

All bypass caps should be placed as close as possible to their connecting pins

Single point connection between AGND & PGND, should be close to the SupIRBuck and kept away from noise

Figure 41: IRDC3823 Demo Board – Top Layer

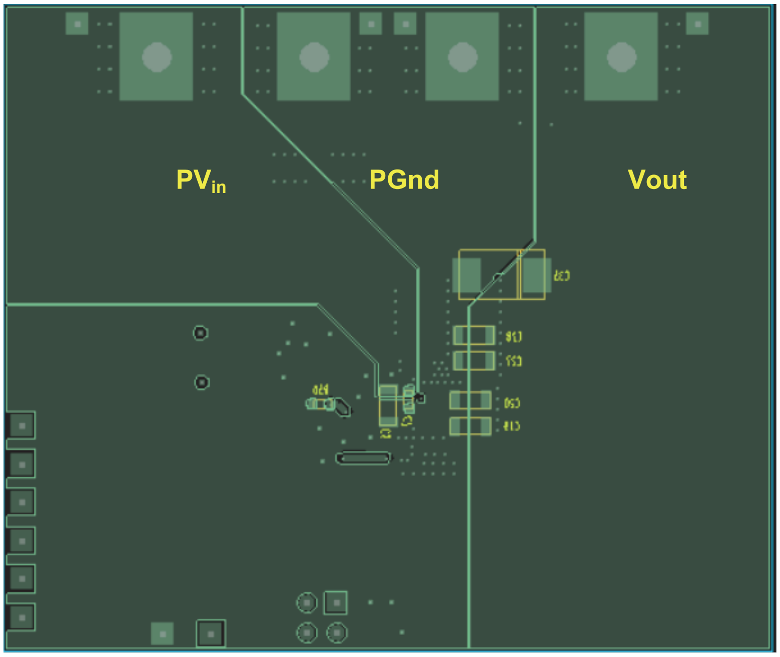

PV$_{in}$
PGnd
Vout

Figure 42: IRDC3823 Demo Board – Bottom Layer

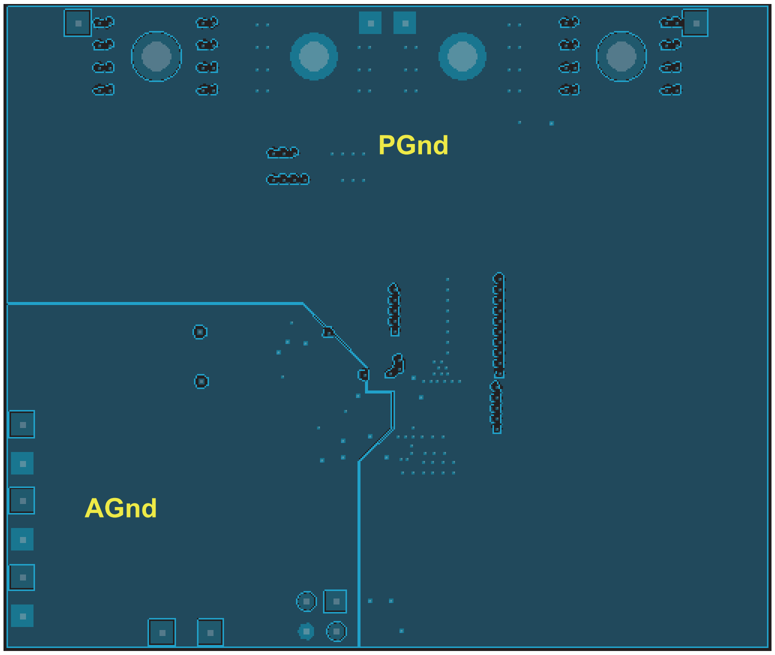
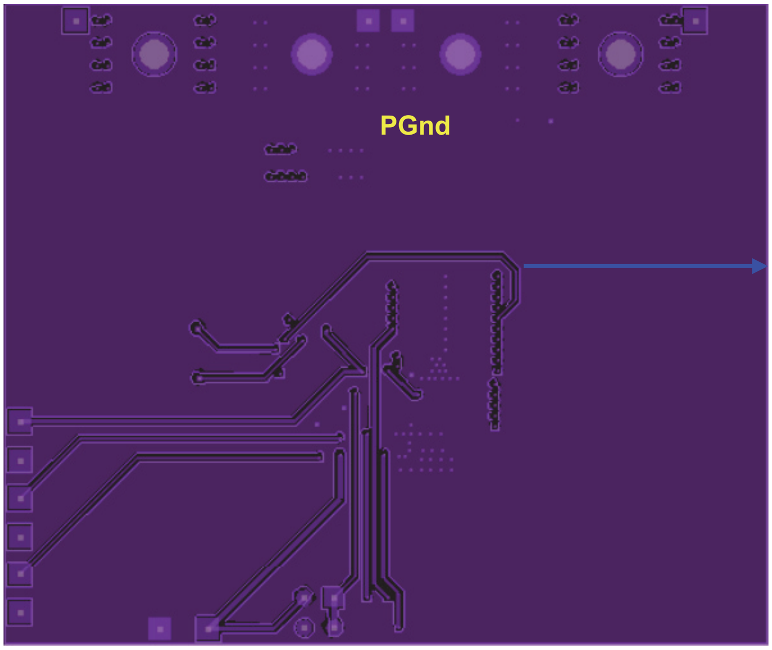


Figure 43: IRDC3823 Demo Board – Middle Layer 1



Feedback and Vsns trace routing should be kept away from noise sources

Figure 44: IRDC3827 Demo Board – Middle Layer 2

PCB METAL AND COMPONENT PLACEMENT

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout as shown in following figures. PQFN devices should be placed to an accuracy of 0.050mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

For further information, please refer to “SupIRBuck® Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note.” (AN1132)

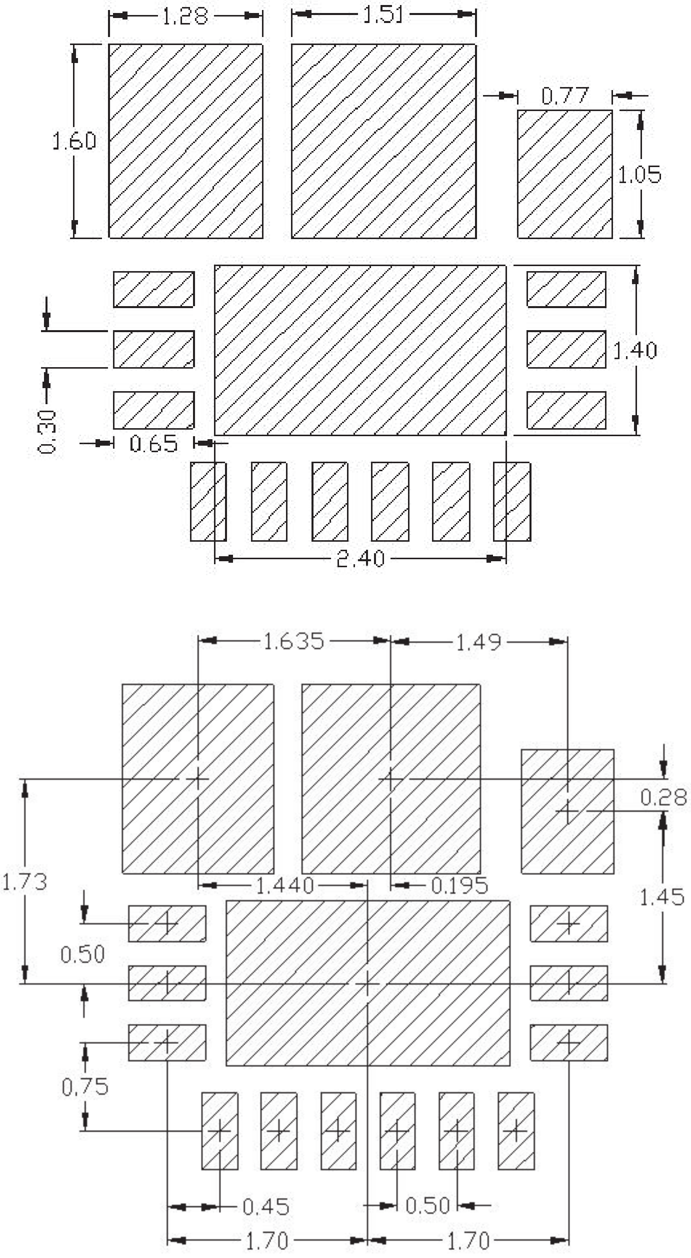


Figure 45: PCB Metal Pad Spacing (all dimensions in mm)

* Contact International Rectifier to receive an electronic PCB Library file in your preferred format

SOLDER RESIST

IR recommends that the larger Power or Land Area pads are Solder Mask Defined (SMD.) This allows the underlying Copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability.

When using SMD pads, the underlying copper traces should be at least 0.05mm larger (on each edge) than the Solder Mask window, in order to accommodate any layer to layer misalignment. (i.e. 0.1mm in X & Y.)

However, for the smaller Signal type leads around the edge of the device, IR recommends that these are Non Solder Mask Defined (NSMD) or Copper Defined.

When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025mm on each edge, (i.e. 0.05mm in X&Y,) in order to accommodate any layer to layer misalignment.

Ensure that the solder resist in-between the smaller signal lead areas are at least 0.15mm wide, due to the high x/y aspect ratio of the solder mask strip.

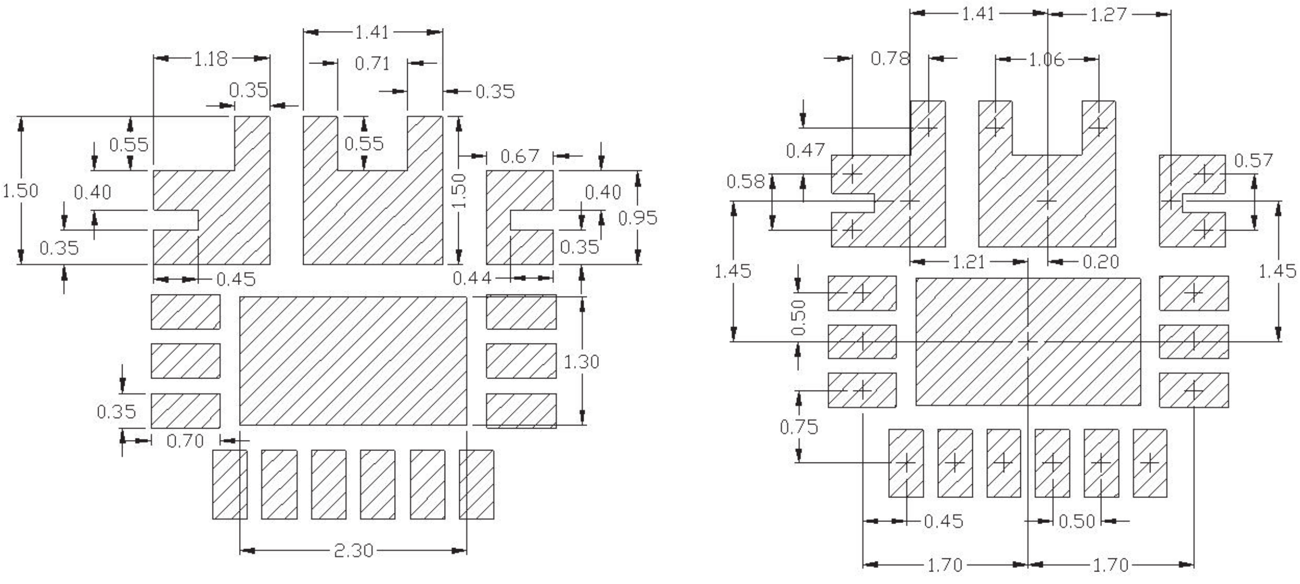

1.18
1.41
0.71
0.35
0.35
0.55
0.55
1.50
0.40
0.35
0.45
1.50
0.67
0.40
0.95
0.35
0.44
1.30
0.35
0.70
2.30
1.41
1.27
0.78
1.06
0.47
0.58
0.57
1.45
1.21
0.20
1.45
0.50
0.75
0.45
0.50
1.70
1.70

Figure 46: Solder Resist

STENCIL DESIGN

Stencils for PQFN can be used with thicknesses of 0.100-0.250mm (0.004-0.010"). Stencils thinner than 0.100mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125mm-0.200mm (0.005-0.008"), with suitable reductions, give the best results.

Evaluations have shown that the best overall performance is achieved using the stencil design shown in following figure. This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

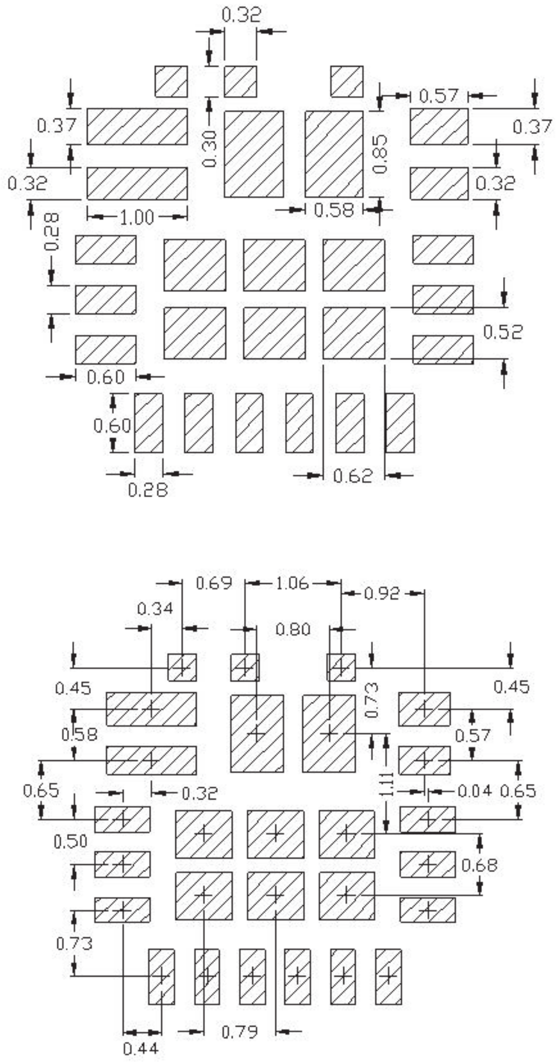
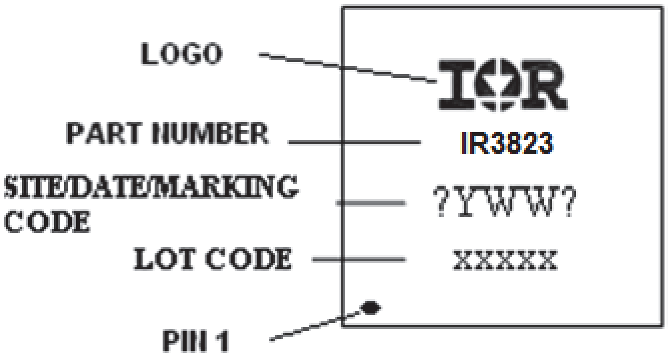
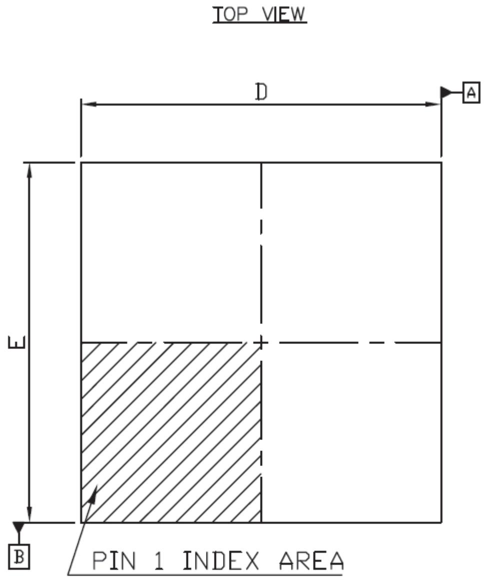

0.32
0.57
0.37
0.37
0.30
0.85
0.32
0.32
1.00
0.58
0.28
0.52
0.60
0.60
0.28
0.62
0.69
1.06
0.92
0.34
0.80
0.45
0.45
0.73
0.58
0.57
0.65
0.32
1.11
0.04
0.65
0.50
0.68
0.73
0.44
0.79

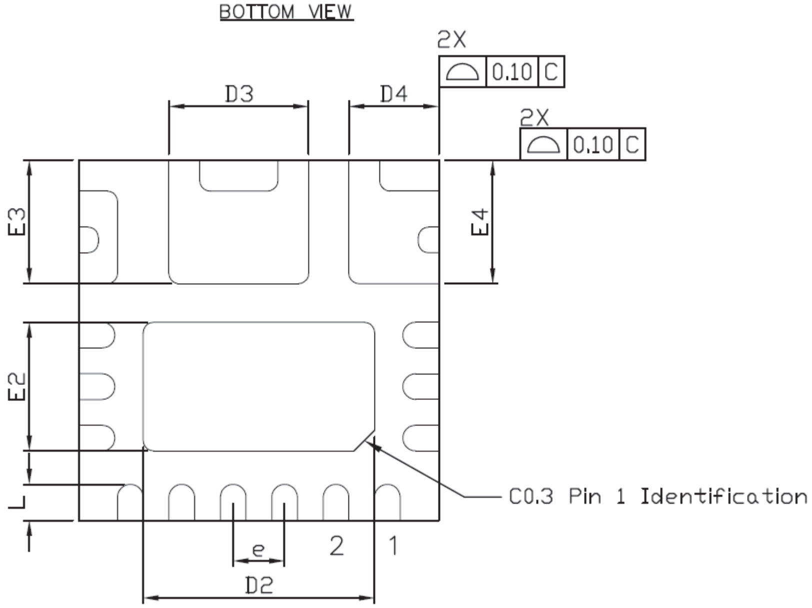
Figure 47: Stencil Pad Spacing (all dimensions in mm)

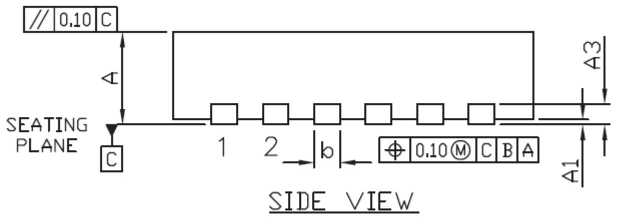
MARKING INFORMATION


LOGO
PART NUMBER
SITE/DATE/MARKING CODE
LOT CODE
PIN 1
IR3823
?YWW?
XXXXX

PACKAGE INFORMATION


TOP VIEW
D
A
E
B
PIN 1 INDEX AREA


BOTTOM VIEW
2X
0.10 C
D3
D4
2X
0.10 C
E3
E4
E2
L
e
2
1
D2
C0.3 Pin 1 Identification


//0.10 C
A
A3
SEATING PLANE
C
1
2
b
⌖ 0.10 Ⓜ C B A
A1
SIDE VIEW

SYMBOL	Common					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.85	0.90	0.95	0.034	0.036	0.038
A3	0.203 REF.			0.008 REF.		
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
D	3.40	3.50	3.60	0.134	0.138	0.142
D2	2.20	2.25	2.30	0.087	0.089	0.091
D3	1.31	1.36	1.41	0.052	0.054	0.056
D4	0.82	0.87	0.92	0.032	0.034	0.036
E	3.40	3.50	3.60	0.134	0.138	0.142
E2	1.20	1.25	1.30	0.047	0.049	0.051
E3	1.15	1.20	1.25	0.045	0.047	0.049
E4	1.15	1.20	1.25	0.045	0.047	0.049
e	0.50 BSC			0.020 BSC		
L	0.30	0.35	0.40	0.014	0.016	0.018

ENVIRONMENTAL QUALIFICATIONS

Qualification Level		Industrial	
Moisture Sensitivity Level		3.5mm x 3.5mm PQFN	JEDEC Level 2 @ 260°C
ESD	Machine Model (JESD22-A115A)	Class B ≥200V to <400V	
	Human Body Model (JESD22-A114F)	Class 2 ≥2000V to <4000V	
	Charged Device Model (JESD22-C101D)	Class III ≥500V to ≤1000V	
RoHS6 Compliant		Yes	

† Qualification standards can be found at International Rectifier web site: http://www.irf.com
†† Exceptions to AEC-Q101 requirements are noted in the qualification report.

Data and specifications subject to change without notice.
Qualification Standards can be found on IR's Web site.

International
Rectifier

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