

# RJK2061JPE

Silicon N Channel MOS FET  
High Speed Power Switching

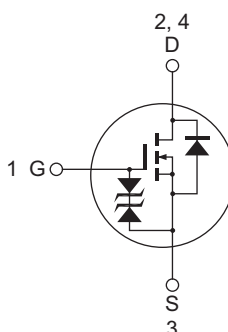
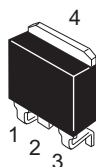
R07DS0369EJ0100  
Rev.1.00  
May 12, 2011

## Features

- For Automotive application
- AEC-Q101 compliant
- Low on-resistance :  $R_{DS(on)} = 55 \text{ m}\Omega$  typ.
- Low input capacitance :  $C_{iss} = 1850 \text{ pF}$  typ

## Outline

RENESAS Package code: PRSS0004AE-B  
(Package name: LDPAK(S)-(1) )



1. Gate
2. Drain
3. Source
4. Drain

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Value	Unit
Drain to source voltage	$V_{DSS}$	200	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	40	A
Drain peak current	$I_D$ (pulse) <sup>Note1</sup>	160	A
Body-drain diode reverse drain current	$I_{DR}$	40	A
Body-drain diode reverse drain peak current	$I_{DR}$ (pulse) <sup>Note1</sup>	160	A
Avalanche current	$I_{AP}$ <sup>Note2</sup>	15	A
Avalanche energy	$E_{AR}$ <sup>Note2</sup>	15	mJ
Channel dissipation	$P_{ch}$ <sup>Note3</sup>	150	W
Channel temperature	$T_{ch}$ <sup>Note4</sup>	175	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

- Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$   
 2.  $T_{ch} = 25^\circ\text{C}$ ,  $R_g \geq 50 \Omega$   
 3.  $T_c = 25^\circ\text{C}$   
 4. AEC-Q101 compliant

## Thermal Impedance Characteristics

- Channel to case thermal impedance  $\theta_{ch-c}$ :  $1.0^\circ\text{C/W}$

## Electrical Characteristics

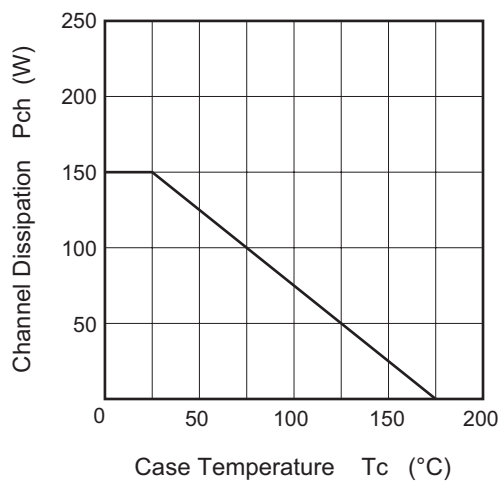
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu A$	$V_{GS} = \pm 20 V, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu A$	$V_{DS} = 200 V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.5	—	3.5	V	$I_D = 1 mA, V_{DS} = 10 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	55	75	m $\Omega$	$I_D = 20 A, V_{GS} = 10 V$ <sup>Note5</sup>
Input capacitance	$C_{iss}$	—	2100	—	pF	$V_{DS} = 10 V,$ $V_{GS} = 0$ $f = 1 MHz$
Output capacitance	$C_{oss}$	—	385	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	65	—	pF	
Total gate charge	$Q_g$	—	32	—	nC	$V_{DD} = 25 V, V_{GS} = 10 V$ $I_D = 40 A$
Gate to source charge	$Q_{gs}$	—	9.5	—	nC	
Gate to drain charge	$Q_{gd}$	—	4	—	nC	
Turn-on delay time	$t_{d(on)}$	—	17	—	ns	$I_D = 20 A, R_L = 1.5 \Omega$ $V_{GS} = 10 V, R_G = 4.7 \Omega$
Rise time	$t_r$	—	3.5	—	ns	
Turn-off delay time	$t_{d(off)}$	—	45	—	ns	
Fall time	$t_f$	—	5	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.9	1.17	V	$I_F = 40 A, V_{GS} = 0$ <sup>Note5</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	155	—	ns	$I_F = 40 A, V_{GS} = 0,$ $di_F/dt = 100 A/\mu s$

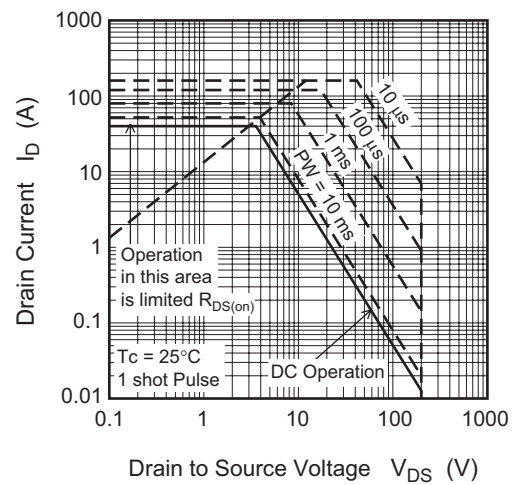
Note: 5. Pulse test

## Main Characteristics

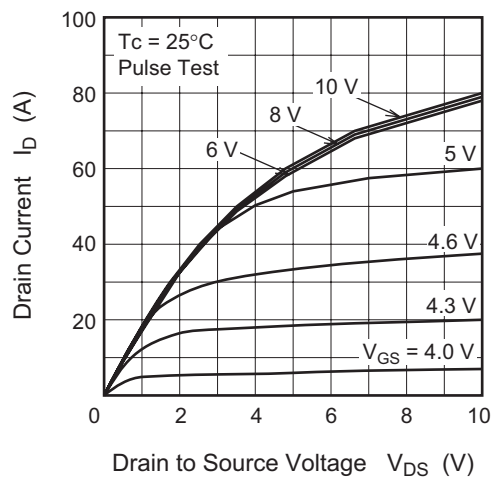
Power vs. Temperature Derating



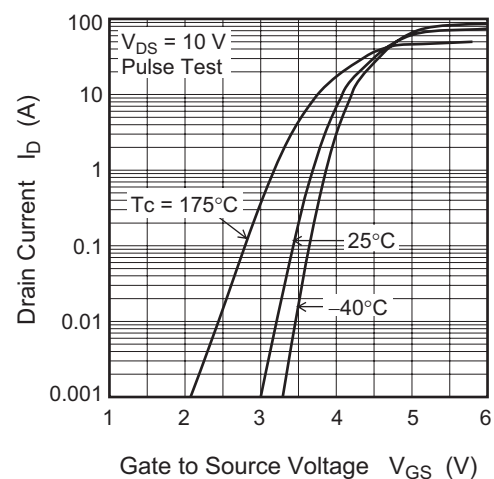
Maximum Safe Operation Area



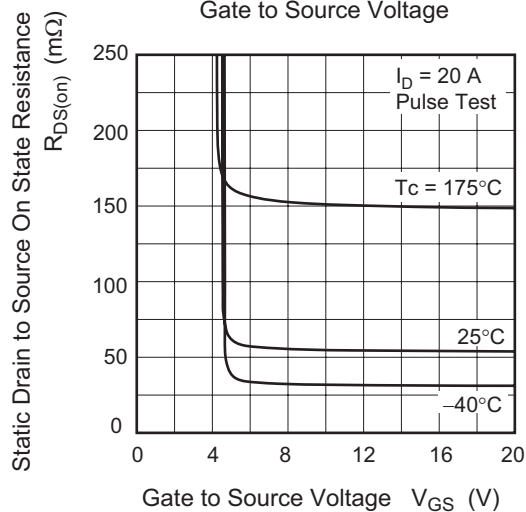
Typical Output Characteristics



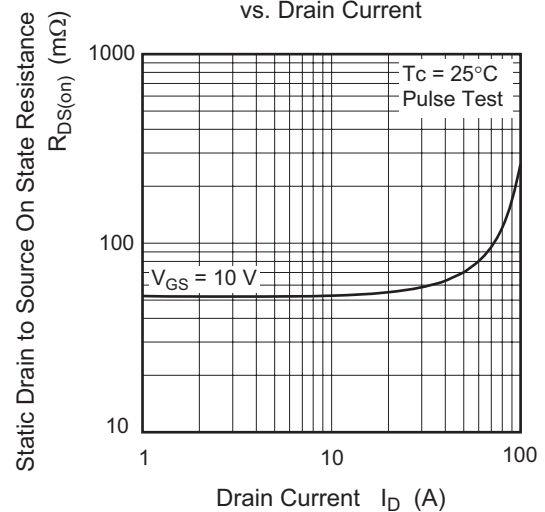
Typical Transfer Characteristics



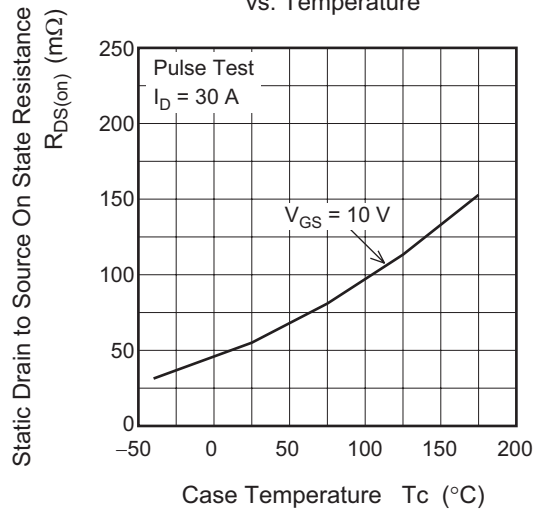
Static Drain to Source On State Resistance vs. Gate to Source Voltage



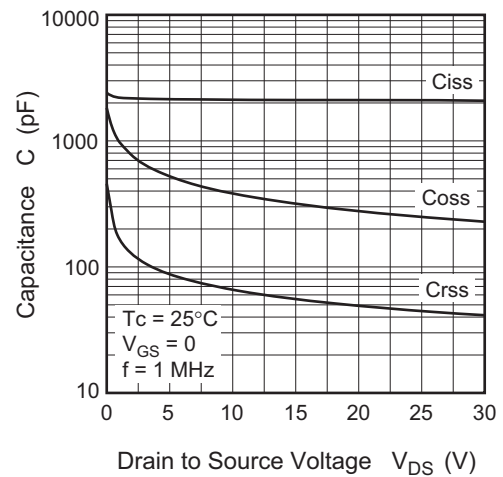
Static Drain to Source On State Resistance vs. Drain Current



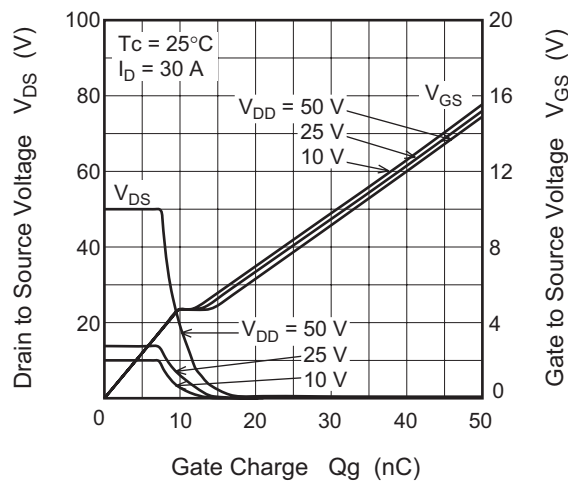
Static Drain to Source On State Resistance vs. Temperature



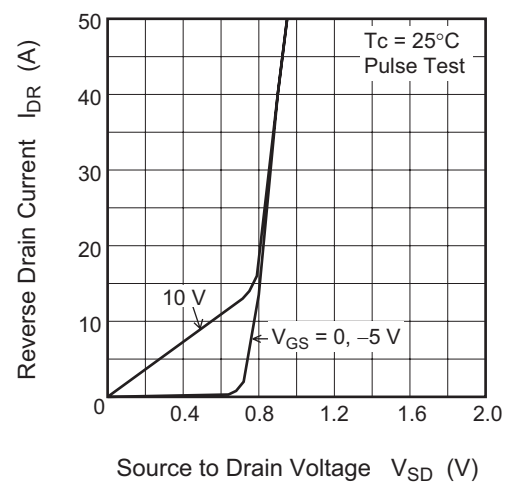
Typical Capacitance vs. Drain to Source Voltage



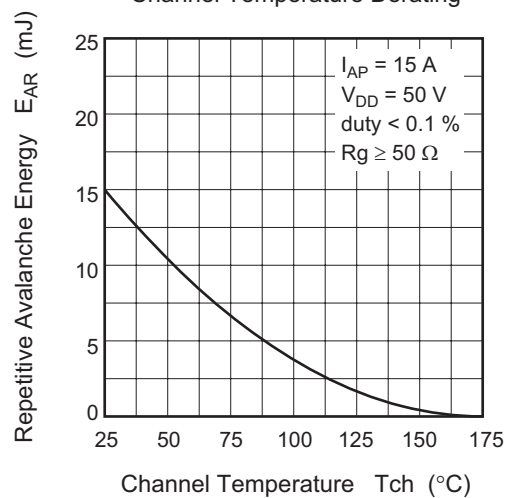
Dynamic Input Characteristics

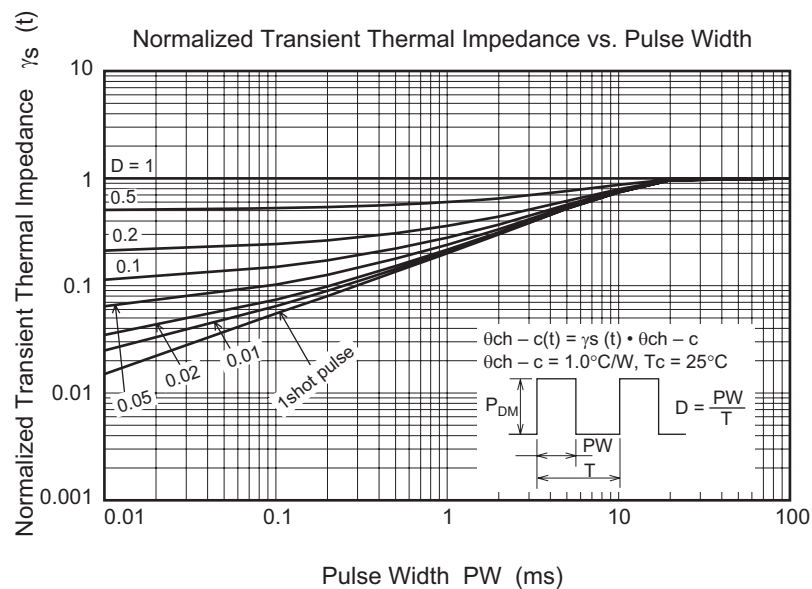


Reverse Drain Current vs. Source to Drain Voltage

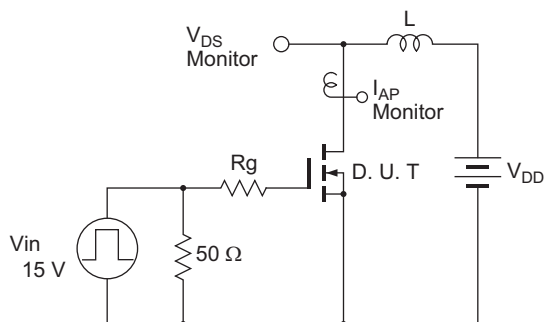


Avalanche Energy vs. Channel Temperature Derating

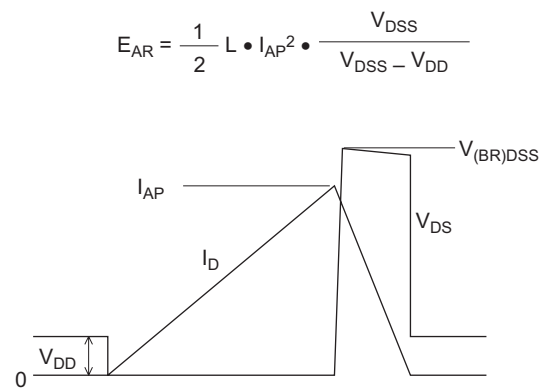




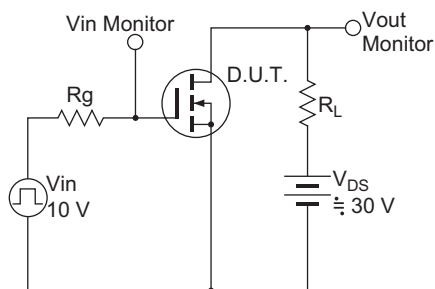
Avalanche Test Circuit



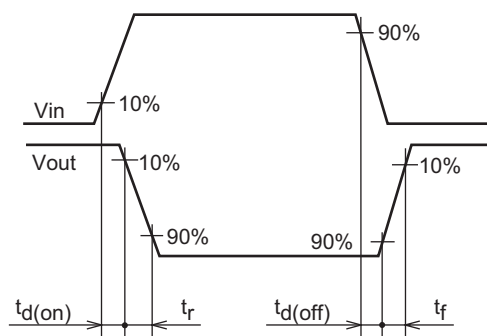
Avalanche Waveform



Switching Time Test Circuit



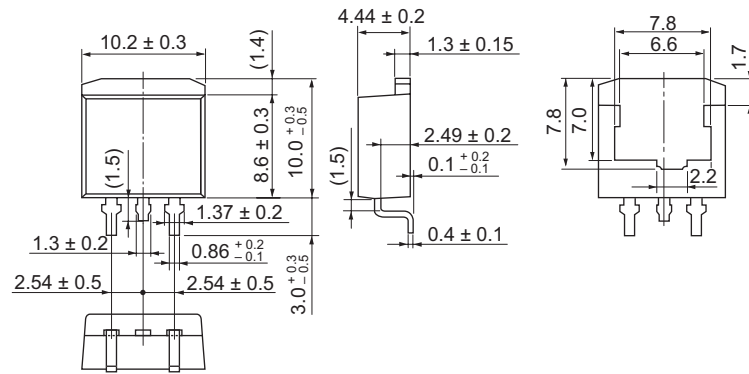
Switching Time Waveform



## Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBAK(S)-(1)	SC-83	PRSS0004AE-B	LDBAK(S)-(1) / LDBAK(S)-(1)V	1.30g

Unit: mm



## Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK2061JPE-00-J3	1000 pcs	Taping (Sinistrorse)

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