MC14417

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

TSAC
TIME SLOT ASSIGNER CIRCUIT

BASIC TIME SLOT ASSIGNER CIRCUIT (TSAC)

The MC14417 is a per channel Time Slot Assigner Circuit (TSAC) that produces 8-bit receive and transmit time slots for a PCM Codec. The pins D0 to D5 are the time slot data inputs which can be either hard-wired on the printed circuit board for fixed time slot assignment, or externally programmed through the use of these pins and the latch enable function. The receive and transmit frame syncs and enables are independent. In addition, a T/R (TXE/RXE swap) input is provided which allows a simplified switching mechanism for a small systems architecture (i.e., key systems).

The MC14417 can operate from a single 5-volt supply for TTL levels or up to 16-volts for CMOS levels. The MC14417 is fabricated using the CMOS technology for reliable low-power performance.

● TTL and CMOS Level Compatibility
● 5 to 16 Volt Operation
● Low Operating Power Consumption
● For Use With Up to 2.56 MHz Clocks
● Independent Transmit and Receive Frame Syncs and Enables
● Up to 64 Time Slots Per Frame
● Compatible with MC14400/01/02/03/05 PCM Mono-Circuits
● Allows Swapping of Transmit Enable (TXE) and Receive Enable (RXE) Signals
● CMOS Metal Gate for High Reliability

L SUFFIX
CERAMIC PACKAGE
CASE 726

P SUFFIX
PLASTIC PACKAGE
CASE 707
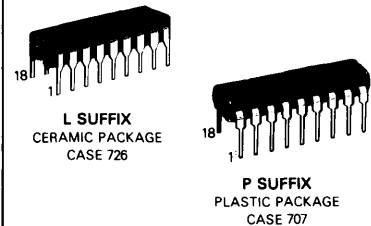
ORDERING INFORMATION

MC14XXX
└─ Suffix Denotes
  ├─ L Ceramic Package
  └─ P Plastic Package

BLOCK DIAGRAM

PIN ASSIGNMENT

VCC	1	18	VDD
D5	2	17	ST
D4	3	16	TXE
D3	4	15	RXE
D2	5	14	DC
D1	6	13	LE
D0	7	12	T/R̄
NDC	8	11	FSR
VSS	9	10	FST

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14417
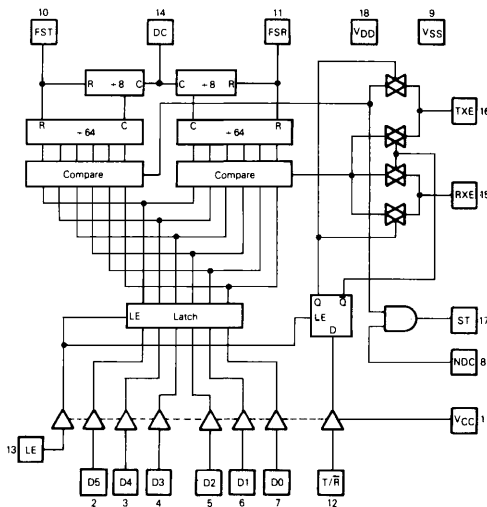
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to 18	V
Level Shift Voltage	V_{CC}	-0.5 to V_{DD}	V
Input Voltage Inputs Referenced to V_{DD} to V_{CC}	V_{in1} V_{in2}	-0.5 to $V_{DD}+0.5$ -0.5 to $V_{DD}+0.5$	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	-40 to $+85$	°C
Storage Temperature Range	T_{stg}	-65 to $+165$	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25$°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
DC Supply Voltage, $V_{SS} = 0$ V	V_{DD}	—	4.5	12	16	V
DC Supply Voltage, $V_{SS} = 0$ V	V_{CC}	—	4.5	5	V_{DD}	V
Output Current TXE, RXE, ST ($V_{OL} = 0.4$ V) ($V_{OL} = 1.0$ V)	I_{OL}	5 12	0.51 2.0	— 4.0	— —	mA
($V_{OH} = 4.6$ V) ($V_{OH} = 11.0$ V)	I_{OH}	5 12	-0.2 -2.0	— -4.0	— —	mA
Input Voltage (CMOS) FST, FSR, DC1, DC2, NDC "0"	V_{IL}	5 12	— —	— —	1.0 2.4	V
"1"	V_{IH}	5 12	4.0 9.6	— —	— —	V
Input Voltage (TTL) D0–D5, LE, T/$\overline{R}$, $V_{CC} = 5$ V "0"	V_{IL}	5 12 16	— — —	— — —	0.8 0.8 0.7	V
"1"	V_{IH}	5 12	2.0 2.0	— —	— —	V
Total Supply Current (Outputs Unloaded) DC1 at 2.048 MHz	I_T	5 12	— —	1.5 2.5	— —	mA

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25$°C, Unless Otherwise Noted)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time, TXE, RXE, ST	t_r	5 12	— —	100 50	200 100	ns
Output Fall Time, TXE, RXE, ST	t_f	5 12	— —	100 50	200 100	ns
Frame Sync Setup Time (See Figure 1)	t_{SFS}	5 12	-150 -75	— —	$+150$ $+75$	ns
Frame Sync Pulse Width	t_{PWFS}	5 12	200 100	— —	— —	ns
Propagation Delay (Note 1) DC1 to TXE, DC2 to RXE, $C_L = 20$ pF	t_{PHLE}, t_{PLHE}	5 12	— —	130 80	180 125	ns
Data Clock Frequency	f_{DC}	5 12	— —	— —	2.048 2.6	MHz
Data Clock Pulse Width at f_{DC} (Max)	t_{PWDC}	5 12	200 140	244 192	293 260	ns
LE Pulse Width	t_{PWLE}	5 12	1 1	— —	— —	μs
NDC to ST Propagation Delay		5 12	— —	— —	120 80	ns
FST to ST Propagation Delay		5 12	— —	— —	200 130	ns

NOTE 1: For time slot 0, t_{PHLE} and t_{PLHE} are measured from the leading edge of DC or FST (FSR), whichever occurs last.

FIGURE 1 — TIMING DIAGRAMS

2

DC

tSFS

tPWFS

FST, FSR

NOTE: No restriction on falling edge.

tPWDC

DC

tPLHE

tPHLE

8 Data Clocks

TXE, RXE
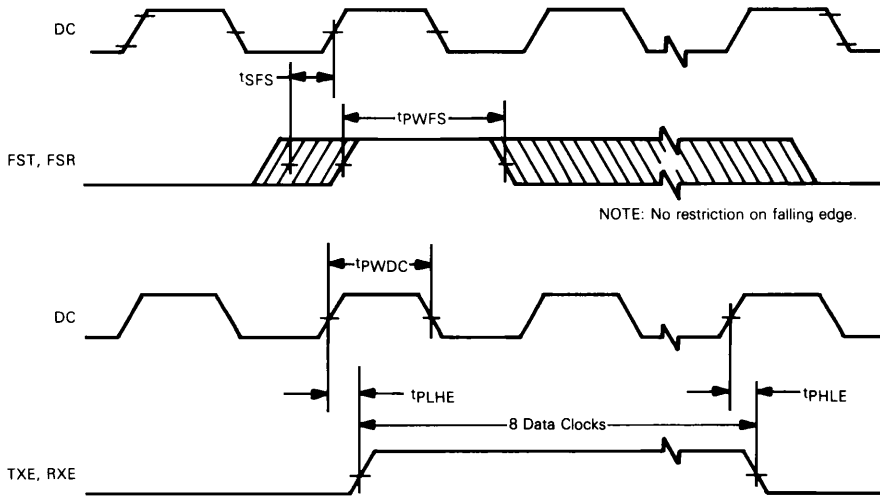
PIN DESCRIPTIONS

V_{CC} **(Positive Supply)** — The V_{CC} power supply controls the inputs LE, D0-D5 and T/$\overline{R}$. It can be supplied by any voltage from 4.5 to V_{DD}. In typical usage, V_{CC} is 5 volts for TTL or microprocessor compatibility of the control inputs to the TSAC while V_{DD} and V_{SS} are connected to the Codec supplies.

D5-D0 (Parallel Time Slot Data Inputs) — The six inputs to the input-storage latch are the time-slot data. D0 is the least-significant bit while D5 is the most-significant. The binary word at this input represents the number of 8 bit time slots from FST and FSR where TXE and RXE will occur, respectively. These can be 5-volt input compatible with TTL and are internally level shifted to the V_{DD} supply.

LE (Latch Enable Input with Internal Pull-Up) — This input allows the data D0 through D5 and T/$\overline{R}$ bits to be latched in the input-storage latch. If LE is held high, then the inputs to the latch are combinational and directly applied to the compare circuits. When LE is pulled low, the input values applied at D0 through D5 and T/$\overline{R}$ are latched and held in the storage latch.

T/$\overline{R}$ (TXE/RXE Swap Input with Internal Pull-Up) — This input allows the TXE and RXE inputs to be swapped. When T/$\overline{R}$ is a one, the TXE output is derived from FST and RXE from FSR. If T/$\overline{R}$ is a zero, the derivation is reversed. If FST and FSR are eight data clocks apart, then two TSAC channels programmed to the same D0 through D5 and different T/$\overline{R}$ bits will create a completed conversation. This feature is intended for use in simplifying small-key systems.

DC (Data Clock Input) — The data clock input establishes the bit rate for the TSAC. This is typically 1.544 or 2.048 MHz but can be any frequency up to 2.56 MHz. The data clock is divide-by-8 for both transmit- and receive-time slots. The data clock input is a CMOS compatible input between V_{DD} and V_{SS}.

FST (Frame Sync Transmit Input) — This input identifies the beginning of the zero-transmit time slot by resetting the divide-by-8 and divide-by-64 counters. FST is a CMOS compatible input between V_{DD} and V_{SS}. The TXE output will begin and end on one 8-bit word boundary which is synchronized with the FST input. The FST signal should be aligned with the leading edge of data clock and is typically 8 kHz.

FSR (Frame Sync Receive Input) — The FSR input provides the same functions for the RXE output as FST did for TXE. The FSR and FST inputs can be any number of data clocks different, or can be the same.

TXE, RXE (Transmit-Enable and Receive-Enable Outputs) — These outputs are used to control the transmitting and receiving of data words to and from Codecs. Each output swings from V_{DD} to V_{SS} and is eight data clocks long. TXE and RXE go high at the beginning of the programmed time slot and low at the end. TXE is derived from FST and RXE is derived from FSR, provided the T/$\overline{R}$ bit is high.

ST (Strobe Output) — The strobe output is provided to allow simplified input data storage or off-hook multiplexing control. ST is the logical AND of an enable signal (NDC) and the TXE time slot period. Thus, ST can only be high during a programmed TXE time slot. Since no other TSAC in a bank can have the same TXE programming, the ST output on any TSAC can be used to uniquely identify that TSAC by a pulse input on NDC. In many applications ST is used to control the LE input.

NDC (New Data Clock Input with Internal Pull-Up) — This input can be used in conjunction with ST to strobe data into a TSAC bank. NDC can be used to enable the strobe output.

V_{DD}, V_{SS} — The TSAC will operate from any single supply from 4.5 to 16 volts. The TSAC can be used in a 5-volt-only system by making both V_{CC} and V_{DD} 5 volts.

FIGURE 2 — MOTOROLA MONO-CIRCUIT/TSAC COMBINATIONS
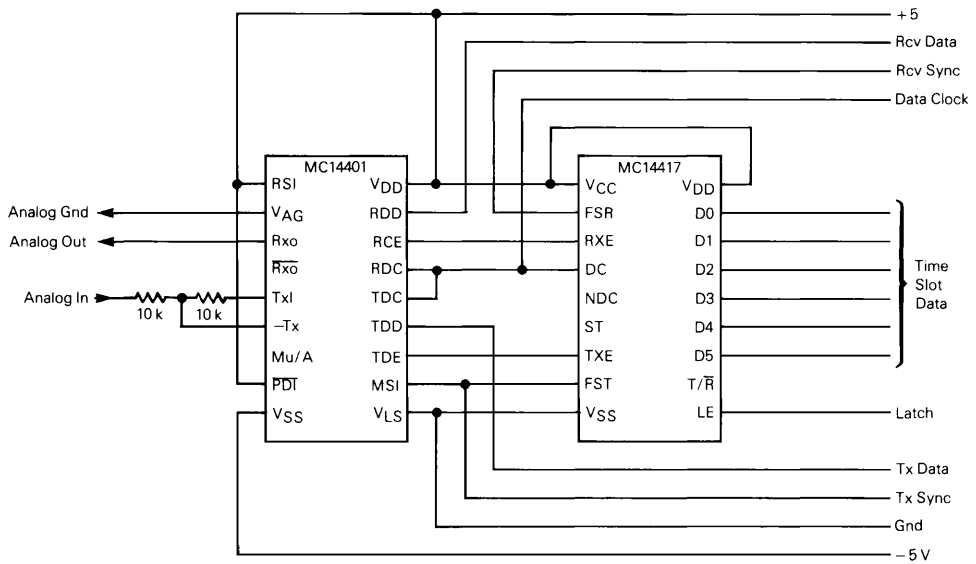
The MC14417 TSAC offers simple flexible time slot assignment for
the PCM mono-circuit. Assignments are wired or latched into
the data port. The MC14401 offers supply flexibility of ±5, ±6, +12,
or +10 V with 18 pin packages and TTL compatibility.