v00.0911

HMC993LP5E

RF AUTOMATIC GAIN CONTROLLER (RF-AGC), 700 - 3000 MHz

Typical Applications

The HMC993LP5E is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

Wide Gain Control Range: -11 to +32 dB

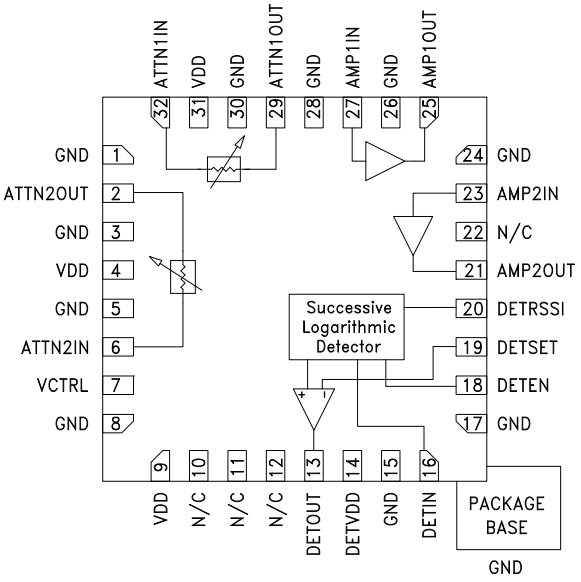
High Output IP3: +46 dBm

Positive Analog Control: 0V to +5V

Configurable with 1 or 2 Attenuators

32 Lead 5x5 mm SMT Package: 25 mm^2

Functional Diagram



General Description

The HMC993LP5E is an RF analog controlled variable gain amplifier composed of two identical voltage variable attenuators in combination with an InGaP HBT gain block MMIC amplifier which operates from 0.7 to 3.0 GHz, and can be controlled to provide anywhere from -11 dB attenuation, to 32 dB of gain. The HMC993LP5E delivers noise figure of 8 dB in its maximum gain state, with output IP3 of up to +46 dBm. The HMC993LP5E is housed in a RoHS compliant 5x5 mm QFN leadless package.

Electrical Specifications,

T_A = +25° C, 50 Ohm System, VDD = DETVDD = +5V [1]

Parameter		Frequency	Min.	Typ.	Max.	Units
Gain (min. Attenuation)	1 Attenuator Operation	0.9 GHz 1.9 GHz 2.4 GHz 2.8 GHz		36 26 23 20		dB dB dB dB
	2 Attenuator Operation	0.9 GHz 1.9 GHz 2.4 GHz		32 21 17		dB dB dB
Gain Control Range	1 Attenuator Operation	0.9 GHz 1.9 GHz 2.4 GHz 2.8 GHz		21 22 23 24		dB
	2 Attenuator Operation	0.9 GHz 1.9 GHz 2.4 GHz		43 33 28		dB

Electrical Specifications (continued),

T_A = +25° C, 50 Ohm System, VDD = DETVDD = +5V [1]

Parameter		Frequency	Min.	Typ.	Max.	Units
Input Return Loss (min. Attenuation)	1 Attenuator Operation	0.9 GHz 1.9 GHz 2.4 GHz 2.8 GHz		15 13 13 13		dB
	2 Attenuator Operation	0.9 GHz 1.9 GHz 2.4 GHz		15 15 13		dB
Output Return Loss (min. Attenuation)	1 Attenuator Operation	0.9 GHz 1.9 GHz 2.4 GHz 2.8 GHz		17 23 17 18		dB
	2 Attenuator Operation	0.9 GHz 1.9 GHz 2.4 GHz		16 28 18		dB
Output Third Order Intercept Point (Two-Tone Output Power= 0 dBm Each Tone) (min. Attenuation)		0.9 GHz 1.9 GHz 2.4 GHz 2.8 GHz		46 45 45 40		dBm dBm
Output Power for 1dB Compression (min. Attenuation)		0.9 GHz 1.9 GHz 2.4 GHz 2.8 GHz		25 25 24.8 24		dBm dBm
Noise Figure (min. Attenuation)		0.9 GHz 1.9 GHz 2.4 GHz 2.8 GHz		7.6 9.5 10.7 11.8		dB
Supply Current (Idd)				260		mA
Power Detector						
		Typ.	**Typ.**	**Typ.**	**Typ**	**Units**
Input Frequency		900	1900	2400	2800	MHz
±3 dB Dynamic Range		61	61	61	62	dB
DETOUT Slope		15.5	15.4	15.4	15.5	mV/dB
DETOUT Intercept		-68.2	-69.9	-70	-71.3	dBm
Veriation of DETOUT with Temperature from -40°C to +85°C @20dBm Input		-1.3	-1.2	-1.2	-1.2	dB

[1] Unless otherwise noted, test conditions: ATTN1 + ATTN2 + AMP1 + AMP2 in cascade.

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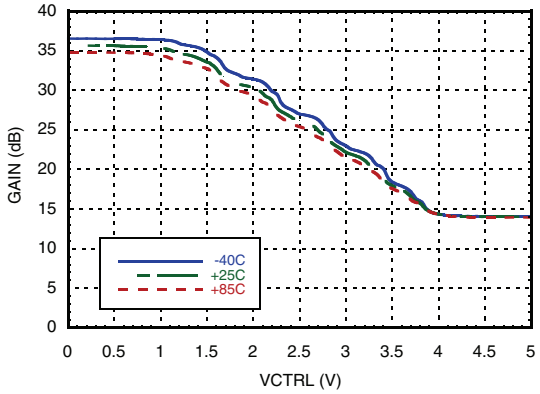
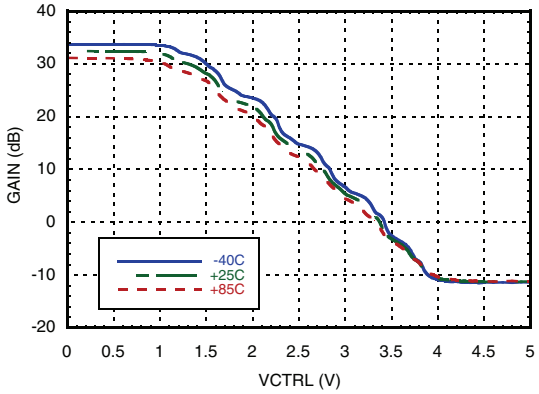
900MHz TUNE

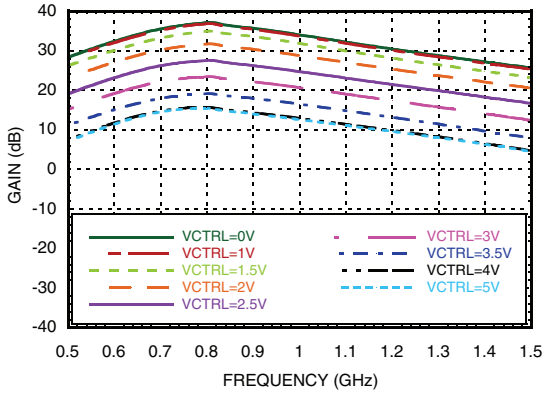
Gain vs. VCTRL [1]



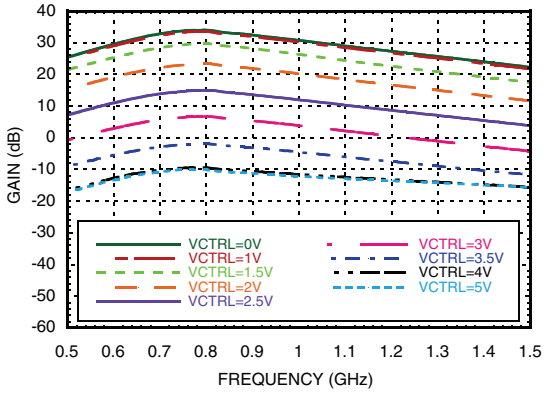
Gain vs. VCTRL [2]



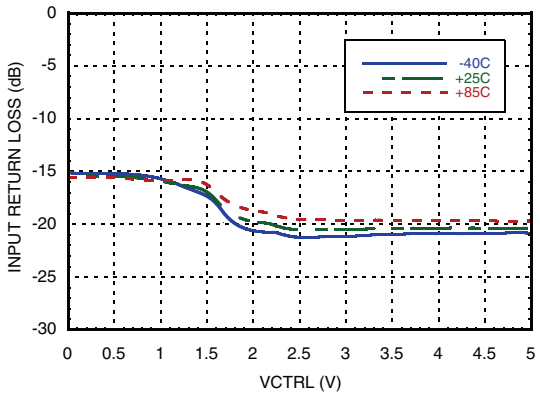
Gain vs. Frequency [1]



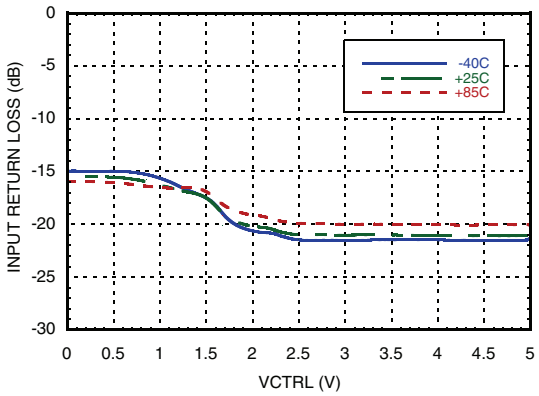
Gain vs. Frequency [2]



Input Return Loss vs. VCTRL [1]

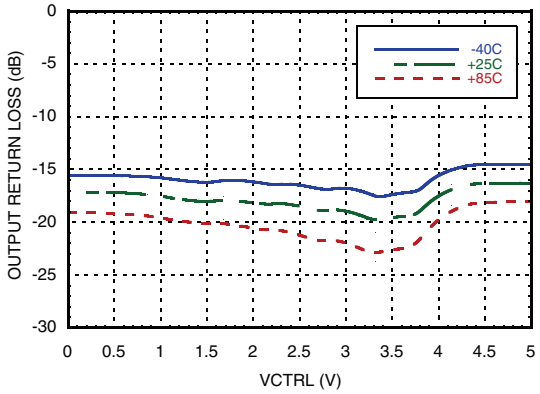


Input Return Loss vs. VCTRL [2]

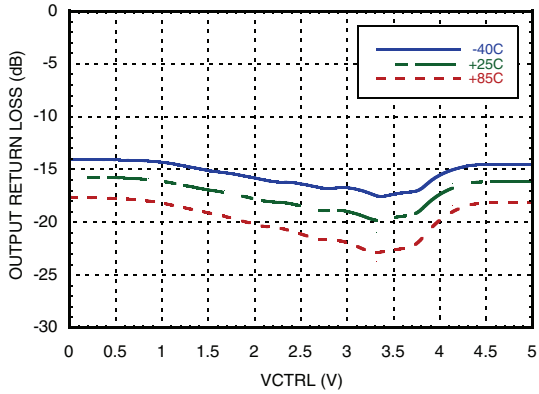


[1] ATTN1 + AMP1 + AMP2
[2] ATTN1 + ATTN2 + AMP1 + AMP2

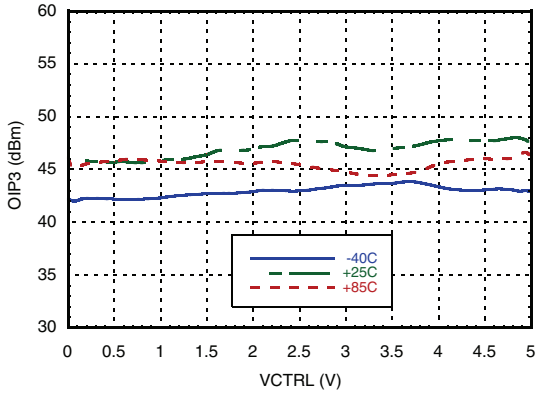
Output Return Loss vs. VCTRL [1]



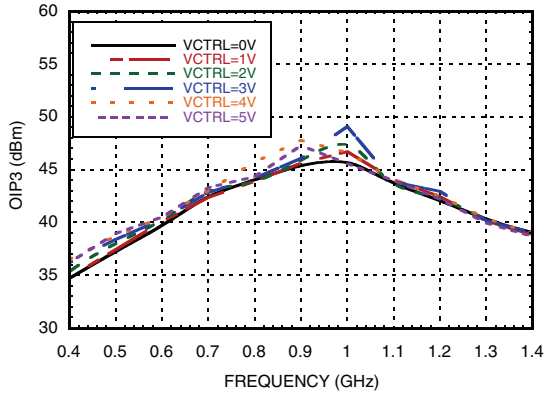
Output Return Loss vs. VCTRL[2]



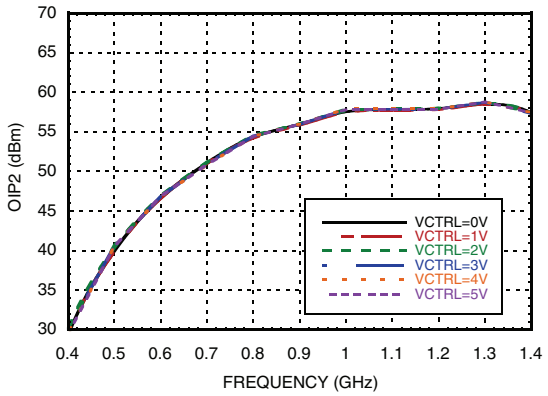
Output IP3 vs. VCTRL [1]



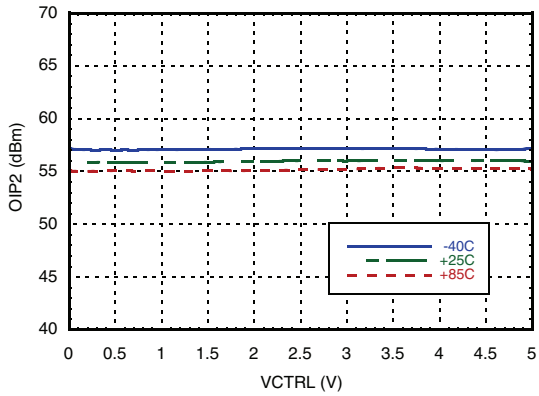
Output IP3 vs. Frequency [1]



Output IP2 vs. Frequency [1]



Output IP2 vs.VCTRL [1]



[1] ATTN1 + AMP1 + AMP2
[2] ATTN1 + ATTN2 + AMP1 + AMP2

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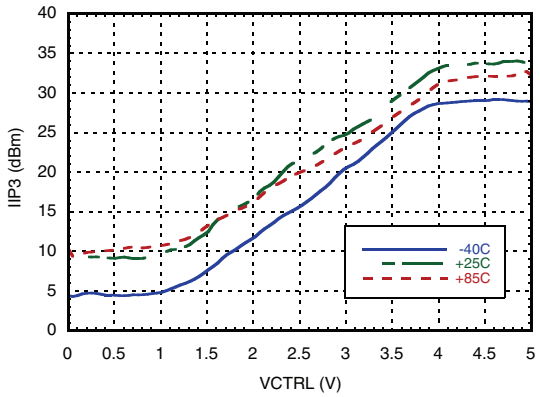
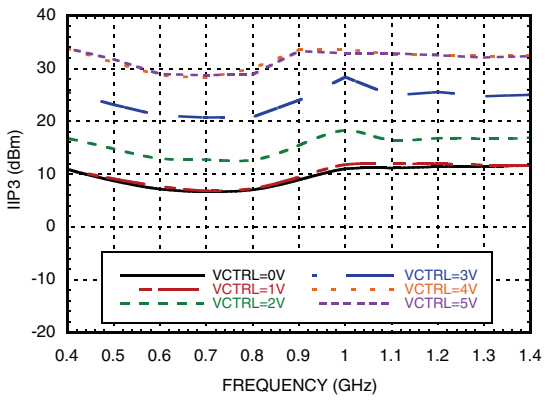
900MHz TUNE

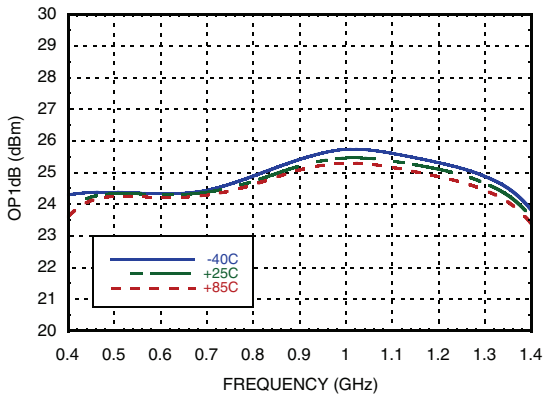
Input IP3 vs.VCTRL [1]



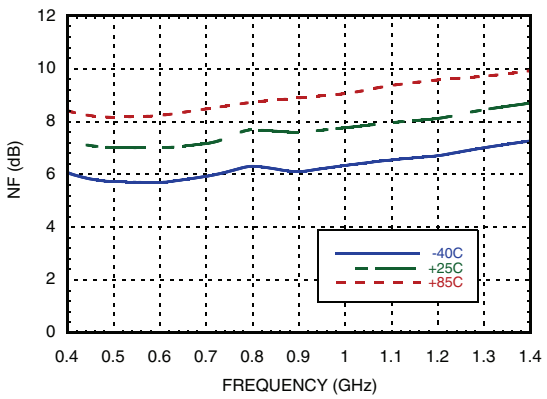
Input IP3 vs. Frequency [1]



Output P1dB vs. Frequency [1] [2]



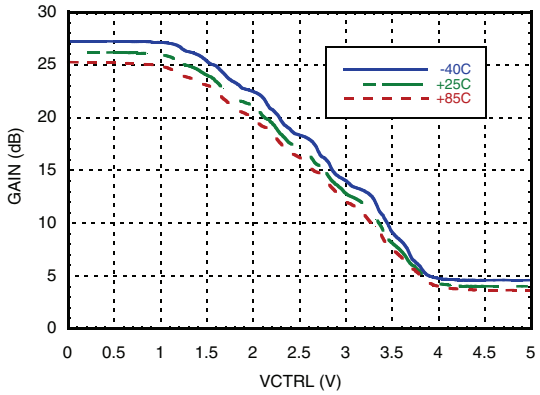
Noise Figure vs. Frequency [1] [2]



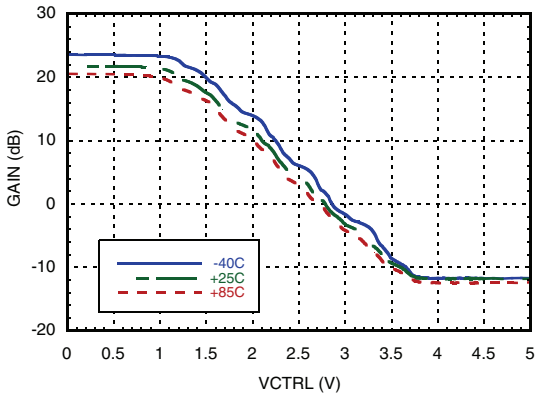
[1] ATTN1 + AMP1 + AMP2
[2] VCTRL=Minimum Attenuation

1900MHz TUNE

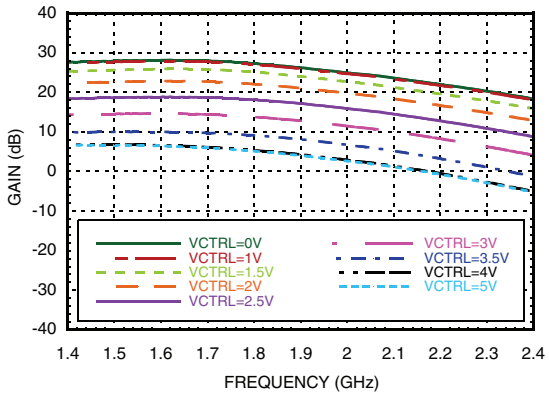
Gain vs. VCTRL [1]



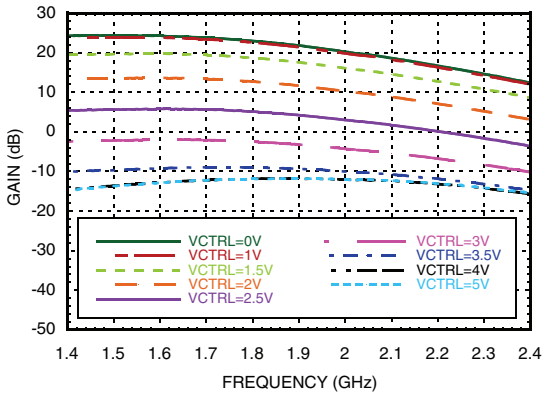
Gain vs. VCTRL [2]



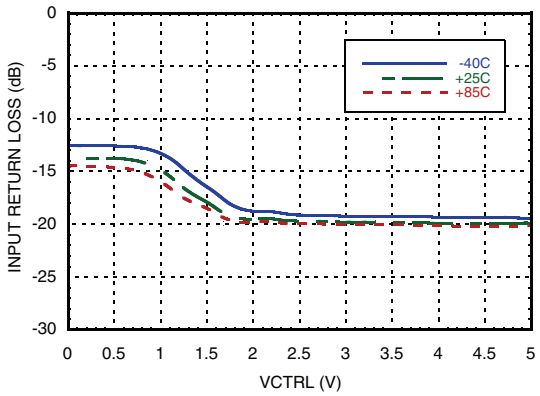
Gain vs. Frequency [1]



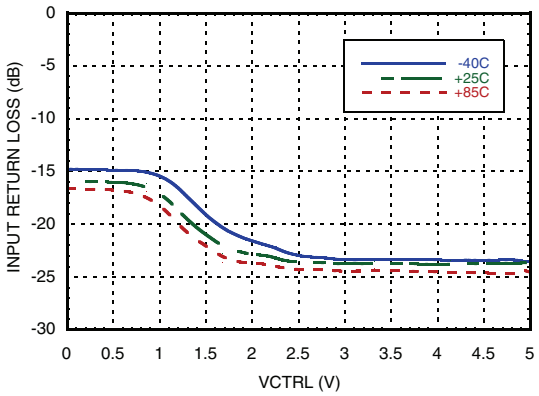
Gain vs. Frequency [2]



Input Return Loss vs. VCTRL [1]



Input Return Loss vs. VCTRL [2]



[1] ATTN1 + AMP1 + AMP2
[2] ATTN1 + ATTN2 + AMP1 + AMP2

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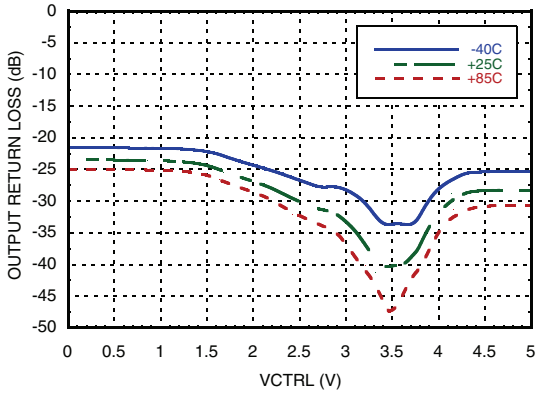
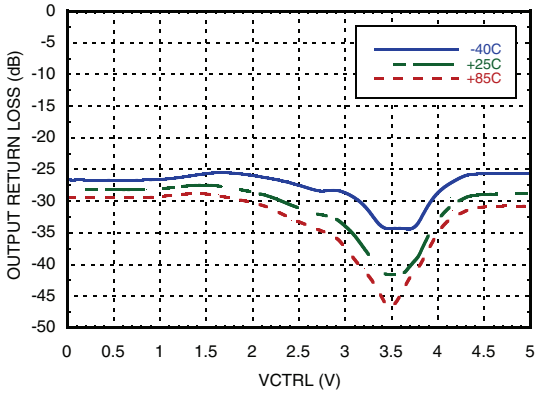
1900MHz TUNE

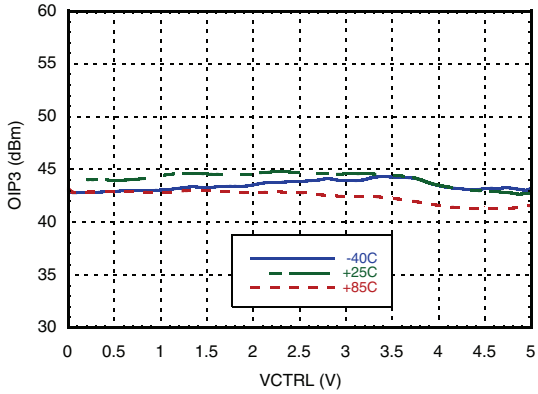
Output Return Loss vs. VCTRL [1]



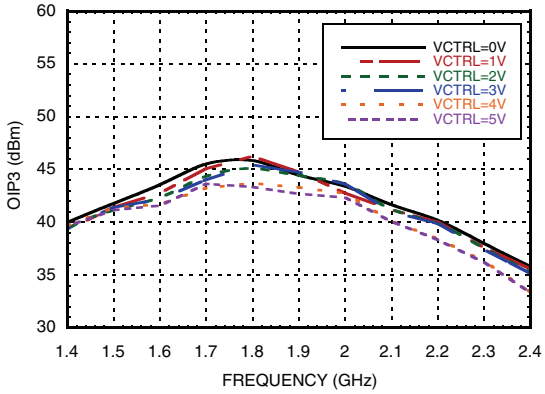
Output Return Loss vs. VCTRL [2]



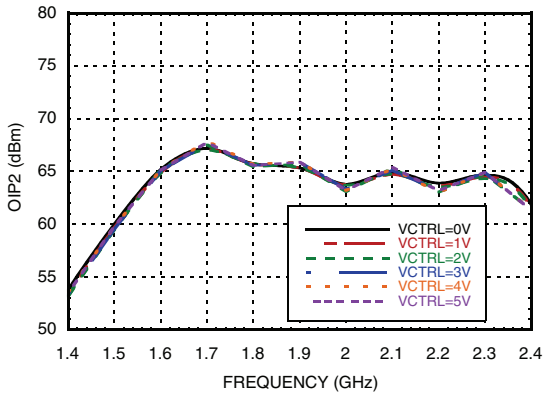
Output IP3 vs. VCTRL [1]



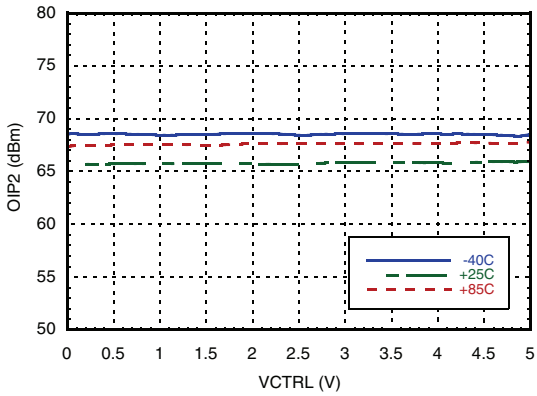
Output IP3 vs. Frequency [1]



Output IP2 vs. Frequency [1]



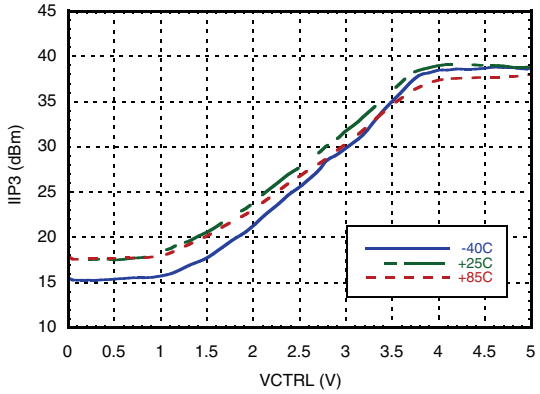
Output IP2 vs.VCTRL [1]



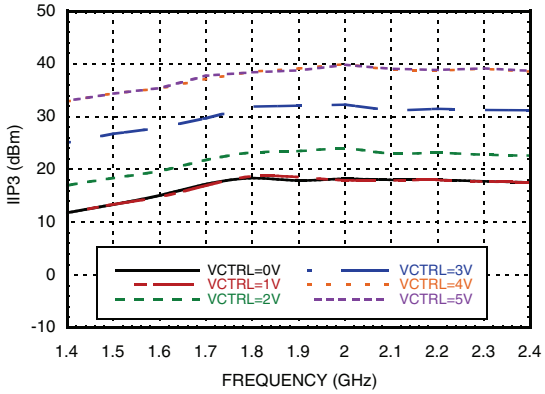
[1] ATTN1 + AMP1 + AMP2
[2] ATTN1 + ATTN2 + AMP1 + AMP2

1900MHz TUNE

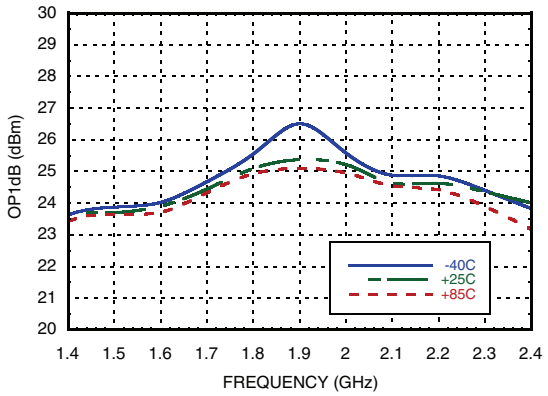
Input IP3 vs.VCTRL [1]



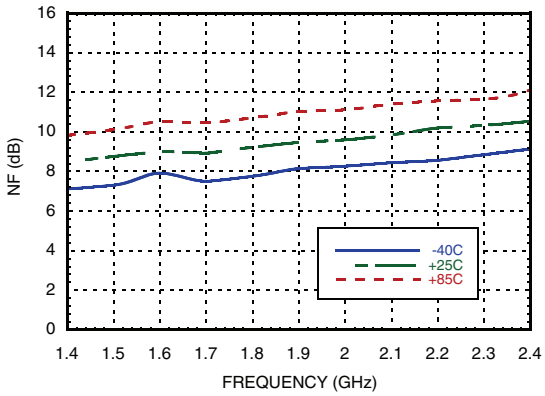
Input IP3 vs. Frequency [1]



Output P1dB vs. Frequency [1] [2]



Noise Figure vs. Frequency [1] [2]



[1] ATTN1 + AMP1 + AMP2
[2] VCTRL=Minimum Attenuation

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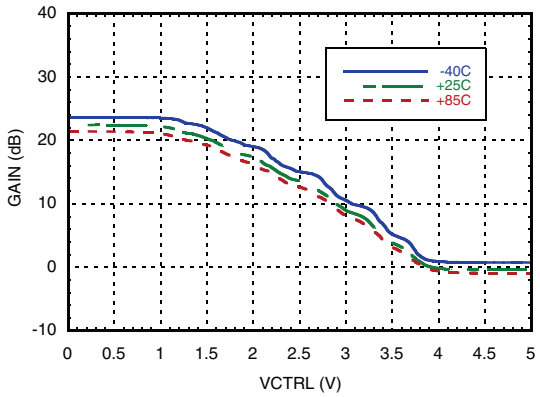
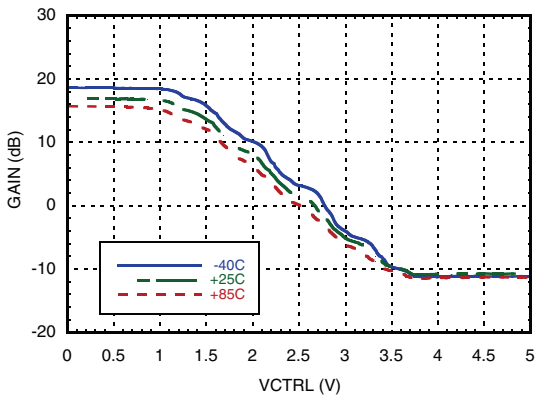
2400MHz TUNE

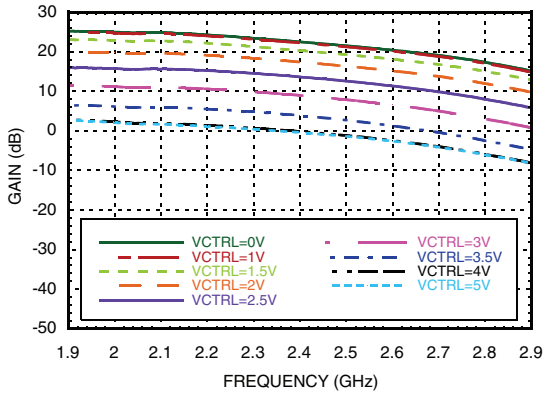
Gain vs. VCTRL [1]



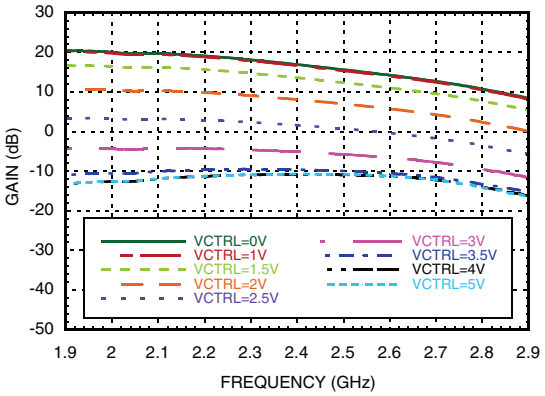
Gain vs. VCTRL [2]



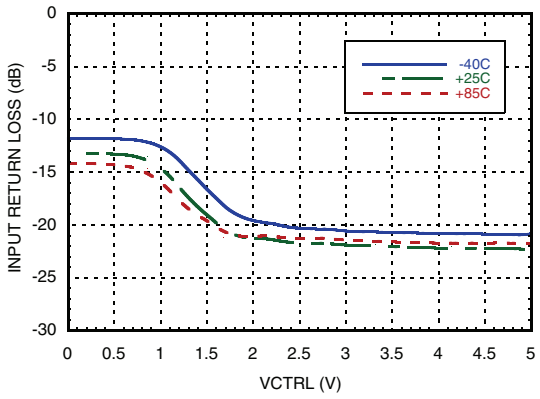
Gain vs. Frequency [1]



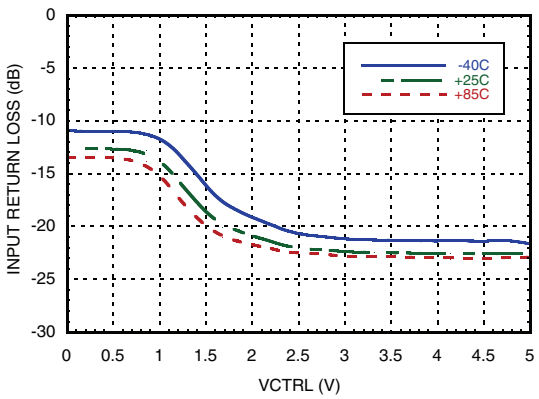
Gain vs. Frequency [2]



Input Return Loss vs. VCTRL [1]



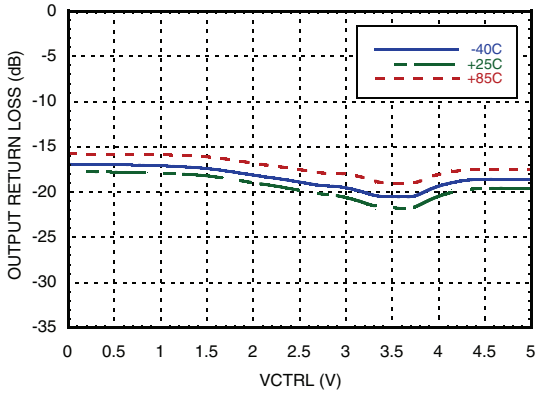
Input Return Loss vs. VCTRL [2]



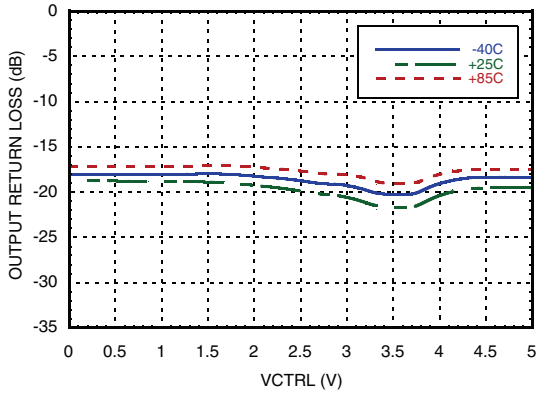
[1] ATTN1 + AMP1 + AMP2
[2] ATTN1 + ATTN2 + AMP1 + AMP2

2400MHz TUNE

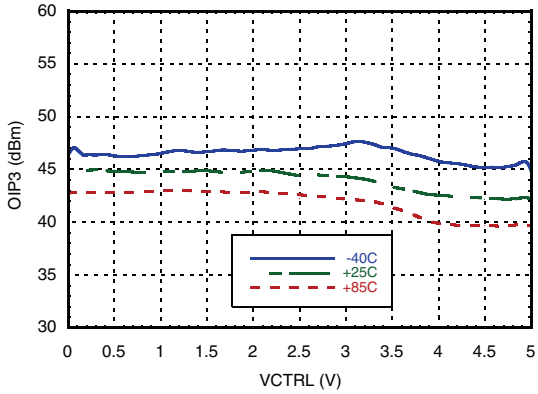
Output Return Loss vs. VCTRL [1]



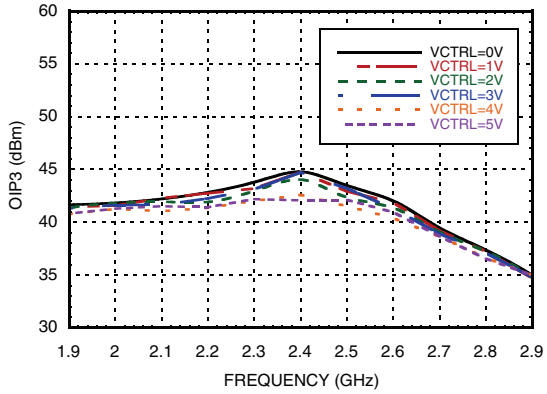
Output Return Loss vs. VCTRL [2]



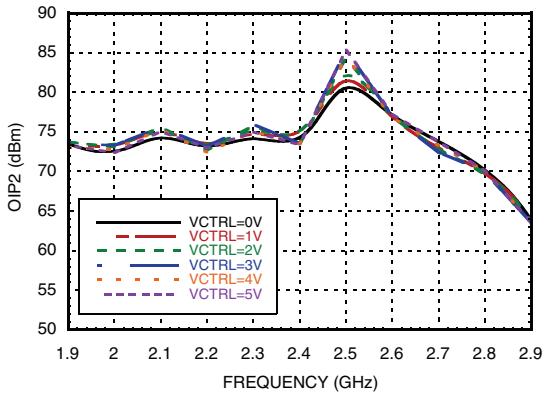
Output IP3 vs. VCTRL [1]



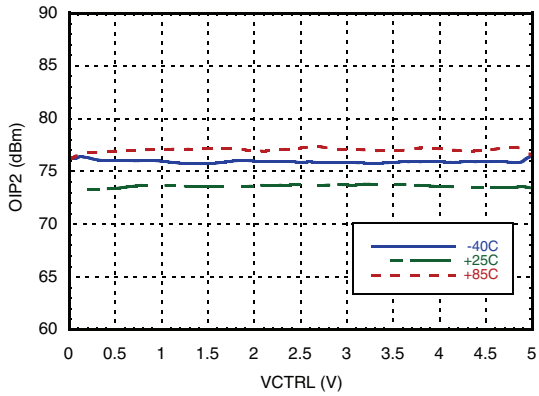
Output IP3 vs. Frequency [1]



Output IP2 vs. Frequency [1] [3]



Output IP2 vs.VCTRL [1]



[1] ATTN1 + AMP1 + AMP2
[2] ATTN1 + ATTN2 + AMP1 + AMP2

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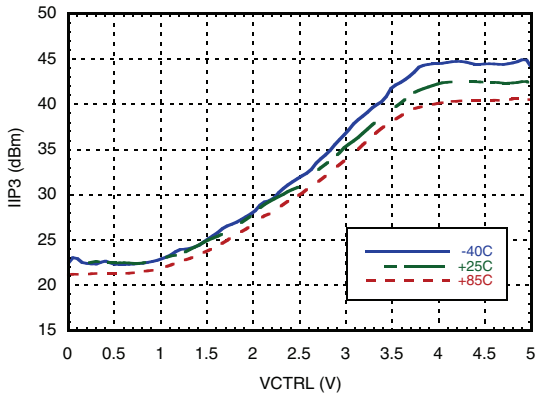
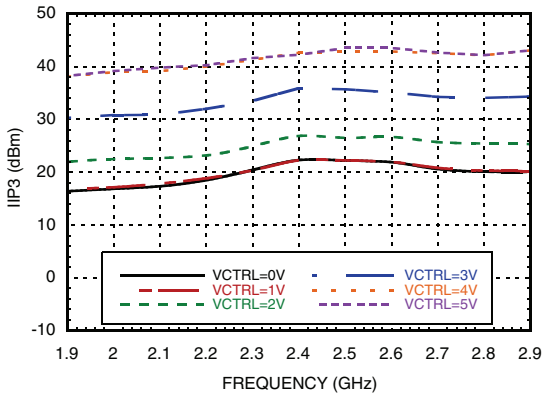
2400MHz TUNE

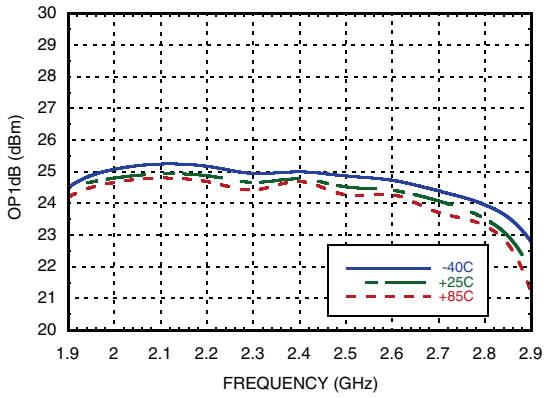
Input IP3 vs.VCTRL [1]



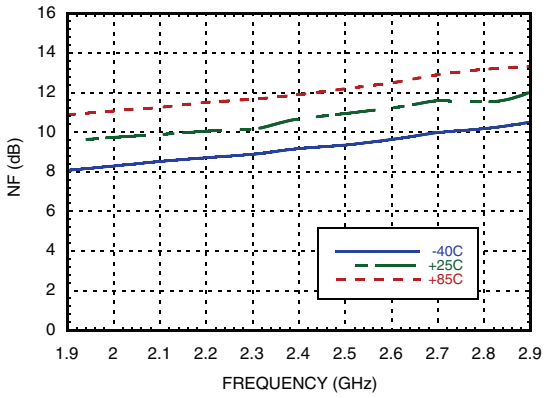
Input IP3 vs. Frequency [1]



Output P1dB vs. Frequency [1] [2]



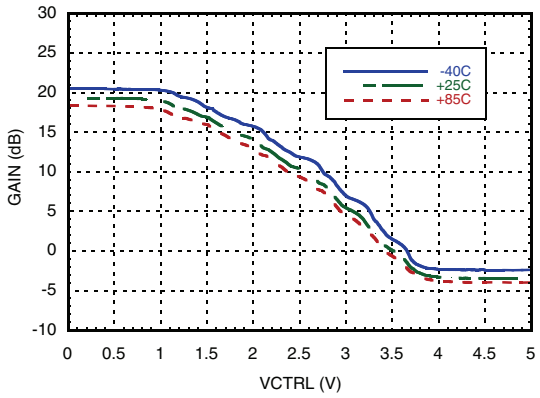
Noise Figure vs. Frequency [1] [2]



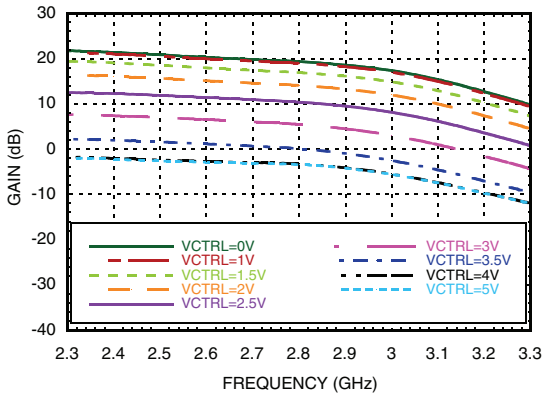
[1] ATTN1 + AMP1 + AMP2
[2] VCTRL=Minimum Attenuation

2800MHz TUNE

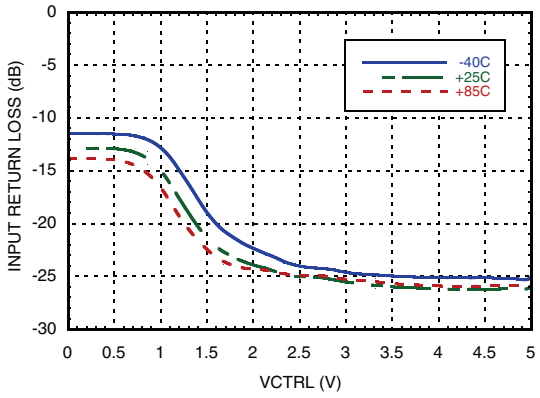
Gain vs. VCTRL [1]



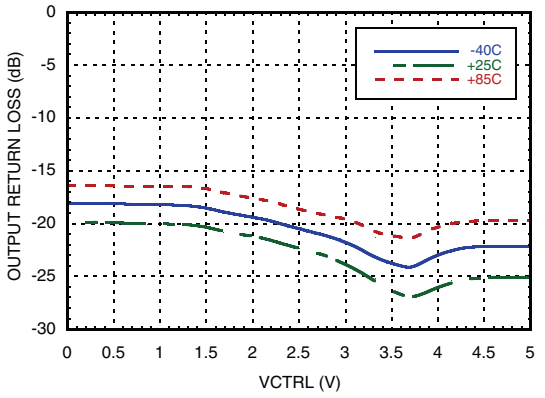
Gain vs. Frequency [1]



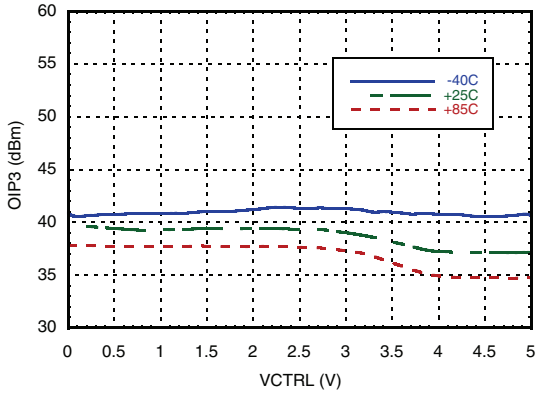
Input Return Loss vs. VCTRL [1]



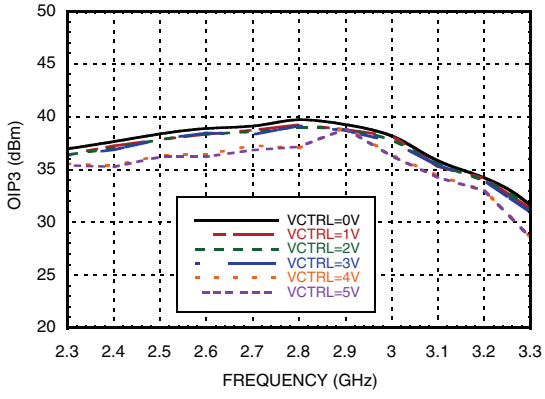
Output Return Loss vs. VCTRL [1]



Output IP3 vs. VCTRL [1]



Output IP3 vs. Frequency [1]



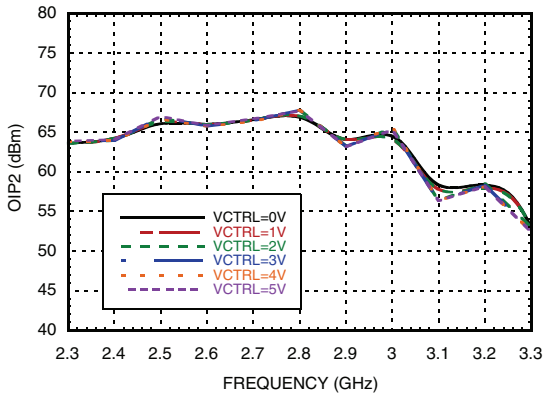
[1] ATTN1 + AMP1 + AMP2

HMC993LP5E

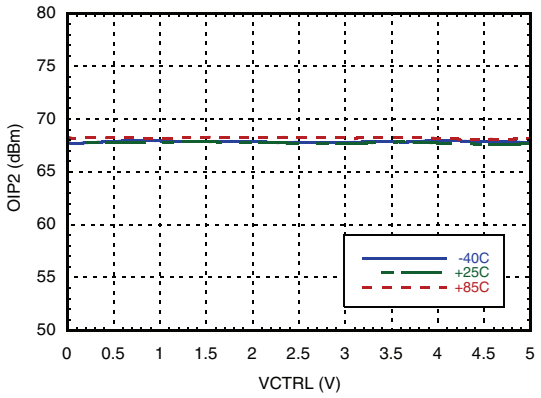
RF AUTOMATIC GAIN CONTROLLER (RF-AGC), 700 - 3000 MHz

2800MHz TUNE

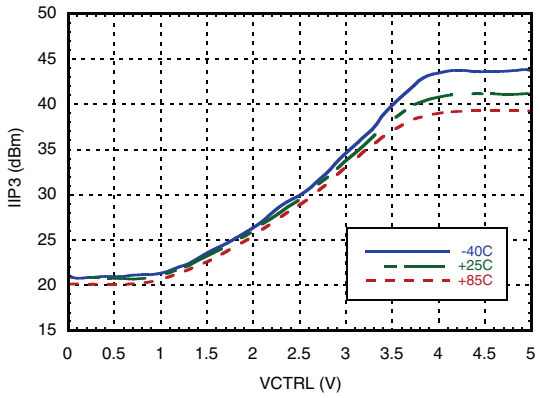
Output IP2 vs. Frequency [1]



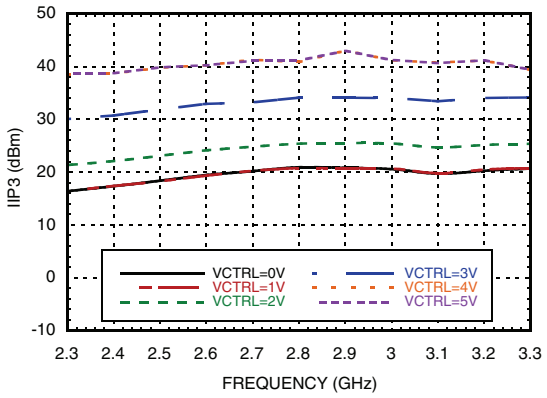
Output IP2 vs.VCTRL [1]



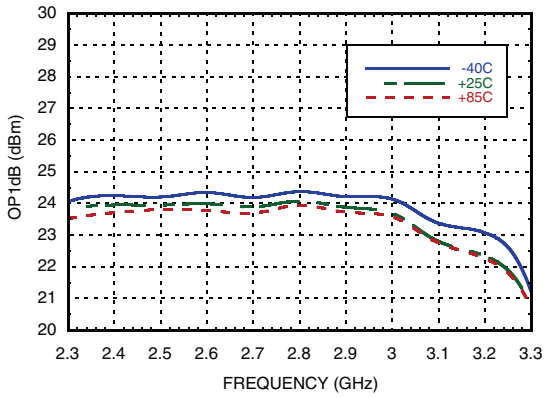
Input IP3 vs.VCTRL [1]



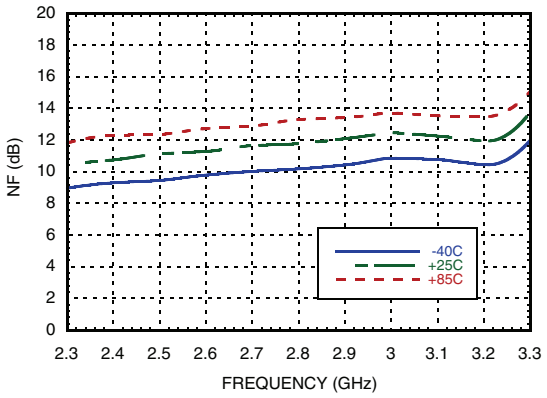
Input IP3 vs. Frequency [1]



Output P1dB vs. Frequency [1] [2]



Noise Figure vs. Frequency [1] [2]



[1] ATTN1 + AMP1 + AMP2
[2] VCTRL=Minimum Attenuation

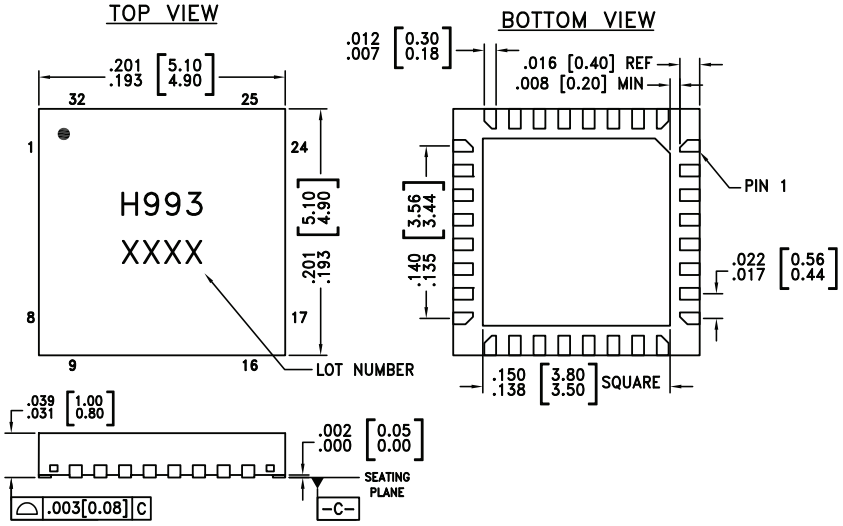
Absolute Maximum Ratings

VDD, DETVDD, DETEN, DETSET,DETRSSI, AMP1OUT, AMP2OUT	+5.6 V
VCTRL	-0.6V to VDD+0.6V
ATTN1IN, ATTN2IN Input Power	+20 dBm
AMP1IN RF Input Power	+8 dBm
AMP2IN RF Input Power	+18 dBm
DETOUT Output Current	5 mA
DETIN RF Iput Power	12 dBm
Junction Temperature	125°C

Continuous Pdiss (T=85 °C) Derate 41.8 mW/°C above 85 °C	1.7 W
Thermal Resistance (R_{th}) (junction to package bottom)	23.9°C/W
Storage Temperature	-65 to +150°C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

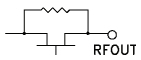
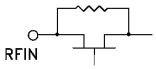
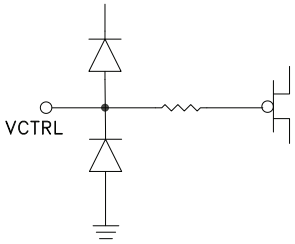
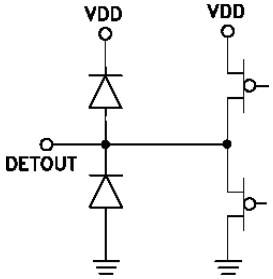
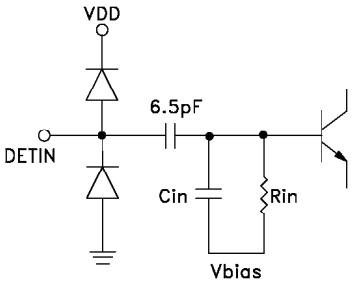
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

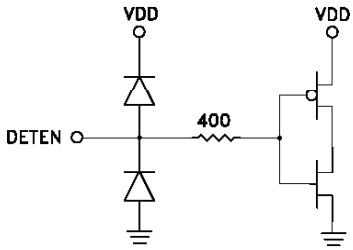
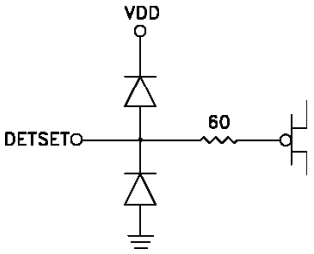
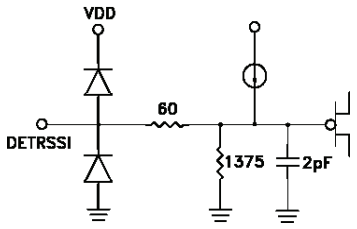
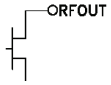
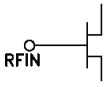
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC993LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H993 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

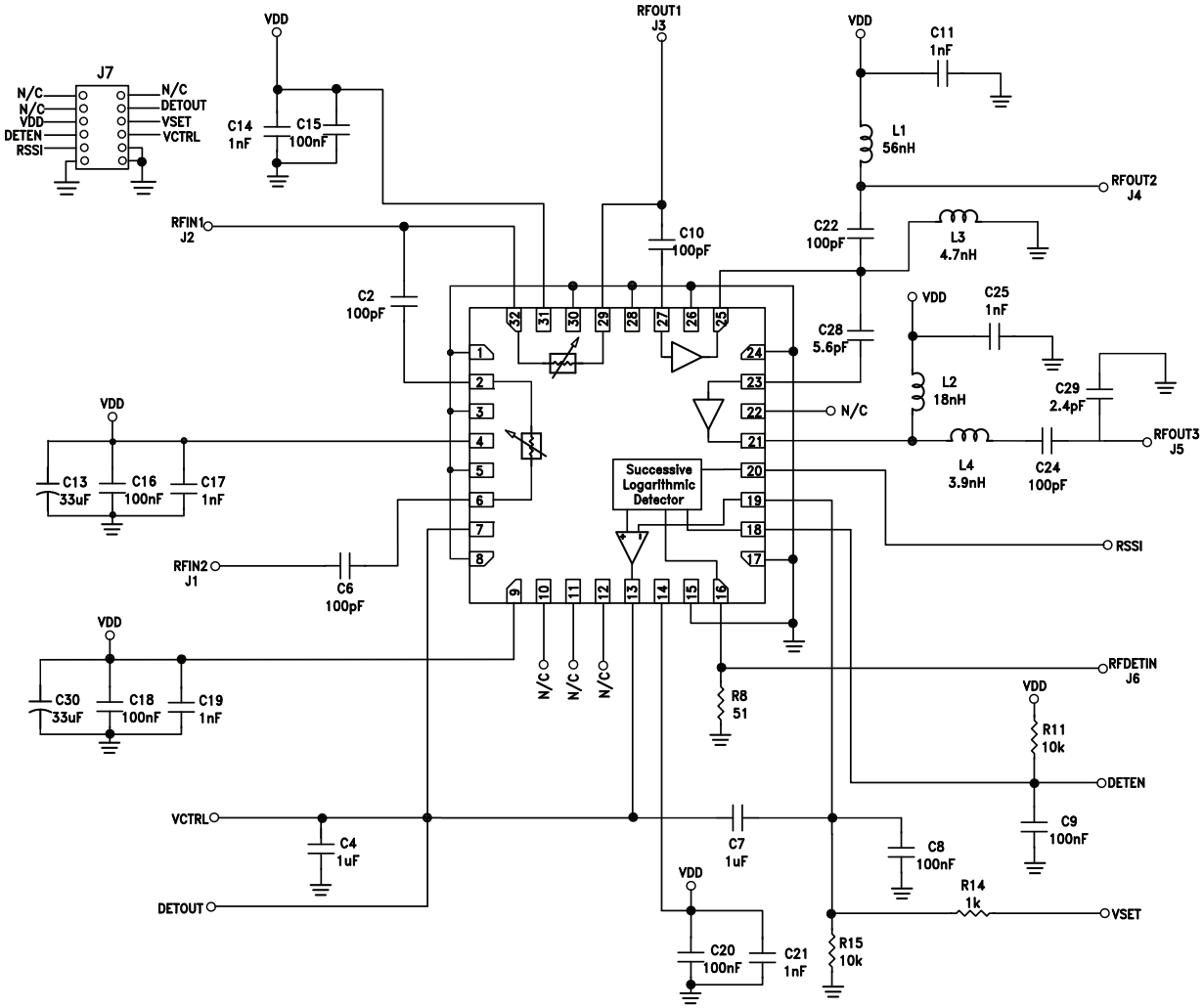
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 5, 8, 15, 17, 24, 26, 28, 30	GND	These pins and package bottom must be connected to RF ground.	
2, 29	ATTN2OUT, ATTN1OUT	These ports are matched to 50 Ohms. Blocking capacitor is required.	
4, 9, 31	VDD	Power supply for the attenuator. External bypass capacitors are required. See application circuits.	
6, 32	ATTN2IN, ATTN1IN	These ports are matched to 50 Ohms. Blocking capacitor is required.	
7	VCTRL	Attenuation control voltage for the attenuator. 0V for minimum attenuation, 5V for maximum attenuation.	
10, 11, 12, 22	N/C	No connection required. These pins may be connected to RF ground without affecting performance.	
13	DETOUT	Logarithmic output that converts the input power to a DC level in detector mode. Output voltage increases with increasing amplitude.	
14	DETVDD	Power supply for the logarithmic detector. External by pass capacitors are required. See application circuit.	
16	DETIN	Detector RF input pin.	

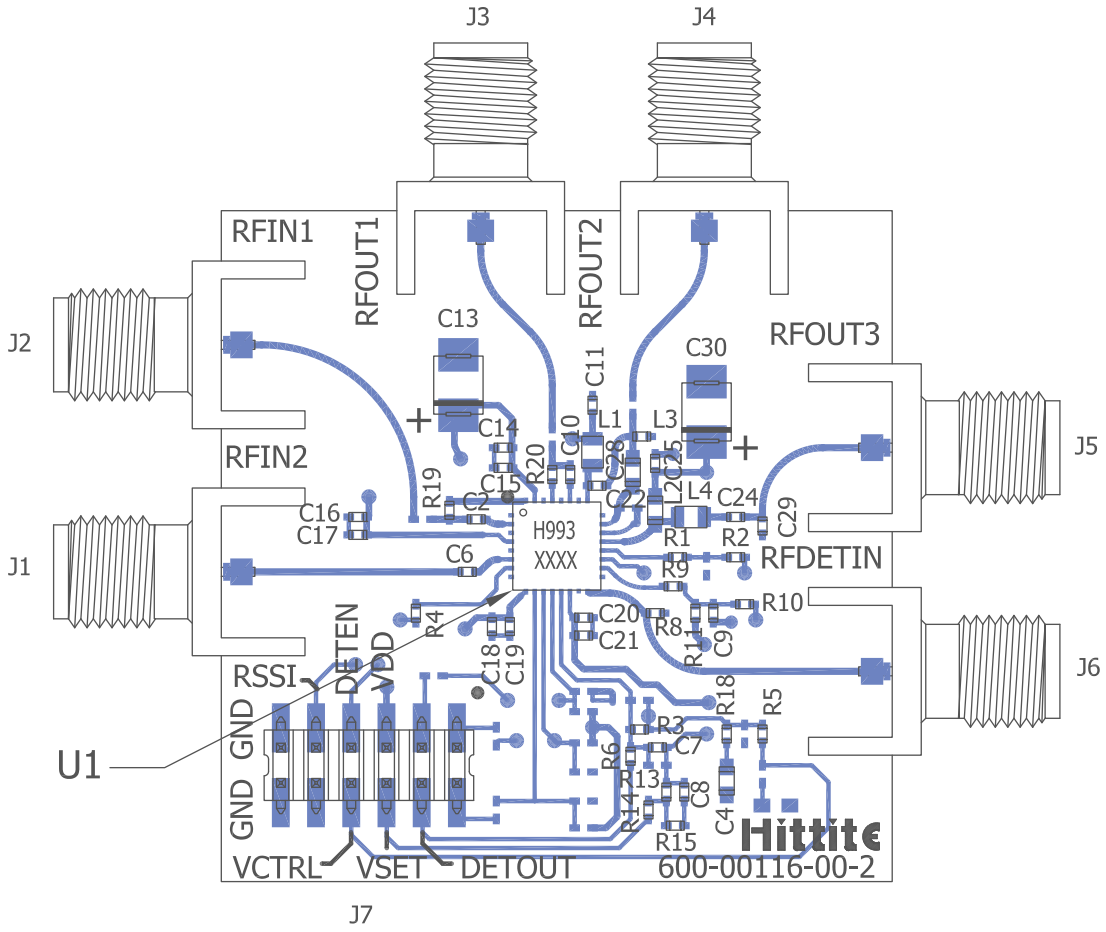
Pin Descriptions *(continued)*

Pin Number	Function	Description	Interface Schematic
18	DETEN	Enable pin. Apply VEN > 0.8xVcc for normal operation. Apply VEN < 0.2xVcc to disable the detector.	
19	DETSET	Set point input for controller mode. Connect to DETOUT with the resistor network shown in evaluation board drawing for detector mode.	
20	DETRSSI	Connection for ground referenced external lowpass filter capacitor.	
21, 25	AMP2OUT, AMP1OUT	These ports are mathed to 50 Ohms. External Choke inductor and DC blocking capacitor are required. See application circuits.	
23, 27	AMP2IN, AMP1IN	These ports are matched to 50 Ohms. Blocking capacitor is required.	

Application Circuit - 900 MHz



Evaluation PCB - 900 MHz



List of Materials for Evaluation PCB EVAL01-HMC993LP5E[1]

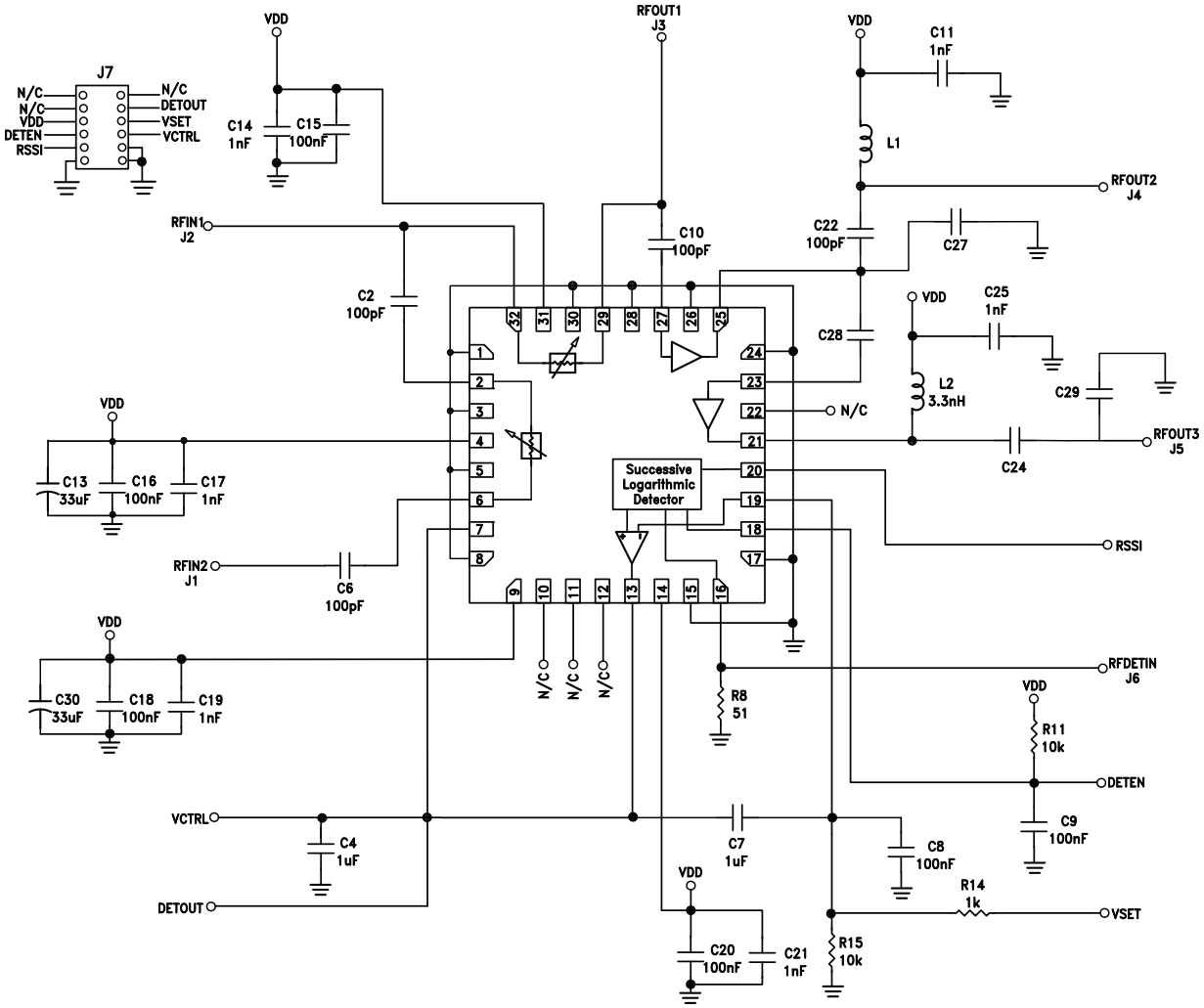
Item	Description
J1-J6	SMA Connector
J7	DC Connector Header
C2, C6, C10, C22, C24	100 pF Capacitor, 0402 Pkg.
C4	1 µF Capacitor, 0603 Pkg.
C7	1 µF Capacitor, 0402 Pkg.
C8-C9, C15-C16, C18, C20	0.1 µF Capacitor, 0402 Pkg.
C11, C14, C17, C19, C21, C25	1000 pF Capacitor, 0402 Pkg.
C13, C30	33 µF Capacitor, Tantalum
C28	5.6 pF Capacitor, Ultra Low ESR, 0603 Pkg.
C29	2.4 pF Capacitor, Ultra Low ESR, 0402 Pkg.
L1	56 nH Inductor, 0603 Pkg.
L2	18 nH Inductor, 0603 Pkg.
L3	4.7 nH Inductor, 0402 Pkg.

Item	Description
L4	3.9 nH Inductor, 0603 Pkg.
R1-R6, R9-R10, R13, R18-R20	0 Ohm Resistor, 0402 Pkg.
R8	51 Ohms Resistor, 0402 Pkg.
R11, R15	10 kOhms Resistor, 0402 Pkg.
R14	1 kOhms Resistor, 0402 Pkg.
U1	HMC993LP5E RF-Automatic Gain Controller
PCB [2]	600-00116-00 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25 FR

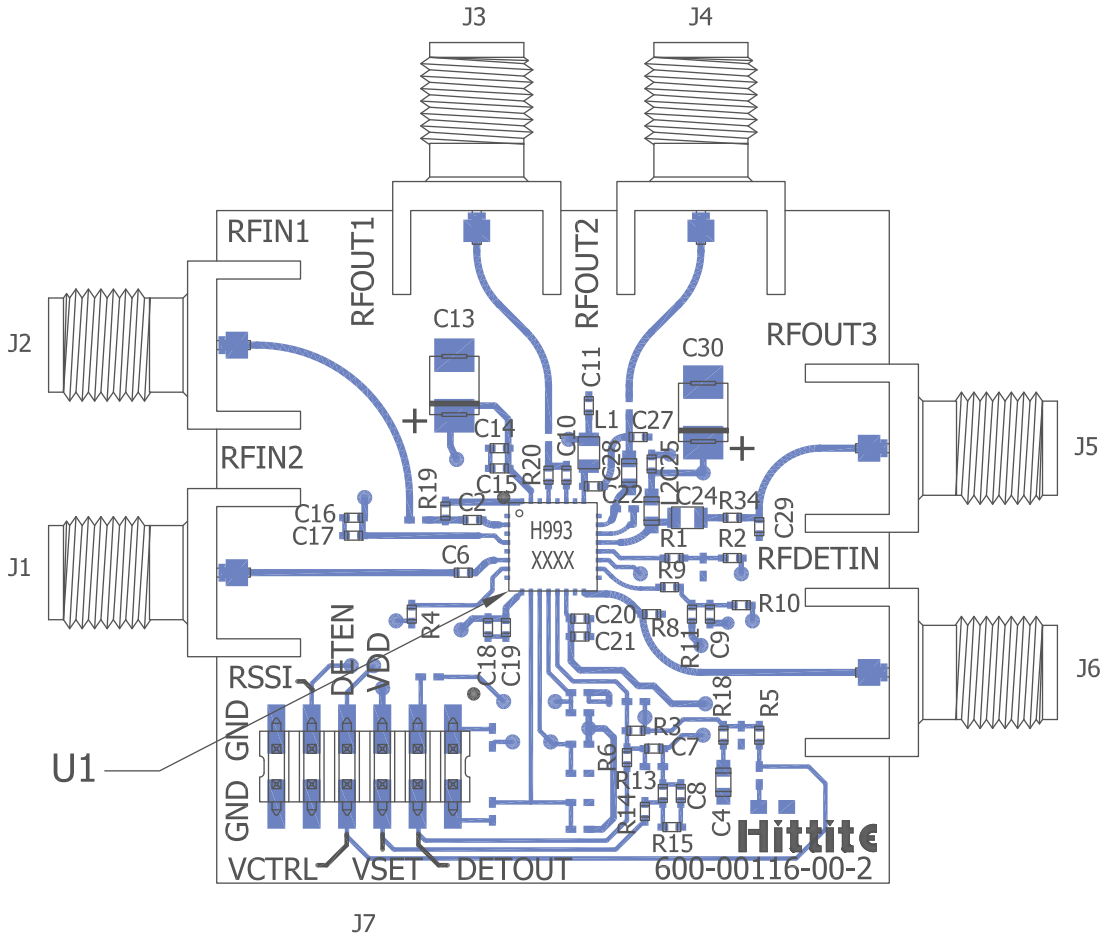
Application Circuit - 1900, 2400 & 2800 MHz



Components for Selected Frequency Values

Tune Option	Evaluation PCB Number	C24	C27	C28	C29	L1
1900 MHz	EVAL02-HMC993LP5E	15 pF	2.7 pF	6.8 pF	1.2 pF	24 nH
2400 MHz	EVAL03-HMC993LP5E	10 pF	1.6 pF	3.0 pF	0.8 pF	15 nH
2800 MHz	EVAL04-HMC993LP5E	6.8 pF	1.5 pF	1.5 pF	0.7 pF	15 nH

Evaluation PCB - 1900, 2400 & 2800 MHz



List of Materials for Evaluation PCB [1]

Item	Description
J1-J6	SMA Connector
J7	DC Connector Header
C2, C6, C10, C22	100 pF Capacitor, 0402 Pkg.
C4	1 µF Capacitor, 0603 Pkg.
C7	1 µF Capacitor, 0402 Pkg.
C8-C9, C15-C16, C18, C20	0.1 µF Capacitor, 0402 Pkg.
C11, C14, C17, C19, C21, C25	1000 pF Capacitor, 0402 Pkg.
C13, C30	33 µF Capacitor, Tantalum
C24	Capacitor, Ultra Low ESR, 0603 Pkg.
C27	Capacitor, Ultra Low ESR, 0402 Pkg.
C28	Capacitor, Ultra Low ESR, 0603 Pkg.
C29	Capacitor, Ultra Low ESR, 0402 Pkg.
L1	Inductor, 0603 Pkg.
L2	3.3 nH Inductor, 0603 Pkg.

Item	Description
R1-R6, R9-R10, R13, R18-R20, R34	0 Ohm Resistor, 0402 Pkg.
R8	51 Ohms Resistor, 0402 Pkg.
R11, R15	10 kOhms Resistor, 0402 Pkg.
R14	1 kOhms Resistor, 0402 Pkg.
U1	HMC993LP5E RF-Automatic Gain Controller
PCB [2]	600-00116-00 Evaluation PCB

[1] When requesting an evaluation board, please reference the appropriate evaluation PCB number listed in the table “Components for Selected Frequency Tune”

[2] Please refer to “Components for Selected Frequency Tune” table for values

[3] Circuit Board Material: Rogers 4350 or Arlon 25 FR

Application Information

Introduction

The HMC993LP5E is a complete high performance Automatic Gain Control (AGC) solution, housing a Variable Gain Amplifier (VGA) core and a control core in a single package. Its unique VVA technology provides constant OIP3 over the entire control voltage range. The HMC993LP5E greatly simplifies the design of gain control loops by increasing the integration level and reducing the number of required circuit elements. The VGA core of the HMC993LP5E is composed of two identical voltage variable attenuators followed by two gain block amplifiers which operate from 0.7 to 3.0 GHz. The HMC993LP5E's control core features a high accuracy log detector. As shown in the functional block diagram, the HMC993LP5E combines all of these cores in a highly compact 5 x 5 mm plastic package, and offers an easy-to-use, temperature stable AGC solution.

The HMC993LP5's VGA core has a flexible structure where a single attenuator (22.2 dB at 1900 MHz) or two attenuators (33.6 dB at 1900 MHz) can be used depending upon the dynamic range requirement. Inputs and outputs of the HMC993LP5E's attenuators and first amplifier (ATTIN1, ATTOUT1, ATTIN2, ATTOUT2, AMPIN1, AMPOUT1) are broadband matched to 50 Ohm single-ended and require only external DC blocking capacitors over the entire frequency band of operation. The input of the HMC993LP5E's log detector (RFDETIN) is also broadband matched to 50 Ohm single-ended and does not require any matching components. Input and output of the HMC993LP5E's second amplifier (AMPIN2, AMPOUT2) need power matching components for key application frequencies. Refer to application circuits for example application frequencies.

The HMC993LP5E requires a single 5V supply with adequate power supply decoupling as recommended in the application schematics.

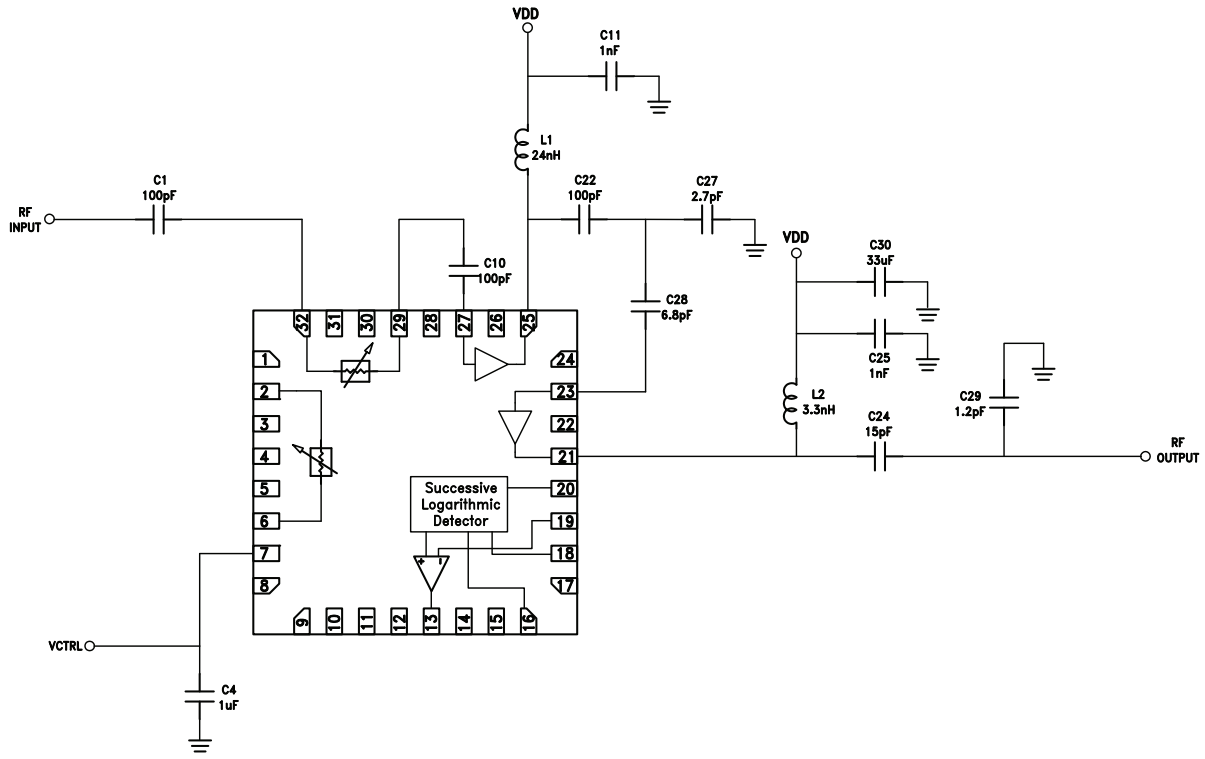


Figure 1a: The HMC993LP5E's VGA configuration with 1 attenuator, 1900 MHz tune.

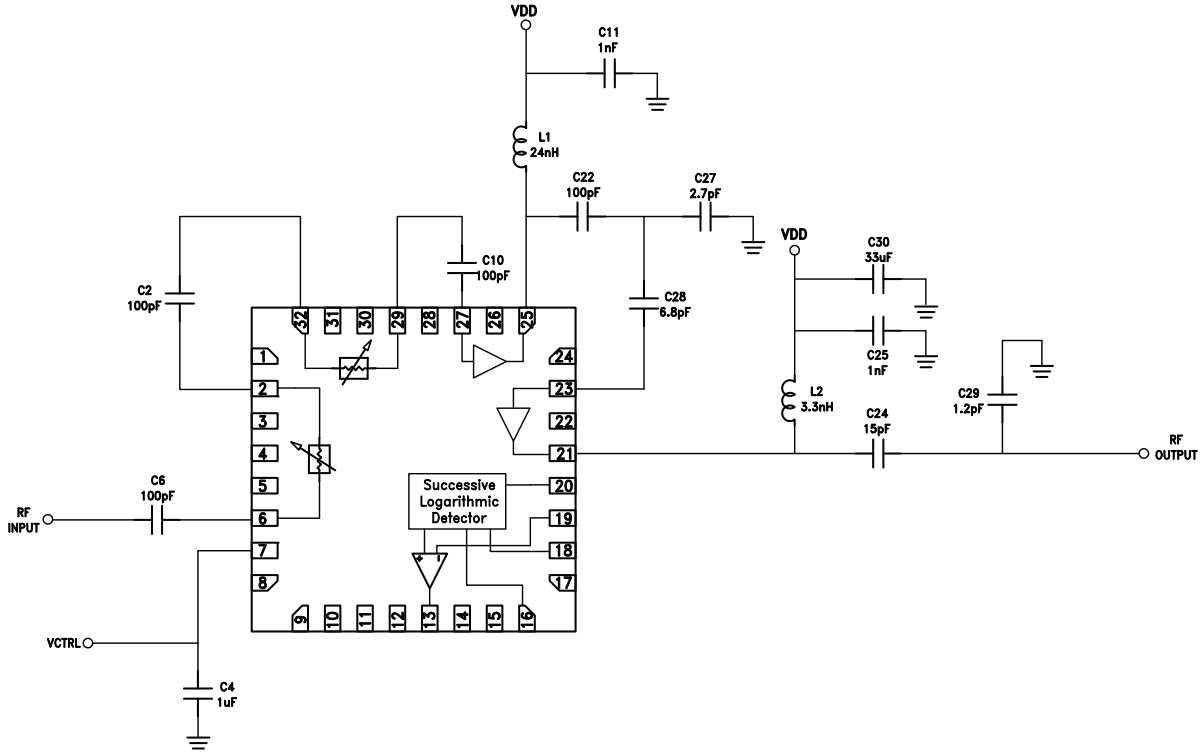


Figure 1b: The HMC993LP5E's VGA configuration with 2 attenuators, 1900 MHz tune.

VGA Operation

The HMC993LP5E's VGA core can be configured with one or two variable attenuators followed by two fixed gain amplifiers for different control ranges as shown in Figure 1a and Figure 1b (basic connections are not shown). Note that the link between VCTRL and DETOUT pins must be broken for correct VGA Operation. The VCTRL pin should be used to set the attenuation of the HMC993LP5E.

Gain Control Interface VCTRL

The VCTRL pin is the gain control pin common to both of HMC993LP5E's identical voltage variable attenuators. The VCTRL gain control voltage ranges between 1V and 4V. A VCTRL control voltage of 1V provides the lowest attenuation, while 4V provides the highest attenuation.

Figure 2 represents the VGA operation of HMC993LP5E with two attenuators and two amplifiers for different gain control voltages applied to the VCTRL pin. The output power increases linearly with the input power until the power saturation is reached when the VCTRL voltage is constant. The useable input power range of such a system is limited by the saturation level of the final stage amplifier. So the input power level required for power saturation and the dynamic range of the HMC993LP5E's VGA is defined by the value of the gain control voltage applied to the VCTRL pin. Refer to the Figure 2 for the useable input power range at different VCTRL levels.

When VCTRL=1V, the gain of HMC993LP5E's VGA with 2 attenuators is 21.5 dB at 1900 MHz. The input power required for 1 dB compression point at the output is given by: Pin1dB = Pout1dB – Gain (dB) + 1 = 25 – 21.5 + 1 = 4.5 dB.

When VCTRL=2V, the gain of the HMC993LP5E's VGA with 2 attenuators is 11.7 dB at 1900 MHz. The input power required for 1 dB compression point at the output is given by: Pin1dB = Pout1dB – Gain (dB) + 1 = 25 – 11.7 + 1 = 14.3 dB.

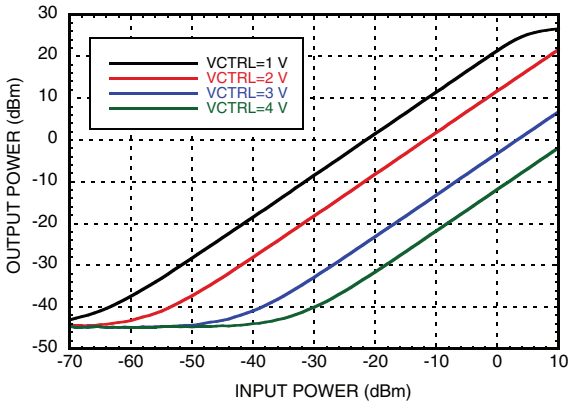


Figure 2: Pout vs. Pin at 1900 MHz, 1 attenuator

Therefore, increasing the VCTRL pin voltage reduces the gain of the HMC993LP5E's VGA and increases input power level required for power saturation. When the input signal is weak, the attenuation level of the variable attenuators should be reduced. When the input signal is large; the attenuation level of the variable attenuators should be increased to achieve a constant output level.

The gain control performance of the HMC993LP5E at 1900 MHz is shown in Figures 3. The HMC993LP5E provides 22.2 dB of gain control range with a maximum gain of 26 dB when it is configured in 1 attenuator + 2 amplifiers mode, and similarly a 33.6 dB of gain control range with a maximum gain of 21.5 dB of gain when it is configured in 2 attenuators + 2 amplifiers mode. The HMC993LP5E's VGA has a very flat linear-in-dB gain control characteristic with a slope of -12.97 dB/V for the 2 attenuators configuration and -7.28 dB/V for the 1 attenuator configuration. The log-linearity error of the HMC993LP5 VGA is typically less than ± 2dB over the entire gain control range.

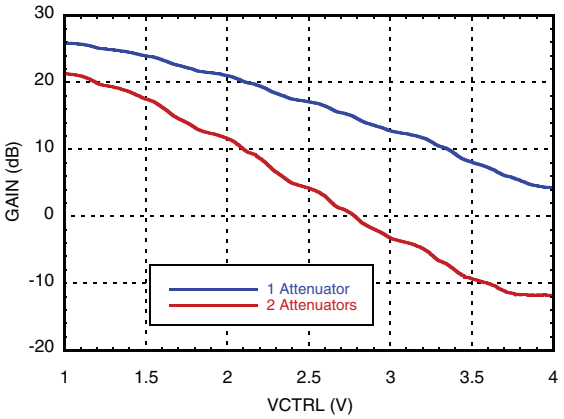


Figure 3: Gain vs. VCTRL at 1900 MHz

Noise and Distortion

As with any multistage VGA consisting of voltage variable attenuators and gain blocks, the noise figure (NF) and input referred distortion (IIP3) characteristics of the HMC993LP5E's VGA are dependent on the gain control voltage VCTRL. When the attenuation level of the variable attenuators is set to minimum (maximum gain state), the noise figure of the HMC993LP5E's VGA is minimized; however the IIP3 is degraded to minimum as well. The noise figure and IIP3 of the HMC993LP5E's VGA increases with the attenuation level of the variable attenuators.

For low attenuation levels, the noise contribution from the VGA is important since the input signal is weak. For high atten-

uation levels of the variable attenuators, the noise contribution from the VGA is less important and the noise requirement of the VGA is relaxed since the input signal is high. The noise figure performance of the HMC993LP5E's VGA at 1900 MHz is shown in Figure 4. The HMC993LP5E's VGA delivers a noise figure of 9.8 dB in its maximum gain state when it is configured in 1 attenuator + 2 amplifiers mode.

For low attenuation levels of the variable attenuators, IIP3 is less important since high gain of whole VGA improves distortion performance at its output (OIP3). For high attenuation levels of the variable attenuators, IIP3 is more important because of low gain of whole VGA. The distortion performance of the HMC993LP5E's VGA at 1900 MHz is shown in Figure 4. The HMC993LP5E's VGA provides an almost constant OIP3 of up to +45 dBm in any state when it is configured in one attenuator and two amplifiers mode.

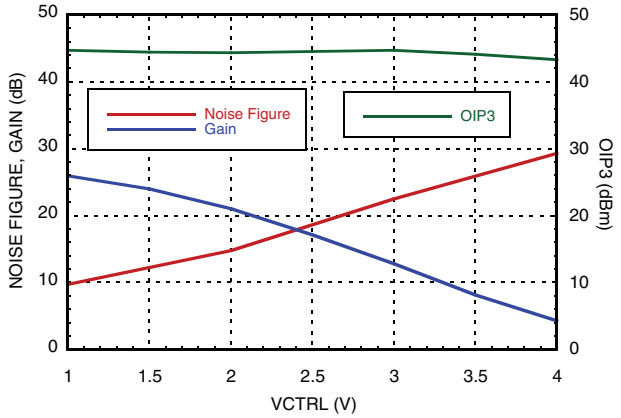


Figure 4: Noise Figure & Gain & OIP3 vs. VCTRL at 1900 MHz, 1 attenuator.

AGC Operation

The HMC993LP5E can be configured as an AGC amplifier by using VGA core and the built in log detector. An example for AGC amplifier configuration of the HMC993LP5E is depicted in Figure 5.

In AGC amplifier configuration, the input signal is amplified by the HMC993LP5E's VGA. The output of the HMC993LP5E's VGA core is fed back to the input of the HMC993LP5E's log detector (RFDETIN) through an external coupler or attenuator to drop the maximum and minimum output level of the HMC993LP5E's VGA to within the dynamic range of the HMC993LP5E's log detector. The HMC993LP5E's log detector produces a voltage at the output of the log detector (DETOUT) proportional to the output power level of the HMC993LP5E's VGA. The high impedance output pin DETOUT is connected to the gain control pin VCTRL of VGA to form the AGC loop. The VSET pin is the constant output power set point of the AGC amplifier. As a result of negative feedback, the gain of the VGA is automatically adjusted to maintain a constant signal power level at the output of AGC amplifier. The output signal power level is determined by the AGC set point VSET, regardless of the input signal variation.

AGC Set point Interface VSET

In closed loop AGC operation the output power level of the HMC993LP5E is controlled by the VSET pin. An input voltage between 0.2V and 1.2V should be applied to the VSET input pin to control the output power level. Output power vs. VSET characteristic is shown in Figure 6a and Figure 6b for different input power levels and different coupler ratios used. The slope of the gain vs. VSET characteristic is 58.3dB/V and it is independent of the coupler ratio used.

The relation between the gain of HMC993LP5E's output power and VSET pin voltage at 1900 MHz can be approximated as given in Equation (1) when it is configured in AGC amplifier configuration with 2 attenuator + 2 amplifiers.

$$\text{Output Power (dBm)} = -67.7 + |\text{Coupler Ratio}| + 58.3 \times \text{VSET} \qquad \text{Equation (1)}$$

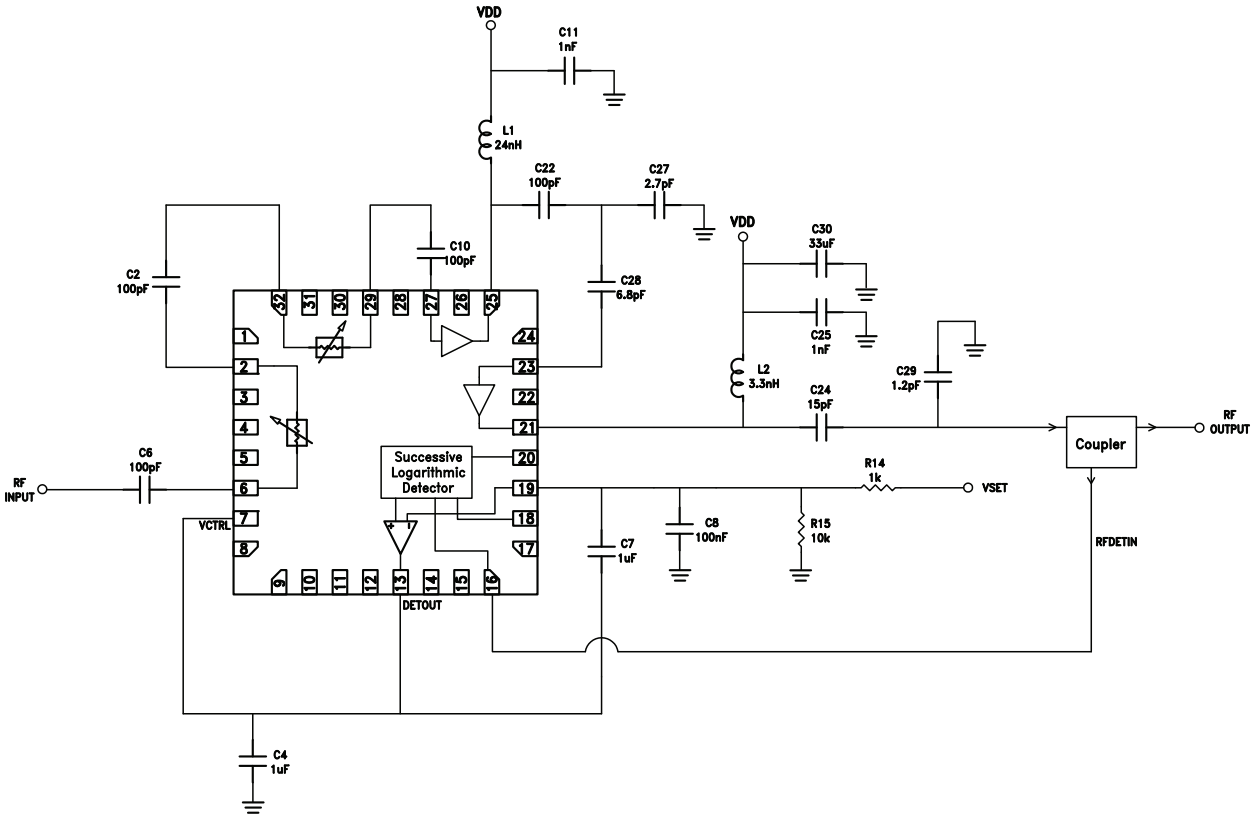


Figure 5: The HMC993LP5E's AGC configuration with 2 attenuators, 1900 MHz tune.

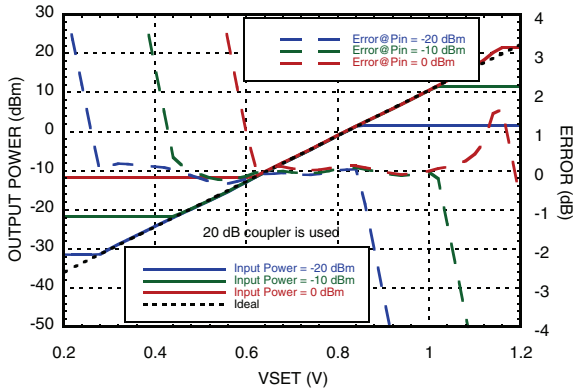


Figure 6a: Output Power vs. VSET over Input Power, 2 attenuators @ 1900 MHz.

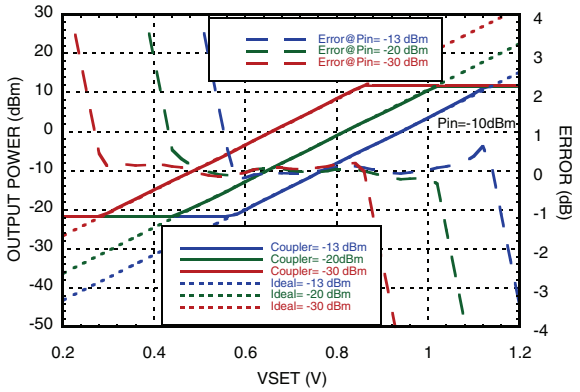


Figure 6b: Output Power vs. VSET over coupler ratio, 2 attenuators @ 1900 MHz.

In closed loop operation the HMC993LP5E is able to automatically adjust the RF gain over a gain adjustment range of up to 33.6 dB at 1900 MHz. The HMC993LP5E's output dynamic range is a function of both input power level and the coupler ratio used to close the AGC loop. The combined effect of the input power and coupler ratio on the output power dynamic range is presented in Figures 6a and 6b.

For high input power levels, the maximum level of output dynamic range is limited by the Psat of the VGA or the highest detectable power level by the log detector. To eliminate any limitations that can arise due to highest detectable log

detector, a high enough coupler ratio should be chosen to translate the maximum VGA output power level to a value lower than the highest detectable log detector power level.

Similarly, the lower side of the dynamic range is limited by the noise floor of the VGA or the lowest power level detectable by the log detector. To eliminate any limitations on the lower side of the dynamic range, the coupler ratio should be low enough to translate the minimum VGA output power level to a value higher than the lowest detectable log detector power level.

Please also refer to the Log Detector section for more information.

Figure 7a shows the output power vs. input power transfer characteristic of the HMC993LP5E over different VSET voltages for a closed AGC loop configuration. For low and high input power levels the HMC993LP5E attenuation rage is saturated and the output is a linear function of the input. For input power levels within the dynamic range, the HMC993LP5E automatically adjusts the attenuation level as shown in Figure 7b to maintain a constant output power level. When Vset=0.5 V, the output power level is set to -18.7 dBm and the HMC993LP5E's AGC amplifier provides a gain control range of 33.6 dB from -40.2 dBm to -6.6 dBm with an excellent ripple within 0.7 dB.

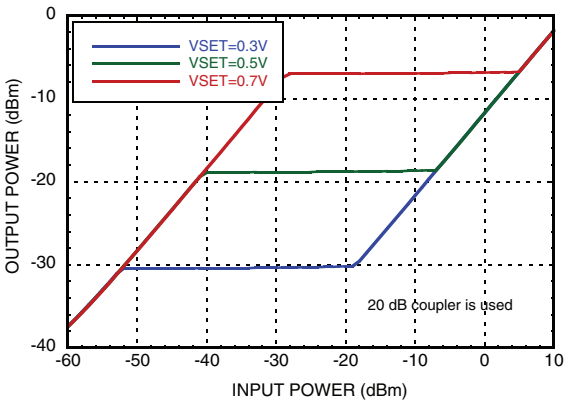


Figure 7a: Output Power vs. input power over VSET, 2 attenuators @ 1900 MHz.

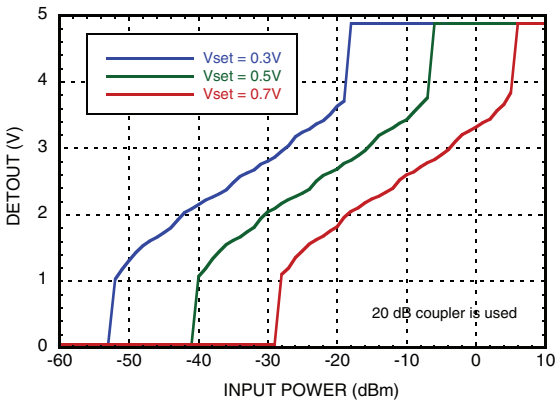


Figure 7b: DETOUT vs. input power over VSET, 2 attenuators @ 1900 MHz..

Log Detector

The logarithmic detector of the HMC993LP5E converts the average envelope of RF input power to a proportional DC voltage at its output (DETOUT), as shown in Figure 8. In detection mode, the DETOUT pin should be connected to the VSET input. The HMC993LP5E's logarithmic detector employs a successive compression technology which delivers 50 dB of dynamic range (±1dB) with high conversion accuracy over a wide input frequency range. Note that the link between DETOUT and VCTRL pins must broken and DETOUT must connected to VSET via 1k Ohms resistor for LOGAMP operation.

The HMC993LP5E's logarithmic detector can be used in the controller mode where an external voltage is applied to the VSET pin to create an AGC loop. The linear-in-dB behavior of the HMC993LP5E's VGA and logarithmic detector creates a linear AGC system. For linear operation, the signal fluctuations at the input of the log detector should remain within the dynamic range of the log detector. In closed loop AGC operation, the HMC993LP5E's response to large input level changes is not slew-rate limited, and the speed of the transient response can be adjusted through loop filter capacitors C4 and C7 (see Figure 5).

To achieve maximum gain adjustment range of the HMC993LP5E, the coupler ratio should be chosen based on the output power desired. A coupler ratio which translates the output power to the center (~-25dBm) of the usable dynamic

range of the log detector should be chosen. The gain adjustment range of the HMC993L5E is maximized in this configuration.

If the linear operation range of the HMC993LP5E is maximized by selecting the appropriate coupler ratio, the HMC993LP5E can handle larger changes in input level. For example, an input voltage of 0.5 V is applied to the Vset pin to set the constant output power level to -18.7 dBm. A coupler ratio of ~7 dB can be chosen to provide a maximum dynamic range of 33.6 dB.

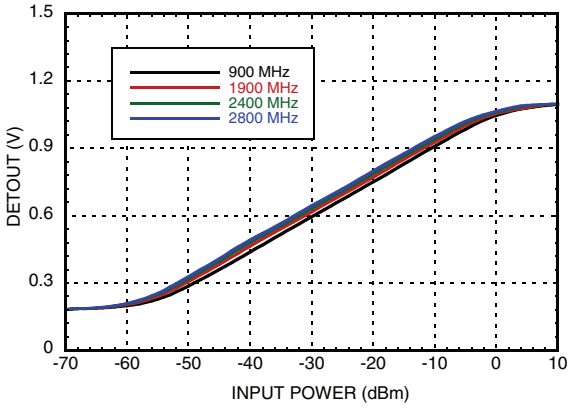


Figure 8: DETOUT vs. input power over frequency.

Loop Bandwidth and Response Time

The AGC system has a response time to undesired input level fluctuations. Response time and the stability of the HMC993LP5E's AGC loop is determined by C4 and C7 in the application schematic. The HMC993LP5E's response to voltage changes in VSET with C4=C7=1µF when the input level is kept constant is shown in Figure 9.

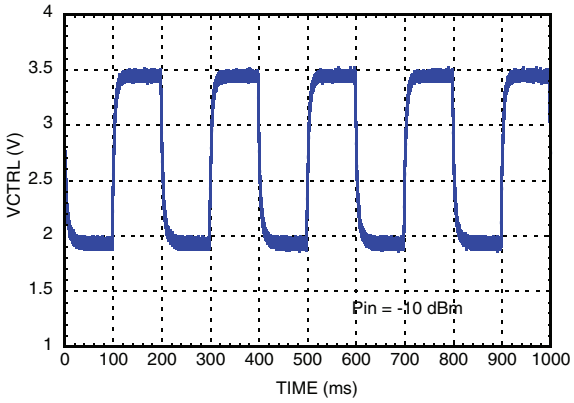


Figure 9: HMC993LP5E's gain control voltage when VSET is toggled between 0.3V - 0.7V and input level is kept constant in closed loop.