

HI-3182PSx-N, HI-3184PSx-N HI-3185PSx-N

May 2008

ARINC 429 Differential Line Driver

GENERAL DESCRIPTION

The HI-3182, HI-3184 and HI-3185 bus interface products are silicon gate CMOS devices designed as a line driver in accordance with the ARINC 429 bus specifications. In addition to being functional upgrades of Holt's HI-8382 product, they are also alternate sources for a variety of similar line driver products from other manufacturers.

Inputs are provided for clocking and synchronization. These signals are AND'd with the DATA inputs to enhance system performance and allow the HI-318X series of products to be used in a variety of applications. Both logic and synchronization inputs feature built-in 2,000V minimum ESD input protection as well as TTL and CMOS compatibility.

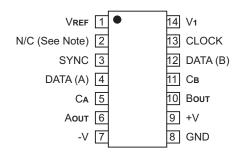
The differential outputs of the HI-318X series of products are programmable to either the high speed or low speed ARINC 429 output rise and fall time specifications through the use of two external capacitors. The output voltage swing is also adjustable by the application of an external voltage to the VREF input. A 37.5 ohm resistor is in series with each ARINC output. In addition the HI-3182 and HI-3184 products also have a fuse in series with each output.

The HI-318X series of line drivers are intended for use where logic signals must be converted to ARINC 429 levels such as when using an ASIC, the HI-8584/HI-3282/HI-8282A ARINC 429 Serial Transmitter/Dual Receivers, the HI-6010 ARINC 429 Transmitter/Receiver or the HI-8783 ARINC Interface Device. Holt products are readily available for both industrial and military applications. Please contact the Holt Sales Department for additional information.

FEATURES

- Low power CMOS
- . TTL and CMOS compatible inputs
- Programmable output voltage swing
- Adjustable ARINC rise and fall times
- Operates at data rates up to 100 Kbits
- · Overvoltage protection
- · Industrial and Military temperature ranges

PIN CONFIGURATION (Top View)

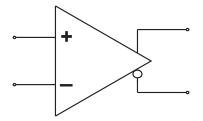


HI-3184PSx-N & HI-3185PSx-N 14-PIN PLASTIC NARROW SMALL OUTLINE (SOIC)

Note: Pin 2 not internally connected

(See Page 5 for HI-3182PSx-N package pin configurations)

FUNCTION



ARINC 429 DIFFERENTIAL LINE DRIVER

TRUTH TABLE

| SYNC | CLOCK | DATA(A) | DATA(B) | AOUT | BOUT | COMMENTS |
|------|-------|---------|---------|-------|-------|----------|
| Х | L | Х | Х | 0V | 0V | NULL |
| L | Х | Х | Х | 0V | 0V | NULL |
| Н | Н | L | L | 0V | 0V | NULL |
| Н | Н | L | Н | -VREF | +VREF | LOW |
| Н | Н | Н | L | +VREF | -VREF | HIGH |
| Н | Н | Н | Н | 0V | 0V | NULL |

FUNCTIONAL DESCRIPTION

The SYNC and CLOCK inputs establish data synchronization utilizing two AND gates, one for each data input (figure 2). Each logic input is TTL/CMOS compatible.

Figure 1 illustrates a typical ARINC 429 bus application. Three power supplies are necessary to operate the HI-318X; typically +15V, -15V and +5V. The chip also works with ±12V supplies. The +5V supply can also provide a reference voltage that determines the output voltage swing. The differential output voltage swing will equal 2VREF. If a value of VREF other than +5V is needed, a separate +5V power supply is required for pin V1.

With the DATA (A) input at a logic high and DATA (B) input at a logic low, AOUT will switch to the +VREF rail and BOUT will switch to the -VREF rail (ARINC HIGH state). With both data input signals at a logic low state, the outputs will both switch to OV (ARINC NULL state).

The driver output impedance, Rout, is nominally 75 ohms. The rise and fall times of the outputs can be calibrated through the selection of two external capacitor values that are connected to the CA and CB input pins. Typical values for high-speed operation (100KBPS) are CA = CB = 75pF and for low-speed operation (12.5 to 14KBPS) CA = CB = 500pF.

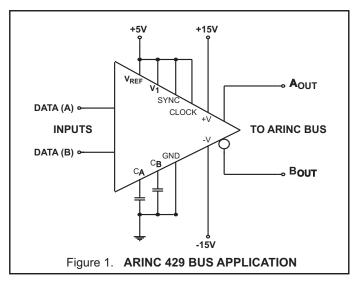
The CA and CB pins swing between +5V and ground allowing the switching of capacitor values with an external single-supply analog switch.

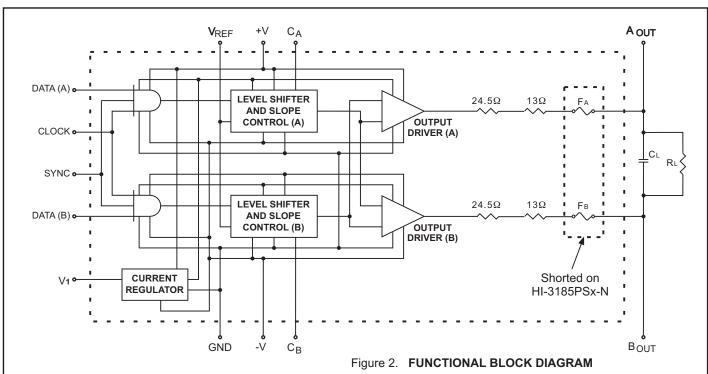
The ARINC outputs of the HI-3182 and HI-3184 are protected by internal fuses capable of sinking between 800 - 900 mA for short periods of time (125μ s).

The Vref pin has an internal pull-up resistor to V+, allowing the use of a simple external zener diode to set the reference voltage.

POWER SUPPLY SEQUENCING

The power supplies should be controlled to prevent large currents during supply turn-on and turn-off. The recommended sequence is +V followed by V1, always ensuring that +V is the most positive supply. The -V supply is not critical and can be asserted at any time.





PIN DESCRIPTIONS

| SYMBOL | FUNCTION | DESCRIPTION | |
|----------|----------|---|--|
| VREF | ANALOG | Ref. voltage used to determine output voltage swing. Pin sources current to allow use of a zener reference. | |
| SYNC | INPUT | Synchronizes data inputs | |
| DATA (A) | INPUT | Data input terminal A | |
| CA | INPUT | Connection for DATA (A) slew-rate capacitor | |
| Аоит | OUTPUT | ARINC output terminal A | |
| -V | POWER | -12V to -15V | |
| GND | POWER | 0.0V | |
| +V | POWER | +12V to +15V | |
| Воит | OUTPUT | ARINC output terminal B | |
| Св | INPUT | Connection for DATA (B) slew-rate capacitor | |
| DATA (B) | INPUT | Data input terminal B | |
| CLOCK | INPUT | Synchronizes data inputs | |
| V1 | POWER | +5V ±5% | |

ABSOLUTE MAXIMUM RATINGS

All Voltages referenced to GND, TA = Operating Temperature Range (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | OPERATING RANGE | MAXIMUM | UNIT |
|-------------------------------|----------------|--|--|-------------------------|----------|
| Differential Voltage | VDIF | Voltage between +V and -V terminals | | 40 | V |
| Supply Voltage | +V -V V1 | | +10.8 to +16.5 -10.8 to -16.5 +5 ±5% | +7 | V V |
| Voltage Reference | VREF | For ARINC 429 For Applications other than ARINC | +5 ±5% 1.5 to 6 | 6 6 | V |
| Input Voltage Range | Vin | | | ≥ GND -0.3 ≤ V1 +0.3 | V |
| Output Short-Circuit Duration | | See Note: 1 | | | |
| Output Overvoltage Protection | | See Note: 2 | | | |
| Operating Temperature Range | Та | High-temp & Military Industrial | -55 to +125 -40 to +85 | | °C °C |
| Storage Temperature Range | Тѕтс | Ceramic & Plastic | -65 to +150 | | °C |
| Lead Temperature | | Soldering, 10 seconds | | +275 | °C |
| Junction Temperature | TJ | | | +175 | °C |

Note 1. Heatsinking may be required for continuous Output Short Circuit operation at +125°C and for 100KBPS (high speed) data rate operation at +125°C. Under either of these conditions the HI-318xPSx product with the Enhanced SOIC (ESOIC) package should be selected (see Data Sheet for HI-3182PSx, HI-3184PSx and HI-3185PSx).

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2. The fuses used for Output Overvoltage Protection may be blown by the presence of a voltage at either output that is greater than ±12.0V with respect to GND. (HI-3182PSx-N and HI-3184PSx-N only)

DC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V1 = VREF = +5.0V, TA = Operating Temperature Range (unless otherwise specified).

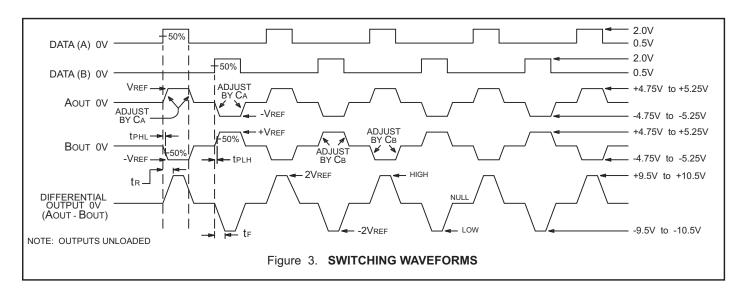
| PARAMETER | SYMBOL | CONI | DITION | MIN | TYP | MAX | UNITS |
|---|--------------|-----------------|----------------------|-------------|------|---------------|-------|
| Supply Current +V (Operating) | ICCOP (+V) | No Load | (0 - 100KBPS) | | | +16 | mA |
| Supply Current -V (Operating) | ICCOP (-V) | No Load | (0 - 100KBPS) | -16 | | | mA |
| Supply Current V1 (Operating) | ICCOP (V1) | No Load | (0 - 100KBPS) | | | 500 | μΑ |
| Reference Pin Current VREF (Operating) | ICCOP (VREF) | No Load, VREF = | = 5V (0 - 100KBPS) | -1.0 | -0.4 | -0.15 | mA |
| Supply Current +V (During Short Circuit Test) | Isc (+V) | Short to Ground | (See Note: 1) | | | 150 | mA |
| Supply Current -V (During Short Circuit Test) | Isc (-V) | Short to Ground | (See Note: 1) | -150 | | | mA |
| Output Short Circuit Current (Output High) | Іонѕс | Short to Ground | VMIN=0 (See Note: 2) | | | -80 | mA |
| Output Short Circuit Current (Output Low) | lolsc | Short to Ground | VMIN=0 (See Note: 2) | +80 | | | mA |
| Input Current (Input High) | lін | | | | | 1.0 | μA |
| Input Current (Input Low) | lı∟ | | | -1.0 | | | μΑ |
| Input Voltage High | VIH | | | 2.0 | | | V |
| Input Voltage Low | VIL | | | | | 0.5 | V |
| Output Voltage High (Output to Ground) | Voн | No Load | (0 -100KBPS) | +VREF 25 | | +VREF +.25 | V |
| Output Voltage Low (Output to Ground) | Vol | No Load | (0 -100KBPS) | -VREF 25 | | -VREF +.25 | V |
| Output Voltage Null | Vnull | No Load | (0-100KBPS) | -250 | | +250 | mV |
| Input Capacitance | CIN | See Note 1 | | | 15 | | pF |

Note 1. Not tested, but characterized at initial device design and after major process and/or design change which affects this parameter.

AC ELECTRICAL CHARACTERISTICS

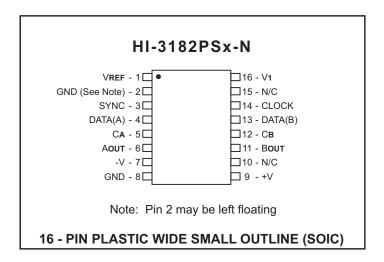
+V = +15V, -V = -15V, V1 = VREF = +5.0V, TA = Operating Temperature Range (unless otherwise specified).

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|----------------------------------|--------|------------------------------|-----|-----|-----|-------|
| Rise Time (AOUT, BOUT) | tr | CA = CB = 75pF See Figure 3. | 1.0 | | 2.0 | μs |
| Fall Time (AOUT, BOUT) | tF | CA = CB = 75pF See Figure 3. | 1.0 | | 2.0 | μs |
| Propagtion Delay Input to Output | tplH | CA = CB = 75pF See Figure 3. | | | 3.0 | μs |
| Propagtion Delay Input to Output | tphl | CA = CB = 75pF See Figure 3. | | | 3.0 | μs |



Note 2. Interchangeability of force and sense is acceptable.

ADDITIONAL PIN CONFIGURATIONS (See page 1 for 14-Pin Narrow Small Outline SOIC)



ORDERING INFORMATION

HI - 318xPS x x - N

| PART PACKAGE NUMBER DESCRIPTION | |
|---------------------------------|---|
| Blank | Tin / Lead (Sn / Pb) Solder |
| F | 100% Matte Tin (Pb-free RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN | |
|----------------|-------------------|------|------------|--|
| I | -40°C TO +85°C | I | No | |
| Т | -55°C TO +125°C | T | No | |

| PART | PACKAGE | OUTPUT SEI | RIES |
|--------|---|------------|------|
| NUMBER | DESCRIPTION | RESISTANCE | FUSE |
| 3182PS | 16 PIN PLASTIC WIDE SMALL OUTLINE SOIC (16HW) | 37.5 Ohms | Yes |
| 3184PS | 14 PIN PLASTIC NARROW SMALL OUTLINE SOIC (14HN) | 37.5 Ohms | Yes |
| 3185PS | 14 PIN PLASTIC NARROW SMALL OUTLINE SOIC (14HN) | 37.5 Ohms | No |

REVISION HISTORY

| Revision | Date | Page | Description of Change |
|-----------------|----------|-------|--|
| DS3182N, Rev. C | 05/01/08 | 1 | Date was "March 2007", is "May 2008". Footer was "Rev. B", is "Rev. C" and was "03/07", is "05/08" |
| | | 1 | Added "HI-3184PSx-N" to the document title and in the Pin Configuration. |
| | | 1 | "HI-3182" in first sentence of the first paragraph of the GENERAL DESCRIPTION changed to "HI-3182, HI-3184". |
| | | 1 | "HI-3182 product also has" in the last sentence of the third paragraph of the GENERAL DESCRIPTION changed to "and HI-3184 products also have". |
| | | 2 - 5 | "HI-3182PSx-N" added to header. |
| | | 2 | "HI-3182," in the sixth paragraph of the FUNCTIONAL DESCRIPTION changed to "HI-3182 and HI-3184". |
| | | 3 | Clarified Note 1 to read "Heatsinking may be required for continuous Output Short Circuit operation at +125°C and for 100KBPS (high speed) data rate operation at +125°C. Under either of these conditions the HI-318xPSx product with the Enhanced SOIC (ESOIC) package should be selected (see Data Sheet for HI-3182PSx, HI-3184PSx and HI-3185PSx)." |
| | | 3 | "HI-3182" in Note 2. changed to "HI-3182PSx-N and HI-3184PSx-N". |
| | | 5 | Added "HI-3184PS" to ORDERING INFORMATION table. |
| | | 6 | Added "REVISION HISTORY" table. |
| | | 7 | Renumbered old page"6" as "7". |

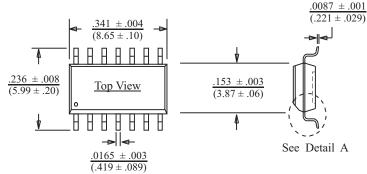
HI-318xPSx-N PACKAGE DIMENSIONS

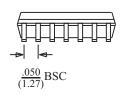
14-PIN PLASTIC SMALL OUTLINE (SOIC) - NB

(Narrow Body)

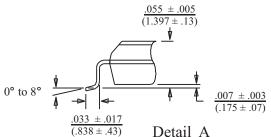
inches (millimeters)

Package Type: 14HN





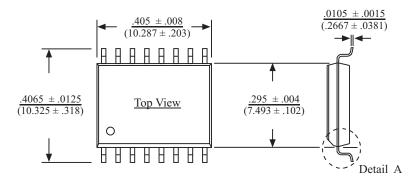
BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

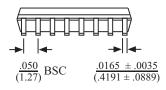


16-PIN PLASTIC SMALL OUTLINE (SOIC) - WB

(Wide Body)

inches (millimeters) Package Type: 16HW





BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

