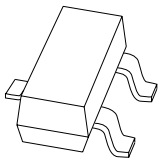


PMV40UN

TrenchMOS™ ultra low level FET

Rev. 01 — 05 August 2003 Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PMV40UN in SOT23.

1.2 Features

- Ultra low level threshold
- Surface mount package.

1.3 Applications

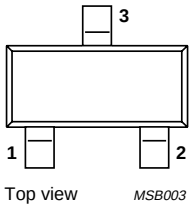
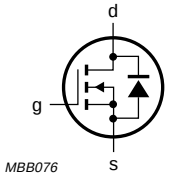
- Battery management
- High-speed switch.

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $I_D \leq 4.9$ A
- $P_{tot} \leq 1.9$ W
- $R_{DSon} \leq 47$ mΩ.

2. Pinning information

Table 1: Pinning - SOT23, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	source (s)		
3	drain (d)		

SOT23

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PMV40UN	-	plastic surface mounted package; 3 leads	SOT23

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C	-	30	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	gate-source voltage (DC)		-	±8	V
I_D	drain current (DC)	T_{sp} = 25 °C; V_{GS} = 4.5 V; Figure 2 and 3	-	4.9	A
		T_{sp} = 100 °C; V_{GS} = 4.5 V; Figure 2	-	3.1	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	-	19.6	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; Figure 1	-	1.9	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{sp} = 25 °C	-	1.6	A
I_{SM}	peak source (diode forward) current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs	-	6.4	A

5. Characteristics

Table 4: Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	30	-	-	V
		T_j = –55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				V
		T_j = 25 °C	0.45	0.7	-	V
		T_j = 150 °C	0.25	0.4	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 30 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	1	µA
		T_j = 150 °C	-	-	100	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±8 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 2 A; Figure 7 and 8				
		T_j = 25 °C	-	40	47	mΩ
		T_j = 150 °C	-	68	79.9	mΩ
		V_{GS} = 2.5 V; I_D = 1.5 A; Figure 7 and 8	-	45	53	mΩ
		V_{GS} = 1.8 V; I_D = 1 A; Figure 7 and 8	-	55	73	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 1 A; V_{DD} = 15 V; V_{GS} = 4.5 V; Figure 13	-	9.3	-	nC
Q_{gs}	gate-source charge		-	0.7	-	nC
Q_{gd}	gate-drain (Miller) charge		-	2.2	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 30 V; f = 1 MHz; Figure 11	-	445	-	pF
C_{oss}	output capacitance		-	65	-	pF
C_{rss}	reverse transfer capacitance		-	50	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 15 V; R_L = 15 Ω; V_{GS} = 4.5 V; R_G = 6 Ω	-	6	-	ns
t_r	rise time		-	12	-	ns
$t_{d(off)}$	turn-off delay time		-	38	-	ns
t_f	fall time		-	12	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 1.25 A; V_{GS} = 0 V; Figure 12	-	0.66	1.2	V