



PMV31XN

N-channel TrenchMOS FET

Rev. 2 — 30 November 2011

[Product data sheet](#)

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a SOT23 (TO-236AB) small Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Low threshold voltage
- Trench MOSFET technology

1.3 Applications

- Battery-powered motor control
- High-speed switching in set top box power supplies

1.4 Quick reference data

Table 1. Quick reference data

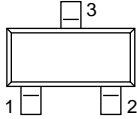
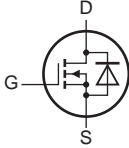
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	20	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = 4.5\text{ V}$; see Figure 2 ; see Figure 3	-	-	5.9	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 1	-	-	2	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 2.5\text{ V}$; $I_D = 1\text{ A}$; $T_j = 25\text{ °C}$; see Figure 9 ; see Figure 10	-	44	53	mΩ
		$V_{GS} = 4.5\text{ V}$; $I_D = 1.5\text{ A}$; $T_j = 25\text{ °C}$; see Figure 9 ; see Figure 10	-	31	37	mΩ

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2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT23 (TO-236AB)</p>	 <p>017aaa253</p>
2	S	source		
3	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV31XN	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PMV31XN	%M4

[1] % = placeholder for manufacturing site code

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	20	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	20	V
V_{GS}	gate-source voltage		-12	12	V
I_D	drain current	$T_{sp} = 100\text{ °C}$; $V_{GS} = 4.5\text{ V}$; see Figure 2	-	3.75	A
		$T_{sp} = 25\text{ °C}$; $V_{GS} = 4.5\text{ V}$; see Figure 2 ; see Figure 3	-	5.9	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	23.7	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 1	-	2	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ °C}$	-	1.7	A

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	18	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	20	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 8	-	-	1.8	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$; see Figure 8	0.35	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 8	0.5	-	1.5	V
I_{DSS}	drain leakage current	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ C$	-	-	100	μA
		$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = -12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 2.5 \text{ V}; I_D = 1 \text{ A}; T_j = 25 \text{ }^\circ C$; see Figure 9 ; see Figure 10	-	44	53	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 1.5 \text{ A}; T_j = 25 \text{ }^\circ C$; see Figure 9 ; see Figure 10	-	31	37	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 6 \text{ A}; V_{DS} = 10 \text{ V}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ C$; see Figure 11	-	5.8	-	nC
Q_{GS}	gate-source charge		-	1.4	-	nC
Q_{GD}	gate-drain charge		-	1.7	-	nC
C_{iss}	input capacitance	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; see Figure 12	-	410	-	pF
C_{oss}	output capacitance		-	115	-	pF
C_{rss}	reverse transfer capacitance		-	80	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 \text{ V}; R_L = 10 \text{ }^\Omega; V_{GS} = 4.5 \text{ V}; R_{G(ext)} = 6 \text{ }^\Omega; T_j = 25 \text{ }^\circ C$	-	10	-	ns
t_r	rise time		-	15	-	ns
$t_{d(off)}$	turn-off delay time		-	25	-	ns
t_f	fall time		-	12	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 1.5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$; see Figure 13	-	0.75	1.2	V