

The PJ3100 family is a positive voltage linear regulator developed utilizing CMOS technology featured low quiescent current (30 $\mu$ A typ), low dropout voltage, and high output voltage accuracy, making them ideal for battery applications. EN input connected to CMOS has low bias current. The space-saving SOT-23-5L package is attractive for “Pocket” and “Hand Held” application.

These rugged devices have both Thermal Shutdown, and Current Fold-back to prevent device failure under the “Worst” of operating conditions.

In application requiring a low noise, regulated supply, place a 1000pF capacitor between Bypass and Ground.

The PJ3100 is stable with an output capacitance of 2.2 $\mu$ F or greater.

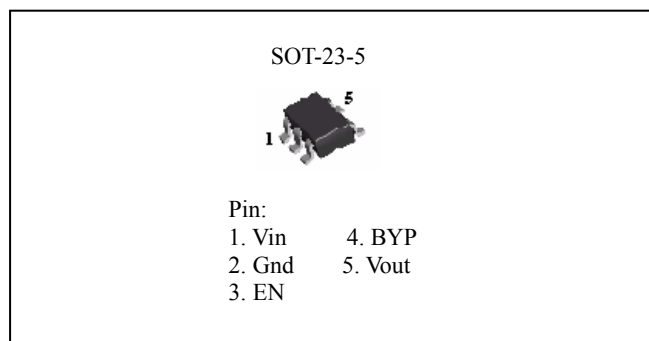
### FEATURES

- Very Low Dropout Voltage
- High Accuracy Output Voltage:  $\pm 1.5\%$
- Low Current Consumption : Typ. 30 $\mu$ A, Max. 35 $\mu$ A
- Output Voltage Range :1.5V, 1.8V, 1.9V, 2.2V, 2.5V, 2.7V, 2.8V, 3.3V, 3.5V, 3.6V, and 3.8V
- Thermal Shutdown
- Low Temperature Coefficient

### APPLICATION

- Battery-powered devices
- Personal communication devices
- Home electric/electronic application
- PC peripherals

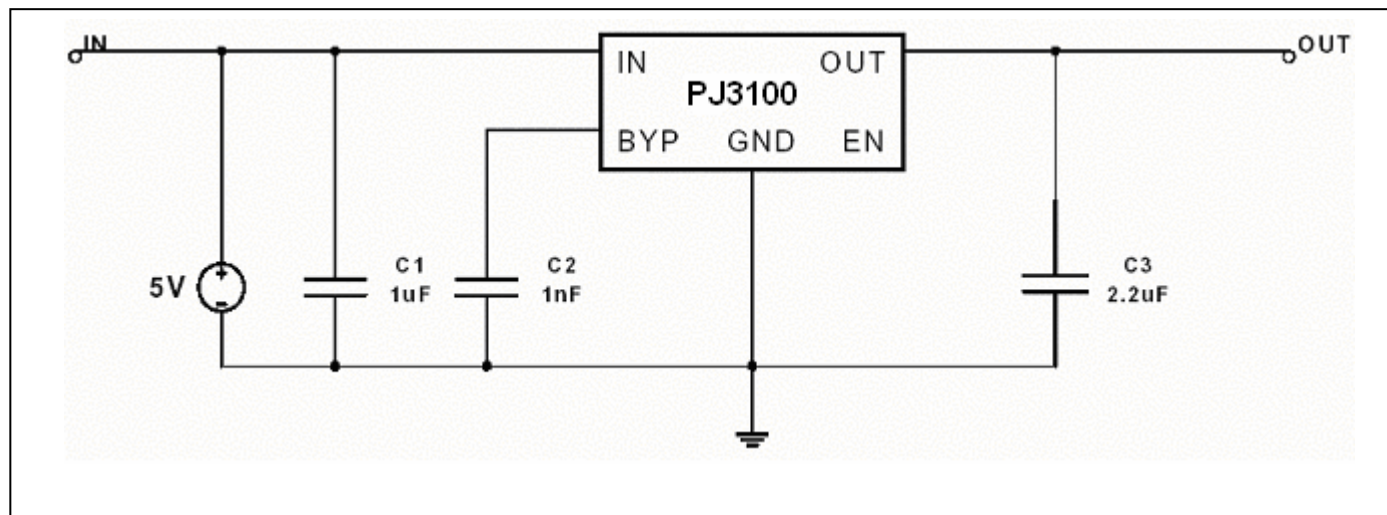
### TYPICAL APPLICATIONS



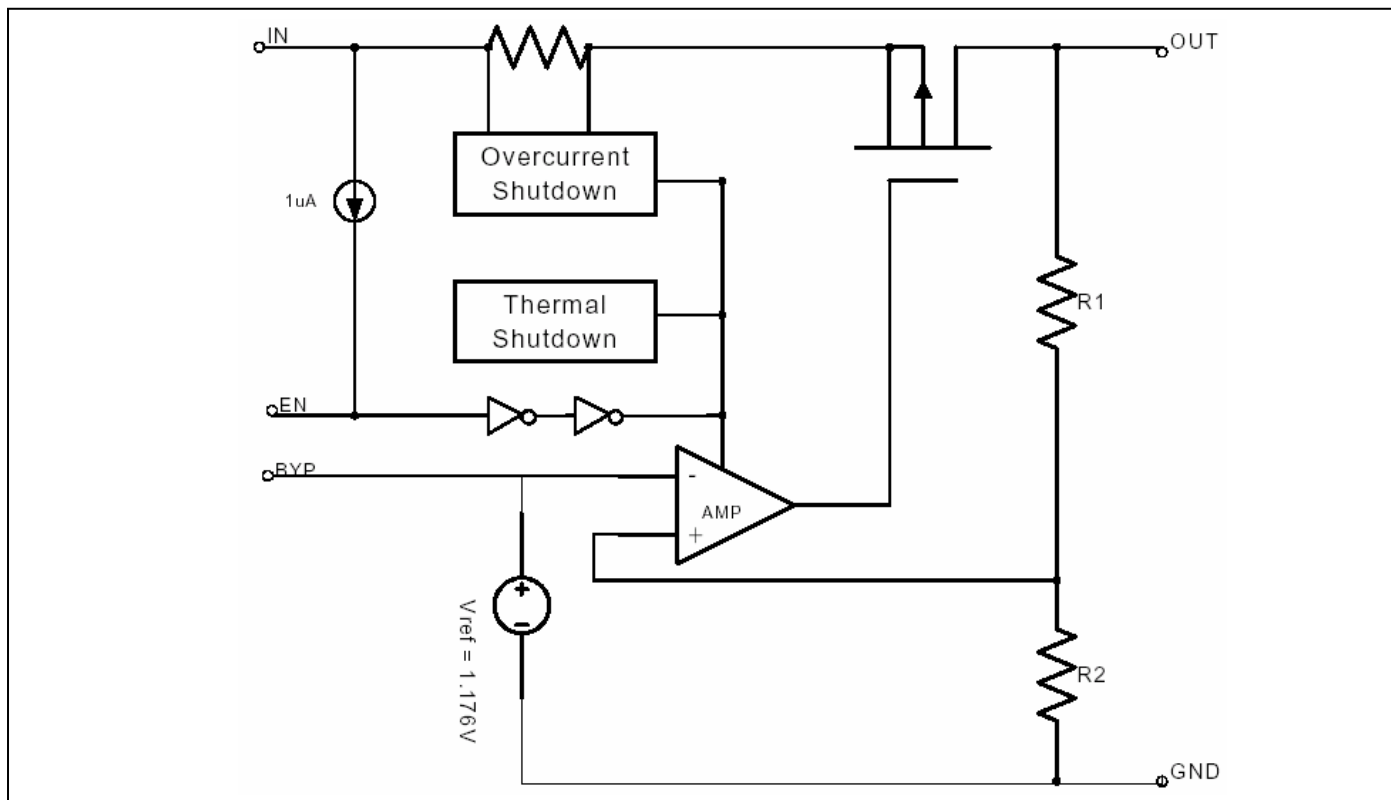
### ORDER INFORMATION

Device	Operation Temperature (Ambient)	Package
PJ3100CX	-40°C ~ +85°C	SOT-23-5

- Short Circuit Current Fold-Back
- Compact package : SOT-23-5
- Factory Pre-set Output Voltage
- Current Limiting
- Input Range of 2.6V to 7.0V
- Guaranteed 300mA Output



**BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Input Voltage	$V_{IN}$	7	V
Output Current	$I_{OUT}$	$P_D / (V_{IN} - V_O)$	mA
Output Voltage	$V_{OUT}$	GND-0.3V ~ $V_{IN} + 0.3$	V
Junction Temperature	$T_j$	-40 ~ +125	°C
Storage Temp.	$T_{stg}$	-40 ~ +125	°C

**THERMAL INFORMATION**

Parameter		Maximum	Unit
Thermal Resistance ( $\theta_{JC}$ )	SOT-23-5	260	°C/W
Internal Power Dissipation ( $P_D$ ) ( $\Delta T = 100^\circ\text{C}$ )	SOT-23-5	380	°C/W
Maximum Junction Temperature		150	°C
Maximum Lead Temperature		300	°C

**ELECTRICAL CHARACTERISTICS** (Ta = +25°C unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Voltage	V <sub>IN</sub>			Note 1		7	V
Output Voltage Accuracy	V <sub>OUT</sub>	I <sub>O</sub> =1mA ~ 300mA		-2		2	%
Load Regulation	REG <sub>LOAD</sub>	I <sub>O</sub> =1mA ~ 300mA			0.2	1	%
Line Regulation	REG <sub>LINE</sub>	I <sub>O</sub> =5mA, V <sub>IN</sub> =V <sub>OUT</sub> +1 to V <sub>OUT</sub> +2	V <sub>OUT</sub> ≤ 3.0V	-0.15	0.03	0.15	%
			V <sub>OUT</sub> > 3.0V	-0.3	0.06	0.3	%
Dropout Voltage	V <sub>DROPOUT</sub>	I <sub>O</sub> =300mA, V <sub>OUT</sub> =V <sub>O(NOM)</sub> -2%, V <sub>OUT</sub> ≥ 2.5V			300		mV
		I <sub>O</sub> =300mA, V <sub>OUT</sub> =V <sub>O(NOM)</sub> -2%, V <sub>OUT</sub> < 2.5V			800		
Output Current	I <sub>O</sub>	V <sub>OUT</sub> > 1.2V		300			mA
Current Limit	I <sub>LIMIT</sub>	V <sub>OUT</sub> > 1.2V		300	450		mA
Short Circuit Current	I <sub>SC</sub>	V <sub>OUT</sub> < 0.95V			150	300	mA
Quiescent Current	I <sub>Q</sub>	I <sub>O</sub> = 0mA			30	35	μA
Ground Pin Current	I <sub>GN</sub>	I <sub>O</sub> = 1mA ~ 300mA			30	50	μA
Over Temperature Shutdown	OTS				150		°C
Over Temperature Hysteresis	OTH				30		°C
V <sub>OUT</sub> Temperature Coefficient	TC				25		ppm/°C
Power Supply Rejection	PSRR	I <sub>O</sub> = 100mA Co=2.2μF ceramic	f=1KHz		60		dB
			f=10KHz		50		
			f=100KHz		40		
Power Supply Rejection	PSRR	I <sub>O</sub> = 100mA Co=2.2μF ceramic C <sub>BYP</sub> =0.01μF	f=1KHz		75		dB
			f=10KHz		55		
			f=100KHz		30		
Output Voltage Noise	e <sub>N</sub>	f=10Hz to 100KHz I <sub>O</sub> =10mA, C <sub>BYP</sub> =0μF	Co=2.2μF		30		μV <sub>rms</sub>
			Co=100μF		20		
Output Voltage Noise	e <sub>N</sub>	f=10Hz to 100KHz I <sub>O</sub> =10mA, C <sub>BYP</sub> =0.01μF	Co=2.2μF		30		μV <sub>rms</sub>
			Co=100μF		20		
Shutdown Supply Current	I <sub>SD</sub>	V <sub>IN</sub> =5V, V <sub>OUT</sub> =0V, V <sub>EN</sub> <V <sub>EL</sub>			2.0	3.0	μA
EN Input Bias Current	I <sub>EH</sub>	V <sub>EN</sub> =V <sub>EL</sub> , V <sub>IN</sub> =2.6V~7V				0.1	μA
	I <sub>EL</sub>	V <sub>EN</sub> =V <sub>EL</sub> , V <sub>IN</sub> =2.6V~7V			1.0	3.0	
EN Input Threshold	V <sub>EH</sub>	V <sub>IN</sub> =2.6V~7V			V <sub>IN</sub> /2+0.8V	V <sub>IN</sub>	V
	V <sub>EL</sub>	V <sub>IN</sub> =2.6V~7V		0	V <sub>IN</sub> /2-0.8V		

**Note:** 1. V<sub>IN(MIN)</sub> = V<sub>OUT</sub>+V<sub>DROPOUT</sub>

**ORDERING INFORMATION**

Part Number	Output Voltage	Voltage Code	Package
PJ3115CX	1.5V	A	SOT-23-5L
PJ3118CX	1.8V	D	SOT-23-5L
PJ3119CX	1.9V	E	SOT-23-5L
PJ3122CX	2.2V	H	SOT-23-5L
PJ3125CX	2.5V	K	SOT-23-5L
PJ3127CX	2.7V	M	SOT-23-5L
PJ3128CX	2.8V	N	SOT-23-5L
PJ3129CX	2.9V	O	SOT-23-5L
PJ3130CX	3.0V	P	SOT-23-5L
PJ3133CX	3.3V	S	SOT-23-5L
PJ3135CX	3.5V	U	SOT-23-5L
PJ3136CX	3.6V	V	SOT-23-5L
PJ3138CX	3.8V	X	SOT-23-5L

**DETAILED DESCRIPTION**

The PJ3100 family of CMOS regulators contain a PMOS pass transistor, voltage reference, error amplifier, over-current protection, thermal shutdown, and short circuit protection.

The P-channel pass transistor receives data from the error amplifier, over current shutdown, short output protection, and thermal protection circuits. During normal operation, the error amplifier compares the output voltage to a precision reference. Over-current and Thermal shutdown circuits become active when the junction temperature exceeds 150°C, or the current exceeds 300mA.

During thermal shutdown, the output voltage remains low. Normal operation is restored when the junction temperature drops below 120°C.

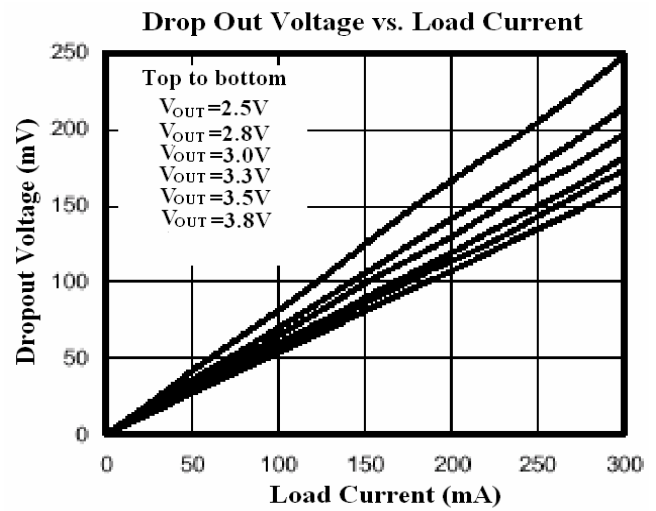
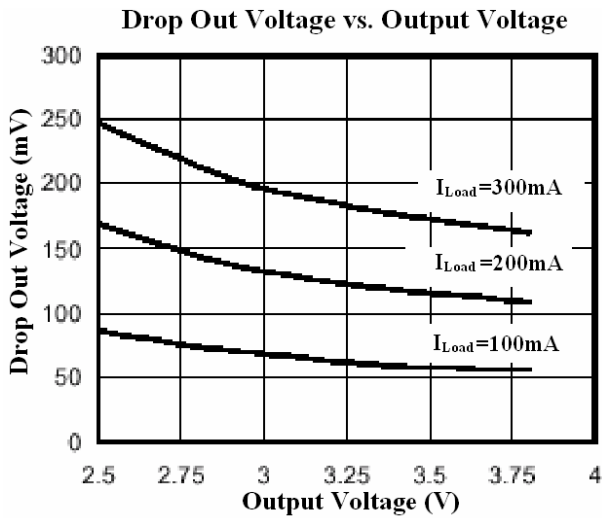
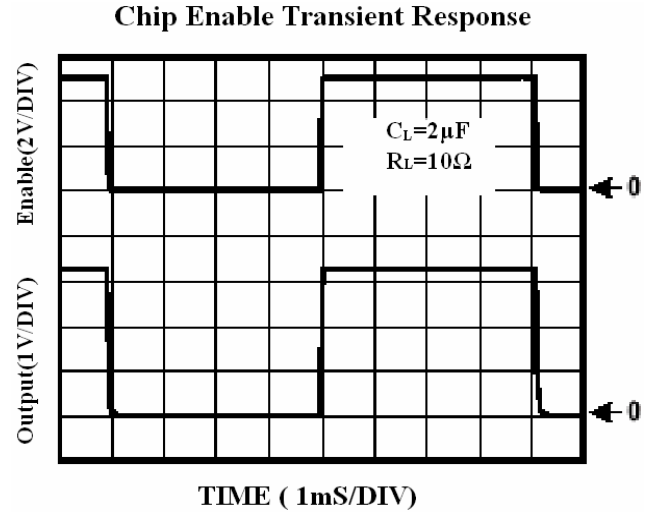
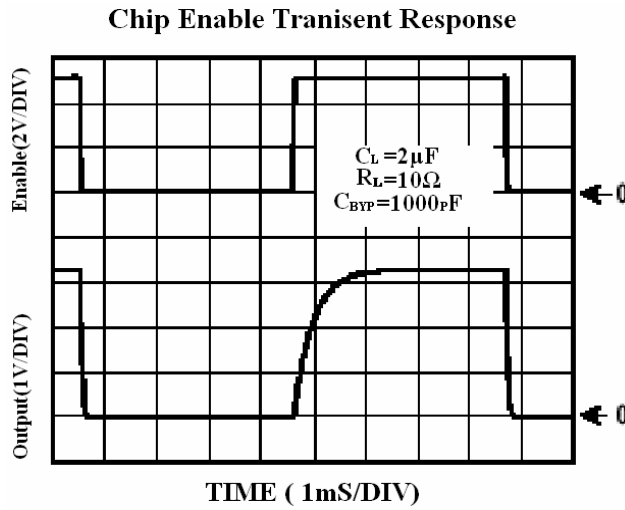
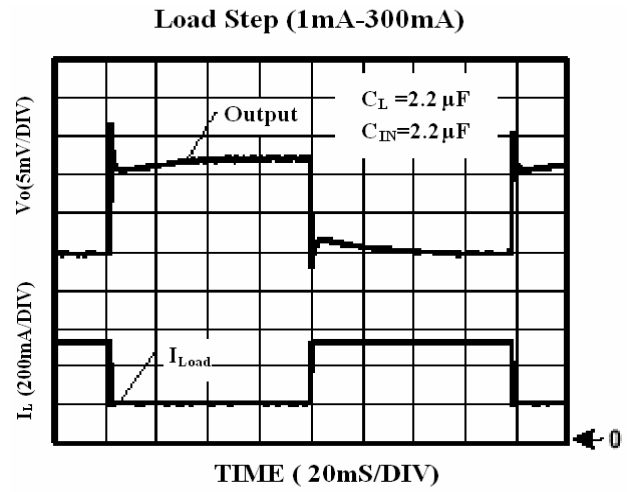
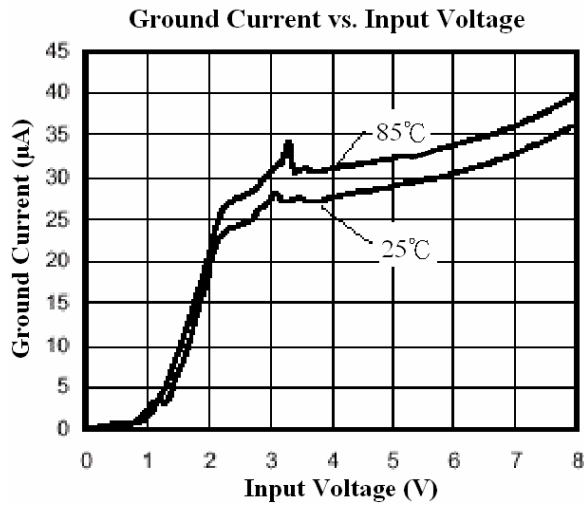
The PJ3100 switches from voltage mode to current mode when the load exceeds the rated output current. This prevents over-stress. The PJ3100 also incorporates current fold-back to reduce power dissipation when the output is short-circuited. This feature becomes active when the output drops below 1.05V, and reduces the current flow by 65%. Full current is restored when the voltage exceeds 0.95V.

**ENABLE**

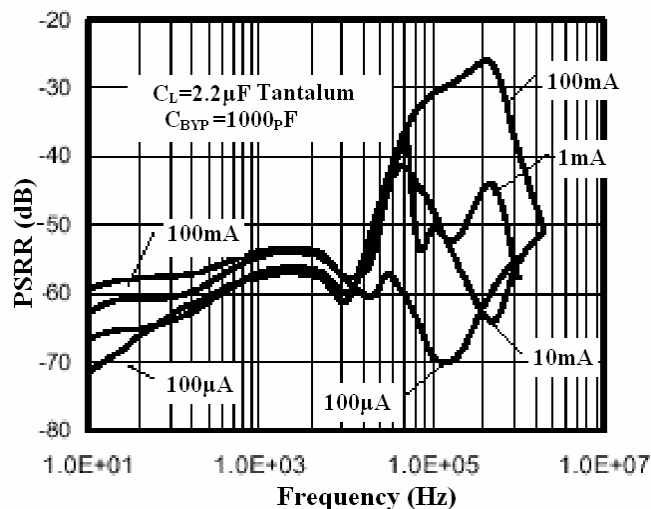
The Enable pin normally floats high. When actively, pulled low, the PMOS pass transistor shut off, and all internal circuits are powered down. In this state, the quiescent current is less than 2μA. This pin behaves much like an electronic switch.

**EXTERNAL CAPACITOR**

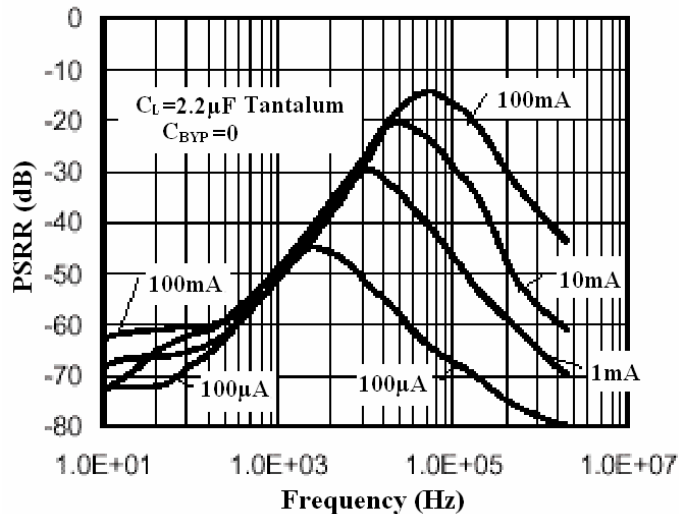
The PJ3100 is stable with an output capacitor to ground of 2.2μF or greater. It can keep stable even with higher or poor ESR capacitors. A second capacitor is recommended between the input and ground to stabilize VIN. The input capacitor should be larger than 0.1μF to have a beneficial effect. All capacitors should be placed in close proximity to the pins. A “quiet” ground termination is desirable.



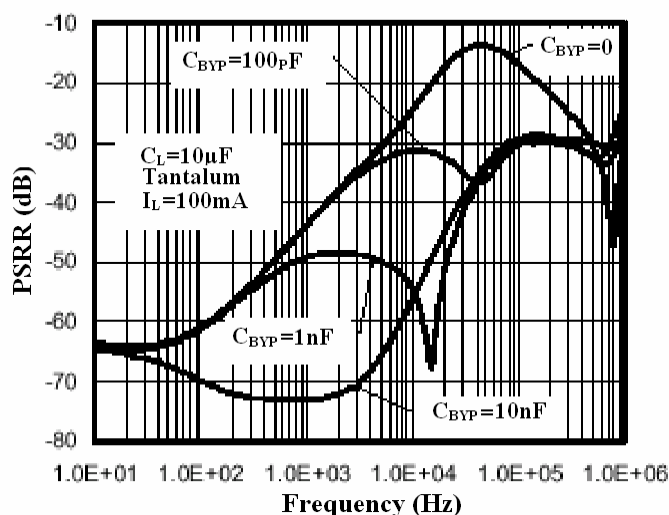
Power Supply Rejection Ratio



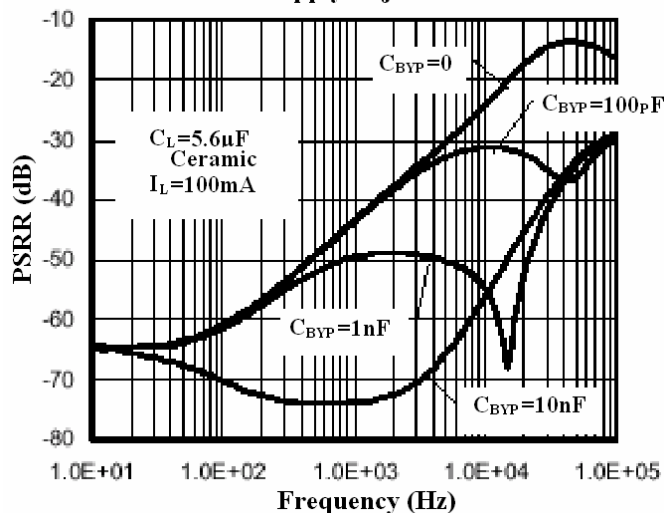
Power Supply Rejection Ratio



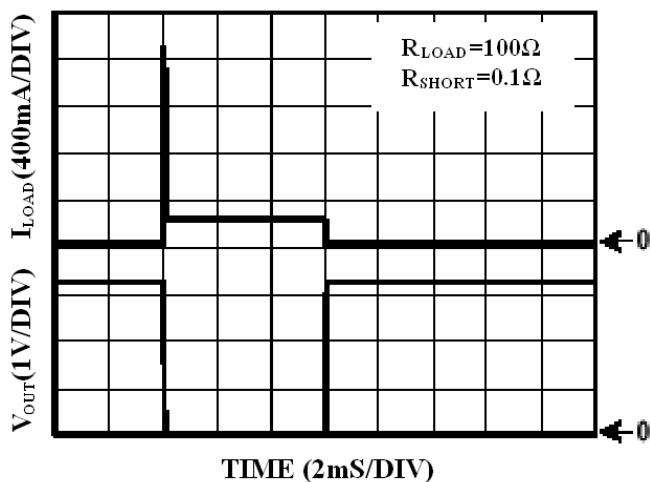
Power Supply Rejection Ratio



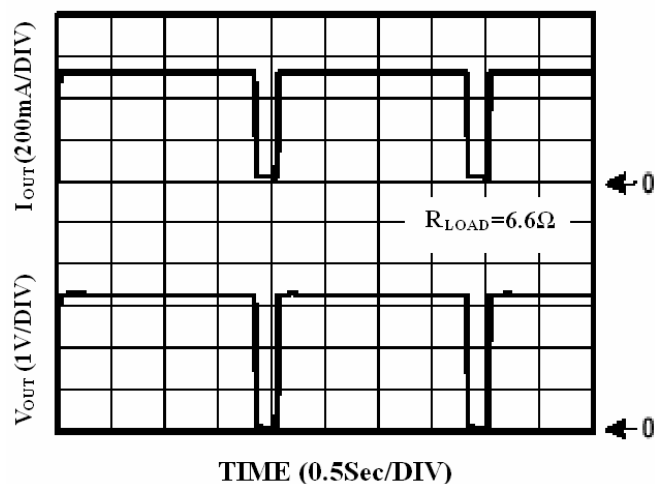
Power Supply Rejection Ratio



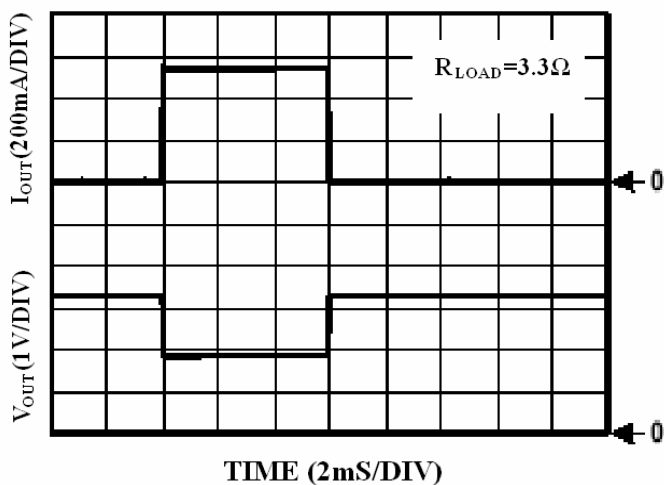
Short Circuit Response



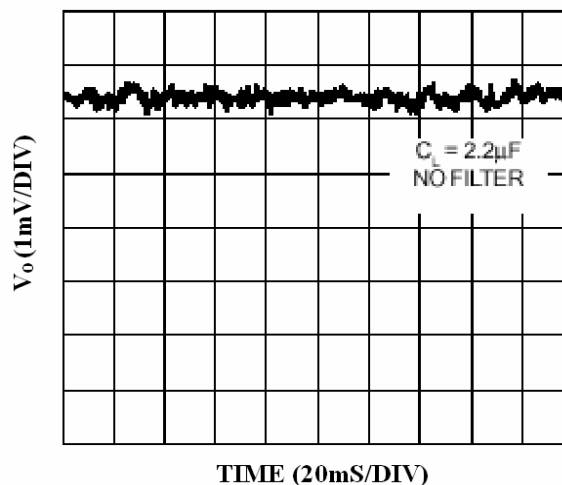
Over Temperature Shutdown



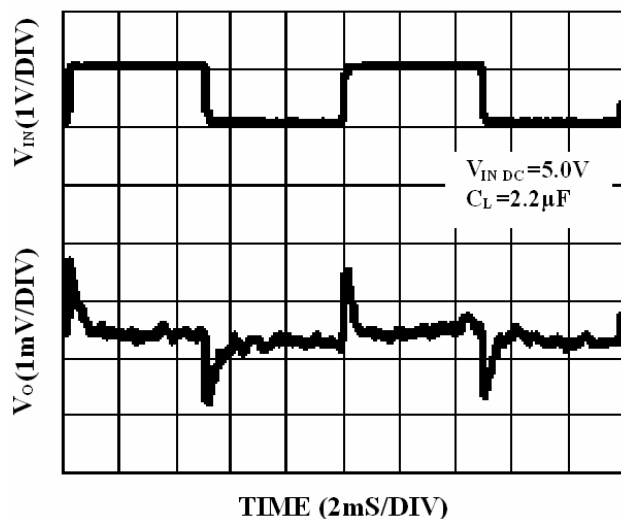
Current Limit Response



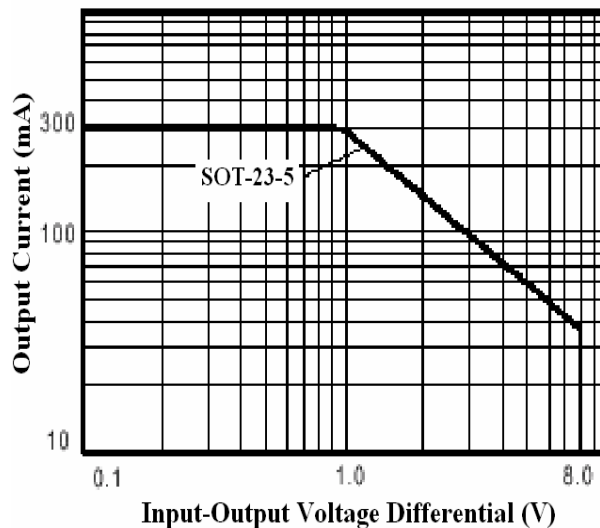
Noise Measurement



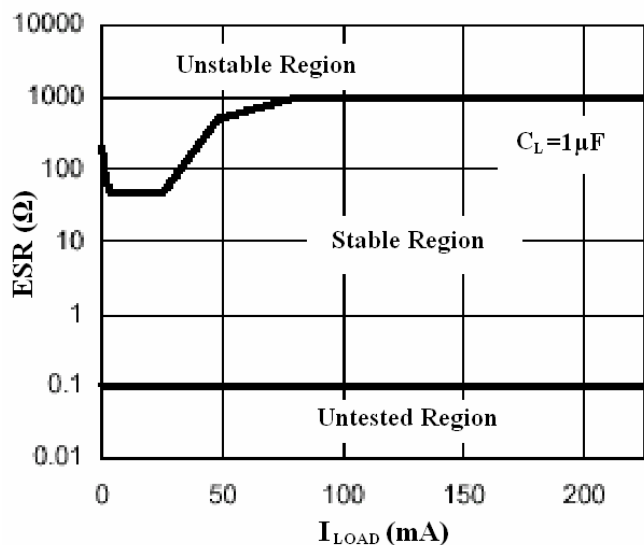
Transient Line Response



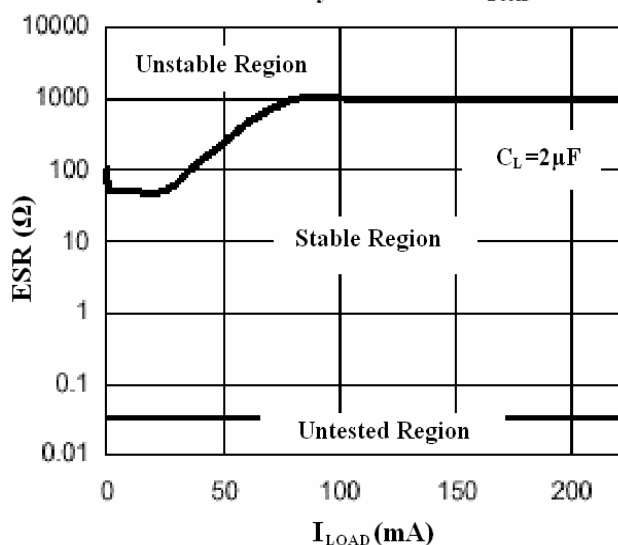
Safe Operating Area

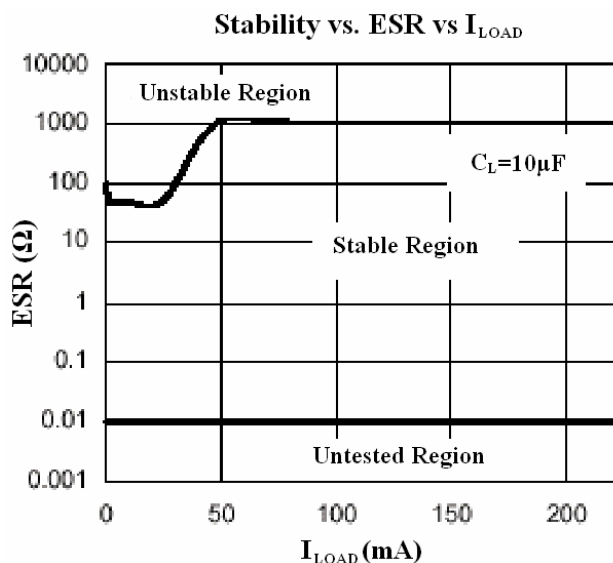
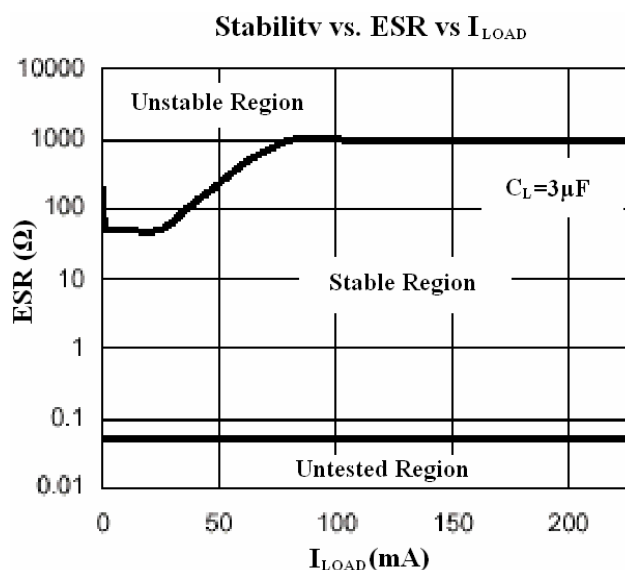


Stability vs. ESR vs  $I_{LOAD}$



Stability vs. ESR vs  $I_{LOAD}$





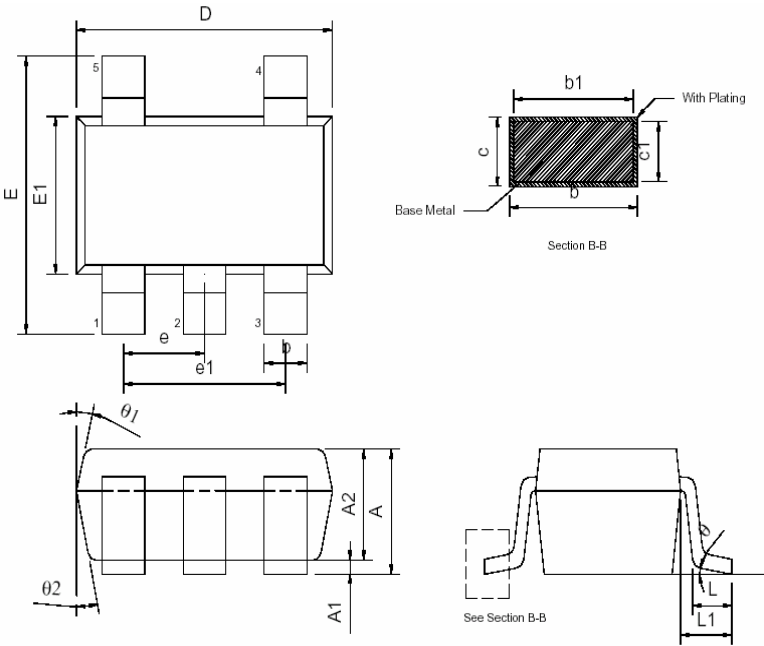
### IMPORTANT NOTICE

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SOT-23-5L



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.05	---	1.35	0.041	---	0.053
A1	0.05	---	0.15	0.002	---	0.006
A2	1.00	1.10	1.20	0.039	0.043	0.047
b	0.25	---	0.50	0.010	---	0.020
b1	0.25	0.40	0.45	0.010	0.016	0.018
c	0.08	---	0.20	0.003	---	0.008
c1	0.08	0.11	0.15	0.003	0.004	0.006
D	2.70	2.90	3.00	0.106	0.114	0.118
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.50	1.60	1.70	0.059	0.063	0.067
L	0.35	0.45	0.55	0.014	0.018	0.022
L1	0.60 REF			0.024 REF		
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
θ	0°	5°	10°	0°	5°	10°
θ1	3°	5°	7°	3°	5°	7°
θ2	6°	8°	10°	6°	8°	10°