NCP1560

Advance Information

Full Featured Voltage Mode PWM Controller

The NCP1560 PWM controller contains all of the features and flexibility needed to implement voltage–mode control for modern high performance power converters. This device cost effectively reduces system part count with the inclusion of a high voltage start–up regulator that operates over a wide input range of 33 V to 150 V. The NCP1560 provides two control outputs, OUT1 which controls the main PWM switch and OUT2 with adjustable over–lap delay, which can control a synchronous rectifier. Other distinctive features include: two mode over current protection, line under/over voltage lockout, fast line feedforward, softstart and a maximum duty cycle clamp.

Features

- Internal High Voltage Start–up Regulator
- Dual Control Outputs with Adjustable Overlap Delay
- Single Resistor Oscillator Frequency Setting
- Fast Line Feedforward
- Line Under/Over Voltage Lockout
- Dual Mode Over Current Protection
- Programmable Maximum Duty Cycle Control
- Maximum Duty Cycle Proportional to Line Voltage
- Programmable Softstart
- Precision 5.0 V Reference

Typical Applications

- Telecommunication Power Converters
- Industrial Power Converters
- High Voltage Power Modules
- +42 V Automotive Systems
- Control Driven Synchronous Rectifier Power Converters

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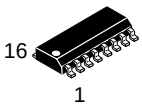
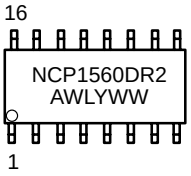
MARKING DIAGRAM



SO–16
D SUFFIX
CASE 751B



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NCP1560DR2	SO–16	2500 Units/Reel

This document contains information on a new product. Specifications and information herein are subject to change without notice.

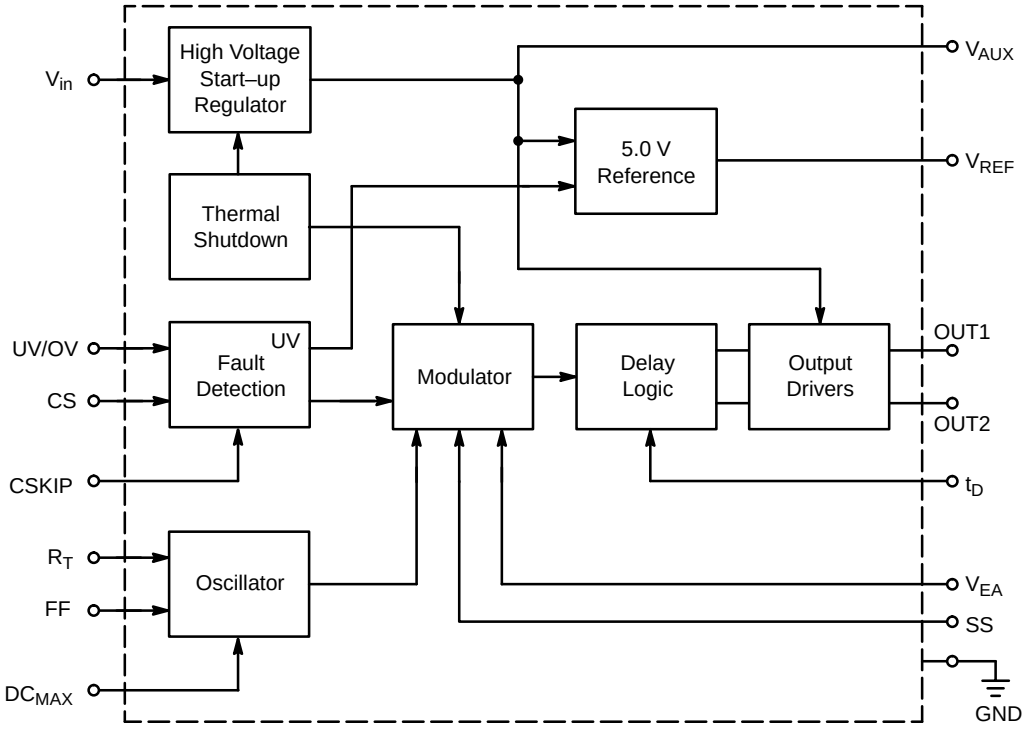


Figure 1. Simplified Block Diagram

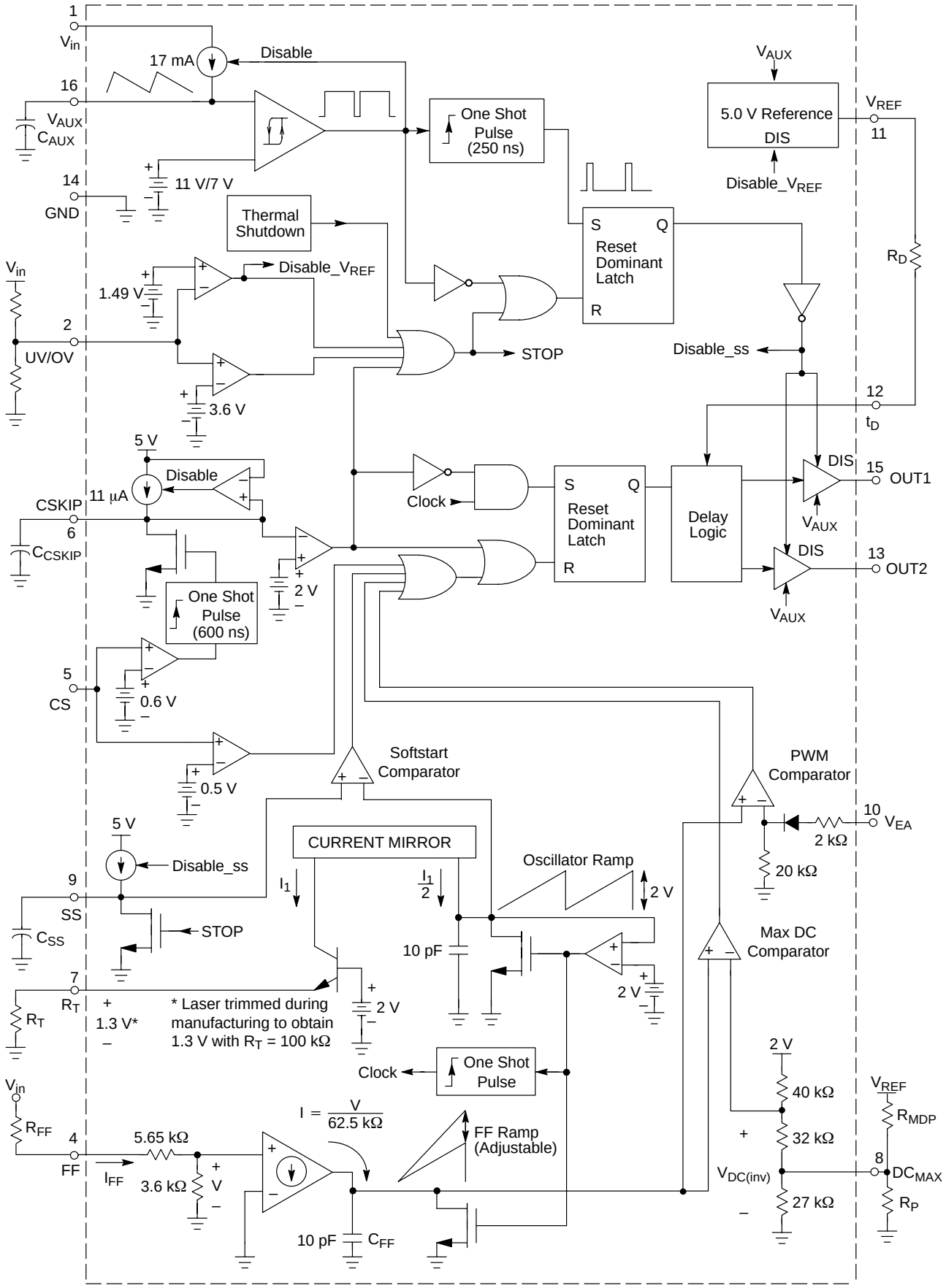


Figure 2. NCP1560 Block Diagram

PIN DESCRIPTION

Pin	Name	Application Information
1	V_{in}	This pin is connected to the bulk DC input voltage supply. A constant current source supplies current from this pin to the capacitor connected on the V_{AUX} pin. The charge current is typically 17 mA. Input voltage range is 33 V to 150 V.
2	UV/OV	Input supply voltage is scaled down and sampled by means of a resistor divider. The supply voltage must be scaled down between 1.49 V and 3.60 V within the specified input voltage range.
3	NC	Not Connected.
4	FF	An external resistor between V_{in} and this pin adjusts the amplitude of the FF Ramp in proportion to V_{in}. By varying the feedforward ramp amplitude in proportion to V_{in} voltage, changes in loop bandwidth resulting from V_{in} changes are eliminated.
5	CS	Over current sense input. If the CS voltage exceeds 0.47 V or 0.57 V, the converter enters Cycle by Cycle or Cycle Skip current limit mode, respectively.
6	CSKIP	The capacitor connected to this pin sets the CS Fault timer after a Cycle Skip current limit fault is detected. A softstart sequence will follow at the conclusion of the fault timer.
7	R_T	A single external resistor between this pin and GND sets the fixed oscillator frequency.
8	DC_{MAX}	An external resistor between this pin and GND sets the voltage on the Max DC Comparator inverting input. The duty cycle is limited by comparing the voltage on the Max DC Comparator inverting input to the Feedforward Ramp.
9	SS	An internal 6.0 μA current source charges the external capacitor connected to this pin. The duty cycle is limited during start–up by comparing the voltage on this pin to the Oscillator Ramp.
10	V_{EA}	The error signal from an external error amplifier is fed into this input and compared to the Feedforward Ramp. A series diode and resistor offset the voltage on this pin before it is applied to the PWM Comparator inverting input.
11	V_{REF}	Precision 5.0 V reference output. Maximum output current is 10 mA.
12	t_D	An external resistor between V_{REF} and this pin sets the leading and trailing edge time delay between OUT1 and OUT2 transitions.
13	OUT2	Output of the PWM controller with leading and trailing edge time delay. OUT2 can be used to drive a synchronous rectifier.
14	GND	Control circuit ground.
15	OUT1	Main output of the PWM controller.
16	V_{AUX}	Positive input supply voltage. This pin is connected to an external capacitor for energy storage. An internal current supplies current from V_{in} to this pin. Once the V_{AUX} voltage reaches 11 V, the current source turns OFF. It turns ON again once V_{AUX} falls to 7 V. Power is then supplied to the IC via this pin, by means of an auxiliary winding.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Input Line Voltage	V_{in}	–0.3 to 150	V
Auxiliary Supply Voltage	V_{AUX}	–0.3 to 16	V
OUT1 and OUT2 Voltage	V_{OUT}	–0.3 to V_{AUX} – 0.8 V	V
OUT1 and OUT2 Output Current	I_{OUT}	10	mA
5.0 V Reference Voltage	V_{REF}	–0.3 to 6.0	V
5.0 V Reference Output Current	I_{REF}	10	mA
DC_{MAX} Voltage	V_{DCMAX}	–0.3 to 2.0	V
All Other Inputs/Outputs Voltage	V_{IO}	–0.3 to 5.5	V
All Other Inputs/Outputs Current	I_{IO}	TBD	mA
Operating Junction Temperature	T_J	–40 to +150	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Power Dissipation at T_A = 25°C	P_D	0.88	W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	130	°C/W

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
   A. This device series contains ESD protection and exceeds the following tests:
      Pin 1: Human Body Model 2000 V per MIL–STD–883, Method 3015.
      Machine Model Method 150 V.
      Pins 2–16: Human Body Model 2000 V per MIL–STD–883, Method 3015.
      Machine Model Method 200 V.
      Pin 1 is the HV startup of the device and is rated to the max rating of the part, or 150 V.
   B. This device contains Latch–Up protection and exceeds ±XX mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS (V_{in} = 48 V, V_{AUX} = 12 V, V_{EA} = 2 V, R_T = 100 kΩ, C_{CSKIP} = 6800 pF, R_D = 60.4 kΩ, R_{FF} = 464 kΩ, for typical values T_J = 25°C, for min/max values, T_J = –40°C to 125°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
START–UP CONTROL AND V_{AUX} REGULATOR					
V_{AUX} Regulation					V
Startup Threshold/V_{AUX} Regulation Peak (V_{AUX} increasing)	$V_{AUX(on)}$	TBD	11	TBD	
Minimum Operating V_{AUX} Valley Voltage After Turn–On	$V_{AUX(off)}$	TBD	7.0	TBD	
Hysteresis	V_H	–	4.0	–	
Start–up Circuit Output Current	I_{START}				mA
V_{AUX} = 0 V					
T_J = 25°C		11	17.6	TBD	
T_J = –40°C to 125°C		TBD	TBD	TBD	
V_{AUX} = $V_{AUX(on)}$ – 0.2 V					
T_J = 25°C		TBD	16.6	TBD	
T_J = –40°C to 125°C		TBD	TBD	TBD	
Start–up Circuit Off–State Leakage Current (V_{in} = 150 V)	$I_{START(off)}$				μA
T_J = 25°C		–	18	50	
T_J = 125°C		–	10	TBD	
Auxilliary Supply Current After V_{AUX} Turn–On					mA
Outputs Disabled					
V_{EA} = 0 V	I_{AUX1}	–	3.0	5.0	
$V_{UV/OV}$ = 0 V	I_{AUX2}	–	1.55	2.5	
Outputs Enabled	I_{AUX3}	TBD	4.6	TBD	
LINE UNDER/OVERVOLTAGE DETECTOR					
Undervoltage Threshold (V_{in} Increasing)	V_{UV}	1.42	1.52	1.62	V
Undervoltage Hysteresis	$V_{UV(H)}$	–	0.155	–	V
Overvoltage Threshold (V_{in} Increasing)	V_{OV}	3.52	3.55	3.72	V
Overvoltage Hysteresis	$V_{OV(H)}$	–	0.150	–	V
Undervoltage Propagation Delay to Output	t_{UV}	–	250	–	ns
Overvoltage Propagation Delay to Output	t_{OV}	–	160	–	ns
LINE FEEDFORWARD					
Feedforward Ramp Amplitude	$V_{FF(P–P)}$	–	2.7	–	V
CURRENT LIMIT AND THERMAL SHUTDOWN					
Cycle by Cycle Threshold Voltage	I_{LIM1}	0.44	0.47	0.50	V
Propagation Delay to Output (V_{EA} = 2.0 V) V_{CCS} = I_{LIM1} to 2.0 V, measured when OUT1 reaches 10 V.	t_{ILIM}	–	–	150	ns
Cycle Skip Threshold Voltage	I_{LIM2}	0.54	0.57	0.60	V
Cycle Skip Timer Period	T_{CSKIP}	–	1.2	–	ms
Thermal Shutdown Threshold (Junction Temperature Increasing) (Note 2)	T_{SHDN}	–	150	–	°C
Thermal Shutdown Hysteresis (Junction Temperature Decreasing) (Note 2)	T_H	–	25	–	°C

2. Guaranteed by design only.

ELECTRICAL CHARACTERISTICS (V_{in} = 48 V, V_{AUX} = 12 V, V_{EA} = 2 V, R_T = 100 kΩ, C_{CSKIP} = 6800 pF, R_D = 60.4 kΩ, R_{FF} = 464 kΩ, for typical values T_J = 25°C, for min/max values, T_J = –40°C to 125°C, unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (R_T = 100 kΩ) T_J = 25°C T_J = –40°C to 125°C	f_{OSC1}	 285 –	 300 –	 315 –	kHz
Frequency (R_T = 60.4 kΩ) T_J = 25°C T_J = –40°C to 125°C	f_{OSC2}	 – –	 500 –	 – –	kHz
MAXIMUM DUTY CYCLE COMPARATOR					
Maximum Duty Cycle (V_{in} = 36 V) R_P = 0 Ω, R_{MDP} = open R_P = open, R_{MDP} = open R_P = open, R_{MDP} = 100 kΩ	$D_{(max)}$	 57 76 –	 62 80 –	 65 84 –	%
SOFTSTART					
Charge Current (V_{SS} = 1.0 V)	$I_{SS(C)}$	5.0	6.0	7.0	μA
Discharge Current (V_{SS} = 5.0 V, $V_{UV/OV}$ = 3.75 V)	$I_{SS(D)}$	–	52.5	–	mA
PWM COMPARATOR					
Input Bias Current	I_{EA}	–	1.0	–	nA
Lower Input Threshold	$V_{FB(L)}$	–	0.7	–	V
Delay to Output (from X to X)	t_{PWM}	–	200	–	ns
5.0 V REFERENCE					
Output Voltage (I_{REF} = 0 mA) T_J = 25°C T_J = –40°C to 150°C	V_{REF}	 4.9 TBD	 5.0 TBD	 5.1 TBD	V
Load Regulation (I_{REF} = 0 to 10 mA)	$V_{REF(Load)}$	–	50	–	mV
Line Regulation (V_{AUX} = 7 to 11 V)	$V_{REF(Line)}$	–	50	–	mV
CONTROL OUTPUTS					
Overlap Delay (T_J = 25°C) Rd = open Leading Trailing Rd = 60 kΩ Leading Trailing	t_D	 – – – –	 220 170 85 70	 – – – –	ns
Output Voltage Low State (I_{SINK} = 10 mA) High State (I_{SOURCE} = 10 mA)	 V_{OL} V_{OH}	 – –	 0.25 11.0	 – –	V
Rise Time (C_L = 100 pF, 10% to 90%)	t_{on}	–	35	–	ns
Fall Time (C_L = 100 pF, 10% to 90%)	t_{off}	–	20	–	ns

Typical Characteristics

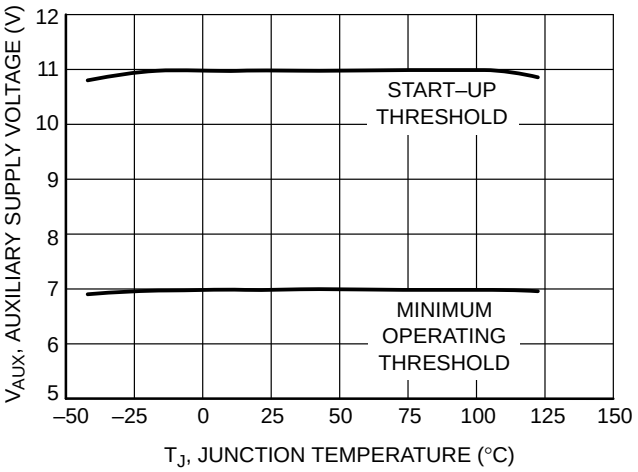


Figure 3. Auxiliary Supply Voltage Thresholds versus Junction Temperature

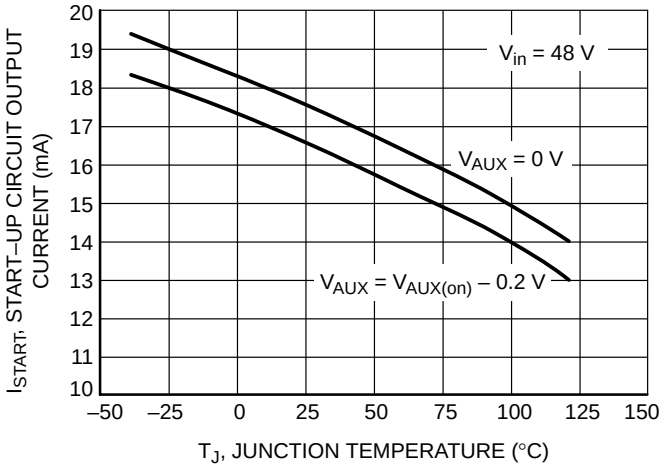


Figure 4. Start–up Circuit Output Current versus Temperature

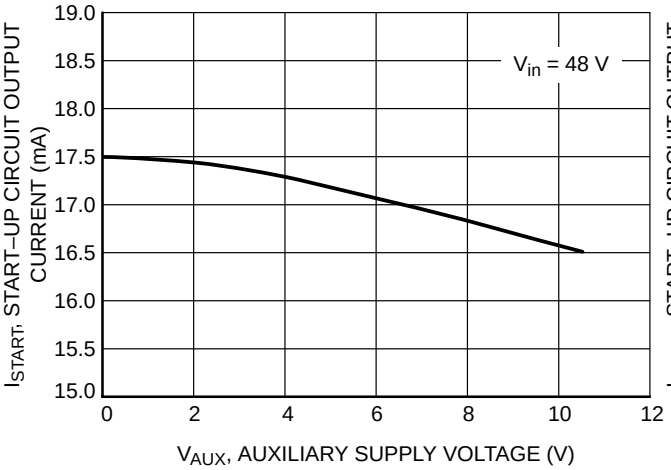


Figure 5. Start–up Circuit Output Current versus Auxiliary Supply Voltage

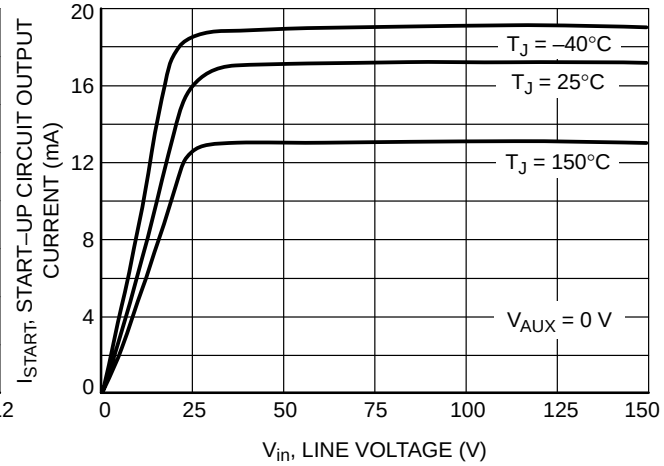


Figure 6. Start–up Circuit Output Current versus Line Voltage

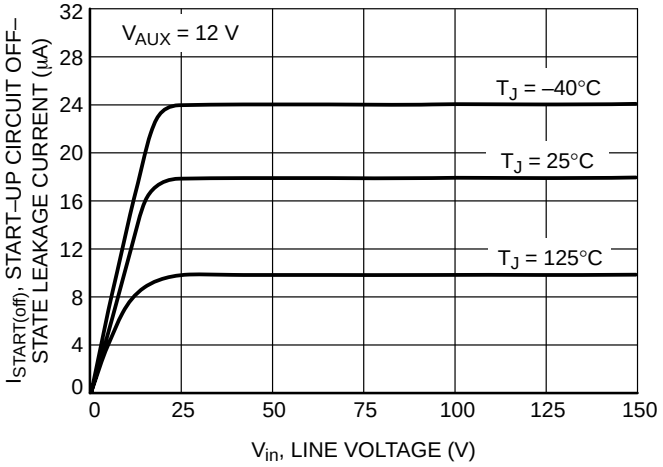


Figure 7. Startup Circuit Off–State Leakage Current versus Line Voltage

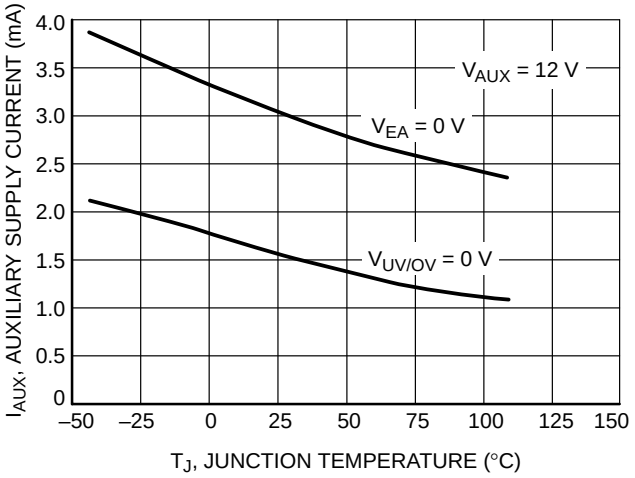


Figure 8. Auxiliary Supply Current versus Junction Temperature

Typical Characteristics

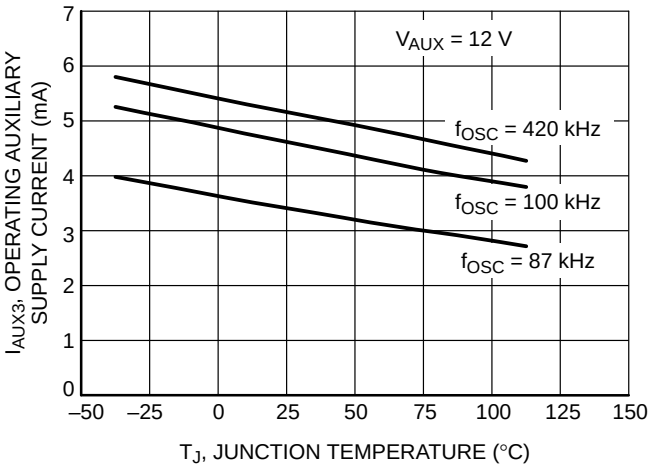


Figure 9. Operating Supply Current versus Junction Temperature

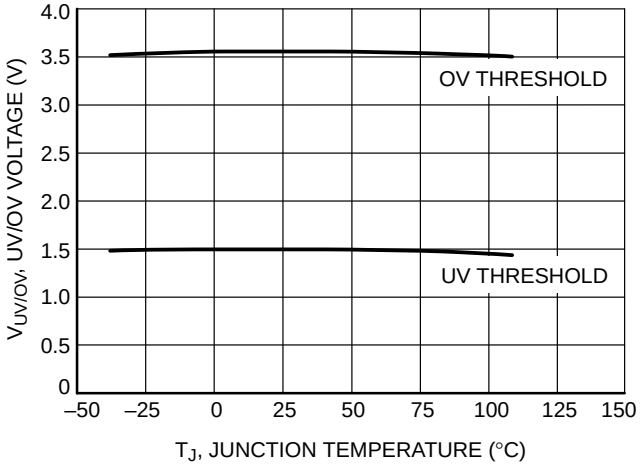


Figure 10. Line Under/Overvoltage Thresholds versus Junction Temperature

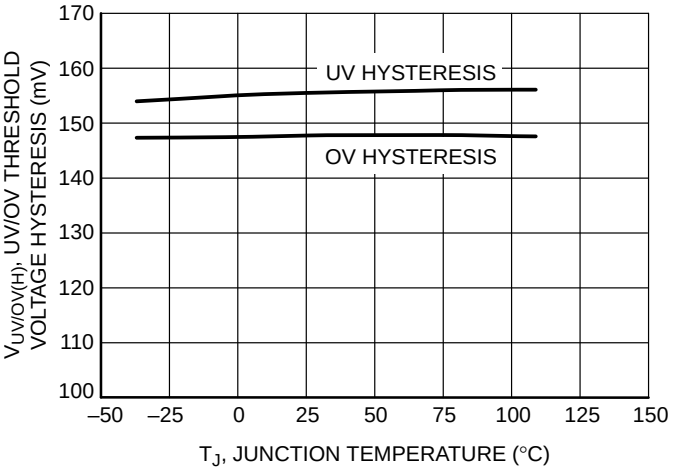


Figure 11. Line Under/Over Voltage Thresholds Hysteresis versus Junction Temperature

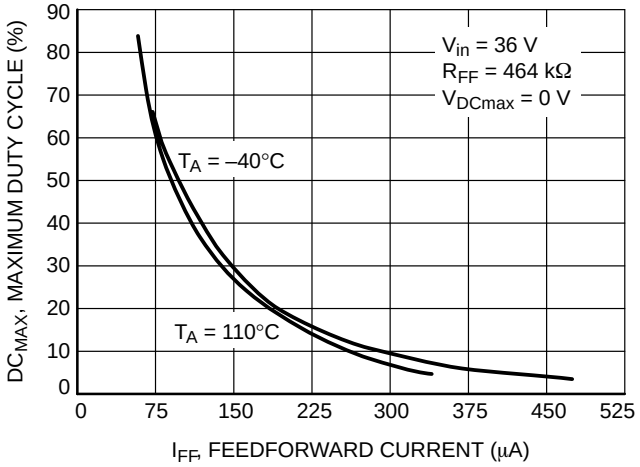


Figure 12. Maximum Duty Cycle versus Feedforward Current

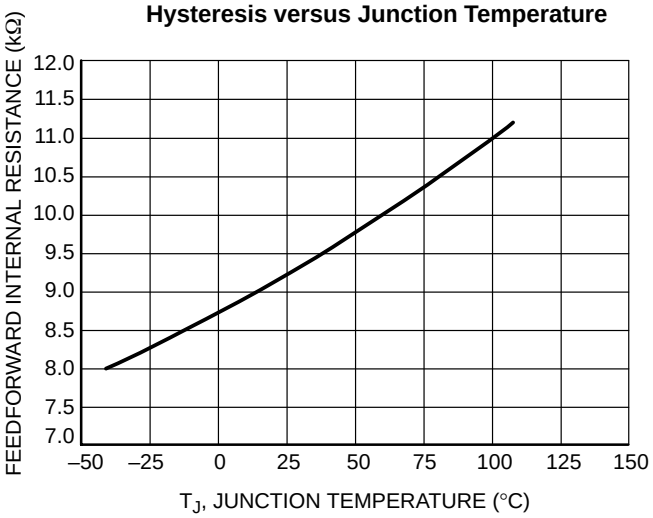


Figure 13. Feedforward Internal Resistance versus Junction Temperature

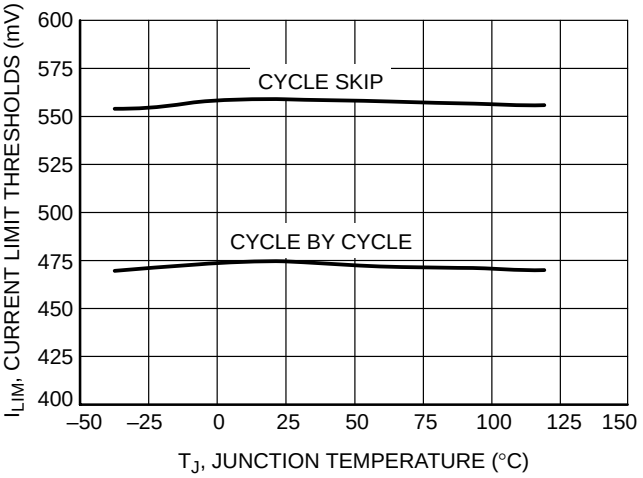


Figure 14. Current Limit Thresholds versus Junction Temperature

Typical Characteristics

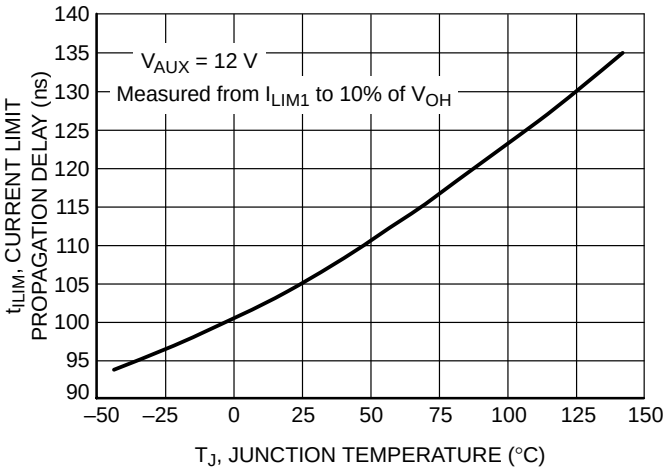


Figure 15. Current Limit Propagation Delay versus Junction Temperature

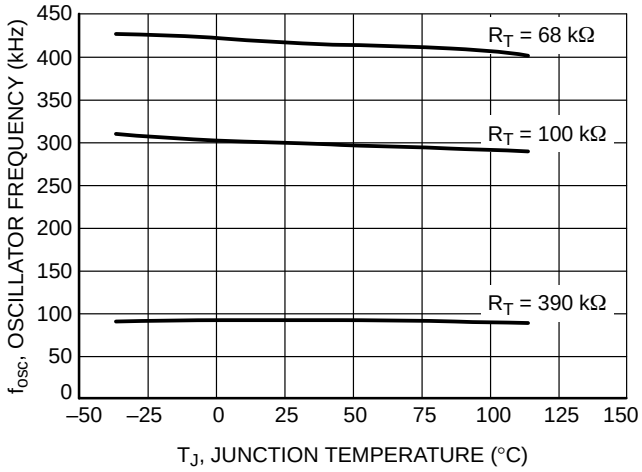


Figure 16. Oscillator Frequency versus Junction Temperature

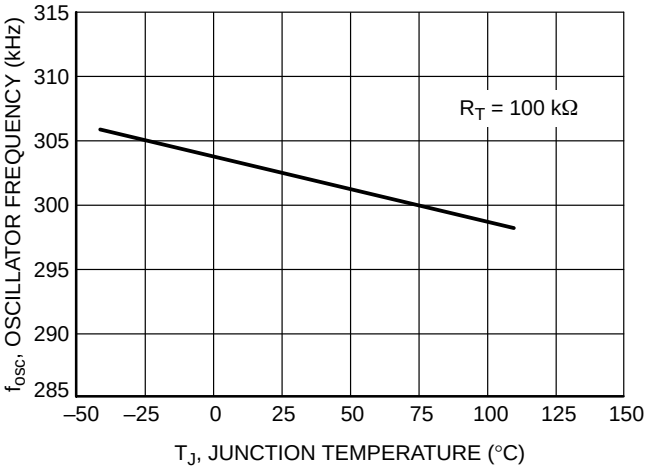


Figure 17. Oscillator Frequency versus Junction Temperature

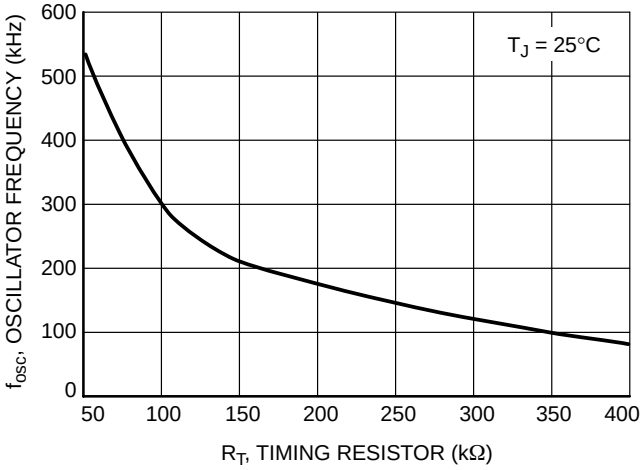


Figure 18. Oscillator Frequency versus Timing Resistor

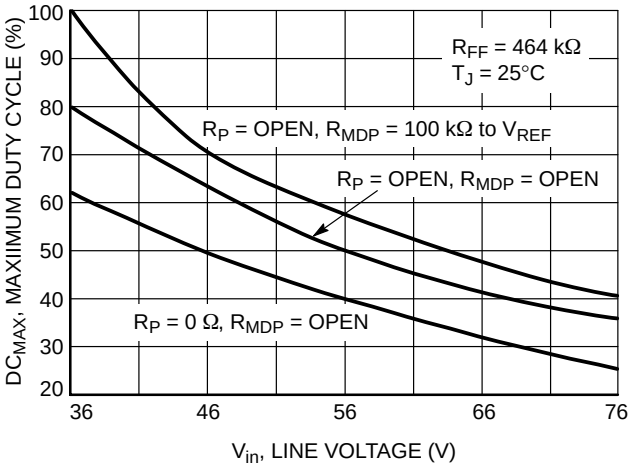


Figure 19. Maximum Duty Cycle versus Line Voltage

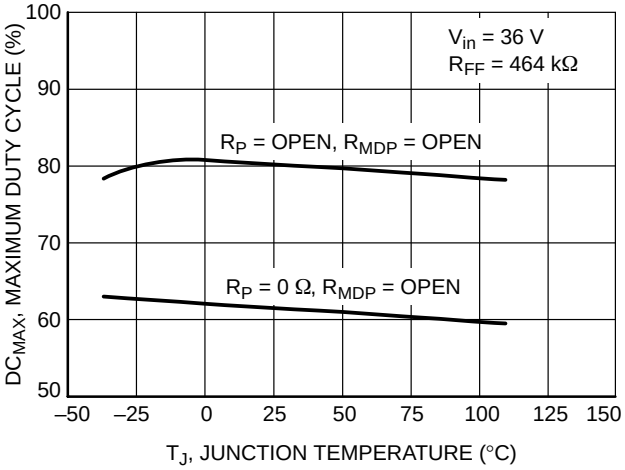


Figure 20. Maximum Duty Cycle versus Junction Temperature

Typical Characteristics

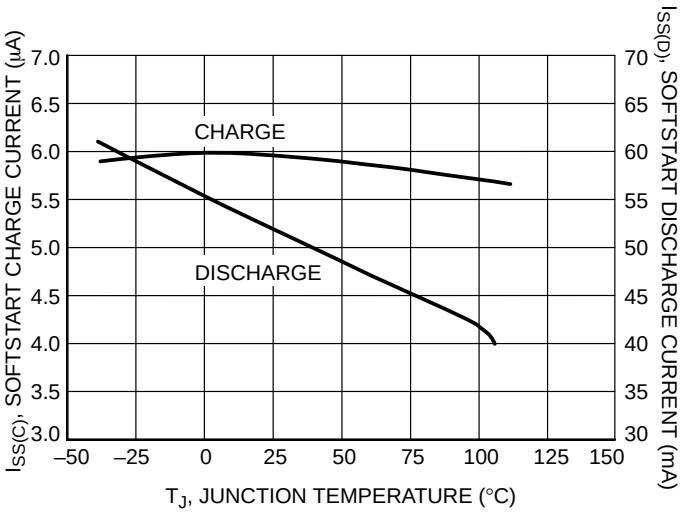


Figure 21. Softstart Charge/Discharge Currents versus Junction Temperature

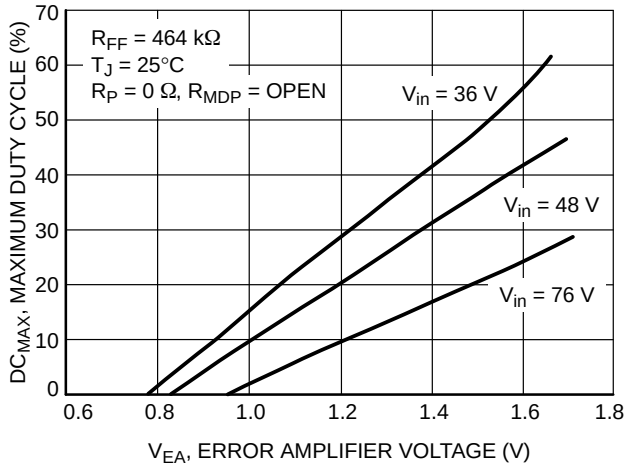


Figure 22. Maximum Duty Cycle versus Error Amplifier Voltage

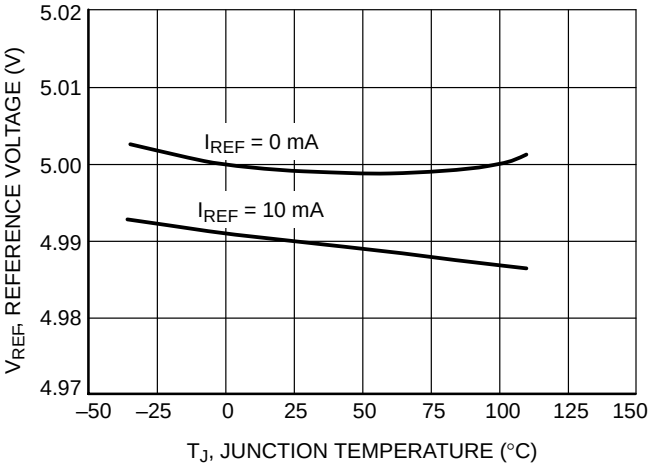


Figure 23. Reference Voltage versus Junction Temperature

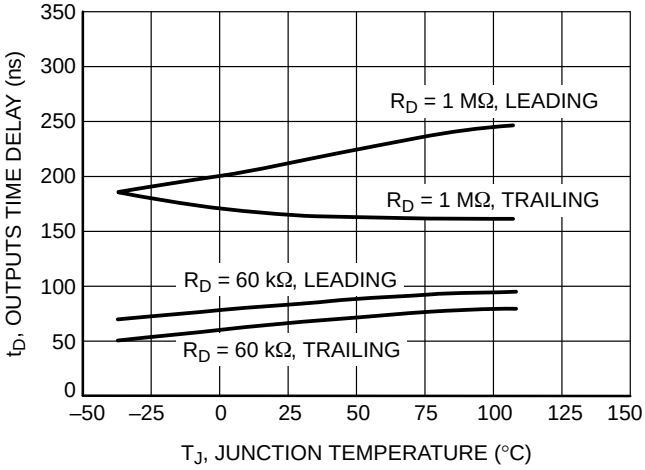


Figure 24. Outputs Overlap Delay versus Junction Temperature

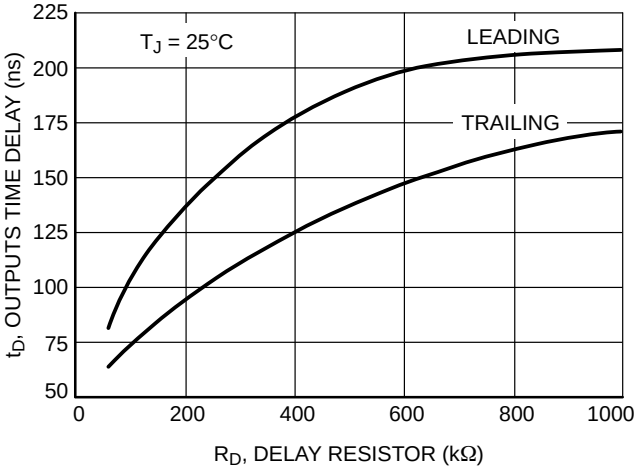


Figure 25. Outputs Overlap Delay versus Delay Resistor

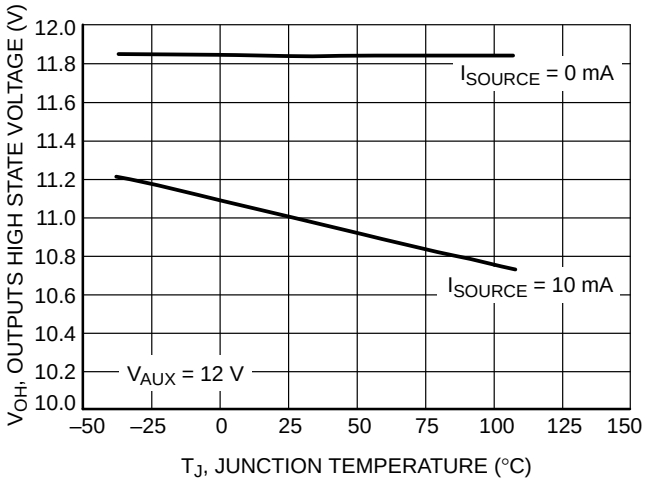


Figure 26. Outputs High State Voltage versus Junction Temperature

Typical Characteristics

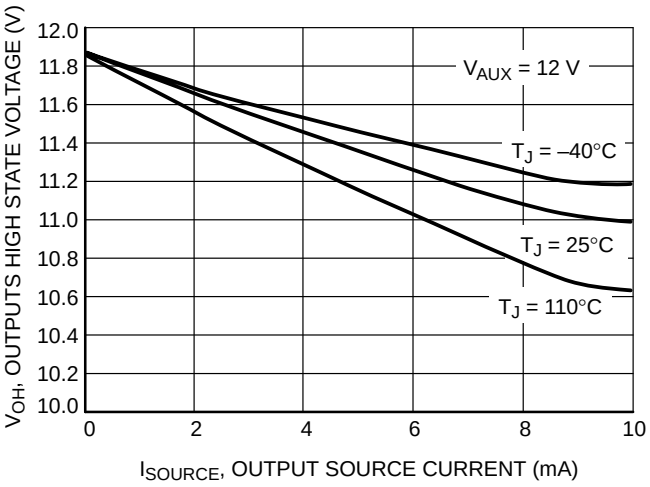


Figure 27. Outputs High State Voltage versus Output Current

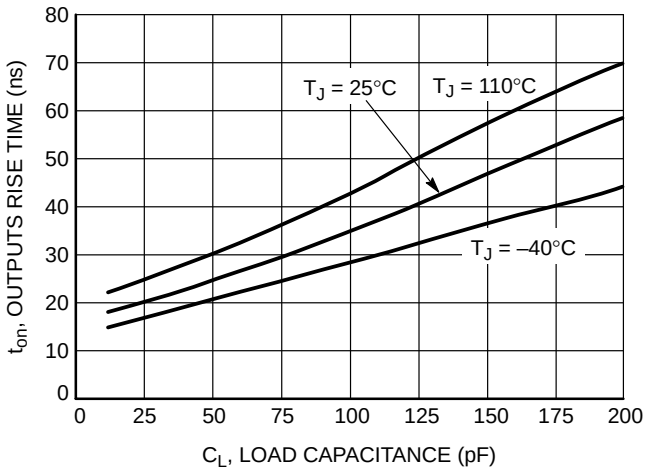


Figure 28. Outputs Rise Time versus Load Capacitance

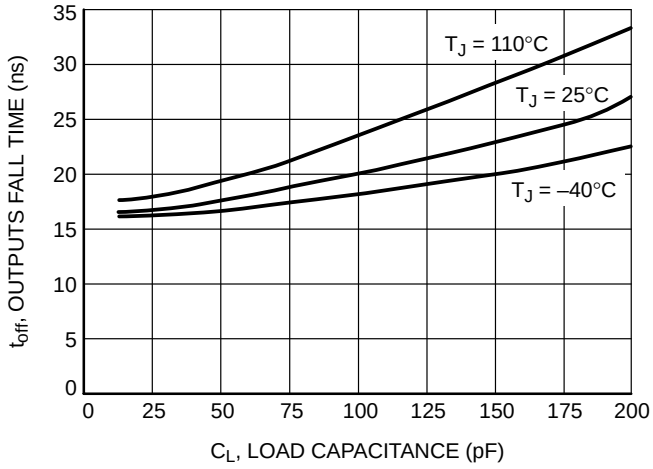


Figure 29. Outputs Fall Time versus Load Capacitance

DETAILED OPERATING DESCRIPTION

The NCP1560 PWM controller contains all the features and flexibility needed for implementation of Voltage–Mode Control for modern high performance power converters. This device cost effectively reduces system part count with the inclusion of a high voltage start–up regulator. The NCP1560 provides two control outputs, OUT1 which controls the main PWM switch and OUT2 with adjustable overlap delay, which can control a synchronous rectifier switch. Other distinctive features include: two mode overcurrent protection, line under/over voltage lockout, fast line feedforward, softstart and a maximum duty cycle clamp. The Functional Block Diagram is shown in Figure 2.

The NCP1560 is designed for Voltage–Mode Control converters. The features included in the NCP1560 enable all of the advantages of Current–Mode Control, fast line feedforward, and cycle by cycle current limit. It eliminates the disadvantages of low power jitter, slope compensation and noise susceptibility. Finally the dual outputs of the NCP1560 allow for optimum control of a synchronous rectifier switch.

High Voltage Start–up Regulator

The NCP1560 contains an internal high voltage start–up regulator that eliminates the need for external start–up components. In addition, this regulator increases the efficiency of the supply as it uses no power when in the normal mode of operation, but instead uses power supplied by an auxiliary winding.

The start–up regulator consists of a constant current source that supplies current from the input line voltage (V_{in}) to the capacitor on the V_{AUX} pin (C_{AUX}). The start–up current is typically 17 mA. Once V_{AUX} reaches 11 V, the outputs are

allowed to turn ON, as long as no faults are present. Once V_{AUX} reaches 7 V again, the outputs are immediately disabled with no overlap delay and the start–up regulator turns ON. This “7–11” mode of operation is known as Dynamic Self Supply (DSS). As the DSS sources current to the V_{AUX} pin, a diode should be placed between C_{AUX} and the auxiliary winding as shown in Figure 30. This will allow the NCP1560 to charge C_{AUX} while preventing the start–up regulator from biasing the auxiliary winding circuit.

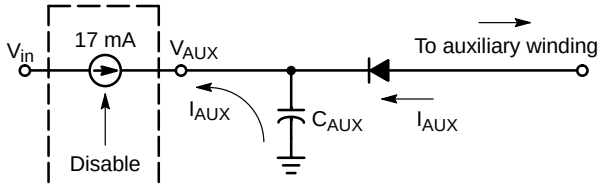


Figure 30. Recommended V_{AUX} Configuration

The V_{AUX} pin can be biased externally above 7 V once the main output starts switching to prevent the start–up regulator from turning ON. It is recommended to bias the V_{AUX} pin using an auxiliary winding. An independent voltage supply can also be used. However, if V_{AUX} is biased before the outputs start switching or when a fault is present, the One Shot Pulse Generator (Figure 2) won’t be enabled and the outputs will remain OFF.

Power to the controller while operating in the self–bias mode is provided by C_{AUX}. Therefore, C_{AUX} must be sized such that a V_{AUX} voltage greater than 7 V is maintained while the outputs are switching and the converter reaches regulation. Also, the V_{AUX} discharge time must be greater that the softstart charge period to assure the converter turns ON.

The start–up circuit is rated at a maximum voltage of 150 V. If the device operates in the DSS mode, power dissipation should be controlled to avoid exceeding the maximum power dissipation of the controller.

Line Under/Over Voltage Shutdown

The NCP1560 incorporates a line under/over voltage shutdown (UV/OV) circuit. The under voltage (UV) threshold is 1.49 V and the over voltage threshold (OV) is 3.60 V, for a ratio of 1:2.4.

The UV/OV circuit can be biased using an external resistor divider connected to the input voltage line. The resistor divider must be sized to enable the controller once V_{in} is within the required operating range. If the UV or OV threshold is reached, the softstart capacitor is discharged, and the outputs are immediately disabled with no overlap delay as shown in Figure 31. Also, if an UV condition is detected, the 5.0 V Reference Supply is disabled.

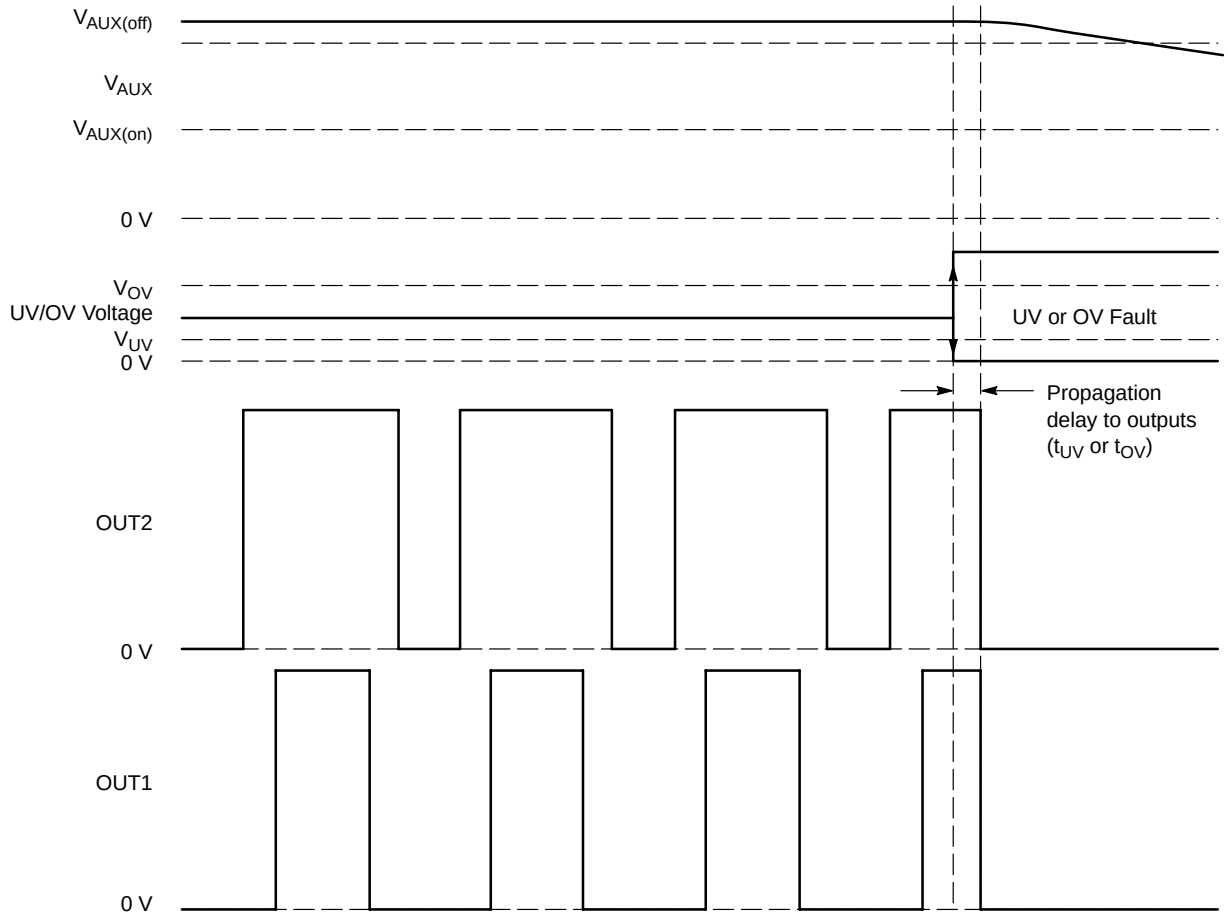


Figure 31. UV/OV Fault Timing Diagram

Once the UV or OV condition is removed, the controller initiates a softstart cycle and allows the outputs to switch once V_{AUX} reaches 11 V. Figure 32 shows the relationship between the UV/OV voltage, the outputs and the softstart voltage.

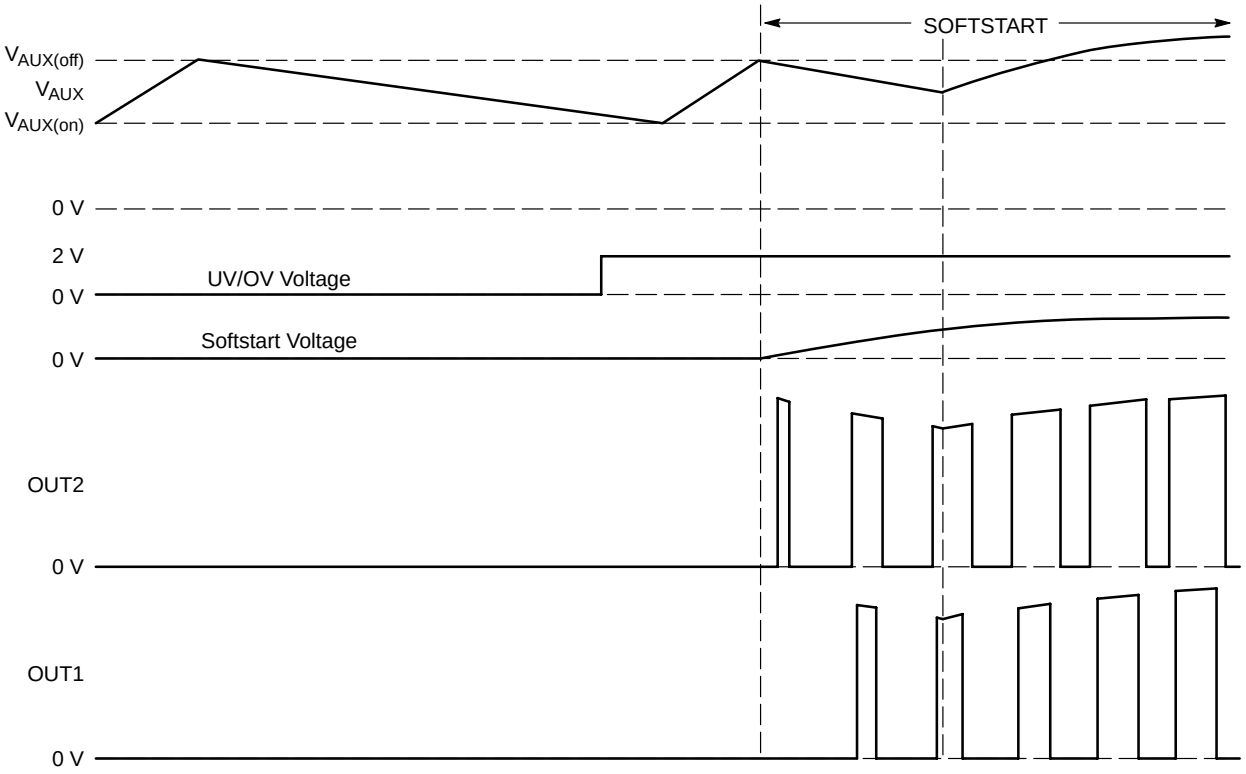


Figure 32. Softstart Timing Diagram (Using Auxiliary Winding)

The UV/OV pin can also be used to implement a remote enable/disable function. Biasing the UV/OV pin below its UV threshold disables the converter.

Feedforward Ramp Generator

The NCP1560 incorporates line feedforward (FF) to compensate for changes in line voltage. A FF Ramp proportional to V_{in} is generated and compared to V_{EA}. If the line voltage changes, the FF Ramp slope changes accordingly. The duty cycle will be adjusted immediately instead of waiting for the line voltage change to propagate around the system and be reflected back on V_{EA}.

A resistor between V_{in} and the FF pin (R_{FF}) sets the feedforward current (I_{FF}). The FF Ramp is generated by charging an internal 10 pF capacitor (C_{FF}) with a constant current proportional to I_{FF}. The FF Ramp is finished (capacitor is discharged) once the Oscillator Ramp reaches 2.0 V. Please refer to Figure 2 for a detailed description of the Feedforward Ramp generator.

I_{FF} is usually a few hundred microamps, depending on the operating frequency and the required duty cycle. If the operating frequency and maximum duty cycle are known, I_{FF} is calculated using the equation below:

$$I_{FF} = \frac{C_{FF} \times V_{DC(inv)} \times 62.5\ k\Omega}{3.6\ k\Omega \times t_{on(max)}}$$

where $V_{DC(inv)}$ is the voltage on the inverting input of the Max DC Comparator and $t_{on(max)}$ is the maximum ON time. Figure 12 shows the relationship between I_{FF} and DC_{MAX} at 36 V. For example, if a system is designed to operate at 300 kHz, with a 60% maximum duty cycle, DC_{MAX} pin is grounded and a minimum line voltage of 36 V, I_{FF} is calculated as follows:

$$T = \frac{1}{f} = \frac{1}{300\ kHz} = 3.33\ \mu s$$

$$t_{on(max)} = DC_{MAX} \times T = 0.6 \times 3.33\ \mu s = 2.0\ \mu s$$

$$I_{FF} = \frac{C \times V_{DC(inv)} \times 62.5\ k\Omega}{3.6\ k\Omega \times t_{on(max)}} =$$

$$\frac{10\ pF \times 0.888\ V \times 62.5\ k\Omega}{3.6\ k\Omega \times 2.0\ \mu s} = 77.2\ \mu A$$

If the minimum line voltage is 36 V, the required feedforward resistor is calculated using the equation below:

$$R_{FF} = \frac{V_{in}}{I_{FF}} - 9.25\ k\Omega = \frac{36\ V}{77.2\ \mu A} - 9.25\ k\Omega \approx 464\ k\Omega$$

From the above calculations it can be observed that I_{FF} is controlled predominantly by the value of R_{FF}, as the feedforward internal resistance is only 9.25 kΩ. If a tight maximum duty cycle control over temperature is required, R_{FF} should have a low thermal coefficient.

Current Limit

The NCP1560 has two over current protection modes, cycle by cycle and cycle skip. It allows the NCP1560 to handle momentary and hard shorts differently for the best tradeoff in performance and safety. The outputs are disabled typically 120 ns after a current limit fault is detected.

The cycle by cycle mode terminates the conduction cycle (reducing the duty cycle) if the voltage on the CS pin exceeds 0.47 V. The cycle skip mode is enabled if the voltage on the CS pin reaches 0.55 V. Once a cycle skip fault is detected, the outputs are turned OFF, the softstart and cycle skip capacitors are discharged, and the cycle skip period (T_{CSKIP}) commences.

The cycle skip period is set by an external capacitor (C_{CSKIP}). Once a cycle skip fault is detected, the cycle skip capacitor is discharged followed by a charge cycle. The charge current is 11 μA. The cycle skip period ends when the voltage on the cycle skip capacitor reaches 2.0 V. The cycle skip period is calculated as follows:

$$C_{CSKIP} \approx \frac{T_{CSKIP} \times 2\ V}{11\ \mu A}$$

Using the above equation, a cycle skip period of 12.3 μs requires a cycle skip capacitor of 68 pF. The differences between the cycle by cycle and cycle skip modes can be observed in Figure 33.

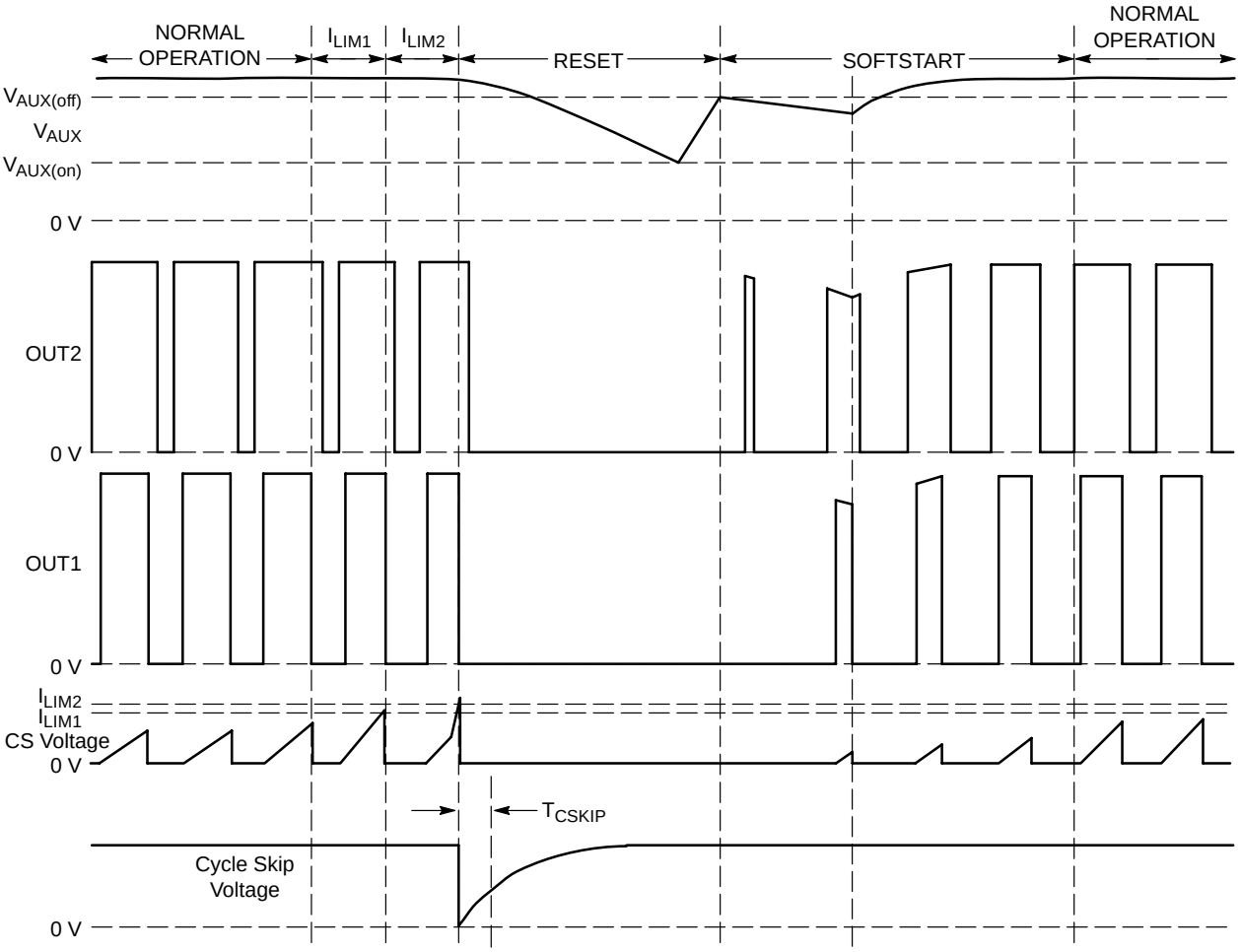


Figure 33. Over Current Faults Timing Diagram

Once the cycle skip period is complete and V_{AUX} reaches 11 V, a softstart sequence commences. The minimum possible OFF time is set by C_{CSKIP}. However, the actual OFF time is generally greater than the cycle skip period because it is the cycle skip period added to the time it takes V_{AUX} to reach 11 V.

Oscillator

The NCP1560 oscillator frequency is set by a single external resistor connected between the R_T pin and GND. The oscillator is designed to operate up to 500 kHz.

The voltage on the R_T pin is laser trim adjusted during manufacturing to 1.3 V for an R_T of 100 kΩ. A current set by R_T generates an Oscillator Ramp by charging an internal 10 pF capacitor as shown in Figure 2. The period ends (capacitor is discharged) once the Oscillator Ramp reaches 2.0 V. If R_T increases, the current and the Oscillator Ramp slope decrease, thus reducing the frequency. If R_T decreases, the opposite effect is obtained. Figure 17 shows the oscillator frequency vs R_T.

Maximum Duty Cycle

A dedicated internal comparator limits the maximum ON time of OUT1 by comparing the FF Ramp to the voltage on the inverting terminal of the Max DC Comparator. If the FF Ramp voltage exceeds $V_{DC(inv)}$, the output of the Max DC Comparator goes high. This will reset the Output Latch, thus turning OFF the outputs and limiting the duty cycle.

By definition, duty cycle is defined as:

$$DC = \frac{t_{on}}{T} = t_{on} \times f$$

Therefore, the maximum ON time can be set to yield the desired DC if the operating frequency is known. The maximum ON time is set by adjusting the FF Ramp to reach $V_{DC(inv)}$ in a time equal to $t_{on(max)}$ as shown in Figure 34. The maximum ON time should be set for the minimum line voltage. As line voltage increases, the slope of the FF Ramp increases. This reduces the duty cycle below DC_{MAX}, which is a desirable feature as the duty cycle is inversely proportional to the line voltage.

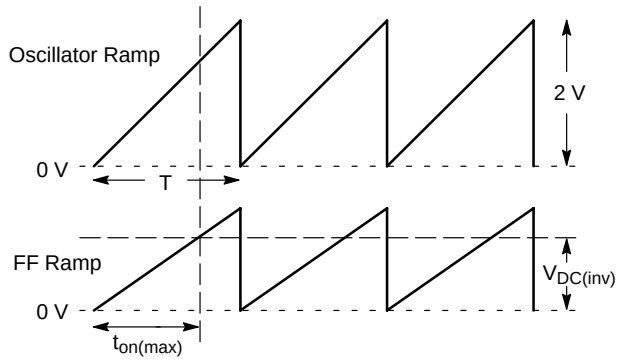


Figure 34. Maximum ON Time Limit Waveforms

An internal resistor divider from a 2.0 V reference is used to set $V_{DC(inv)}$. If the DC_{MAX} pin is grounded, $V_{DC(inv)}$ is 0.88 V. If the pin is floating, $V_{DC(inv)}$ is 1.19 V. This is equivalent to 60% or 80% of a 1.5 V FF Ramp. $V_{DC(inv)}$ can be adjusted to other values by using an external resistor network on the DC_{MAX} pin. For example, if the minimum line voltage is 36 V, R_{FF} is 464 kΩ, operating frequency is 300 kHz with a maximum duty cycle of 70%, $V_{DC(inv)}$ is calculated as follows:

$$V_{DC(inv)} = \frac{I_{FF} \times 3.6\ k\Omega \times t_{on(max)}}{C_{FF} \times 62.5\ k\Omega}$$

$$V_{DC(inv)} = \frac{77.2\ \mu A \times 3.6\ k\Omega \times 2.33\ \mu s}{10\ pF \times 62.5\ k\Omega} = 1.03\ V$$

This can be implemented by connecting a 16.9 kΩ resistor from the DC_{MAX} pin to GND. The maximum duty cycle limit can be disabled connecting a 100 kΩ resistor between the DC_{MAX} and V_{REF} pins.

5.0 V Reference

The NCP1560 includes a precision 5.0 V reference output. The reference output is biased directly from V_{AUX} and it can supply up to 10 mA. Line and load regulation are 50 mV within the specified operating range.

It is recommended to bypass the reference output with a 0.1 μF ceramic capacitor. The reference output is only disabled when an UV fault is detected.

PWM Comparator

The output of an external error amplifier is compared to the FF Ramp by means of the PWM Comparator. The external error amplifier drives the V_{EA} input. There is a 0.65 V offset between the V_{EA} input and the PWM Comparator inverting input. The offset is provided by a series diode and resistor. If the voltage on the V_{EA} input is below 0.65 V, the PWM Comparator output is high and the outputs turn OFF.

The PWM Comparator controls the duty cycle by turning OFF the outputs once the FF Ramp voltage exceeds the offset V_{EA} voltage.

Softstart

The softstart (SS) feature allows the converter to gradually reach steady state operation, thus reducing start–up stresses and surges on the system. The duty cycle is limited during a softstart sequence by comparing the Oscillator Ramp to the SS voltage (V_{SS}) by means of the Softstart Comparator.

A 6.0 μA current source starts to charge the capacitor connected to the SS pin once no faults are present and V_{AUX} reaches 11 V. The Softstart Comparator controls the duty cycle as long as the SS voltage is below 2.0 V. Once V_{SS} is above 2.0 V, it exceeds the Oscillator Ramp voltage and the duty cycle is not limited any more by the Softstart Comparator. Figure 35 shows the relationship between the outputs duty cycle and the softstart voltage.

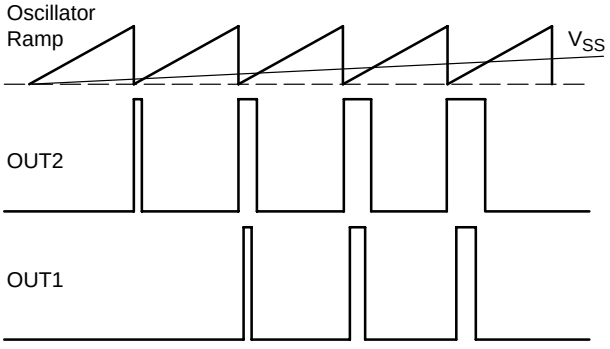


Figure 35. Softstart Timing Diagram

If the softstart period is too long, V_{AUX} will discharge to 7 V, turning OFF the outputs before the converter output is completely in regulation. If the converter output is not completely discharged when the outputs are re–enabled, the converter will eventually reach regulation exhibiting a non–monotonic startup behavior. But, if the converter output is completely discharged when the outputs are re–enabled, the cycle will repeat and the converter will not start.

In the event of a UV, OV, thermal shutdown, or cycle skip fault, the softstart capacitor is discharged. Once the fault is removed, a softstart cycle commences. The softstart steady state voltage is approximately 4.1 V.

Control Outputs

The NCP1560 has two in–phase control outputs, OUT1 and OUT2, with adjustable overlap delay (t_D). OUT2 precedes OUT1 during a low to high transition and OUT1 precedes OUT2 at any high to low transition. Figure 36 shows the relationship between OUT1 and OUT2.

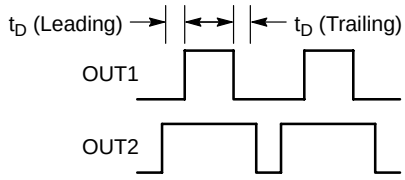


Figure 36. Control Outputs Timing Diagram

Generally, OUT1 controls the main switching element. OUT2, once inverted, can drive the free wheeling synchronous rectifier switching element. The overlap delay prevents simultaneous conduction.

Once V_{AUX} reaches 11 V, the internal start–up circuit is disabled and the One Shot Pulse Generator is enabled. If no faults are present, the outputs turn ON. Otherwise, the outputs remain OFF until the fault is removed and V_{AUX} reaches 11 V again.

The control outputs are biased from V_{AUX}. The outputs can supply up to 10 mA each and their high state voltage is usually 0.8 V below V_{AUX}. Therefore, the control outputs load should be considered when designing the auxiliary winding supply.

If the control outputs need to drive a large capacitive load, a driver should be used between the NCP1560 and the load. The MC33152 is a good selection for an integrated driver. Figures 28 and 29 shows the relationship between the output rise and fall times vs capacitive load.

Time Delay

The overlap delay between the outputs is controlled using a single resistor (R_D) between the t_D and V_{REF} pins. A minimum time delay of 80 ns is obtained when R_D is 60 kΩ. If R_D is not present, the delay is 210 ns.

The output duty cycle can be adjusted from 0% to 100% selecting appropriate values of R_{FF} and $V_{DC(inv)}$. It should be note that OUT2 will reach 100% duty cycle before OUT1 because of the overlap delay. Therefore, if OUT2 is used to control a synchronous rectifier, the maximum duty cycle needs to be less than 100% depending on the selected t_D. The allowable time delay depends on the maximum duty cycle and frequency of operation. The maximum time delay is calculated using the equation below.

$$t_{D(max)} \leq \frac{(1 - DC)}{2f}$$

For example, if the converter operates at a frequency of 300 kHz with a maximum duty cycle of 80%, the maximum allowed time delay is 333 ns. However, this is a theoretical limit and variations over the complete operating range should be considered.

Thermal Protection

Internal Thermal Shutdown Circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 150°C, the controller is forced into a low power reset state, discharging the softstart capacitor and disabling the output drivers and the bias regulator. Once the junction temperature falls below 125°C, the NCP1560 enters a softstart mode and it is allowed to resume normal operation. This feature is provided to prevent catastrophic failures from accidental device overheating.

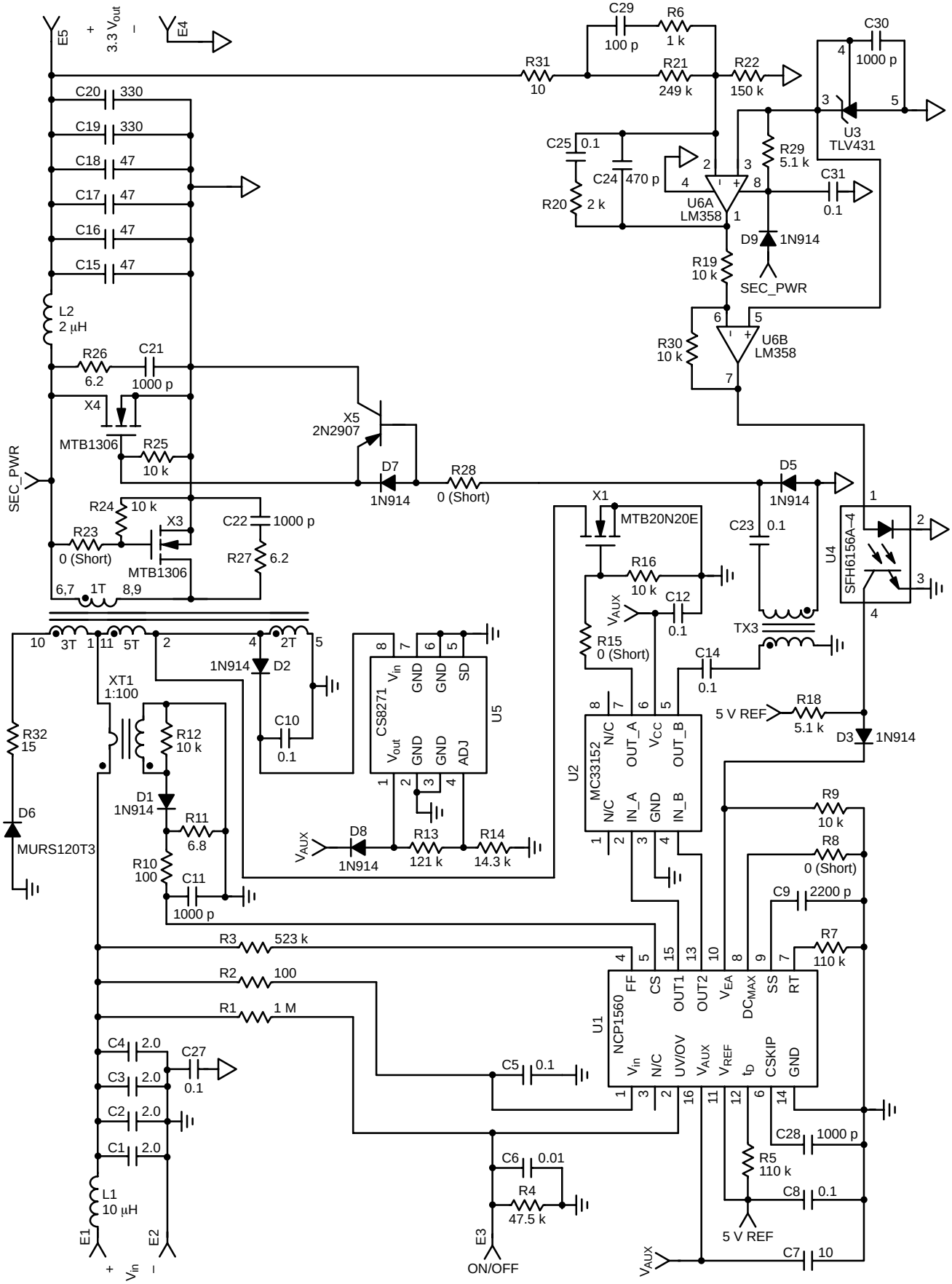


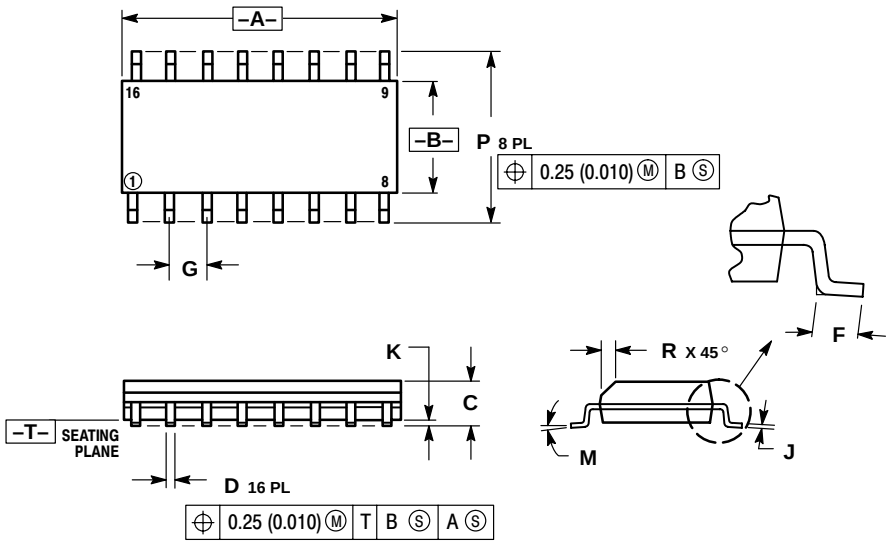
Figure 37. 100 W Reference Design

REFERENCE DESIGN BILL OF MATERIALS

Quantity	Reference	Part/Description	Value	Vendor	Notes
4	C1 – C4	CKG45DX7R2A225M			
7	D1 – D3, D5, D7–D9	MMBD914LT1			High Speed Diode
1	D6	MURS120T3			Ultrafast Rectifier, 200 V
8	C8,C10,C12,C14, C23,C25,C27,C31	C1206C104K5RAC	0.1 μF, 50 V		
4	C15 – C18	C4532X5R0J476M	4.7 μF, 6.3 V		
2	C19 – C20	T495X337K006AS	330 μF, 6.3 V		
5	C11, C21, C22, C28, C30	C0805C102K1RAC	1000 pF, 100 V		
1	C5	C3216X7R2A104K	0.1 μF, 100 V	TDK	
1	C6	C0805C103K5RAC	0.01 μF, 50 V	KEMET	
1	C7	C5750X7R1E106M	10 μF, 25 V	TDK	
1	C9	VJ1206Y222KXXA	2200 pF, 25 V	VISHAY	
1	C24	C0805C471J1GAC	470 pF, 100 V	KEMET	
1	C29	C0805C101J1GAC	100 pF, 100 V	KEMET	
1	R1	CRCW1206105J	1 MΩ		
2	R2, R10	CRCW1206101J	100 Ω		
1	R3	RK73H2B–5233F	523 kΩ		
1	R4	RK73H2B–4752F	47.5 kΩ		
1	R5	CRCW12061003F	100 kΩ		
1	R6	CRCW1206102J	1 kΩ		
1	R7	CRCW12061103F	110 kΩ		
4	R8, R15, R23, R28		0 Ω		Short
1	R9	CRCW1206103J	10 kΩ		
1	R11	CRCW12066R81F	6.81 Ω		
5	R12, R16, R19, R24, R25	CRCW1206103J	10 kΩ		
1	R13	CRCW12061213F	121 kΩ		
1	R14	CRCW12061432F	14.3 kΩ		
2	R18, R29	CRCW1206512J	5.1 kΩ		
1	R20	CRCW1206202J	2.0 kΩ		
1	R21	CRCW12062493F	249 kΩ		
1	R31	CRCW1206100J	10 Ω		
1	R32	1W015	15 Ω	RESISTOR–NTE	1 Watt
1	TX1	CS105		Vanguard Electronics	Current Transformer
1	TX2	9452 (Custom)		Payton	Power Transformer
1	TX3	GD103		Vanguard Electronics	Isolation Transformer
1	U1	NCP1560		ON Semiconductor	PWM Controller
1	U2	MC33152		ON Semiconductor	Dual MOSFET Driver
1	U3	TLV431ASNT1		ON Semiconductor	Voltage Regulator
1	U4	SFH6156–4		Infineon	Optocoupler
1	U5	CS8271		ON Semiconductor	Voltage Regulator
1	U6	LM358D		ON Semiconductor	Dual OpAmp
1	X1	MTB20N20E		ON Semiconductor	Power MOSFET, 200 V
2	X3, X4	MTB1306		ON Semiconductor	Power MOSFET, 30 V
1	X5	MMBT2907AWT1		ON Semiconductor	PNP Transistor
1	L1	DO3316–103	10 μH	Coilcraft	Input Choke
1	L2	9453 (Custom)	2 μH	Payton	Output Choke

PACKAGE DIMENSIONS

SO–16
D SUFFIX
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

The product described herein (NCP1560) may be covered by one or more U.S. patents. There may be other patents pending.

PUBLICATION ORDERING INFORMATION

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