Atmel LED Drivers

MSL2023 / MSL2024

2-String LED Driver with Individual PWM Dimming and Adaptive Headroom Control for High CRI LED Luminaires

Features

- Dual-string LED driver for 2-color or 2 unequal V_F LEDs
- Phase shifted register controlled dimming (MSL2023)
- Individual PWM inputs (MSL2024)
- Adaptively controls headroom of AC/DC or DC/DC, isolated or non-isolated topologies
- Main LED string driven by linear current controller
  - Drives external N-channel MOSFET
  - ± 3% current accuracy, no ripple current
  - 8-bit DAC for peak current control
- Color-adjust LED string uses floating buck controller
  - Drives external N-channel MOSFET
  - Over 100:1 dimming range
  - Open and short LED detection
  - 8-bit DAC allows changing current sense threshold
- I^2C accessible driver settings and EEPROM
- Open-drain fault indicator output
- -40°C to +105°C operating temperature range

Typical Applications

- General and architectural lamps
- High CRI LED fixtures
- Down lights and recessed lights
- PAR lamps

1. Introduction

The MSL2023/24 LED drivers for two-color systems include a linear current controller for the main string, typically for white LEDs, and a second floating buck controller for a color-adjust LED string. Both the switching and linear controllers drive external MOSFETs to provide flexibility over a wide range of power levels (LED currents and voltages).

The MSL2023/24 adaptively manage the voltage powering the main LED string. A proprietary and patent pending efficiency optimizer algorithm controls the voltage output of any AC/DC or DC/DC isolated or non-isolated topology, including ultra-low bandwidth single-stage PFC flyback controller.

The MSL2023/24 feature peak current control and individual string PWM dimming. The MSL2023 features individual, register controlled, 180° out of phase PWM dimming at 400Hz. The MSL2024 offers individual string PWM inputs.

The MSL2023/24 operate from a 9.5V to 15V power supply. The Main LED string is driven by a high accuracy, ripple free linear current controller. The color-adjust string voltage regulation loop uses a constant off-time control algorithm to achieve stable control with good transient behavior. For flexibility of design, off-time is set using an external resistor. LED current in both strings can be adjusted using internal 8-bit DACs.

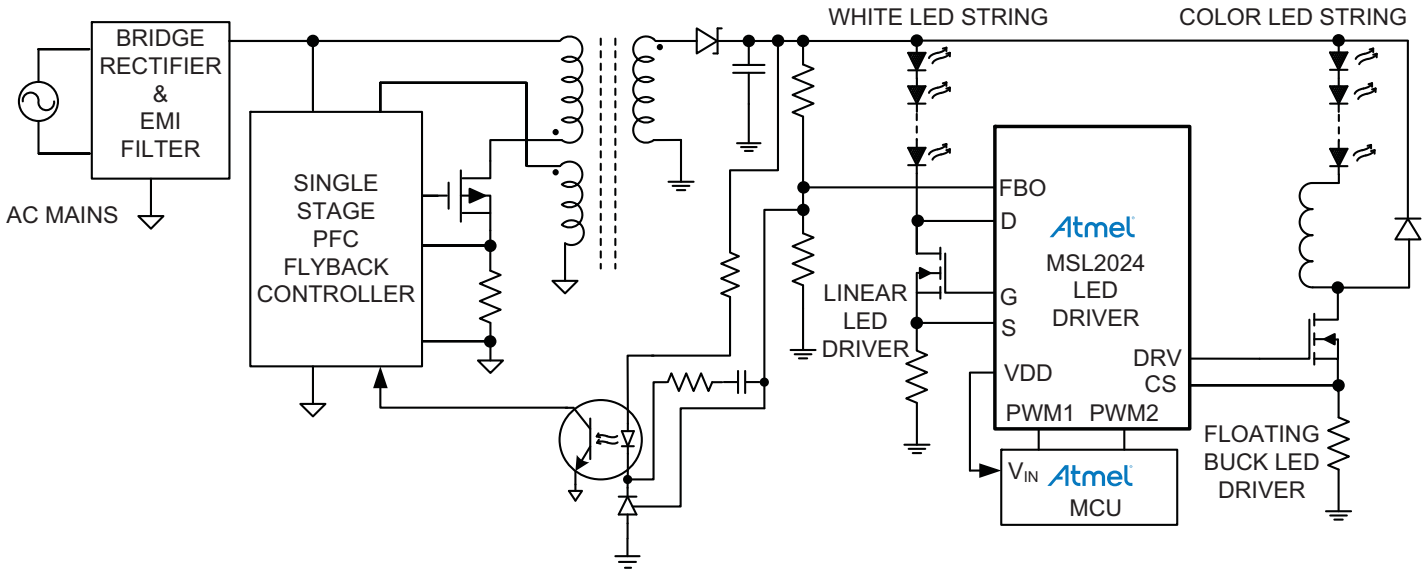
The MSL2023/24 are available in space-saving 24-pin 4x4mm QFN package and operate over the extended -40°C to 105°C operating range.

2. Ordering Information

Ordering code	Description	Package[1]
MSL2023IN	Two String LED Driver	4 x 4mm 24-pin QFN
MSL2024IN	Two String LED Driver	4 x 4mm 24-pin QFN

Note: 1. Lead-Free, Halogen-Free, RoHS Compliant Package

3. Application Circuit



4. Absolute Maximum Ratings

Voltage with respect to AGND		
	AVIN, PVIN, EN	-0.3V to +16.5V
	VCC, PWM1, PWM2, FLTB, SDA, SCL, TOFF, REXT, FBO	-0.3V to +5.5V
	VDD	-0.3V to +2.75V
	CS, S	-0.3V to VDD+0.3V
	D	-0.3V to +22V
	G, DRV	-0.3V to VIN+0.3V
	PGND	-0.3V to +0.3V

Current (into pin)		
	AVIN, PVIN, DRV, G (average)	100mA
	PVIN (peak, =1% duty)	1A
	DRV, G (peak, =1% duty)	±1A
	PGND (peak, =1% duty)	-1A
	AGND, PGND (average)	-100mA
	All other pins	±10mA

Continuous Power Dissipation at 70°C		
	24-Pin 4mm x 4mm VQFN (derate 21.8mW/°C above TA = +70°C)	1200mW

Ambient Operating Temperature Range	-40°C to +105°C
Junction Temperature	+125°C
Storage Temperature Range	-65°C to +125°C
Lead Soldering Temperature, 10s	+300°C

5. Electrical Characteristics

AVIN = PVIN = 12V, -40°C ≤T_A ≤ 105°C, Typical Operating Circuit, unless otherwise noted.
Typical values at T_A = +25°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DC Electrical Characteristics						
AVIN, PVIN Operating Supply Voltage			9.5	12	15	V
AVIN Operating Supply Current		LEDs on at PWM = 100%, serial interface idle		10		mA
AVIN Idle Supply Current		EN = SLEEP = 1, all digital inputs = 0		7	10	mA
PVIN Idle Supply Current		EN = SLEEP = 1, all digital inputs = 0		0		µA
AVIN Disable Supply Current		V_{EN} = 0, all digital inputs = 0			5	µA
VCC Regulation Voltage		I_{VCC} = 10mApeak(7)	4.5	5	5.5	V
VDD Regulation Voltage		I_{VDD} = 10mApeak(7)	2.25	2.5	2.75	V
PWM1, PWM2, SCL, SDA Input High Voltage			0.7∗V_{VDD}			V
PWM1, PWM2, SCL, SDA Input Low Voltage					0.3∗V_{VDD}	V
EN Input High Voltage			2			V
EN Input Low Voltage					0.5	V
EN Input Hysteresis				100		mV
SDA, FLTB Output Low Voltage		Sinking 6mA			0.3	V
SCL, SDA, PWM1, PWM2, FLTB leakage current			-5		5	µA
S Current Sense Regulation Voltage		MREF = 0x64	194	200	206	mV
S Current Sense Regulation Voltage Accuracy		Main string at 100% duty cycle, T_A = 25°C, MREF = 0x64	-3		+3	%
S Current Sense Regulation Voltage Temperature Coefficient				-220		ppm/ºC
G Maximum Output Voltage			AVIN - 3.5		AVIN - 2.0	V
D Regulation Threshold		EOCTRL = 0xE5	0.9	1	1.1	V
CS Current Sense Regulation Voltage		CAREF = 0x64		200		mV
DRV Impedance		V_{DRV} = 12V, I_{DRV} = 20mA		5.6	9	Ω
		V_{DRV} = 0V, I_{DRV} = -20mA		5.6	9	Ω

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
FBO Full Scale Current			170	255	340	µA
FBO LSB Current				1.0		µA
Thermal Shutdown Temperature		Temperature rising		133		°C
Thermal Shutdown Hysteresis				15		°C
AC Electrical Characteristics						
DRV t_{OFF} timing		R_{TOFF} = 45.3kΩ		0.5		µs
PWM Input Frequency		PWM1[8]	60		22,000	Hz
		PWM2[8]	100		500	Hz
PWM Duty Cycle		PWM1, PWM2	1		100	%
PWM Duty Cycle Resolution		MSL2023		0.024		%
I²C Switching Characteristics						
SCL Clock Frequency		[1]	0.05		1,000	kHz
STOP to START Condition Bus Free Time	t_{BUF}		0.5			µs
Repeated START condition Hold Time	$t_{HD:STA}$		0.26			µs
Repeated START condition Setup Time	$t_{SU:STA}$		0.26			µs
STOP Condition Setup Time	$t_{SU:STOP}$		0.26			µs
SDA Data Hold Time	$t_{HD:DAT}$		5			ns
SDA Data Valid Acknowledge Time		[2]	0.05		0.55	µs
SDA Data Valid Time		[3]	0.05		0.55	µs
SDA Data Set-Up Time	$t_{SU:DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		0.5			µs
SCL Clock High Period	t_{HIGH}		0.26			µs
SDA, SCL Fall Time	t_F	[4], [5]			120	ns
SDA, SCL Rise Time	t_R				120	ns
SDA, SCL Input Suppression Filter Period		[6]		50		ns
Bus Timeout	$t_{TIMEOUT}$	[1]		25		ms

Notes:
1. Minimum SCL clock frequency is limited by the bus timeout feature, which resets the serial bus interface when either SDA or SCL is held low for $t_{TIMEOUT}$.
2. SDA Data Valid Acknowledge Time is SCL LOW to SDA (out) LOW acknowledge time.
3. SDA Data Valid Time is minimum SDA output data-valid time following SCL LOW transition.
4. A master device must internally provide an SDA hold time of at least 300ns to ensure an SCL low state.
5. The maximum SDA and SCL rise times is 300ns. The maximum SDA fall time is 250ns. This allows series protection resistors to be connected between SDA and SCL inputs and the SDA/SCL bus lines without exceeding the maximum allowable rise time.
6. Includes input filters on SDA and SCL that suppress noise less than 50ns.
7. Additional decoupling may be required when pulling current from VCC and/or VDD in noisy environments.
8. 2µs minimum on time, 0% duty cycle is supported. PWM between 0% and 1% not guaranteed.

Typical Operating Characteristics

Figure 5-1. START-UP behavior, PWM = 10% duty cycle.

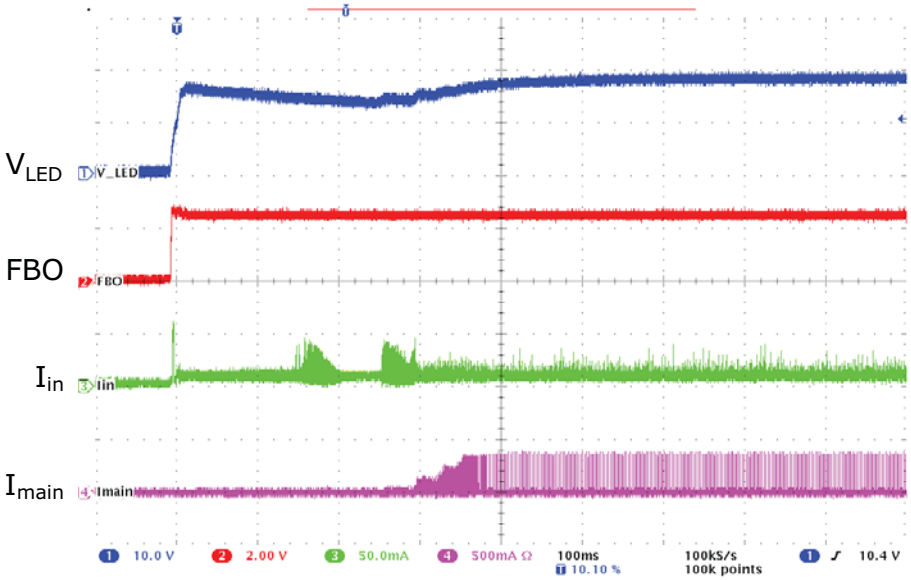


Figure 5-2. START-UP behavior, PWM = 90% duty cycle.

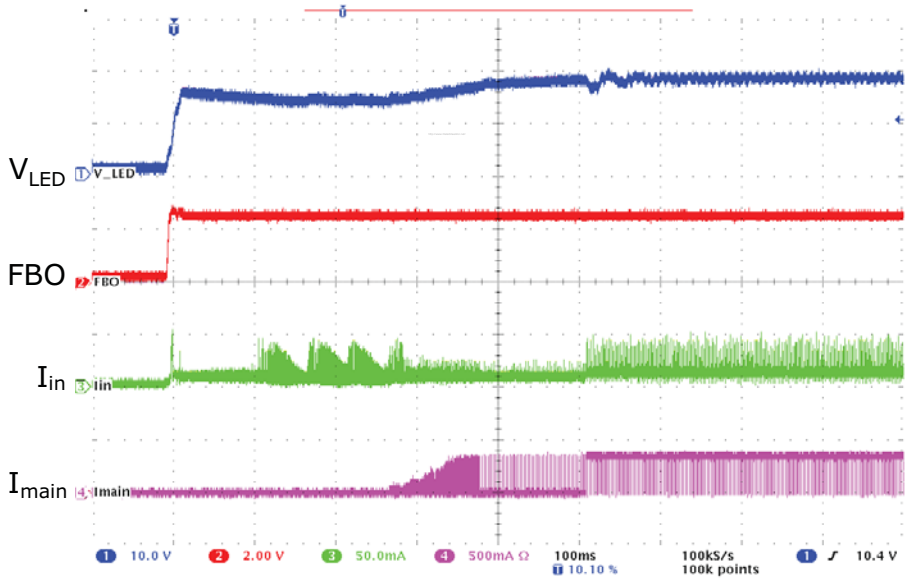


Figure 5-3. MSL2023 operation, PWM = 10% duty cycle.

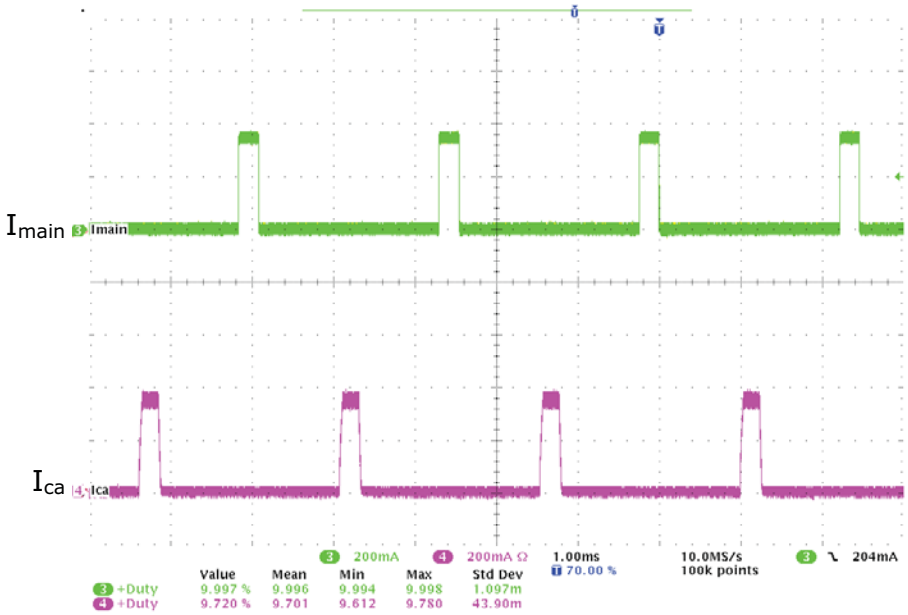


Figure 5-4. MSL2023 operation, PWM = 90% duty cycle.

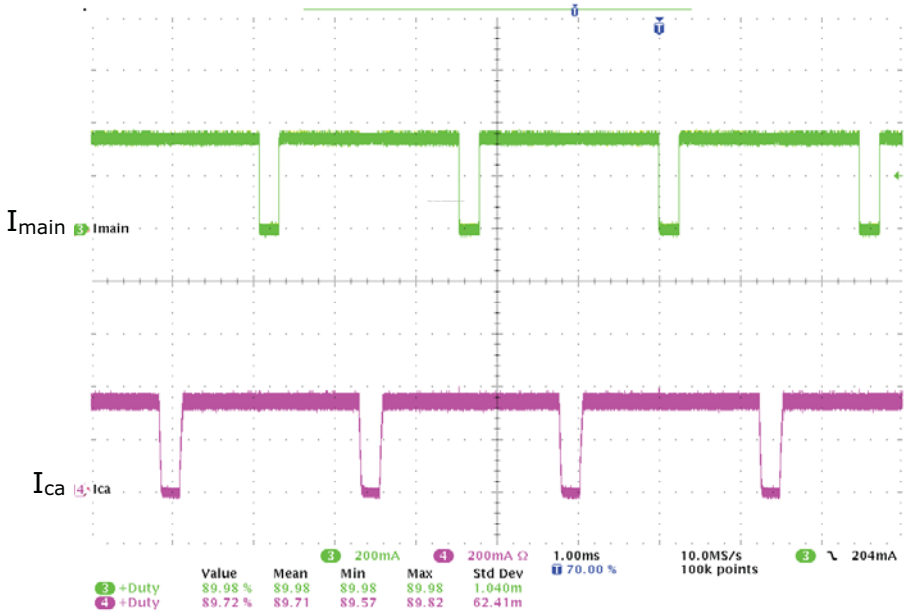


Figure 5-5. MSL2024 operation, PWM = 10% duty cycle.

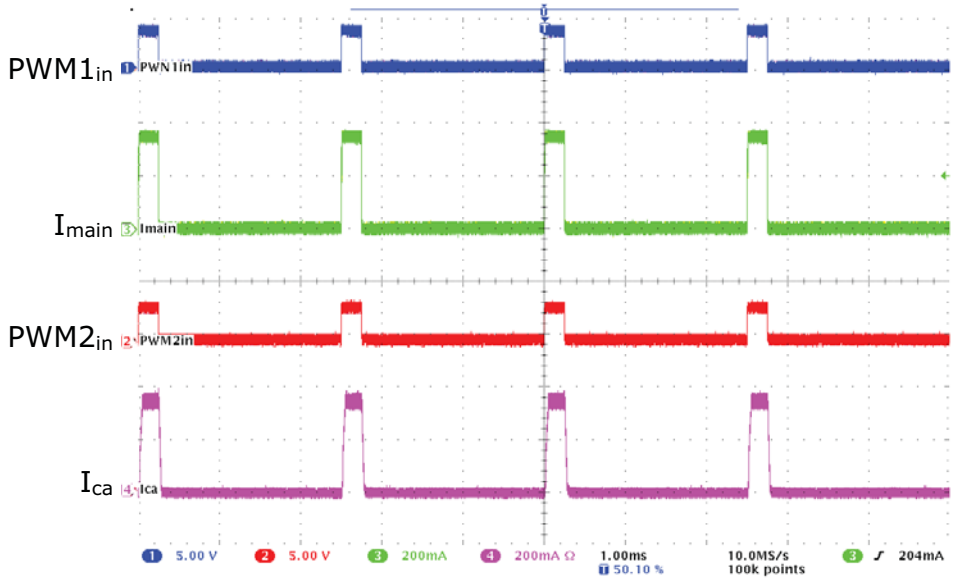


Figure 5-6. MSL2024 operation, PWM = 90% duty cycle.

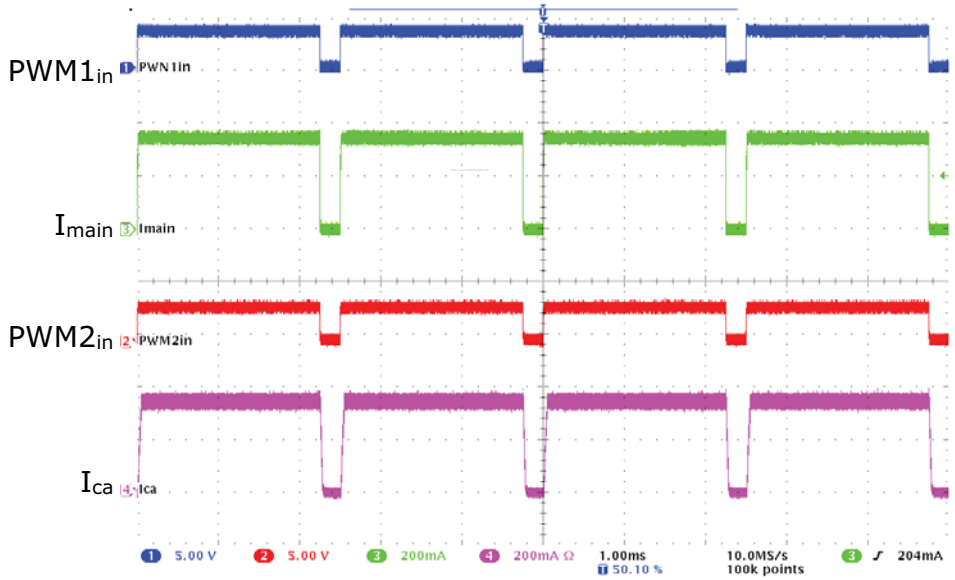


Figure 5-7. Fault response, string open circuit.

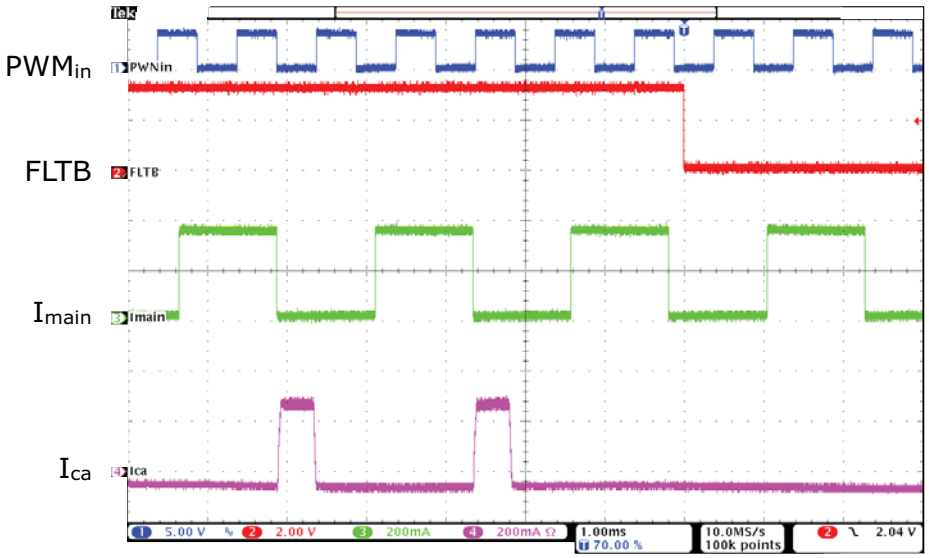


Figure 5-8. Fault response, LED short circuit.

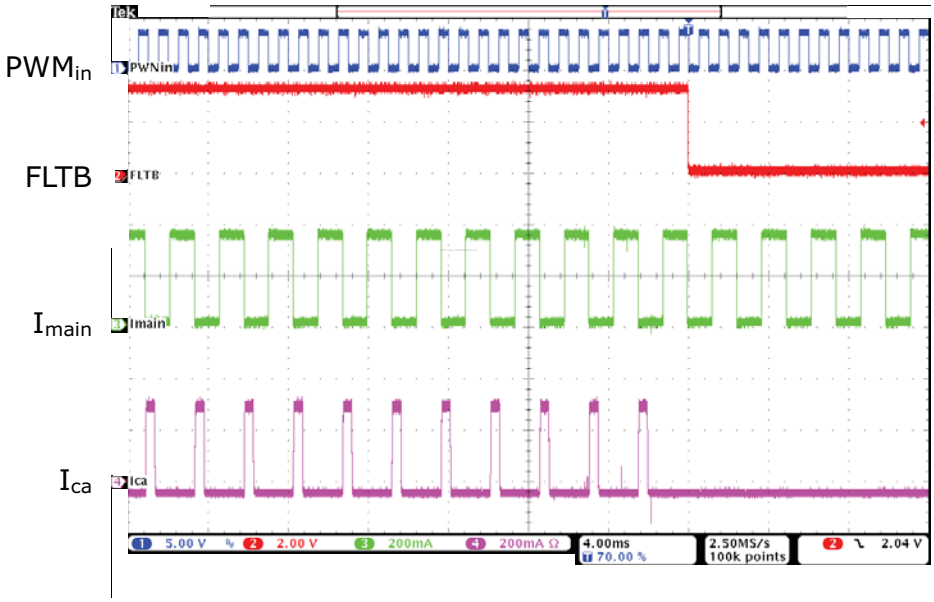


Figure 5-9. Input current vs. input voltage.

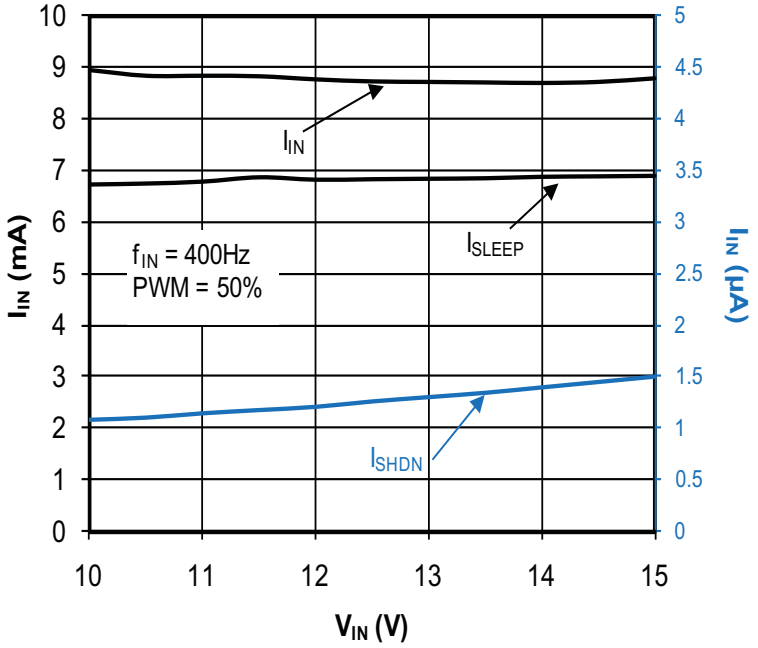


Figure 5-10. Average LED current vs. input PWM duty cycle.

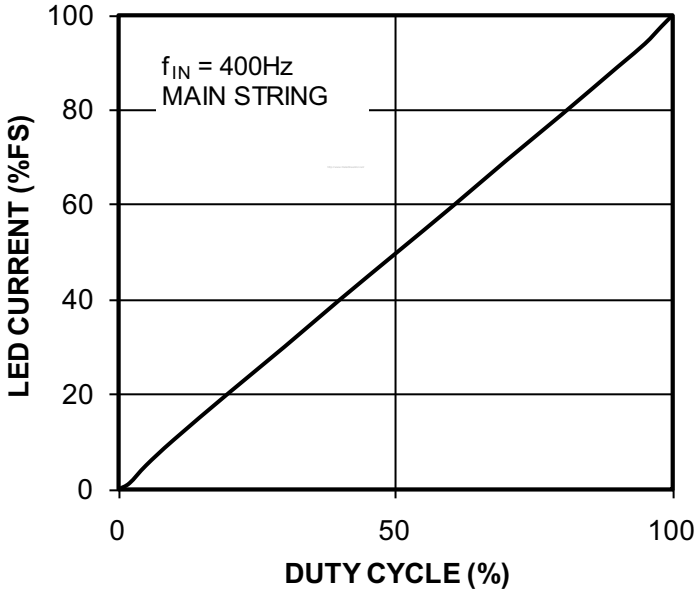
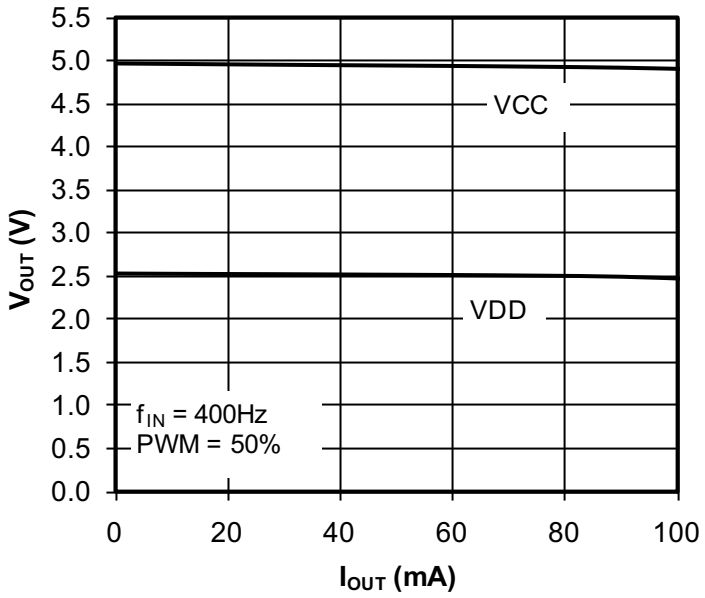


Figure 5-11. V_{CC} and V_{DD} regulation.



6. Block Diagram

Figure 6-1. MSL2023 block diagram.

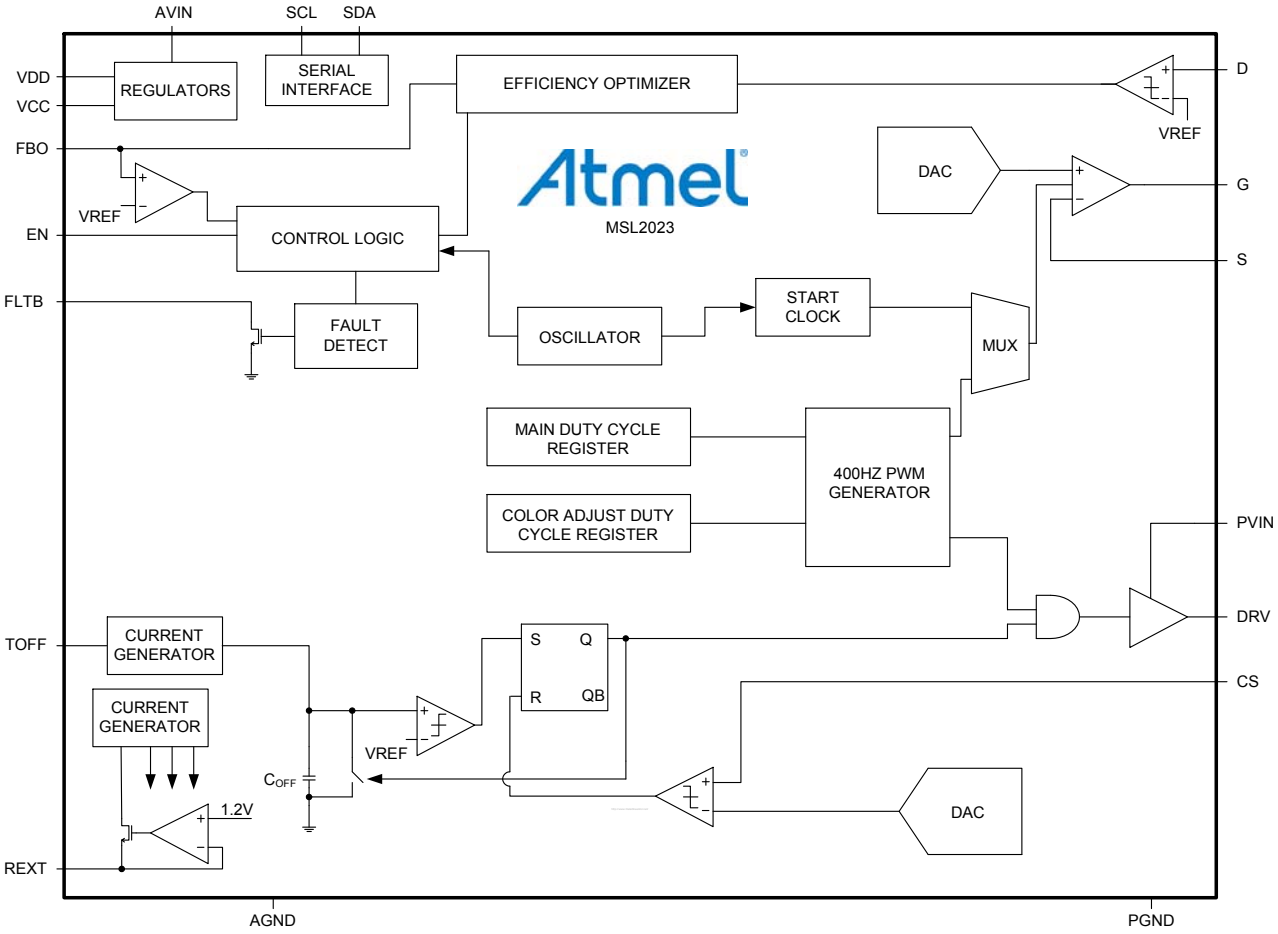
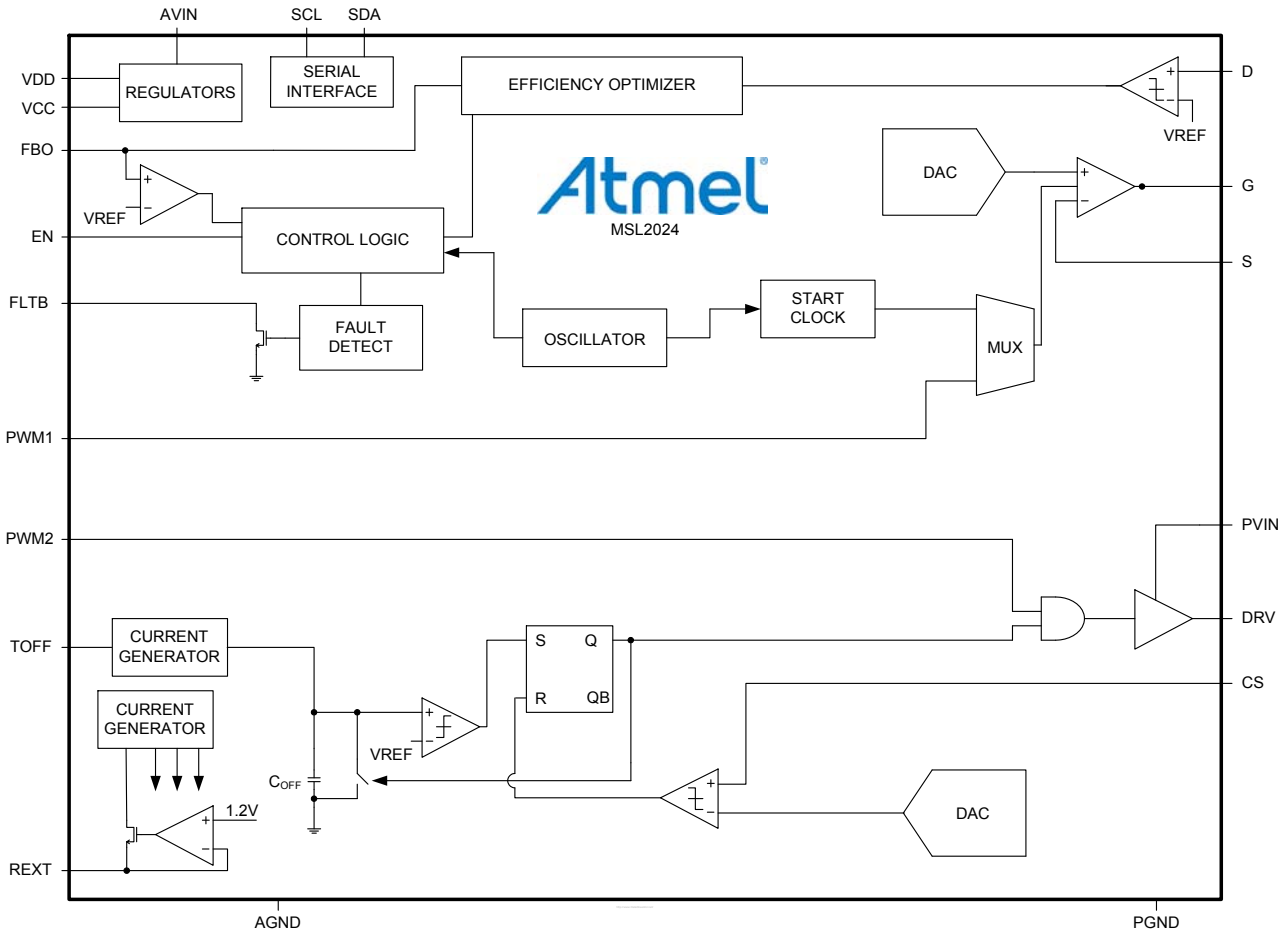
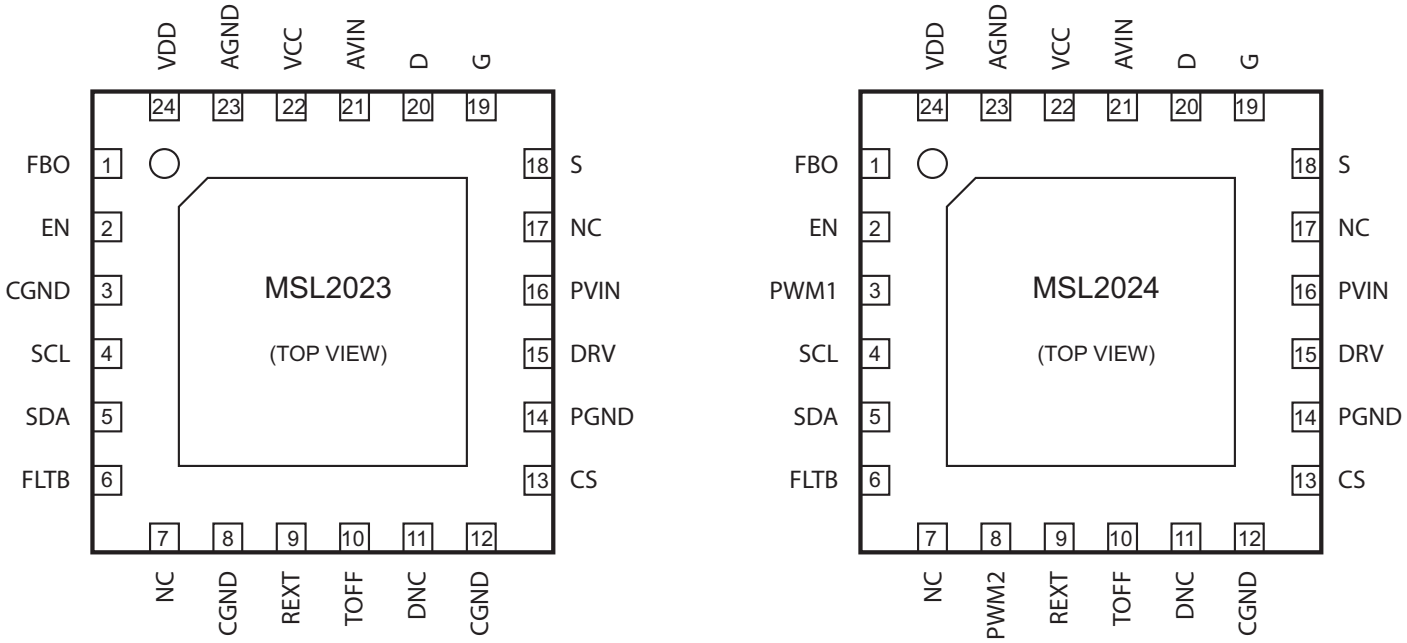


Figure 6-2. MSL2024 block diagram.



7. Pinout and Pin Description

7.1 Pinout – MSL2023 and MSL2024



7.2 Pin Descriptions

Name	Pin		Description
	MSL2023	MSL2024	
FBO	1	1	**Feedback Output** Feedback output from efficiency optimizer. Connect FBO to the LED power supply regulation feedback node to control V_{LED}. When unused connect FBO to VCC.
EN	2	2	**Enable Input (Active High)** Drive EN high to turn on the MSL2023/24, drive EN low to turn it off. For automatic start-up connect EN to AVIN. Taking EN high initiates a turn-on sequence. See "Turn-On Sequence" on page 19 for details.
CGND	3, 8, 12	12	**Connect to Ground**. Connect CGND to AGND
PWM1	–	3	**PWM1 Dimming Input** Drive PWM1 with a pulse-width modulated signal to control LED brightness of the main string. See "PWM and LED Brightness" on page 24 for details.
SCL	4	4	**Serial Clock Input** SCL is the I²C serial interface clock input. See "I²C Serial Interface " on page 30 for details.
SDA	5	5	**Serial Data Input/Output** SDA is the I²C serial interface data I/O. See "I²C Serial Interface " on page 30 details.
FLTB	6	6	**Fault Output (Open Drain, Active Low)** FLTB sinks current to AGND when a fault condition exists. Toggle EN low then high to clear FLTB, or clear faults through the serial interface (see "Fault Status register (FAULTSTAT, 0x23), Read Only" on page 28). Use the serial interface to access fault information and to enable/disable fault response.

Name	Pin		Description
	MSL2023	MSL2024	
NC	7, 17	7, 17	No internal connection
PWM2	–	8	**PWM2 Dimming Input** Drive PWM2 with a pulse-width modulated signal to control LED brightness of the color-adjust string. See “PWM and LED Brightness” on page 24 for details.
REXT	9	9	**External Resistor** Connect a 46.4kΩ, 1% resistor from REXT to AGND.
TOFF	10	10	**Off-Time Set Input** A resistor from TOFF to AGND controls the constant off time for the color-adjust string floating buck converter, where $R_{TOFF} = t_{OFF} * (90.9 \times 10^9)$, with t_{OFF} in seconds and R_{TOFF} in Ohms. For example, an off time of 0.5µs results in a resistor value of 45.3kΩ (to the nearest 1% value).
DNC	11	11	**Do Not Connect** Do not make external connection to DNC.
CS	13	13	**Current Sense Input for the Color-Adjust String** Connect CS to the external current sense resistor of the color-adjust string. The default current sense threshold is 200mV.
PGND	14	14	**Power Ground** PGND is the ground connection for the FET gate drivers. Connect PGND to AGND close to the MSL2023/2024.
DRV	15	15	**Gate Drive for Color-Adjust (Floating Buck Regulator) MOSFET** Connect DRV to the gate of the external power MOSFET.
PVIN	16	16	**Power Voltage Input (12V Nominal)** PVIN powers DRV, the floating buck FET gate driver. Bypass PVIN to PGND with a 1.0µF or greater capacitor.
S	18	18	**Source Sense Input for Main LED String MOSFET** Connect S to the source of the external MOSFET, and to the current sense resistor for the main LED string. The current sense threshold is 200mV.
G	19	19	**Gate Output for Main String MOSFET** Connect G to the gate of the Main string external MOSFET.
D	20	20	**Drain Output for Main String MOSFET** Connect D to the drain of the main string external MOSFET.
AVIN	21	21	**Analog Voltage Input (12V Nominal)** AVIN is the power input to the MSL2023/2024. Bypass AVIN to AGND with a 1.0µF or greater capacitor placed close to AVIN.
VCC	22	22	**5V Internal Voltage** Connect 10uF bypass capacitor from VCC to AGND.

Name	Pin		Description
	MSL2023	MSL2024	
AGND	23	23	**Analog Ground** Connect AGND to system ground.
VDD	24	24	**2.5V Internal Voltage** Connect 10µF bypass capacitor from VDD to AGND.
EP	EP	EP	**Exposed Pad** Connect EP to a large copper plane connected to PGND and AGND.

8. Typical Application Circuit

MSL2023/24 controlling the output of an isolated PFC controller; a linear current sink regulates the white LED current and a floating buck converter regulates the color LED string current.

Figure 8-1. MSL2023 typical application circuit.

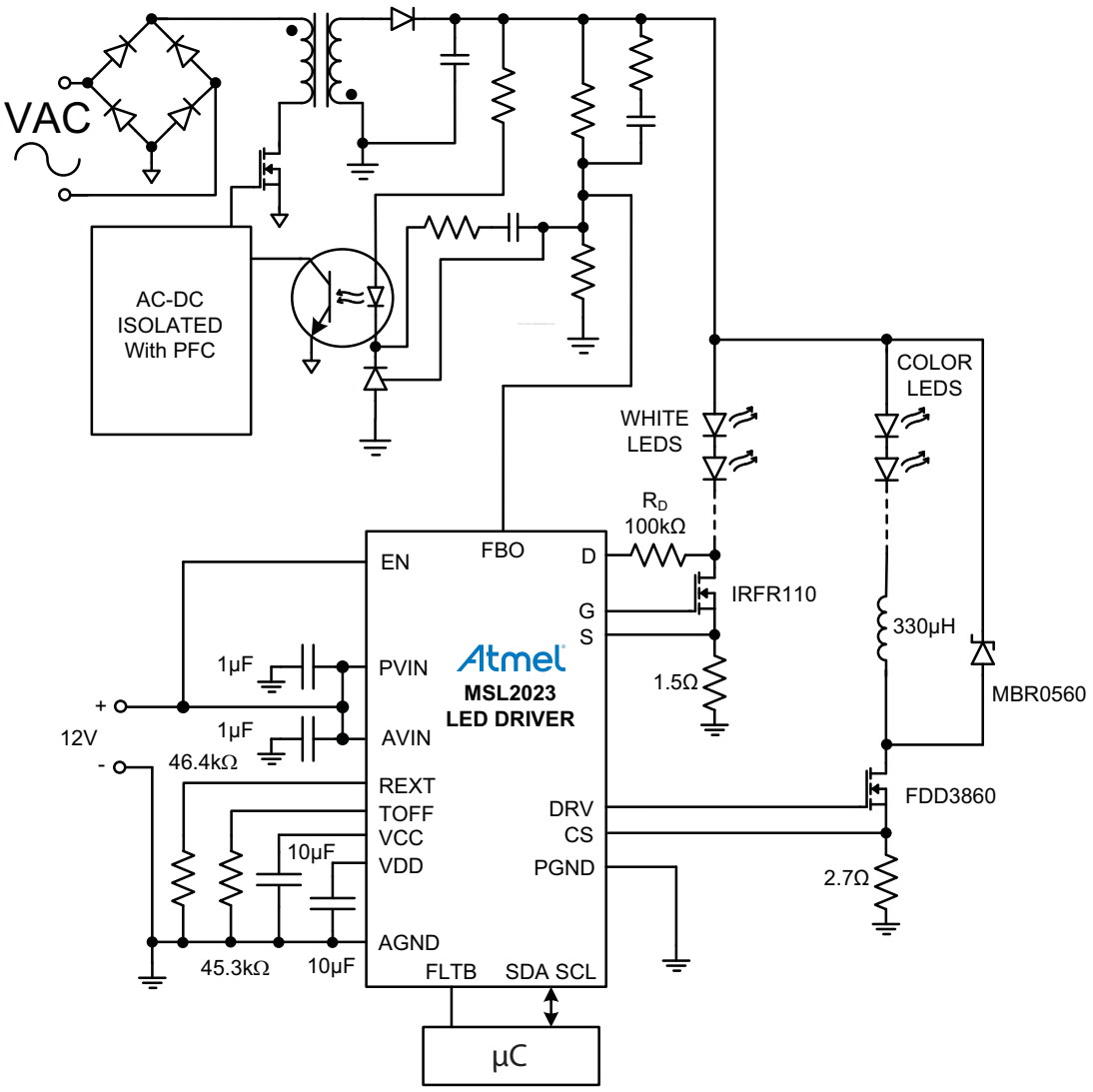
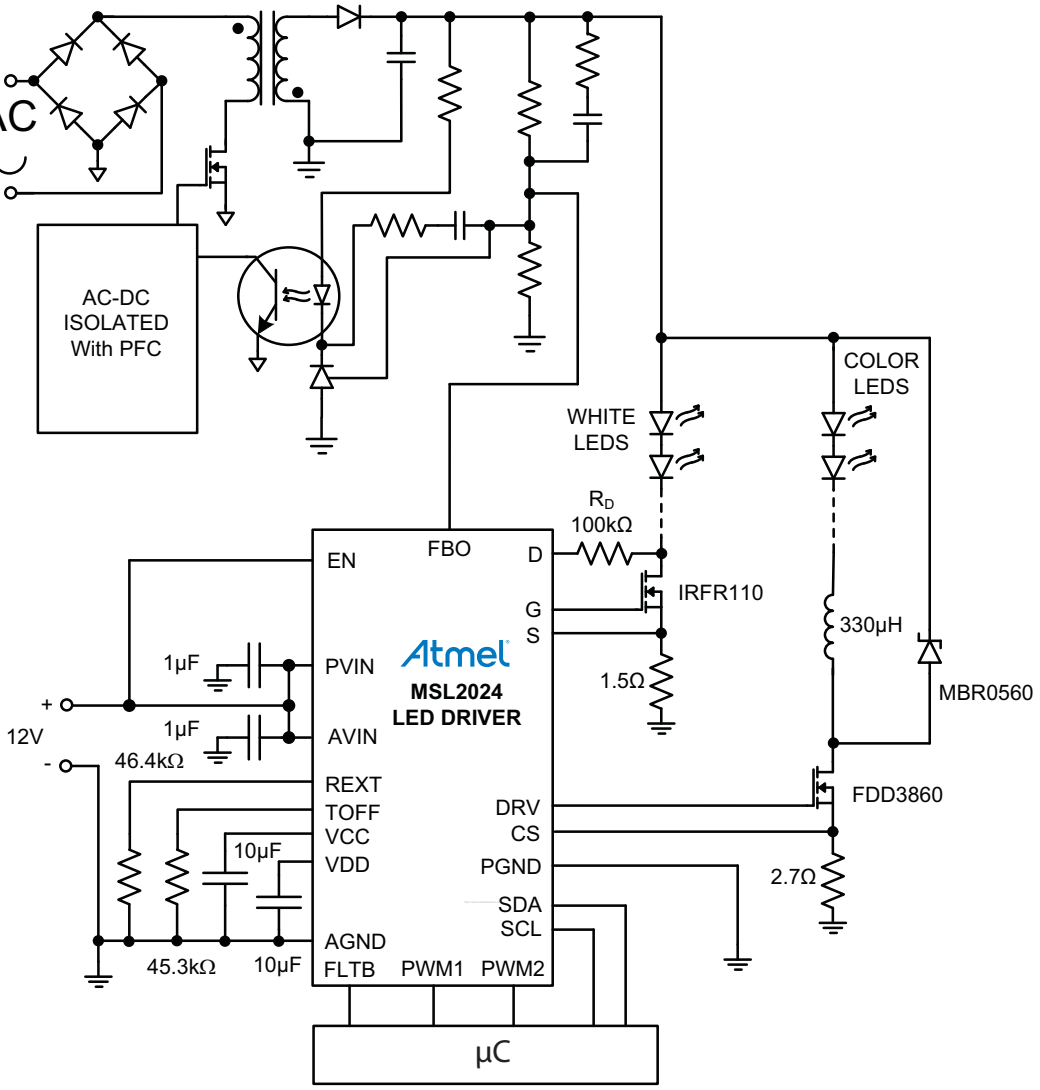


Figure 8-2. MSL2024 typical application circuit.



9. Detailed Description

Table 9-1. Device selection guide, LED brightness control by part number.

Part	LED brightness control		PWM dimming frequency
	Main string	Color adjust string	
MSL2023	Main PWM register(1)	Color adjust PWM register(1)	400Hz
MSL2024	Duty cycle at the PWM1 input	Duty cycle at the PWM2 input	Input frequency main: 60Hz to 22kHz (minimum t_{ON} = 2µs) CA: 100Hz to 500Hz

Note: 1. Access registers through I^2C serial interface.

The MSL2023/24 drive two LED strings, the main string and the color-adjust string. The main string LEDs are typically white and used to provide an accurate light intensity control. The color-adjust string LEDs are used to control the color temperature. The combined light output is a blend, with intent to offer a warmer high CRI light for example, than what white LEDs can alone produce. The main string is directly controlled by a Pulse Width Modulated (PWM) constant current controller (current sink to ground). An Efficiency Optimizer (EO) output controls the main string voltage, via feed-back to the LED string power supply, to minimize the voltage across the LED current controller, minimizing power loss.

The color-adjust string is regulated by a floating buck controller. The buck controller converts the voltage of the main string's supply to a voltage appropriate for the color-adjust LEDs. Additionally, the MSL2023/24 have programmable 8-bit registers that allows adjustment of the current by changing the source feedback reference voltages (see"Block Diagram" on page 12).

10. Fault Conditions

The MSL2023/24 detect fault conditions, and take corrective action when faults are verified.

String open circuit and LED short circuit conditions of the Color-Adjust string are monitored. When one of these faults occurs, FLTB pulls low to indicate a fault condition and the Color-Adjust LEDs turn off. Read Fault Status register 0x23 to determine the fault type and to clear the faults, or clear faults by toggling EN low then high. Faults that persist re-establish the fault response. Mask string faults using Fault Disable register 0x22. Clear string faults by toggling EN low then high, or with "Fault Disable register (FAULT, 0x22)" on page 27. For the main LED string when an LED open occurs the V_{LED} voltage will reach the maximum allowed.

Over Temperature Protection puts the device to sleep when the die temperature is above 147°C. The device turns back on when the die temperature falls below 127°C, and normal operation resumes. While asleep, the I^2C interface remains active (see "Fault Disable register (FAULT, 0x22)" and "Fault Status register (FAULTSTAT, 0x23), Read Only" on page 28 for more information about thermal shutdown).

Table 10-1. Fault conditions, response and recovery.

Fault	Response	Recovery action
Die Temperature > 147°C	Asleep (I^2C still active)	When die temperature falls below 127°C operation resumes
Color-Adjust String has Shorted LEDs	Color-Adjust string turns off, FLTB pulls low, and bit 0 of the Fault Status register 0x23 sets high	Correct the short condition in LED string. Toggle EN low to high to resume operation, or clear faults using register 0x22 (page 27)
Color-Adjust String is Open Circuit	Color-Adjust string turns off, FLTB pulls low, and bit 1of the Fault Status register 0x23 sets high	Correct the open condition in LED string. Toggle EN low to high resume operation, or clear faults using register 0x22 (page 27)

11. Applications Information

11.1 Turn-On Sequence

When power is applied the EEPROM contents copy into the control registers, setting up the device for operation; any previously programmed control register settings are lost unless they are programmed into the EEPROM (page 25). The MSL2023/24 wait for 250ms to allow the AC/DC or DC/DC input stage to establish the default voltage. The MSL2023/24 then starts to optimize the LED string voltage (V_{LED}), and then begin to drive the LED strings. It is critical that the AC/DC or DC/DC converter that powers the LED strings reaches its nominal output voltage in less than 250ms after power is applied. When the 250ms start-up delay is complete the Efficiency Optimizer adjusts the LED voltage to the proper level to drive the main string. After the voltage is set, normal PWM operation begins for both the Main and Color-Adjust strings.

11.2 Setting the Main String Current with R_S

The main string LED current regulates by monitoring the voltage at the S pin, the main string MOSFET source resistor connection. The default feedback voltage at the S pin is 200mV. Choose the string current sense resistor R_S using:

$$R_S = \frac{0.2}{I_{LED}}\Omega$$

where I_{LED} is the main string regulation current. The main string reference voltage (MREF) register 0x20 sets the feedback voltage to 200mV, at 2mV per LSB. The regulation voltage, $V_{S(FB)}$, is:

$$V_{S(FB)} = (0.002 \cdot MREF)V$$

where MREF is the decimal equivalent of the value in register 0x20. The default value for MREF is 0x64, for a feedback voltage of 0.2V. Change the feedback voltage by changing the value in register 0x20 using the serial interface. LED average current is within ±3% of targeted value when a 1% resistor is used for R_S.

11.3 Setting AC/DC Output Voltage

The efficiency optimizer output, FBO, connects to the AC/DC or DC/DC converter's output voltage feedback node, and pulls current from the node to force the converter's output voltage up. The MSL2023/24 works with any input power converter topology that uses a resistor divider to set its output voltage. Additionally, the two strings will operate off of independent rails. Operation with and AC/DC PFC converter is described below.

Select the two resistors that set the nominal LED power supply's output voltage by first determining the minimum output voltage using:

$$V_{OUT(MIN)} \leq (V_{fMIN}) \cdot (N) + 0.2V$$

where V_{fMIN} is the minimum LED forward voltage for the main string LEDs at the expected LED current, N is the number of LEDs in the string, and 0.2V is the minimum overhead required for the current sense resistor and the FET. Then determine the maximum output voltage using:

$$V_{OUT(MAX)} = (V_{fMAX}) \cdot (N) + 1.2V$$

where V_{fMAX} is the maximum LED forward voltage for the main string LEDs at the operating LED current, N is the number of LEDs in the string, and 1.2V is the maximum overhead required for the current sense resistor and the FET. Determine the value for the upper voltage setting resistor using:

$$R_{TOP} \geq \frac{V_{OUT(MAX)} - V_{OUT(MIN))}}{170 \cdot 10^{-6}} \Omega$$

where 170µA is the minimum FBO full scale current. Determine the lower resistor using:

$$R_{BOTTOM} = R_{TOP} \cdot \frac{V_{FB}}{V_{OUT(MIN)} - V_{FB}} \Omega$$

where V_{FB} is the feedback regulation voltage of the switch mode converter.

11.4 Selecting the Main String MOSFET

The Main string MOSFET sinks the string current to ground through current sense resistor R_S. Output G drives the gate of the MOSFET at up to VIN - 2.0V. Select a MOSFET with a low RDS(ON) and a maximum drain-source voltage of at least 20% greater than:

$$V_{fb}\left(\frac{R_{TOP}}{R_{BOTTOM}} + 1\right) + 340\mu A \cdot R_{TOP}$$

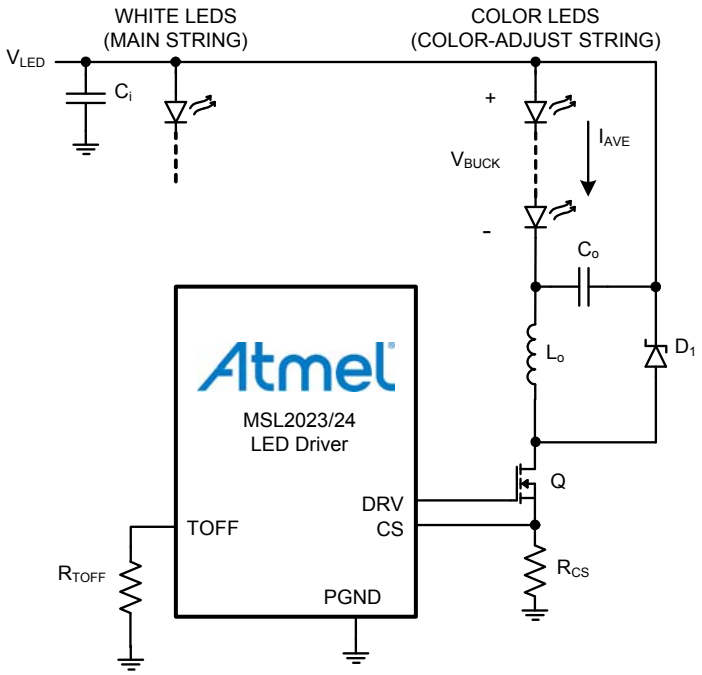
where 340µA is the maximum FBO full scale current.

11.5 Selecting the Drain Resistor – R_D

The drain resistor, R_D in the “Typical Application Circuit ” on page 16, connects the MSL2023/24 to the Drain of the Main string external MOSFET. Use a 100kΩ for R_D.

11.6 Selecting the Color-Adjust String Floating Buck Components

Figure 11-1. Floating buck LED driver.



The MSL2023/24 includes a driver for a constant off-time floating buck topology, shown in Figure 11-1, to convert the main string voltage to a value appropriate for the color-adjust LED string. The buck is operated in continuous conduction mode.

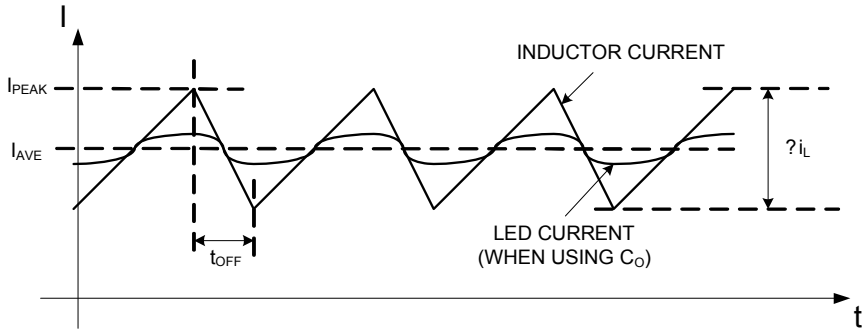
Continuous conduction operation is assured when the peak-to-peak ripple current in the inductor, Δi_L, is less than twice the average LED current. A peak-to-peak ripple current magnitude of 15% of the average LED on-current is suggested, i.e.

$$\Delta i_L = 0.15 I_{AVE} \text{ A}$$

where I_{AVE} is the average color-adjust LED string on-current. Choose I_{AVE} appropriate for the color-adjust LEDs (Figure 11-1 on page 21 and Figure 11-2 on page 22) and calculate the peak string on-current using

$$I_{PEAK} = I_{AVE} + \frac{\Delta i_L}{2} \text{ A}$$

Figure 11-2. Color-adjust string LED on-current details.



The color-adjust string LED on-current regulates by monitoring the voltage at CS, the color-adjust string FET source resistor connection. The reference voltage V_{CSFB} for CS is 200mV (V_{CSFB} is 200mV by default, and is adjustable through the serial interface; see the register definitions for details about changing V_{CSFB}). Choose the current sense resistor R_{CS} using

$$R_{CS} = \frac{V_{CSFB}}{I_{PEAK}}\Omega$$

Determine V_{BUCK}, the voltage across the color-adjust LEDs, using

$$V_{BUCK} = NV_f\text{V}$$

where N is the number of LEDs in the string and V_F is the forward voltage drop of the LEDs at I_{PEAK}.

The duty ratio of MOSFET *Q* is

$$D = \frac{V_{BUCK}}{V_{LED}}$$

where V_{LED} is the main string voltage, Figure 11-1 on page 21. The constant off-time of the MOSFET is t_{off} and calculated in seconds using

$$t_{off} = \frac{1-D}{f_s}\text{s}$$

where f_S is the selected switching frequency in Hz. Use 100kHz to 1MHz for f_S. Set t_{off} with resistor R_{TOFF} from TOFF to GND (Figure 11-1 on page 21), whose value is

$$R_{t_{off}} = t_{off}(90.9 \cdot 10^9)\Omega$$

Choose the inductor value using

$$L_O = \frac{V_{BUCK} \cdot t_{off}}{\Delta i_L}\text{H}$$

Use a ferrite inductor with a saturation current at least 50% higher than the peak current flowing in it:

$$I_{L_{SAT}} > 1.5 \cdot I_{PEAK}\text{A}$$

Note here a particular advantage of constant off-time operation of the buck converter is that ripple current is independent of the input voltage. The circuit provides a constant average LED current, I_{AVE}, but the buck converter actually regulates the peak inductor current, I_{PEAK} (Figure 11-1 on page 21 and Figure 11-2 on page 22). From the equation for the inductor value L_0 above, we see that because t_{off} is constant, and V_{BUCK} is relatively constant, the ripple current Δi_L is also constant, so that I_{AVE} is a constant, as desired. If the main string voltage changes, the switching frequency changes to keep the on-time constant, thus the ripple current is independent of the input voltage.

This topology does not require an output capacitor, C_o in Figure 11-1 on page 21. When used, C_o steers the inductor's ripple current away from the LEDs but reduces the accuracy of PWM dimming because the voltage across it cannot change quickly. When using C_o, a ceramic capacitor of between 1.0µF and 10µF is adequate, with a voltage rating higher than V_{BUCK}.

The output capacitor of the AC/DC converter that produces the main string voltage, C_i in Figure 11-1 on page 21, doubles as the buck's input capacitor. The capacitor's function is to provide a smooth voltage to the buck converter. It should be able to handle the R.M.S. ripple current of the buck converter, which is approximately equal to

$$I_{C_i} = I_{AVE}\sqrt{D(1-D)} \text{ A}$$

This ripple current peaks at a duty ratio of D = 0.5.

Select an N-channel MOSFET for Q with a maximum drain-source voltage at least 25% above V_{LED}. The R.M.S. current in the MOSFET is approximately equal to

$$I_Q = I_{AVE}\sqrt{D} \text{ A}$$

The MOSFET conduction power loss due to this current is

$$P_{CON} = I_Q^2 R_{DS} = I_{AVE}^2 R_{DS} D \text{ W}$$

where R_{DS} is the hot on-resistance of the MOSFET, which can be found in the MOSFET datasheet, and is typically 1.5 to 1.8 times greater than the cold resistance. The MOSFET will also incur switching losses, which can be difficult to calculate exactly. A good rule-of-thumb is to choose a MOSFET in a package that dissipates at least four times P_{CON}.

The average current in the output rectifier D_1 is

$$I_{D_i} = I_{AVE}(1-D) \text{ A}$$

and the power dissipated in the rectifier due to conduction is

$$P_{CON_{D_1}} = I_{D_1} V_{on} \text{ W}$$

where V_{on} is the voltage drop across the rectifier at the forward current of I_{D1}. Pick a rectifier with an average current rating at least 50% higher than I_{D1}. Use a Schottky rectifier if the LED voltage is less than 50V. The Schottky rectifier's voltage rating should be at least 25% higher than V_{LED}. Schottky rectifiers have very low on-state voltage and very fast switching speed, but at high voltage and high temperatures their leakage current becomes significant. The power dissipated in the Schottky rectifier due to the leakage current at any temperature and duty ratio is

$$P_{lkg} = V_{LED} I_r D \text{ W}$$

where I_r is the reverse leakage current, found in the diode's datasheet. This power must be added to the conduction power loss.

$$P_{D_1} = P_{CON_D} + P_{lkg} \text{ W}$$

Make sure that the rectifier's total power dissipation is within the rectifier's specifications.

11.7 PWM and LED Brightness

Figure 6-1 on page 12 is a block diagram that shows how the MSL2023 controls the brightness of the LEDs. The duty cycle of each string equals the value programmed into the 12-bit PWM control registers MainDuty[11:0] and ColorAdjustDuty[11:0], (registers 0x34 through 0x37). The frequency of the PWM dimming is 400Hz. The dimming signals for the two strings are 180º out of phase.

Figure 6-2 on page 13 is a block diagram that shows how the MSL2024 controls the brightness of the LEDs. The duty cycle of each string equals the duty cycle of the inputs at PWM1 (main string) and PWM2 (color-adjust string). The frequency of each string's PWM dimming signal equals the frequencies of the respective input signals. The frequency range of the PWM1 input is 120Hz to 22kHz, while the minimum on-time for the main string driver output G is 2µs. The frequency range of the PWM2 input is 200Hz to 500Hz.

12. Control Registers

Table 12-1. Register map[1].

Address and Register name		Function	Default value[2]	Bit functions							
				D7	D6	D5	D4	D3	D2	D1	D0
Control and monitor registers											
0x00 to 0x1F		RAM	0xXX	Free RAM							
0x20	MREF	Main String Feedback Reference Voltage	0x64	M_{REF} = 2mV per LSB							
0x21	CAREF	Color-Adjust String Reference Feedback Voltage	0x64	CA_{REF} = 2mV per LSB							
0x22	FAULT DISABLE	Color-Adjust Fault Disable	0x00	–	–	–	–	–	TSDMASK	OCDIS	SCDIS
0x23	FAULTSTAT	Fault Status	Read Only	–	–	–	–	–	TSD	OCFLT	SCFLT
0x24	SLEEP	Configuration	0x00	–	–	–	–	–	–	–	SLEEP
0x34	MDUTYHIGH	Main String Duty Cycle High Byte	0xFF	MainDuty[11:4] MSL2023 ONLY							
0x35	MDUTYLOW	Main String Duty Cycle Low Bits	0x0F	–	–	–	–	MainDuty[3:0] MSL2023 ONLY			
0x36	CADUTYHIGH	Color Adjust String Duty Cycle High Byte	0xFF	ColorAdjustDuty[11:4] MSL2023 ONLY							
0x37	CADUTYLOW	Color Adjust String Duty Cycle Low Bits	0x0F	–	–	–	–	ColorAdjustDuty[3:0] MSL2023 ONLY			
0x40	EOCTRL	Efficiency Optimizer	0xE5	–	–	–	–	DThresh[3:0]			
0x60	E2ADDR	EEPROM Address	0x00	–	EEPROM Address Pointer						
0x61	E2CTRL	EEPROM Control	0x00	–	–	–	–	–	RWCTRL[2:0]		

Notes: 1. Do not change the contents of undefined bits or unlisted registers.

2. Unless changed through the EEPROM, these default values load at power-up, and when EN is taken from low to high.

12.1 EEPROM and Power-Up Defaults

An on-chip EEPROM holds all the default register values (Table 12-1 on page 24). At power-up the data in the EEPROM automatically copy directly to control registers 0x00 thru 0x51, setting up the device for operation.

Any changes made to registers 0x00 thru 0x51 after power-up are not reflected in the EEPROM and are lost when power is removed from the device, or when the enable input EN is forced low. If a different power-up condition is desired program the values into the EEPROM via the serial interface as explained in the next section, or contact the factory to inquire about ordering a customized power-up setting.

12.2 EEPROM Address and Control/Status Registers

The EEPROM can be visualized as an image of the control registers from 0x00 thru 0x51. Change an EEPROM register value by writing the new value into the associated control register, and then instructing the device to program that value into the EEPROM. Two control registers facilitate this process, the EEPROM address register E2ADDR (0x60), and the EEPROM control register E2CTRL (0x61). Into E2ADDR write the location of the data that is to be programmed into the EEPROM, and write 0x03 to E2CTRL to command the device to program that data into the EEPROM. Programming the EEPROM takes a finite amount of time; after sending a command to E2CTRL wait 5ms, then end the write cycle by writing 0x00 to E2CTRL.

Example: Change the string current feedback voltage MREF to 100mV.

Commands: To register 0x20 (MREF) write 0x32 (the new value for MREF). To register 0x60 (E2ADDR) write 0x20 (the address of the MREF register). To register 0x61 (E2CTRL) write 0x03 (the command to copy the value to EEPROM). Wait 5ms. To register 0x61 (E2CTRL) write 0x00, to turn off EEPROM access.

Result: The value 0x32, located in the MREF register, is programmed into the EEPROM and becomes the new power-up default value for MREF.

Summary:

- 0x20 32
- 0x60 20
- 0x61 03
- Wait 5ms
- 0x61 00

E2CTRL provides additional functions beyond simply programming a register's value into the EEPROM. Data may be transferred in either direction, from the registers to the EEPROM, or from the EEPROM to the registers. Register data may be transferred into or out of the EEPROM in groups of eight, a page at a time. The page address boundaries are predefined, and E2ADDR must be loaded with the address of the first byte of the page that is to be copied. Page addresses begin at 0x00 and increment by eight, with the second page beginning at 0x08, the third at 0x10, etc. To program a full page of data into the EEPROM, write the address of the page's first byte to E2ADDR, and write 0x04 to E2CTRL. Wait 5ms, and then end the write cycle by writing 0x00 to E2CTRL. When finished accessing the EEPROM always write 0x00 to E2CTRL to block inadvertent EEPROM read/writes. Table 12-3 on page 26 details the functions available through E2CTRL.

Table 12-2. EEPROM Address register (E2ADDR, 0x60), defaults highlighted.

Register	Address	Register data							
		D7	D6	D5	D4	D3	D2	D1	D0
E2ADDR	0x60	–	E2ADDR[6:0]						
DEFAULTS		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
EEPROM Minimum Address 0x00		–	0	0	0	0	0	0	0
EEPROM Maximum Address 0x51		–	1	0	1	0	0	0	1

Table 12-3. EEPROM Control register (E2CTRL, 0x61), defaults highlighted.

Register	Address	Register data							
		D7	D6	D5	D4	D3	D2	D1	D0
E2CTRL	0x61	–	–	–	–	–	RWCTRL[2:0]		
DEFAULTS		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
EEPROM Read / Write Disabled		x	x	x	x	x	**0**	**0**	**0**
Read 1 Byte from EEPROM		x	x	x	x	x	0	0	1
Read 8 Bytes from EEPROM		x	x	x	x	x	0	1	0
Write 1 Byte to EEPROM		x	x	x	x	x	0	1	1
Write 8 Bytes to EEPROM		x	x	x	x	x	1	0	0
Unused		x	x	x	x	x	1	0	1
		x	x	x	x	x	1	1	x

13. Detailed Register Descriptions

The MSL2023/24 registers are summarized in “Control Registers” on page 24. Detailed register information follows.

13.1 RAM (0x00 through 0x1F)

32 Bytes of RAM accessible through the I^2C serial interface. Copy data from RAM into EEPROM (see “EEPROM and Power-Up Defaults” on page 25) to have the data automatically load into the RAM at power up, and when EN is taken high.

Table 13-1. RAM (0x00 through 0x1F), defaults undetermined.

Register name	Address	Register data							
		D7	D6	D5	D4	D3	D2	D1	D0
RAM	0x00 – 0x1F	RAM							
DEFAULTS		**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**

13.2 Main String Reference Voltage register (MREF, 0x20)

Holds the DAC value that controls the reference voltage for the main string FET source feedback voltage. The reference voltage equals decimal value of this register times 2mV. The default value for MSREF is 0x64, which equates to M_{REF} = 200mV.

Table 13-2. Main String Reference register (MREF, 0x20), defaults highlighted.

Register name	Address	Register data							
		D7	D6	D5	D4	D3	D2	D1	D0
MREF	0x20	MREF[7:0]							
DEFAULT = 0x64: M_{REF} = 100 * 2mV = 200mV		**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**
M_{REF} = 0 ∗ 2mV = 0V		0	0	0	0	0	0	0	0
M_{REF} = 255 * 2mV = 510mV		1	1	1	1	1	1	1	1

13.3 Color-Adjust String Reference Voltage register (CAREF, 0x21)

Holds the DAC value that controls the reference voltage for the color-adjust string FET source feedback voltage. The reference voltage equals decimal value of this register times 2mV. The default value for CAREF is 0x64, which equates to V_{CAREF} = 200mV.

Table 13-3. Color-Adjust String Reference register (CAREF, 0x21), defaults highlighted.

Register name	Address	Register data							
		D7	D6	D5	D4	D3	D2	D1	D0
CAREF	0x21	CAREF[7:0]							
DEFAULT = 0x64: V_{CAREF} = 100 * 2mV = 200mV		**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**
V_{CAREF} = 0 ∗ 2mV = 0mV		0	0	0	0	0	0	0	0
V_{CAREF} = 255 ∗ 2mV = 510mV		1	1	1	1	1	1	1	1

13.4 Fault Disable register (FAULT, 0x22)

Bits D0 and D1 control the fault response for the color-adjust string. For fault response behavior see “Fault Conditions” on page 18. Bit D2 prevents the thermal shutdown fault from pulling FLTB low. Write 0x03 to this register to clear faults; write 0x00 to re-enable fault response.

Table 13-4. Fault Disable register (FAULT, 0x22), defaults highlighted.

Register name	Address	Register data							
		D7	D6	D5	D4	D3	D2	D1	D0
FAULT	0x22	–	–	–	–	–	TSDMASK	OCDIS	SCDIS
DEFAULT = 0x00		0	0	0	0	0	0	0	0
Act on faults		x	x	x	x	x	0	0	0
Disable LED Short Circuit Fault		x	x	x	x	x	0	0	1
Disable String Open Circuit Fault		x	x	x	x	x	0	1	x
Do Not Allow Thermal Shutdown Fault to Pull FLTB Low		x	x	x	x	x	1	x	x

13.5 Fault Status register (FAULTSTAT, 0x23), Read Only

Reports the fault status for the color-adjust string. When a fault is reported in this register, the fault output FLTB pulls low. Toggle EN low, then high to clear the faults. Faults recur if the fault persists.

Table 13-5. Fault Status register (FAULTSTAT, 0x23).

Register name	Address	Register data							
		D7	D6	D5	D4	D3	D2	D1	D0
FAULTSTAT	0x23	–	–	–	–	–	TSD	OCFLT	SSFLT
No Faults Detected		x	x	x	x	x	0	0	0
LED Short Circuit Fault Detected		x	x	x	x	x	0	0	1
String Open Circuit Fault Detected		x	x	x	x	x	0	1	0
The MSL2023/24 is in Thermal Shutdown		x	x	x	x	x	1	x	x

13.6 Sleep register (SLEEP, 0x24)

Puts the device to sleep (the serial interface remains awake). When asleep the gate drive outputs stop switching, and the LEDs turn off.

Table 13-6. Sleep register (SLEEP, 0x24), defaults highlighted.

Register name	Address	Register data							
		D7	D6	D5	D4	D3	D2	D1	D0
SLEEP	0x24	–	–	–	–	–	–	–	SLEEP
DEFAULT = 0x00		0	0	0	0	0	0	0	0
Device is Awake		x	x	x	x	x	x	x	0
Device is Asleep		x	x	x	x	x	x	x	1

13.7 Main String Duty Cycle register, High Byte (MDUTYHIGH, 0x34)

Contains the upper 8-bits of the 12-bit MSL2023 main string duty cycle setting. The remaining 4-bits are in register 0x35. The registers combine to form the main string duty cycle, a linear relation where 0x000 = 0% to 0xFFF = 100%. When changed, the duty cycle updates at the beginning of the next output PWM period.

Table 13-7. Main String Duty Cycle High register (MDUTYHIGH, 0x34), defaults highlighted.

Register name	Address	Register name							
		D7	D6	D5	D4	D3	D2	D1	D0
MDUTYHIGH	0x34	MDUTYHIGH[11:4]							
DEGAULT = 0xFF		1	1	1	1	1	1	1	1

13.8 Main String Duty Cycle register, Low Byte (MDUTYLOW, 0x35)

Contains the lower 4-bits of the 12-bit MSL2023 main string duty cycle setting. The upper 8-bits are in register 0x34. The registers combine to form the main string duty cycle, a linear relation where 0x000 = 0% to 0xFFF = 100%. When changed, the duty cycle updates at the beginning of the next output PWM period.

Table 13-8. Main String Duty Cycle Low register (MDUTYLOW, 0x35), defaults highlighted.

Register name	Address	Register name							
		D7	D6	D5	D4	D3	D2	D1	D0
MDUTYLOW	0x35	–	–	–	–	MDUTYLOW [3:0]			
DEFAULT = 0x0F		0	0	0	0	1	1	1	1

13.9 Color Adjust String Duty Cycle register, High Byte (CADUTYHIGH, 0x36)

Contains the upper 8-bits of the 12-bit MSL2023 color-adjust string duty cycle setting. The remaining 4-bits are in register 0x37. The registers combine to form the color-adjust string duty cycle, a linear relation where 0x000 = 0% to 0xFFF = 100%. When changed, the duty cycle updates at the beginning of the next output PWM period.

Table 13-9. Color Adjust String Duty Cycle High register (CADUTYHIGH, 0x36), defaults highlighted.

Register name	Address	Register data							
		D7	D6	D5	D4	D3	D2	D1	D0
CADUTYHIGH	0x36	CADUTYHIGH[11:4]							
DEFAULT = 0xFF		1	1	1	1	1	1	1	1

13.10 Color Adjust String Duty Cycle register, Low Byte (CADUTYLOW, 0x37)

Contains the lower 4-bits of the 12-bit MSL2023 color-adjust string duty cycle setting. The upper 8-bits are in register 0x36. The registers combine to form the color-adjust string duty cycle, a linear relation where 0x000 = 0% to 0xFFF = 100%. When changed, the duty cycle updates at the beginning of the next output PWM period.

Table 13-10. Color Adjust String Duty Cycle Low register (CADUTYLOW, 0x37), default highlighted.

Register name	Address / Default	Register data							
		D7	D6	D5	D4	D3	D2	D1	D0
CADUTYLOW	0x37	–	–	–	–	CADUTYLOW[3:0]			
DEFAULTS = 0x0F		**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**

13.11 Efficiency Optimizer Control Register (EOCTRL, 0x40)

Configures three functions associated with the Adaptive SourcePower™ Efficiency Optimizer (EO). It is recommended that all EO controls be configured while SLEEP (bit D0 in the Configuration register 0x24) is 1 to avoid perturbations of the string power supply. The MSL2023/24 always perform a power supply voltage calibration when power is applied, EN is taken high, or SLEEP is reset to 0.

DThresh sets the voltage feedback threshold for D, the main string MOSFET drain connection. D Threshold = (DThresh*150mV) + 250mV. This is how the device monitors V_{LED} to control the magnitude of the EO current. The default value for DThresh is 1V.

Table 13-11. Efficiency Optimizer Control Register (FBOCTRL, 0x40), defaults highlighted.

Register name	Address	Register data							
		D7	D6	D5	D4	D3	D2	D1	D0
FBOCTRL	0x40	Reserved[3:0]				DTHRESH[3:0]			
DEFAULT = 0xE5		**1**	**1**	**1**	**0**	**0**	**1**	**0**	**1**
D Threshold = (0 * 150mV) + 250mV = 0.25V		1	1	1	0	0	0	0	0
D Threshold = (5 * 150mV) + 250mV = 1V		1	1	1	0	0	1	0	1
D Threshold = (15 * 150mV) + 250mV = 2.5V		1	1	1	0	1	1	1	1

13.12 Registers 0x60 and 0x61, EEPROM Access

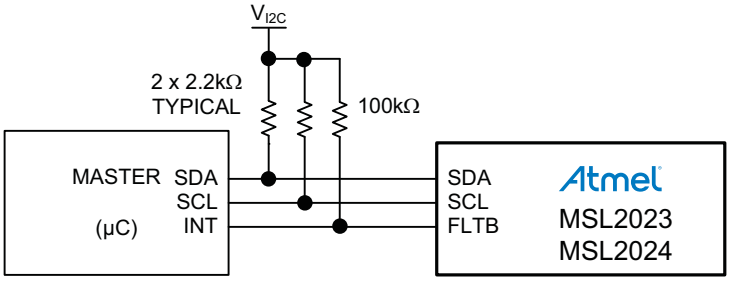
These registers control access to the EEPROM. See “EEPROM and Power-Up Defaults” and “EEPROM Address and Control/Status Registers” on page 25 for information.

14. I²C Serial Interface

The MSL2023/24 operate as slaves that send and receive data through an I²C/SMBus compatible 2-wire serial interface. The interface is not needed for operation, but is provided to allow control and monitoring of device functions. These functions include changing the string current reference feedback voltages, reading and adjusting the fault response behavior and status, putting the device to sleep without losing the register settings, and programming the EEPROM. The I²C/SMBus compatible interface is suitable for 100kHz, 400kHz and 1MHz communication. The interface uses data I/O SDA and clock input SCL to achieve bidirectional communication between master and slaves. Fault output FLTB optionally alerts the host system to faults detected by the MSL2023/24 (Figure 14-1 on page 31 and “Fault Conditions” on page 18). During over temperature shutdown the serial interface is disabled.

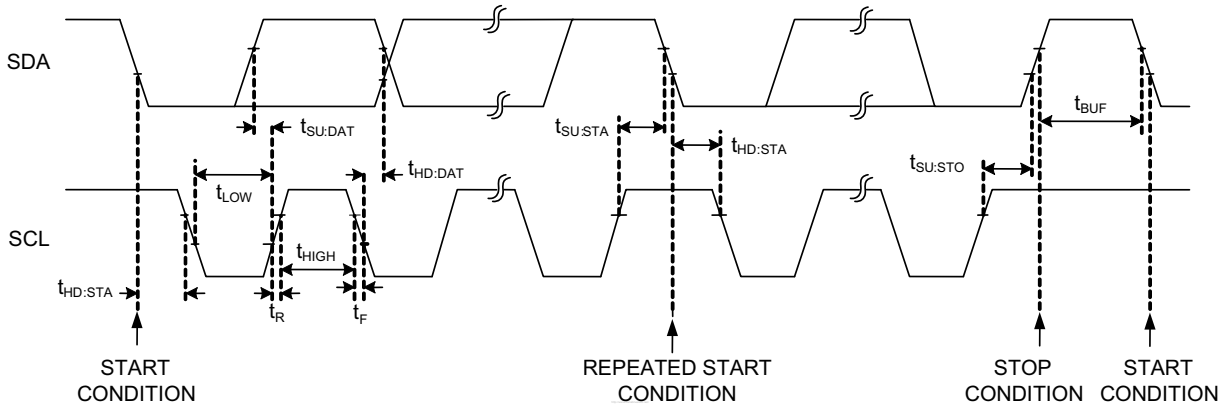
The master, typically a microcontroller, initiates all data transfers, and generates the clock that synchronizes the transfers. SDA operates as both an input and an open-drain output. SCL operates only as an input, and does not perform clock-stretching. Pull-up resistors are required on SDA, SCL and FLTB.

Figure 14-1. I²C interface connections.



A transmission consists of a START condition sent by a master, a 7-bit slave address plus one R/W bit, an acknowledge bit, none or many data bytes each separated by an acknowledge bit, and a STOP condition (Figure 14-2, Figure 14-4 and Figure 14-5 on page 32).

Figure 14-2. I²C serial interface timing details.



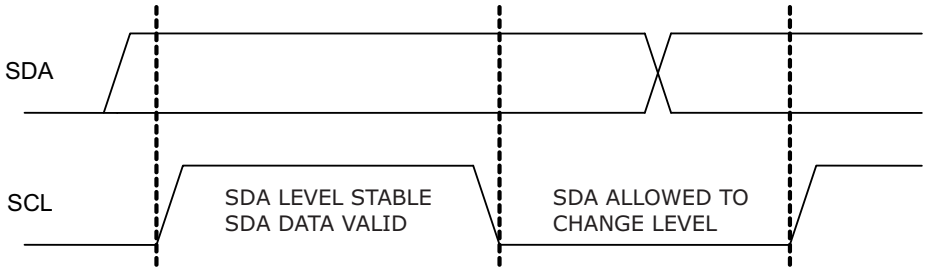
14.1 I²C Bus Timeout

The bus timeout feature allows the MSL2023/24 to reset the serial bus interface if a communication ceases before a STOP condition is sent. If SCL or SDA is low for more than 25ms (typical), then the MSL2023/24 terminates the transaction, releases SDA and waits for another START condition.

14.2 I²C Bit Transfer

One data bit is transferred during each clock pulse. SDA must remain stable while SCL is high.

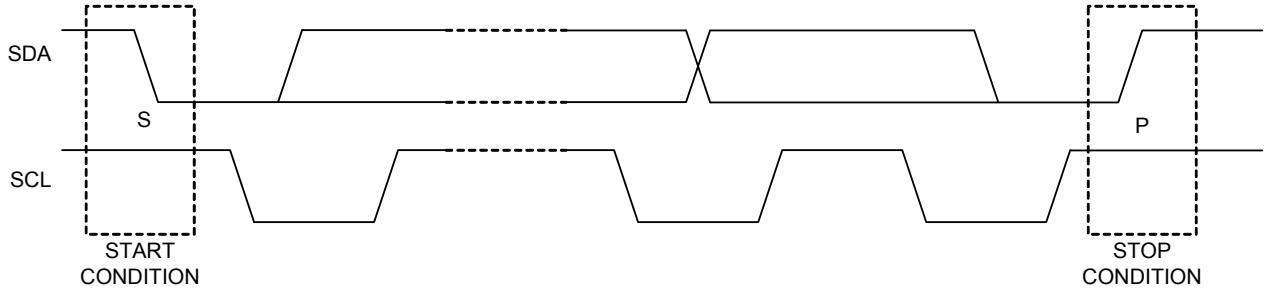
Figure 14-3. I²C bit transfer.



14.3 I²C START and STOP Conditions

Both SCL and SDA remain high when the interface is free. The master signals a transmission with a START condition (S) by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition (P) by transitioning SDA from low to high while SCL is high. The bus is then free.

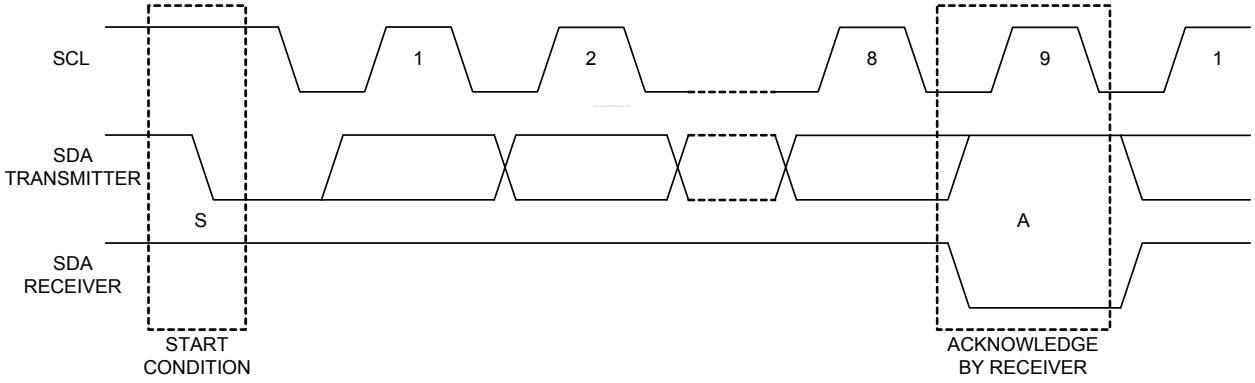
Figure 14-4. I²C START and STOP conditions.



14.4 I²C Acknowledge Bit

The acknowledge bit is a clocked 9th bit which the recipient uses to handshake receipt of each byte of data. The master generates the 9th clock pulse, and the recipient holds SDA low during the high period of the clock pulse. When the master is transmitting to the MSL2023/24, the MSL2023/24 pulls SDA low because the MSL2023/24 is the recipient. When the MSL2023/24 is transmitting to the master, the master pulls SDA low because the master is the recipient.

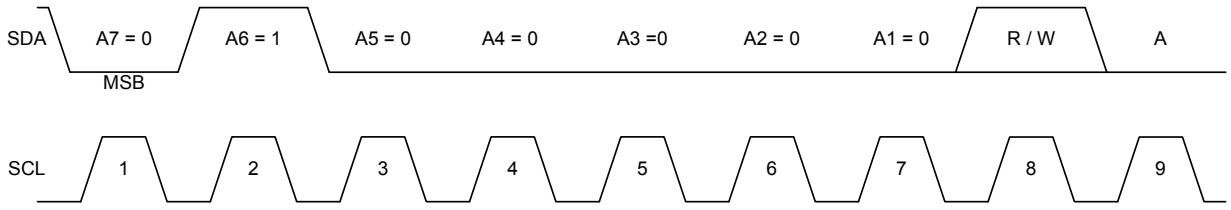
Figure 14-5. I²C acknowledge.



14.5 I²C Slave Address

The MSL2023/24 has a 7-bit long slave address, 0b0100000, followed by an eighth bit, the R/W bit. The R/W bit is low for a write to the MSL2023/24, high for a read from the MSL2023/24. All MSL2023/24 devices have the same slave address; when using multiple devices and communicating with them through their serial interfaces, make external provision to route the serial interface to the appropriate device. Note that development systems that use I²C often left-shift the address one position before they insert the R/W bit, and so expect a default address of 0x20 (not 0x40).

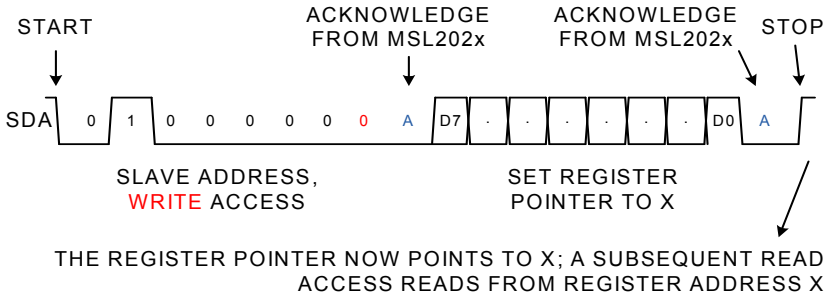
Figure 14-6. I²C slave address.



14.6 I²C Message Format for Writing to the MSL2023/24

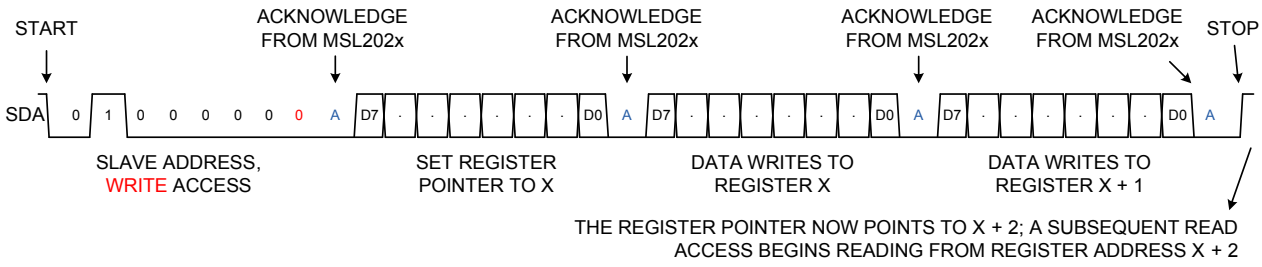
A write to the MSL2023/24 contains the MSL2023/24's slave address, the R/W bit cleared to 0, and at least 1 byte of information (Figure 14-7 on page 33). The first byte of information is the register address byte. The register address byte is stored as a register pointer, and determines which register the following byte is written into. If a STOP condition is detected after the register address byte is received, then the MSL2023/24 takes no further action beyond setting the register pointer.

Figure 14-7. I²C writing a register pointer.



When no STOP condition is detected, the byte transmitted after the register address byte is a data byte, and is placed into the register pointed to by the register address byte (Figure 14-8). To simplify writing to multiple consecutive registers, the register pointer auto-increments during each following acknowledge period. Further data bytes transmitted before a STOP condition fill subsequent registers.

Figure 14-8. I²C writing two data bytes.

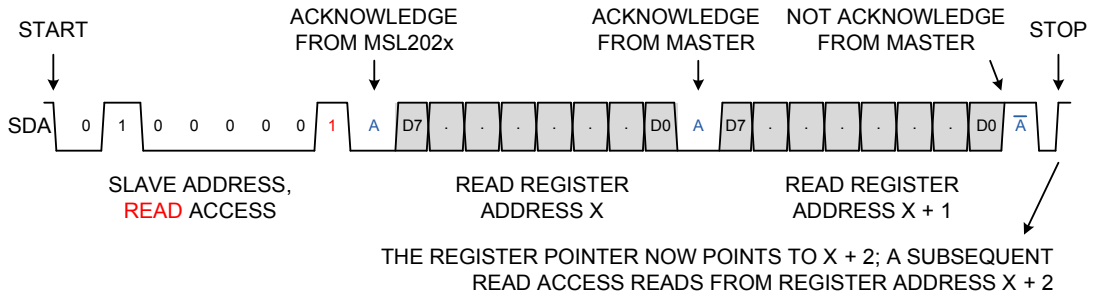


14.7 I²C Message Format for Reading from the MSL2023/24

The first technique begins the same way as a write, by setting the register address pointer as shown in Figure 14-7, including the STOP condition (note that even though the final objective is to read data, the R/W bit is first sent as a write because the address pointer byte is being written into the device). Follow the Figure 14-7 transaction by what shown in Figure 14-9, with a new START condition and the slave address, this time with the R/W bit set to 1 to indicate a read. Then, after the slave initiated acknowledge bit, clock out as many bytes as desired, separated by master initiated

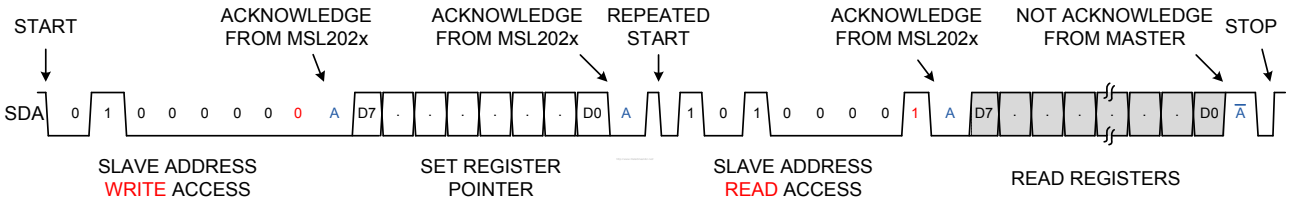
acknowledges. The pointer auto-increments during each master initiated acknowledge period. End the transmission with a not-acknowledge followed by a stop condition.

Figure 14-9. I²C reading register data with preset register pointer.



The second read technique is illustrated in Figure 14-10. Write to the MSL2023/24 to set the register pointer, send a repeated START condition after the second acknowledge bit, then send the slave address again with the R/W bit set to 1 to indicate a read. Then clock out the data bytes separated by master initiated acknowledge bits. The register pointer auto-increments during each master initiated acknowledge period. End the transmission with a not-acknowledge followed by a stop condition. This technique is recommended for buses with multiple masters, because the read sequence is performed in one uninterruptible transaction.

Figure 14-10. I²C reading register data using a repeated START

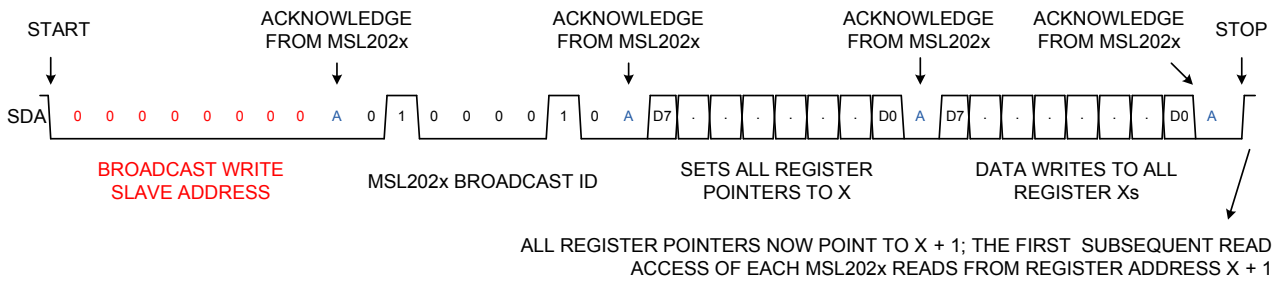


14.8 I²C Message Format for Broadcast Writing to Multiple devices

With a broadcast write to MSL2023/24, a master broadcasts the same register data to all MSL2023/24s on the bus. First send the broadcast write slave address of 0x00, followed by the MSL2023/24 broadcast device ID of 0x42. These two bytes are followed by the register address in the MSL2023/24s that the following data are to be written into, and finally the data byte(s) to be written into all devices.

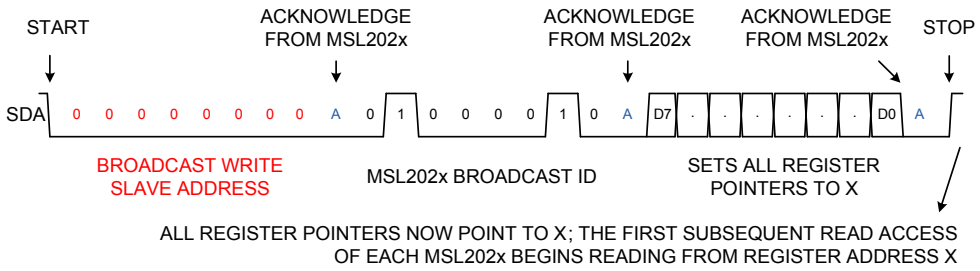
A broadcast write example is shown in Figure 14-11. Here, the same register address in every MSL2023/24 is written to with identical data. If further data bytes are transmitted before the STOP condition, they are stored in subsequent internal registers of each MSL2023/24.

Figure 14-11. I²C broadcast writing a data byte.

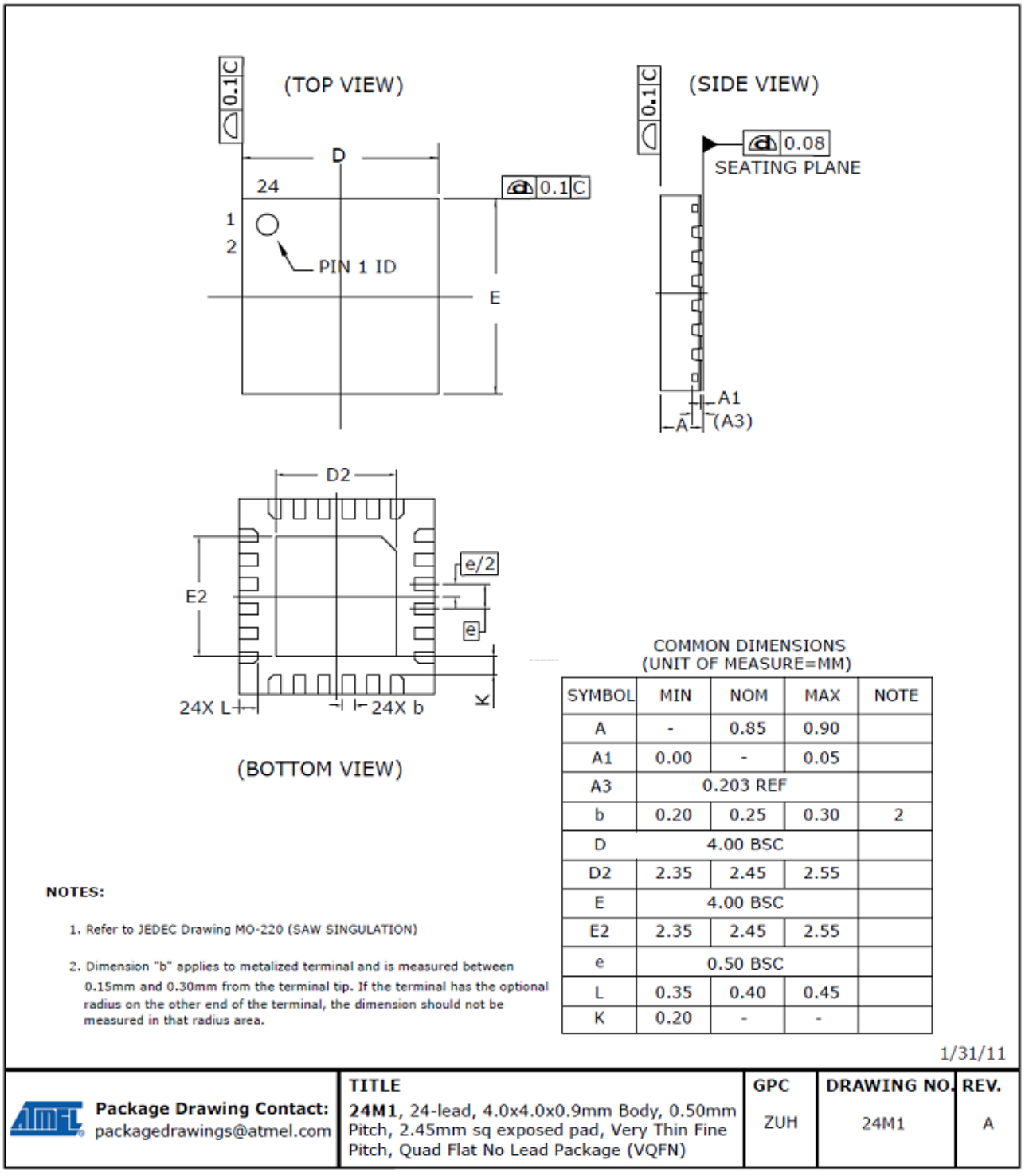


There is no broadcast read. However, a broadcast write may be used to set up the internal register pointers of all the MSL2023/24s in a system to speed up the subsequent individual reading of, for example, all the status registers. Figure 14-12 illustrates a broadcast write that sets all the register pointers, and issues a STOP.

Figure 14-12. I²C broadcast writing a register pointer.



15. Packaging Information



COMMON DIMENSIONS
(UNIT OF MEASURE=MM)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	0.85	0.90	
A1	0.00	-	0.05	
A3		0.203 REF		
b	0.20	0.25	0.30	2
D		4.00 BSC		
D2	2.35	2.45	2.55	
E		4.00 BSC		
E2	2.35	2.45	2.55	
e		0.50 BSC		
L	0.35	0.40	0.45	
K	0.20	-	-	

NOTES:

1. Refer to JEDEC Drawing MO-220 (SAW SINGULATION)
2. Dimension "b" applies to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

1/31/11

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	24M1, 24-lead, 4.0x4.0x0.9mm Body, 0.50mm Pitch, 2.45mm sq exposed pad, Very Thin Fine Pitch, Quad Flat No Lead Package (VQFN)	ZUH	24M1	A

No representation or warranties are made concerning third-party patents with regard to the use of Atmel® products. The mixing of red LEDs with phosphor-converted LEDs may be protected by certain third-party patents, such as U.S. Patent No. 7,213,940 and related patents of Cree, Inc.

16. Datasheet Revision History

16.1 42063A – 02/2013

1.	Initial revision.

Table of Contents

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Atmel | Enabling Unlimited Possibilities®

Atmel Corporation
1600 Technology Drive
San Jose, CA 95110
USA
Tel: (+1) (408) 441-0311
Fax: (+1) (408) 487-2600
www.atmel.com

Atmel Asia Limited
Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Roa
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan G.K.
16F Shin-Osaki Kangyo Bldg
1-6-4 Osaki, Shinagawa-ku
Tokyo 141-0032
JAPAN
Tel: (+81) (3) 6417-0300
Fax: (+81) (3) 6417-0370