

MITSUBISHI LSTTLs

M74LS256P

DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION

The M74LS256P is a semiconductor integrated circuit containing a dual demultiplexer circuit configured into a 4-bit latch addressable in 2-bit binary code.

FEATURES

- Easily expandable
- May be used as a 2-bit binary-to-quaternary decoder/demultiplexer
- Active low common reset
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

APPLICATION

General purpose, for use in industrial and consumer equipment

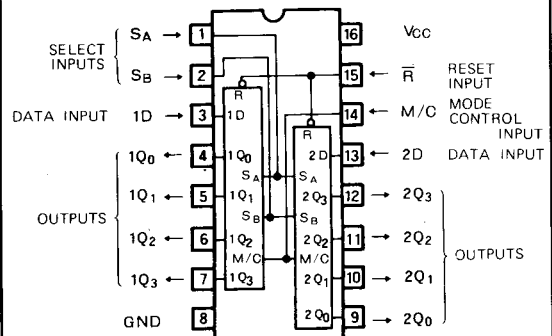
FUNCTIONAL DESCRIPTION

This device is configured from two circuits providing the capability to function as a 2-bit binary-to-quaternary demultiplexer or as a 4-bit latch. The operational modes listed below are selectable using mode control input M/C. (common to both circuits) and reset input \bar{R} in combination.

- (1) 2-bit binary-to-quaternary decoder/demultiplexer
- (2) Addressable latch
- (3) Data input inhibit
- (4) Reset

When used as a 2-bit binary-to-quaternary decoder/demultiplexer and a 2-bit binary number is applied to select inputs S_A and S_B , one of the $Q_0 \sim Q_3$ outputs will correspond to that number, and the signal appearing at its output will be the same as the one present at data input D. All other outputs will remain low-level at this time; and latch operations are not performed in this mode.

PIN CONFIGURATION (TOP VIEW)



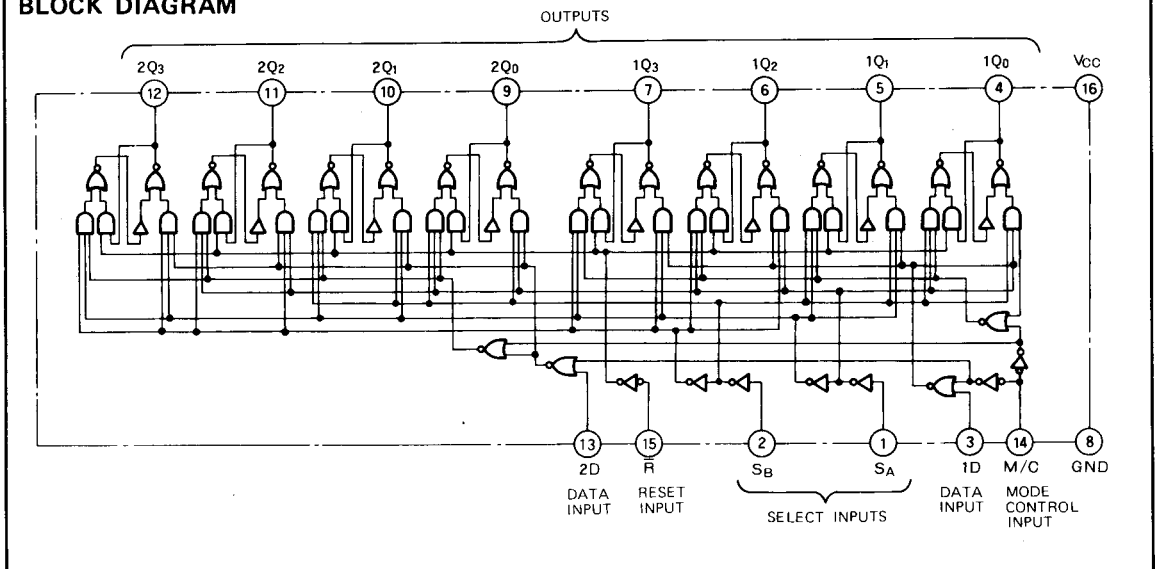
Outline 16P4

When used as an addressable latch, S_A and S_B will be decoded as in the above operation, with the corresponding latch being selected. The signal present at data input D will then appear at output. When M/C transits from low to high (data inhibit mode), the information present at D immediately prior to that event will be latched. When M/C is low-level, changing the signal at D will also change the signal present at Q .

During the data input inhibit mode, changes applied to D will not affect $Q_0 \sim Q_3$, and the status prior to M/C transiting high will be held.

Direct reset is activated by all outputs at low-level, regardless of the status of D, S_A , and S_B .

BLOCK DIAGRAM



DUAL 4-BIT ADDRESSABLE LATCH
FUNCTION TABLE (Note 1)

Operational mode	\bar{R}	M/C	D	S _A	S _B	Q ₀	Q ₁	Q ₂	Q ₃
Reset	L	H	X	X	X	L	L	L	L
Active high 4-channel demultiplexers	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	H	L	L	L
	L	L	L	H	L	L	L	L	L
	L	L	H	H	L	L	H	L	L
	L	L	L	L	H	L	L	L	L
	L	L	H	L	H	L	L	H	L
	L	L	L	H	H	L	L	L	L
Memory	H	H	X	X	X	Q ₀ ⁰	Q ₁ ⁰	Q ₂ ⁰	Q ₃ ⁰
Addressable latch	H	L	L	L	L	L	Q ₁ ⁰	Q ₂ ⁰	Q ₃ ⁰
	H	L	H	L	L	H	Q ₁ ⁰	Q ₂ ⁰	Q ₃ ⁰
	H	L	L	H	L	Q ₀ ⁰	L	Q ₂ ⁰	Q ₃ ⁰
	H	L	H	H	L	Q ₀ ⁰	H	Q ₂ ⁰	Q ₃ ⁰
	H	L	L	L	H	Q ₀ ⁰	Q ₁ ⁰	L	Q ₃ ⁰
	H	L	H	L	H	Q ₀ ⁰	Q ₁ ⁰	H	Q ₃ ⁰
	H	L	L	H	H	Q ₀ ⁰	Q ₁ ⁰	Q ₂ ⁰	L
	H	L	H	H	H	Q ₀ ⁰	Q ₁ ⁰	Q ₂ ⁰	H

Note 1. X : Irrelevant

 Q⁰ : Indicates output status prior to input conditions being set.

ABSOLUTE MAXIMUM RATINGS (T_a = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V _{CC}	Supply voltage		-0.5 ~ +7	V
V _i	Input voltage		-0.5 ~ +15	V
V _o	Output voltage	High-level state	-0.5 ~ V _{CC}	V
T _{opr}	Operating free-air ambient temperature range		-20 ~ +75	°C
T _{stg}	Storage temperature range		-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V _{CC}	Supply voltage		4.75	5	5.25	V
I _{OH}	High-level output current	V _{OH} ≥ 2.7V	0		-400	μA
I _{oL}	Low-level output current	V _{OL} ≤ 0.4V	0		4	mA
		V _{OL} ≤ 0.5V	0		8	mA

DUAL 4-BIT ADDRESSABLE LATCH
ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ *	Max		
V_{IH}	High-level input voltage		2			V	
V_{IL}	Low-level input voltage				0.8	V	
V_{IC}	Input clamp voltage	$V_{CC}=4.75\text{V}$, $I_{IC}=-18\text{mA}$			-1.5	V	
V_{OH}	High-level output voltage	$V_{CC}=4.75\text{V}$, $V_I=0.8\text{V}$ $V_I=2\text{V}$, $I_{OH}=-400\mu\text{A}$	2.7	3.4		V	
V_{OL}	Low-level output voltage	$V_{CC}=4.75\text{V}$		0.25	0.4	V	
		$V_I=0.8\text{V}$, $V_I=2\text{V}$		0.35	0.5	V	
I_{IH}	High-level input current	M/C			40	μA	
		Exclusive of M/C			20		
		M/C	$V_{CC}=5.25\text{V}$, $V_I=10\text{V}$			0.2	mA
		Exclusive of M/C				0.1	
I_{IL}	Low-level input current	M/C			-0.8	mA	
		Exclusive of M/C	$V_{CC}=5.25\text{V}$, $V_I=0.4\text{V}$			-0.4	
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25\text{V}$, $V_O=0\text{V}$	-20		-100	mA	
I_{CC}	Supply current	$V_{CC}=5.25\text{V}$ (Note 3)		20	36	mA	

* : All typical values are at $V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

3. I_{CC} is measured with all inputs at 0V.

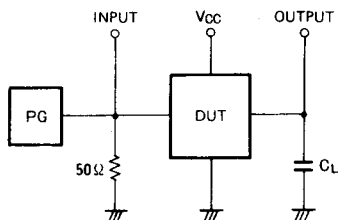
SWITCHING CHARACTERISTICS ($V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PHL}	High-to-low-level output propagation time, from input \bar{R} to output $Q_0\sim Q_3$	$C_L=15\text{pF}$ (Note 4)		9	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to output $Q_0\sim Q_3$			15	32	ns
t_{PHL}				11	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input S_A, S_B to output $Q_0\sim Q_3$			15	38	ns
t_{PHL}				11	29	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input M/C to output $Q_0\sim Q_3$			14	35	ns
t_{PHL}				13	24	ns

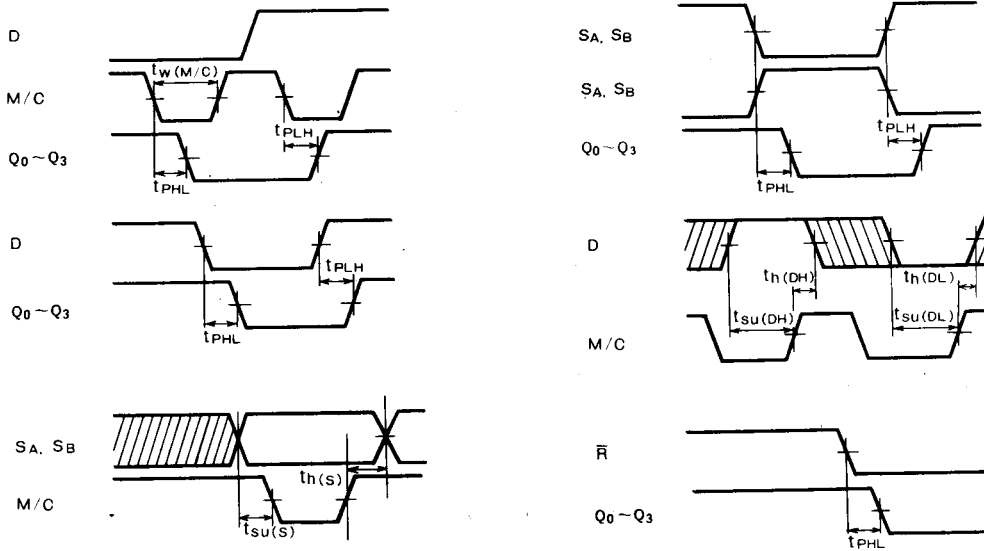
TIMING REQUIREMENTS ($V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su}(DH)$	D high-level setup time to M/C		15	10		ns
$t_h(DH)$	D high-level hold time to M/C		5	-	5	ns
$t_{su}(DL)$	D low-level setup time to M/C		15	8		ns
$t_h(DL)$	D low-level hold time to M/C		5	-	7	ns
$t_{su}(S)$	S_A, S_B setup time to M/C		15	7		ns
$t_h(S)$	S_A, S_B hold time to M/C		5	-	5	ns
$t_w(M/C)$	M/C pulse width		15	8		ns
$t_w(\bar{R})$	\bar{R} pulse width		15	7		ns

Note 4. Measurement Circuit



- (1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, $t_r = 6\text{ns}$, $t_f = 6\text{ns}$, $t_w = 500\text{ns}$, $V_p = 3V_{p-p}$, $Z_0 = 50\Omega$.
- (2) C_L includes probe and jig capacitance.

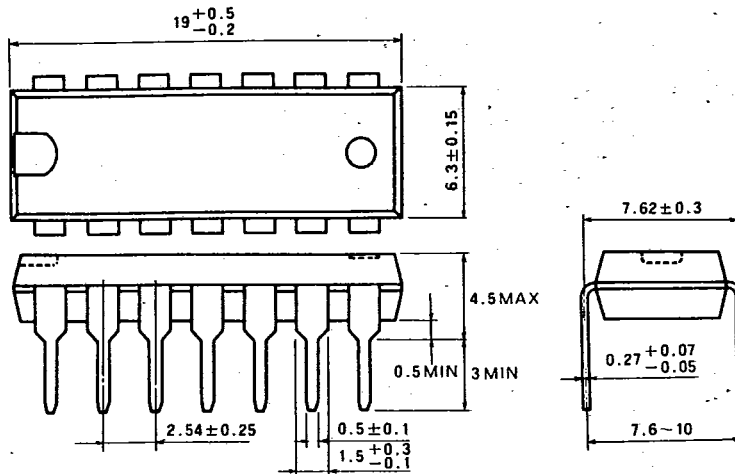
DUAL 4-BIT ADDRESSABLE LATCH
TIMING DIAGRAM (Reference level = 1.3V)


Note 5. Shaded area denotes the time period in which switching is possible.

www.DataSheet4U.com

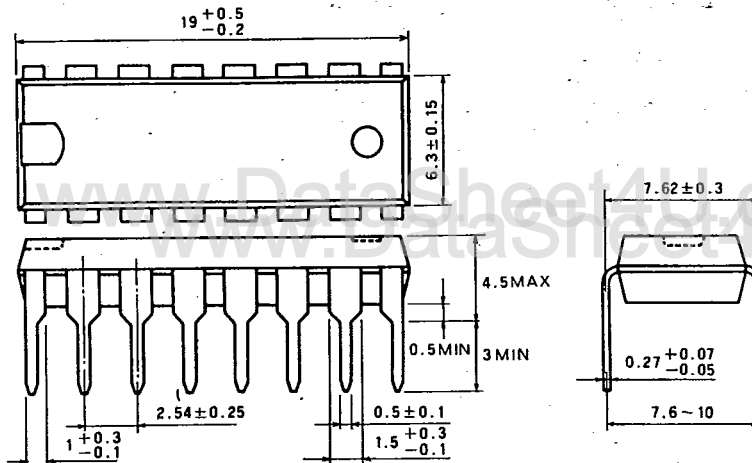
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

