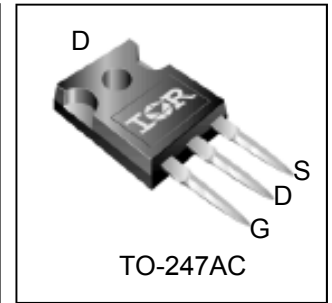
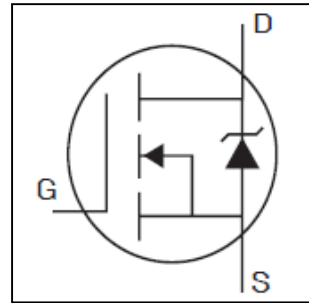


$V_{DSS}$	<b>300V</b>
$R_{DS(on)}$ <b>typ.</b>	<b>25.5m<math>\Omega</math></b>
<b>max.</b>	<b>32m<math>\Omega</math></b>
$I_D$	<b>70A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

**Applications**

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP4868PbF	TO-247AC	Tube	25	IRFP4868PbF

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	70	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	49	
$I_{DM}$	Pulsed Drain Current ①	280	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	517	W
	Linear Derating Factor	3.4	W/ $^\circ\text{C}$
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ\text{C}$
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf.in (1.1N.m)	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	1093	mJ
$I_{AR}$	Avalanche Current ①	See Fig. 14, 15, 22a, 22b	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦⑧	—	0.29	
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient	—	40	

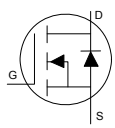
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	300	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.29	—	V/°C	Reference to 25°C, I <sub>D</sub> = 5mA <sup>①</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	25.5	32	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 42A <sup>④</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0	—	5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 300V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 300V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
R <sub>G</sub>	Internal Gate Resistance	—	1.1	—	Ω	

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	80	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 42A
Q <sub>g</sub>	Total Gate Charge	—	180	270	nC	I <sub>D</sub> = 42A
Q <sub>gs</sub>	Gate-to-Source Charge	—	60	—		V <sub>DS</sub> = 150V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	57	—		V <sub>GS</sub> = 10V <sup>④</sup>
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	123	—		I <sub>D</sub> = 42A, V <sub>DS</sub> = 0V, V <sub>GS</sub> = 10V
t <sub>d(on)</sub>	Turn-On Delay Time	—	24	—	ns	V <sub>DD</sub> = 195V
t <sub>r</sub>	Rise Time	—	16	—		I <sub>D</sub> = 42A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	62	—		R <sub>G</sub> = 1.0Ω
t <sub>f</sub>	Fall Time	—	45	—		V <sub>GS</sub> = 10V <sup>④</sup>
C <sub>iss</sub>	Input Capacitance	—	10774	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	612	—		V <sub>DS</sub> = 50V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	193	—		f = 1.0 MHz, See Fig. 5
C <sub>oss</sub> eff. (ER)	Effective Output Capacitance (Energy Related) <sup>⑥</sup>	—	406	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 240V <sup>⑥</sup> , See Fig. 11
C <sub>oss</sub> eff. (TR)	Effective Output Capacitance (Time Related) <sup>⑤</sup>	—	710	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 240V <sup>⑤</sup>

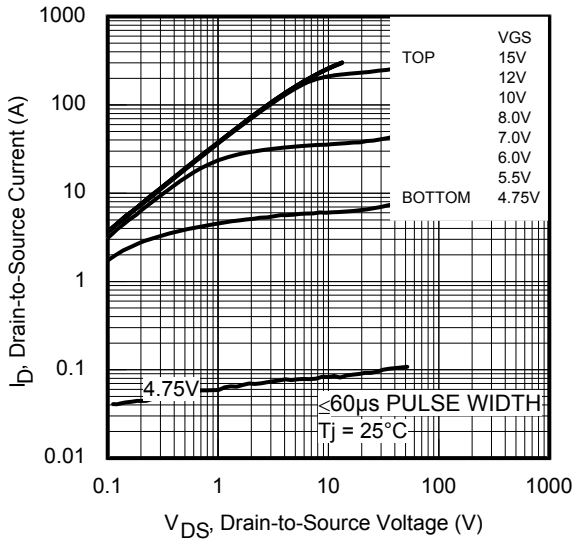
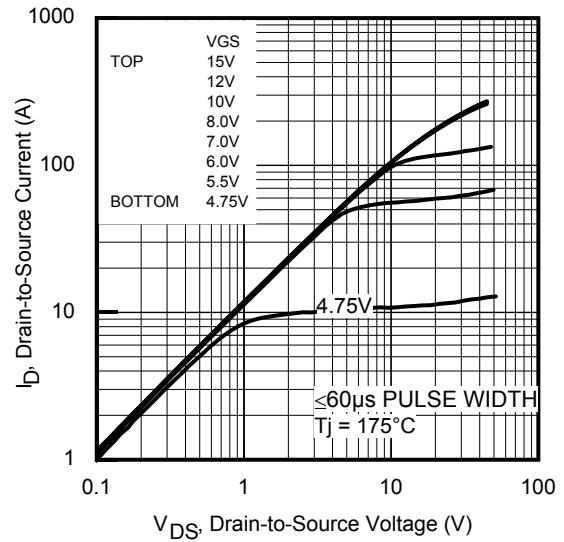
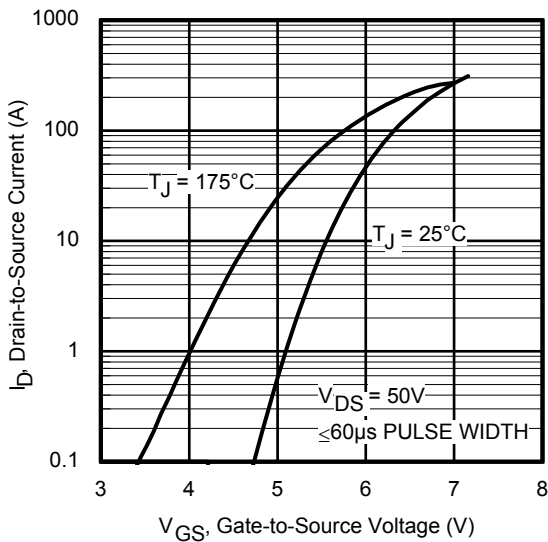
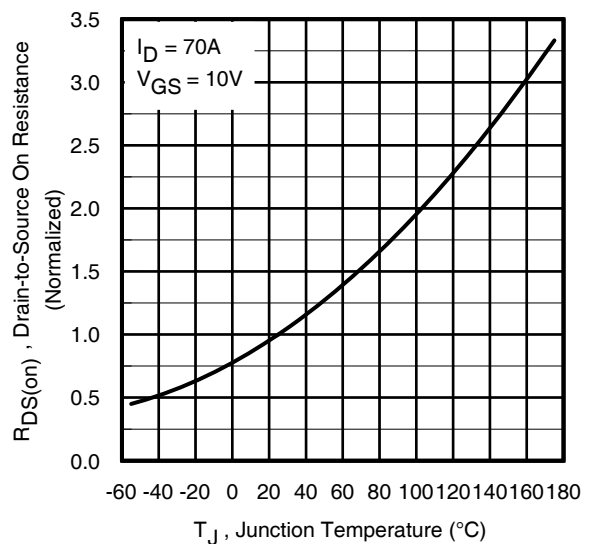
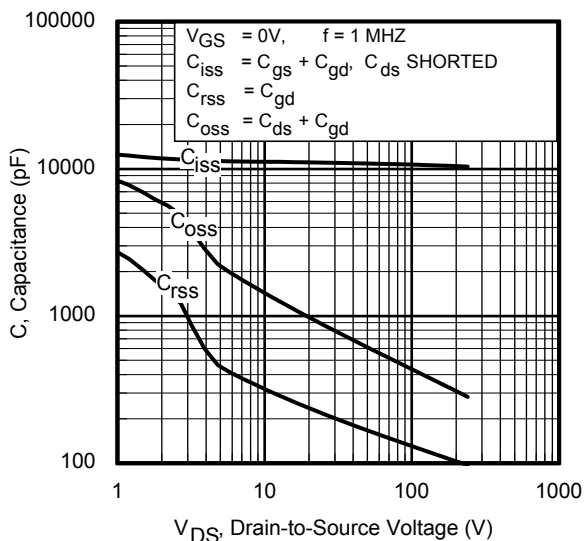
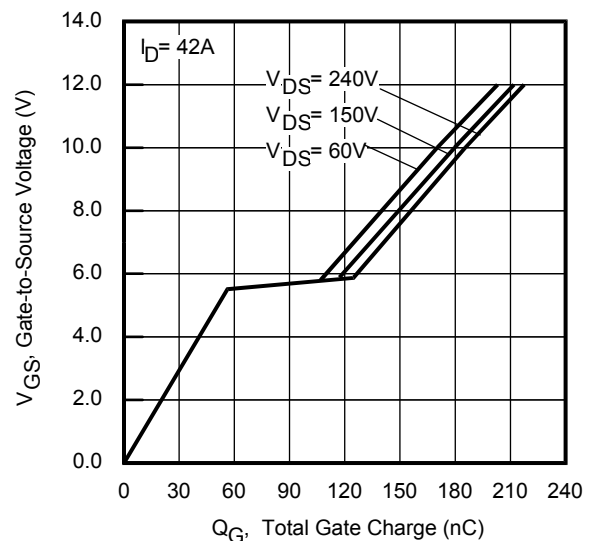
**Diode Characteristics**

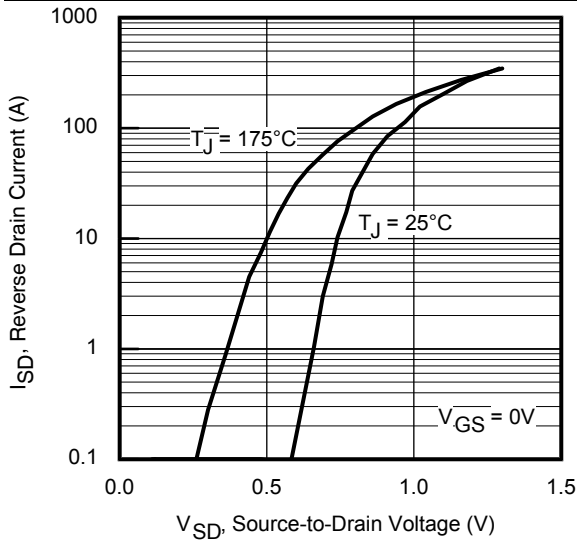
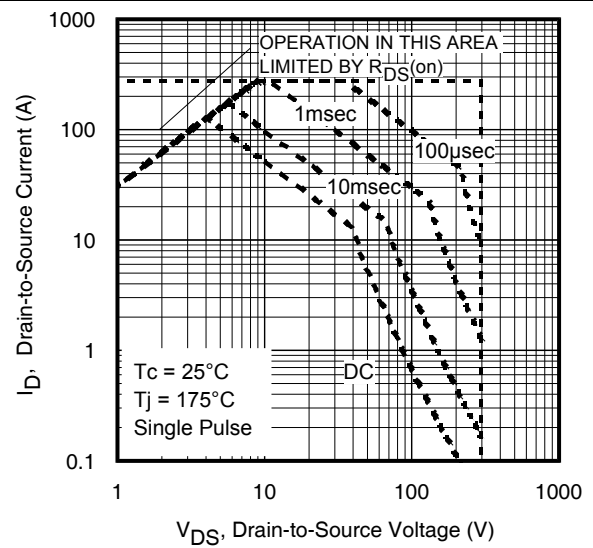
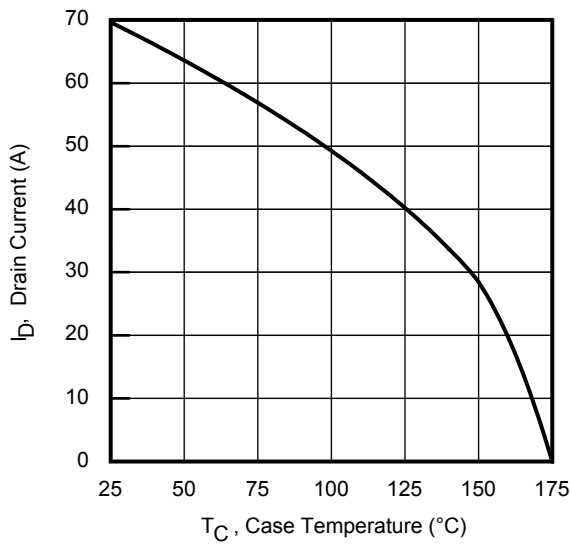
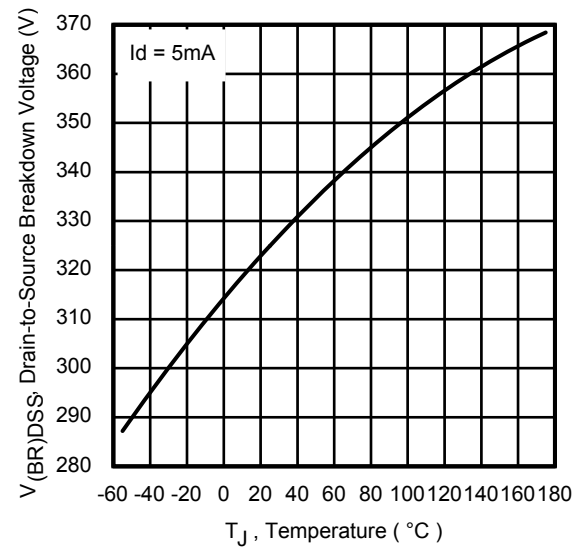
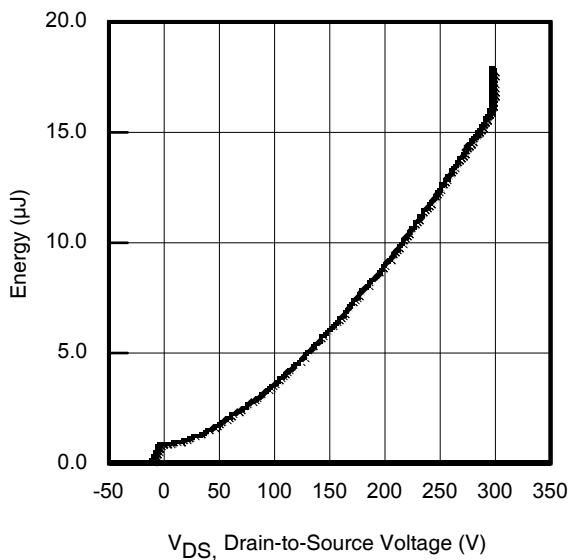
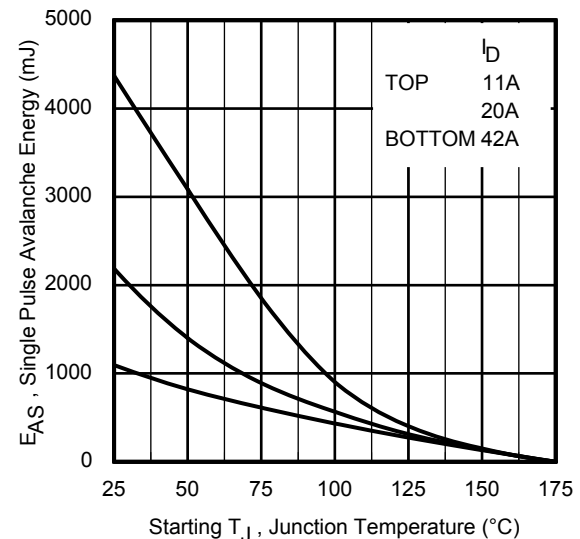
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	70	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①</sup>	—	—	280	A	
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 42A, V <sub>GS</sub> = 0V <sup>④</sup>
dv/dt	Peak Diode Recovery <sup>③</sup>	—	7.3	—	V/ns	T <sub>J</sub> = 25°C, I <sub>S</sub> = 42A, V <sub>DS</sub> = 300V
t <sub>rr</sub>	Reverse Recovery Time	—	351	—	ns	T <sub>J</sub> = 25°C
		—	454	—		T <sub>J</sub> = 125°C
Q <sub>rr</sub>	Reverse Recovery Charge	—	2520	—	nC	T <sub>J</sub> = 25°C
		—	3686	—		T <sub>J</sub> = 125°C
I <sub>RRM</sub>	Reverse Recovery Current	—	16	—	A	T <sub>J</sub> = 25°C
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

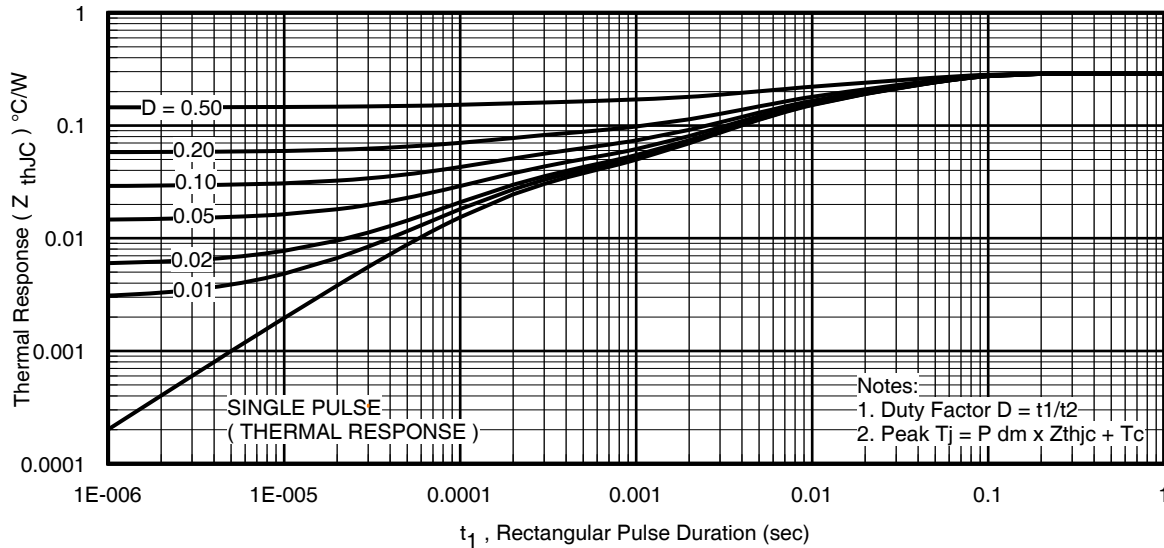
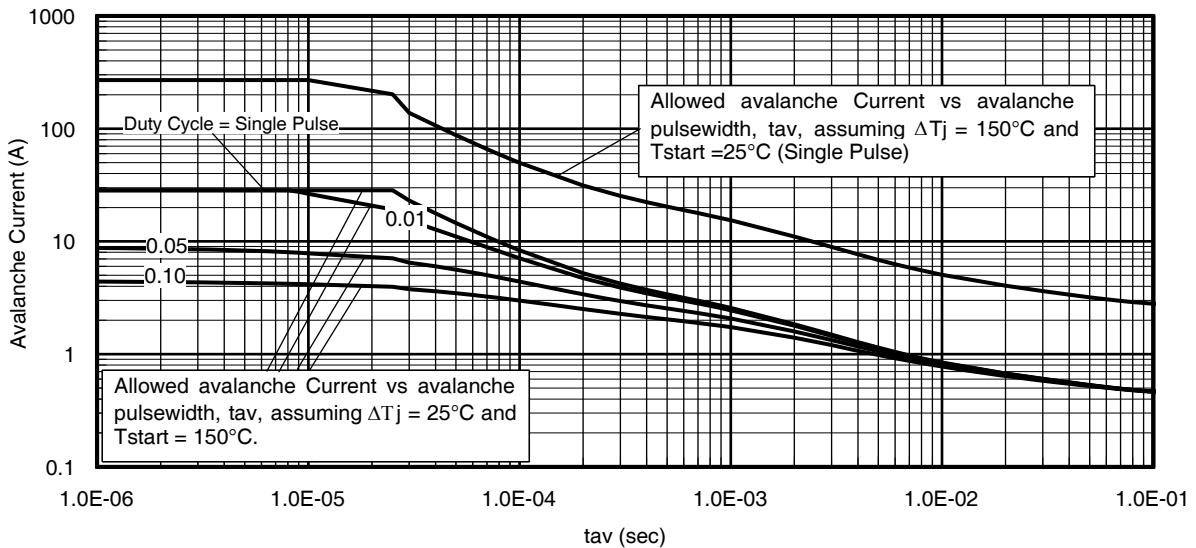
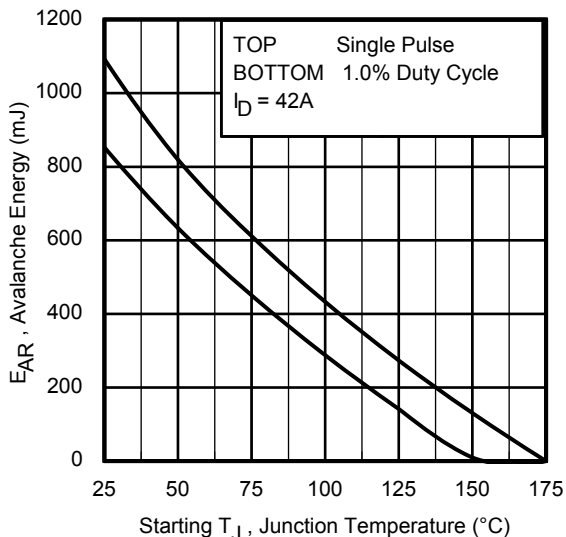
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 1.2mH, R<sub>G</sub> = 50Ω, I<sub>AS</sub> = 42A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ③ I<sub>SD</sub> ≤ 42A, di/dt ≤ 1706A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

- ⑤ C<sub>oss</sub> eff. (TR) is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ C<sub>oss</sub> eff. (ER) is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.
- ⑧ R<sub>θJC</sub> value shown is at time zero.


**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 7.** Typical Source-to-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Drain-to-Source Breakdown Voltage

**Fig 11.** Typical  $C_{oss}$  Stored Energy

**Fig 12.** Maximum Avalanche Energy vs. Drain Current

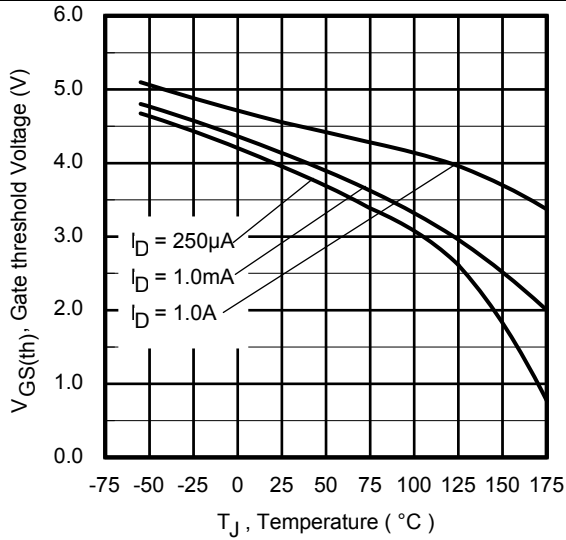
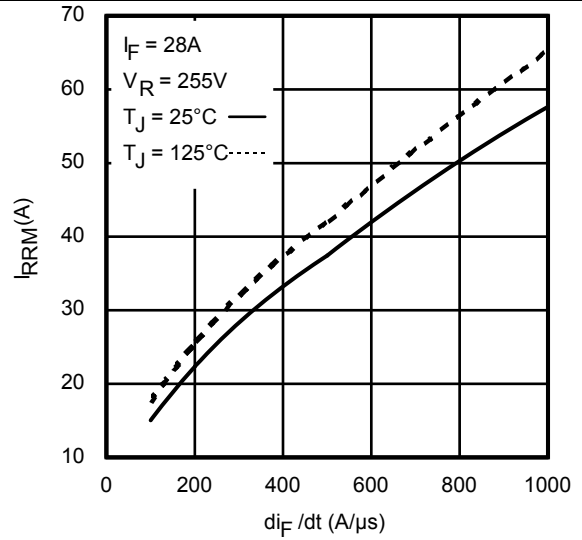
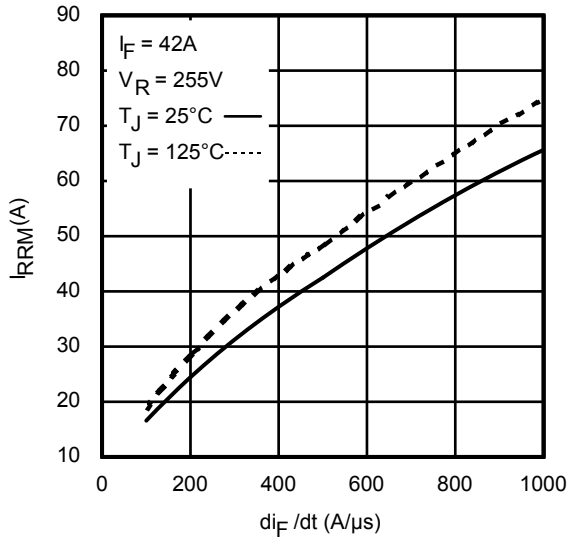
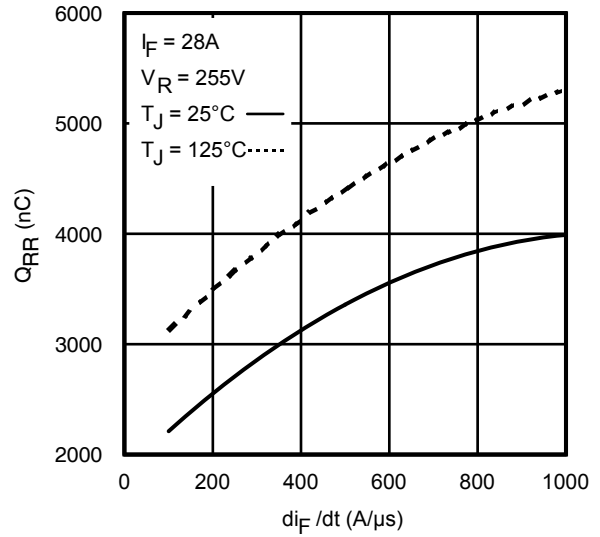
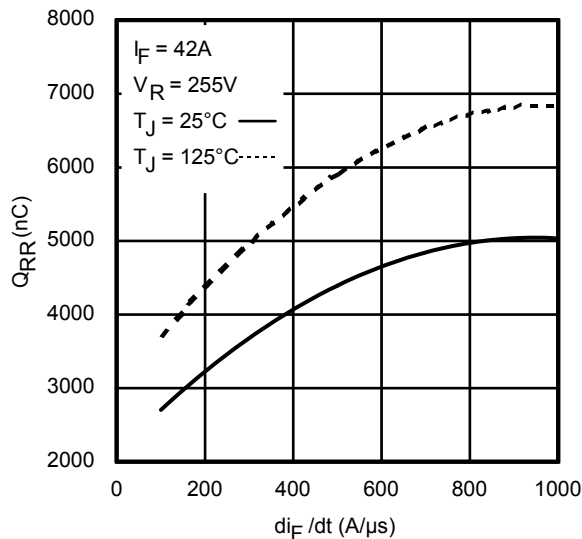

**Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 14. Typical Avalanche Current vs. Pulsewidth**

**Fig 15. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 14, 15:  
(For further info, see AN-1005 at www.irf.com)**

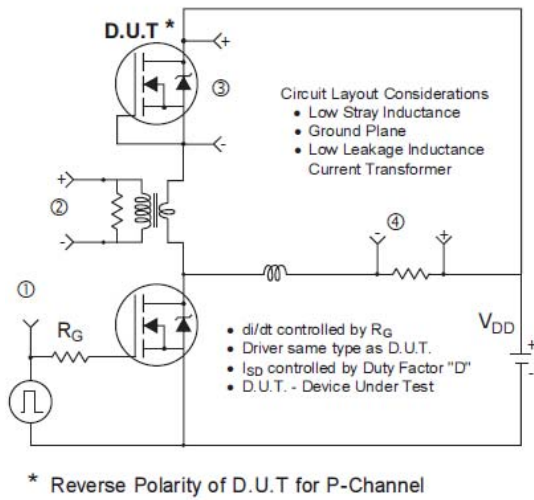
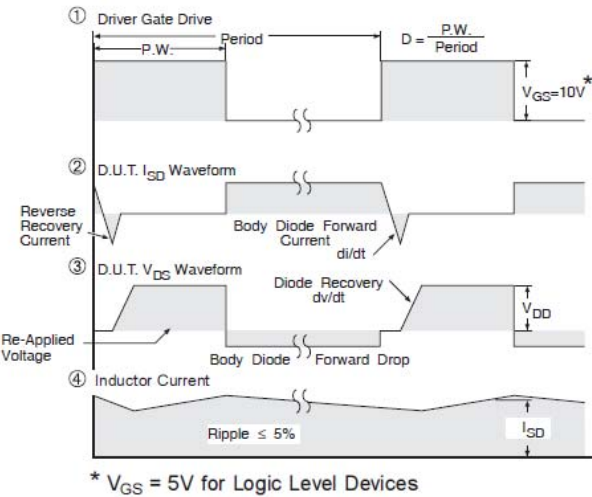
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $tav \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

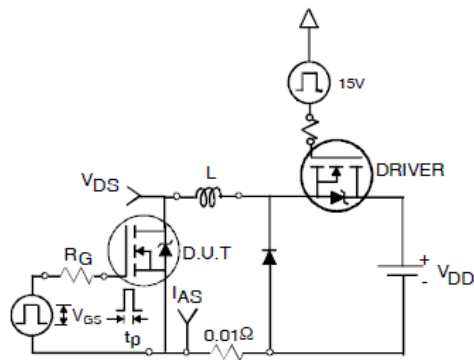
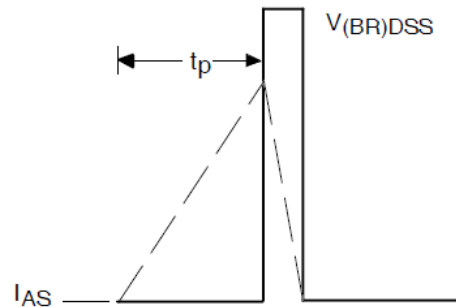
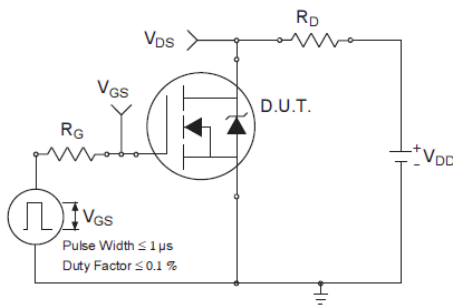
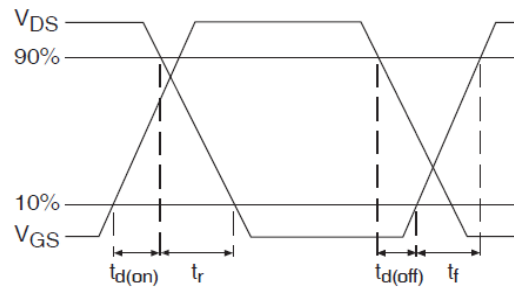
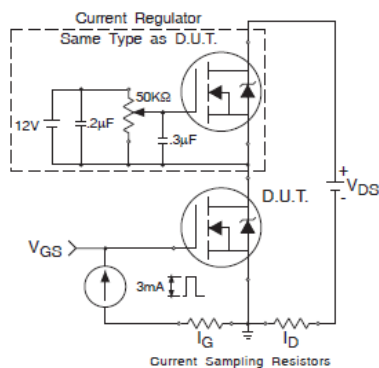
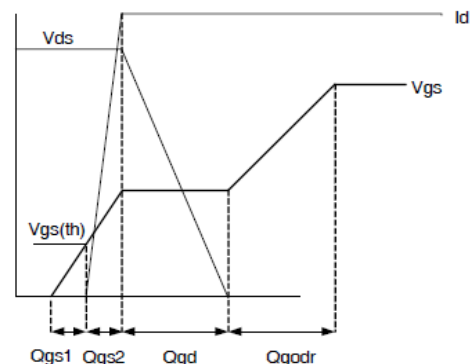
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


**Fig. 16** Threshold Voltage vs. Temperature

**Fig. 17** Typical Recovery Current vs.  $di_F/dt$ 

**Fig. 18.** Typical Recovery Current vs.  $di_F/dt$ 

**Fig. 19.** Typical Stored Charge vs.  $di_F/dt$ 

**Fig. 20.** Typical Stored Charge vs.  $di_F/dt$

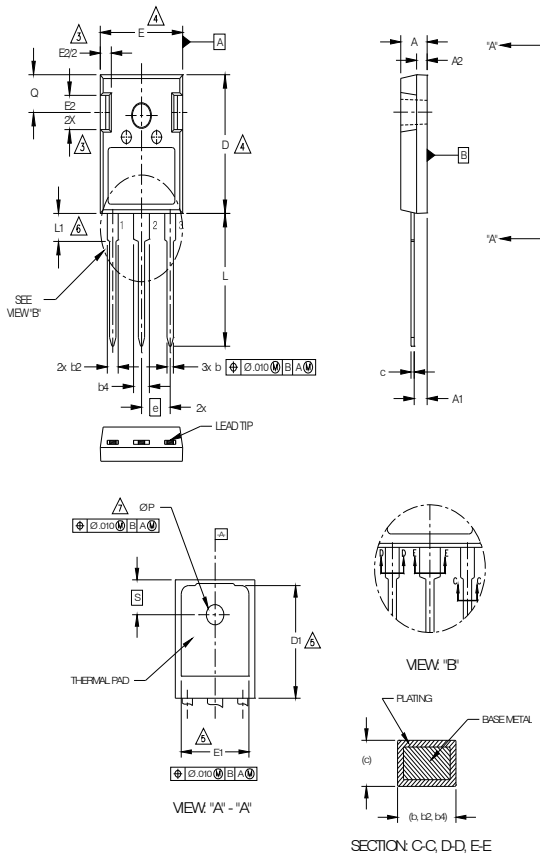

**Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**


\*  $V_{GS} = 5V$  for Logic Level Devices


**Fig 22a. Unclamped Inductive Test Circuit**

**Fig 22b. Unclamped Inductive Waveforms**

**Fig 23a. Switching Time Test Circuit**

**Fig 23b. Switching Time Waveforms**

**Fig 24a. Gate Charge Test Circuit**

**Fig 24b. Gate Charge Waveform**

# TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.190	.204	4.83	5.20	
A1	.090	.100	2.29	2.54	
A2	.075	.085	1.91	2.16	
b	.042	.052	1.07	1.33	
b2	.075	.094	1.91	2.41	
b4	.113	.133	2.87	3.38	
c	.022	.026	0.55	0.68	
D	.819	.830	20.80	21.10	4
D1	.640	.694	16.25	17.65	5
E	.620	.635	15.75	16.13	4
E1	.512	.570	13.00	14.50	
E2	.145	.196	3.68	5.00	
e	.215 Typical		5.45 Typical		
L	.780	.800	19.80	20.32	
L1	.161	.173	4.10	4.40	
ø P	.138	.143	3.51	3.65	
Q	.216	.236	5.49	6.00	
S	.238	.248	6.04	6.30	

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

**DIODES**

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

**NOTES:**

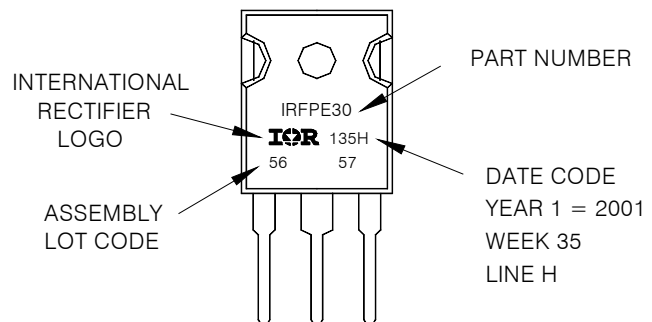
- 1 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
- 2 DIMENSIONS ARE SHOWN IN INCHES AND MILLIMETERS.
- 3 CONTOUR OF SLOT OPTIONAL.
- 4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
- 6 LEAD FINISH UNCONTROLLED IN L1.
- 7 ø P TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.

## TO-247AC Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2001  
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-247 package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



**Qualification information<sup>†</sup>**

Qualification level	Industrial <sup>††</sup> (per JEDEC JESD47F <sup>†††</sup> guidelines )	
Moisture Sensitivity Level	TO-247AC	N/A
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site  
<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.  
 Please contact your International Rectifier sales representative for further information:  
<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.

International  
 Rectifier

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 TAC Fax: (310) 252-7903

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