

August 1991

Features

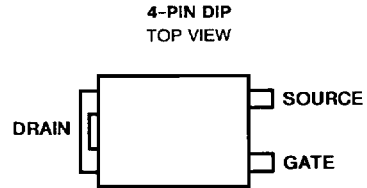
- 0.3A and 0.4A, 350V - 400V
- $r_{DS(on)} = 3.6\Omega$ and 5.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFD310, IRFD311, IRFD312, and IRFD313 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD310R, IRFD311R, IRFD312R, and IRFD313R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

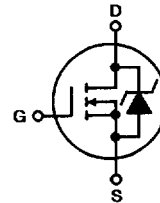
The IRFD types are supplied in the 4-pin dual-in-line plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

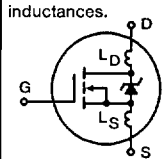
	IRFD310 IRFD310R	IRFD311 IRFD311R	IRFD312 IRFD312R	IRFD313 IRFD313R	UNITS	
Drain-Source Voltage (1)	V_{DS}	400	350	400	350	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR}	400	350	400	350	V
Continuous Drain Current						
$T_C = +25^\circ\text{C}$	I_D	0.4	0.4	0.3	0.3	A
Pulsed Drain Current (3)	I_{DM}	1.6	1.6	1.2	1.2	A
Gate-Source Voltage	V_{GS}	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation						
$T_C = +25^\circ\text{C}$ (See Figure 14)	P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped	I_{LM}	1.6	1.6	1.2	1.2	A
(See Figure 14, $L = 100\mu\text{H}$)						
Single Pulse Avalanche Energy Rating (4)	E_{as}^*	45	45	45	45	mJ
Operating and Storage Junction	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Temperature Range						
Maximum Lead Temperature for Soldering	T_L	300	300	300	300	°C
(0.063" (1.6mm) from case for 10s)						

NOTES:

- $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$.
- Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 15).
- $V_{DD} = 40\text{V}$, starting $T_J = +25^\circ\text{C}$, $L = 44.89\text{mH}$, $R_{GS} = 50\Omega$, $I_{PEAK} = 1.4\text{A}$. See Figure 15.

* R Suffix Types Only

Electrical Characteristics $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
Drain-Source Breakdown Voltage IRFD310/312, IRFD310R/312R IRFD311/313, IRFD311R/313R	BV _{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	400	-	-	V	
			350	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	-	4.0	V	
Gate-Source Leakage Forward	I_{GSS}	$V_{GS} = 20V$	-	-	500	nA	
Gate-Source Leakage Reverse	I_{GSS}	$V_{GS} = -20V$	-	-	-500	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Max Rating}, V_{GS} = 0V$	-	-	250	μA	
		$V_{DS} = \text{Max Rating} \times 0.8, V_{GS} = 0V, T_C = +125^\circ\text{C}$	-	-	1000	μA	
On-State Drain Current (Note 2) IRFD310/311, IRFD310R/311R IRFD312/313, IRFD312R/313R	$I_D(ON)$	$V_{DS} > I_D(ON) \times r_{DS(ON) \text{ Max}}, V_{GS} = 10V$	0.4	-	-	A	
			0.3	-	-	A	
Static Drain-Source On-State Resistance (Note 2) IRFD310/311, IRFD310R/311R IRFD312/313, IRFD312R/313R	$r_{DS(ON)}$	$V_{GS} = 10V, I_D = 0.2A$	-	3.3	3.6	Ω	
			-	3.6	5.0	Ω	
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_D(ON) \times r_{DS(ON) \text{ Max}}, I_D = 0.2A$	0.5	1.2	-	S(V)	
Input Capacitance	C_{ISS}	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$	-	135	-	pF	
Output Capacitance	C_{OSS}	See Figure 10	-	35	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	8.0	-	pF	
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \approx 0.5BV_{DSS}, I_D = 0.4A, R_G = 9.1\Omega$ See Figure 17. (MOSFET switching times are essentially independent of operating temperature)	-	3.0	10	ns	
Rise Time	t_r		-	10	20	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	5.0	10	ns	
Fall Time	t_f		-	8.0	15	ns	
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g		$V_{GS} = 10V, I_D = 0.4A, V_{DS} = 0.8 \text{ Max Rating}$. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	6.0	7.5	nC
Gate-Source Charge	Q_{gs}		-	3.0	-	nC	
Gate-Drain ("Miller") Charge	Q_{gd}		-	3.0	-	nC	
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die.		-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.		-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	120	$^\circ\text{C/W}$	

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	0.4	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	1.6	A
Diode Forward Voltage (Note 2)	V_{SD}	$T_J = +25^\circ\text{C}, I_S = 1.6A, V_{GS} = 0V$	-	-	1.6	V
Reverse Recovery Time	t_{rr}	$T_J = +150^\circ\text{C}, I_F = 1.6A, dI_F/dt = 100A/\mu s$	-	380	-	ns
Reverse Recovered Charge	Q_{RR}	$T_J = +150^\circ\text{C}, I_F = 1.6A, dI_F/dt = 100A/\mu s$	-	2.7	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES:

- $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$
- Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
- Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
- $V_{DD} = 40V$, starting $T_J = +25^\circ\text{C}$, $L = 44.89\text{mH}$, $R_{GS} = 50\Omega$, $I_{PEAK} = 1.4A$. (See Figure 15.)

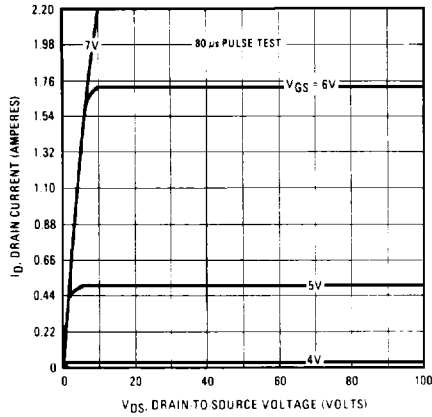


Fig. 1 — Typical Output Characteristics

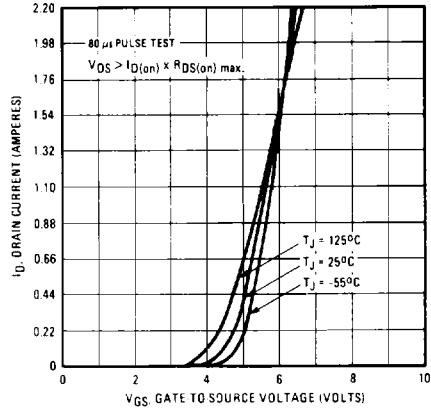


Fig. 2 — Typical Transfer Characteristics

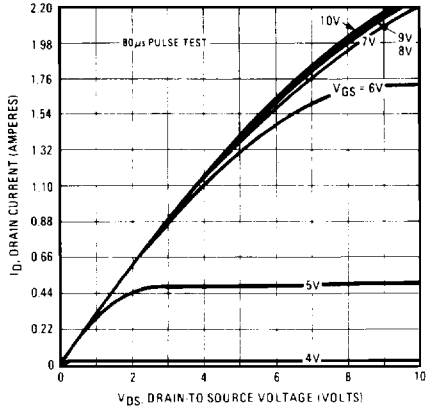


Fig. 3 — Typical Saturation Characteristics

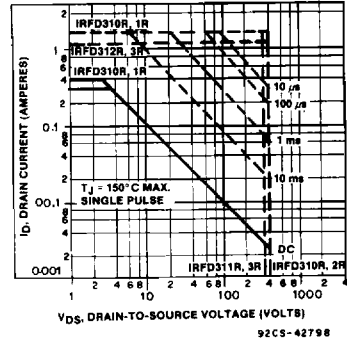


Fig. 4 — Maximum Safe Operating Area

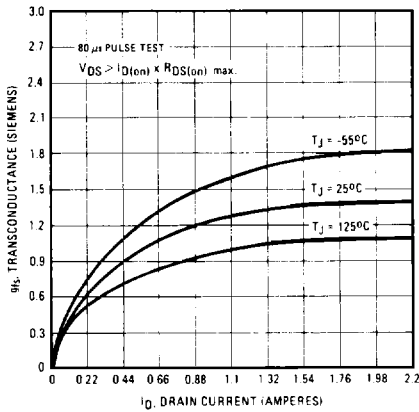


Fig. 5 — Typical Transconductance Vs. Drain Current

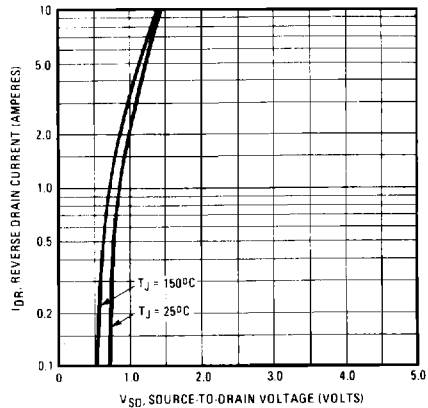


Fig. 6 — Typical Source-Drain Diode Forward Voltage

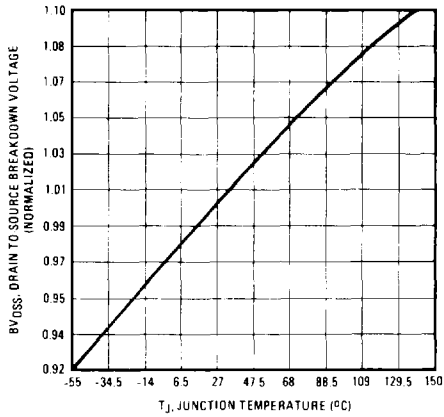


Fig. 7 — Breakdown Voltage Vs. Temperature

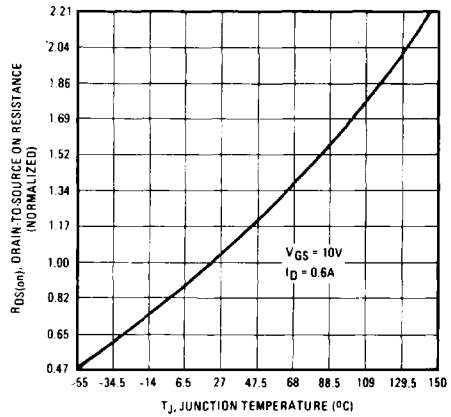


Fig. 8 — Normalized On-Resistance Vs. Temperature

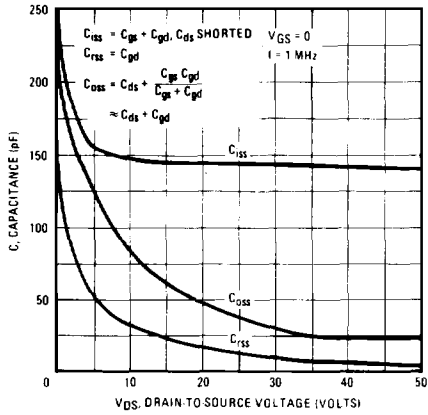


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

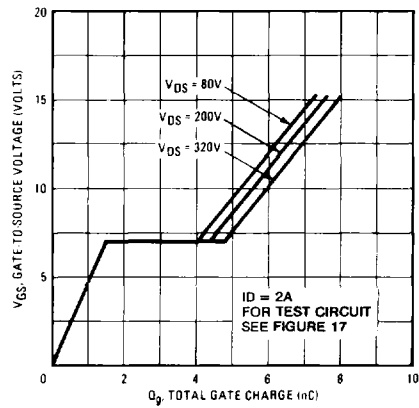


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

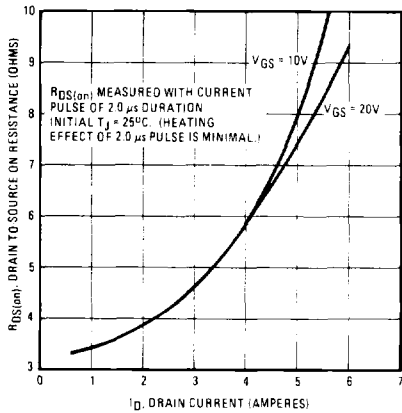


Fig. 11 — Typical On-Resistance Vs. Drain Current

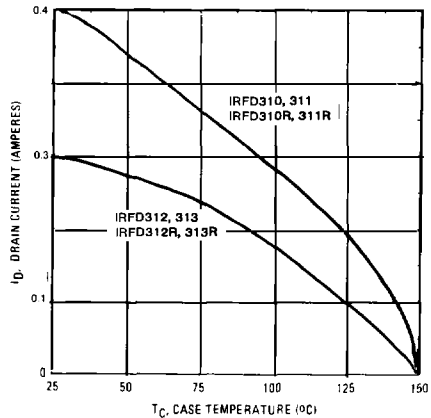


Fig. 12 — Maximum Drain Current Vs. Case Temperature

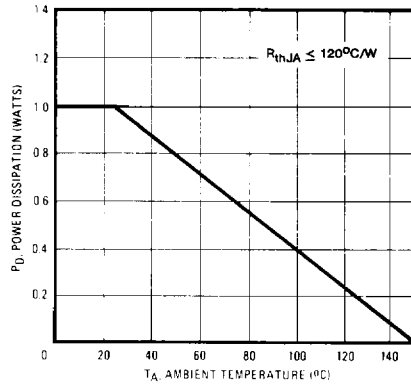


Fig. 13 - Power Vs. Temperature Derating Curve

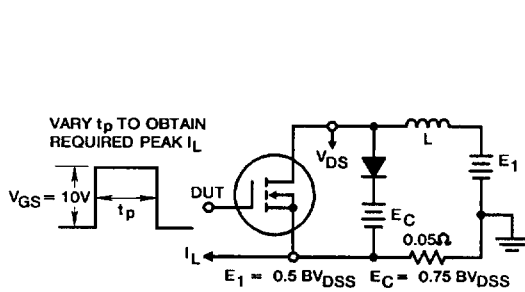


Fig. 14a - Clamped Inductive Test Circuit

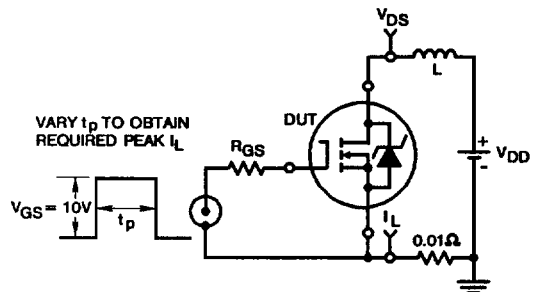


Fig. 15a - Unclamped Energy Test Circuit

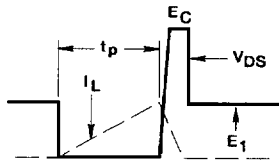


Fig. 14b - Clamped Inductive Waveforms

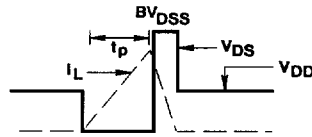


Fig. 15b - Unclamped Energy Waveforms

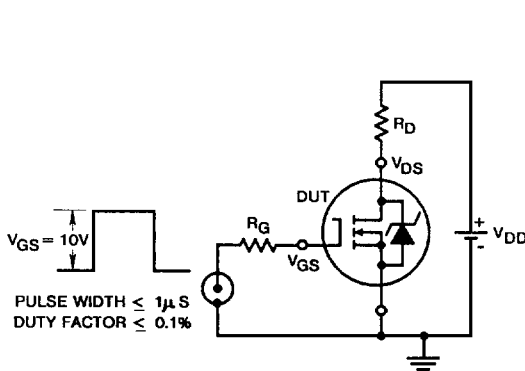


Fig. 16 - Switching Time Test Circuit

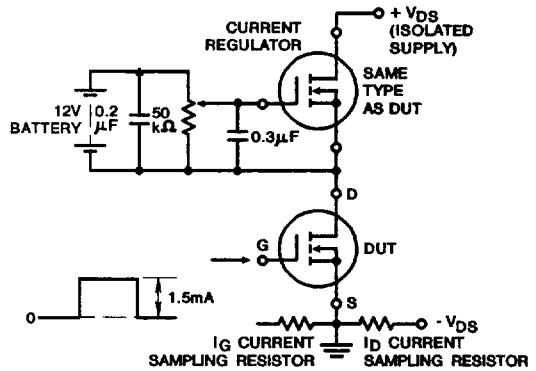


Fig. 17 - Gate Charge Test Circuit