Integrated Device Technology, Inc.

256K (64K x 4-BIT) CMOS STATIC RAM PLASTIC SIP MODULE

IDT 7MP456

FEATURES:

- High-density 256K (64K x 4) CMOS static RAM module
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Available in 28-pin SIP (single in-line package) for maximum space saving
- Fast access times: 25ns (max.) over commercial temperature
- Low power consumption
  - —Dynamic: less than 1.2W (typ.)
  - —Full standby: less than 30 mW(typ.)
- Utilizes IDT7187 high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

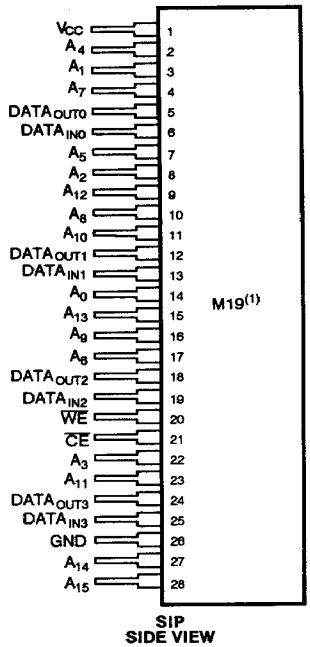
The IDT7MP456 is a 256K (64K x 4-bit) high-speed static RAM module constructed on an epoxy laminate surface using four IDT7187 64K x 1 static RAMs in plastic surface mount packages. Extremely fast speeds can be achieved with this technique due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology .

The 7MP family of surface mounted SIP technology is a cost-effective solution allowing for very high packing density. The IDT7MP456 is offered in a 28-pin SIP. The IDT7MP456 can be mounted on 200 mil centers, yielding 1.25 megabits of memory in less than 3 square inches of board space.

The IDT7MP456 is available with maximum access times as fast as 25ns, with maximum power consumption of 3.3 watts. The module also offers a full standby mode of 440mW(max.).

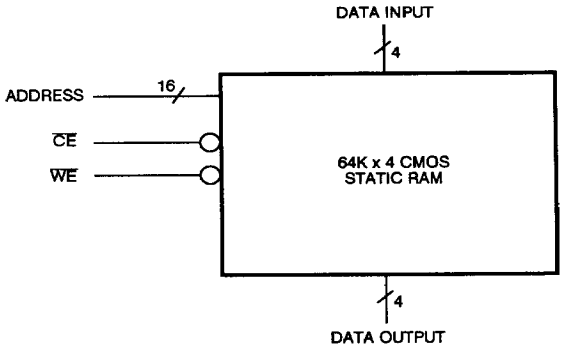
All inputs and outputs of the IDTMP456 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

PIN CONFIGURATION



SIP
SIDE VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{15}	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
D_{IN_0} - D_{IN_3}	Data Input
D_{OUT_0} - D_{OUT_3}	Data Output
V_{CC}	Power
GND	Ground

NOTE:

1. For module dimensions, please refer to module drawing M19 in the packaging section.

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS V_{CC}= 5.0V ±10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MP456 MIN.	TYP.(1)	MAX.(2)	MAX.(3)	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	–	–	15	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	15	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open F = 0	–	180	360	480	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open f = f_{MAX}	–	240	440	600	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or (TTL Level) V_{CC} = Max. Output Open	–	90	180	240	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{HC}, V_{IN} ≥ V_{HC} or ≤ V_{LC} V_{CC} = Max., Output Open	–	6	60	80	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	–	–	V

NOTES:

1. V_{CC} = 5V, t_{AA} = 25°C
2. t_{AA} = 35, 45, 55ns
3. t_{AA} = 25, 30ns

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

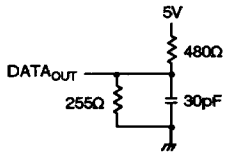

Figure 1. Output Load

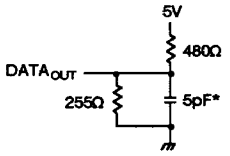

Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7MP456S25 MIN.	MAX.	IDT7MP456S30 MIN.	MAX.	IDT7MP456S35 MIN.	MAX.	IDT7MP456S45 MIN.	MAX.	IDT7MP456S55 MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	25	–	30	–	35	–	45	–	55	ns
$t_{CLZ1,2}$ (1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ} (1)	Chip Select to Output in High Z	–	20	–	25	–	30	–	35	–	40	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns
t_{PU} (1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{PD} (1)	Chip Deselect to Power Down Time	–	25	–	30	–	35	–	45	–	55	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	55	–	ns
t_{CW}	Chip Selection to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AW}	Address Valid to End of Write	25	–	25	–	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	25	–	35	–	45	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ} (1)	Write Enable to Output in High Z	–	20	–	25	–	25	–	30	–	30	ns
t_{DW}	Data to Write Time Overlap	15	–	20	–	20	–	25	–	25	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	5	–	ns
t_{OW} (1)	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	ns

NOTE:
1. This parameter guaranteed but not tested.

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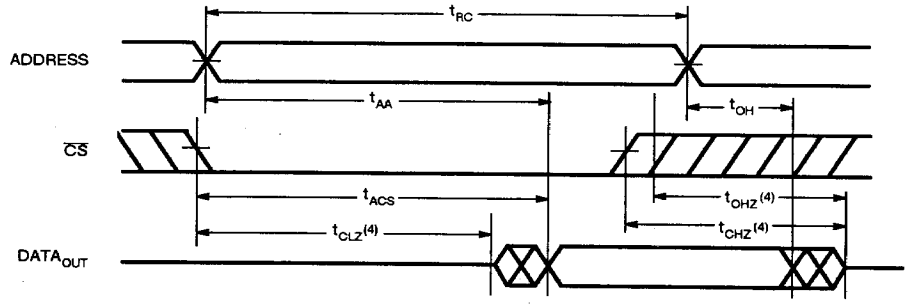
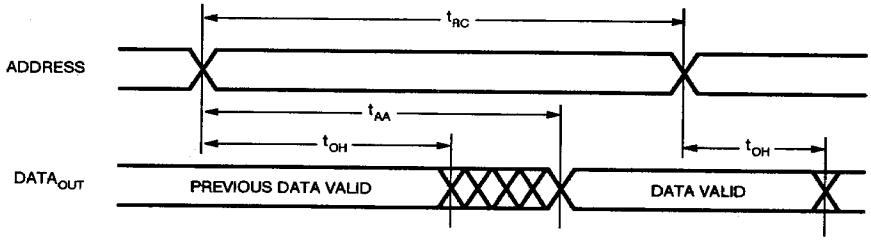
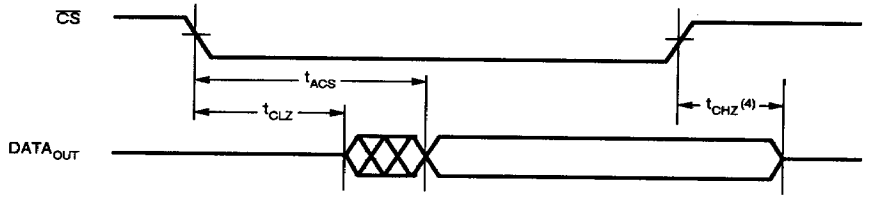
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 3)



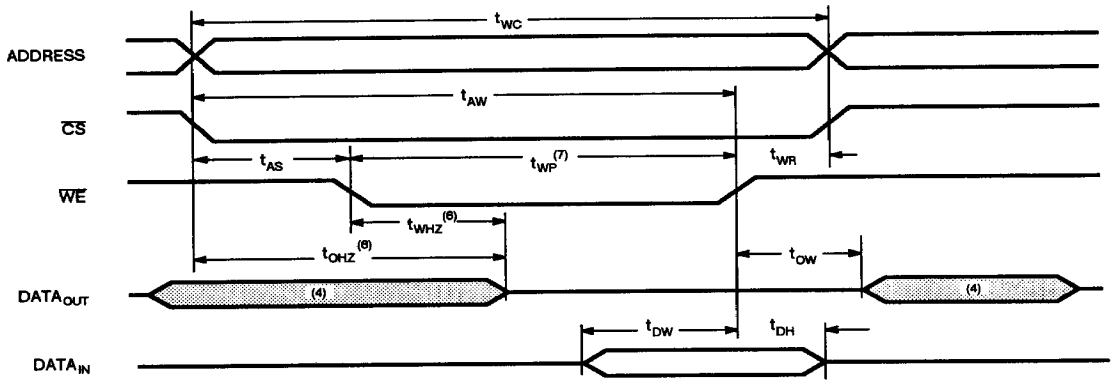
TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3)



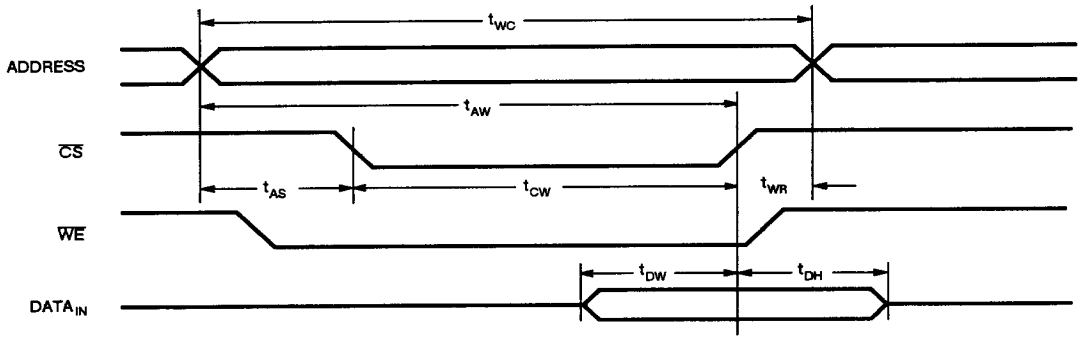
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} .
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



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NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION