CYPRESS SEMICONDUCTOR

64K x 18 and 128K x 18 Synchronous Pipelined Cache R/W RAM

Features

- **Supports 200-MHz cache systems**
- **64K by 18 (7B1051) and 128K by 18 (7B1061) common I/O**
- **BiCMOS for optimum speed/power**
- **3-ns access delay (clock to output)**
- **5-ns cycle time (input to output)**
- **3.3V power supply**
- **3.3V GTL-capable I/O logic levels**
- **Write-through and byte-write capability**
- **Synchronous self-timed write**
- **Direct interface with the processor**
- **Two complementary synchronous chip enables**
- **Asynchronous output enable option**

Functional Description

The CY7B1051 and CY7B1061 are 3.3V devices with the 5-ns t_{CYC} and 3-ns t_{CO} needed to run at 200-MHz clock speeds. Since Pentium™ (P5) and the new RISC processors have 64-bit and wider data buses with ECC and parity, x9, x18, and x36 wide parts will be necessary to trade off between cache depth and width to satisfy both low-end and high-end systems (see the and CY7B1055/65 datasheet). The I/O

is designed for GTL-capable signal swings to achieve maximum speed with minimal noise. C_{IN} on all inputs except DQ is 5 pF max. and $DQ_0 - DQ_{17}$ is 7 pF to provide less loading on the processor outputs. A pipelined architecture is implemented by placing registers at both the data inputs and data outputs of the device. The advantage of this architecture is that it allows the designer to minimize the cycle time for the device by equalizing the delays through each segment of the pipeline. The devices are completely synchronous, therefore all the registers in the CY7B1051 and CY7B1061 (including the address and control registers) operate off the same clock. A consequence of these features is a one-clock latency between address and data. In other words, when an address is registered at a clock rise, the data corresponding to that address will be delivered to the data outputs following the next rising edge of the clock. Also, the control signals (write enable, output enable, and chip enable) follow a similar pipelined path to insure that the proper control accompanies the appropriate access. The write operations are greatly simplified by the self-timed write mechanism. An asynchronous output enable ($\overline{OE}$) option is available as well as a

control pin to disable the output register to allow for flow-through operation where latency needs to be avoided. The CY7B1051 and CY7B1061 are packaged in 100-pin PBGAs (plastic ball grid array) and PGAs.

Pipelined SRAMs have architectures such that the propagation delays through the device are divided by a technique of registering information at intermediate states with a common clock signal. In this manner, each of the processes may be done concurrently. In a pipelined SRAM, the registers are inserted in two locations, between the address/control/data inputs and the memory cell and also between the memory cells and the data outputs. In this arrangement, the address, control, and data in (in case of a write) of the current access are clocked into the RAM while the data from the previous access is clocked out to the I/O pins. A write pass-through mode is included. In this mode, when chip enable ($\overline{CE}$) is deasserted while write ($\overline{WE}$) is asserted, the values registered at the data inputs are routed around the core to the output registers and presented at the data output pins on the next clock. This mode requires that the $\overline{OE}$ pin be asserted during the same cycle that the write is asserted.

Logic Block Diagram

1051-1
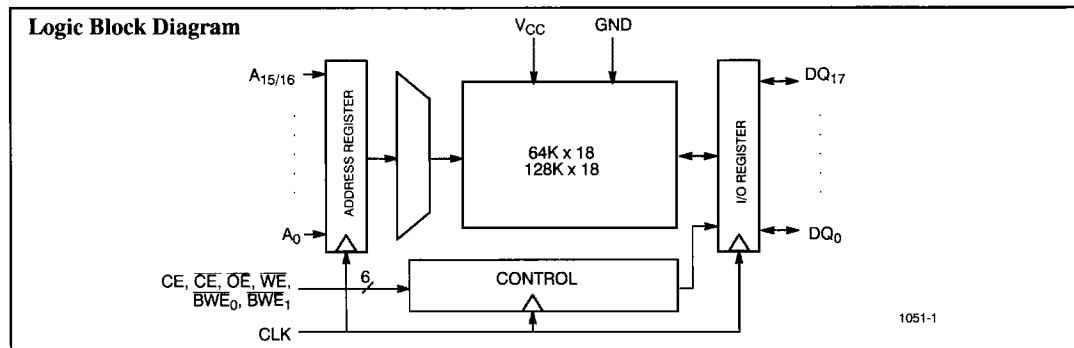
Selection Guide

		7B1051−5 7B1061−5	7B1051−7 7B1061−7
Maximum Cycle Time (ns)		5	7
Maximum Operating Current (mA)	Commercial	TBD	TBD
	Military		TBD

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