Features

- **SVGA Resolution, Active CMOS Imager Sensor for Highest Quality Images**
- **CIF-sized Sub-sample Mode for Easy Video Conferencing**
- **Stand-alone Operation – Need Only to Supply One 26.6MHz Clock**
- **Ultra-low Fixed Pattern Noise**
- **Triple 10-bit ADCs and Column-based CDS for Highest Readout Speed**
- **High Fill Factor and Sensitivity without Microlens Distortions**
- **Full 10-bit Data Width Digital Interface for Simple, Fast Transfer**
- **Easy Register-based Programming of Modes**
- **Region of Interest Image Scan Control for Digital Zoom and Metering**
- **On-board Color Offset and Gain Control**
- **Option for Full Timing and Scan Control through External FPGA**
- **Direct Interface to 8- or 16-bit-based Microprocessor Bus**
- **Full Power Control – Low-power Viewfinder Mode**
- **Internal Timing Mode Only Covered in this Datasheet**

Description

The Atmel AT76C401 is a complete imager system on one IC that has been designed to give high-quality images using an easy interface and simple operation to reduce overall system cost and time-to-market.

The core is a pixel array of 1281 x 480 rectangular active pixels with a high physical fill factor of 43% (without micro-lenses). A vertical stripe RGB pastel color filter is used with individual column-correlated double-sampling (CDS) correction circuitry to produce an exceptionally low level of fixed-pattern image noise (FPN). Individual color gain and offset controls followed by a triple 10-bit analog-to-digital converter further ensure an even color response in the digitized images.

All timing and voltages are generated internally from a single 3.3V voltage rail and master clock, but the option is available to take control of every aspect of scan timing externally in an FPGA if the user requires the modes of operation extended for advanced imaging.

Pre-programmed modes are available for full-resolution still- and motion-imaging with exposures of 1 µs to 1 second, as well as for a sub-sampled CIF-sized image suitable for the quality and data rates required for video conferencing.

Region of Interest mode additionally allows the user to define on a frame-by-frame basis the area of the imager to be read, enabling easy digital zone or complex multi-spot metering routines utilizing an external FPGA.

The interface resembles a standard microprocessor bus with a 4-bit address bus and the full image data width of 10 bits operating in a slave mode. When a local processor is not available, the device will stream data in a host mode out to a parallel interface with minimal flow control.

Dual-mode CMOS Integrated Imager

AT76C401

Preliminary

Rev. 1174A–03/00

Pin Configuration

Figure 1. AT76C401 Pinout (Top View)

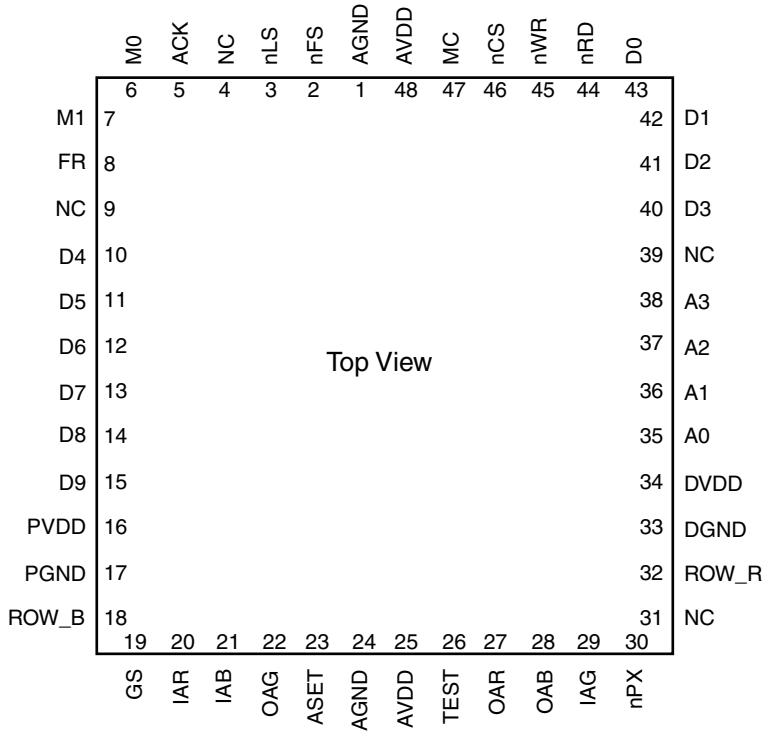


Table 1. Pin Description

Pin Number	ID Name	Full Name	Description
1, 48	AGND, AVDD	Analog Ground and Power	Supply rail for pixel array and CDS block.
2	nFS	Not Frame Sync	Falling edge indicates last row in Frame Read Out.
3	nLS	Not Line Sync	Falling edge indicates last pixel in Row Read Out.
4	NC	No Connect	See auxiliary datasheet, “External Timing Mode”.
5	ACK	Acknowledge	Rising edge signals Internal State Machines finished last operation.
6, 7	M0, M1	Mode 0, Mode1	Mode control between internal and external timing modes.
8	FR	Frame Reset	Reset read out counter and pixel array.
9, 31, 39	NC	No Connect	See auxiliary datasheet, “External Timing Mode”.
16, 17	PVDD, PGND	Pad V_{DD} and Ground	Digital supply (AC supply).
18	ROW_B	Row Blanking	Triggers internal reset and processing of complete row of pixels.
19	GS	Global Set	Global Reset Control. Returns all registers and counters to default values.
20, 29, 21	IAR, IAG, IAB	Analog Input RGB	Switchable input to A/D converters (or pin can be left NC).

Table 1. Pin Description (Continued)

Pin Number	ID Name	Full Name	Description
27, 22, 28	OAR, OAG, OAB	Analog Output RGB	Switchable output from gain and offset stage (or pin can be left NC).
24, 25	AGND, AVDD	Analog Power and Ground	Supply rail for all analog sections.
26	Test	VPIX	Test pixel voltage (or pin can be left NC).
23	ASET	Analog Set	Current reference bias via external resistor.
30	nPX	Not Pixel clock	Imager pixel data valid on falling edge.
32	ROW_R	Row Read	Triggers the readout of the complete row of pixel data onto the data bus.
33, 34	DGND, DVDD	Digital Ground and Power	Supply rail for digital core section (DC supply).
35, 36, 37, 38	A0 - A3	Address Bus	Register address line.
43, 42, 41, 40, 10, 11, 12, 13, 14, 15	D0 - D9	Data Bus	Tristate data bus for read/write to registers and pixel data output.
44	nRD	Not Read	Falling edge reads addressed register to data bus.
45	nWR	Not Write	Falling edge writes data bus to addressed register.
46	nCS	Not Chip Select	Chip select for register read/write. Data enable during image readout. Triggers register to counter transfer on falling edge.
47	MC	Master Clock	26.6MHz (typ) clock. Provides synchronous clocking for all digital and data and control.

Block Diagram

Figure 2. Block Diagram of AT76C401

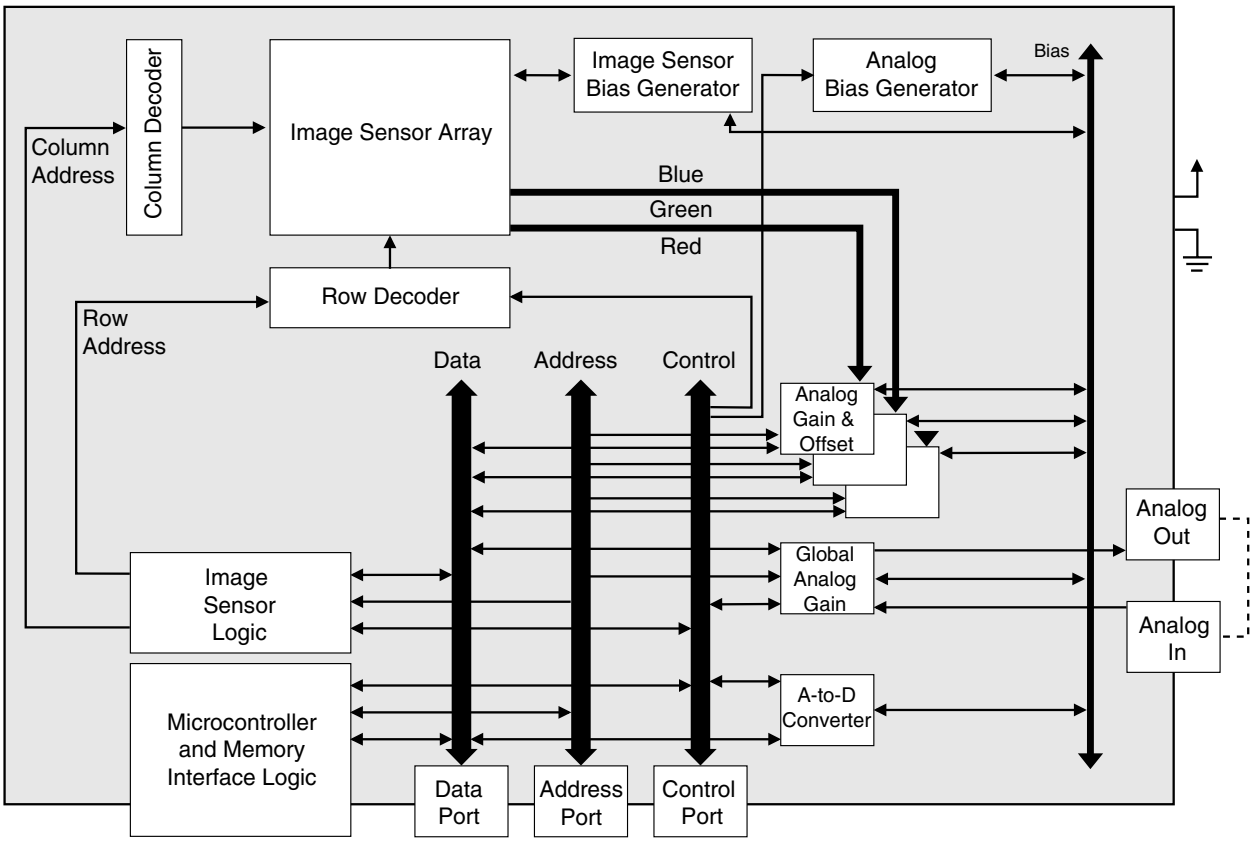


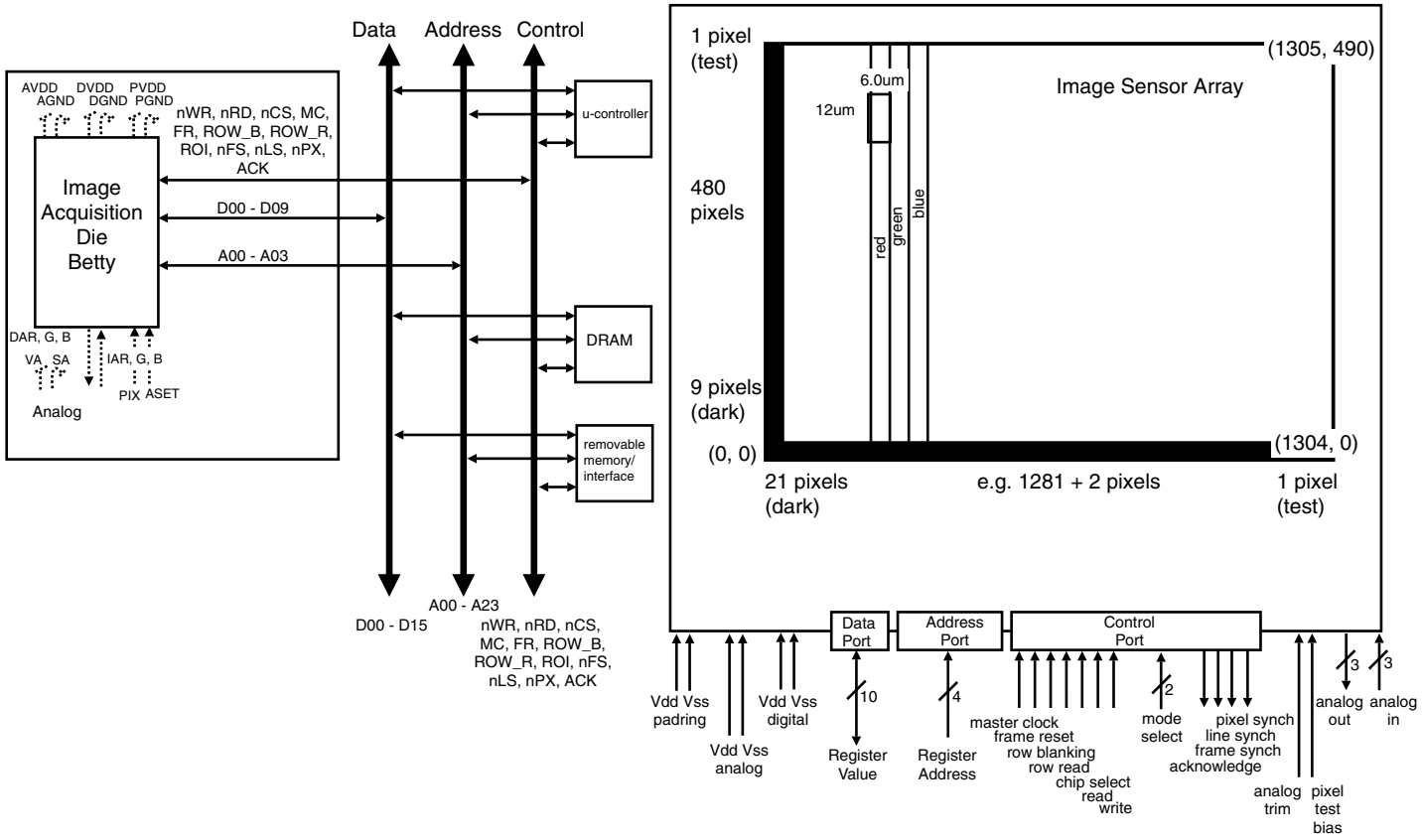
Table 2. Physical and Electrical Parameters

Parameter	Measurement	Units
Resolution	1281 x 480 or 320 x 120 sub-sampled	
Pixel Size	12 x 6	µm
Image Area	7.7 x 5.7	mm
Fill Factor	43	%
Max Col FPN	0.2	%
Dynamic Range	57	dB
Power Supply	3.3 ± 10%	V
Power Consumption	76	mW
Readout Rate	10	Mpixels/second
Frame Rate	16	
Sensitivity (Saturation)	20	µA/µx-sec.
Conversion Gain	1.05	nA/e-
Dark Current	0.3 @Room Temperature	nA/cm^2

Table 2. Physical and Electrical Parameters (Continued)

Parameter	Measurement	Units
Noise	130	e-
Saturation	100	uA
Peak Quantum Efficiency	21	%
Full Well Capacity	95000	e-
Programmable Gain Range	2x - 48x	

Figure 3. Image Format



Architectural Overview

Active Pixel Array

The pixel used is a three-transistor voltage mode photodiode design. To initialize the pixel, the reset transistor Trst (which is commoned with others across each row) is turned on, and the photodiode active area charges up to the Vrstbias line. When Trst is turned off to start the integration, the photodiode begins to discharge and the resulting voltage level is buffered by Tbuf through to the row select transistor Tsel. After integration is complete, transistor Tsel (also commoned with other Tsel across the row) is turned on, presenting the pixel voltage to the column readout bus.

Note that the photodiode will continue to integrate if still illuminated or until it is reset again by activating Trst in preparation for another exposure period.

See Figure 4, Figure 5, Figure 6 and Figure 7.

Figure 4.

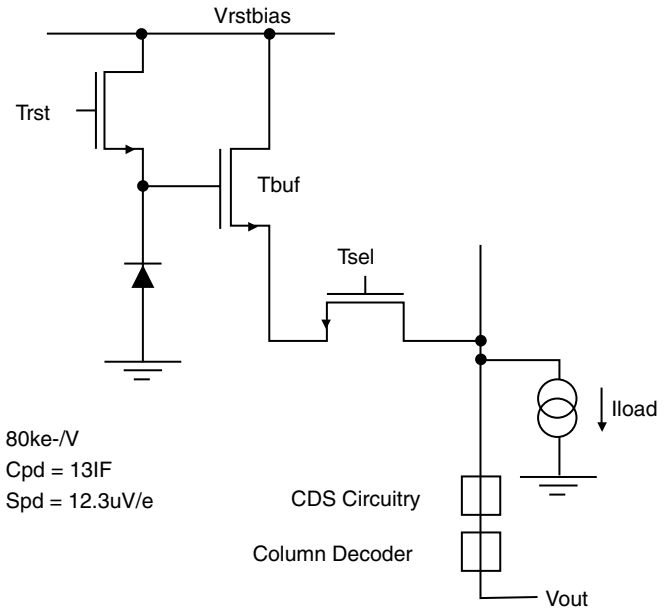


Figure 5.

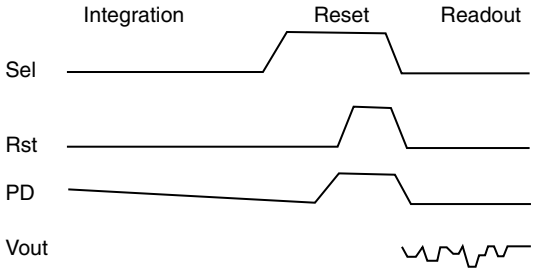


Figure 6.

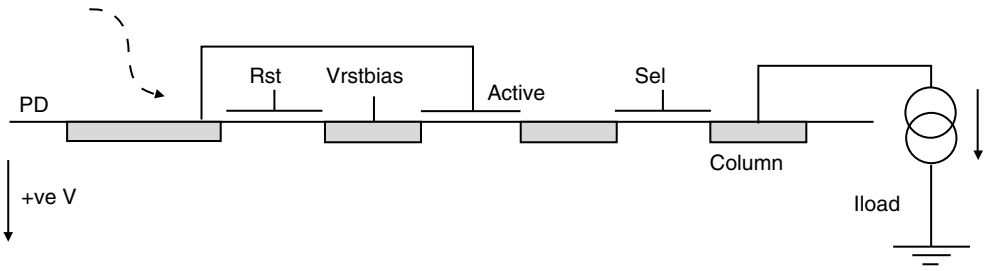
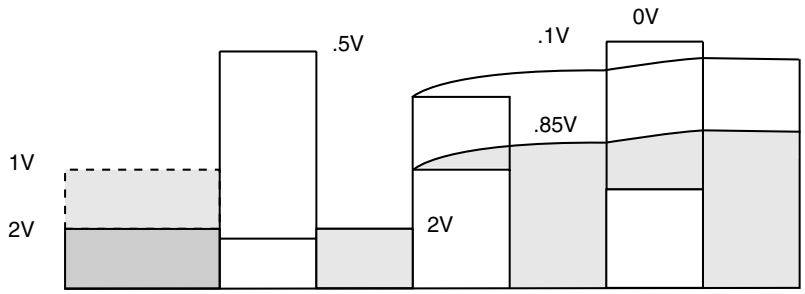


Figure 7.



Correlated Double Sampling

A CDS block is placed at the bottom of every pixel column bus. Using the timing generated from a small state machine (or from an external FPGA) the photodiode voltages from all the pixels in a row are applied in parallel to their CDS blocks, buffered, clamped and converted to a current. This is then stored in the first of two current memories within each block.

CDS is then performed by turning on Trst, resetting the pixel and storing the reset voltage (after buffering and conversion) in a second current memory.

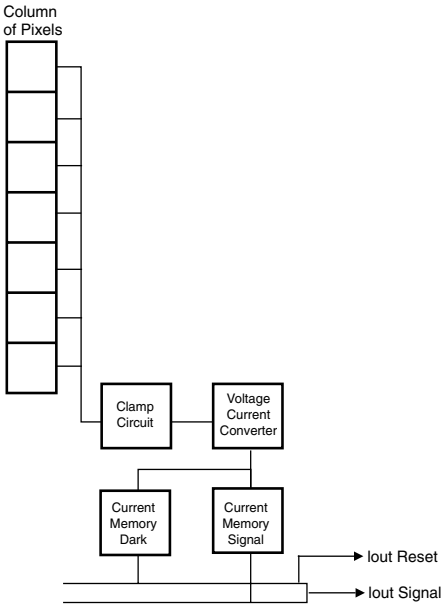
Finally, the reset and pixel values are passed out of the CDS block (still as a current value) onto one of the three color buses (Red, Green and Blue).

If however the CDS is turned off by writing to bit 8 of the Interface Logic register, the operation is reversed with the pixel reading being stored in the second memory location and a reference level equating to a fully saturated pixel written into the first location.

The difference of these values, which is passed for A to D conversion, therefore represents an inverse image (note: intensity-inverse rather than color-inverse).

When CDS is turned off, the pixel is NOT reset as part of the read cycle, enabling this mode to be used for continuous meter during the integration period.

Figure 8. Column Signal Processor Block Diagram



Gain and Offset

Individual gain and offset of output of the three buses is performed using current mode amplifiers under the control of DACs driven by the contents of six registers (5-10) in the Analog Logic (AL) register. A seventh register (11), through a single DAC, is used to control three additional amplifiers ganged together to perform global gain.

Analog Access Port

After gain and offset amplification, the three color buses are made available through ports OAR, OAG and OAB as current signals at a constant voltage for external processing as required, being reinserted into ports IAR, IAG and IAB.

It is not necessary (or desirable) to link the ports externally if this feature is not used, as the signal can be bridged internally under the control of bits 3 and 4 in the Interface Logic (INL) register.

10-bit Analog to Digital Converter

Following the internal or external loopback, the three color bus current signals are passed to three 10-bit, 10 MHz pipelined Analog-to-Digital converters which require 5 master clocks for each conversion. To allow settling time on the bus, however, overall each bus is converted at 3.3 Mpixels per second.

The results of these conversions are available in the Analog Processing (AP) register which is usually presented as full 10-bit width data onto the digital bus under internal or external handshake (see description of operation modes).

Power Control

Individual control over the main power-consuming blocks are provided in bits 0 to 2 of the Interface Logic (INL) control register. The bias generators, ADC converters and analog amplifiers can be turned off to conserve power in standby.

For low power operation, the master clock can also be reduced down to a minimum of 1 MHz.

Power consumption can further be optimized by reduction of the scan rate under internal control of the RowB and RowR inputs.

Row/Column Timing and Counters

At the core of the scanning circuits are two counters that are incremented to scan across the rows and up the columns. Under control of bit 9 in the Interface Logic register, these counters are incremented by one or by four between pixels or rows.

The start coordinate of the scan and the block size is written into the Interface Sensor Logic register by the user over the external bus. This information does not however become active until the control line nCS is strobed high by the user.

The leading edge of nCS causes the start coordinate to be loaded into the internal start register for the main counters and for the end coordinate to be calculated from the start coordinate and the block size, the result being loaded into a second internal stop register. The leading edge of nCS also causes the main counters to be reset to the contents of the internal start register.

As the counters are incremented, they are compared with the contents of the internal stop register to determine end of row and frame, triggering a reload to the contents of the internal start register. The user is not required to reload the region of interest registers for every scan of the imager, and anything that is loaded will not become active until nCS is strobed by the user.

Pulling global set high resets all the registers to their default and automatically triggers this calculation and thus the user is not required to strobe nCS manually.

Functional Description

Scan Control

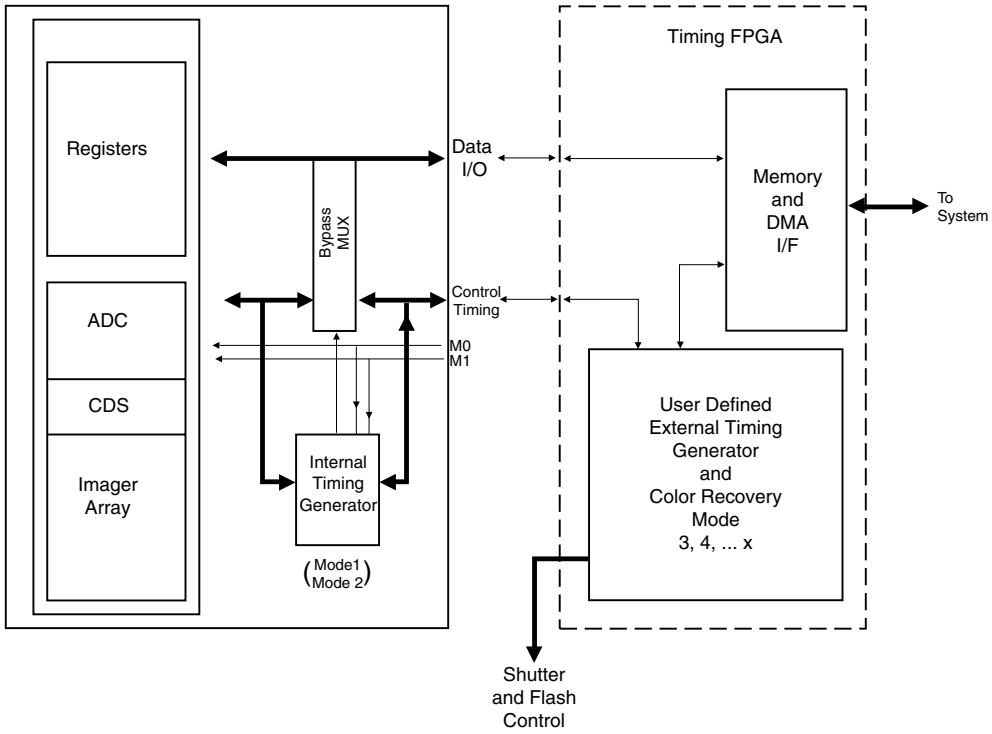
The Atmel Imager integrates all the functions required to capture, digitize and image. To allow maximum flexibility, the individual functions are register programmable and are accessible from a standard databus. The user can therefore control precisely the various function blocks to accomplish a customized operation or they can use the four automatic modes of operation most commonly used which are provided by a pre-programmed internal state machine. To use the internally controlled scan modes, only a subset of the total device pins are required and the others should be left unconnected.

If the user needs to control the imager completely, an external logic block (possibly in a PLD or FPGA) needs to be interfaced to the imager utilizing all the device pins. This block will then provide ALL the timing and control signals to the imager and the internal automatic mode state machines are bypassed.

The imager recognizes the two different timing modes by inspection of two control lines and uses an impossible state to force operation to internal timing. Pins M0 and M1 (also designated nPR and nPS in external control mode) have pull down resistors internal and will automatically force the device to internal timing if left unconnected or tied to 0v.

Only the timing information and pin designations for the internal timing modes are provided in this datasheet. An appendix is available on request containing the full timing diagrams and sample source code from the internal state engine blocks.

Figure 9. Camera System with Internal and External Timing



Internal Image Scan Modes

Single Still Frame

Still operation is achieved using an electronic half shutter and would usually be augmented by an external mechanical shutter for high speed exposures.

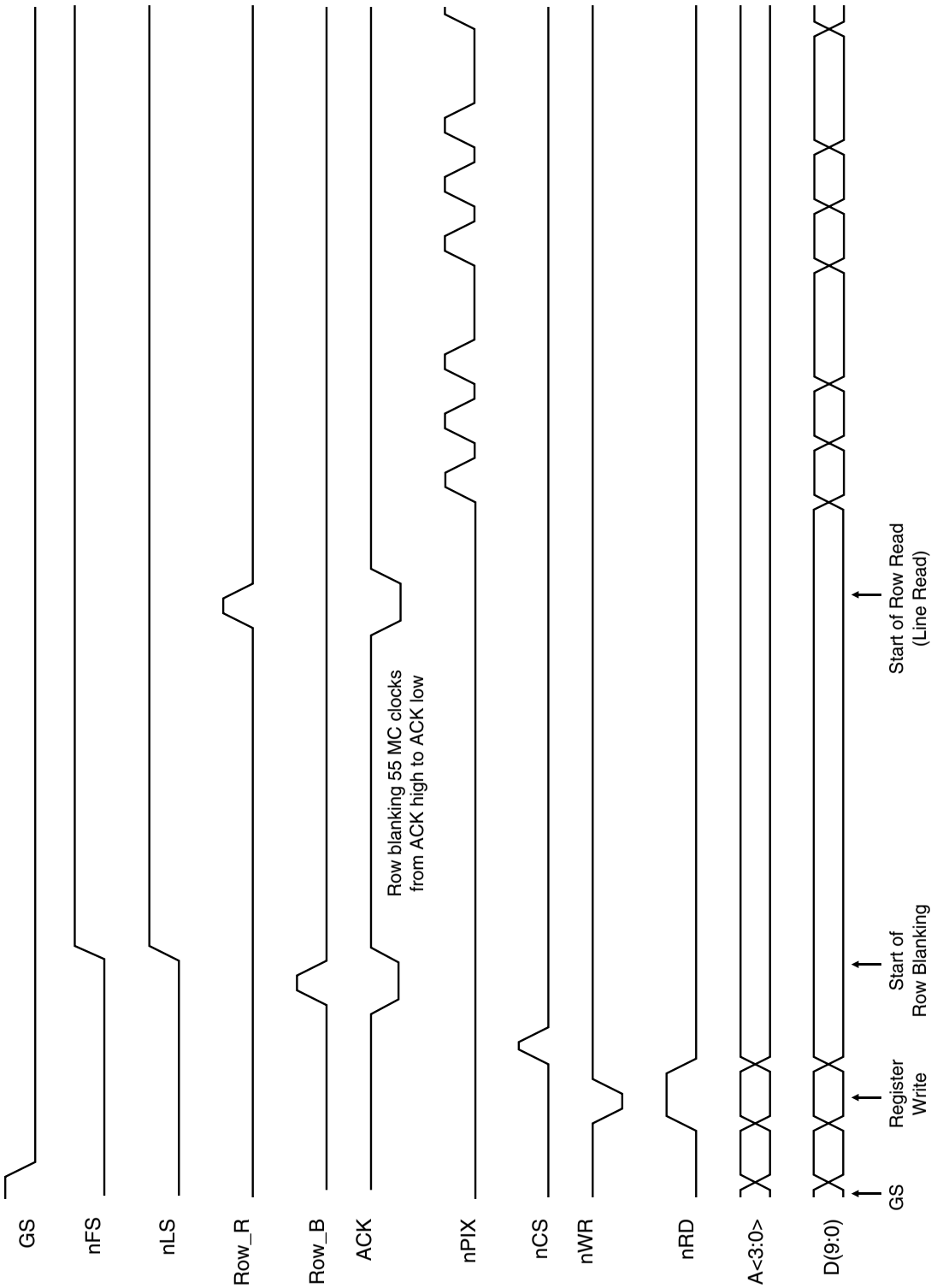
The Image Sensor Logic register is first set to 111111111 and the imager reset by strobing input FR (Frame Reset) high. The exposure time is determined under external control and can be as short as one ACK cycle or as long as the user requires.

After the exposure period (and possibly after the external shutter has been closed), the imager is read out on a line-by-line basis starting with the lower left hand corner of the area defined in the Image Sensor Logic (IL) register. Strobing the Row Blanking (RowB) high causes the imager to process a complete row of image through the CDS block (if activated through the MSB of Interface Logic (INL) register). When this cycle is complete the imager drops ACK low and is ready to stream data out. The user then lifts RoW-Read (RowR) high and the imager puts the data on the bus at a maximum rate of one pixel every two Master Clock (MC) cycles indicating good data on the falling edge of nPX. One half master clock cycle after the last falling edge of nPX for the last pixel in the row, the imager also drops nLS to indicate Line Sync. Strobing RowB again will cause the second row to be read out and so on. After the last line has been read out, the imager also drops nFS low coincident with nLS to indicate Frame Sync.

Although a mechnical shutter may be used to prevent direct exposure after reading of the image has begun, the pixels will continue to integrate dark current. The readout period once the shutter is closed should therefore be kept as short as possible in relation to the exposure time to avoid a brightness gradient down the picture. If this is not possible due to system or transmission channel constraints, then a simple algorithm can be implemented to correct for it.

The next frame exposure is started again by strobing Frame Reset (FR).

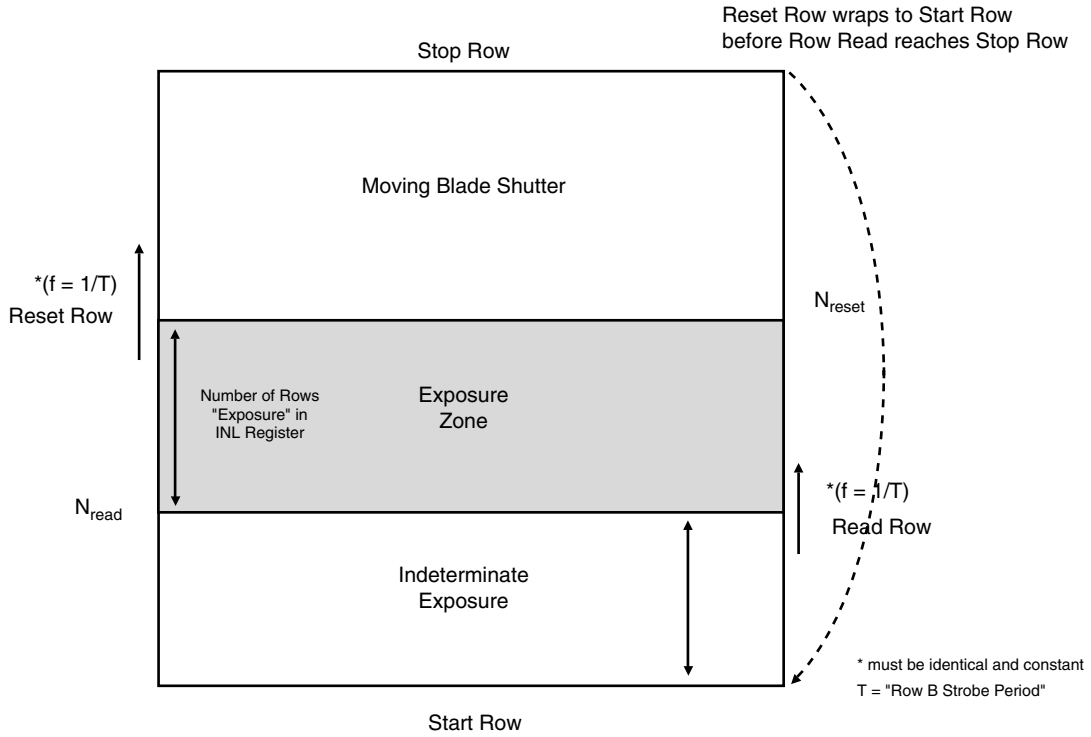
Figure 10. Row Blanking and Row Read - Exploded View of Start Pattern



Full Motion

For continuous image acquisition, exposure is controlled using a moving blade electronic shutter the width of which is written into the Image Sensor Logic (IL) register before a frame is exposed.

Figure 11. Moving Blade Shutter



A single frame is acquired by strobing Frame Reset (FR) to reset to the top of the frame. FR does not reset the full frame of pixels in this mode. After the reset operation is ACK'd, the user then moves the shutter across the imager by strobing RowB high for each row. This rate should be calculated such that the datastream produced by the imager does not exceed the maximum interface bandwidth and requires to be at a constant rate so that the exposure does not vary across the image.

The exposure can be calculated as:

$$\text{Exposure(ms)} = \text{Row B strobe period} \times \text{no. of rows in register INL}$$

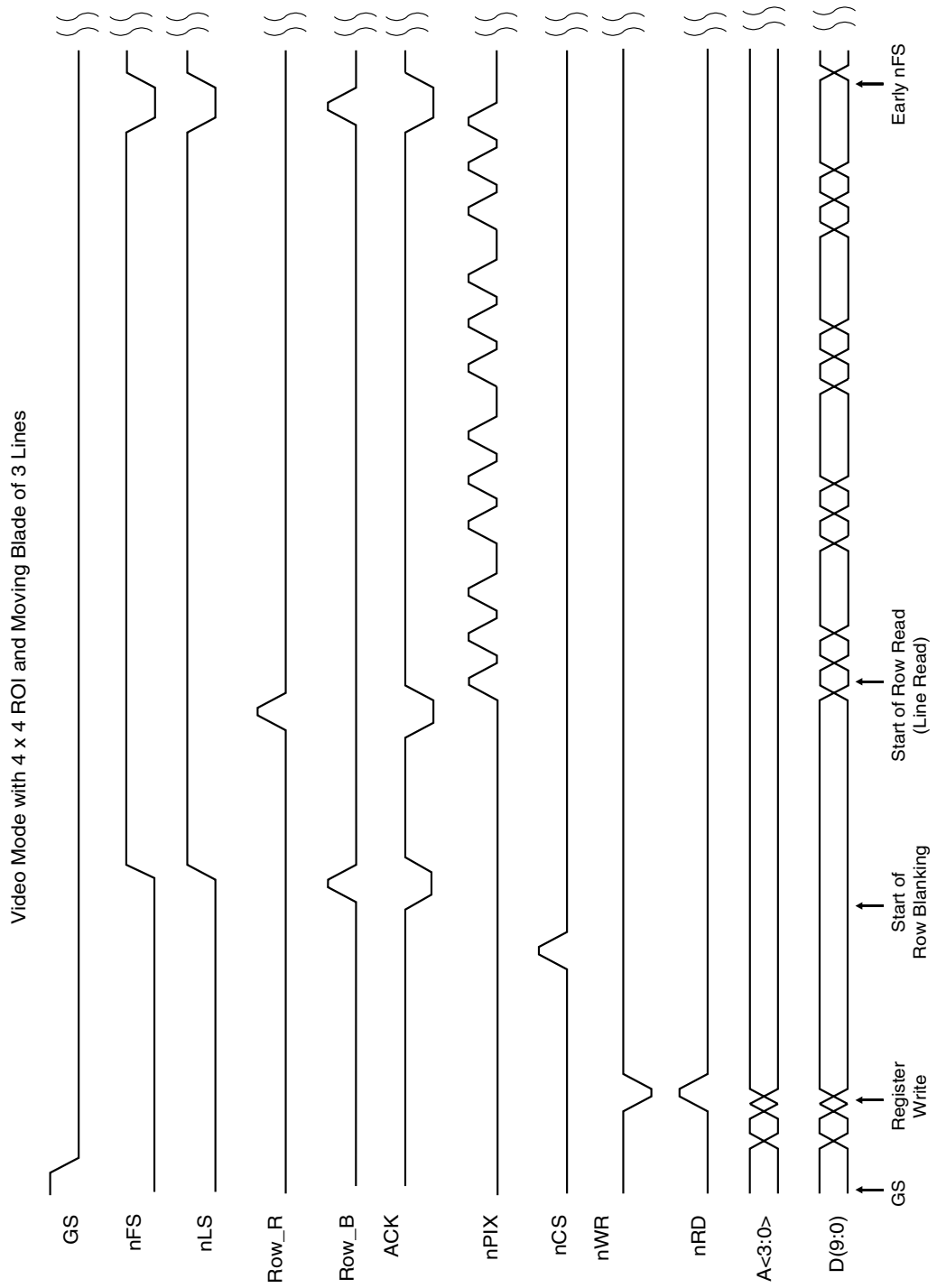
The data rate can be calculated as:

$$\text{Data Rate} = (1/\text{Row B strobe period}) \times 3 \times \text{'x' Block Size}$$

The exact interface bandwidth will most likely depend heavily upon how the 10-bit data is coded into bytes. Users requiring only 8-bit images may opt to drop the 2 LSBs.

For the first frame following a Frame Reset or nCS, valid data is not available until the programmed exposure period for the first line has been reached. During this period, the last n (where n is the number of lines of the exposure) lines of the imager are read out followed by the nFS line going low. As these lines will have been reset at an indeterminate time, the data obtained will be random. To establish the true start of the image, the user should flush the TX buffer following the first frame sync (nFS) and not attempt to count lines as the period will not be constant. The first frame of the image will thus appear to be much shorter/ smaller than the programmed region of interest being the width of the exposure.

Figure 12. Timing diagram showing short first frame



Subsequent frames of image will contain full valid data as the reset and read points will smoothly wrap around the imager.

After the latency determined by the exposure programmed into the exposure register (IL), real image data is available at the output. To receive the data, the user strobes RowR after RowB is acknowledged for each row and latches the data on the falling edge of nPX. The user MUST strobe RowR early enough so that the last pixel in the row is output before the next RowB strobe is applied to avoid the data being curtailed. However, unless the imager is being run at maximum speed, this is unlikely to pose a problem.

Figure 13. Timing Diagram showing short first frame (continued)

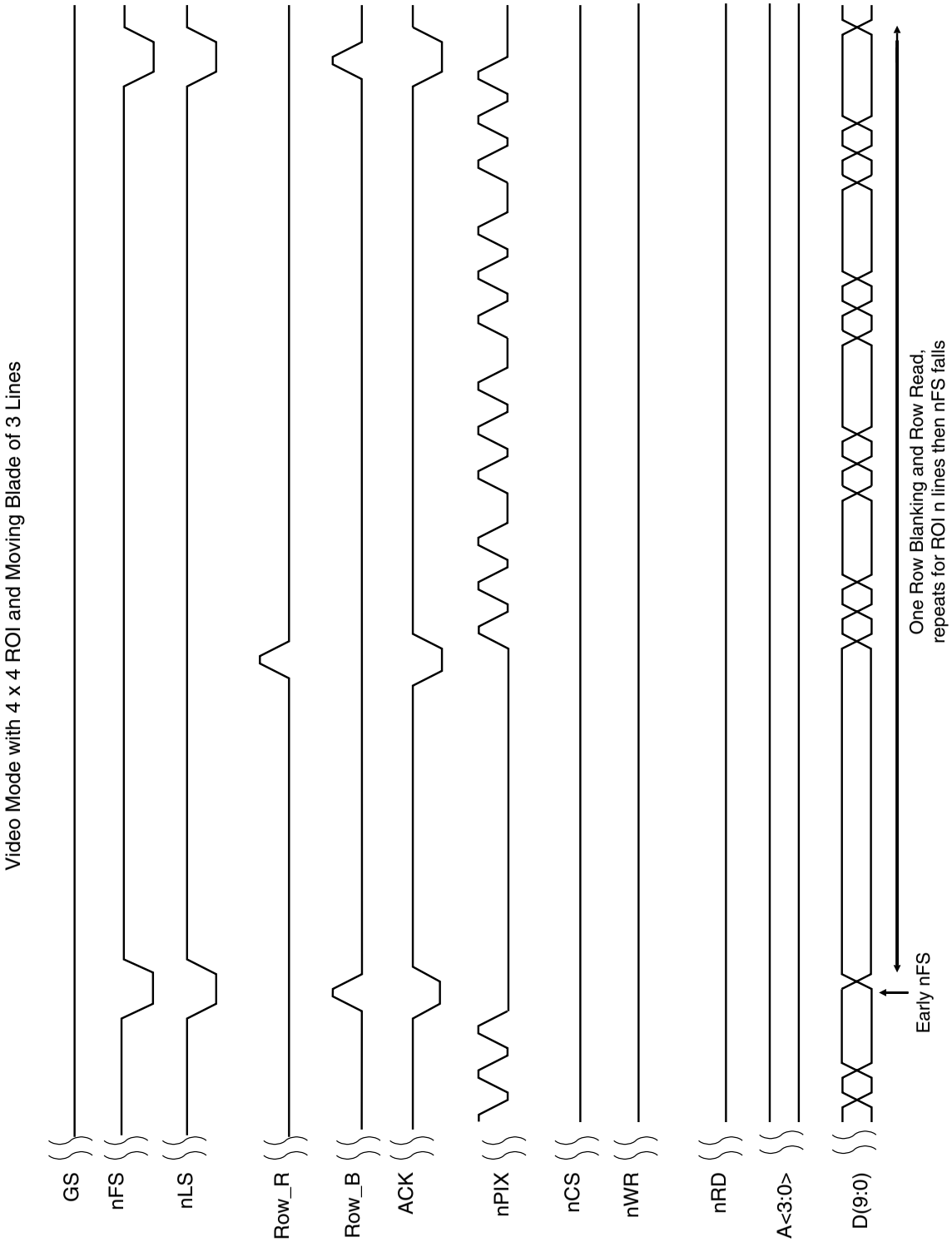


Figure 14. Correct Placement of Row Blanking Strobe

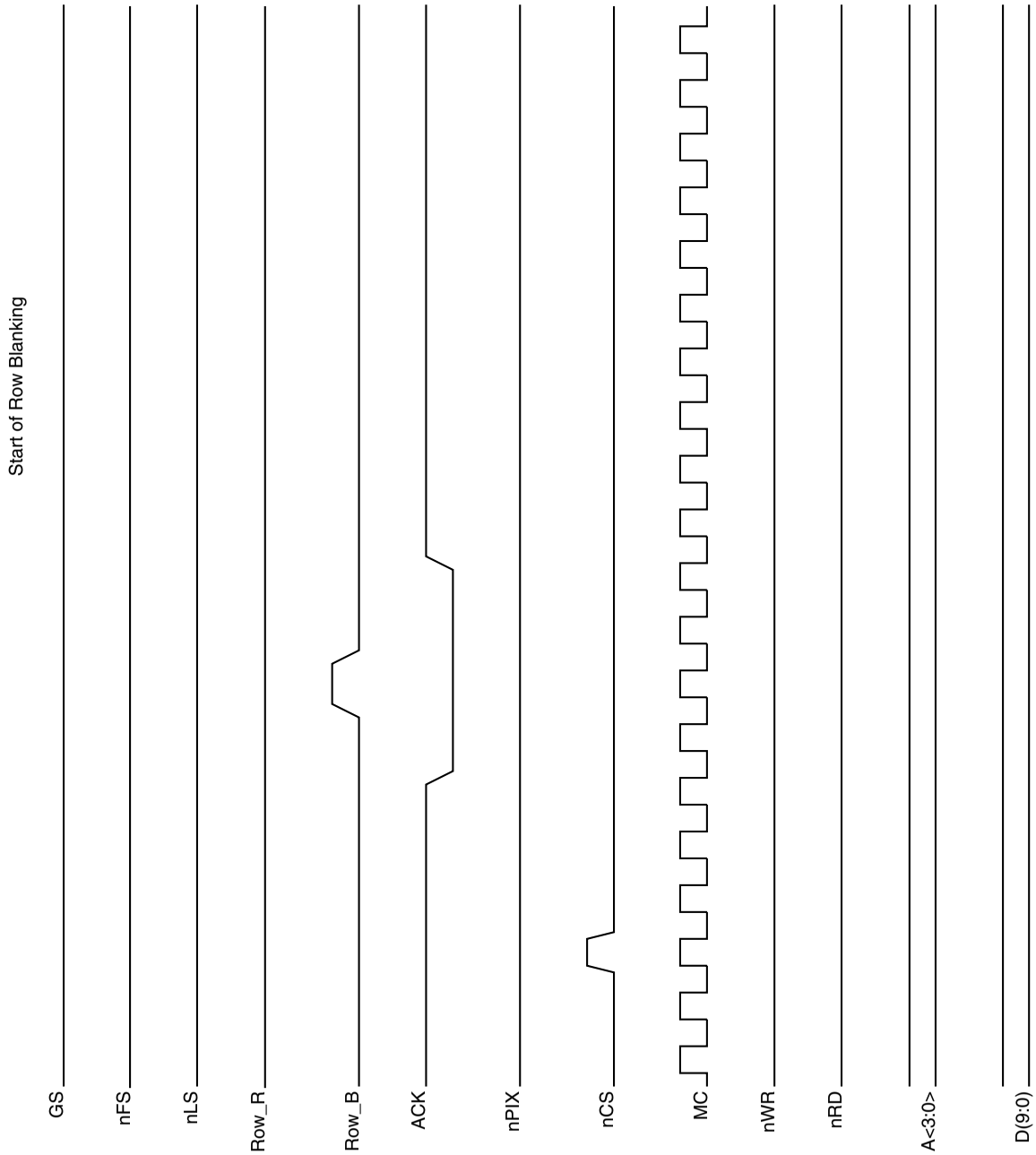


Figure 15. Correct Placement of Row Read Strobe

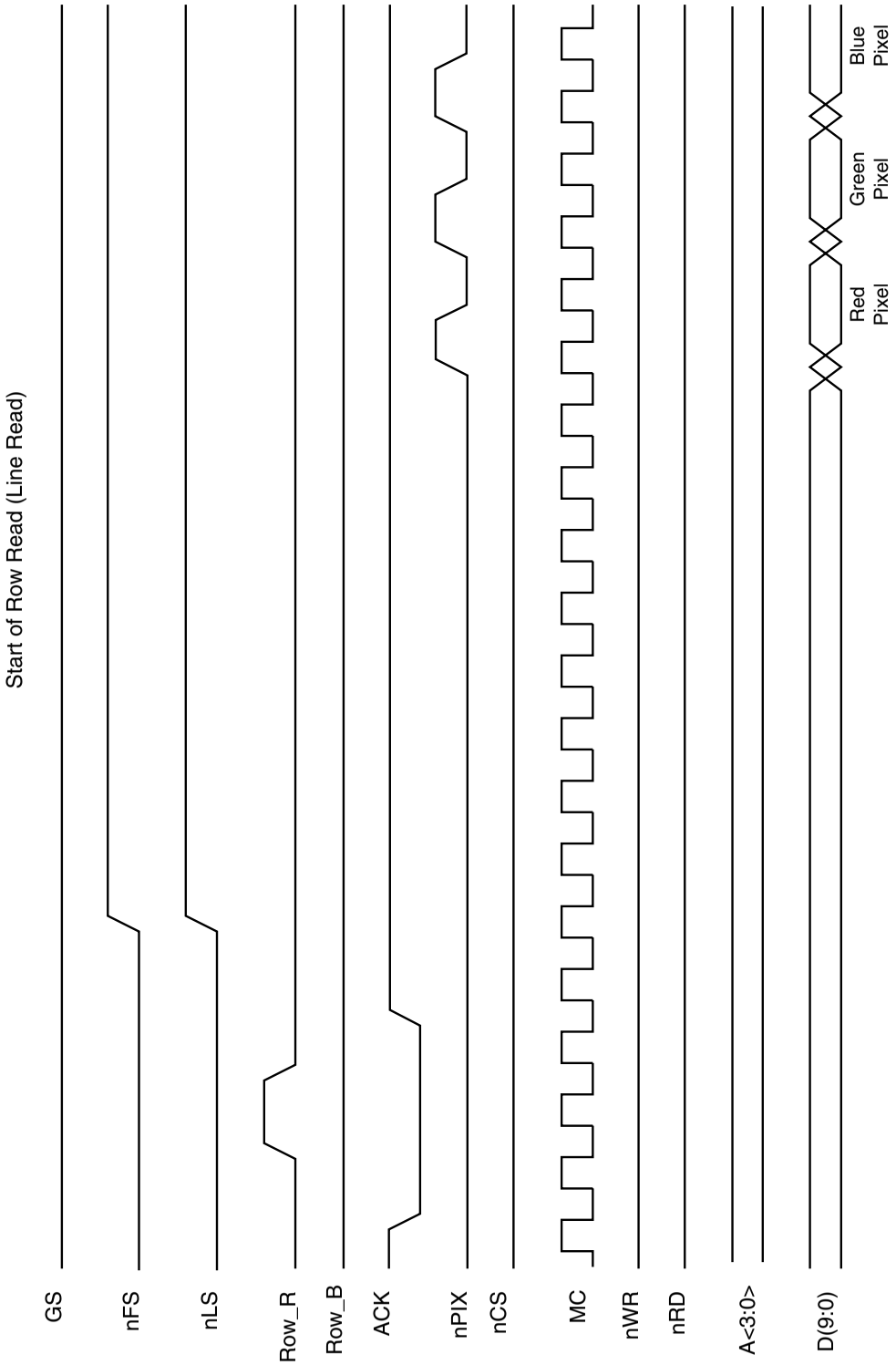


Figure 16. Timing showing End of Row Read

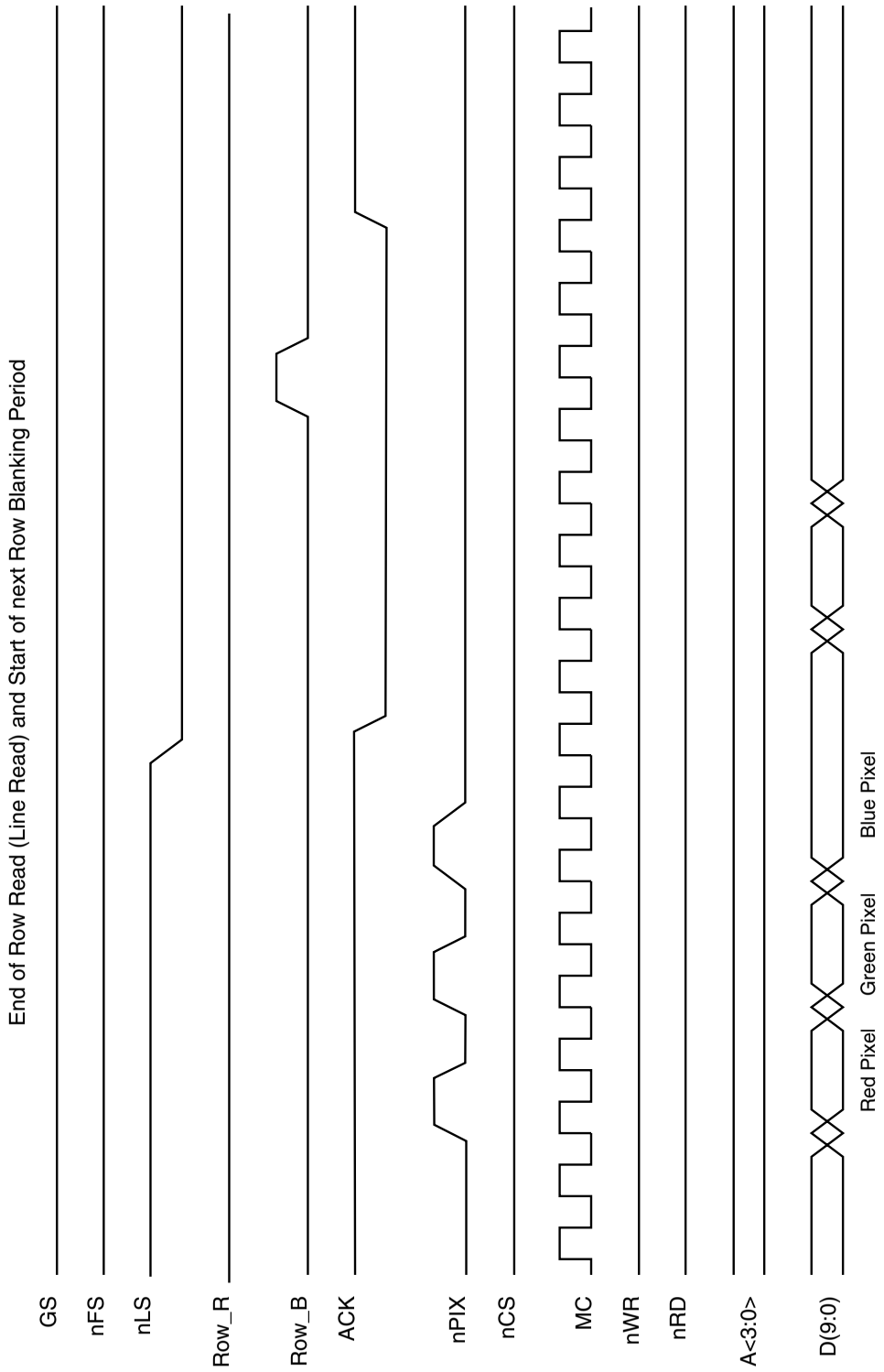
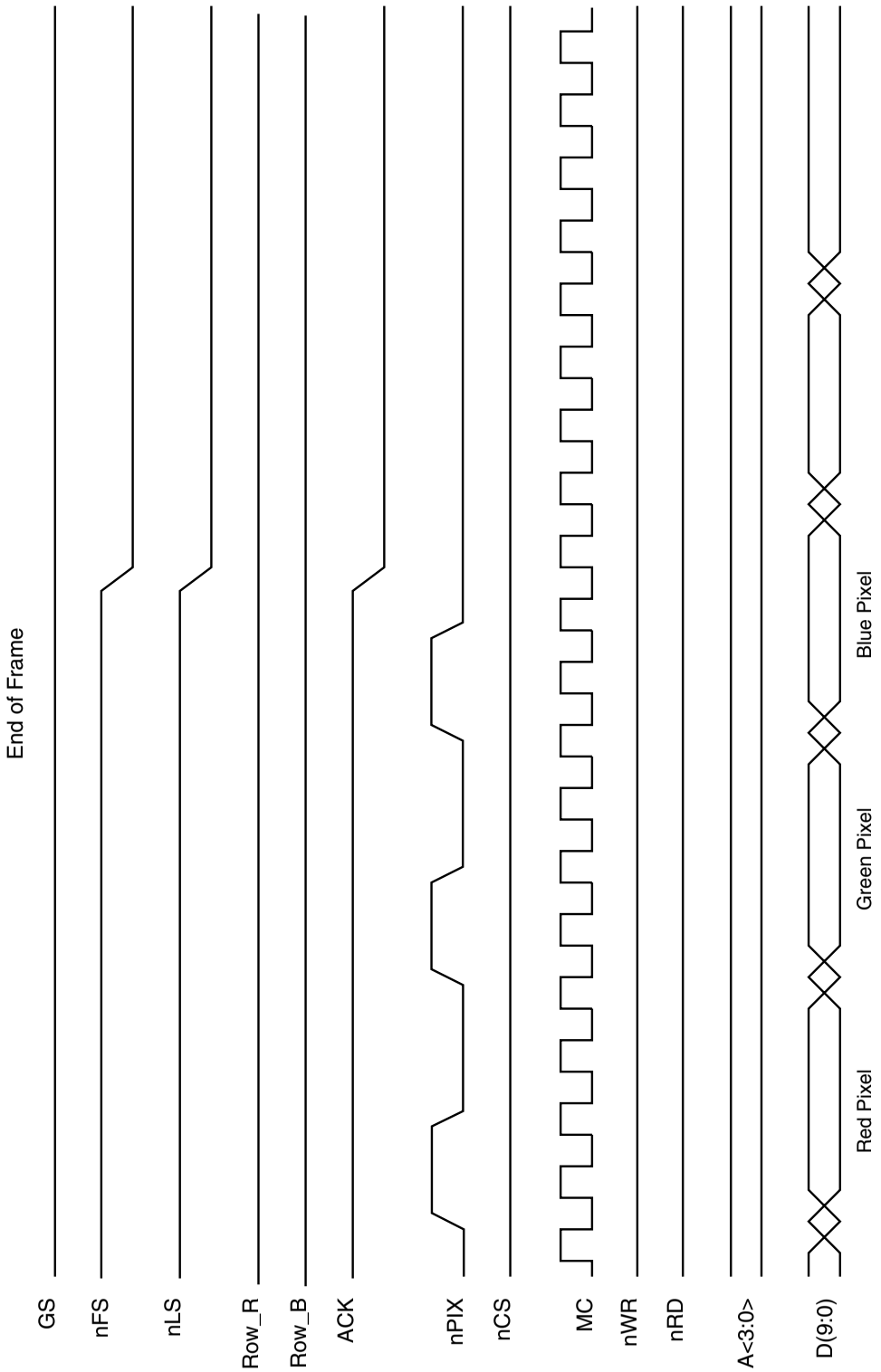


Figure 17. Timing showing End of Frame



Region of Interest

It is possible to define the area of the pixel array the imager scans by writing to register Image Sensor Logic. The lower left hand corner is used as the start address written into the registers as the number of RGB triplets in from the left hand edge and the number of pixel rows up from the bottom. For this calculation, all rows are taken into account, including the black rows (1) and columns (7 RGB triplets).

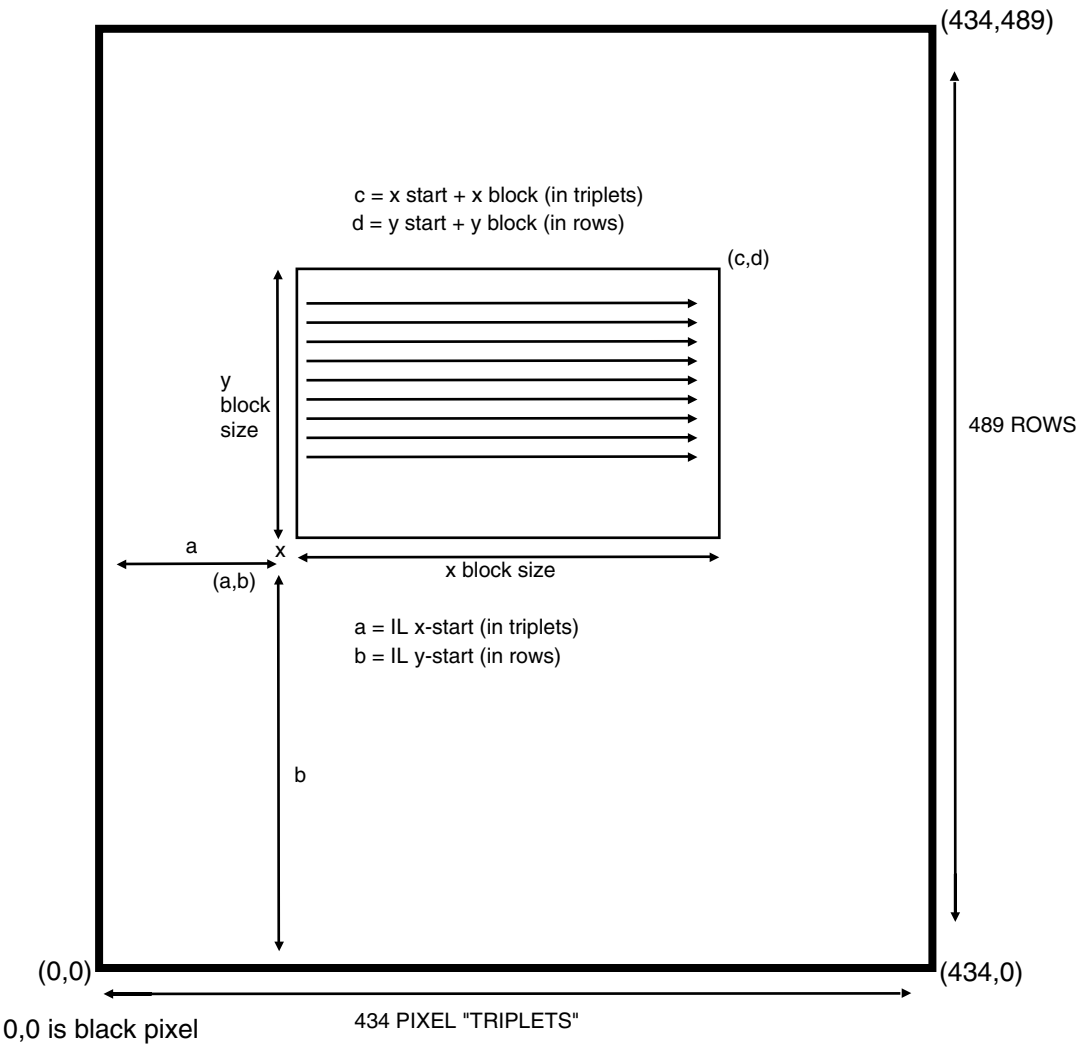
The end position of the scan is set by the user defining the size of the block he wishes to read, writing it as the number of triplets horizontally and the number of rows vertically.

If the start point and the size of the block defined would take the scan region over the edge of the pixel array, the imager will scan up to the boundary and then will continue to read out dummy white pixels (fully saturated) up to the specified count when it will stop and raise the appropriate Line and Field Sync lines, continuing with the next row scan at the correct position. The imager will not wrap around onto the beginning of the same or next row.

The default value for this register is 0 start point with block size which defines all the 1283 x 481 usable pixels (but it includes the single black pixels on the end/top of the imager).

Pixels that are not read will not be reset other than through the user strobing Frame Reset (FR). It is not necessary however as the unread pixels will simply integrate up to saturation and no blooming effect will be visible.

Figure 18. Region of Interest – Calculation



Low Resolution Sub-Sample

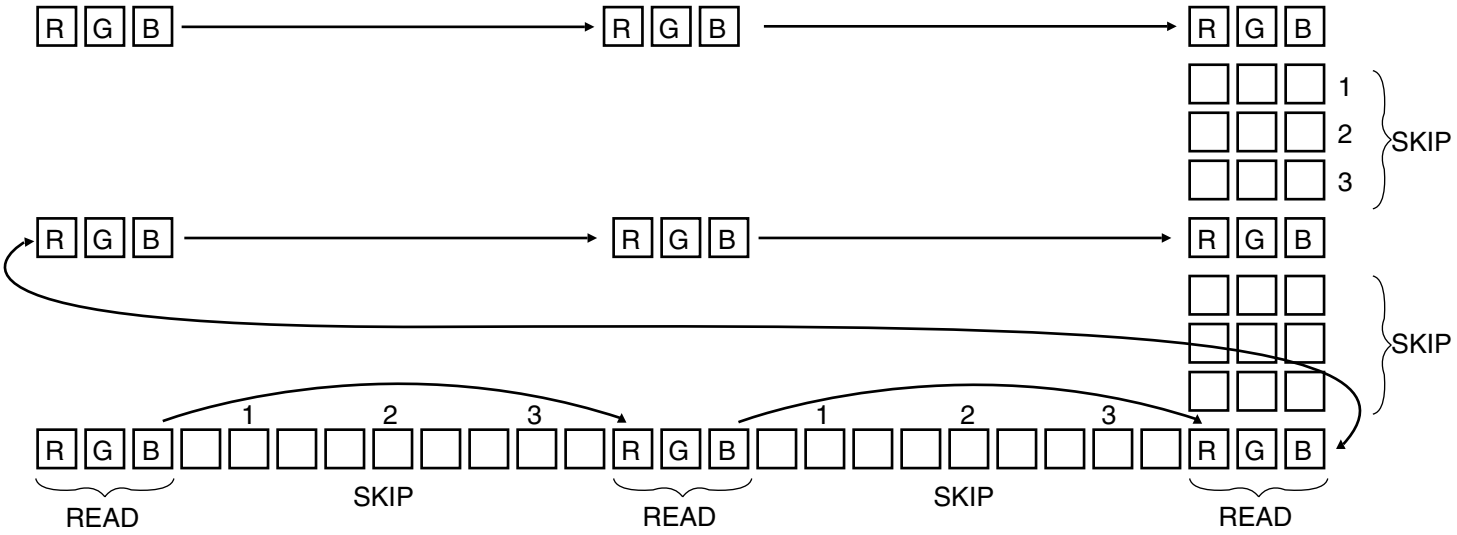
A low-resolution mode that does not require external decimation by the user is implemented in the device. The resolution of this mode approximates to a CIF resolution and is designed for easy operation of video conferencing or where interface bandwidths are a limiting factor.

The low-resolution mode is set by writing the MSB of the Interface Logic (INL) register. This register controls the row and column decode counters to increment by four instead of one so that the resolution is reduced by a factor of 16 to 320 x 120 pixels.

One row in every four is read out vertically. Similarly, one adjacent RGB triplet is read out and then the next three are skipped. During low resolution mode operation, the start point and block size is still defined in terms of absolute rows and pixel triplets from the bottom left hand corner of the imager. The defaults for the mode are therefore the same as for full resolution.

If the region of interest is set at the same time such that the corners of the region do not fall on an even multiple of four, the imager will start scanning at the row and pixel triplet specified and will continue until it is within two rows and two pixel triplets of the specified end point. The user may either calculate this point in advance (setting the registers appropriately) or may detect the end by inspection of the Line Sync and Field Sync outputs.

Figure 19. Sub-Resolution Mode - Pixel Pattern



Non-Destructive Readout

The correlated double sampling mode can be inhibited under control of bit 8 of the Interface Logic (INL) register. Under normal operation, the pixel is reset after every read operation and immediately read again so that fixed offsets can be removed giving the lowest noise possible.

When CDS is inhibited, the pixel is not reset in between successive reads, allowing scanning of the array during an integration period. To reset the whole pixel array when CDS is inhibited, the user must strobe the FR control line (waiting for the ACK) if required.

Note that any image read out when CDS is inhibited will be an inverse image as the pixel value is being subtracted from a reference equal to a saturated pixel. The user may thus use this reading for metering purposes with zero being a known maximum exposure.

Registers

Table 3. Registers

Block	Register	Length	External Address	Default Value	Description
Interface Logic (INL)	Mode Register	10	15 (1111)	0 (0000000000)	Sets mode for analog circuits (i.e. stand-by power & outputs)
Image Sensor Logic (IL)	x-start address	9	0 (0000)	0 (0000000000)	ROI horizontal start coordinate
	y-start address	9	1 (0001)	0 (0000000000)	ROI vertical start coordinate
	sblock size	9	2 (0010)	435 (110110011)	ROI horizontal block size
	y block size	9	3 (0011)	490 (111101010)	ROI vertical block size
	readout	9	4 (0100)	490 (111101010)	Vertical block size for exposure; select readout mode
Analog Logic (AL)	blue gain	6	5 (0101)	0 (000000)	Gain for blue channel
	blue offset	5	6 (0110)	0 (00000)	Offset for blue channel
	green gain	6	7 (0111)	0 (000000)	Gain for green channel
	green offset	5	8 (1000)	0 (00000)	Offset for green channel
	red gain	6	9 (1001)	0 (000000)	Gain for red channel
	red offset	5	10 (1010)	0 (00000)	Offset for red channel
	global gain	2	11 (1011)	0 (00)	Overall gain
Analog Processing (AP)	data	10	12 (1100)	x (xxxxxxxxxx)	Data output from converter
Row Decoder (RD)	test pattern	9	13 (1101)	501 (111110101)	Test word from row decoder
Column Decoder (CD)	test pattern	9	14 (1110)	256 (100000000)	Test word from column decoder

Table 4. Modes

Block	Register	Length	Data	State
Interface Logic (INL)	Mode	10	xxxxxxxxx0	Analog cells on
			xxxxxxxxx1	Analog cells off
			xxxxxxxx0x	A-to-d on
			xxxxxxxx1x	A-to-d powered off
			xxxxxxx0xx	Image sensor bias generator on
			xxxxxxx1xx	Image sensor bias generator off
			xxxxx00xxx	Internal analog signal pathE
			xxxxx01xxx	External analog path between internal analog core & a-to-d core
			xxxxx10xxx	Test mode: external connection to internal analog core
			xxxxx11xxx	Test mode: external analog path between image sensor array and a-to-d core
			xxxx0xxxxx	Test mode: encode select pattern in row decoder
			xxxx1xxxxx	Test mode: encode reset pattern in row decoder
			xx00xxxxxx	Normal operation of digital pad drivers
			xx01xxxxxx	Test mode #1 for digital pad drivers (NAND tree)
			xx10xxxxxx	Test mode #2 for digital pad drivers (NAND tree)
			x0xxxxxxxx	Low noise readout
			x1xxxxxxxx	Non-destructive readout
			0xxxxxxxxx	Sequential readout
			1xxxxxxxxx	Sub-sampled readout
Image Sensor Logic (IL)	Readout Mode	9	111111111	Progressive readout only
			otherwise	Moving blade readout

Figure 20. Timing for Loading and Reading Registers: Modes 1 and 2

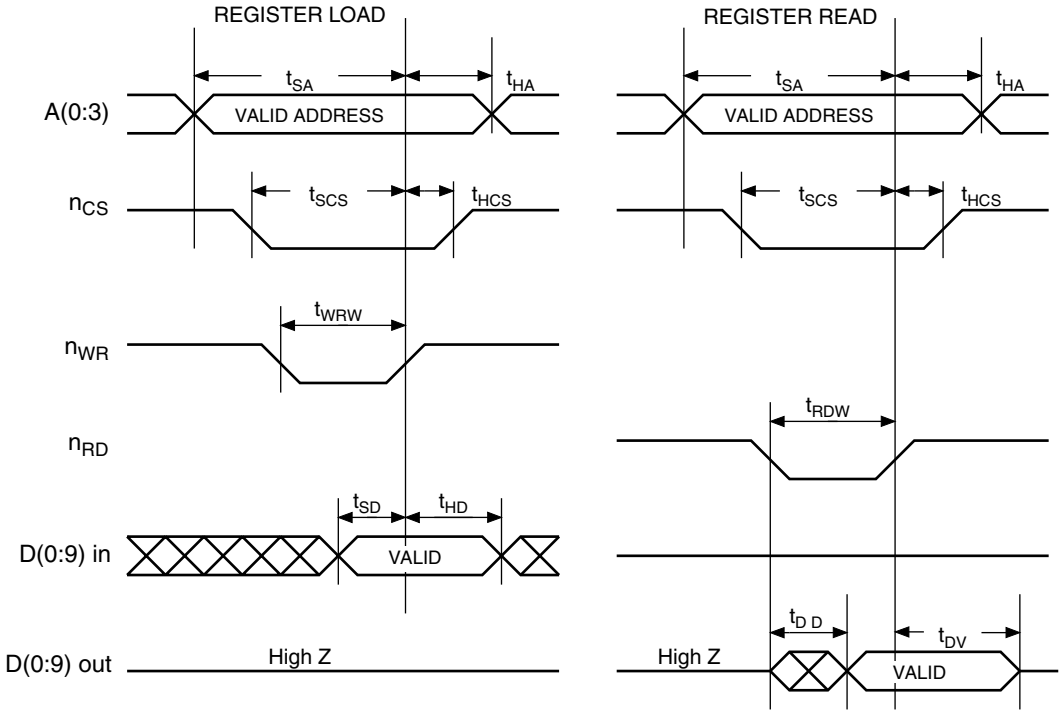


Table 5. Timing Table

Symbol	Characteristic	Min	Typ	Max	Units
t_{WRW}	Write Pulse	18.75			ns
t_{SCS}	Setup Select Device	18.75			ns
t_{SA}	Setup Up Address	18.75			ns
t_{SD}	Setup Up Data	18.75			ns
t_{HCS}	Hold Select Device	18.75			ns
t_{HA}	Hold Address	37.5			ns
t_{HD}	Hold Data	37.5			ns
t_{RDW}	Read Pulse	18.75			ns
t_{DD}	Invalid Data Period	13.00			ns
t_{SCS}	Setup Select Device	18.75			ns
t_{SA}	Setup Up Address	18.75			ns
t_{HCS}	Hold Select Device	18.75			ns
t_{HA}	Hold Addrss	37.5			ns
t_{DV}	Valid Data	13			ns

Gain and Offset Values

$$I_{out} = 2g_{global}g_{color}I_{in} - o_{color}$$

where

I_{out} = Megadac Output Current

I_{in} = Input Current

g_{global} = Global Gain

g_{color} = Gain

o_{color} = Offset

Table 6. Blue, Green & Red Gain Registers (g_{color})

Register Value	Gain
000000	1.00
000001	1.03
000010	1.06
000011	1.09
000100	1.12
...	...
111110	2.86
111111	2.89

Table 7. Global Gain Registers (g_{global})

Register Value	Gain
00	1.0
01	2.0
10	4.0
11	8.0

Table 8. Blue, Green & Red Offset Registers (o_{color})

Register Value	Offset
00000	-2.4 uA(1)
00001	-2.2 uA(1)
...	...
01100	0 uA(1)
...	...
11110	+3.6 uA(1)
11111	+3.8 uA(1)

Note: 1. These values will be validated when analog cores are fixed.

Table 9. Exposure in Continuous Mode

Register Value	Exposure
000000000	1 line
000000000	2 lines
...	...
111101000	489 lines
111101001	490 lines

Color Filtering and Color Recovery

The imager utilizes vertical stripes of pastel red, green and blue filtering laid over the pixels which are rectangular with a height to width ratio of 2:1.

Black and white versions of the imager are available without the color filter layers but these still retain the rectangular pixels.

To produce full color information for each pixel, the user must perform color recovery externally to the imager, either in hardware or software. When low resolution mode is used, however, it is anticipated that due to the subsampling utilized in the imager, full color recovery would not yield improved image quality.

Full color information is available vertically and thus color recovery can be achieved simply by processing nine adjacent pixels sequentially across the row in real time as they are read out of the imager.

Optimum color recovery is achieved by using a simple Median Filter Transform. This color recovery method is covered under US and international patents (US 4,663,665; 4,774,565 and 4,724,395) but a license to use this algorithm will be made available royalty-free to be used ONLY in conjunction with this device.

As a working estimate, the color recovery can be performed using less than 2000 gates of logic with no additional RAM requirements.

An appendix to this datasheet giving a full description of the color recovery method is available under NDA and a diskette containing source code examples of Verilog and C-based implementations will be available upon purchase of the imager.

The following is a diagram extracted from the patent, outlining the color recovery method.

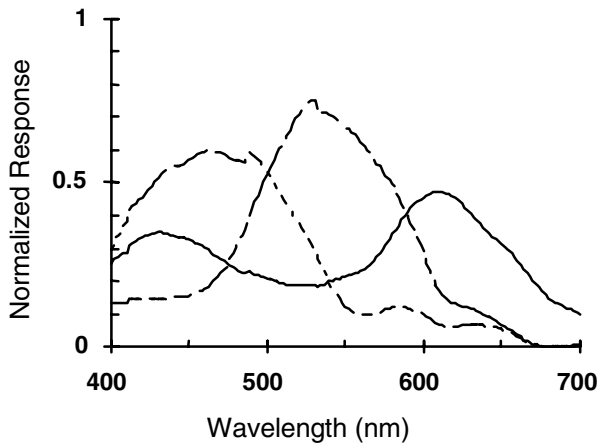
When sub-sampling low-resolution mode is enabled, there is an optical gap of nine pixels between samples which would be incorrectly interpreted by an MFT color recovery algorithm as a sharp luminance edge. A preferred color processing algorithm can be provided on request and under NDA.

Due to the design of the imager, pixels are always read out in triplets whatever the size or region of scan set. The color recovery circuit can therefore expect the same RGBRGBRGB sequence within each data stream and that it will start with the red channel.

Table 10.

Quantum efficiency for pixel of sensor without color filters at 450nm, 550nm, 650nm	>20%
Color filters	rgb color stripes (spectral response)
Optical conversion (including color filters)	>40,000 e-/lux-s
Relative Signal (same gain for all channels): broadband filter at 450 nm, 550nm & 650nm	Matched within 20%
Triplet Order	Red, Green, Blue

Figure 21. Filter Response Characteristic Diagram – Color Filter Transmission in Combination with CM500 ir-cutoff



Suggested Lens Information

To be supplied.

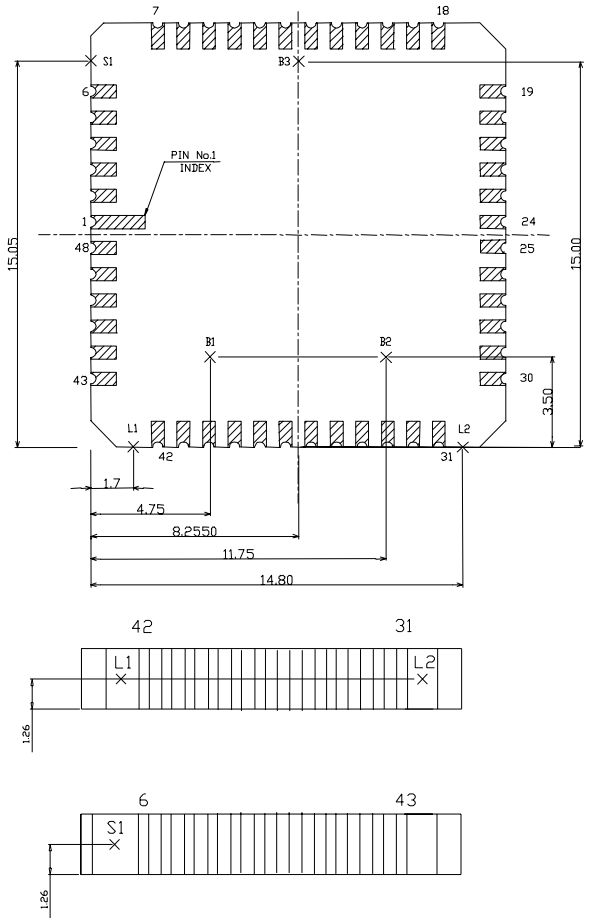
Packaging Information

Table 11. Package and Assembly

Parameter	Tolerance	Unit	Description
Translation in Focal Plane	0 ± 60	µm	Displacement in x- and y-direction of image array center protected onto focal plane
Rotation in Focal Plane	0 ± 0.25	degree	Displacement of focal plane centerline axis due to rotation
Displacement from Focal Plane	0 ± 25	µm	Displacement perpendicular to focal plane of any part of image sensor arrray
Cover Glass[1]	0.55 ± 0.05 none > 20µm 60 - 20	µm	Thickness Occlusions[2] Scratch and dig[2] (MIL-0-13830A)
Cover Glass Placement	> 2.29	mm	Distance from front surface of cover glass to focal plane

Notes: 1. Standard quality cover glass: Clear glass, ground and polished on both sides, no coatings.
2. Occlusion, scratch and dig specification applies only to 9.0 mm by 9.0 mm area centered over the cavity.

Figure 22. 48-lead CLCC Package



Note: For details on plastic packaging, contact your local Atmel sales office.

Figure 23. Package Marking

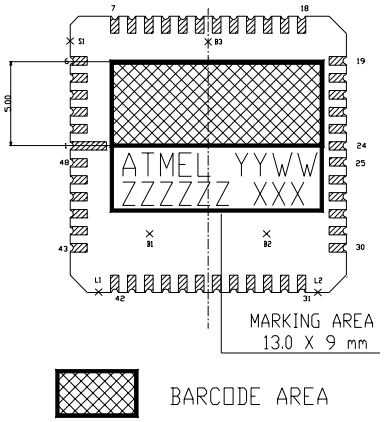
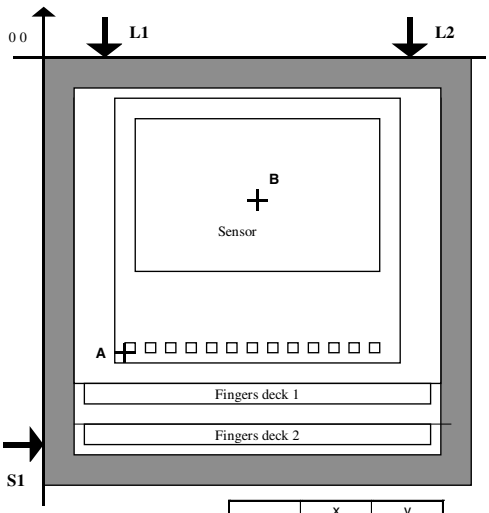


Figure 24. Die and Sensor Location



A:Left borders pad
B:Sensor center

	x	y
A	3893	-11795
B	8345	-6194

Specification

Table 12. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Operating Supply Voltage	-0.3		4.6	V
V_{IN}	DC Input Voltage	-0.3		V_{DD}+0.3	V
V_{OUT}	DC Output Voltage	-0.3		V_{DD}+0.3	V
Temp	Operating Free Air Temp	-40		+85	°C

Table 13. DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Operating Supply Voltage	3.0	3.3	3.6	V
I_{DD}	Overall Supply Current			70	mA
V_{IH}	High Level Input Voltage	0.7 x V_{DD}		V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	0		0.3 x V_{DD}	V
V_{OH}	High Level Output Voltage	V_{DD} - 0.1			V
V_{OL}	Low Level Output Voltage			V_{SS} + 0.1	V
	Leakage Currents		100		nA
Ci load	Digital Input Cap Load		8		pF
Co load	Digital Output Cap Load		43		pF

Notes:
1. I_{DD} is with no Load on all output.
2. V_{OH} is with I_{OL} = 0.3 mA.
3. V_{OL} Low Level Output Voltage is with I_{OL} = 0.3 mA.
4. V_{OL} Leakage Current with for Outputs and Bidirectional Pads.

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

1174A–03/00/0M