

### General Description

AOT500 uses an optimally designed temperature compensated gate-drain zener clamp. Under overvoltage conditions, the clamp activates and turns on the MOSFET, safely dissipating the energy in the MOSFET.

The built in resistor guarantees proper clamp operation under all circuit conditions, and the MOSFET never goes into avalanche breakdown. Advanced trench technology provides excellent low  $R_{ds(on)}$ , gate charge and body diode characteristics, making this device ideal for motor and inductive load control applications.

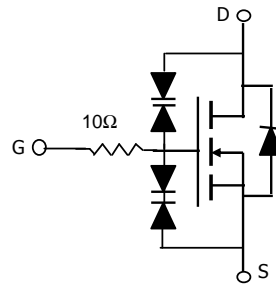
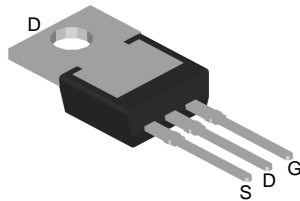
Standard Product AOT500 is Pb-free (meets ROHS & Sony 259 specifications)

### Features

$V_{DS}$  (V) = Clamped

$I_D = 80A$  ( $V_{GS} = 10V$ )

$R_{DS(ON)} < 5.3 m\Omega$  ( $V_{GS} = 10V$ )



#### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	clamped	V
Gate-Source Voltage	$V_{GS}$	clamped	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ C$	80
		$T_C=100^\circ C$	57
Continuous Drain Gate Current	$I_{DG}$	$\pm 50$	mA
Continuous Gate Source Current	$I_{GS}$	$\pm 50$	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	250	A
Avalanche Current $L=100\mu H^H$	$I_{AR}$	50	A
Repetitive avalanche energy <sup>H</sup>	$E_{AR}$	125	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	115
		$T_C=100^\circ C$	58
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ C$

#### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	60	75	$^\circ C/W$
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	0.7	1.3	$^\circ C/W$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS(z)</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =10mA, V <sub>GS</sub> =0V	33			V
BV <sub>CLAMP</sub>	Drain-Source Clamping Voltage	I <sub>D</sub> =1A, V <sub>GS</sub> =0V	36		44	V
I <sub>DSS(z)</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =16V, V <sub>GS</sub> =0V			30	μA
BV <sub>GSS</sub>	Gate-Source Voltage	V <sub>DS</sub> =0V, I <sub>D</sub> =250μA	20			V
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±10V			10	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.5	2	3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	250			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =30A		4.1	5.3	mΩ
		T <sub>J</sub> =125°C		6.2		
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =30A		95		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				80	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		4200	5500	pF
C <sub>oss</sub>	Output Capacitance			765		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			340		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		13	30	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =30A		69	89	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			34		nC
Q <sub>gs</sub>	Gate Source Charge			12		nC
Q <sub>gd</sub>	Gate Drain Charge			15		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.5Ω, R <sub>GEN</sub> =3Ω		25		ns
t <sub>r</sub>	Turn-On Rise Time			35		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			150		ns
t <sub>f</sub>	Turn-Off Fall Time			62		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =30A, dI/dt=100A/μs		60	78	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =30A, dI/dt=100A/μs		84		nC

A: The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C.

B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C.

G: The maximum current rating is limited by bond-wires.

H: E<sub>AR</sub> and I<sub>AR</sub> are based on a 100uH inductor with T<sub>J(start)</sub> = 25C for each pulse.

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## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

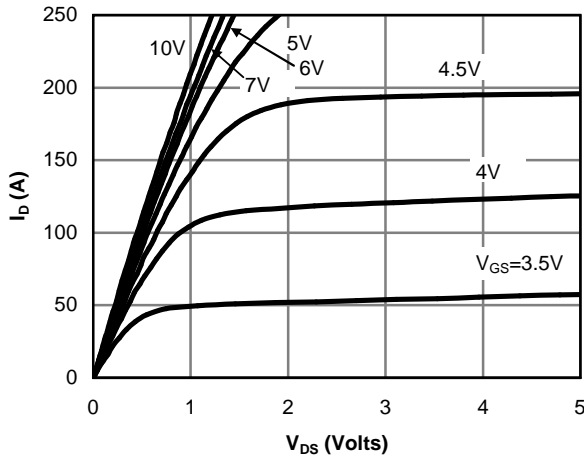


Fig 1: On-Region Characteristics

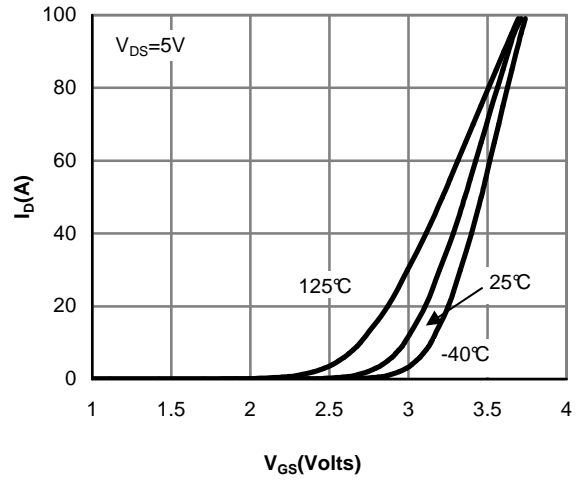


Figure 2: Transfer Characteristics

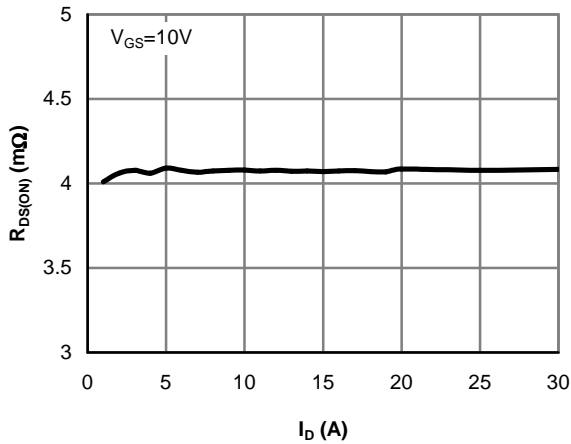


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

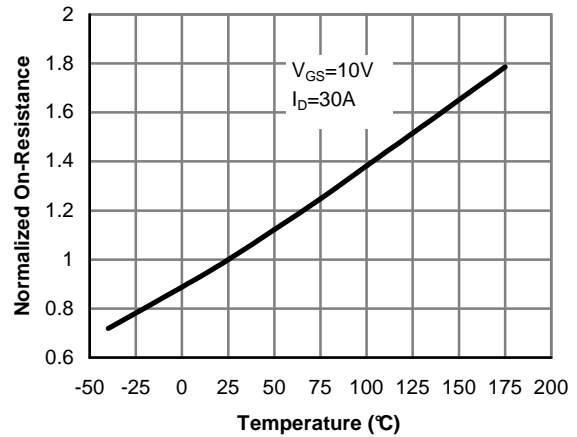


Figure 4: On-Resistance vs. Junction Temperature

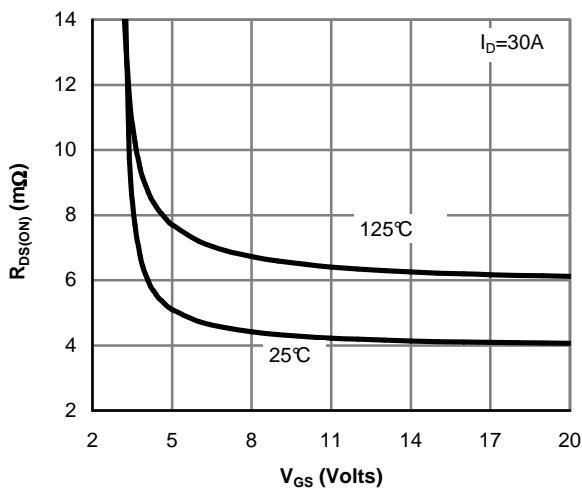


Figure 5: On-Resistance vs. Gate-Source Voltage

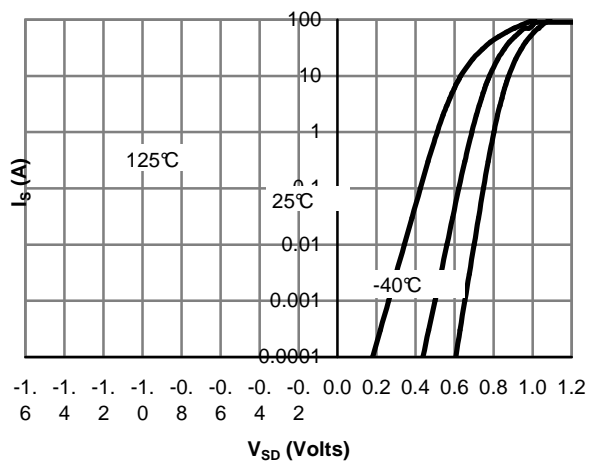


Figure 6: Body-Diode Characteristics

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

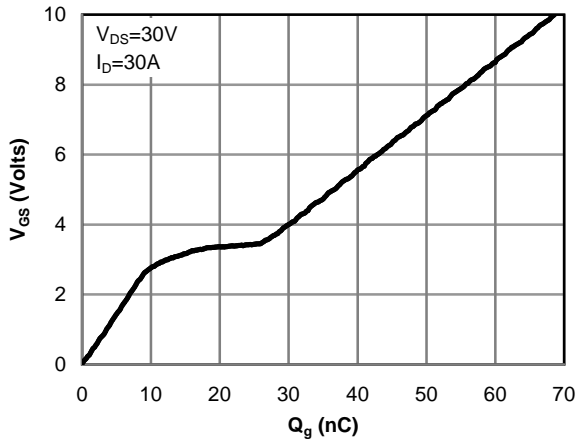


Figure 7: Gate-Charge Characteristics

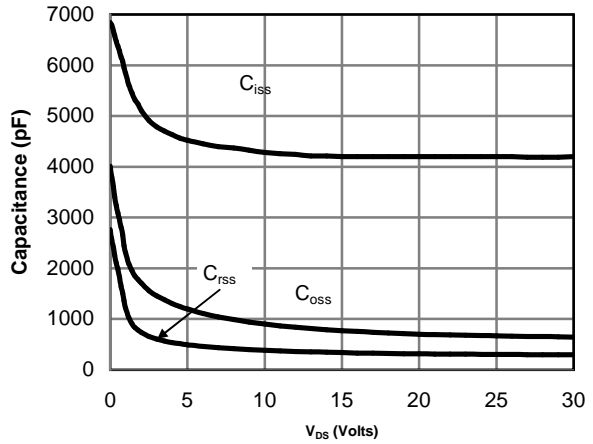


Figure 8: Capacitance Characteristics

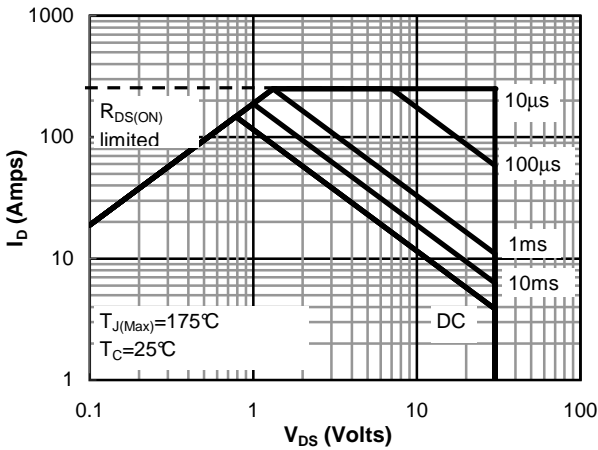


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

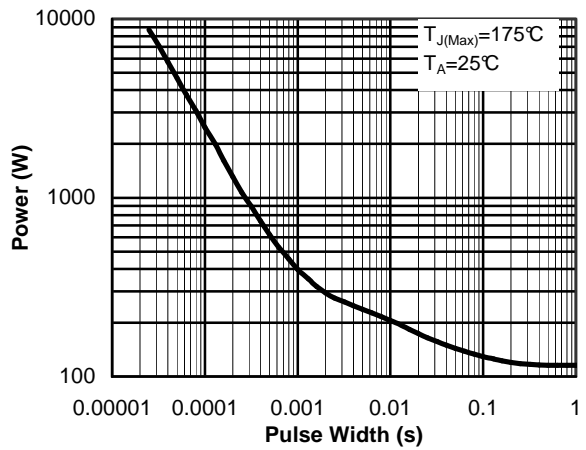


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

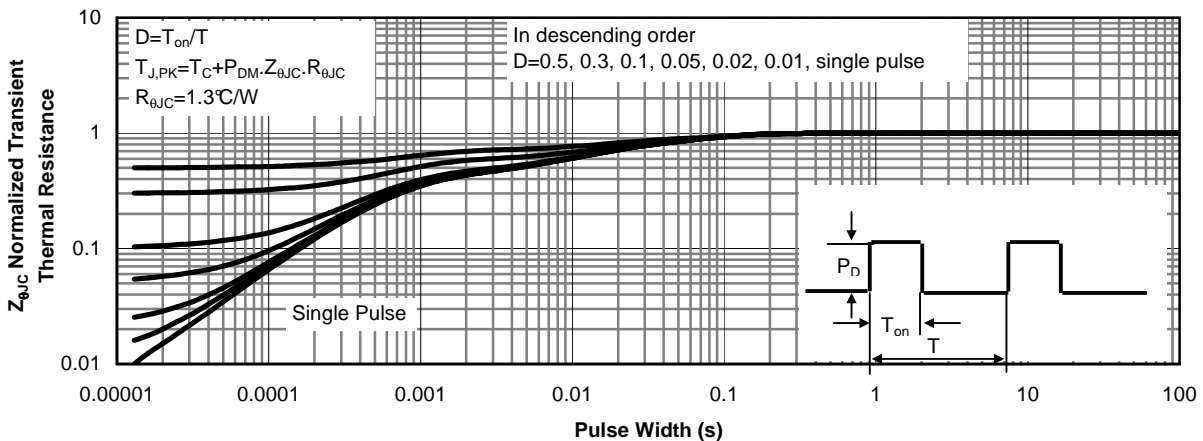


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

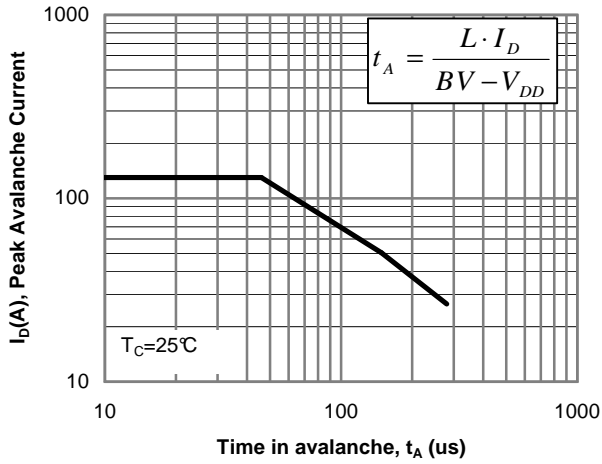


Figure 12: Single Pulse Avalanche capability

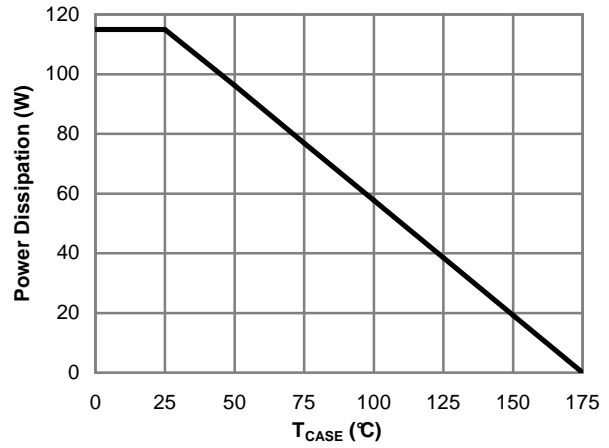


Figure 13: Power De-rating (Note B)

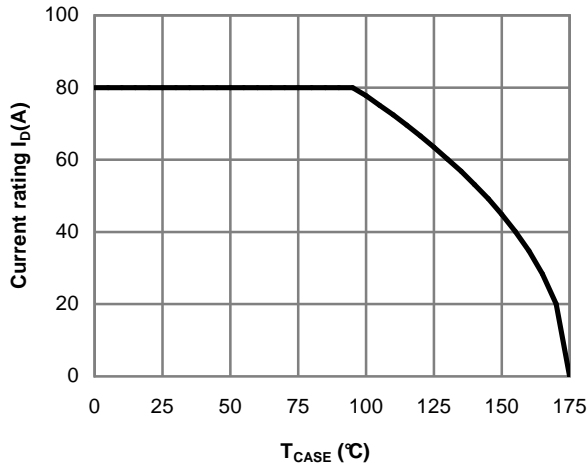
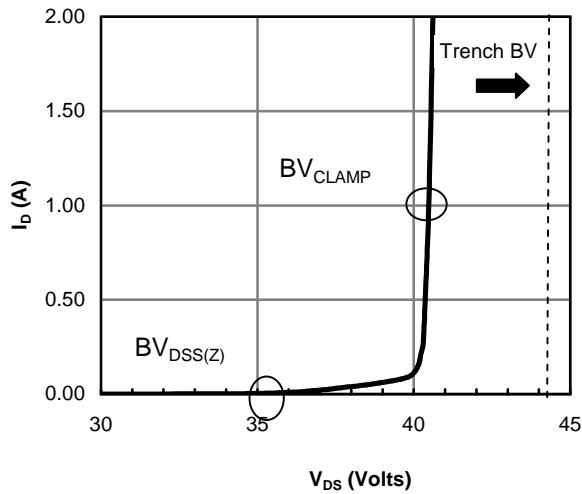


Figure 14: Current De-rating (Note B)

### TYPICAL PROTECTION CHARACTERISTICS



**Fig 15:  $BV_{CLAMP}$  Characteristic**

This device uses built-in Gate to Source and Gate to Drain zener protection. While the Gate-Source zener protects against excessive  $V_{GS}$  conditions, the Gate to Drain protection, clamps the  $V_{DS}$  well below the device breakdown, preventing an avalanche condition within the MOSFET as a result of voltage over-shoot at the Drain electrode.

It is designed to breakdown well before the device breakdown. During such an event, current flows through the zener clamp, which is situated internally between the Gate to Drain. This current flows at  $BV_{DSS(Z)}$ , building up the  $V_{GS}$  internal to the device. When the current level through the zener reaches approximately 300mA, the  $V_{GS}$  is approximately equal to  $V_{GS(PLATEAU)}$ , allowing significant channel conduction and thus clamping the Drain to Source voltage. The  $V_{GS}$  needed to turn the device on is controlled with an internally lumped gate resistor  $R$  approximately equal to 10Ω.

$$V_{GS(PLATEAU)} = 10\Omega \times 300mA = 3V$$

It can also be said that the  $V_{DS}$  during clamping is equal to:

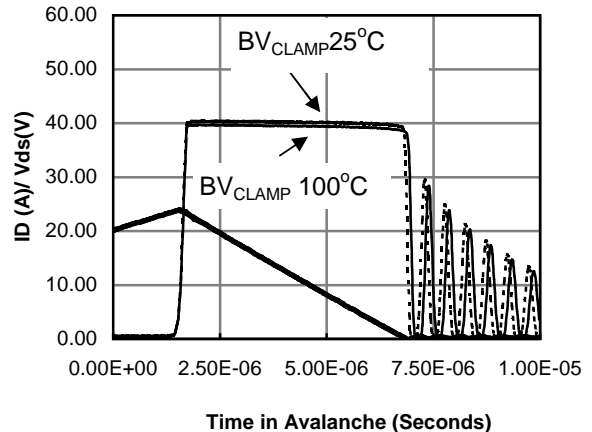
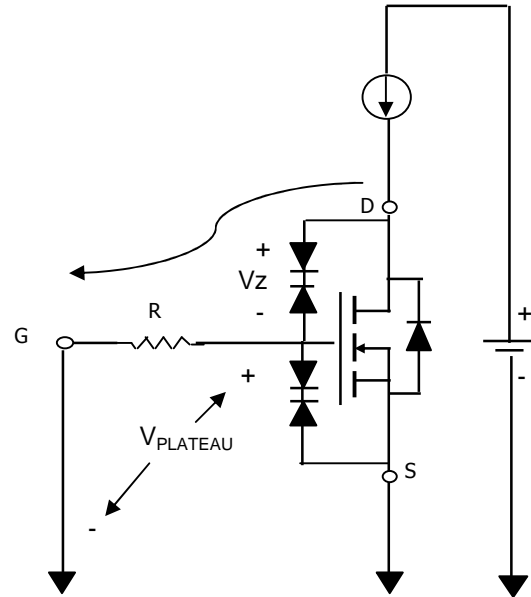
$$BV_{DSS} = BV_{CLAMP} + V_{GS(PLATEAU)}$$

Additional power loss associated with the protection circuitry can be considered negligible when compare to the conduction losses of the MOSFET itself;

EX:

$$PL = 30\mu A_{max} \times 16V = 0.48mW \quad (\text{Zener leakage loss})$$

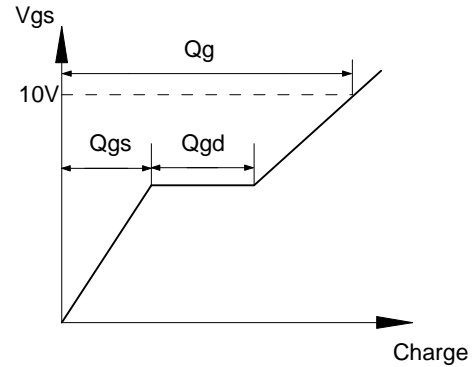
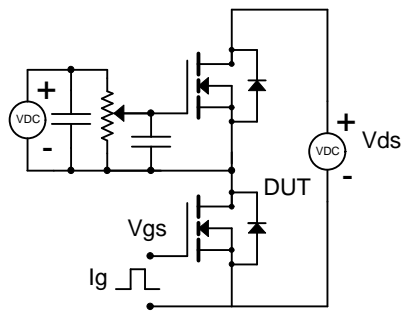
$$PL(rds) = 102A \times 6m\Omega = 300mW \quad (\text{MOSFET loss})$$



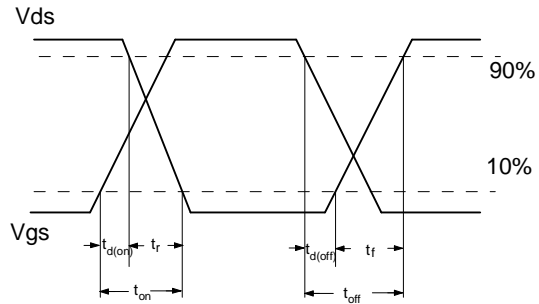
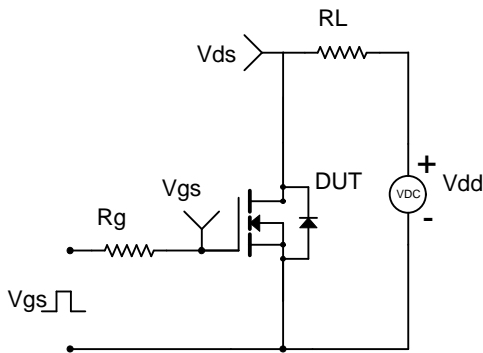
**Fig 16: Unclamped Inductive Switching**

Fig16: The built-in Gate to Drain clamp prevents the device from going into Avalanche by setting the clamp voltage well below the actual breakdown of the device. When the Drain to Gate voltage approaches the  $BV_{CLAMP}$ , the internal Gate to Source voltage is charged up and channel conduction occurs, sinking the current safely through the device. The  $BV_{CLAMP}$  is virtually temperature independent, providing even greater protection during normal operation.

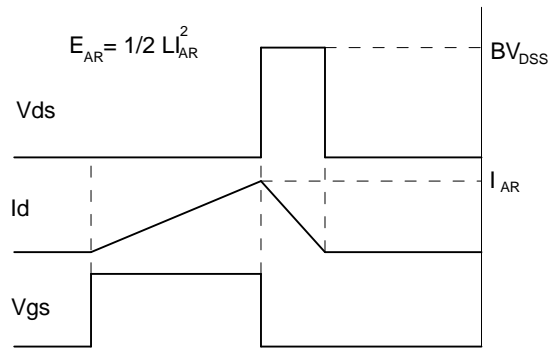
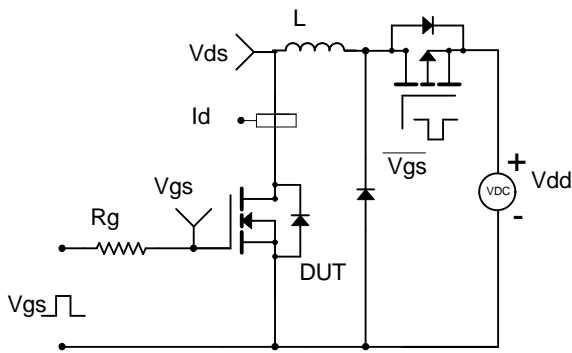
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



### Diode Recovery Test Circuit & Waveforms

