Analog Power AM3414N

## **N-Channel Logic Level MOSFET**

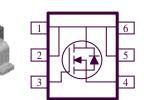
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY				
$V_{DS}(V)$ $r_{DS(on)}(\Omega)$ $I_{D}(A)$				
30	$0.023 @ V_{GS} = 10 V$	6.9		
	$0.030 @ V_{GS} = 4.5V$	6.0		

- Low r<sub>DS(on)</sub> provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSOP-6 saves board space
- Fast switching speed
- High performance trench technology







ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter			Maximum	Units		
Drain-Source Voltage			30	V		
Gate-Source Voltage			±20	V		
	$T_A=25^{\circ}C$	T	6.9			
Continuous Drain Current <sup>a</sup>	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	$\mathbf{I}^{\mathrm{D}}$	5.6	A		
Pulsed Drain Current <sup>b</sup>			±32			
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	1.3	A		
D D: a	$T_A=25^{\circ}C$	D	1.6	W		
Power Dissipation <sup>a</sup>	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	PD	1.0	•••		
Operating Junction and Storage Temperature Range	-	Tı. Teta	-55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Maximum	Units			
Maximum Junction-to-Ambient <sup>a</sup>	t <= 5 sec	$R_{THJA}$	78.0	°C/W		

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## Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

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D	C	T4 C14:	Limits			TT	
Parameter	Symbol	<b>Test Conditions</b>	Min	Тур	Max	Unit	
Switch Off Characteristics							
Gate-Body Leakage	Igss	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA	
Zara Cata Valtaga Drain Current	Ingg	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$			1	A	
Zero Gate Voltage Drain Current	Idss	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			10	uA	
Switch On Characteristics							
Gate-Threshold Voltage	VGS(th)	$V_{DS} = V_{GS}$ , $I_{D} = 250 \text{ uA}$	1			V	
D : G . C D : A		$V_{GS} = 10 \text{ V}, I_{D} = 1 \text{ A}$			23	mΩ	
Drain-Source On-Resistance <sup>A</sup>	fDS(on)	$V_{GS} = 4.5 \text{ V}, I_{D} = 1 \text{ A}$			30		
Forward Tranconductance <sup>A</sup>	gfs	$V_{DS} = 10 \text{ V}, I_{D} = 1 \text{ A}$		45		S	
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			A	
Diode Forward Voltage	V <sub>SD</sub>	Is = 1 A, VGS = 0 V		0.75		V	
Dynamic <sup>b</sup>							
Total Gate Charge	Qg	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 1 A		4		nC	
Gate-Source Charge	$Q_{gs}$	$VDS = 13 \text{ V}, VGS = 3 \text{ V}, ID = 1 \text{ A}$ $R_L = 6 \Omega$		1			
Gate-Drain Charge	$Q_{\mathrm{gd}}$	RL = 0.22		1			
Switching Characteristics							
Turn-On Delay Time	td(on)			6			
Rise Time	t <sub>r</sub>	$V_{DS} = 15 \text{ V},  R_L = 6 \Omega,  I_D = 1 \text{ A},$		4		ne	
Turn-Off Delay Time	td(off)	$V_{GEN} = 10 \text{ V}$		18		ns	
Fall-Time	tf			8			

Notes

a. Pulse test:  $PW \le 300$ us duty cycle  $\le 2\%$ .

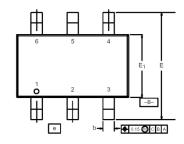
b. Guaranteed by design, not subject to production testing.

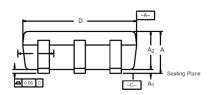
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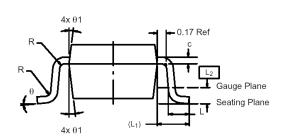
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## Package Information

TSOP-6: 6LEAD







	MILLIMETERS			INCHES			
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.91	-	1.10	0.036	_	0.043	
A <sub>1</sub>	0.01	_	0.10	0.0004	-	0.004	
A <sub>2</sub>	0.84	_	1.00	0.033	0.038	0.039	
b	0.30	0.32	0.45	0.012	0.013	0.018	
С	0.10	0.15	0.20	0.004	0.006	0.008	
D	2.95	3.05	3.10	0.116	0.120	0.122	
E	2.70	2.85	2.98	0.106	0.112	0.117	
E <sub>1</sub>	1.55	1.65	1.70	0.061	0.065	0.067	
е	1.00 BSC			0.0394 BSC			
L	0.35	_	0.50	0.014	_	0.020	
L <sub>1</sub>	0.60 Ref			0.024 Ref			
L <sub>2</sub>	0.25 BSC			0.010 BSC			
R	0.10	-	_	0.004	_	_	
θ	0°	4°	8°	0°	4°	8°	
$\theta_1$	7° Nom			7° Nom			