

## 74VHC08 Quad 2-Input AND Gate

### General Description

The VHC08 is an advanced high speed CMOS 2 Input AND Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including buffer output, which provide high noise immunity and stable output. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

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### Features

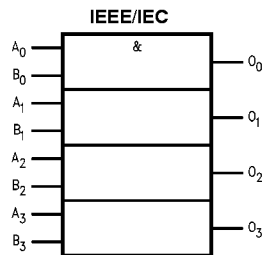
- High Speed:  $t_{PD} = 4.3$  ns (typ) at  $T_A = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Power down protection is provided on all inputs
- Low power dissipation:  $I_{CC} = 2 \mu\text{A}$  (Max) @  $T_A = 25^\circ\text{C}$
- Low noise:  $V_{OLP} = 0.8\text{V}$  (max)
- Pin and function compatible with 74HC08

### Ordering Code:

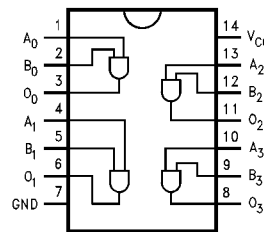
Order Number	Package Number	Package Description
74VHC08M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
74VHC08SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC08MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC08N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$A_n, B_n$	Inputs
$O_n$	Outputs

### Truth Table

A	B	O
L	L	L
L	H	L
H	L	L
H	H	H

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to $V_{CC} + 0.5V$
Input Diode Current ( $I_{IK}$ )	-20 mA
Output Diode Current ( $I_{OK}$ )	$\pm 20$ mA
DC Output Current ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}/GND$ Current ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	260°C

**Recommended Operating Conditions** (Note 2)

Supply Voltage ( $V_{CC}$ )	2.0V to +5.5V
Input Voltage ( $V_{IN}$ )	0V to +5.5V
Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Operating Temperature ( $T_{OPR}$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	
$V_{CC} = 3.3V \pm 0.3V$	0 ns/V ~ 100 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ns/V ~ 20 ns/V

**Note 1:** Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions	
			Min	Typ	Max	Min	Max			
$V_{IH}$	HIGH Level Input Voltage	2.0 3.0 - 5.5	1.50 0.7 $V_{CC}$			1.50 0.7 $V_{CC}$		V		
$V_{IL}$	LOW Level Input Voltage	2.0 3.0 - 5.5			0.50 0.3 $V_{CC}$	0.50 0.3 $V_{CC}$		V		
$V_{OH}$	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu\text{A}$
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4		V		$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$
		3.0	2.58			2.48				
4.5	3.94			3.80						
$V_{OL}$	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu\text{A}$
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1	V		$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$
		3.0			0.36		0.44			
4.5			0.36		0.44					
$I_{IN}$	Input Leakage Current	0 - 5.5			$\pm 0.1$	$\pm 1.0$		$\mu\text{A}$	$V_{IN} = 5.5V$ or GND	
$I_{CC}$	Quiescent Supply Current	5.5			2.0	20.0		$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND	

**Noise Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$		Units	Conditions
			Typ	Limits		
$V_{OLP}$ (Note 3)	Quiet Output Maximum Dynamic $V_{OL}$	5.0	0.3	0.8	V	$C_L = 50 \text{ pF}$
$V_{OLV}$ (Note 3)	Quiet Output Minimum Dynamic $V_{OL}$	5.0	-0.3	-0.8	V	$C_L = 50 \text{ pF}$
$V_{IHD}$ (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50 \text{ pF}$
$V_{ILD}$ (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50 \text{ pF}$

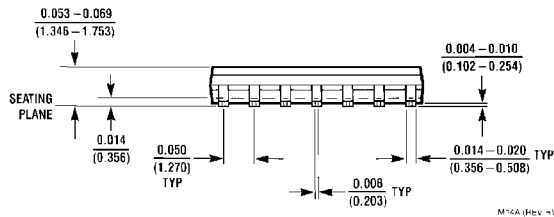
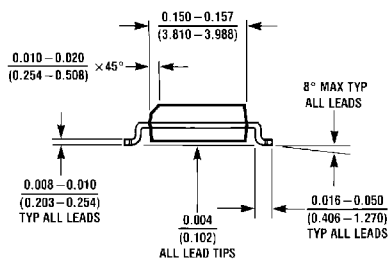
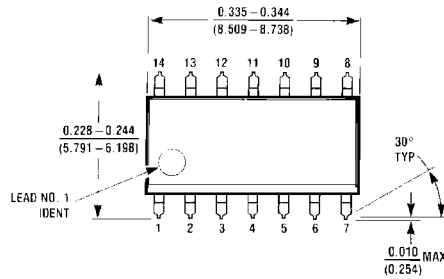
**Note 3:** Parameter guaranteed by design.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t <sub>PHL</sub>	Propagation Delay	3.3 ± 0.3	6.2	8.8	1.0	10.5	ns	C <sub>L</sub> = 15 pF	
t <sub>PLH</sub>			8.7	12.3	1.0	14.0		C <sub>L</sub> = 50 pF	
		5.0 ± 0.5	4.3	5.9	1.0	7.0	ns	C <sub>L</sub> = 15 pF	
			5.8	7.9	1.0	9.0		C <sub>L</sub> = 50 pF	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF	V <sub>CC</sub> = Open	
C <sub>PD</sub>	Power Dissipation Capacitance		18				pF	(Note 4)	

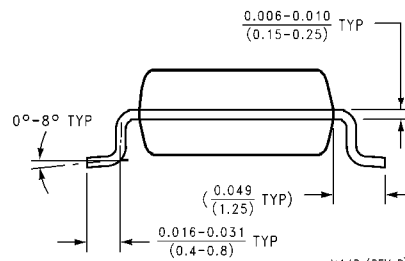
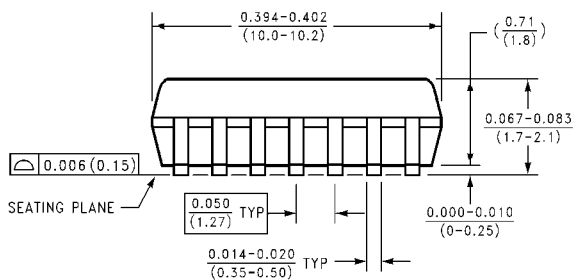
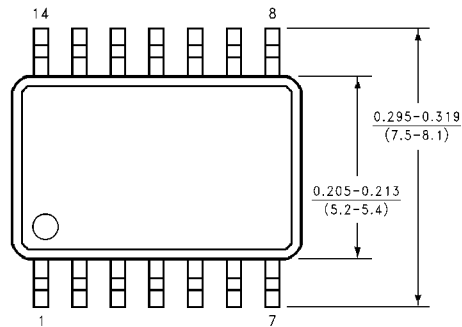
**Note 4:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$  (per gate).

**Physical Dimensions** inches (millimeters) unless otherwise noted



M14A (REV -1)

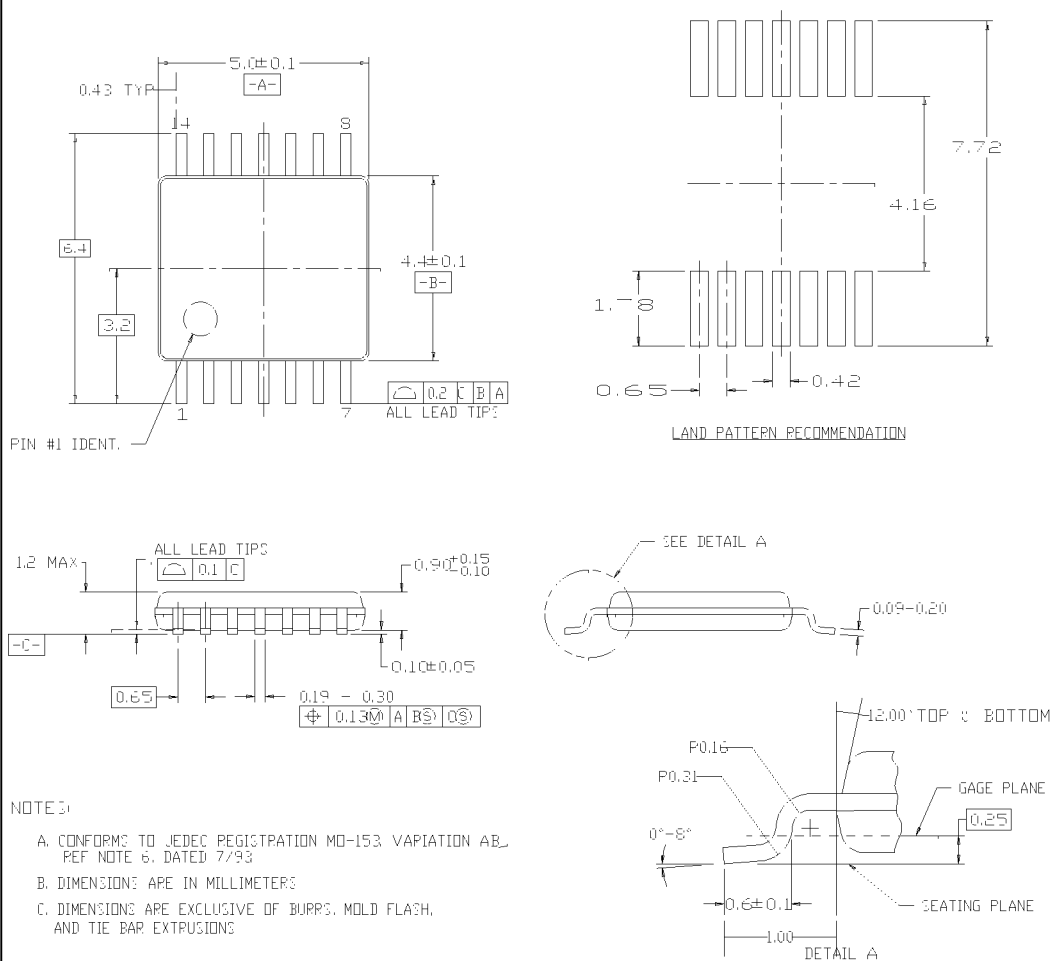
**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow  
Package Number M14A**



M14D (REV B)

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

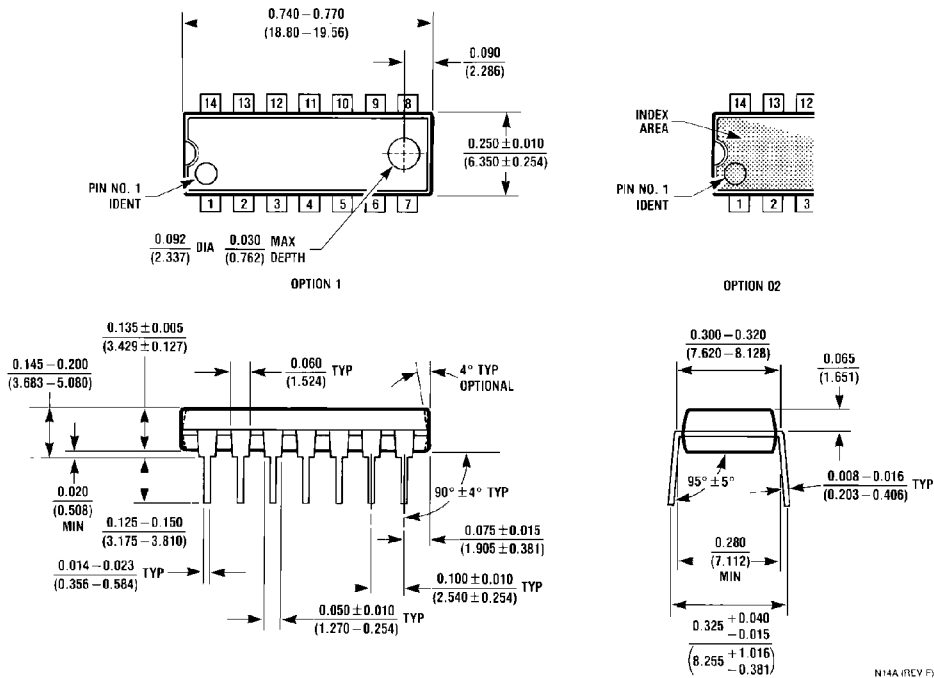


NOTE 3

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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