

256K

Military

X28256M

32K x 8 Bit

## Electrically Erasable PROM

### FEATURES

- 250 ns Access Time
- Fast Write Cycle Times
  - 64-Byte Page Write Operation
  - Byte or Page Write Cycle: 5 ms Typical
  - Complete Memory Rewrite: 2.5 Sec. Typical
  - Effective Byte Write Cycle Time: 78  $\mu$ s Typical
- Software Data Protection
- End of Write Detection
  - DATA Polling
  - Toggle Bit
- Simple Byte and Page Write
  - Single TTL Level  $\overline{WE}$  Signal
  - Internally Latched Address and Data
  - Automatic Write Timing
- Upward Compatible with X2864A
- JEDEC Approved Byte-Wide Pinout

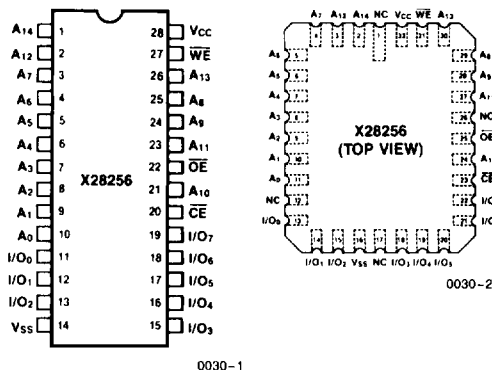
### DESCRIPTION

The Xicor X28256 is a 32K x 8 E<sup>2</sup>PROM, fabricated with Xicor's proprietary, high performance, N-channel floating gate MOS technology. Like all Xicor program-able nonvolatile memories the X28256 is a 5V only device. The X28256 features the JEDEC approved pin-out for byte-wide memories, compatible with industry standard RAMs.

The X28256 supports a 64-byte page write operation, effectively providing a 78  $\mu$ s/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28256 also features  $\overline{DATA}$  Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

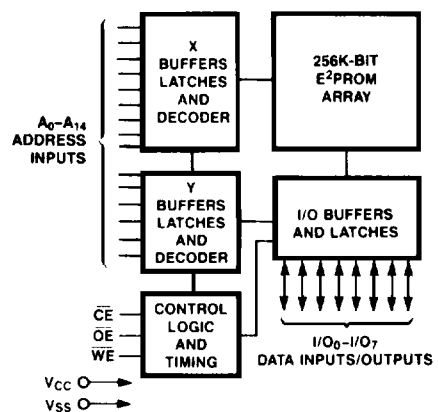
### PIN CONFIGURATIONS



### PIN NAMES

A <sub>0</sub> –A <sub>14</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

### FUNCTIONAL DIAGRAM



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# X28256M

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	−65°C to +135°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin with Respect to Ground	−1.0V to +7V
D.C. Output Current	5 mA
Lead Temperature (Soldering, 10 Seconds)	300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. OPERATING CHARACTERISTICS

$T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ , unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
$I_{CC}$	$V_{CC}$ Current (Active)		60	120	mA	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = $V_{CC}$
$I_{SB}$	$V_{CC}$ Current (Standby)		35	60	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = $V_{CC}$
$I_{LI}$	Input Leakage Current			10	$\mu\text{A}$	$V_{IN} = \text{GND to } V_{CC}$
$I_{LO}$	Output Leakage Current			10	$\mu\text{A}$	$V_{OUT} = \text{GND to } V_{CC}$ , $\overline{CE} = V_{IH}$
$V_{IL}$	Input Low Voltage	−1.0		0.8	V	
$V_{IH}$	Input High Voltage	2.0		$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage			0.4	V	$I_{OL} = 2.1\text{ mA}$
$V_{OH}$	Output High Voltage	2.4			V	$I_{OH} = -400\text{ }\mu\text{A}$

## TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
$t_{PUR}^{(2)}$	Power-Up to Read Operation	100	$\mu\text{s}$
$t_{PUW}^{(2)}$	Power-Up to Write Operation	5	ms

**CAPACITANCE**  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = 5\text{V}$

Symbol	Test	Max.	Units	Conditions
$C_{I/O}^{(2)}$	Input/Output Capacitance	10	pF	$V_{I/O} = 0\text{V}$
$C_{IN}^{(2)}$	Input Capacitance	6	pF	$V_{IN} = 0\text{V}$

## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100\text{ pF}$

## MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	$D_{OUT}$	Active
L	H	L	Write	$D_{IN}$	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

**Notes:** (1) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.

(2) This parameter is periodically sampled and not 100% tested.

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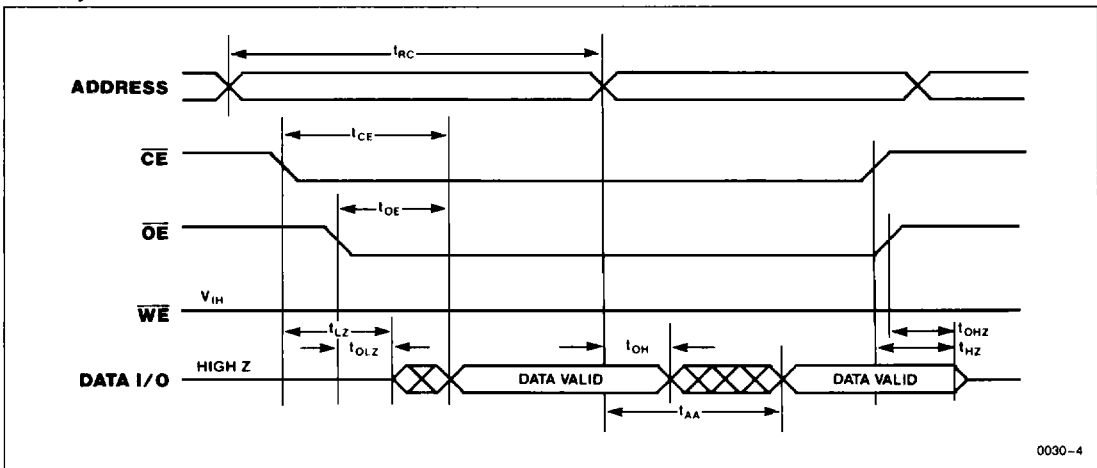
## A.C. CHARACTERISTICS

$T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ , unless otherwise specified.

### Read Cycle Limits

Symbol	Parameter	X28256M-25		X28256M		X28256M-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	250		300		350		ns
$t_{CE}$	Chip Enable Access Time		250		300		350	ns
$t_{AA}$	Address Access Time		250		300		350	ns
$t_{OE}$	Output Enable Access Time		100		100		100	ns
$t_{LZ}$	$\overline{CE}$ Low to Active Output	0		0		0		ns
$t_{OLZ}$	$\overline{OE}$ Low to Active Output	0		0		0		ns
$t_{HZ}^{(3)}$	$\overline{CE}$ High to High Z Output	0	80	0	80	0	80	ns
$t_{OHZ}^{(3)}$	$\overline{OE}$ High to High Z Output	0	80	0	80	0	80	ns
$t_{OH}$	Output Hold from Address Change	0		0		0		ns

### Read Cycle



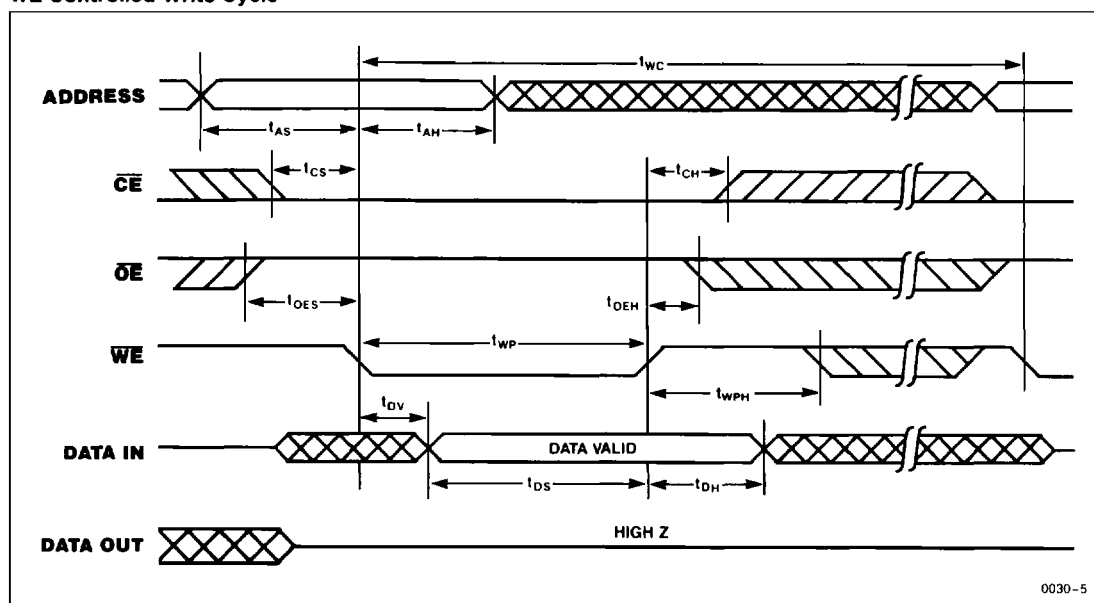
**Note:** (3)  $t_{HZ}$  and  $t_{OHZ}$  are measured from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

## X28256M

### Write Cycle Limits

Symbol	Parameter	Min.	Typ.(4)	Max.	Units
$t_{WC}$	Write Cycle Time		5	10	ms
$t_{AS}$	Address Setup Time	0			ns
$t_{AH}$	Address Hold Time	150			ns
$t_{CS}$	Write Setup Time	0			ns
$t_{CH}$	Write Hold Time	0			ns
$t_{CW}$	$\overline{CE}$ Pulse Width	150			ns
$t_{OES}$	$\overline{OE}$ High Setup Time	10			ns
$t_{OEH}$	$\overline{OE}$ High Hold Time	10			ns
$t_{WP}$	$\overline{WE}$ Pulse Width	150			ns
$t_{WPH}$	$\overline{WE}$ High Recovery	1			$\mu$ s
$t_{DV}$	Data Valid			300	ns
$t_{DS}$	Data Setup	100			ns </td
$t_{DH}$	Data Hold	15			ns
$t_{DW}$	Delay to Next Write	10			$\mu$ s
$t_{BLC}$	Byte Load Cycle	2		100	$\mu$ s

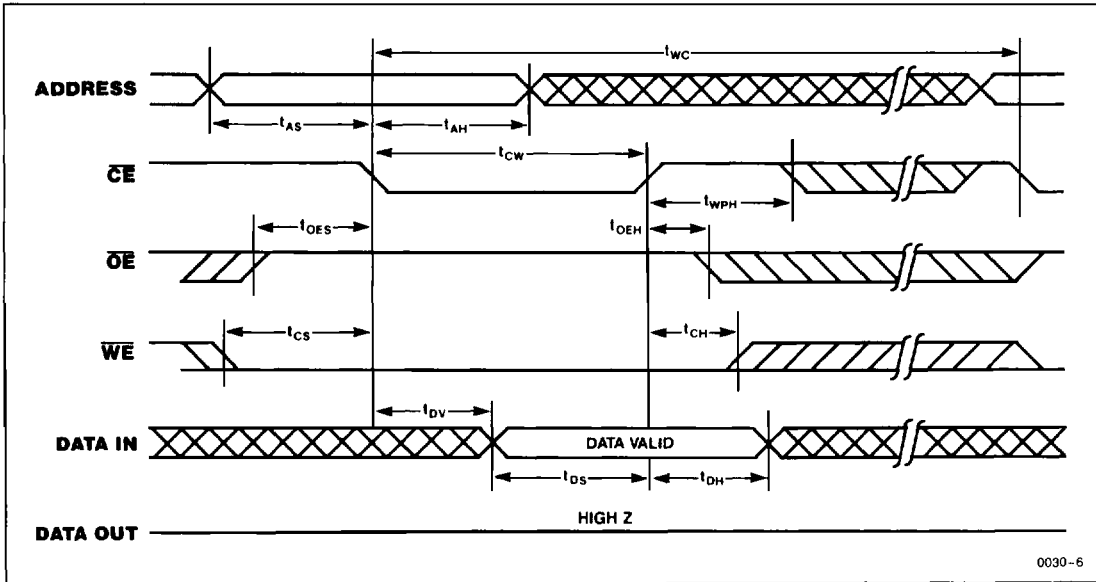
### $\overline{WE}$ Controlled Write Cycle



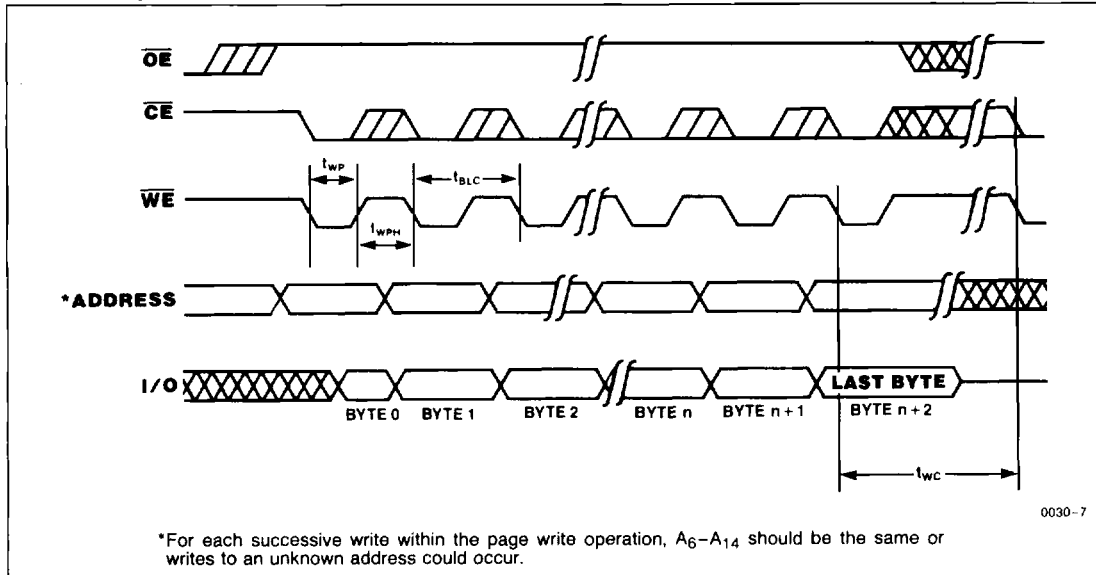
**Note:** (4) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.

# X28256M

## CE Controlled Write Cycle



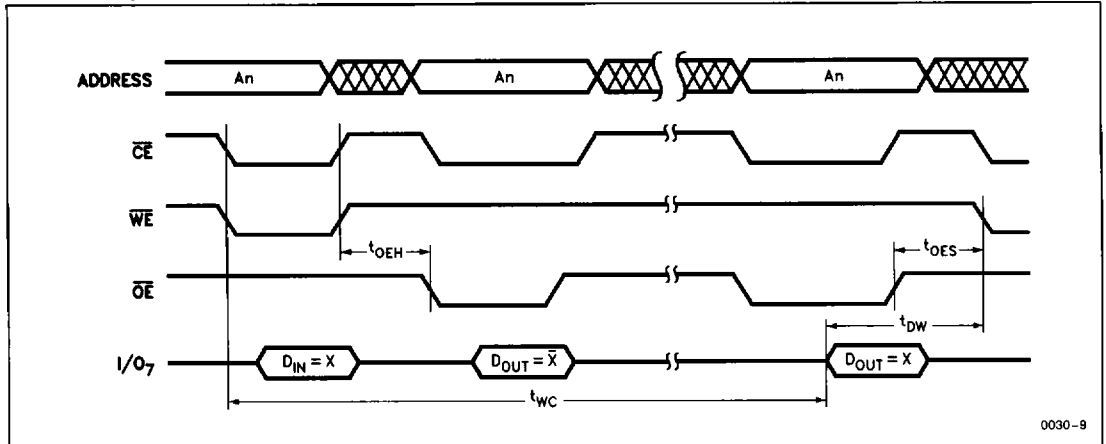
## Page Write Cycle



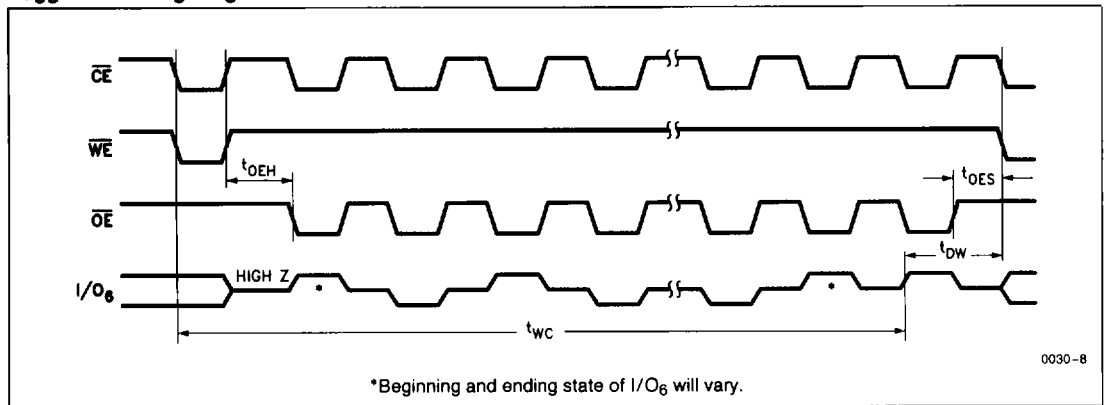
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**DATA Polling Timing Diagram**



**Toggle Bit Timing Diagram**



## X28256M

### PIN DESCRIPTIONS

#### Addresses ( $A_0$ – $A_{14}$ )

The Address inputs select an 8-bit memory location during a read or write operation.

#### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced.

#### Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

#### Data In/Data Out ( $I/O_0$ – $I/O_7$ )

Data is written to or read from the X28256 through the I/O pins.

#### Write Enable ( $\overline{WE}$ )

The Write Enable input controls the writing of data to the X28256.

### DEVICE OPERATION

#### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

#### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X28256 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

#### Page Write Operation

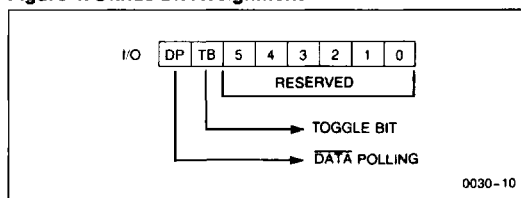
The page write feature of the X28256 allows the entire memory to be written in 2.5 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28256 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_6$  through  $A_{14}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100  $\mu$ s.

#### Write Operation Status Bits

The X28256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



#### DATA Polling ( $I/O_7$ )

The X28256 features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X28256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on  $I/O_7$  (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete,  $I/O_7$  will reflect true data. Note: If the X28256 is in the protected state and an illegal write operation is attempted DATA Polling will not operate.

#### Toggle Bit ( $I/O_6$ )

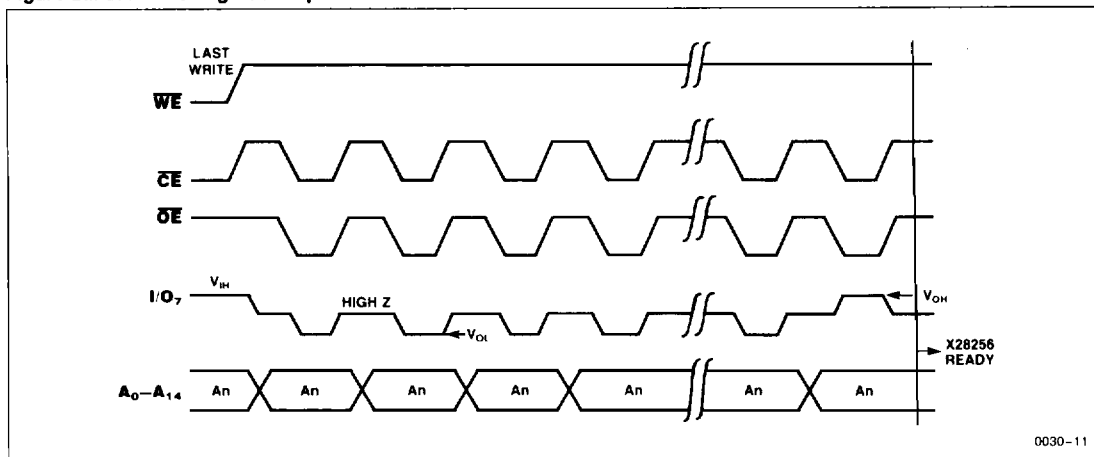
The X28256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle  $I/O_6$  will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

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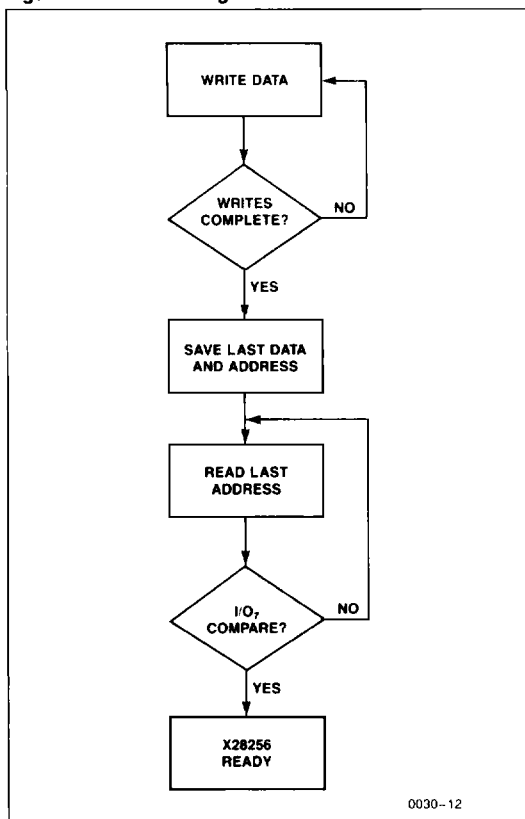
### DATA POLLING I/O<sub>7</sub>

Figure 2a: DATA Polling Bus Sequence



0030-11

Figure 2b: DATA Polling Software Flow



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DATA Polling can effectively halve the time for writing to the X28256. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.



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## THE TOGGLE BIT I/O<sub>6</sub>

Figure 3a: Toggle Bit Bus Sequence

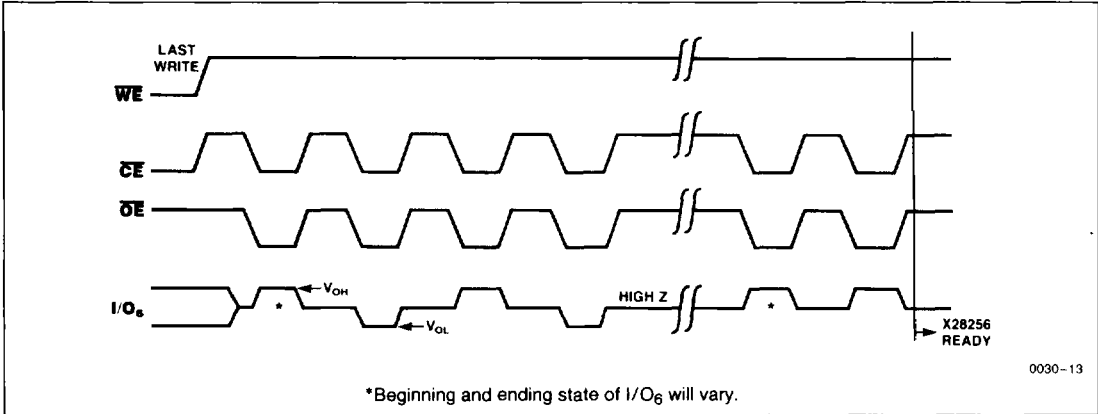
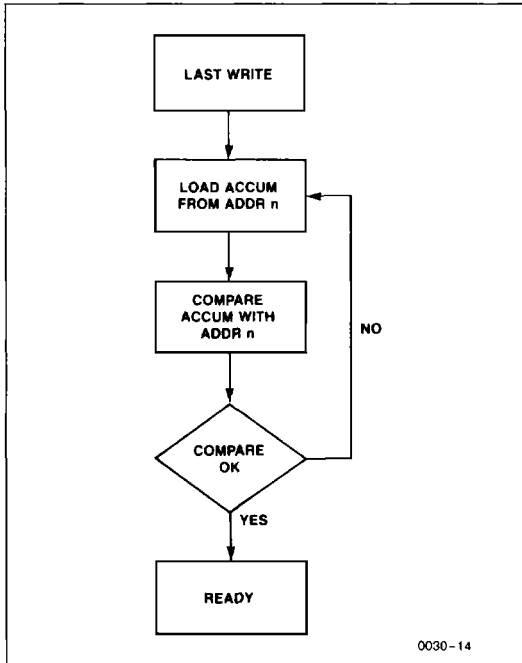


Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28256 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

## X28256M

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### HARDWARE DATA PROTECTION

The X28256 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse less than 20 ns will not initiate a write cycle.
- Default  $V_{CC}$  Sense—All functions are inhibited when  $V_{CC}$  is  $\leq 3V$ , typically.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH, or  $\overline{CE}$  HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

### SOFTWARE DATA PROTECTION

The X28256 offers a software controlled data protection feature. The X28256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once  $V_{CC}$  was stable.

The X28256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software data protection is enabled, the X28256 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

### SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.<sup>(5)</sup> Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

**Note:** (5) Once the three byte sequence is issued it must be followed by a valid byte or page write operation.

SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write

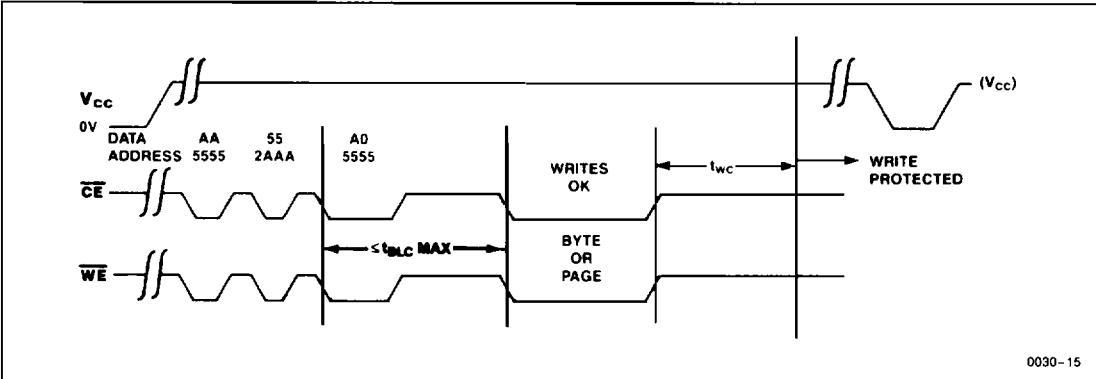
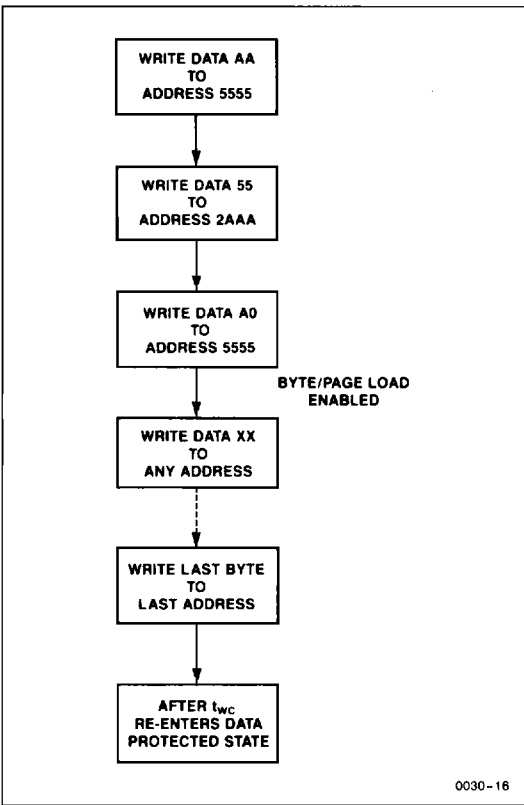


Figure 4b: Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28256 will be write protected during power-down and after any subsequent power-up.

**Note:** Once initiated, the sequence of write operations should not be interrupted.

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### RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

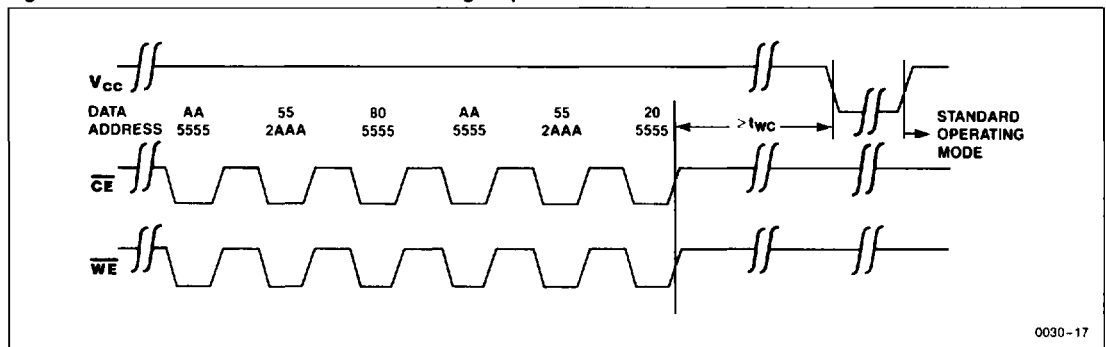
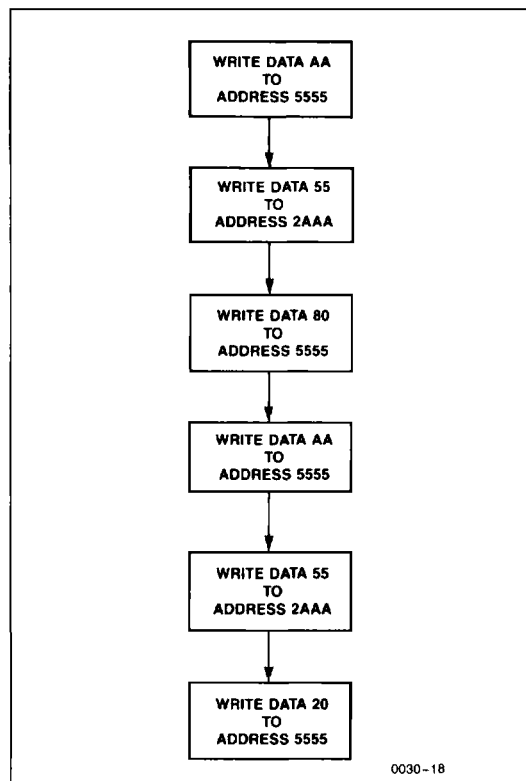


Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E2PROM programmer, the following six step algorithm will reset the internal protection circuit. The next time the X28256 is powered-up the device will be in the standard operating mode.

**Note:** Once initiated, the sequence of write operations should not be interrupted.

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## SYSTEM CONSIDERATIONS

Because the X28256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.





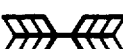
Because the X28256 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu$ F high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu$ F electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

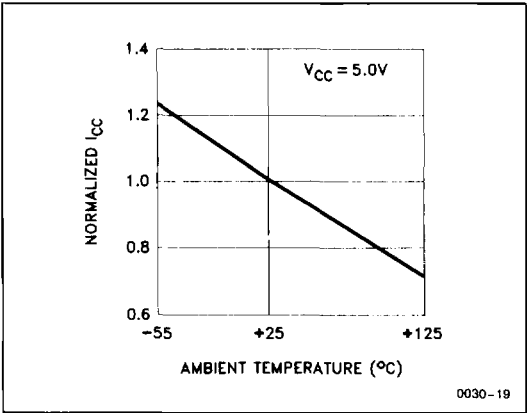
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SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care : Changes Allowed	Changing : State Not Known
	N/A	Center Line is High Impedance

**X28256M**

**Normalized Active Supply Current  
vs. Ambient Temperature**



**Normalized Standby Supply Current  
vs. Ambient Temperature**

