

## Description

The μPD8088 and μPD8088-2 are powerful 8-bit microprocessors that are software-compatible with the μPD8086. They have the same bus interface signals as μPD8085A, allowing them to interface directly with multiplexed bus peripherals. Both having a 20-bit address space which can be divided into four segments of up to 64K bytes each.

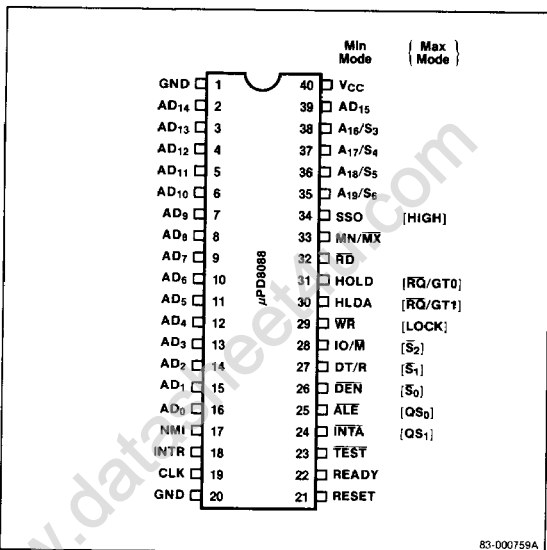
## Features

- 8-bit data bus interface
- 16-bit internal architecture
- Addresses 1 Mbyte of memory
- Software-compatible with the 8086
- Provides byte, word, and block operations
- Performs 8- and 16-bit signed and unsigned arithmetic in binary and decimal
- Multiply and divide instruction
- Directly interfaces to 8155, 8355, and 8755A multiplexed peripherals

## Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD8088D	40-pin ceramic DIP	5 MHz
μPD8088D-2	40-pin ceramic DIP	8 MHz

## Pin Configuration



## Pin Identification

No.	Symbol	Function
1, 20	GND	Ground
2-8, 35-39	A <sub>19</sub> -A <sub>8</sub>	Most significant address bits
9-16	AD <sub>7</sub> -AD <sub>0</sub>	Address/data bus
17	NMI	Non-maskable interrupt
18	INTR	Interrupt request
19	CLK	Clock
21	RESET	Reset
22	READY	Ready
23	TEST	Test
24	INTA	Interrupt acknowledge
25	ALE	Address latch enable
24, 25	QS <sub>1</sub> , QS <sub>0</sub>	Queue status
26	DEN	Data enable
27	DT/R	Data transmit/receive
28	IO/M	IO status/memory
29	WR	Write
29	LOCK	Lock
30	HLDA	Hold acknowledge
31	HOLD	Hold
30, 31	R̄Q/GT <sub>0</sub> R̄Q/GT <sub>1</sub>	Request/grant
32	R̄D	Read
33	MN/MX	Minimum/maximum
34	SS0	Status line
26-28	S̄ <sub>0</sub> -S̄ <sub>2</sub>	Status outputs
35-38	S <sub>3</sub> -S <sub>6</sub>	Status outputs
40	V <sub>CC</sub>	Power supply

**Pin Function****Ground**

Ground.

**Most Significant Address Bits**

Most significant bits for memory operations.

**Address/Data Bus**

Multiplexed address and data bus. 8-bit peripherals tied to these bits use  $A_0$  to condition chip select functions. These lines are three-state during interrupt acknowledge and hold states.

**Non-Maskable Interrupt**

This edge-triggered input causes a type 2 interrupt. The processor uses a look-up table for vectoring information.

**Interrupt Request**

This is a level-triggered interrupt sampled on the last clock cycle of each instruction. A look-up table is used for vectoring. INTR can be masked in software by resetting the interrupt enable bit.

**Clock**

The clock input is a  $1/3$  duty cycle input providing basic timing for the processor and bus controller.

**Reset**

This active high signal must be high for 4 clock cycles. When it returns low, the processor restarts execution.

**Ready**

An acknowledgement from memory or I/O that data will be transferred. Synchronization is done by the μPD8284 clock generator.

**Test**

This input is examined by the "WAIT" instruction, and if low, execution continues. Otherwise the processor waits in an "Idle" state. Synchronized by the processor on the leading edge of CLK.

**Interrupt Acknowledge**

This is a read strobe for reading vectoring information. During T2, T3, and TW of each interrupt acknowledge cycle it is low.

**Address Latch Enable**

This is used in conjunction with the μPD8282/8283 latches to latch the address, during T1 of any bus cycle.

**Queue Status**

(Max mode) tracks the internal μPD8088 instruction queue.

**Data Enable**

This is the output enable for the μPD8286/8287 transceivers. It is active low during memory and I/O access and  $\overline{INTA}$  cycles.

**Data Transmit/Receive**

Controls the direction of data flow through the transceivers.

**IO Status/Memory**

Separates memory access from I/O access.

**Write**

Depending on the state of the  $IO/\overline{M}$  line, the processor is either writing to I/O or memory.

**Lock**

(Max mode) this output is set by the "LOCK" instruction to prevent other system bus masters from gaining control.

**Hold Acknowledge**

A response to the HOLD input, causing the processor to three-state the local bus. The bus becomes active one cycle after HOLD returns low.

**Hold**

When another device requests the local bus, HOLD is driven high, causing the μPD8088 to issue a HLDA.

**Request/Grant**

(Max mode) other local bus masters can force the processor to rebase the local bus at the end of the current bus cycle.

**Read**

Depending on the state of the  $IO/\overline{M}$  line, the processor is reading from either memory or I/O.

## Minimum/Maximum

This input tells the processor in which mode it is to be used. This affects some of the pin descriptions.

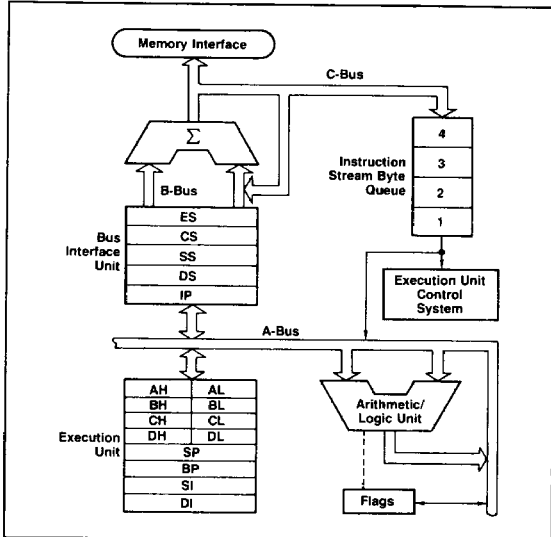
## Status Outputs

(Max mode) These are the status outputs from the processor. They are used by the μPD8288 to generate bus control signals.

## V<sub>CC</sub>

5 V power supply input.

## Block Diagram



## Absolute Maximum Ratings

T<sub>A</sub> = 25°C, Tentative

Power supply voltage, V <sub>DD</sub>	-0.5 V to +7 V
Input voltage, V <sub>I</sub>	-0.5 V to +7 V
Output voltage, V <sub>O</sub>	-0.5 V to +7 V
Operating temperature, T <sub>OPT</sub>	0°C to +70°C
Storage temperature, T <sub>STG</sub>	-65°C to +150°C
Power dissipation, P <sub>D</sub>	2.5 W

**Comment:** Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +5 V ± 10%

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input voltage low	V <sub>IL</sub>	-0.5		+0.8	V	
Input voltage high	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.5	V	
Output voltage low	V <sub>OL</sub>			+0.45	V	I <sub>OL</sub> = 2.0 mA
Output voltage high	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -400 μA
Input clock voltage low	V <sub>CL</sub>	-0.5		+0.6	V	
Input clock voltage high	V <sub>CH</sub>	3.9		V <sub>CC</sub> +1.0	V	
Input leakage current	I <sub>LI</sub>			±10	μA	0 V < V <sub>I</sub> < V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>			±10	μA	0.45 V ≤ V <sub>O</sub> ≤ V <sub>CC</sub>
Power supply current	I <sub>CC</sub>					
μPD8088 /				340	mA	T <sub>A</sub> = 25°C
μPD8088-2				350	mA	T <sub>A</sub> = 25°C

## Capacitance

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input capacitance	C <sub>I</sub>			15	pF	(Note 1)
I/O capacitance	C <sub>I/O</sub>			15	pF	(Note 2)

### Note:

- (1) All input pins except AD<sub>0</sub>-AD<sub>7</sub> and RQ/GT.
- (2) Only input pins AD<sub>0</sub>-AD<sub>7</sub> and RQ/GT.

**AC Characteristics**

**Minimum Complexity Systems**

T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5 V ± 10%

Parameter	Symbol	Limits				Unit	Test Conditions
		μPD8088		μPD8088-2			
		Min	Max	Min	Max		
CLK cycle period	t <sub>CLCL</sub>	200	500	125	500	ns	
CLK low time	t <sub>CLCH</sub>	(2/3 t <sub>CLCL</sub> ) - 15		(2/3 t <sub>CLCL</sub> ) - 15		ns	
CLK high time	t <sub>CHCL</sub>	(1/3 t <sub>CLCL</sub> ) + 2		(1/3 t <sub>CLCL</sub> ) + 2		ns	
CLK rise time	t <sub>CH1CH2</sub>		10		10	ns	From 1.0 V to 3.5 V
CLK fall time	t <sub>CL2CL1</sub>		10		10	ns	From 3.5 V to 1.0 V
Data in setup time	t <sub>DVCL</sub>	30		20		ns	
Data in hold time	t <sub>CLDX</sub>	10		10		ns	
READY setup time into μPD8284	t <sub>R1VCL</sub>	35		35		ns	(Notes 1 & 2)
READY hold time into μPD8284	t <sub>CLR1X</sub>	0		0		ns	(Notes 1 & 2)
READY setup time into μPD8088	t <sub>RYHCH</sub>	(2/3 t <sub>CLCL</sub> ) - 15		(2/3 t <sub>CLCL</sub> ) - 15		ns	
READY hold time into μPD8088	t <sub>CHRYX</sub>	30		20		ns	
READY inactive to CLK	t <sub>RYLCL</sub>	-8		-8		ns	(Note 3)
HOLD setup time	t <sub>HVCH</sub>	35		20		ns	
INTR, NMI, TEST setup time	t <sub>INVCH</sub>	30		15		ns	(Note 2)
Input rise time	t <sub>LIH</sub>		20		20	ns	From 0.8 V to 2.0 V, except clock
Input fall time	t <sub>HL</sub>		12		12	ns	From 2.0 V to 0.8 V, except clock

**Timing Responses**

T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5 V ± 10%

Parameter	Symbol	Limits				Unit	Test Conditions
		μPD8088		μPD8088-2			
		Min	Max	Min	Max		
Address valid delay	t <sub>CLAV</sub>	10	110	10	60	ns	(Note 4)
Address hold time	t <sub>CLAX</sub>	10		10		ns	(Note 4)
Address float delay	t <sub>CLAZ</sub>	t <sub>CLAX</sub>	80	t <sub>CLAX</sub>	50	ns	(Note 4)
ALE width	t <sub>LHLL</sub>	t <sub>CLCH</sub> - 20		t <sub>CLCH</sub> - 10		ns	(Note 4)
ALE active delay	t <sub>CLLH</sub>		80		50	ns	(Note 4)
ALE inactive delay	t <sub>CHLL</sub>		85		55	ns	(Note 4)
Address hold time to ALE inactive	t <sub>LLAX</sub>	t <sub>CHCL</sub> - 10		t <sub>CHCL</sub> - 10		ns	(Note 4)
Data valid delay	t <sub>CLDV</sub>	10	110	10	60	ns	(Note 4)
Data hold time	t <sub>CHDX</sub>	10		10		ns	(Note 4)
Data hold time after WR	t <sub>WHDX</sub>	t <sub>CLCH</sub> - 30		t <sub>CLCH</sub> - 30		ns	(Note 4)
Control active delay 1	t <sub>CVCTV</sub>	10	110	10	70	ns	(Note 4)
Control active delay 2	t <sub>CHCTV</sub>	10	110	10	70	ns	(Note 4)
Control inactive delay	t <sub>CVCTX</sub>	10	110	10	70	ns	(Note 4)
Address float to READ active	t <sub>AZRL</sub>	0		0		ns	(Note 4)
$\overline{RD}$ active delay	t <sub>CLRL</sub>	10	165	10	80	ns	(Note 4)

## AC Characteristics (cont)

### Timing Responses (cont)

T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5 V ± 10%

Parameter	Symbol	Limits				Unit	Test Conditions
		μPD8088		μPD8088-2			
		Min	Max	Min	Max		
RD inactive delay	t <sub>CLR<sub>H</sub></sub>	10	150	10	80	ns	(Note 4)
RD inactive to next address active	t <sub>RHAV</sub>	t <sub>CLCL</sub> - 45		t <sub>CLCL</sub> - 40		ns	(Note 4)
HLDA valid delay	t <sub>CLHAV</sub>	10	160	10	100	ns	(Note 4)
RD width	t <sub>RLRH</sub>	2t <sub>CLCL</sub> - 75		2t <sub>CLCL</sub> - 50		ns	(Note 4)
WR width	t <sub>WLWH</sub>	2t <sub>CLCL</sub> - 60		2t <sub>CLCL</sub> - 40		ns	(Note 4)
Address valid to ALE low	t <sub>AVAL</sub>	t <sub>CLCH</sub> - 60		t <sub>CLCH</sub> - 40		ns	(Note 4)
Output rise time	t <sub>DLOH</sub>		20		20	ns	From 0.8 V to 2.0 V
Output fall time	t <sub>DHOL</sub>		12		12	ns	From 2.0 V to 0.8 V

#### Note:

- (1) Signal at μPD8284 shown for reference only.
- (2) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
- (3) Applies only to T2 state. (8 ns into T3)
- (4) C<sub>L</sub> = 20-100 pF for all μPD8088 outputs (in addition to μPD8088 self-load).

### Maximum Mode System with μPB8288 Bus Controller

T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5 V ± 10%

Parameter	Symbol	Limits				Unit	Test Conditions
		μPD8088		μPD8088-2			
		Min	Max	Min	Max		
CLK cycle period	t <sub>CLCL</sub>	200	500	125	500	ns	
CLK low time	t <sub>CLCH</sub>	( <sup>2</sup> / <sub>3</sub> t <sub>CLCL</sub> ) - 15		( <sup>2</sup> / <sub>3</sub> t <sub>CLCL</sub> ) - 15		ns	
CLK high time	t <sub>CHCL</sub>	( <sup>1</sup> / <sub>3</sub> t <sub>CLCL</sub> ) + 2		( <sup>1</sup> / <sub>3</sub> t <sub>CLCL</sub> ) + 2		ns	
CLK rise time	t <sub>CHCH2</sub>		10		10	ns	From 1.0 V to 3.5 V
CLK fall time	t <sub>CL2CL1</sub>		10		10	ns	From 3.5 V to 1.0 V
Data in setup time	t <sub>DVCL</sub>	30		20		ns	
Data in hold time	t <sub>CLDX</sub>	10		10		ns	
READY setup time into μPD8284	t <sub>RIVCL</sub>	35		35		ns	(Notes 1 & 2)
READY hold time into μPD8284	t <sub>CLRIX</sub>	0		0		ns	(Notes 1 & 2)
READY setup time into μPD8088	t <sub>RYHCH</sub>	( <sup>2</sup> / <sub>3</sub> t <sub>CLCL</sub> ) - 15		( <sup>2</sup> / <sub>3</sub> t <sub>CLCL</sub> ) - 15		ns	
READY hold time into μPD8088	t <sub>CHRYX</sub>	30		20		ns	
READY inactive to CLK	t <sub>RYLCL</sub>	-8		-8		ns	(Note 5)
INTR, NMI, TEST setup time	t <sub>INVCH</sub>	30		15		ns	(Note 2)
RQ / GT setup time	t <sub>GVCH</sub>	30		15		ns	
RQ hold time into μPD8088	t <sub>CHGX</sub>	40		30		ns	
Input rise time	t <sub>LIH</sub>		20		20	ns	From 0.8 V to 2.0 V, except clock
Input fall time	t <sub>LIL</sub>		12		12	ns	From 2.0 V to 0.8 V, except clock

**AC Characteristics (cont)**

**Timing Responses**

μPD8088: T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5 V ± 10%

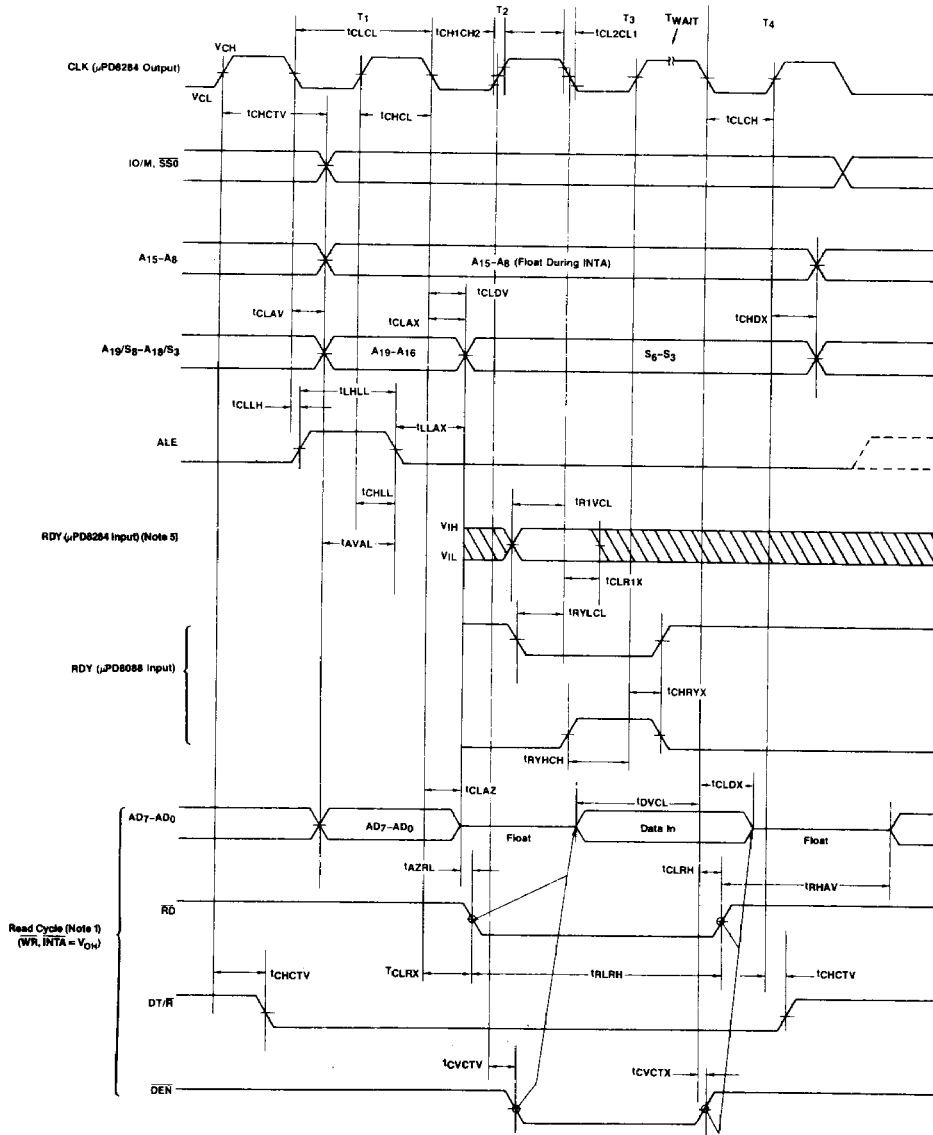
Parameter	Symbol	Limits				Unit	Test Conditions
		μPD8088		μPD8088-2			
		Min	Max	Min	Max		
Command active delay	t <sub>CLML</sub>	10	35	10	35	ns	(Notes 1 & 4)
Command inactive delay	t <sub>CLMH</sub>	10	35	10	35	ns	(Notes 1 & 4)
READY active to status passive	t <sub>RYHSH</sub>		110		65	ns	(Notes 3 & 4)
Status active delay	t <sub>CHSV</sub>	10	110	10	60	ns	(Note 4)
Status inactive delay	t <sub>CLSH</sub>	10	130	10	70	ns	(Note 4)
Address valid delay	t <sub>CLAV</sub>	10	110	10	60	ns	(Note 4)
Address hold time	t <sub>CLAX</sub>	10		10		ns	(Note 4)
Address float delay	t <sub>CLAZ</sub>	t <sub>CLAX</sub>	80	t <sub>CLAX</sub>	50	ns	(Note 4)
Status valid to ALE high	t <sub>SVLH</sub>		15		15	ns	(Notes 1 & 4)
Status valid to MCE high	t <sub>SVMCH</sub>		15		15	ns	(Notes 1 & 4)
CLK low to ALE valid	t <sub>CLLH</sub>		15		15	ns	(Notes 1 & 4)
CLK low to MCE high	t <sub>CLMCH</sub>		15		15	ns	(Notes 1 & 4)
ALE inactive delay	t <sub>CHLL</sub>		15		15	ns	(Notes 1 & 4)
MCE inactive delay	t <sub>CLMCL</sub>		15		15	ns	(Notes 1 & 4)
Data valid delay	t <sub>CLDV</sub>	10	110	10	60	ns	(Note 4)
Data hold time	t <sub>CHDX</sub>	10		10		ns	(Note 4)
Control active delay	t <sub>CVNV</sub>	5	45	5	45	ns	(Notes 1 & 4)
Control inactive delay	t <sub>CVNX</sub>	10	45	10	45	ns	(Notes 1 & 4)
Address float to READ active	t <sub>AZRL</sub>	0		0		ns	(Note 4)
RD active delay	t <sub>CLRL</sub>	10	165	10	100	ns	(Note 4)
RD inactive delay	t <sub>CLRH</sub>	10	150	10	80	ns	(Note 4)
RD inactive to next address active	t <sub>RHAV</sub>	t <sub>CLCL</sub> - 45		t <sub>CLCL</sub> - 40		ns	(Note 4)
Direction control active delay	t <sub>CHDTL</sub>		50		50	ns	(Notes 1 & 4)
Direction control inactive delay	t <sub>CHDTH</sub>		30		30	ns	(Notes 1 & 4)
GT active delay	t <sub>CLGL</sub>	0	85	0	50	ns	(Note 4)
GT inactive delay	t <sub>CLGH</sub>	0	85	0	50	ns	(Note 4)
RD width	t <sub>RLRH</sub>	2t <sub>CLCL</sub> - 75		2t <sub>CLCL</sub> - 50		ns	(Note 4)
Output rise time	t <sub>OLOH</sub>		20		20	ns	From 0.8 V to 2.0 V
Output fall time	t <sub>O HOL</sub>		12		12	ns	From 2.0 V to 0.8 V

**Note:**

- (1) Signal at μPB8284 or μPB8288 shown for reference only.
- (2) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
- (3) Applies only to T3 and wait states.
- (4) C<sub>L</sub> = 20–100 pF for all μPD8088 outputs (in addition to μPD8088 self-load).
- (5) Applies only to T2 state. (8 ns into T3).

## Timing Waveforms

### Minimum Complexity Systems (Note 5)

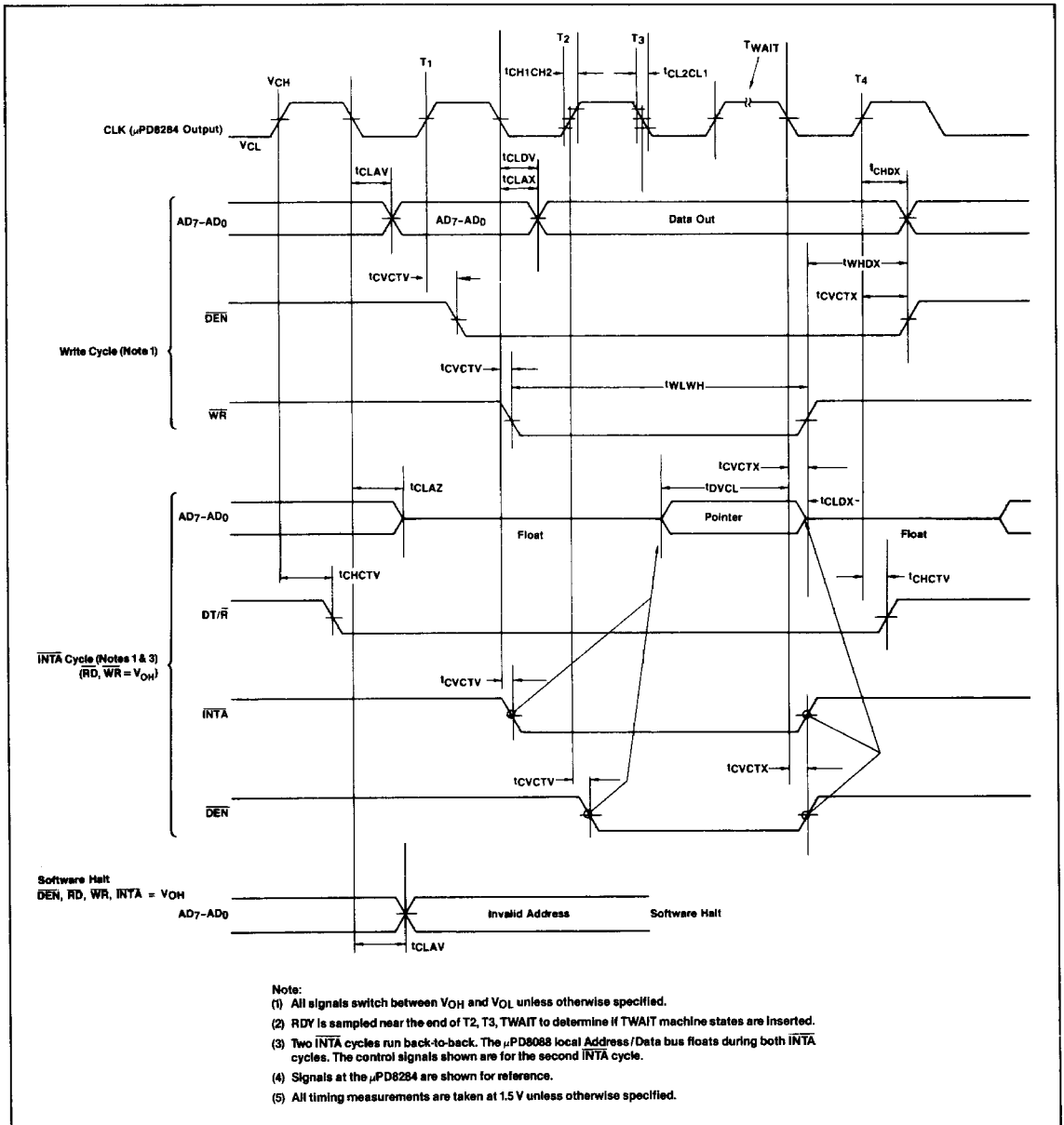


**Note:**

- (1) All signals switch between  $V_{OH}$  and  $V_{OL}$  unless otherwise specified.
- (2) RDY is sampled near the end of T2, T3, TWAIT to determine if TWAIT machine states are inserted.
- (3) Two INTA cycles run back-to-back. The μPD8088 local Address/Data bus floats during both INTA cycles. The control signals shown are for the second INTA cycle.
- (4) Signals at the μPD8284 are shown for reference.
- (5) All timing measurements are taken at 1.5 V unless otherwise specified.

Timing Waveforms (cont)

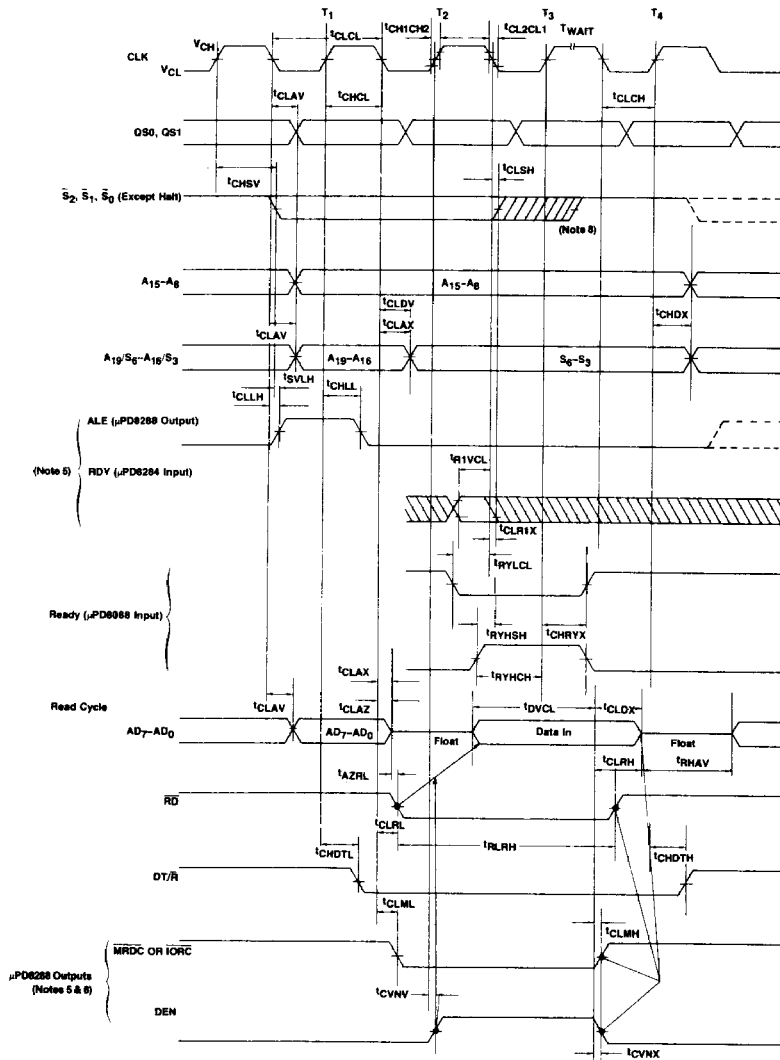
Minimum Complexity Systems (Note 5)





## Timing Waveforms (cont)

### Maximum Mode System Bus Timing Using μPB8288 Bus Controller (Note 7)

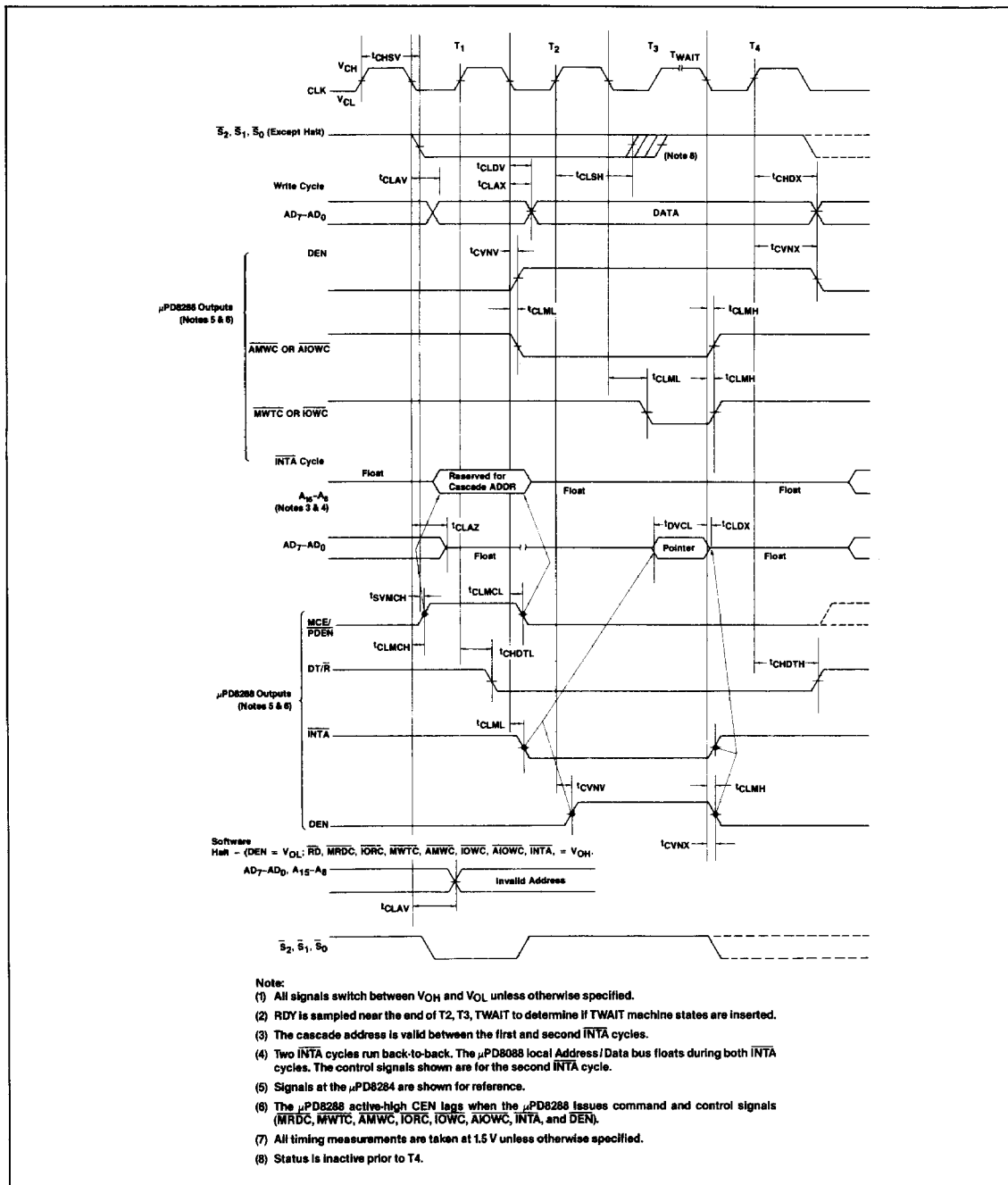


**Note:**

- (1) All signals switch between  $V_{OH}$  and  $V_{OL}$  unless otherwise specified.
- (2) RDY is sampled near the end of T2, T3, TWAIT to determine if TWAIT machine states are inserted.
- (3) The cascade address is valid between the first and second INTA cycles.
- (4) Two INTA cycles run back-to-back. The μPD8088 local Address/Data bus floats during both INTA cycles. The control signals shown are for the second INTA cycle.
- (5) Signals at the μPD8284 are shown for reference.
- (6) The μPD8288 active-high CEN lags when the μPD8288 issues command and control signals (MRDC, MWTC, AMWC, IORC, IDWC, AIOWC, INTA, and DEN).
- (7) All timing measurements are taken at 1.5 V unless otherwise specified.
- (8) Status is inactive prior to T4.

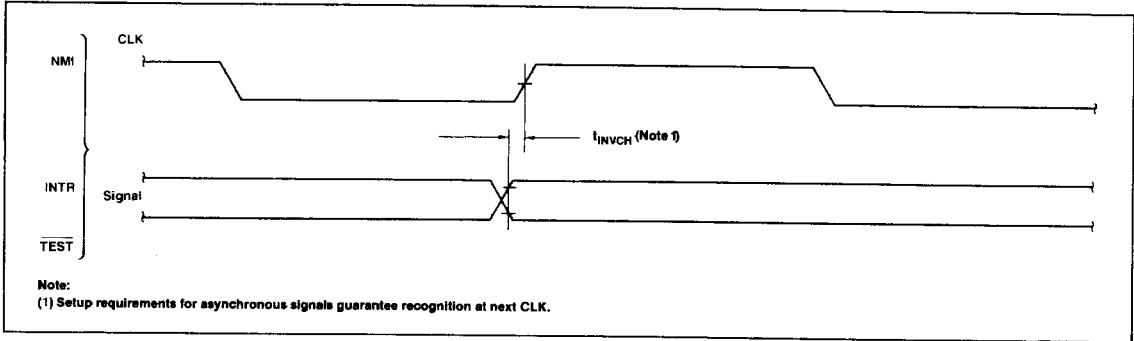
Timing Waveforms (cont)

Maximum Mode System Bus Timing Using μPB8288 Bus Controller (cont) (Note 7)

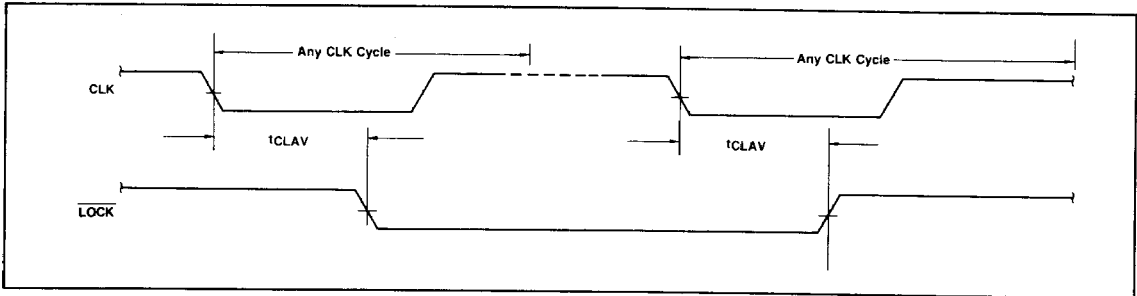


## Timing Waveforms (cont)

### Asynchronous Input Recognition

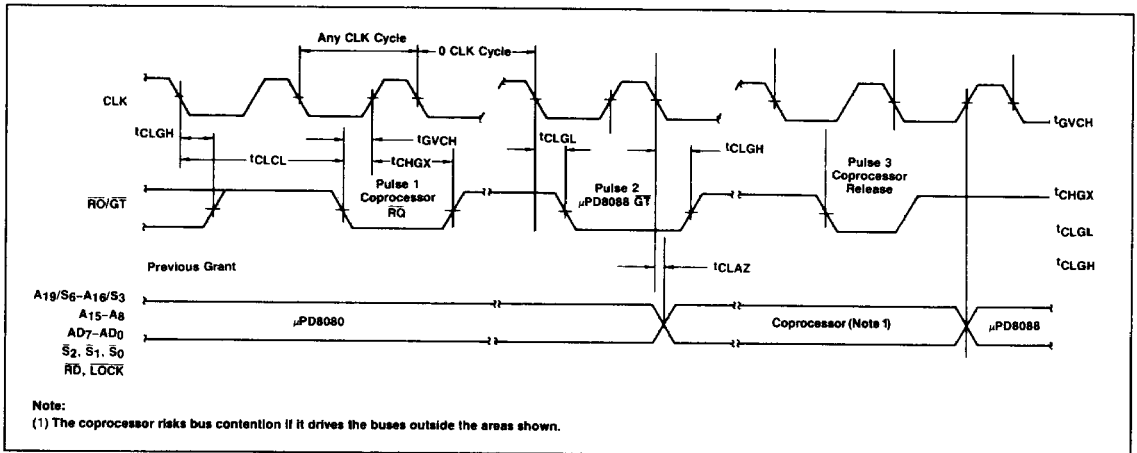


### Maximum Mode Bus Lock Signal Timing



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### Maximum Mode Request/Grant Sequence Timing



Timing Waveforms (cont)

Minimum Mode Hold Acknowledge Timing

