STPMS2

Smart sensor II dual-channel 1-bit, 4 MHz, second-order sigma-delta modulator with embedded PGLNA

Features

- V_{CC} supply range 3.2 V - 5.5 V
- Two second-order sigma-delta ($\Sigma\Delta$) modulators
- Programmable chopper-stabilized low noise and low offset amplifier
- Supports 50-60 Hz, EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-22 and IEC 62053-23 standards specs for class 1, class 0.5 and class 0.2 AC watt meters
- STPM02H: less than 0.5% error over 1:10000 range
- STPM02L: less than 0.5% error over 1:5000 range
- Precision voltage reference: 1.23 V with programmable TC (STPMS2L only)
- Internal low drop regulator @ 3 V (typ.)

Applications

- Power metering
- Motor control
- Industrial process control
- Weight scales
- Pressure transducers

Description

The STPMS2, also called "smart sensor" devices, are ASSPs designed for effective measurement in power line systems utilizing Rogowski coil, current transformer, Hall or shunt sensors. These devices are designed as building blocks for single-phase

QFN16 (4 x 4)
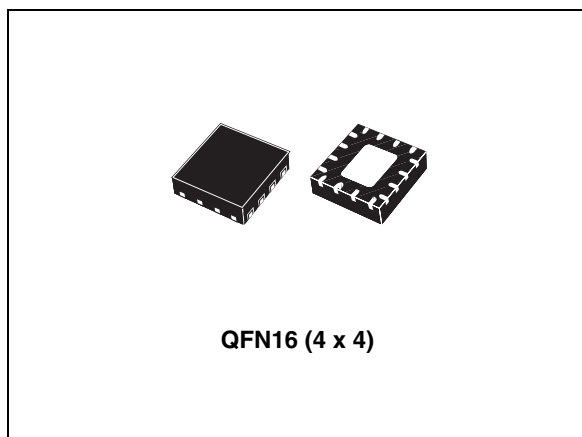
or multi-phase energy meters along with the STPMC1 device, a digital signal processor designed for energy measurement. This device can be used in medium and high resolution measurement applications where single or double inputs must be monitored at the same time. The STPMS2 are mixed signal ICs consisting of an analog and digital section. The analog section consists of a programmable gain, low noise choppered amplifier, two second-order $\Delta\Sigma$ modulator blocks, a band-gap voltage reference, a low-drop voltage regulator and DC buffers, while the digital section consists of a clock generator and output multiplexer.

Table 1.   Device summary

| Order codes	Package	Packaging
STPMS2H-PUR	QFN16 (4 x 4 mm)	4500 parts per reel
STPMS2L-PUR	QFN16 (4 x 4 mm)	4500 parts per reel

Contents

1   Introduction

The STPMS2 is a device designed to measure electrical line parameters (voltage and current) via analog signals from voltage sensors (current divider) and current sensors (inductive Rogowski coil, current transformer or shunt resistors). The device is used together with a digital signal processing circuit to implement an effective measuring system for multi-phase power meters.

The device consists of two analog measuring channels, consisting of second-order sigma-delta modulators with appropriate non-overlapping control signal generator. The STPMS2 also includes a temperature compensated band-gap reference voltage generator, a low-drop supply voltage stabilizer and minimal digital circuitry that includes BIST (built-in self-test) structures. In a current signal processing channel, a low-noise preamplifier is included in front of the sigma-delta converter. All reference voltages (band-gap, AGND) are internally buffered to eliminate channel crosstalk.

The STPMS2 can operate in fast or low-power mode. In fast mode, a nominal clock frequency of 4.1 or 4.9 MHz is applied to the clock input. In this mode, signal bandwidth is specified between 0 and 4 kHz. In low-power mode, the nominal clock is four times slower in order to reduce the power consumption of the circuit. In low-power mode, the quiescent bias currents of the preamplifier and sigma-delta integrators are lowered and the signal bandwidth is narrowed to the frequency bandwidth of 0 to 1 kHz.

2 Internal block diagram

Figure 1. STPMS2 internal block diagram
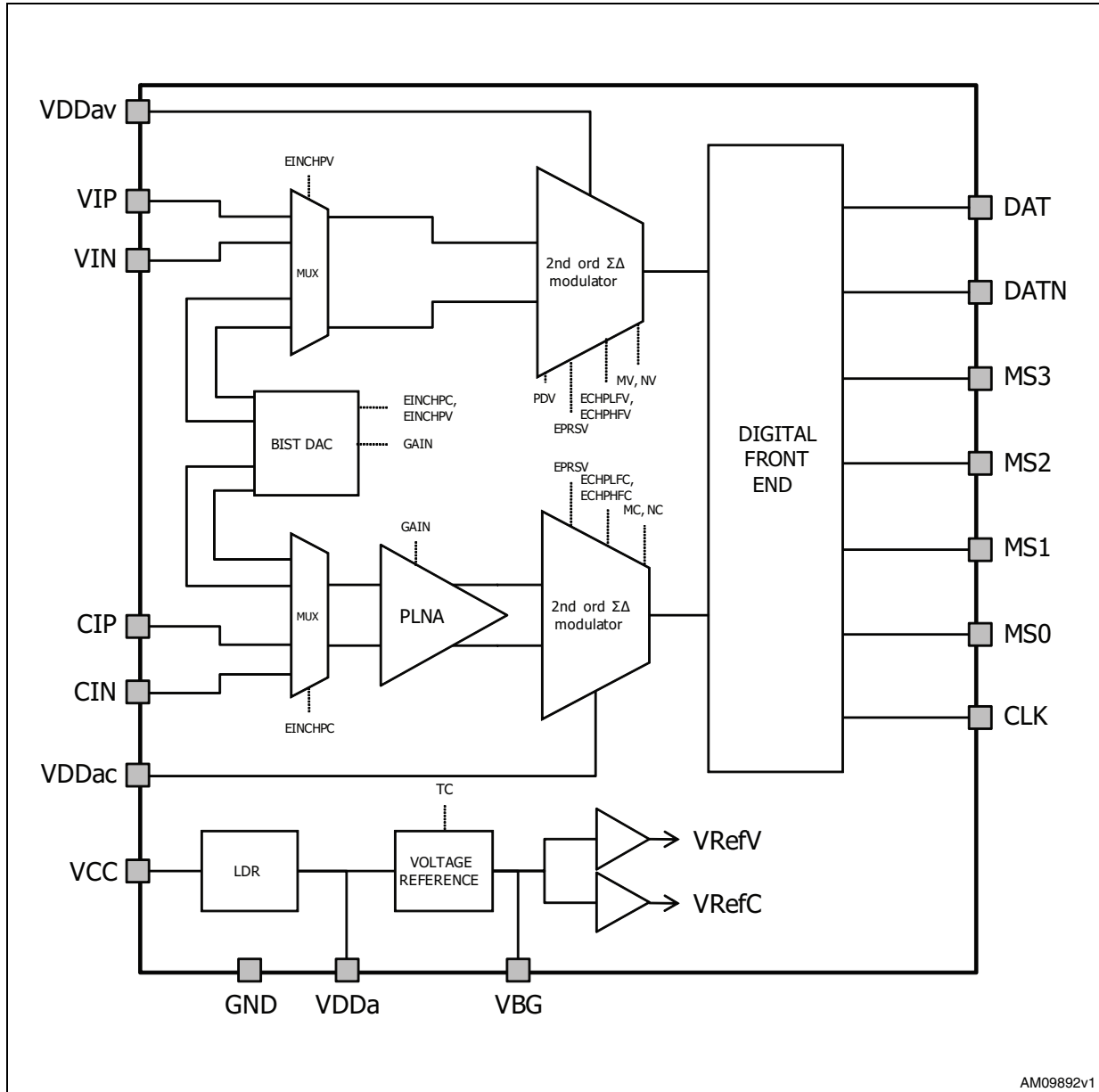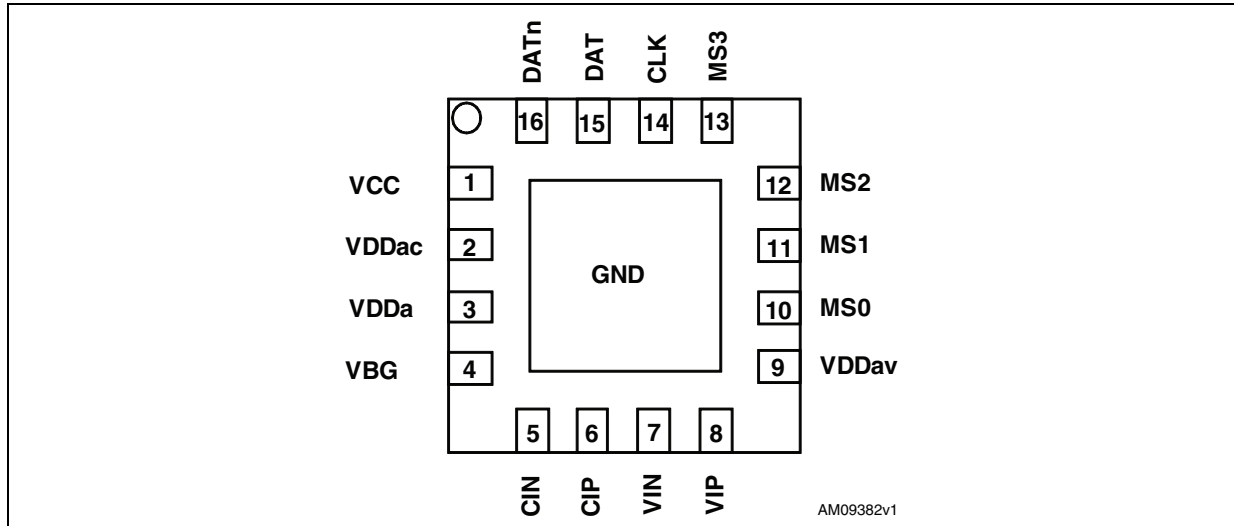
3 Pin configuration

Figure 2. Pin connections

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Table 2. Pin description

Pin n°	Symbol	Description
1	VCC	Unregulated supply voltage for pad-ring, bandgap, low-drop and level shifters
2	VDDac	Current channel modulator supply input
3	VDDa	Output of internal + 3.0 V low drop regulated power supply
4	VBG	Output of internal + 1.23 V bias generator (STPMS2L); Input of external precision reference voltage (STPMS2H)
5	CIN	Current channel -
6	CIP	Current channel +
7	VIN	Voltage channel -
8	VIP	Voltage channel +
9	VDDav	Voltage channel modulator supply input
10	MS0	Input for configurator 0
11	MS1	Input for configurator 1
12	MS2	Input for configurator 2
13	MS3	Input for configurator 3
14	CLK	Input for external measurement clock
15	DAT	Output of multiplexed $\Sigma\Delta$ signal Output of current $\Sigma\Delta$ signal
16	DATn	Output of inverted multiplexed $\Sigma\Delta$ signal Output of voltage $\Sigma\Delta$ signal
Exp PAD	GND	Ground level for signals and pin protection

4 Maximum ratings

Table 3.   Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Input voltage	-0.3 to 6	V
I_{PIN}	Current on any pin (sink/source)	±150	mA
V_{ID}	Input voltage at any pin	-0.3 to V_{CC} +0.3	V
V_{IA}	Input voltage at analog pins (VIP, VIN, IIP, IIN)	-0.7 to 0.7	V
ESD	Human body model (all pins)	±2	kV
T_{OP}	Operating ambient temperature	-40 to 85	°C
T_J	Junction temperature	-40 to 150	°C
T_{STG}	Storage temperature range	-55 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4.   Thermal data

Symbol	Parameter	Value	Unit
R_{thJA} [1]	Thermal resistance junction-ambient	38.66	°C/W

1.   This value is referred to single-layer PCB, JEDEC standard test board.

4.1 General operating conditions

V_{CC} = 5 V, T_{AMB} = 25 °C, 1 µF between V_{CC}, VDDa, VDDac, VDDav and GND, 100 nF between VBG and GND, f_{CLK} = 4.19 MHZ unless otherwise specified.

Table 5.   General operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{CC}	Operating supply voltage		3.135		5.25	V
I_{CC}	Quiescent current	LP, 1.229MHz; V_{CC}=3.3V; C_L=100nF; no loads		1.2	1.5	mA
		HP, 4.915MHz; V_{CC}=3.2V; C_L=100nF; no loads		4	5	
V_{POR}	Power on reset on V_{CC}			2.5		V
V_{DD}	Regulated supply voltage	1.049MHz; V_{CC}=3.2V; C_L=100nF; no loads	2.95	3.00	3.05	V
I_{LATCH}	Current injection latch-up immunity				300	mA
f_{BW}	Effective bandwidth	Limited by chopper	0		4091	Hz
DC measurement accuracy						
	Resolution		11		16	bit
INL	Integral non linearity	Result referred to a 16-bit word of CIP-CIN channel, HP mode, f_{CLK}= 2.047MHz		3.3		LSB
		Result referred to a 12-bit word of VIP-VIN channel, HP mode, f_{CLK}=2.047MHz		3.9		
DNL	Differential linearity	Result referred to a 16-bit word of CIP-CIN channel, HP mode, f_{CLK}=2.047MHz		0.3		LSB
		Result referred to a 12-bit word of VIP-VIN channel, HP mode, f_{CLK}=2.047MHz		0.5		
	Offset error	Result referred to a 16-bit word of CIP-CIN channel, HP mode, f_{CLK}=2.047MHz		0.02		LSB
		Result referred to a 12 bit-word of VIP-VIN channel, HP mode, f_{CLK}=2.047MHz		0.005		
	Gain error	Result referred to a 16-bit word of CIP-CIN channel, HP mode, f_{CLK}=2.047MHz	0.04		0.4	LSB/uV
		Result referred to a 12-bit word of VIP-VIN channel, HP mode, f_{CLK}=2.047MHz		0.003		
NF	Noise floor	CIP-CIN channel gain 2x		120		dB
		CIP-CIN channel gain 16x		118		
		VIP-VIN channel		95		

Table 5.   General operating conditions (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$PSRR_{DC}$	Power supply DC rejection	Voltage signal: 200 mV$_{rms}$/50Hz Current signal: 10 mV$_{rms}$/50Hz f_{CLK}=2.048 MHz V_{CC}=3.3V ±10%, 5V ±10%	90			dB
AC measurement accuracy						
SNR	Signal to noise ratio	CIP-CIN channel – Vin=±230mV @ 55Hz gain 2x over 4 kHz bandwidth		82		dB
		VIP-VIN channel – Vin=±230mV @ 55Hz over 4 kHz bandwidth		52		
SINAD	Signal to noise ratio + distortion	CIP-CIN channel – Vin=±230mV @ 55Hz gain 2x over 4 kHz bandwidth		82		dB
		VIP-VIN channel – Vin=±230mV @ 55Hz over 4 kHz bandwidth		52		
THD	Total harmonic distortion	CIP-CIN channel – Vin=±230mV @ 55Hz gain 2x over 4 kHz bandwidth		-105		dB
		VIP-VIN channel – Vin=±230mV @ 55Hz over 4 kHz bandwidth		-78		
SFDR	Spurious free dynamic range	CIP-CIN channel – Vin=±230mV @ 55Hz gain 2x over 4 kHz bandwidth		90		dB
		VIP-VIN channel – Vin=±230mV @ 55Hz over 4 kHz bandwidth		68		
$PSRR_{AC}$	Power supply AC rejection	Voltage signal: 200 mV$_{rms}$/50Hz Current signal: 10 mV$_{rms}$/50Hz f_{CLK}=2.048 MHz V_{CC}=3.3V+0.2V$_{rms}$1@100Hz V_{CC}=5.0V+0.2V$_{rms}$1@100Hz	120			dB
Analog inputs (CIP, CIN, VIP, VIN)						
V_{MAX}	Maximum input signal levels	VIP-VIN channel	-0.3		+0.3	V
		STPMS2L CIP-CIN channel Gain 2x Gain 4x Gain 8x Gain 16x STPMS2H CIP-CIN channel	-0.3 -0.15 -0.075 -0.0375 -V$_{REF}$/ GAIN		+0.3 +0.15 +0.075 +0.0375 +V$_{REF}$/ GAIN	V
f_{SPL}	A/D sampling frequency			f_{CLK}		Hz
V_{off}	Amplifier offset				±20	mV
Z_{IP}	VIP, VIN impedance	Over total operating voltage range	100		400	kΩ
Z_{IN}	CIP, CIN impedance	Over total operating voltage range	35		50	kΩ
G_{ERR}	Gain error of current channels			±10		%

Table 5.   General operating conditions (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ILV}	Voltage channel leakage current	V_{CC}=5.25V, f_{CLK}=4.19MHz	-1		1	µA
I_{ILI}	Current channel leakage current	V_{CC}=5.25V, f_{CLK}=4.19MHz	-1		1	
		V_{CC}=5.25V, f_{CLK}=4.19MHz input enabled	-10		10	
	Crosstalk between channels			130		dB
Digital I/O (CLK, DAT, DATN, MS0, MS1, MS2, MS3)						
V_{IH}	Input High voltage		0.75V_{CC}		5.3	V
V_{IL}	Input Low Voltage		-0.3		0.25V_{CC}	V
V_{OH}	Output high voltage	I_O=-1mA, C_L=50pF, V_{CC}=3.2V	V_{CC}-0.4			V
V_{OL}	Output low voltage	I_O=+1mA, C_L=50pF, V_{CC}=3.2V			0.4	V
I_{UP}	Pull up current			15		µA
t_{TR}	Transition time	C_{LOAD}=50pF		10		ns
t_L	Latency	From 50% of CLK to 50% to DAT			40	ns
Clock input						
f_{CLK}	Nominal frequencies	Low precision mode	1.0		1.228	MHz
		High precision mode	2.0		2.458	
		Very high precision mode	4.0		4.915	
On chip reference voltage						
V_{REF}	Reference voltage	STPMS2L only [1]	1.21	1.23	1.25	V
Z_{out}	Output impedance		30		200	kΩ
I_L	Maximum load current			0		µA
T_C	Temperature coefficient	After calibration		30	50	ppm/°C

1. This level may be delivered from external source in STPMS2H.

Figure 3.   Timing diagram

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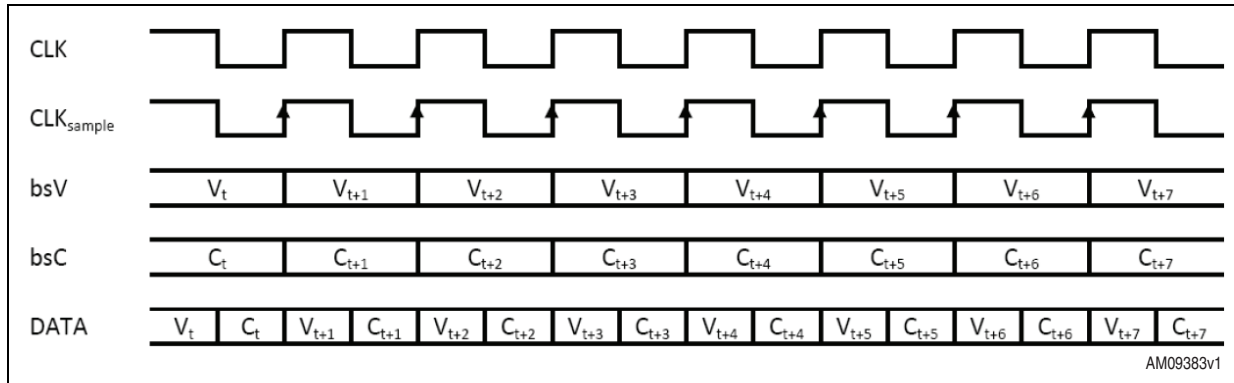
CLK - clock signal on CLK pin

CLK_{sample} - sigma-delta sampling frequency

bsV - sigma-delta bit stream of voltage signal

bsC - sigma-delta bit stream of current signal

DATA - multiplexed data of voltage and current signal on DAT pin

5   Application

The choice of external components in the transduction section of the application is a crucial point in the application design, affecting the precision and the resolution of the entire system.

Among the several considerations, a compromise should be found between the following requirements:

1.   Maximize the signal-to-noise ratio in the voltage and current channel
2.   Choose the current-to-voltage conversion ratio Ks and the voltage divider ratio in a way that calibration can be achieved
3.   Choose Ks to take advantage of the whole current dynamic range in accordance with desired maximum current and resolution.

To maximize the signal-to-noise ratio of the current channel, the voltage divider resistors ratio should be as close as possible to those shown in *Table 6*.

Figure 4 below provides a reference application schematic diagram:

- P = 64000 imp/kWh
- I_{NOM} = 5 A
- I_{MAX} = 60 A

Typical sensitivity values for the current sensors are indicated in *Table 6*.

Figure 4.   Detailed application schematic

Table 6.   Recommended external components in metering applications

Function	Component	Description	Value	Tolerance		Unit
	Calculator	STPMC1	---	---	---	---
Line voltage interface	Resistor divider	R to R ratio V_{RMS}=230V	1:1650	±1%	50ppm/°C	V/V
		R to R ratio V_{RMS}=110V	1:830			
Line current interface	Rogowski coil		0.15	±5%	50ppm/°C	mV/A
	CT	Current-to-voltage ratio K_S	1.7	±5%		
	Shunt		0.43	±5%		

Note: Above listed components refer to typical metering application. Anyhow, STPMS2 operation is not limited to the choice of these external components.

Figure 5.   Simplified application schematics for STPMC1 based energy metering
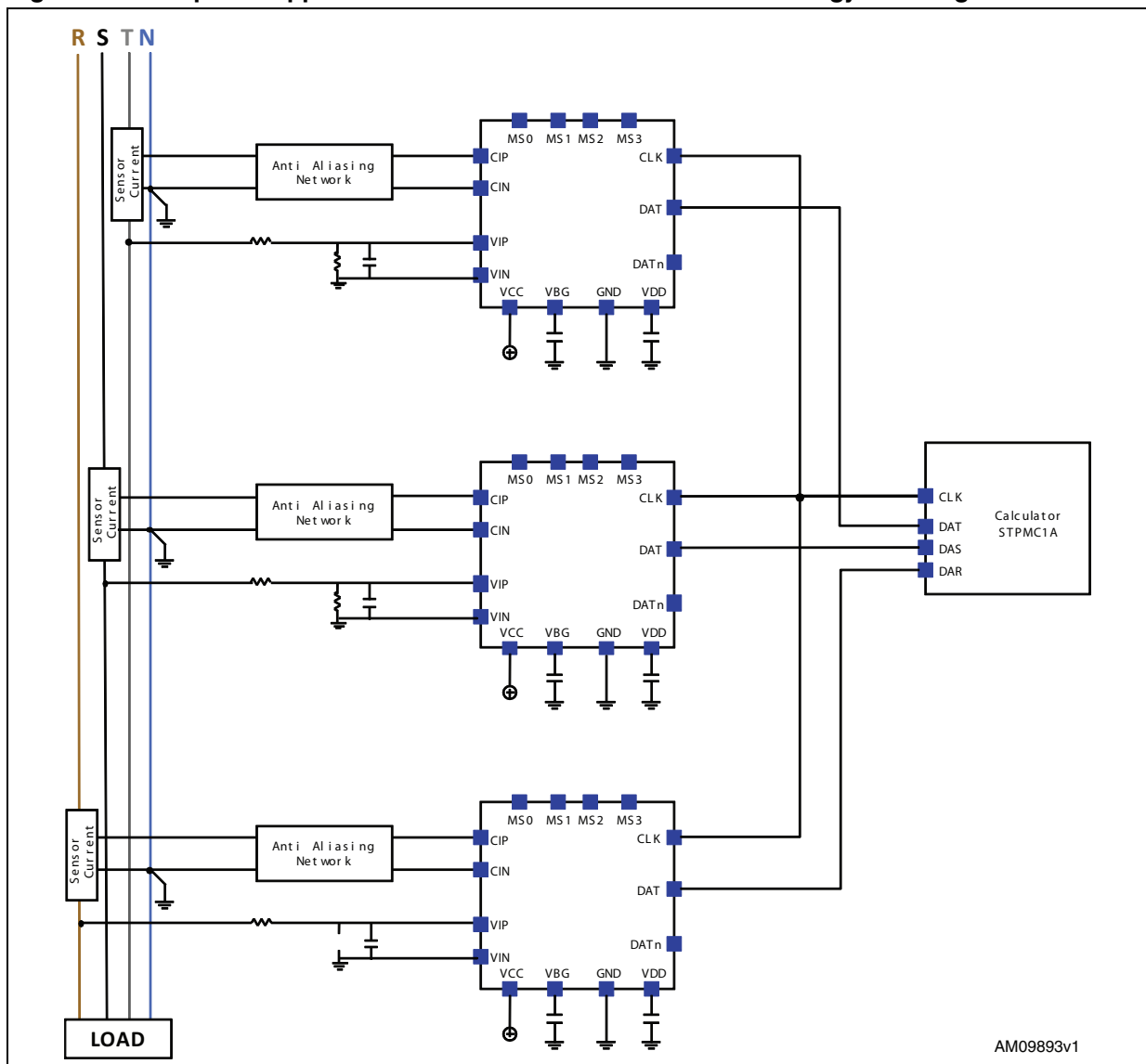
Figure 6. **Connection schematics for DSP-based applications**

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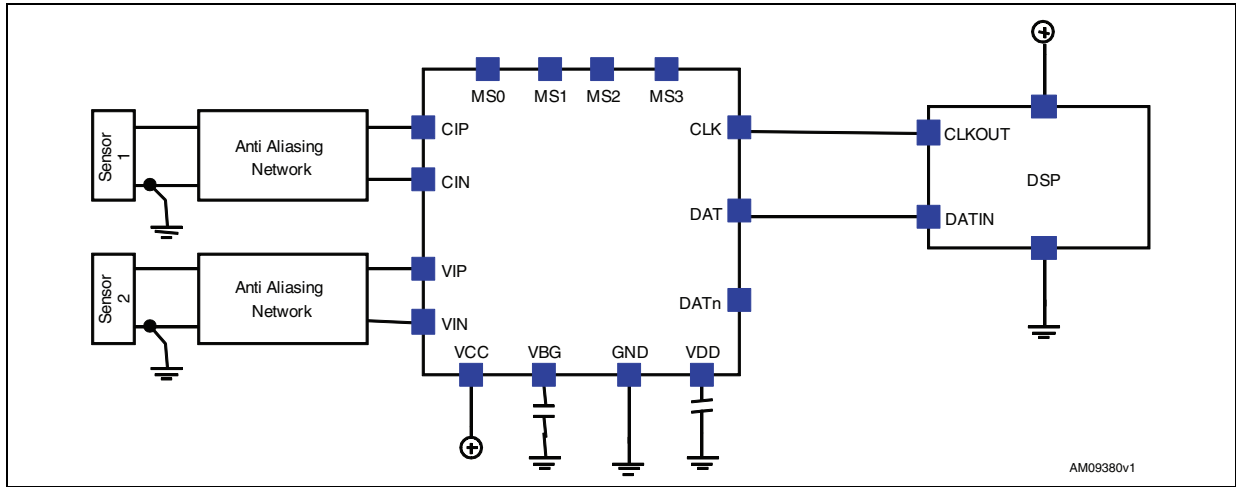
6 Terminology

6.1 Conventions

The lowest analog and digital power supply voltage is called GND which represents the system ground. All voltage specifications for digital input/output pins are referred to GND. The highest power supply voltage is called V_{CC}. The highest core power supply is internally generated and is called V_{DD}.

Positive currents flow into a pin. Sinking current means that the current is flowing into the pin and thus it is positive. Sourcing current means that the current is flowing out of the pin and thus it is negative.

A positive logic convention is used in all equations.

6.2 Notation

Output bit streams of the modulator are indicated as bsV and bsC for voltage and current channels, respectively.

7 Typical performance characteristics

Figure 7. V_{REF}/V_{REF} at 25 deg vs. temp
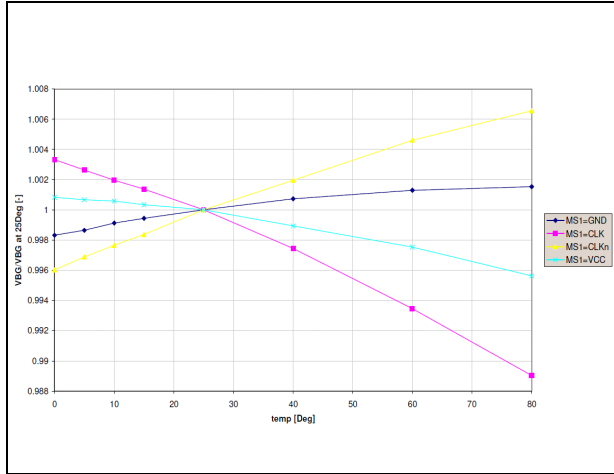
Figure 8. SNHR of I channel, gain 16x
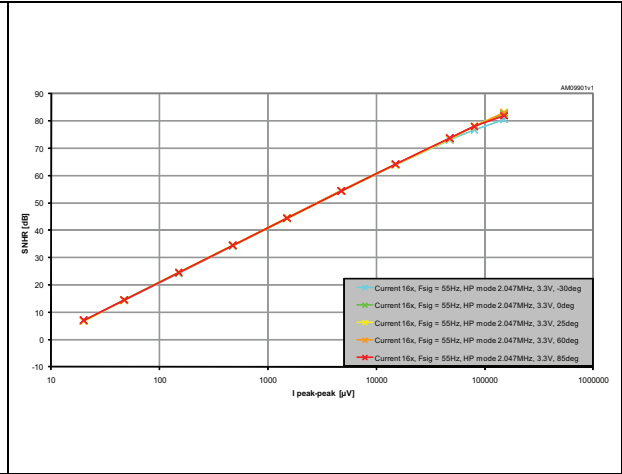
Figure 9. SNHR of I channel, gain 2x
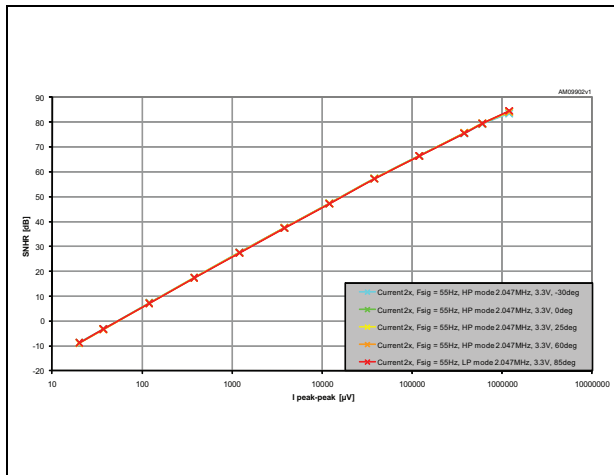
Figure 10. SNHR of V channel, gain 2x
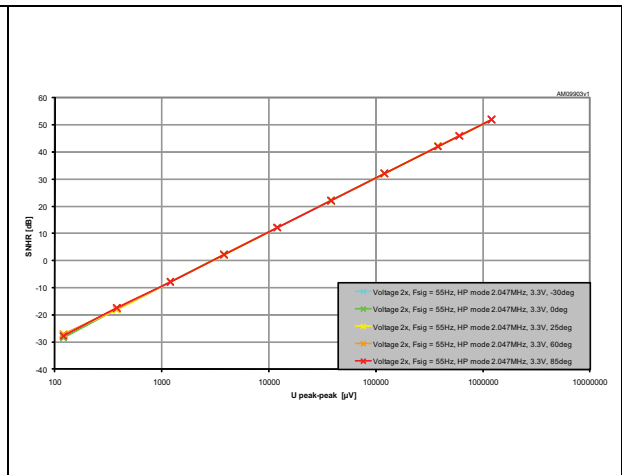
Figure 11. SINAD of I channel, gain 16x (temp. variation)
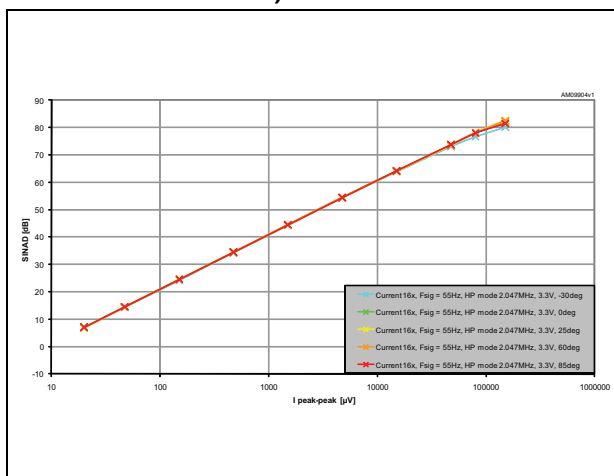
Figure 12. SINAD of I channel, gain 16x (temp. variation)
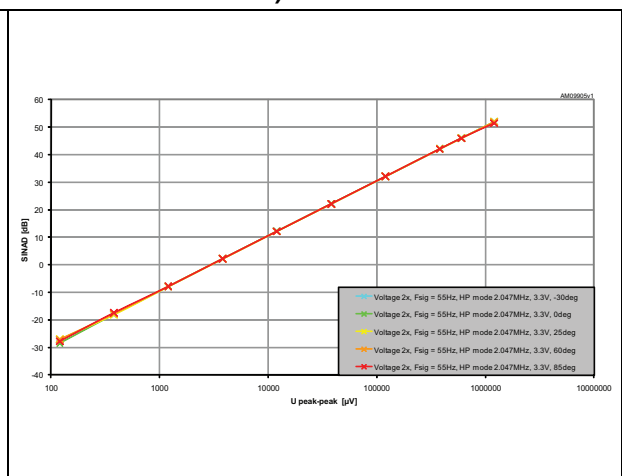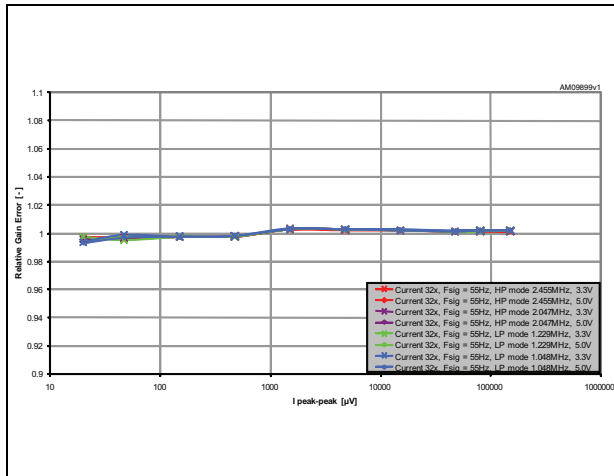
Figure 13. Relative gain error of I channel, gain 16x
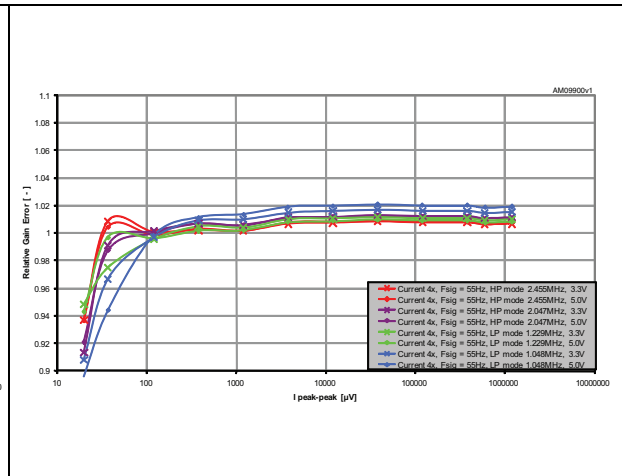

Figure 14. Relative gain error of I channel, gain 2x

Figure 15. Accuracy over dynamic range
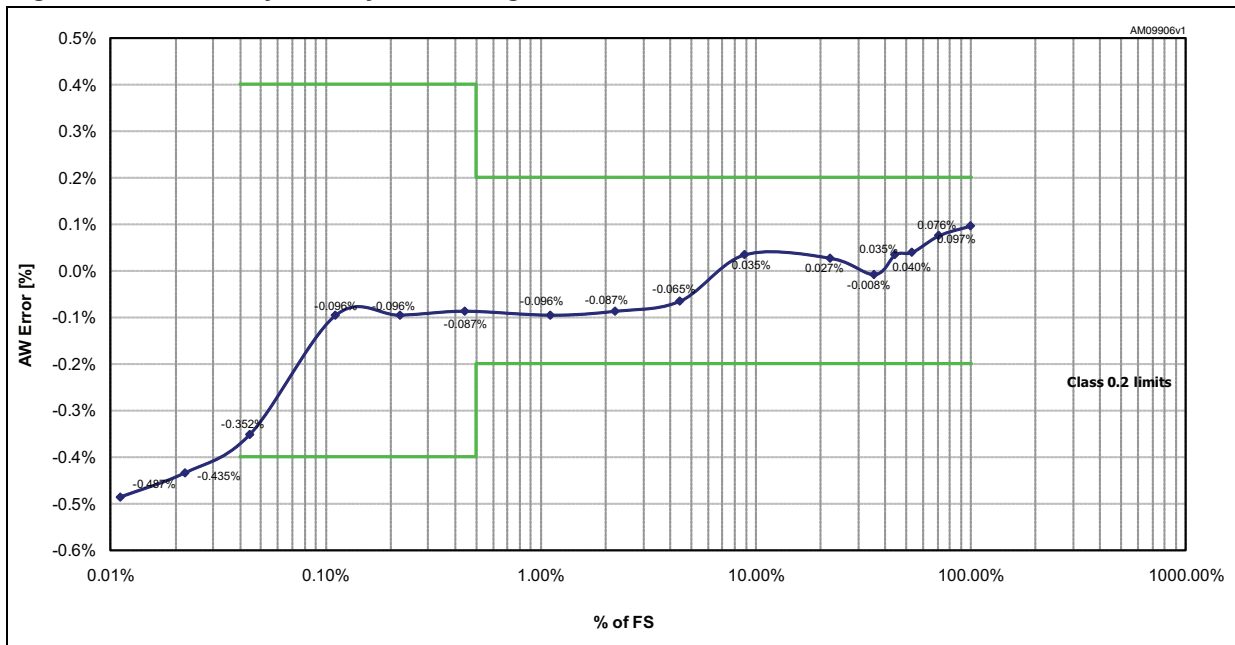
8   Theory of operation

8.1   General operation description

The STPMS2 performs second-order analog modulation of two channels in parallel, with appropriate non-overlapping control signal generator, of signals with frequencies varying from DC to 4 kHz on two independent channels in parallel. The outputs of the converters provide two streams of digital ones and zeros which can be then be multiplexed in time to reduce the number of external connections.

The STPMS2 converts analog signals on two independent channels in parallel via delta-sigma ($\Sigma\Delta$) analog-to-digital converters into a binary stream of sigma-delta signals. The device is particularly suitable to measure electrical line parameters (voltage and current) via analog signals from voltage sensors (current divider) and current sensors (inductive Rogowski coil, current transformer or shunt resistors). There is a current channel for measuring line current and a voltage channel for measuring line voltage. The current channel input is connected through an external anti-aliasing RC filter to a Rogowski coil, current transformer (CT) or shunt current sensor which converts line current into an appropriate voltage signal. The current channel includes a low-noise voltage preamplifier with programmable gain. The voltage channel is connected directly through a resistor voltage divider and anti-aliasing filter to a line voltage modulator (ADC). Both channels have quiescent zero signal point at GND, so the STPMS2 is able to sample differential signals on both channels with their zero point around GND.

The converted $\Sigma\Delta$ signals are multiplexed in time in order to reduce the number of external connections. The conversion and the multiplex are driven by external clock signal CLK.

The device is used in conjunction with a digital signal processing circuit to implement an effective measuring system of a multi-phase power meter.

The STPMS2 also includes a temperature compensated band-gap reference voltage generator, low-drop supply voltage regulator and minimal digital circuitry that includes BIST (built-in self-test) structures. In a current signal processing channel, a low-noise preamplifier is included upstream of the sigma-delta converter. All reference voltages are designed to eliminate channel crosstalk.

The STPMS2 can operate in fast (HP) or low-power (LP) mode (see also *Table 7*). In fast mode, a nominal clock frequency of up to 4.1 / 4.9 MHz is applied to the clock input. In this mode, signal bandwidth is specified between 0 and 4 kHz. In low-power mode, the nominal clock is four times slower (1 MHz) to lower the power consumption of the circuit. In low-power mode, the quiescent bias currents of the preamplifier and sigma-delta integrators are reduced and the signal bandwidth is narrowed to the frequency bandwidth of 0 to 1 kHz.

The mode of operation and configuration of the device can be selected by wiring configuration pins (MS0, MS1, MS2 and MS3) to V_{CC}, GND, CLK or NCLK signal. This approach can be used to change the settings of a current channel, sigma-delta stream output mode and temperature compensation curve of an internal band-gap reference. These pins can act as a serial port to change the configuration of the device.

8.2   Functional description of the analog part

The supply pins for the analog part are VCC, VDDa, VDDac, VDDav, VBG and GND.

The GND pin also represents a reference point. The VDDa is an analog I/O pin of the internal +3.0 V low drop voltage regulator and the VDDac and VDDav are the modulator

supply inputs. A 1 µF capacitor should be connected between VDDxx and GND. The input of the regulator is VCC, which also powers the band-gap and bias generators. The band-gap output is VBG, which should be connected to GND via a 100 nF capacitor.

Figure 16. Power supply external connection scheme
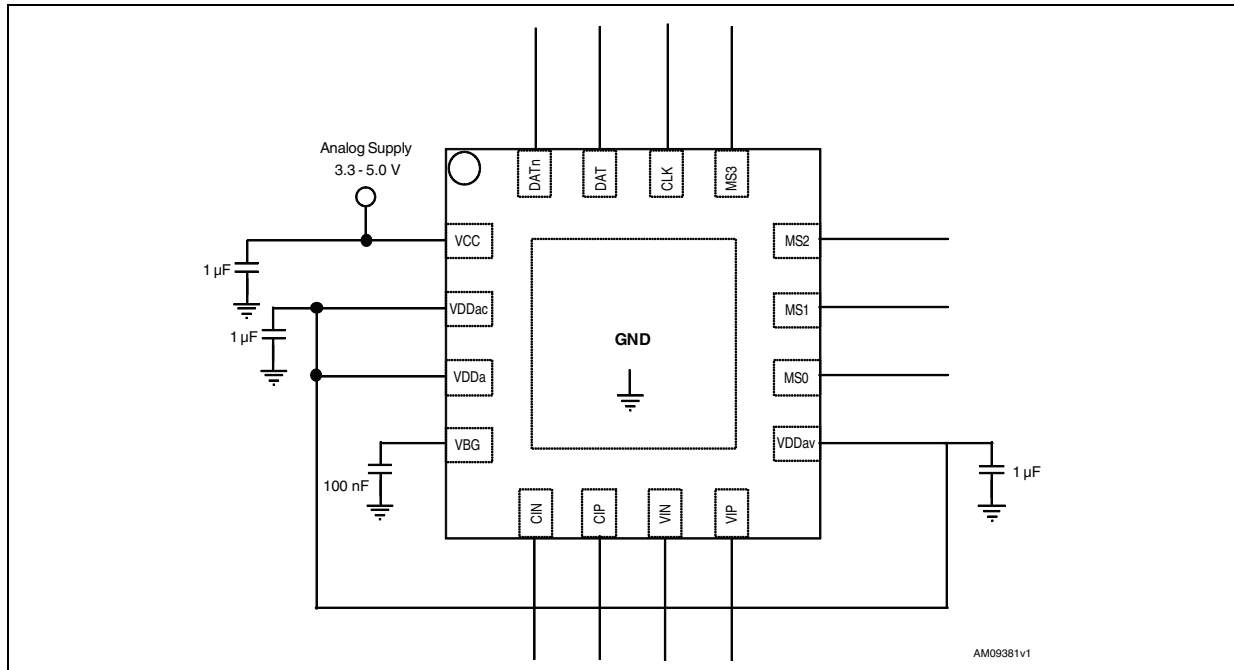
The analog part of the STPMS2 consists of:

● pre-amplifier in the current channel

● 1.23 V reference voltage generator (STPMS2L only)

● +3 V low-drop supply voltage regulator

● two sigma-delta 2nd order modulators

● BIST DAC

● AGND and V_{REF} reference buffers

● bias current generators

The voltage channel has a pre-amplification gain of 2, which defines the maximum differential voltage on voltage channel inputs to ± 300 mV. The relative gain of the current channel is selectable among 2, 4, 8 or 16, which defines the maximum differential voltage on the current channel to ± 300 mV, ± 150 mV, ± 75 mV or ± 37.5 mV, respectively. The full range of gains is available only in soft mode (see *Section 8.5*), while in hard mode only 2 and 16 are selectable.

The temperature-compensated reference voltage generator produces V_{REF} = 1.23 V. This generator is implemented as a band gap generator, whose temperature compensation curve can be selected through configuration.

The low drop regulator fixes and stabilizes the core supply voltage to VDDa = 3 V. All digital pads tolerate 5 V logic levels.

The STPMS2 is clocked by an external clock signal connected to pin CLK.

The STPMS2L sigma-delta modulators work in several operating modes, shown in *Table 7* below.

Table 7.   Operating modes

Operating mode		Device	f_{CLK}	Current consumption
LP (low power)	**LPR** (low precision)	STPMS2L	1 MHZ	1,2 mA typ
HP (fast)	**HPR** (high precision)	STPMS2L	2 MHz – 4MHz	4 mA typ
	HHPR (very high precision)	STPMS2H	4 MHz	

LPR (low precision): f_{CLK} = 1 MHz and settings defined by MS0 through MS3

HPR (high precision): the normal mode of operation with f_{CLK} = 2 MHz to 4 MHz

The STPMS2H sigma-delta modulators work in the following mode:

HHPR (very high precision) external reference must be connected to VBG, f_{CLK} = 4 MHz.

The STPMS2 performs operations in 2 basic modes: Hard mode and Soft mode.

In Hard mode the configuration is set through external pins MS0, MS1, MS2 and MS3.

In Soft mode, 40 configuration bits can be accessed through CFG[39:0], via serial communication. The pins used for serial communication are: MS0, MS1 and MS2.

Switching between Hard and Soft modes is achieved through pin MS3.

● **Hard mode**: In this case the device configuration is bootstrapped at startup and signals come from VIN and VIP for voltage channels, and CIP and CIN for current channels or from internal BIST DAC.

● **Soft mode**: In this mode all possible settings from Hard mode are accessible, as well as the additional settings described in *Section 8.5*.
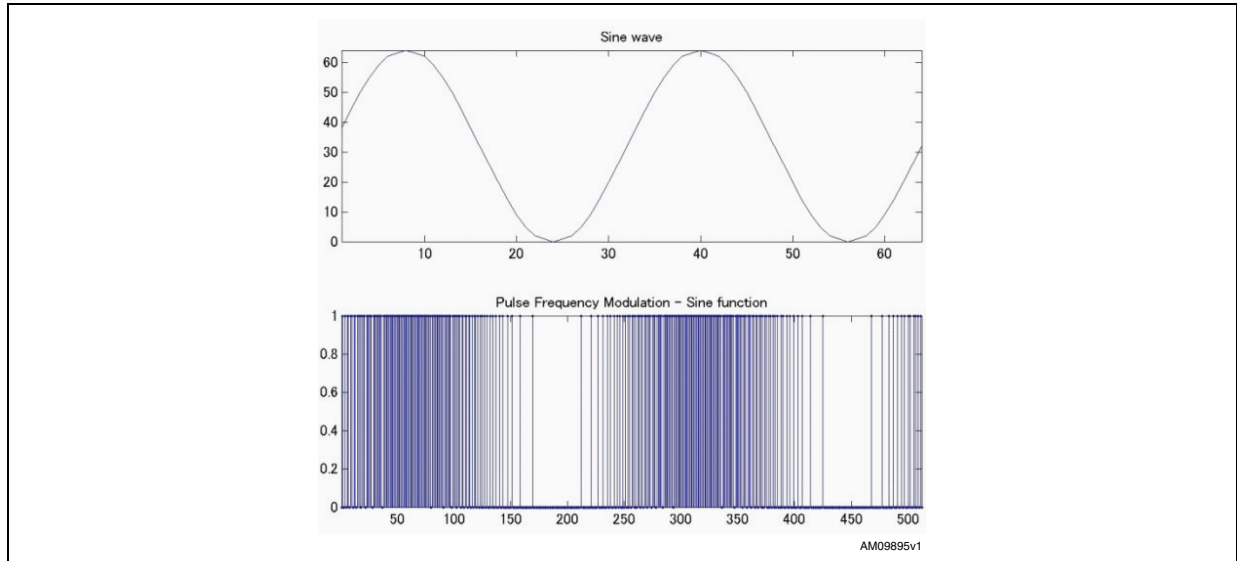
Figure 17.   Block diagram of the modulator
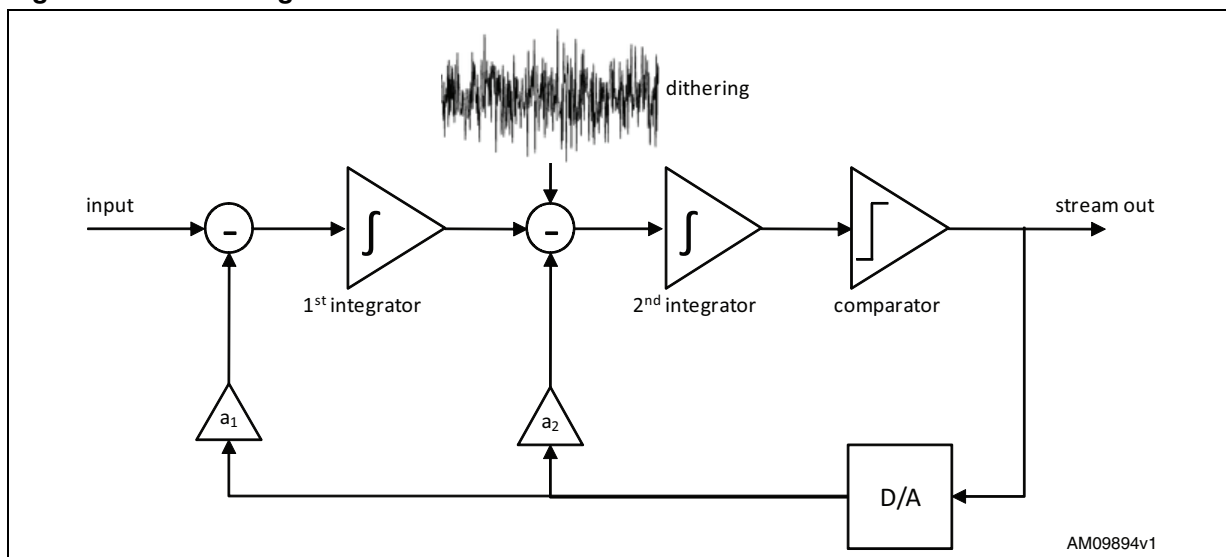
The STPMS2 sends to the DAT and DATn pins selected signals based on the configuration used.

Both outputs have cross-current and slew rate limiters to prevent excessive current spikes on supply lines.

Figure 18. Example of sigma-delta modulator output in case of sinusoidal waveform
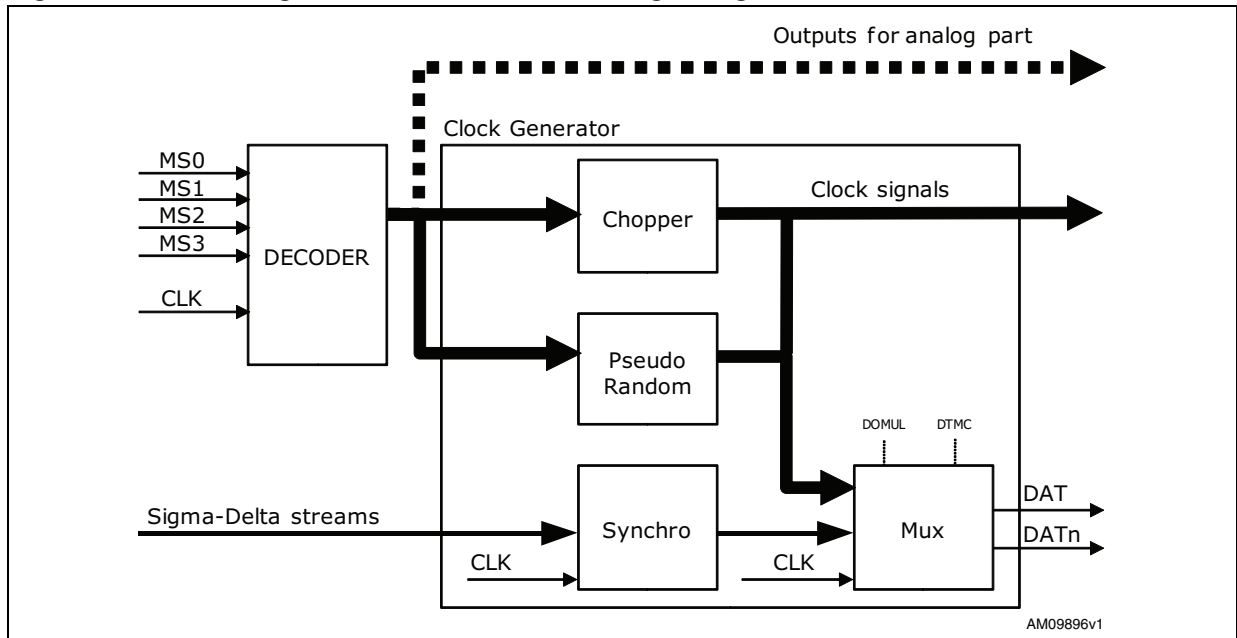

8.3 Functional description of the digital part

The digital section (DFE) includes:

● a decoder for different modes of operation

● a generator for clock frequency

● level shifters, pull-up stages and power buffers outside the DFE block

Figure 19. Block diagram and definition of DFE digital signals

8.3.1 Decoder for different modes of operation

The decoder defines the operating mode according to the state of the bootstrap MS0, MS1, MS2 and MS3 pins. Two different operational modes can be defined:

● Hard mode: In this case the device configuration is bootstrapped at startup and signals come from VIN and VIP for voltage channels, and CIP and CIN for current channels or from internal BIST DAC.

● Soft mode: In this mode all possible settings from Hard mode are accessible, as well as additional settings such as dither and chopper signal frequencies and operation (see *Section 8.5*).

8.3.2 Generator for clock frequency

Chopper and BIST frequency generator

The Chopper block generates the chopper frequencies and BIST signals for the voltage and current channels. The BIST DAC output levels are appropriately adjusted for the current channel according to the gain selection, while for the voltage channel the max DC voltage is used.

The levels are 300 mV for the voltage channel and 300 mV / 150 mV / 75 mV / 37.5 mV for the current channel, in accordance with gain settings 2/4/8/16, respectively, when operating in Soft mode, while 300 mV / 37.5 mV based on gain settings 2/16 when operating in Hard mode.

Pseudo random

The Pseudo random block generates pseudo random signals for the voltage and current channels. These random signals are used to implement a dithering technique to de-correlate the output of the modulators and avoid accumulation points on the frequency spectrum.

Synchro

In Synchro block the synchronization of sigma-delta input streams with strobe signals from analog part and clock signal is performed.

Mux

In the Mux block, which signals are connected to output pins DAT and DATn are selected.

In HardMode, the output signals are selected by input pin MS2.

In SoftMode, the output signals are selected by 8 configuration bits.

8.4 Hard mode

The STPMS2 operates in Hard mode when input pin MS3 is connected to GND or VCC, as described in *Table 11*.

In Hard mode, the STPMS2 has four digital input pins (MS0, MS1, MS2 and MS3) to configure the basic operating parameters:

● BIST DAC enable

● temperature curve of reference voltage

● current and voltage channels settings

● output mode settings

In this way it is possible to access 128 different combinations, which are controlled through pins MS0, MS1, MS2 and MS3.

MS0 sets the operating mode and amplifier gain selection as described in *Table 8*.

For the STPMS2L:

● MS0=GND or CLK to select LPR (low precision); f_{CLK} = 1 MHz is the typical input clock frequency and low power mode is selected.

● MS0=NCLK or VCC to select HPR (high precision): f_{CLK} = 2 MHz is the typical input clock frequency and accuracy is enhanced.

For the STPMS2H, LPR mode is not used and the settings should be chosen between MS0=NCLK or VCC. In this case, f_{CLK} = 4 MHz is typical.

The relative gain of the current channel is selectable between 2 or 16, which defines the maximum differential voltage on the current channel to ± 300 mV or ± 37.5 mV, respectively. The voltage channel gain setting is fixed at 2, which defines the maximum differential voltage on the voltage channel inputs to ± 300 mV.

Table 8.   Precision mode and input amplifier gain selection

MS0	Mode	Description
GND	0	LPR, amplifier GAIN selection g3 = 16
CLK	1	LPR, amplifier GAIN selection g0 = 2
NCLK	2	HPR, amplifier GAIN selection g0 = 2
VCC	3	HPR, amplifier GAIN selection g3 = 16

MS1 defines the temperature compensation (TC) curve of the internal voltage reference of the STPMS2L, as described in *Table 9*. This bootstrap function is not used with the STPMS2H. The temperature-compensated reference voltage generator produces V_{REF} = 1.23 V. This generator is implemented as a band gap generator, whose temperature compensation curve can be selected through the MS1 configuration pin.

Table 9.   TC of the band-gap reference

MS1	Mode	Description
GND	0	TC = 60 ppm/°C
CLK	1	Flattest TC = +30 ppm/°C
NCLK	2	TC = +160 ppm/°C
VCC	3	TC = -160 ppm/°C

MS2 defines the outputs of the device:

The STPMS2 sends to the DAT and DATn pins the sigma-delta streams synchronous to the CLK signal. The output mode can be configured according to *Table 10* as follows:

● The output current channel's sigma-delta stream on DAT and the voltage channel's sigma-delta stream on DATn

● Output multiplexed signals, so when CLK = 0, the current channel output sigma-delta value is set on the DAT pin, and when CLK = 1, the voltage channel output sigma-delta value is set on the DAT pin. The DATn pin tracks DAT, so DATn = ~DAT.

● Output current channel's sigma-delta stream on DAT and the current channel's sigma-delta stream negated on DATn

Table 10.   Control of voltage channel and output signals

MS2	Mode	Description
GND	0	Voltage channel ON, DATn = ~ [DAT =(CLK) ? bsV : bsC)]
CLK	1	Voltage channel OFF, DATn = bsCn, DAT = bsC
NCLK	2	Voltage channel OFF, DATn = bsCn, DAT = bsC
VCC	3	Voltage channel ON, DATn = bsC, DAT = bsV

MS3 enables or disables the BIST DAC output levels.

If enabled (MS3=VCC), the input of the modulators are disconnected from pin VIP, VIN and CIP, and CIN, and connected to the output of BIST DAC which generates 2 different levels appropriately adjusted for the current channel 300 mV / 37.5 mV depending on gain settings 2/16, while for the voltage channel, 300 mV is used. This mode is used as auto diagnostic methodology of good behavior of the two modulators.

When disabled (MS3=GND), the input of the modulators comes from pins VIP, VIN and CIP, and CIN. This is the normal operating condition.

Table 11.   Selection of Hard, Soft or Test mode and enable of BIST

MS3	Mode	Description
GND	0	HardMode, BIST mode OFF
CLK	1	Soft mode
NCLK	2	Reserved
VCC	3	HardMode, BIST mode ON

8.5   Soft mode

The STPMS2 switches to Soft mode when MS3 is connected to CLK. In Soft mode, input pins MS0, MS1 and MS2 control the serial communication port, as described in *Table 12*. This way, all settings of the 40 internal configuration bits can be changed. The old values remain in the registers until they are overwritten.

Table 12.   Pins for SPI communication

Pin	Function	Description
MS0	SCL	Clock input
MS1	TDI	Data input
MS2	TDS	Enable
MS3	CLK	SPI operation

Table 13. Description of output signals and configuration bits CFG[39:0]

Hard mode	Soft mode	Internal signal	Description
MS0	CFG[0]	LP/HP	Operating mode: LP/HP=0: LPR LP/HP=1: HPR
MS0	CFG[1]	GAIN	Gain selector of current channel pre-amplifier: GAIN=0: x2
MS0	CFG[2]		GAIN=1: x4 GAIN=2: x8 GAIN=3: x16
MS1	CFG[3]	TC	Temperature compensation of voltage reference: TC=0: TC = 60 ppm/°C
MS1	CFG[4]		TC=1: Flattest TC = +30 ppm/°C TC=2: TC = +160 ppm/°C TC=3: TC = -160 ppm/°C
MS2	CFG[5]	DOMUL	Output multiplexer enable: DOMUL=0: outputs not multiplexed DOMUL=1: outputs multiplexed
MS2	CFG[6]	PDV	Power-down of voltage modulator: PDV=0: Voltage modulator on PDV=1: Voltage modulator off

MS3	CFG[7]	EBISTC	Current modulator BIST DAC enable:
			EBISTC=0: BISTC disabled
			EBISTC=1: BISTC enabled
			– EBISTC Frequency output
			    0 0
			    1 $CLK/2^{15}$ x LFC

MS3	CFG[8]	EBISTV	Voltage modulator BIST DAC enable:
			EBISTC=0: BISTV disabled
			EBISTC=1: BISTV enabled
			– EBISTV Frequency output
			    0 0
			    1 $CLK/2^{15}$ x LFV

MS3	CFG[9]	EINCHPC	CIP, CIN input pin enable: EINCHPC=0: CIN CIP disabled EINCHPC=1: CIN CIP enabled
MS3	CFG[10]	EINCHPV	VIP, VIN input pin enable: EINCHPC=0: VIN VIP disabled EINCHPC=1: VIN VIP enabled
1	CFG[11]	ECHPLFC	Low frequency chopper of current modulator enable: ECHPLFC=0: LFC disabled ECHPLFC=1: LFC enabled [1]

**Table 13.   Description of output signals and configuration bits CFG[39:0] (continued)**

Hard mode	Soft mode	Internal signal	Description

1	CFG[12]	MC	LFC of current channel frequency selector:
			– MC[2:0] Frequency
			  000 CLK/1024
			  001 [1] CLK/512
			  010 CLK/256
			  011 CLK/128
			  100 CLK/64
			  101 [2] CLK/64
			  110 [2] CLK/64
			  111 [2] CLK/64

0	CFG[13]		
0	CFG[14]		
1	CFG[15]	ECHPHFC	High Frequency Chopper of current modulator enable: ECHPHFC=0: HFC disabled ECHPHFC=1: HFC enabled [1]

1	CFG[16]	NC	HFC of current channel frequency selector
			– NC[2:0] Frequency
			  000 [2] CLK/256
			  001 [2] CLK/128
			  010 CLK/256
			  011 [1] CLK/128
			  100 CLK/64
			  101 CLK/32
			  110 CLK/16
			  111 CLK/8

1	CFG[17]		
0	CFG[18]		
1	CFG[19]	ECHPLFV	Low Frequency Chopper of voltage modulator enable: ECHPLFV=0: LFV disabled ECHPLFV=1: LFV enabled [1]

1	CFG[20]	MV	LFC of voltage channel frequency selector:
			– MV[2:0] Frequency
			  000 CLK/1024
			  001 [1] CLK/512
			  010 CLK/256
			  011 CLK/128
			  100 CLK/64
			  101 [2] CLK/64
			  110 [2] CLK/64
			  111 [2] CLK/64

0	CFG[21]		
0	CFG[22]		
1	CFG[23]	ECHPHFV	High Frequency Chopper of voltage modulator enable: ECHPHFC=0: HFV disabled ECHPHFC=1: HFV enabled [1]

Table 13. Description of output signals and configuration bits CFG[39:0] (continued)

Hard Mode	Soft mode	Internal signal	Description
1	CFG[24]	NV	HFC of voltage channel frequency selector: – NV[2:0] Frequency 000 [2] CLK/256 001 [2] CLK/128 010 CLK/256 011 [1] CLK/128 100 CLK/64 101 CLK/32 110 CLK/16 111 CLK/8
1	CFG[25]		
0	CFG[26]		
1	CFG[27]	EPRSC	Current modulator pseudo random signals enable: EPRSC=0: PRSC disabled EPRSC=1: PRSC enabled [1]
1	CFG[28]	EPRSV	Voltage modulator pseudo random signals enable: EPRSV=0: PRSV disabled EPRSV=1: PRSV enabled [1]
0	CFG[29]	-	Reserved
0	CFG[30]	-	Reserved
0	CFG[31]	-	Reserved
0	CFG[32]	DTMC	DAT and DAT output signal selector: – DTMC[5:0] pdV domul DAT DATn 00XXXX 0 0 bsV bsC 00XXXX 0 1 (bsV,bsC) (bsVn,bsCn) 00XXXX 1 0 bsC bsCn 00XXXX 1 1 bsC bsCn 01XX00 0 0 bsV LFC 01XX01 0 1 (bsV,bsC) HFC 01XX10 1 0 bsC BISTC 01XX11 1 1 bsC PRSC 1000XX 0 0 LFV bsC 1001XX 0 1 HFV (bsVn,bsCn) 1010XX 1 0 BISTV bsCn 1011XX 1 1 PRSV bsCn 110000 X X LFV LFC 110101 X X HFV HFC 111010 X X BISTV BISTC 111111 X X PRSV PRSC
0	CFG[33]		
0	CFG[34]		
0	CFG[35]		
0	CFG[36]		
0	CFG[37]		
0	CFG[38]	-	Reserved
0	CFG[39]	-	Reserved

1. Default value for Hard mode

2. Combinations not used

8.5.1   Writing to the configuration register in Soft mode

All 40 configuration bits must be overwritten.

Figure 20.   Timings to switch to Soft mode after POR
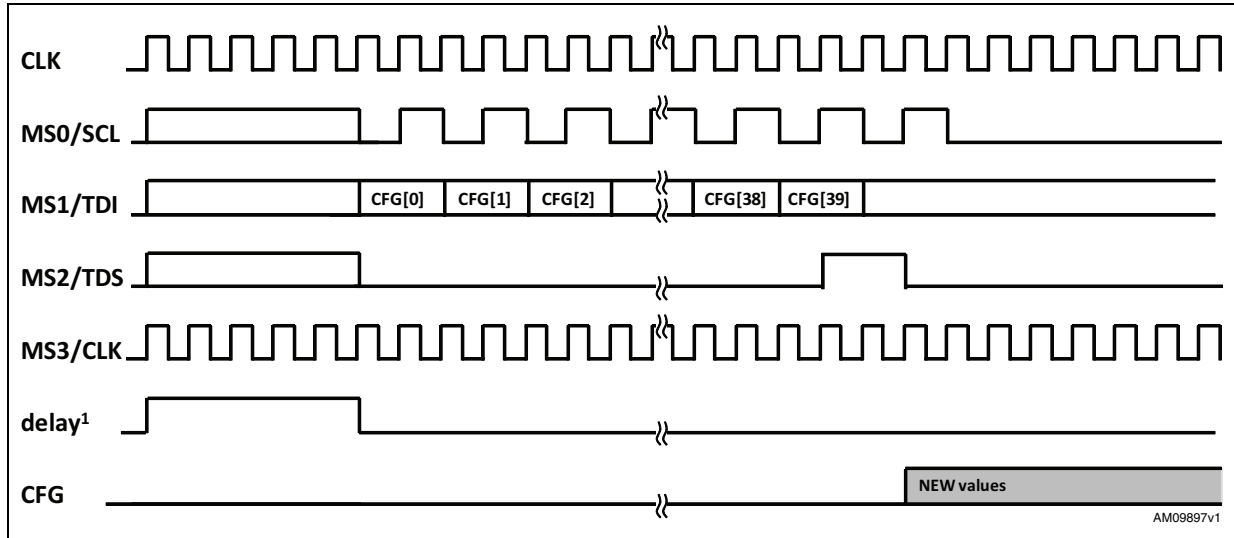
1.   After power-on reset, Soft mode is selected (MS3=CLK), the bits MS0 .. MS2 must be stable at least 5*CLK

Figure 21.   Timings to switch to Soft mode
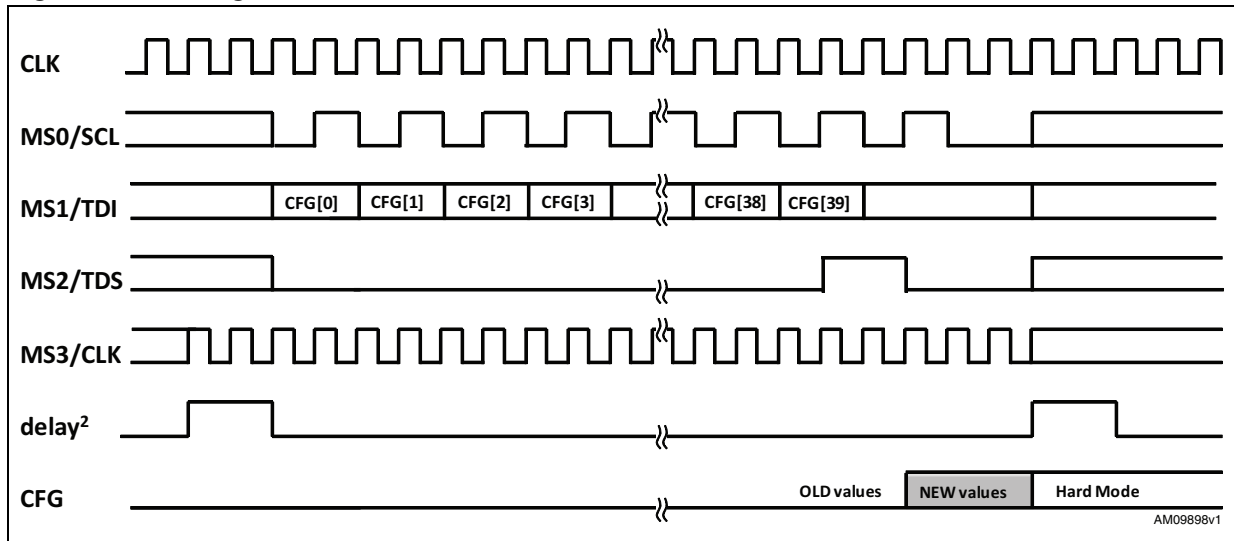
2.   After switching into Soft mode (MS3=CLK), the bits MS0 .. MS2 must be stable at least 2*CLK. The same rule applies when switching from Soft mode to Hard mode: MS0 .. MS2 must be stable at least 2*CLK

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 14. QFN16 (4 x 4 mm.) mechanical data

Dim.	mm.		
	Min.	**Typ.**	**Max.**
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	3.90	4.00	4.10
D2	2.50		2.80
E	3.90	4.00	4.10
E2	2.50		2.80
e		0.65	
L	0.30	0.40	0.50

Figure 22. QFN16 (4 x 4 mm.) drawing

7571203_A
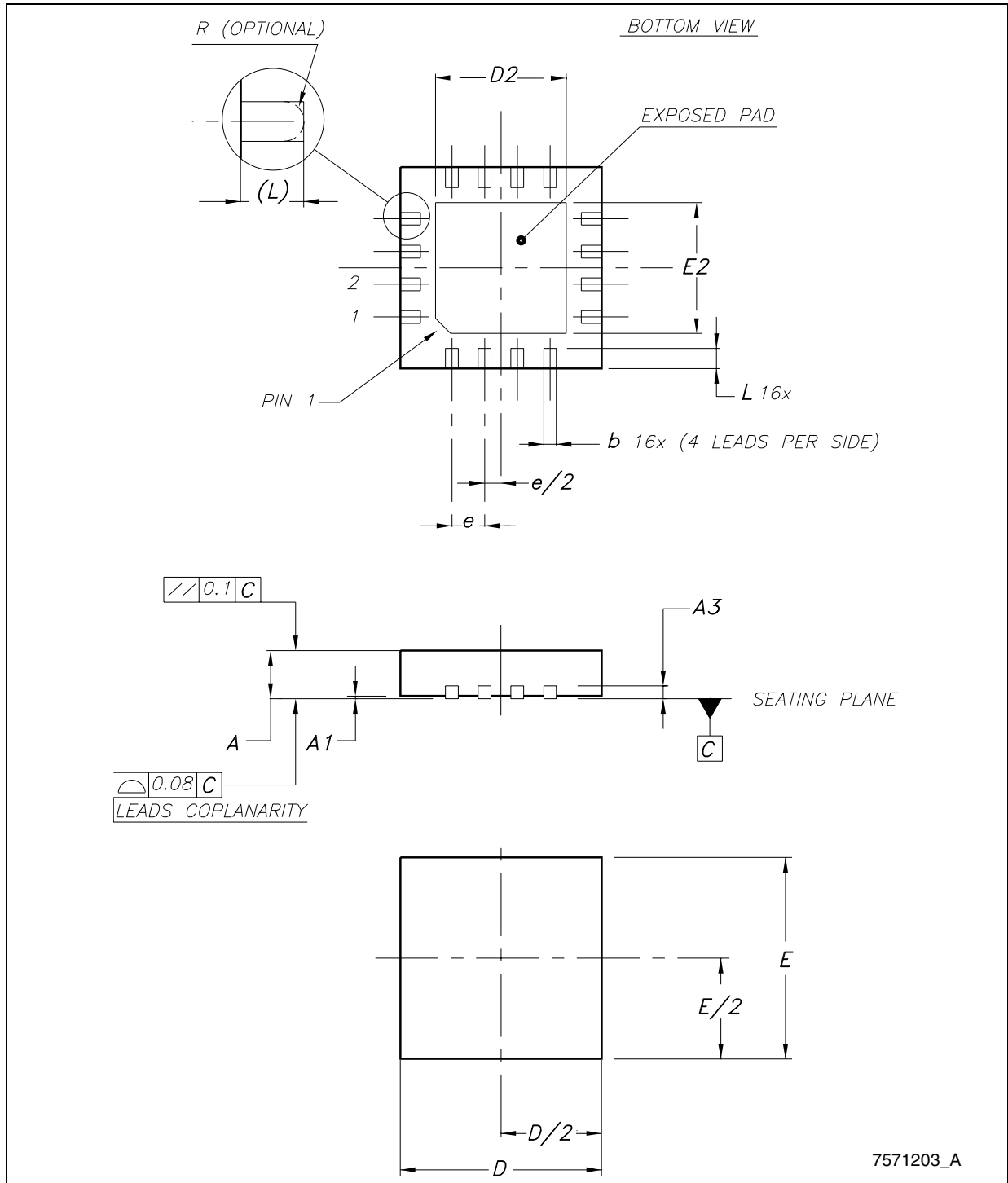
Tape & reel QFNxx/DFNxx (4x4) mechanical data

Dim.	mm.			inch.		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99		101	3.898		3.976
T			14.4			0.567
Ao		4.35			0.171	
Bo		4.35			0.171	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	

Note: Drawing not in scale
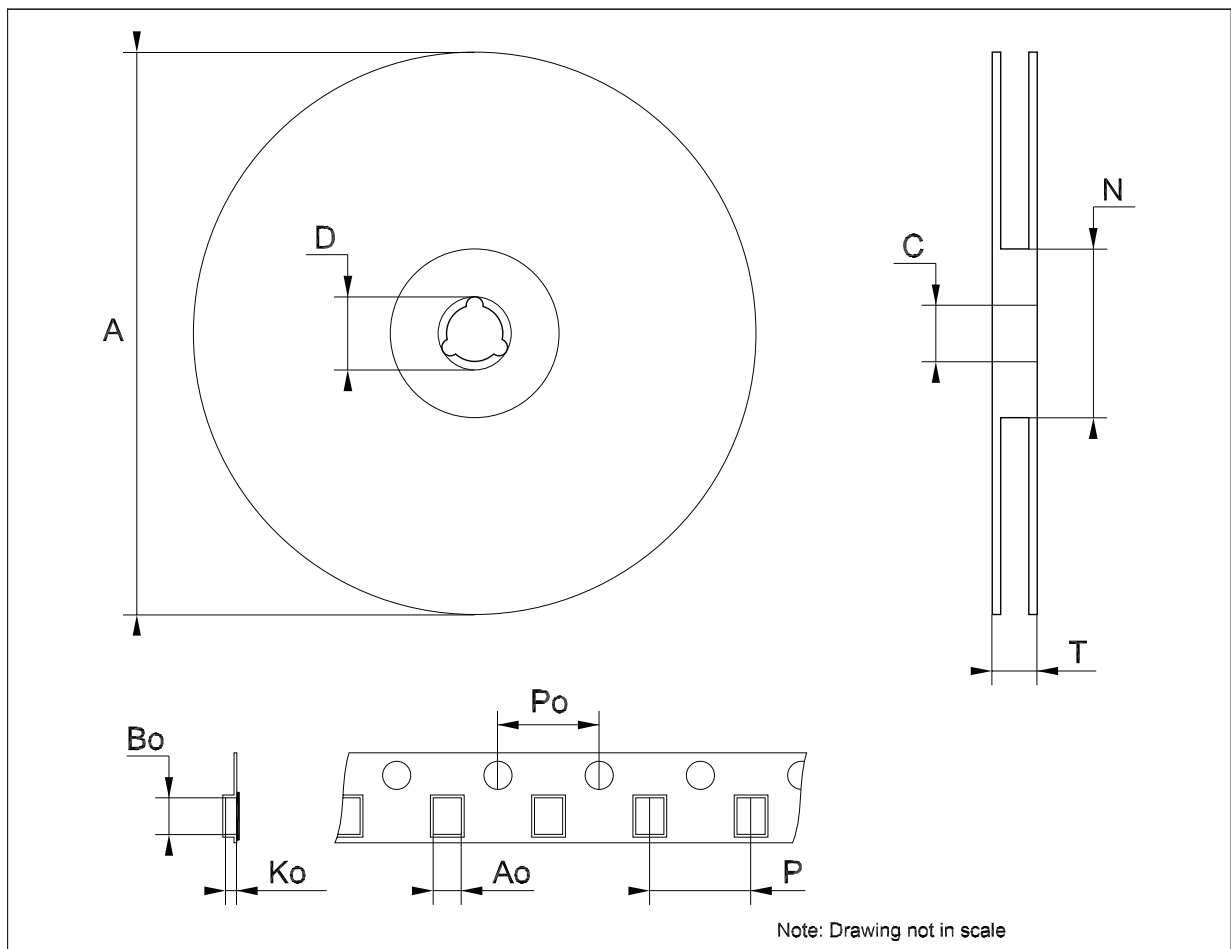
Figure 23.   QFN16 (4 x 4) footprint recommended data (dimension in mm.)
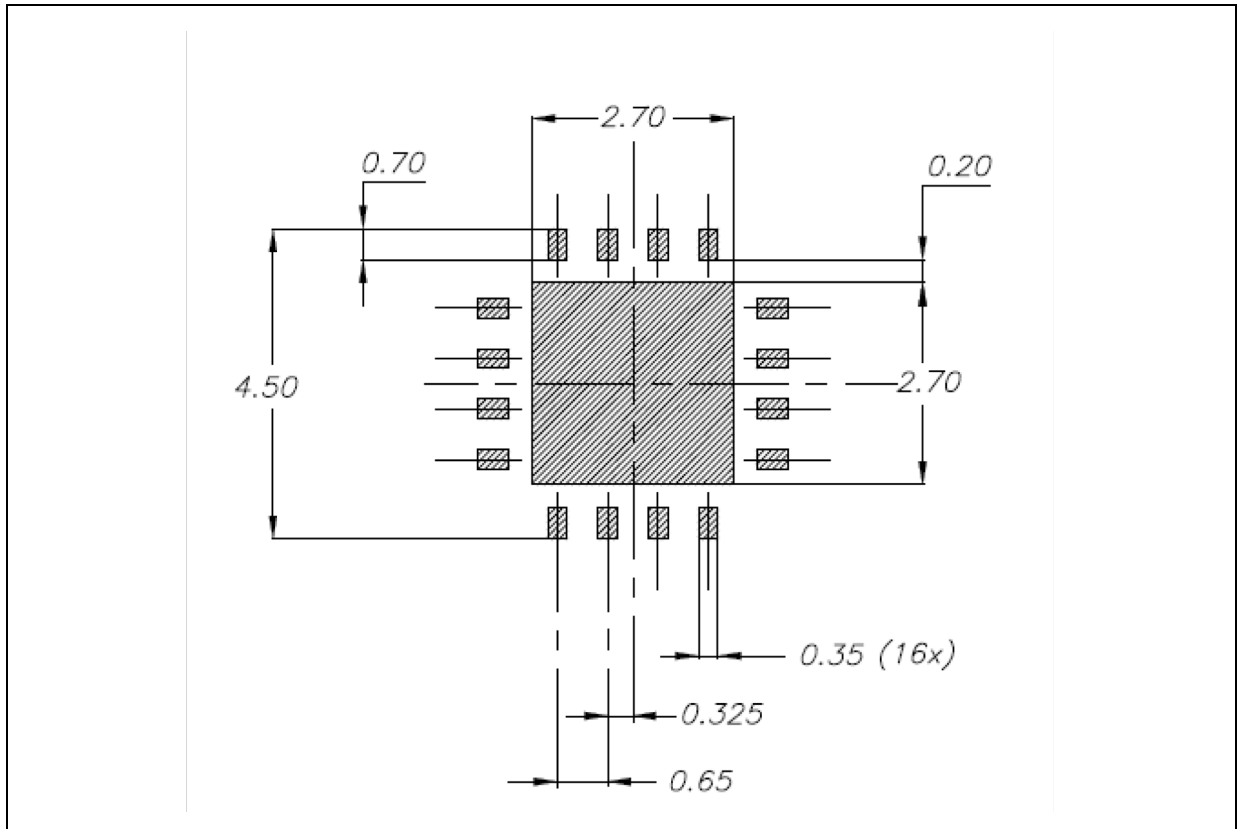
10   Revision history

Table 15.   Document revision history

Date	Revision	Changes
23-Oct-2009	1	Initial release.
06-Jul-2011	2	Document status promoted from preliminary data to datasheet.
11-Oct-2011	3	Modified: 100 µF ==> 100 nF *Section 8.2 on page 17*.