

### Military Linear Products

#### DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

#### FEATURES

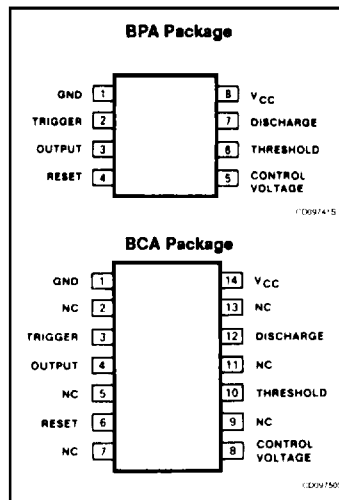
- Turn-off time less than 2 $\mu$ s
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours

- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per  $^{\circ}$ C

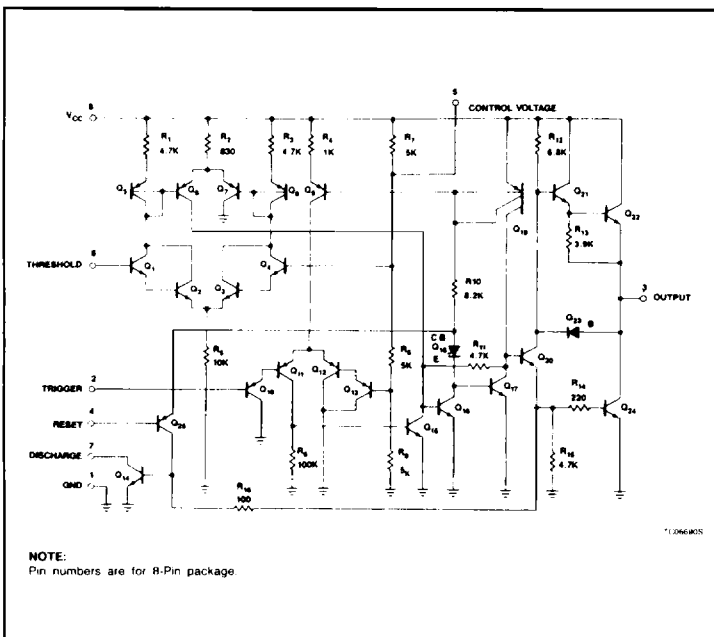
#### APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

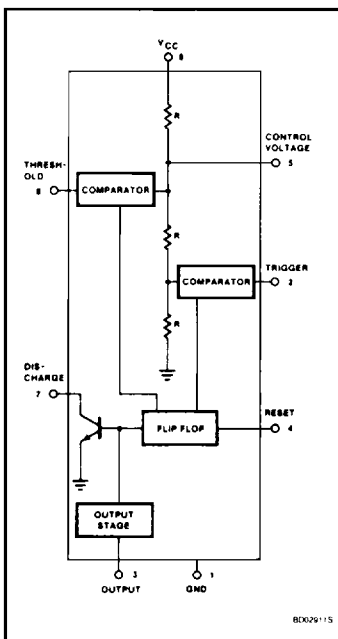
#### PIN CONFIGURATION



#### EQUIVALENT SCHEMATIC



#### BLOCK DIAGRAM



## Timer

555

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	555/BCA
8-Pin Ceramic DIP	555/BPA

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING <sup>1</sup>	UNIT
V <sub>CC</sub>	Supply voltage	+18	V
P <sub>D</sub>	Power dissipation	600	mW
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS V<sub>CC</sub> = +5V to V<sub>CC</sub> = +15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	T <sub>A</sub> = +25°C			T <sub>A</sub> = -55°C, +125°C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	Supply voltage		4.5		18	4.5		18	V
I <sub>CC</sub>	Supply current (low state) <sup>2</sup>	V <sub>CC</sub> = 5V, R <sub>L</sub> = ∞		3	5			6	mA
		V <sub>CC</sub> = 15V, R <sub>L</sub> = ∞		10	12			14	mA
t <sub>M</sub>	Timing error (monostable)	R <sub>A</sub> = 2kΩ to 100kΩ							
	Initial accuracy <sup>3</sup>	C = 0.1μF		0.5	2.0			2.5	%
Δt <sub>M</sub> /ΔT	Drift with temperature <sup>7,8</sup>							100	ppm/°C
Δt <sub>M</sub> /ΔV <sub>S</sub>	Drift with supply voltage			0.05	0.2			0.25	%/V
t <sub>A</sub>	Timing error (astable)	R <sub>A</sub> , R <sub>B</sub> = 1kΩ to 100kΩ							
	Initial accuracy <sup>3</sup>	C = 0.1μF		4	6			10.0	%
Δt <sub>A</sub> /ΔT	Drift with temperature <sup>7</sup>	V <sub>CC</sub> = 15V						500	ppm/°C
Δt <sub>A</sub> /ΔV <sub>S</sub>	Drift with supply voltage <sup>9</sup>			0.15	0.6			1.5	%/V
V <sub>C</sub>	Control voltage level	V <sub>CC</sub> = +15V	9.6	10.0	10.4	9.6		10.4	V
		V <sub>CC</sub> = +5V	2.9	3.33	3.8	2.9		3.8	V
V <sub>TH</sub>	Threshold voltage	V <sub>CC</sub> = +15V	9.4	10.0	10.6	9.4		10.6	V
		V <sub>CC</sub> = +5V	2.7	3.33	4.0	2.4		4.0	V
I <sub>TH</sub>	Threshold current <sup>4</sup>	V <sub>TH</sub> = 10.6V		0.1	0.25			0.35	μA
V <sub>TRIG</sub>	Trigger voltage	V <sub>CC</sub> = +15V	4.8	5.0	5.2	4.5		5.5	V
		V <sub>CC</sub> = +5V	1.45	1.67	1.9	1.5		2.2	V
I <sub>TRIG</sub>	Trigger current	V <sub>TRIG</sub> = 0V		0.5	0.9			2.0	μA
V <sub>RESET</sub>	Reset voltage <sup>5</sup>		0.4		1.0	0.1		1.3	V
I <sub>RESET</sub>	Reset current	V <sub>RESET</sub> = 0.4V		-0.1	-0.4			-0.6	mA
I <sub>RESET</sub>	Reset current	V <sub>RESET</sub> = 0V		-0.4	-1.0			-1.2	mA
V <sub>OL</sub>	Output voltage (low) <sup>10</sup>	V <sub>CC</sub> = +15V		0.1	0.15			0.25	V
		I <sub>SINK</sub> = 10mA		0.4	0.5			0.70	V
		I <sub>SINK</sub> = 100mA		2.0	2.2			2.6	V
		V <sub>CC</sub> = +5V		0.1	0.25			0.43	V
		I <sub>SINK</sub> = 5mA		0.05	0.2			0.38	V
V <sub>OH</sub>	Output voltage (high) <sup>10</sup>	V <sub>CC</sub> = +15V	13.0	13.3		12.5			V
		I <sub>SOURCE</sub> = 100mA	3.0	3.3		2.6			V
I <sub>D</sub>	Discharge leakage current			20	100			500	nA

## Timer

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**AC ELECTRICAL CHARACTERISTICS**  $V_{CC} = +5V$ ,  $V_{CC} = +15V$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	$T_A = +25^\circ C$			$T_A = -55^\circ C, +125^\circ C$			UNIT
			Min	Typ	Max	Min	Typ	Max	
$t_{OFF}$	Turn-off time <sup>6,7</sup>	$V_{RESET} = V_{CC}$		0.5	2.0				$\mu s$
$t_R$ $t_F$	Rise time of output <sup>7</sup> Fall time of output <sup>7</sup>			100 100	200 200				ns ns

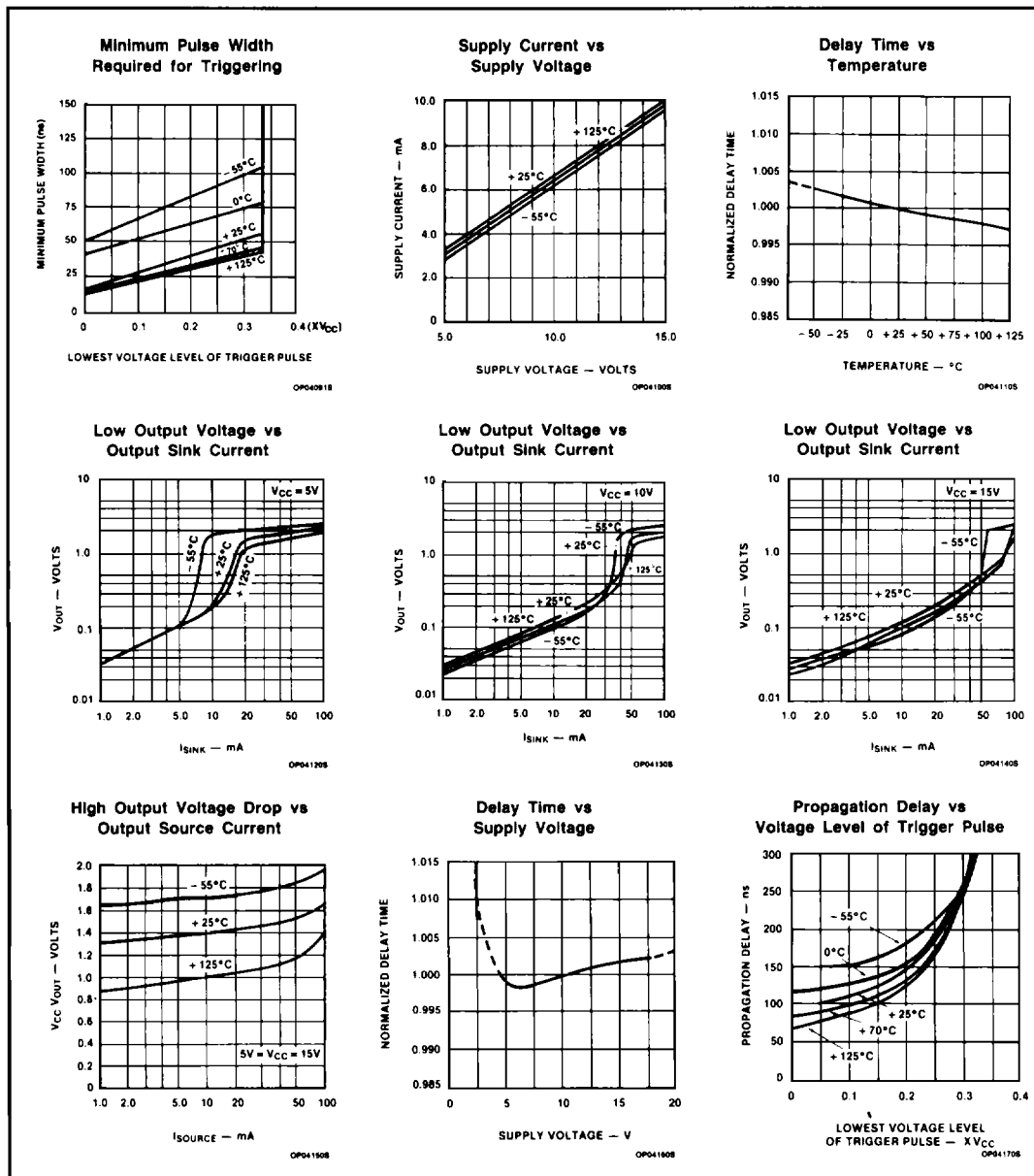
**NOTES:**

1. Operation beyond the limits in this table may impair the useful life of the device.
2. Supply current when output high typically 1mA less.
3. Tested at  $V_{CC} = +5V$  and  $V_{CC} = +15V$ .
4. This will determine the max. value of  $R_A + R_B$ , for 15V operation, the max. total  $R = 10M\Omega$ , and for 5V operation, the max. total  $R = 3.4M\Omega$ .
5. Specified with trigger input high.
6. Time measured from a positive going input pulse from 0 to  $0.8 \times V_{CC}$  into the threshold to the drop from high to low of the output. Trigger is tied to threshold.
7. This parameter is guaranteed but not tested.
8. Testing performed at  $R_A = 100k\Omega$  only.
9. Testing performed at  $R_A = R_B = 1k\Omega$  only.
10. For long term static operation, derate the sink and source currents to 50mA maximum.

## Timer

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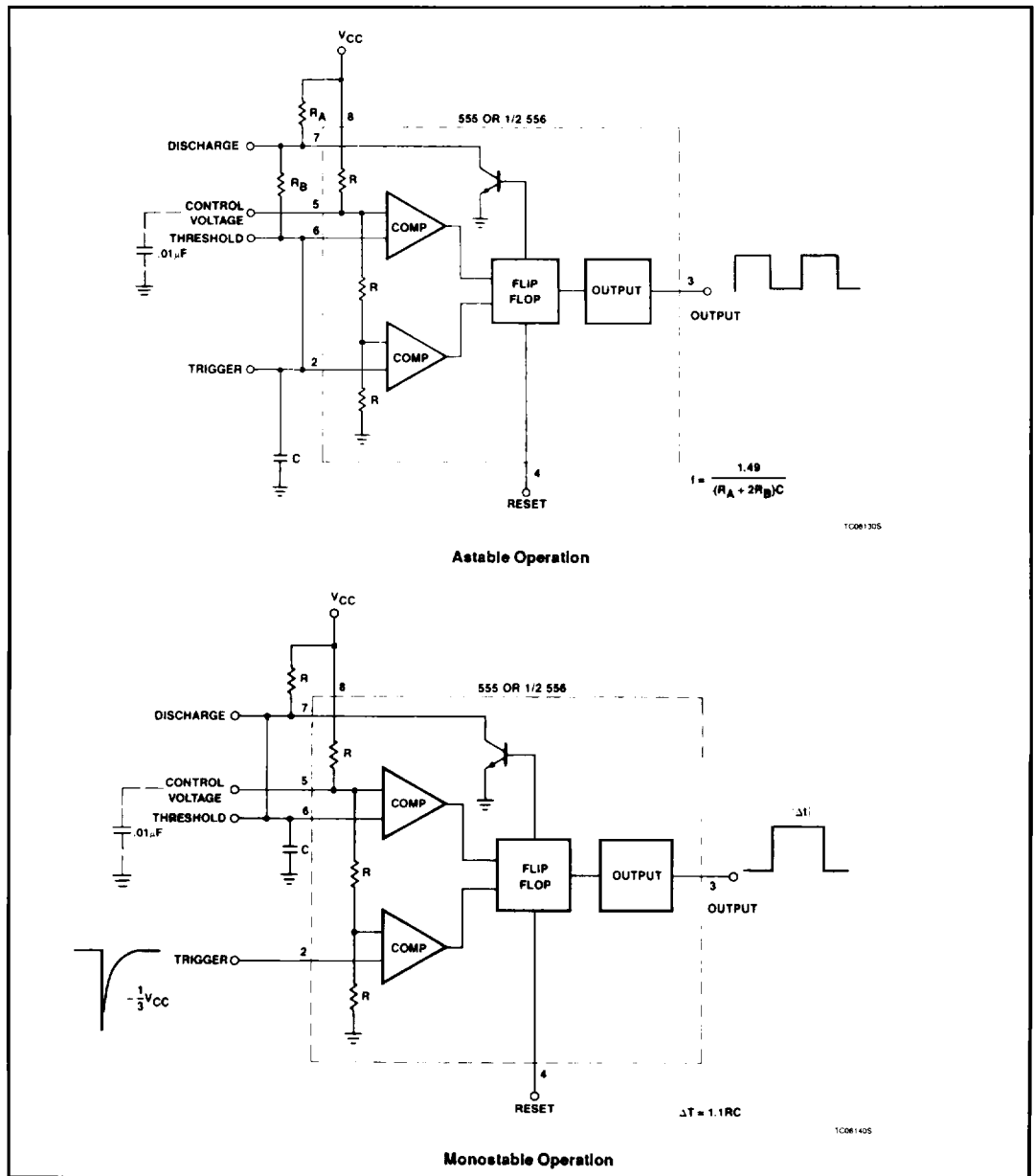
## TYPICAL PERFORMANCE CHARACTERISTICS



## Timer

555

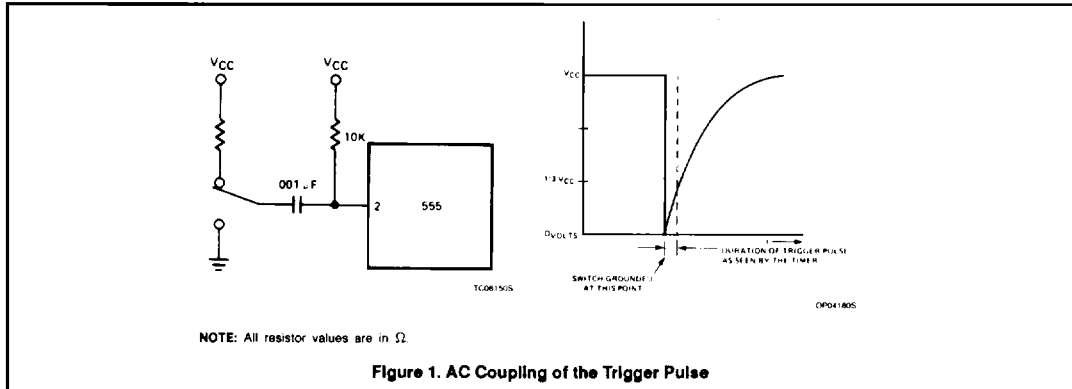
## TYPICAL APPLICATIONS



## Timer

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## TYPICAL APPLICATIONS (Continued)



### Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger (see Figure 1), a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should

the trigger be held low, without AC coupling, for a longer duration than the timing cycle, the output will remain in a high state for the duration of the low trigger signal without regard to the threshold comparator state. This is due to the predominance of  $Q_{15}$  on the base of  $Q_{16}$ , controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn-off time". This is the measurement of the amount of time required after the threshold reaches  $2/3 V_{CC}$  to turn the output low. To explain further,  $Q_1$  at the threshold input turns on after reaching  $2/3 V_{CC}$ , which then turns on  $Q_5$ , which turns on  $Q_6$ . Cur-

rent from  $Q_6$  turns on  $Q_{16}$  which turns  $Q_{17}$  off. This allows current from  $Q_{19}$  to turn on  $Q_{20}$  and  $Q_{24}$  to give an output low. These steps cause the  $2\mu s$  max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low,  $Q_{10}$  is on and turns on  $Q_{11}$  which turns on  $Q_{15}$ .  $Q_{15}$  turns off  $Q_{16}$  and allows  $Q_{17}$  to turn on. This turns off current to  $Q_{20}$  and  $Q_{24}$ , which results in output high. When the trigger is released,  $Q_{10}$  and  $Q_{11}$  shut off,  $Q_{15}$  turns off,  $Q_{16}$  turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.