

# RAA207703GBM/7704GBM/7705GBM

# Synchronous Buck Regulator with Internal Power MOSFETs

R07DS0892EJ0100 Rev.1.00 Aug 02, 2013

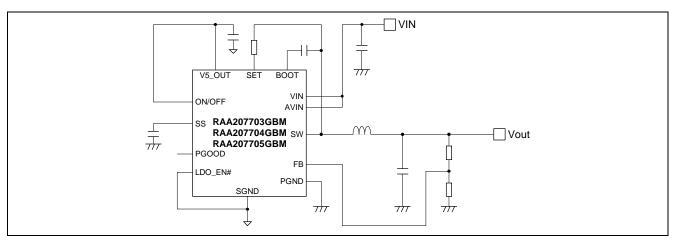
## **Description**

The RAA207703GBM is monolithic synchronous buck regulator with power MOSFETs in extremely small package. The RAA207703GBM delivers high output current by small Rds(on) Power MOSFETs. Constant on time control architecture provides fast transient response, and minimize external components. The RAA207703GBM operates skip mode at light load, it provides high efficiency in all load condition. The RAA207703GBM incorporates internal 5V LDO, so the regulator can operates single power supply. Three current ability products can be selected.

#### **Features**

- · Input voltage range: 5.5 V to 16 V (internal LDO use), 3.0 V to 16 V (external 5 V use)
- Output voltage range: 0.8 V to 5.0 V
- · Constant-On-Time control
- · Built-in power MOSFETs suitable for PC, Server application
- · Internal 5 V LDO for single power supply operation
- 5 V LDO / external 5 V input selectable (LDO remote ON/OFF)
- Switching frequency: Adjustable up to 2 MHz
- · High average output current, up to 15 A (7703GBM), 10 A (7704GBM), 5 A (7705GBM)
- · Controllable driver: Remote ON/OFF
- · Power Good function
- · Over current protection/Over voltage protection/Thermal shutdown function
- · Built-in bootstrapping diode
- · Soft Start period adjustable
- · Enhanced light load mode function for higher efficiency
- · Extremely small chip size package with solder bump
- · Pb-Free/Halogen-Free

# **Application Circuit**



### **Pin Arrangement**

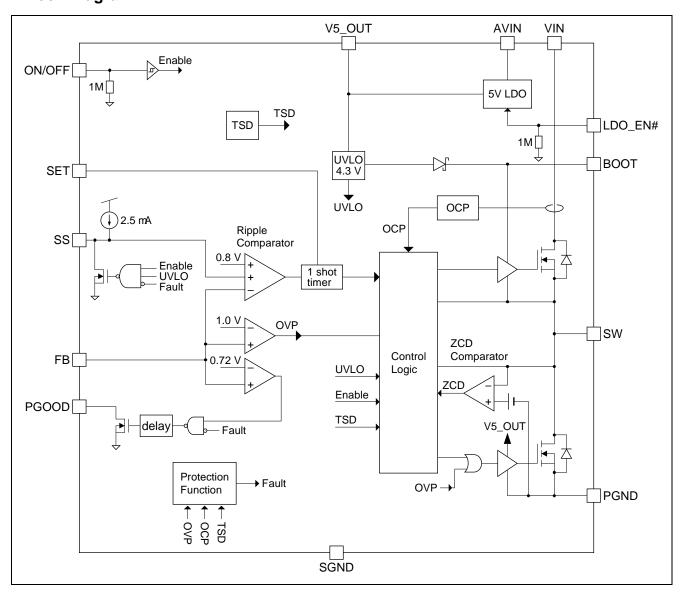


# **Pin Description**

| Pin Name | Pin No. | Description                   | Remarks                                    |
|----------|---------|-------------------------------|--|
| V5_OUT   | 1A      | Controller voltage            | Controller supply (5 V regulator output)   |
| SGND     | 2A      | Controller analog GND         | Should be connected to PGND on PCB pattern |
| FB       | 3A      | Feedback voltage input pin    |  |
| LDO_EN#  | 4A      | Internal 5 V LDO enable pin   |  |
| AVIN     | 5A      | Analog input voltage          | Should be connected to VIN on PCB pattern  |
| BOOT     | 1B      | Bootstrap voltage pin         | To be supplied +5 V through integrated SBD |
| SET      | 2B      | Constant on time program pin  | Tie resistor between SW and SET pin        |
| PGOOD    | 3B      | Power good indicator pin      | Pull low when No Good (open drain output)  |
| SS       | 4B      | Soft start period program pin | Tie capacitor between SS and SGND          |
| ON/OFF   | 5B      | Operation enable pin          | Operation stop when "L" signal asserted    |
| VIN      | _       | Input voltage                 |  |
| SW       | _       | Switching node                |  |
| PGND     | _       | Power GND                     | Should be connected to SGND on PCB pattern |

Note: Pin assign of 1A-5A & 1B-5B is common through RAA207703GBM, RAA207704GBM and RAA207705GBM.

# **Block Diagram**



#### 1. Truth table for the ON/OFF pin

| · · · · · · · · · · · · · · · · · · · |                           |  |  |  |
|---------------------------------------|---------------------------|--|--|--|
| ON/OFF Input                          | Driver Chip Status        |  |  |  |
| "L"                                   | Shutdown (operation STOP) |  |  |  |
| "Open"                                | Shutdown (operation STOP) |  |  |  |
| "H"                                   | Enable (Normal operation) |  |  |  |

#### 2. Truth table for LDO\_EN# pin

| LDO_EN# Input | 5 V Regulator Status |  |  |
|---------------|----------------------|--|--|
| "L"           | LDO enable           |  |  |
| "Open"        | LDO enable           |  |  |
| "H"           | LDO disable          |  |  |

# **Absolute Maximum Ratings**

 $(Ta = 25^{\circ}C)$ 

| Item                           | Item Symbol Ratings  |                     | Unit | Notes |
|--------------------------------|----------------------|---------------------|------|-------|
| Input voltage                  | VIN, AVIN            | -0.3 to +20         | V    | 1     |
| Switch node voltage            | SW                   | 20(DC), 23(<10 ns)  | V    | 1     |
| BOOT voltage                   | VBOOT                | 25(DC), 28(<10 ns)  | V    | 1, 2  |
| Controller voltage             | V5_OUT               | -0.3 to +6          | V    | 1     |
| V5_OUT current                 | ICC                  | -20 to +0.1         | mA   | 3     |
| FB pin voltage                 | $V_{FB}$             | -0.3 to V5_OUT +0.3 | V    | 1, 4  |
| ON/OFF voltage                 | V <sub>ON/OFF</sub>  | -0.3 to VIN         | V    | 1     |
| LDO_EN# voltage                | V <sub>LDO_EN#</sub> | -0.3 to VIN         | V    | 1     |
| SET voltage                    | V <sub>SET</sub>     | -0.3 to VIN         | V    | 1     |
| PGOOD voltage                  | $V_{PGOOD}$          | -0.3 to VIN         | V    | 1     |
| PGOOD sink current             | I <sub>PGOOD</sub>   | +2                  | mA   | 3     |
| Operating junction temperature | Tj-opr               | -40 to +125         | °C   |       |
| Storage temperature            | Tstg                 | -55 to +150         | °C   |       |

Notes: 1. Rated voltages are relative to voltages on the SGND and PGND pins.

- 2. BOOT V5\_OUT < 20 V
- 3. For rated current, (+) indicates inflow to the chip and (-) indicates outflow.
- 4. V5\_OUT + 0.3 V < 6 V

# **Thermal Information**

| Item                            | Symbol | Part No.     | Value | Unit | Note |
|---------------------------------|--------|--------------|-------|------|------|
| Thermal resistance              | qj-a   | RAA207703GBM | 27    | °C/W | 1    |
| (junction to air when device is |        | RAA207704GBM | 33    |      |      |
| mounted on evaluation board)    |        | RAA207705GBM | 39    |      |      |

Note: 1. Not assured value, just reference for design. Above data is taken using Renesas's reference board.

# **Recommended Operating Condition**

| Item                      | Symbol | Ratings    | Unit | Remarks                            |
|---------------------------|--------|------------|------|------------------------------------|
| Input voltage             | VIN    | 3.0 to 16  | V    |                                    |
| Analog input voltage      | AVIN   | 4.5 to 16  | V    |                                    |
| Controller voltage        | V5_OUT | 4.5 to 5.5 | V    | When V5_OUT is supplied externally |
| Continuous output current | IOUT   | 0 to 15    | Α    | 15 A: RAA207703GBM                 |
|                           |        | 0 to 10    |      | 10 A: RAA207704GBM                 |
|                           |        | 0 to 5     |      | 5 A: RAA207705GBM                  |

# **Electrical Characteristics**

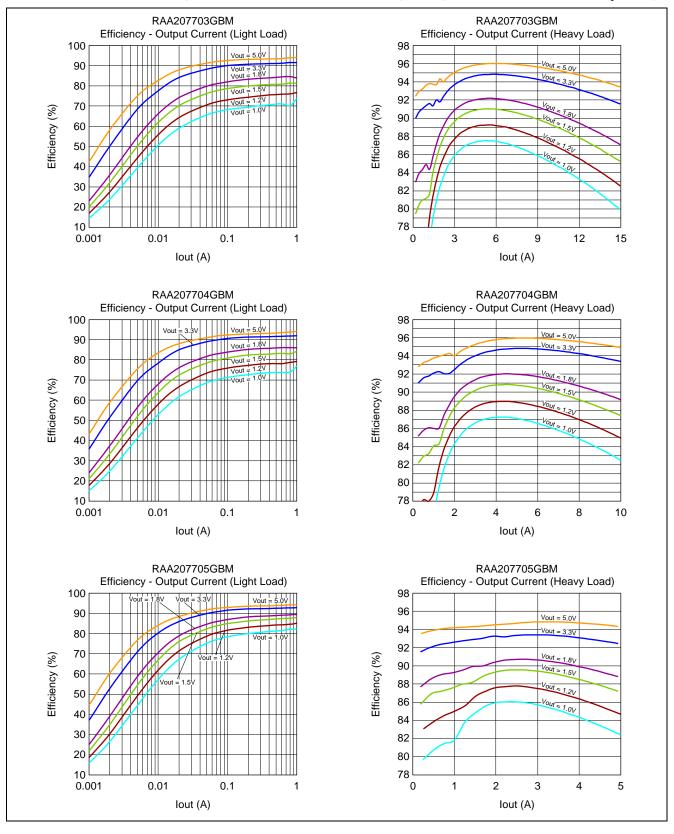
 $(Ta = 25^{\circ}C, VIN = 12 V, unless otherwise specified)$ 

| Item                          |                                       | Symbol                   | Min  | Тур  | Max  | Unit | Test Conditions  |
|-------------------------------|---------------------------------------|--------------------------|------|------|------|------|--|
| Supply                        | AVIN start threshold                  | VH                       | _    | 4.3  | 4.5  | V    |  |
|                               | AVIN shutdown threshold in CCM        | VL                       | 3.6  | 3.8  | _    | V    |  |
|                               | AVIN shutdown threshold in ELL mode   | V <sub>LDCM</sub>        | _    | 3.0  | 3.6  | V    | In ELL mode<br>(DCM, f <sub>SW</sub> < 100 kHz)        |
|                               | AVIN quiescent current                | Iq                       | _    | 400  | 550  | mA   | Output = no load, ELL mode                             |
|                               | AVIN disable current                  | I <sub>IAIN-DISBL1</sub> | _    | 70   | 150  | mA   | ON/OFF = 0 V,  |
|                               | (LDO_EN# = 12 V)                      |                          |      |      |      |      | LDO_EN# = 12 V   |
|                               | VIN disable current                   | I <sub>IAIN-DISBL2</sub> | _    | 130  | 200  | mA   | ON/OFF = 0 V,  |
|                               | (LDO_EN# = 0 V)                       |                          |      |      |      |      | LDO_EN# = 0 V  |
|                               | AVIN operating current (RAA207703GBM) | I <sub>CIN</sub>         | _    | 40   | _    | mA   | $f_{SW} = 1 \text{ MHz}, \text{ ton} = 200 \text{ ns}$ |
|                               | AVIN operating current (RAA207704GBM) | I <sub>CIN</sub>         | _    | 35   | _    | mA   |  |
|                               | AVIN operating current (RAA207705GBM) | I <sub>CIN</sub>         | _    | 20   | _    | mA   |  |
|                               | VIN disable current                   | I <sub>IIN-DISBL1</sub>  |      | _    | 5    | mA   | ON/OFF = 0 V   |
| Remote                        | Disable level                         | V <sub>DISBL</sub>       | _    | _    | 0.6  | V    | 3.3 / 5.0 V interface                                  |
| ON/OFF                        | Enable level                          | V <sub>ENBL</sub>        | 2.0  | _    | _    | V    |  |
|                               | Pull-down resistance                  | R <sub>DISBL</sub>       | 0.7  | 1    | 1.3  | MW   | ON/OFF = 1 V   |
| 5 V LDO                       | 5 V LDO on level                      | V <sub>LDO_ON</sub>      | _    | _    | 0.6  | V    |  |
| enable                        | 5 V LDO off level                     | $V_{LDO\_OFF}$           | 2.0  | _    | _    | V    |  |
|                               | Pull-down resistance                  | R <sub>LDO</sub>         | 0.7  | 1    | 1.3  | MW   | LDO_EN# = 1 V  |
| 5 V LDO<br>output             | 5 V LDO output voltage                | V <sub>LDO</sub>         | 4.5  | 5.0  | 5.5  | V    | at no load   |
| FB                            | Comparator threshold voltage          | V <sub>FB_COMP</sub>     | 792  | 800  | 808  | mV   |  |
|                               | FB input current                      | I <sub>FB_IN</sub>       | -0.1 | 0    | +0.1 | mA   | FB = 1 V   |
| 1shot timer                   | High MOSFET on pulse width            | Pw                       | 170  | 210  | 250  | ns   | VIN = 12 V, Rset = 30 kW                               |
|                               | High MOSFET minimum on pulse width    | P <sub>MIN_ON</sub>      | _    | 70   | _    | ns   |  |
|                               | High MOSFET minimum off pulse         | P <sub>MIN_OFF</sub>     | _    | 50   | _    | ns   |  |
| Power                         | Rising threshold on FB                | V <sub>PG_rise</sub>     | 0.67 | 0.72 | 0.77 | V    |  |
| good                          | Power good falling hysteresis         | $dV_{PG}$                | _    | 50   | _    | mV   |  |
| indicator                     | Power good resistance                 | $R_{PG}$                 | 0.25 | 0.5  | 1    | kW   | FB = 0 V   |
| Soft start                    | Soft start bias current               | I <sub>SS</sub>          | 1.8  | 2.5  | 3.3  | mA   |  |
| Over<br>voltage<br>protection | OVP trip voltage on FB                | V <sub>OVP</sub>         | 0.95 | 1.00 | 1.05 | V    |  |
| Over current                  | OCP trip current<br>(RAA207703GBM)    | I <sub>OCP</sub>         | 16.0 | 20.0 | 24.0 | А    | Fixed internally, inductor peak current *1             |
| protection                    | OCP trip current<br>(RAA207704GBM)    | I <sub>OCP</sub>         | 11.5 | 14.0 | 17.0 | А    | Fixed internally, inductor peak current *1             |
|                               | OCP trip current<br>(RAA207705GBM)    | I <sub>OCP</sub>         | 6.4  | 8.0  | 9.6  | А    | Fixed internally, inductor peak current *1             |
| Over                          | TSD trip temperature                  | T <sub>TSD</sub>         | 130  | 150  | _    | °C   | *1   |
| temperature protection        | Temperature hysteresis                | T <sub>hys</sub>         | _    | 15   | _    | °C   | *1   |

Note: \*1 Not directly tested. Assured by related characteristics test.

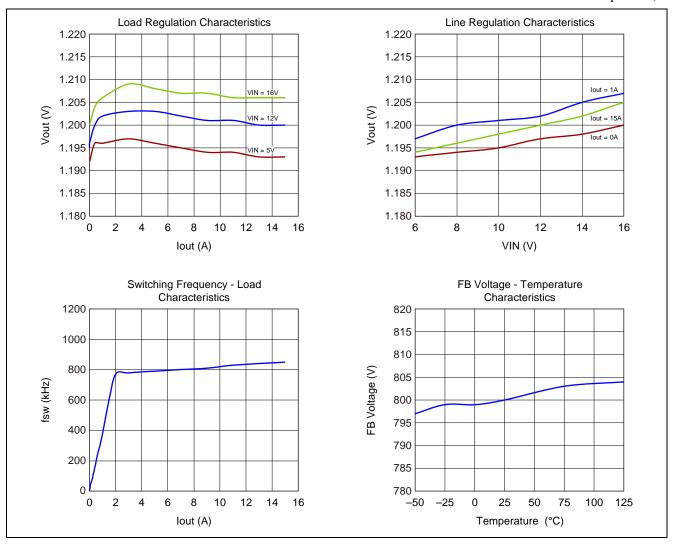
# **Efficiency Performance**

(VIN = 12 V, L = 1 mH, fsw = 500 kHz (at CCM) no airflow, unless otherwise specified)



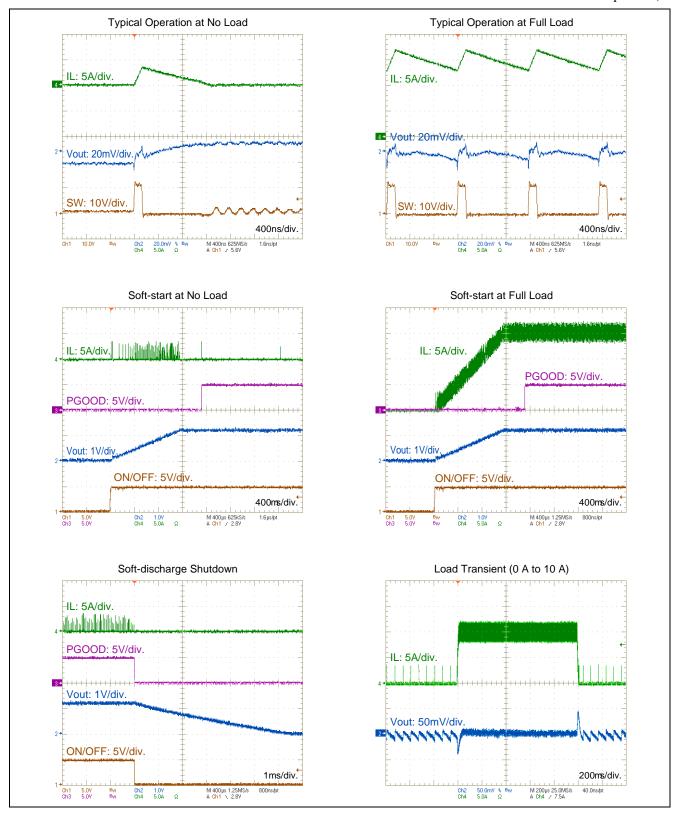
# **Operating Performance**

(RAA207703GBM, VIN = 12 V, Vout = 1.2 V, L = 0.42 nH, Cout = 5  $^{\prime}$  47 nF, ton = 130 ns, unless otherwise specified)



# **Operating Waveform**

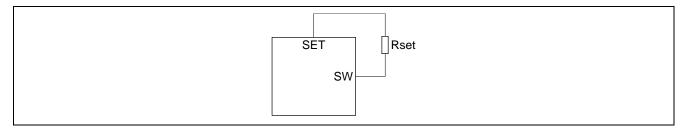
(RAA207703GBM, VIN = 12 V, Vout = 1.2 V, L = 0.42 nH, Cout = 5 ' 47 nF, ton = 130 ns, unless otherwise specified)



### **Description of Operation**

The RAA207703GBM operates as voltage-ripple based constant on time control architecture. Converter output is controlled by output voltage ripple which is determined by inductor ripple current and ESR & ESL of output capacitor. Each switching cycle starts High-side MOSFET turn on which time is decided by 1 shot timer. After High-side MOSFET turns off, Low side turns on, and it keeps until FB voltage becomes lower than reference voltage. In light load condition, Low-side MOSFET on time is decided by inductor zero current.

#### **Switching Frequency, Constant on Time Setting**



Switching Frequency in CCM mode is determined by following equation.

Switching Frequency: (Vout / VIN) • (1 / ton) [Hz] 1/4 (1)

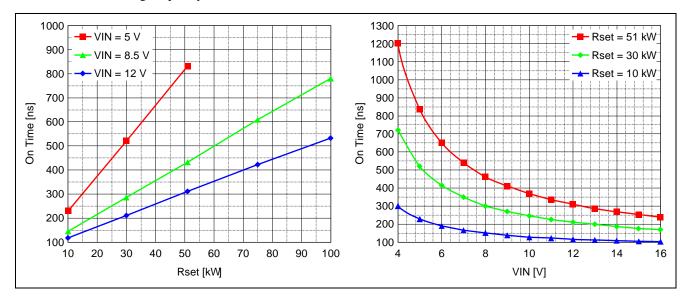
Here, ton is High-side MOSFET on time, and it is determined by following equation.

On time pulse: (50 pF • 1 V / (VIN – 2.0 V)) • Rset + 60 ns [s] 1/4 (2)

From above equation, constant on time is change depend on VIN, so switching frequency is almost constant when VIN change. This architecture is suitable for battery application. From the above equation, Rset is calculated by

Rset: (Vout / (VIN • Fsw) - 60 ns) • (VIN - 2.0 V) / (50 pF • 1 V) [W] 1/4 (3)

Here, Fsw is switching frequency.



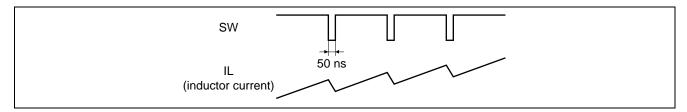
Minimum on time is 70 ns (typ.), so recommended on time pulse is more than 100 ns. Maximum operating frequency is restricted by minimum on time and minimum off time (50 ns, please see next chapter).

#### **Maximum Duty Cycle Operation**

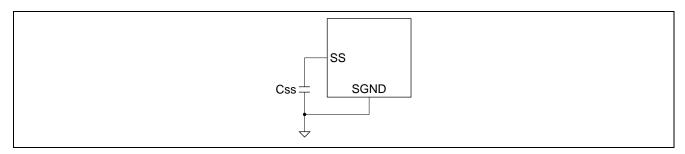
Maximum duty cycle is restricted by following equation.

Here, 50 ns means High-side minimum off time.

If FB voltage does not reach reference voltage after the High-side MOSFET turn on time is expired, Low-side MOSFET turns on 50 ns, and next switching cycle starts. Especially, this condition occurs when output load transient state.



#### **Soft Start**



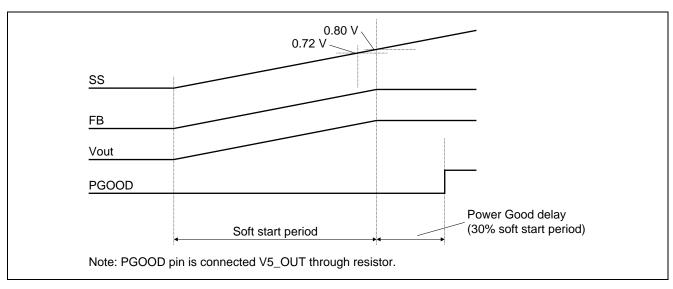
Soft start ramp period is adjustable by external capacitor (Css) selection. When converter start operating, 2.5 mA current from SS pin charges capacitor between SS and GND. Soft start period is determined by following equation.

Soft Start period: Css • 0.8 V / 2.5 mA [s] 1/4 (5)

Here, 0.8 V is internal reference voltage Vref. IC operates diode emulation mode at Soft start period, so it can prevent from reverse current when pre-bias condition. Soft start restarts when Enable signal re-entered, and after OCP, OVP, TSD, UVL release condition.

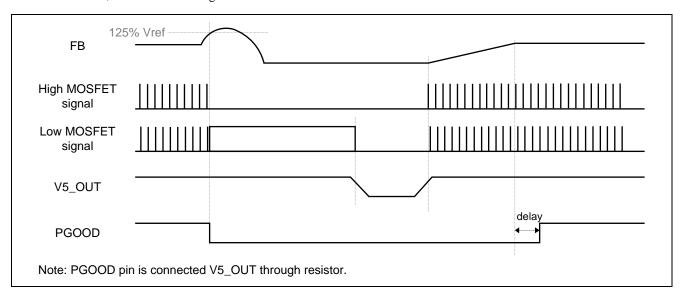
#### **Power Good Indicator**

Power good indicator is useful for controlling multi-converter systems for sequential start up and shut down. FB voltage is monitored continuously by power good comparator. The power good comparator compares FB pin and 90% internal reference voltage (0.72 V). When FB reaches reference voltage, PGOOD pin becomes high impedance after internal delay (30% of soft start period). Under the fault condition (UVLO, OVP, OCP, TSD), PGOOD pin is pulled low.



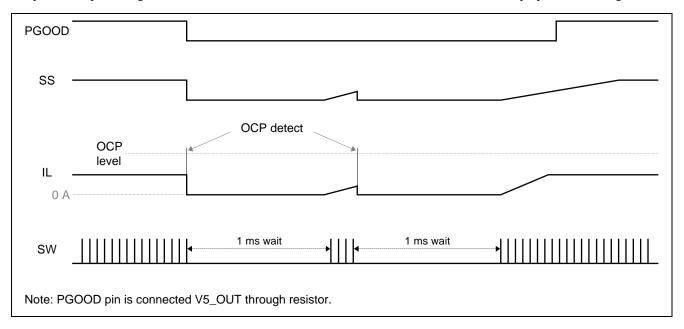
#### **Over Voltage Protection (OVP)**

When FB voltage exceeds 125% of reference voltage (1.00 V), switching stops immediately and latched Low-side MOSFET on state in order to pull the output voltage. To leave the OVP condition, V5\_OUT needs to be pulled under the UVLO level, and re-enter the signal.



#### **Over Current Protection (OCP)**

OCP detection circuit monitors High-side MOSFET drain-source current. When the current exceeds fixed level four times, IC starts hiccup operation. In the hiccup operation, switching stops and operate 1 ms timer. After 1 ms timer is expired, IC operates again from soft start state. If IC detect OCP in the soft start circuit, hiccup operation start again.



# Thermal Shutdown (TSD)

Thermal sensor monitors junction temperature of IC. When junction temperature exceeds 150°C, switching stops. After junction temperature become 135°C, IC restart switching from soft start (Non-latched function).

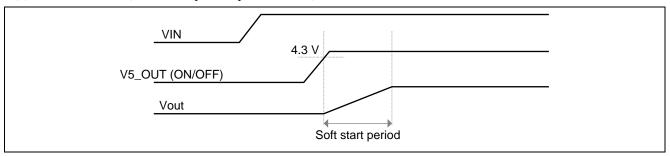
### **Enhanced Light Load Function (ELL)**

IC operates diode emulation mode in light load condition. To enhance light load efficiency, IC detects light load condition automatically, and operate as Enhanced Light Load mode (ELL). In ELL mode, bias current of IC becomes small, so this function can improve the efficiency.

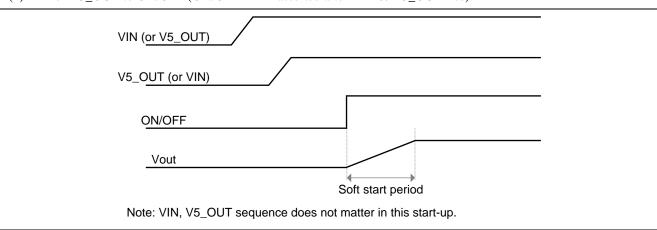
#### Start-up Sequence for External 5 V Use

When LDO function is used, start-up sequence is free. However, it needs specific start-up sequence when LDO function is not used. Please set start-up sequence from following. IC cannot start-up when "V5\_OUT & ON/OFF rise first, VIN rises secondly" sequence.

#### (1) VIN to V5\_OUT (ON/OFF is pulled up to V5\_OUT)

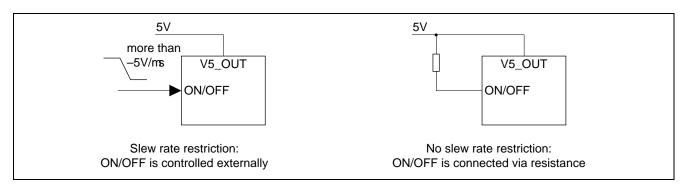


#### (2) VIN or V5\_OUT to ON/OFF (ON/OFF = "H" asserted after VIN & V5\_OUT rise)



#### **ON/OFF Pin Slew Rate Restriction**

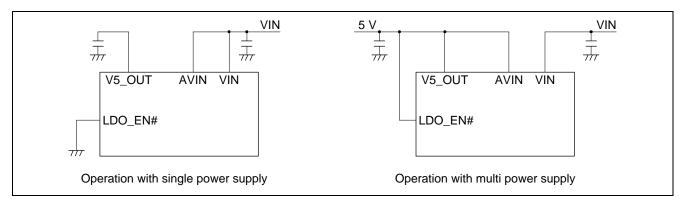
When ON/OFF pin is driven by another controller, the slew rate of H to L transition must be higher than -5 V/ms monotonically (must be rapid transition). If the slew rate is lower than -5 V/ms (slow transition), switching noise affect ON/OFF pin input circuit and lead to malfunction in case of heavy load state. Recommended drive impedance of ON/OFF pin is less than 10 kW. If ON/OFF pin is always pulled up to V5\_OUT or VIN via resistance, slew rate is not a matter.



#### **Controller Power Supply**

The RAA207703GBM incorporates internal 5 V LDO, so it can operate with single power supply. LDO\_EN# can control LDO operation, and select the controller power supply from LDO or V5\_OUT pin. When LDO\_EN# = H state, external 5 V should be applied to V5\_OUT pin and AVIN pin.

Typical pin connection of each operation are below.

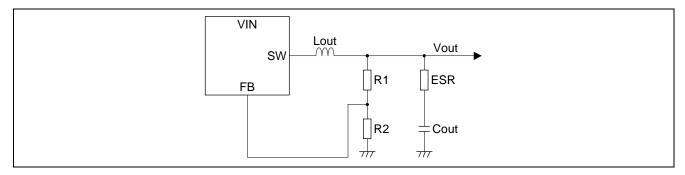


Note: Truth table for LDO\_EN# pin

| LDO_EN# Input | 5 V Regulator Status |  |
|---------------|----------------------|--|
| "L"           | LDO enable           |  |
| "Open"        | LDO enable           |  |
| "H"           | LDO disable          |  |

### Stability Criteria, Output Voltage Setting for High ESR Output Capacitor

Small output ripple voltage makes control loop unstable in constant on time architecture. Ripple voltage needs to be larger than 15 mV on FB pin. When using high ESR (>50 mW) capacitor such as Electrolytic capacitor, Polymer aluminum capacitor for output capacitor, ripple voltage on FB pin will be more than 15 mV.



#### Stability criteria

From loop stability analysis, constant on time control system must satisfy below equation.

Stability criteria: ESR • Cout > ton / 2 1/4 (6)

Here, ton is constant on time. If the system cannot satisfy above equation, subharmonic oscillation will occur.

#### **Vout setting**

FB comparator compares FB voltage and internal accurate reference voltage (0.8 V). Feedback loop controls FB voltage to match the reference voltage. However, Vout ripple voltage affects FB voltage. So, effective FB pin voltage Vfb will be below. (Here, Vout ripple from bulk capacitance is ignored)

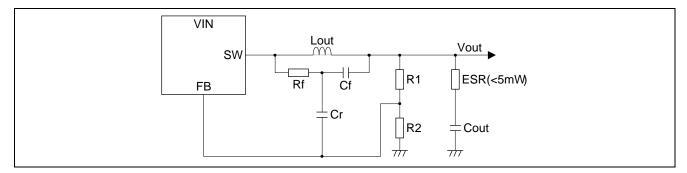
Effective FB voltage (Vfb): 0.8 V + 
$$\frac{1}{2}$$
 ((VIN – Vout) • ton • ESR • R2 / (Lout • (R1 + R2))) [V]  $\frac{1}{4}$  (7)

Here, R1 and R2 is output voltage divider resistor, Lout is inductance of output filter and ESR means ESR of output capacitor (refer to above figure). 0.8 V in above equation means reference voltage of IC. Considering Vout ripple voltage, Vout voltage becomes below equation.

Vout: Vfb • (R1 + R2) / R2 [V] 1/4 (8)

#### **Operating with Small ESR Output Capacitor**

When using low-ESR output capacitor like MLCC, voltage ripple on output voltage node is very small. So, voltage ripple needs to be enhanced by additional components. Recommended ripple enhance method is like below figure.



#### Ripple injection on FB pin

Rf and Cf make ripple voltage using inductor DCR ripple. Cr is used for AC ripple injection to FB pin. Ripple voltage between Rf and Cf is described by following equation.

Recommended ripple voltage is between 15 mV and 20 mV.

#### Stability criteria

To keep voltage ripple amplitude on FB pin, below equation should be satisfied.

Here, Fsw means switching frequency at CCM mode. Recommended value for Cf = 0.01 nF, and Cr = 1000 pF. R1 and R2 are recommended between 10 kW and 100 kW.

From loop stability analysis of above circuit configuration, the system must satisfy below equation.

If the system cannot satisfy above equation, subharmonic oscillation will occur. Capacitance - voltage dependence is must be considered when MLCC use.

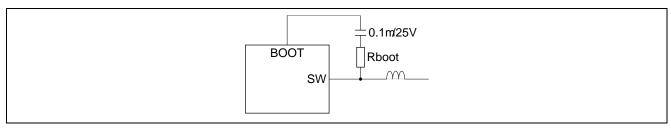
#### **Vout setting**

Additional ripple voltage and ESR voltage ripple also affects Vout accuracy. From above figure, total ripple voltage on FB pin is described by below equation.

Effective FB pin voltage is described by below equation.

So, actual Vout voltage is described by below equation.

#### **BOOT Resistance**

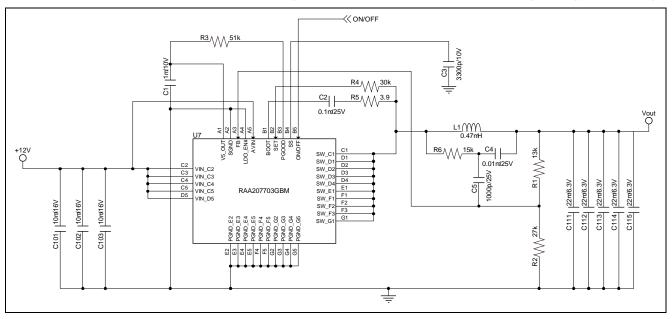


SW node spike occurs when IC is operating. Turn-on spike voltage exceeds absolute maximum voltage of SW pin depends on operating condition. To suppress the spike voltage, adding boot resistor (Rboot) is effective. Recommended Rboot is below.

|              | Recommended Rboot |           |  |
|--------------|-------------------|-----------|--|
| Part No.     | VIN = 12 V        | VIN = 5 V |  |
| RAA207703GBM | 3.9 W             | 0 W       |  |
| RAA207704GBM | 2.0 W             | 0 W       |  |
| RAA207705GBM | 0 W               | 0 W       |  |

# **Design Example**

(VIN = 12 V, Vout = 1.2 V, Fsw = 500 kHz (at CCM), L = 0.47 mH)



1. Setting of ton (constant on time)

In this condition, calculated on time is from equation (1),

Calculated ton: 1.2 V / 12 V • (1 / 500 kHz) = 200 ns

From equation (3),

Calculated R4 =  $(1.2 \text{V} / (12 \text{ V} \cdot 500 \text{ kHz}) - 60 \text{ ns}) \cdot (12 \text{ V} - 2 \text{ V}) / (50 \text{ pF} \cdot 1 \text{ V}) = 28 \text{ kW}$ 

so choose R4 = 30 kW from E24 series.

So, actual on pulse ton is decided by equation (2),

Constant on time:  $((50 \text{ pF} \cdot 1 \text{ V} / (12 \text{ V} - 2 \text{ V})) \cdot 30 \text{ kW} + 60 \text{ ns} = 210 \text{ ns}$ 

2. Setting of ripple injection resistance

Voltage ripple on FB pin needs to be more than 15 mV. Here, C4 = 0.01 nF, C5 = 1000 pF and ESR of output cap = 0.5 mW. To obtain 15 mV additional ripple on FB pin from R6, C4 and C5 network circuit, R6 is calculated by equation (10).

So choose R6 = 15 kW from E24 series and actual ripple voltage from injection circuit becomes 15.1 mV.

So, Total ripple voltage on FB pin is calculate by equation (13),

Total ripple voltage:

 $(12 \text{ V} - 1.2 \text{ V}) \cdot 210 \text{ ns} / (15 \text{ kW} \cdot 0.01 \text{ mF}) + (12 \text{ V} - 1.2 \text{ V}) \cdot 210 \text{ ns} / 0.47 \text{ mH} \cdot 0.5 \text{ mW} = 17.5 \text{ mV}$ 

3. Setting of output voltage resistor

From above setting, effective FB voltage is from equation (15),

Effective FB voltage: 800 mV + 17.5 mV / 2 = 808.8 mV

When R1 = 13 kW, R2 is decided from equation (15).

R2 = 13 kW / ((1.2 V / 808.8 mV) - 1) = 26.8 kW

So, choose R2 = 27 kW from E24 series.

#### 4. Stability criteria confirmation

For output capacitor, please confirm stability criteria. Stability criteria from equation (11),

$$1/(2p \cdot 0.01 \text{ mF} \cdot 500 \text{ kHz}) = 32 \text{ W} << 1/(2p \cdot 1000 \text{ pF} \cdot 500 \text{ kHz}) = 318 \text{ W} << 13 \text{ kW} \cdot 27 \text{ kW}/(13 \text{ kW} + 27 \text{ kW}) = 8.8 \text{ kW}$$

so, above criteria is satisfied.

For output capacitor, please confirm stability criteria. Stability criteria from equation (12),

Cout > 
$$(210 \text{ ns} / 2) \cdot 15 \text{ kW} \cdot 0.01 \text{ mF} / 0.47 \text{ mH} = 34 \text{ mF}$$

So, choose 110 mF (22 mF ' 5 pcs.) for output capacitor. Here, please consider voltage dependence of capacitor.

If you cannot satisfy above criteria, please consider below changes.

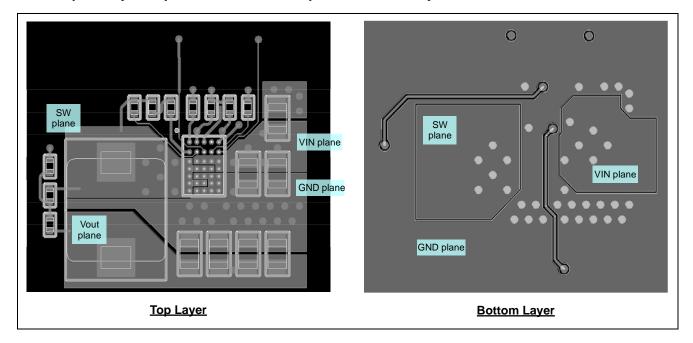
- 3/4 increase L or Cout value
- 3/4 increase frequency (decrease constant on time)
- 34 change Rf value.

#### 5. Other components

 $C1 = 1 \, \text{mF} / 10 \, \text{V}$  and  $C2 = 0.1 \, \text{mF} / 25 \, \text{V}$  are recommended. C3 decides soft start period from equation (5). R5 is decided from the table in "Boot Resistance" section. Input and output capacitors are decided considering voltage ripple, current ripple and voltage tolerance.

# **Board Layout Example (RAA207703GBM)**

Board layer example: 4 layer, internal 2nd and 3rd layer are used for GND plane.



#### 1. Power part

- 3/4 Input capacitor should be placed close to VIN and PGND pin to reduce switching noise and to improve the efficiency.
- 34 Many thermal via should be placed on VIN, SW and PGND planes to spread heat to board. Furthermore, VIN, SW planes on bottom layer are effective for thermal spread (If available).

#### 2. Control part

- 3/4 Decoupling capacitor between V5\_OUT and SGND should be placed as close as possible to the chip in order to stable operation.
- 34 Also, SGND, PGND via should be placed as close as possible to the chip, and connect each pin low impedance by internal GND plane.
- 3/4 FB resistance should be placed close to chip and FB wiring should be short to avoid noise. Furthermore, additional ripple circuit wiring should be kept away from high dv/dt plane such as SW and BOOT wiring.
- <sup>3</sup>/<sub>4</sub> To ensure the reliability of chip board connection, we recommend Solder Mask Defined (SMD) layout. But you can also use Non-Solder Mask Defined (NSMD) layout as far as you can ensure the reliability. In the case of SMD layout, we recommend below size.
  - Solder resist open size: 280 mm, Land size: 280 mm + 50 to 100 mm (please consider processing accuracy)

# **Representative Inductors**

| Maker             | Inductance [mH] | DL/L0 = 20% Change [A] | Dimensions [mm]   |
|-------------------|-----------------|------------------------|-------------------|
| NEC Tokin         | 0.42            | 20.0                   | 6.7 ′ 8.0 ′ 4.0   |
| MPC series        | 0.60            | 19.0                   | 6.7 ′ 8.0 ′ 5.0   |
|                   | 0.88            | 24.0                   | 10.0′ 11.5 ′ 4.0  |
|                   | 1.0             | 25.0                   | 10.0 ´ 11.7 ´ 5.5 |
| ALPS Green Device | 0.47            | 13.9 <sup>*1</sup>     | 6.5 ′ 7.4 ′ 3.0   |
| GLMC series       | 1.0             | 10 <sup>*1</sup>       | 6.5 ′ 7.4 ′ 3.0   |
|                   | 1.5             | 8.8 *1                 | 6.5 ′ 7.4 ′ 3.0   |
| токо              | 0.33            | 15.9                   | 6.7 ′ 7.4 ′ 3.0   |
| FDVE0630 series   | 0.47            | 15.6                   | 6.7 ′ 7.4 ′ 3.0   |
|                   | 0.75            | 10.9                   | 6.7 ′ 7.4 ′ 3.0   |
|                   | 1.0             | 9.5                    | 6.7 ′ 7.4 ′ 3.0   |
| TDK               | 0.35            | 14.9                   | 5.0 ′ 5.2 ′ 3.0   |
| SPM5030 series    | 0.47            | 11.0                   | 5.0 ′ 5.2 ′ 3.0   |
|                   | 0.75            | 9.7                    | 5.0 ′ 5.2 ′ 3.0   |

Note: \*1 30% change

#### · Small size inductor for RAA207705GBM

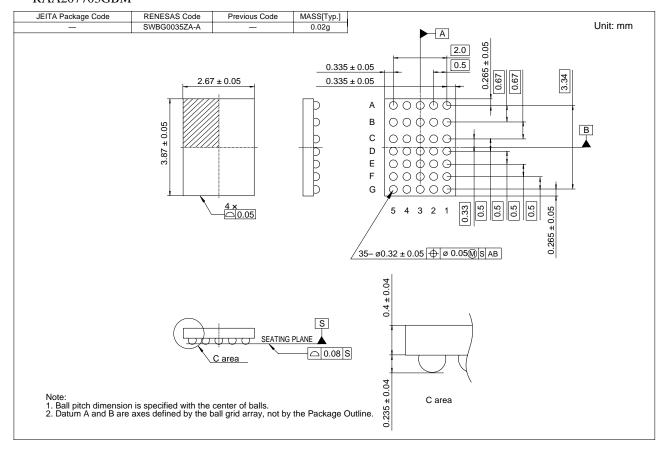
| Maker           | Inductance [mH] | DL/L0 = 30% Change [A] | Dimensions [mm] |
|-----------------|-----------------|------------------------|-----------------|
| токо            | 0.68            | 8.3                    | 4.2 ′ 4.2 ′ 2.0 |
| FDSD0420 series | 1.0             | 6.8                    | 4.2 ´ 4.2 ´ 2.0 |
|                 | 1.5             | 5.7                    | 4.2 ′ 4.2 ′ 2.0 |
| TDK             | 0.47            | 8.3                    | 4.4 ′ 4.1 ′ 1.2 |
| SPM4012 series  | 1.0             | 4.8                    | 4.4 ′ 4.1 ′ 1.2 |

# **Representative Output Capacitors**

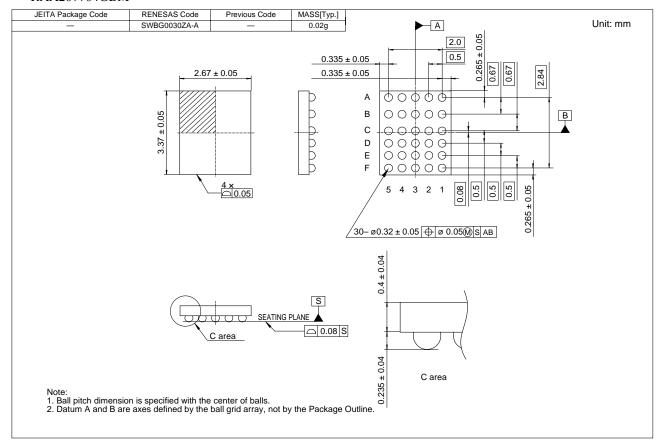
| Maker                   | Maximum Voltage [V] | Capacitance [mF] |
|-------------------------|---------------------|------------------|
| Sanyo POSCAP series     | 2.0 to 10           | 47 to 330        |
| Sanyo OS-CON series     | 2.0 to 10           | 47 to 330        |
| Murata MLCC series      | 6.3 to 10           | 22 to 47         |
| TDK MLCC series         | 6.3 to 10           | 22 to 47         |
| TAIYO YUDEN MLCC series | 6.3 to 10           | 22 to 47         |

# **Package Dimensions**

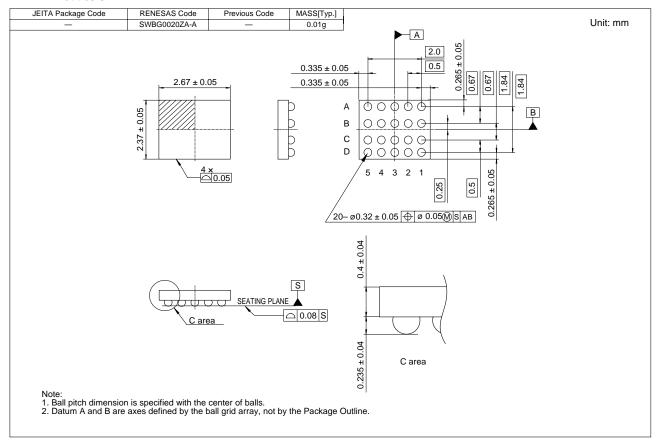
#### · RAA207703GBM



#### · RAA207704GBM



#### RAA207705GBM



# **Ordering Information**

| Part Name        | Quantity | Shipping Container |
|------------------|----------|--------------------|
| RAA207703GBM#HC0 | 2000 pcs | Taping Reel        |
| RAA207704GBM#HC0 | 2000 pcs | Taping Reel        |
| RAA207705GBM#HC0 | 2000 pcs | Taping Reel        |

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