



The Future of Analog IC Technology®

# MP5010

## 5V, 1A- 5A Programmable Current Limit Switch

### DESCRIPTION

The MP5010 is a protection device designed to protect circuitry on the output (source) from transients on input ( $V_{CC}$ ). It also protects  $V_{CC}$  from undesired shorts and transients coming from the source.

At start up, inrush current is limited by limiting the slew rate at the source. The slew rate is controlled by a small capacitor at the dv/dt pin. The dv/dt pin has an internal circuit that allows the customer to float this pin (no connect) and still receive 1.5ms ramp time at the source.

The max load at the output (source) is current limited. This is accomplished by utilizing a sense FET topology. The magnitude of the current limit is controlled by an external resistor from the I-Limit pin to the Source pin.

An internal charge pump drives the gate of the power device, allowing a very low on-resistance DMOS power FET of just 44mΩ.

The source is protected from the  $V_{CC}$  input being too low or too high. Under Voltage Lockout (UVLO) assures that  $V_{CC}$  is above the minimum operating threshold, before the power device is turned on. If  $V_{CC}$  goes above the high output threshold, the source voltage will be limited.

The Enable/Fault pin allows the IC to be turned off and enter a low current shutdown state. This pin is bi-directional and allows feedback of fault information. Momentary current spikes are not considered as faults, neither is the momentary over voltage. However prolonged over current or over voltage conditions will cause excessive power dissipation and result in a thermal shutdown. And the thermal shutdown will cause a fault condition.

### FEATURES

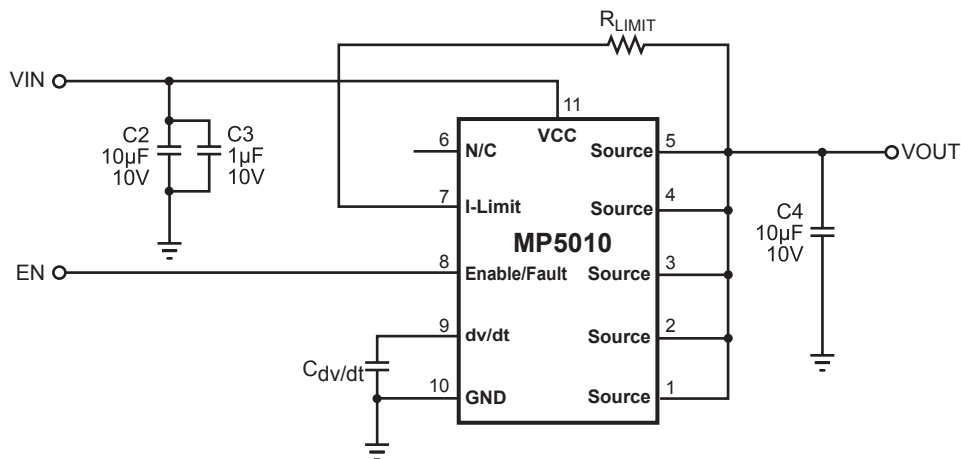
- Integrated 44mΩ Power FET
- Enable/Fault Pin
- Adjustable Slew Rate for Output Voltage
- Adjustable Current Limit
- Thermal Protection
- Over Voltage Limit

### APPLICATIONS

- Hot Swap
- PC Cards
- Laptops

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### TYPICAL APPLICATION

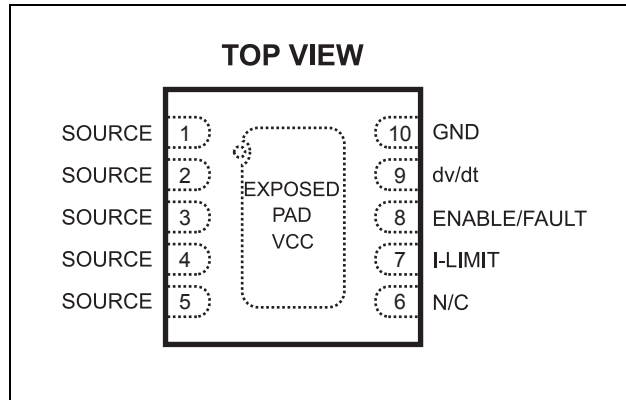


### ORDERING INFORMATION

| Part Number* | Package     | Top Marking | Temperature    |
|--------------|-------------|-------------|----------------|
| MP5010DQ     | QFN10 (3x3) | 8E          | -40°C to +85°C |

\* For Tape & Reel, add suffix -Z (e.g. MP5010DQ-Z). For RoHS Compliant Packaging, add suffix -LF (e.g. MP5010DQ-LF-Z)

### PACKAGE REFERENCE



#### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|   |                 |
|---|-----------------|
| $V_{CC}$ , SOURCE, I-LIMIT .....  | 22V             |
| dv/dt, ENABLE/FAULT .....   | 6V              |
| Storage Temperature.....  | -65°C to +155°C |
| Operating Junction Temperature..  | -40°C to +150°C |
| Continuous Power Dissipation ( $T_A=+25^\circ\text{C}$ ) <sup>(2)</sup> | .....2.5W       |

#### Recommended Operating Conditions <sup>(3)</sup>

|                                     |           |
|-------------------------------------|-----------|
| Input Voltage Operating Range ..... | 4V to 10V |
|-------------------------------------|-----------|

|  |               |               |
|--|---------------|---------------|
| <b>Thermal Resistance <sup>(4)</sup></b> | $\theta_{JA}$ | $\theta_{JC}$ |
| QFN10 .....                              | 50            | 12 ... °C/W   |

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_{J(MAX)}$ , the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ , the maximum allowable power dissipation at any ambient temperature is calculated using:  $P_D(MAX)=(T_{J(MAX)}-T_A)/\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Reduce 0.2 Watts for every 10°C ambient temperature increasing
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7 4-layer board.

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V$ ,  $R_{LIMIT}=22\Omega$ , Capacitive Load=  $10\mu F$ ,  $T_A=25^\circ C$ , unless otherwise noted.

| Parameters                              | Symbol       | Condition   | Min  | Typ  | Max      | Units      |
|---|--------------|---|------|------|----------|------------|
| <b>Power FET</b>                        |              |   |      |      |          |            |
| Delay Time                              | $t_{DLY}$    | Enabling of chip to $I_D=100mA$ with a $12\Omega$ resistive load      |      | 0.2  |          | ms         |
| ON Resistance                           | $R_{DSon}$   | $T_J=25^\circ C$  |      | 44   | 82       | m $\Omega$ |
|   |              | $T_J=80^\circ C$ , Note 5   |      | 95   |          |            |
| Off State Output Voltage                | $V_{OFF}$    | $V_{CC}=18Vdc$ , Enable=0Vdc, $R_L=500\Omega$                         |      |      | 120      | mV         |
| Continuous Current                      | $I_D$        | 0.5 in <sup>2</sup> pad, $T_A=25^\circ C$                             |      | 4.2  |          | A          |
|   |              | minimum copper, $T_A=80^\circ C$                                      |      | 2.3  |          |            |
| <b>Thermal Latch</b>                    |              |   |      |      |          |            |
| Shutdown Temperature                    | $T_{SD}$     |   |      | 175  |          | $^\circ C$ |
| <b>Under/Over Voltage Protection</b>    |              |   |      |      |          |            |
| Output Clamping Voltage                 | $V_{CLAMP}$  | Overvoltage Protection $V_{CC}=8V$                                    | 5.95 | 6.65 | 7.35     | V          |
| Under Voltage Lockout                   | $V_{UVLO}$   | Turn on, Voltage going high   | 3.2  | 3.6  | 4.0      | V          |
| Under Voltage Lockout (UVLO) Hysteresis | $V_{HYST}$   |   |      | 0.4  |          | V          |
| <b>Current Limit</b>                    |              |   |      |      |          |            |
| Hold Current                            | $I_{LIM-SS}$ | 0 $\Omega$ short resistance, $R_{LIM}=22\Omega$ , Note 5              | 1.5  | 2.1  | 2.8      | A          |
| Trip Current                            | $I_{LIM-OL}$ | $R_{LIM}=22\Omega$ ,  |      | 3.3  |          | A          |
| <b>dv/dt Circuit</b>                    |              |   |      |      |          |            |
| Slew Rate                               | dv/dt        | Enable to $V_{OUT}=4.7V$ , Note 6                                     | 0.8  | 1.5  | 2.5      | ms         |
| <b>Enable/Fault</b>                     |              |   |      |      |          |            |
| Low Level Input Voltage                 | $V_{IL}$     | Output Disabled   |      |      | 0.5      | V          |
| Intermediate Level Input Voltage        | $V_{I(INT)}$ | Thermal Fault, Output Disabled  | 0.82 | 1.4  | 1.95     | V          |
| High Level Input Voltage                | $V_{IH}$     | Output Enabled  | 2.5  |      |          | V          |
| High State Maximum Voltage              | $V_{I(MAX)}$ |   |      | 4.8  |          | V          |
| Low Level Input Current (Sink)          | $I_{IL}$     | $V_{ENABLE}=0V$   |      | -28  | -50      | $\mu A$    |
| Maximum Fanout for Fault Signal         |              | Total number of chips that can be connected for simultaneous shutdown |      |      | 3        | Units      |
| Maximum Voltage on Enable Pin           | $V_{MAX}$    | Note 7  |      |      | $V_{CC}$ | V          |
| <b>Total Device</b>                     |              |   |      |      |          |            |
| Bias Current                            | $I_{BIAS}$   | Device Operational  |      | 2    | 3        | mA         |
|   |              | Thermal Shutdown  |      | 1.3  |          |            |
| Minimum Operating Voltage for UVLO      | $V_{MIN}$    | Enable<0.5V   |      |      | 3.0      | V          |

**Notes:**

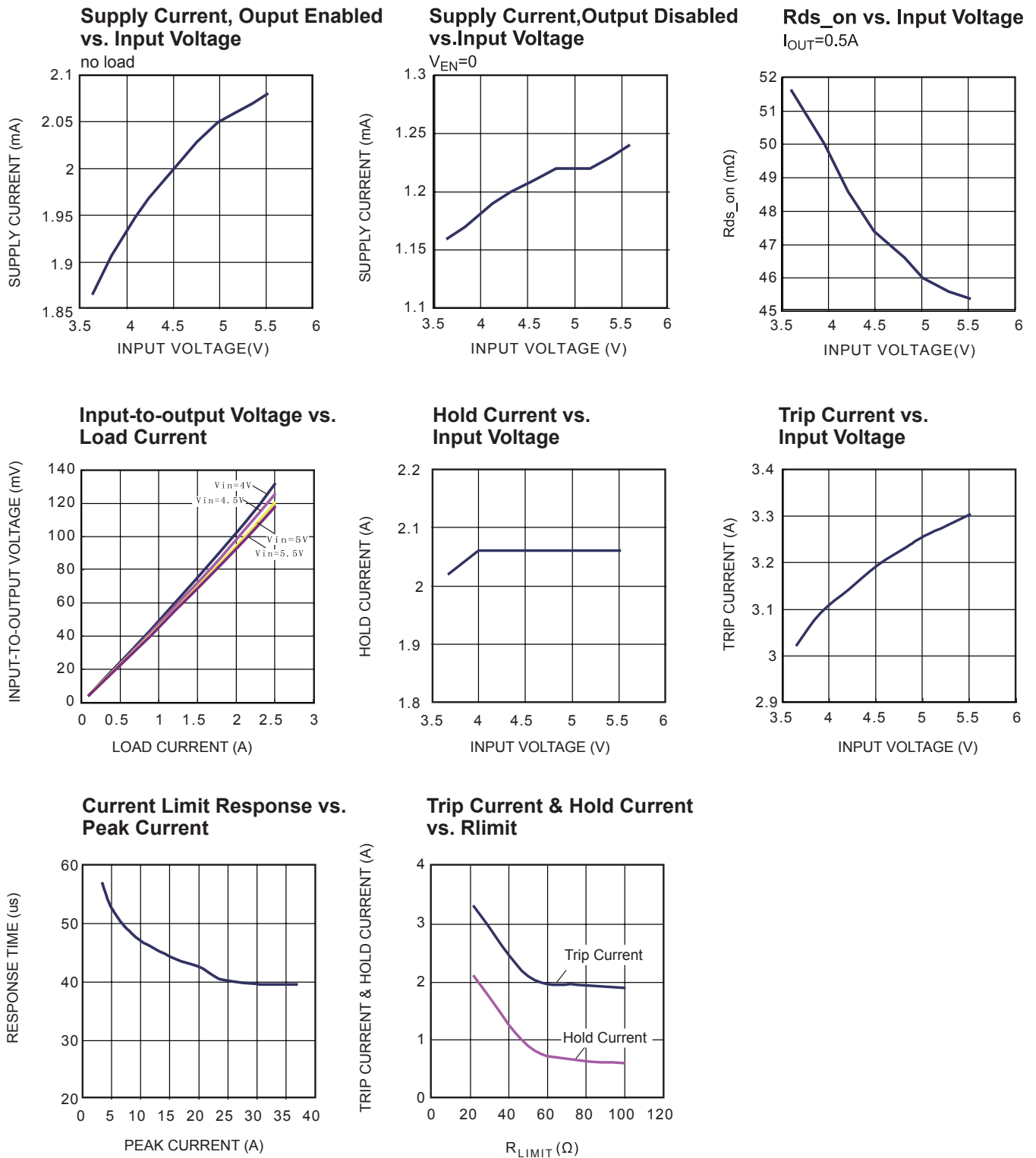
- 5) Guaranteed by design.
- 6) Measure at (30% to 90%)/0.6.
- 7) Maximum Input Voltage on Enable pin to be  $\leq 6.65V$  if  $V_{CC} \geq 6.65V$ . Maximum Input Voltage on Enable pin to be  $V_{CC}$  if  $V_{CC} \leq 6.65V$ .

## PIN FUNCTIONS

| Pin # | Name            | Description  |
|-------|-----------------|--|
| 1-5   | SOURCE          | This pin is the source of the internal power FET and the output terminal of the IC.  |
| 6     | N/C             | DO NOT CONNECT, The pin must be float.   |
| 7     | I-Limit         | A resistor between this pin and the Source pin sets the overload and short circuit current limit levels.   |
| 8     | Enable/Fault    | The Enable/Fault pin is a tri-state, bi-directional interface. It can be used to enable the output of the device by floating the pin, or disable the chip by pulling it to ground (using an open drain or open collector device). If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that the device is in thermal shutdown. |
| 9     | dv/dt           | The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over the period of 1.5ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.  |
| 10    | GND             | Negative Input Voltage to the Device. This is used as the internal reference for the IC.   |
| 11    | V <sub>CC</sub> | Positive input voltage to the device (Exposed Pad).  |

## TYPICAL PERFORMANCE CHARACTERISTICS

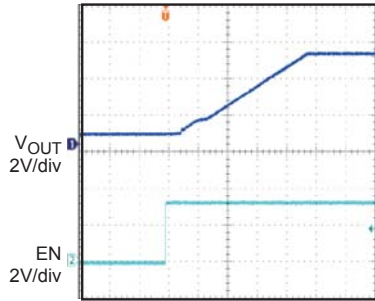
$V_{IN} = 5V$ ,  $V_{EN}=3.3V$ ,  $R_{LIMIT}=22\Omega$ ,  $C_{OUT}=10\mu F$ ,  $C_{dv}/dt = 1nF$ ,  $T_A=25^\circ C$ , unless otherwise noted.



**TYPICAL PERFORMANCE CHARACTERISTICS** *(continued)*

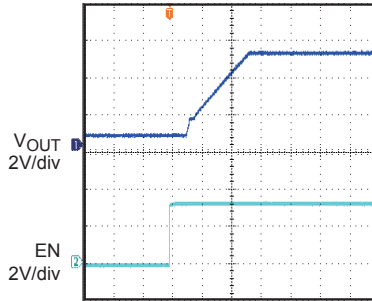
$V_{IN} = 5V$ ,  $V_{EN}=3.3V$ ,  $R_{LIMIT}=22\Omega$ ,  $C_{OUT}=10\mu F$ ,  $C_{dv/dt}=1nF$ ,  $T_A=25^\circ C$ , unless otherwise noted.

**Turn On Delay and Rise Time with 1uF Load, 1nF Cdv/dt**  
 $C_{out}=1\mu F$ , no load



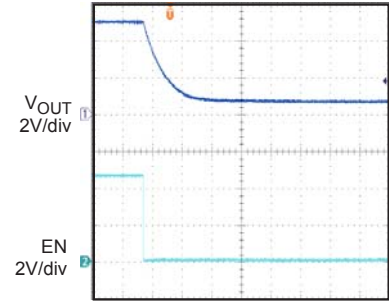
4ms/div

**Turn On Delay and Rise Time with 1uF Load, no Cdv/dt**  
 $C_{out}=1\mu F$ , no load



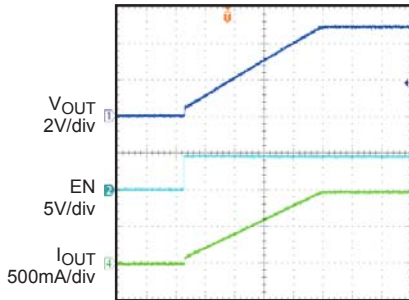
400µs/div

**Turn Off Delay and Fall Time with 10uF Load**  
 $C_{out}=10\mu F$ , no load



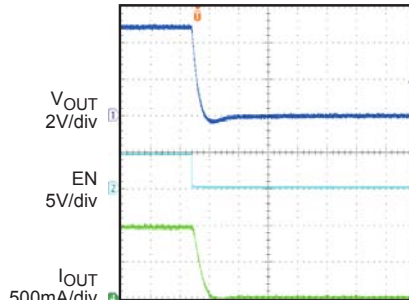
20ms/div

**Turn On Delay and Rise Time with 10uF Load**  
 $R_{load}=5\Omega$



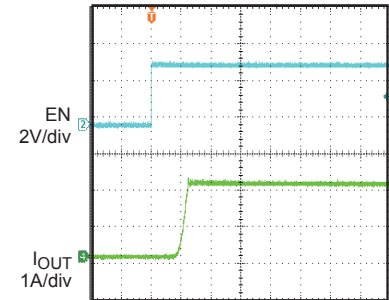
4ms/div

**Turn Off Delay and Fall Time with 10uF Load**  
 $R_{load}=5\Omega$



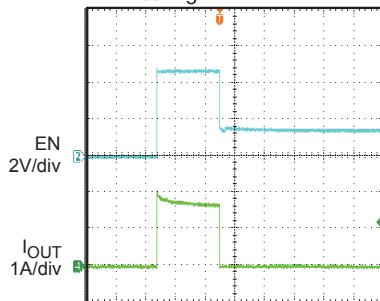
200µs/div

**Short Circuit Current, Device Enabled into Short**



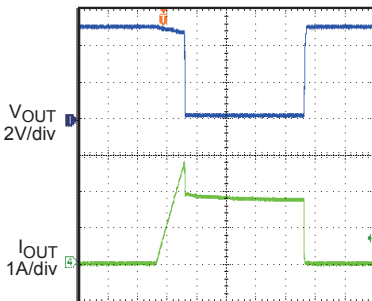
100µs/div

**Short Circuit Current, Device Enabled into Short, and Thermal Shut Down**  
 EN Floating



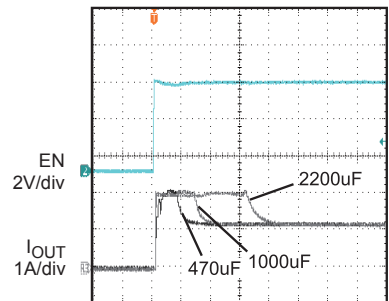
100ms/div

**Trip Current with Ramped Load on Enabled Device**



4ms/div

**Inrush Current with Different Load Capacitance**  
 $R_{load}=3.9\Omega$ , no Cdv/dt, EN Floating

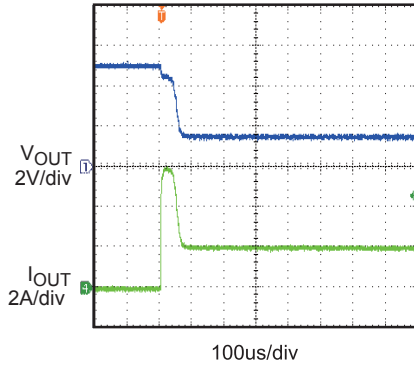


2ms/div

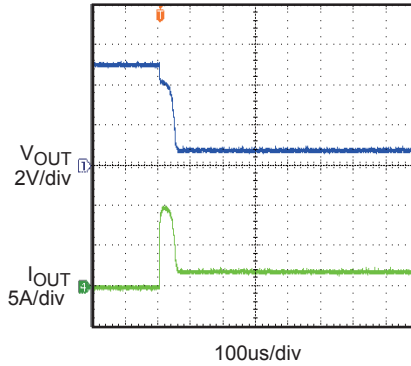
**TYPICAL PERFORMANCE CHARACTERISTICS** *(continued)*

$V_{IN} = 5V$ ,  $V_{EN}=3.3V$ ,  $R_{LIMIT}=22\Omega$ ,  $C_{OUT}=10\mu F$ ,  $C_{dv/dt}=1nF$ ,  $T_A=25^\circ C$ , unless otherwise noted.

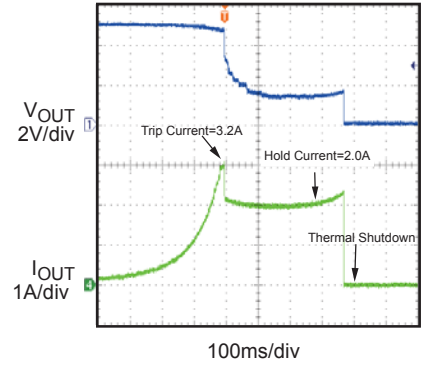
**0.66Ω Load Connected to Enabled Device**



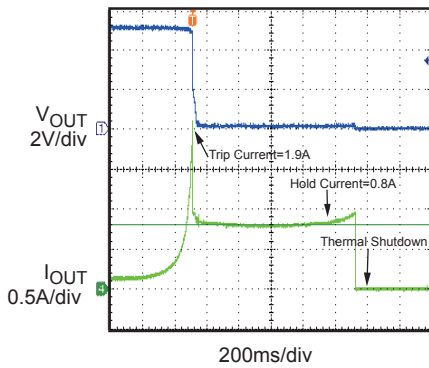
**0.33Ω Load Connected to Enabled Device**



**Current Limit**  
 $R_{LIMIT}=22\Omega$



**Current Limit**  
 $R_{LIMIT}=50\Omega$



BLOCK DIAGRAM

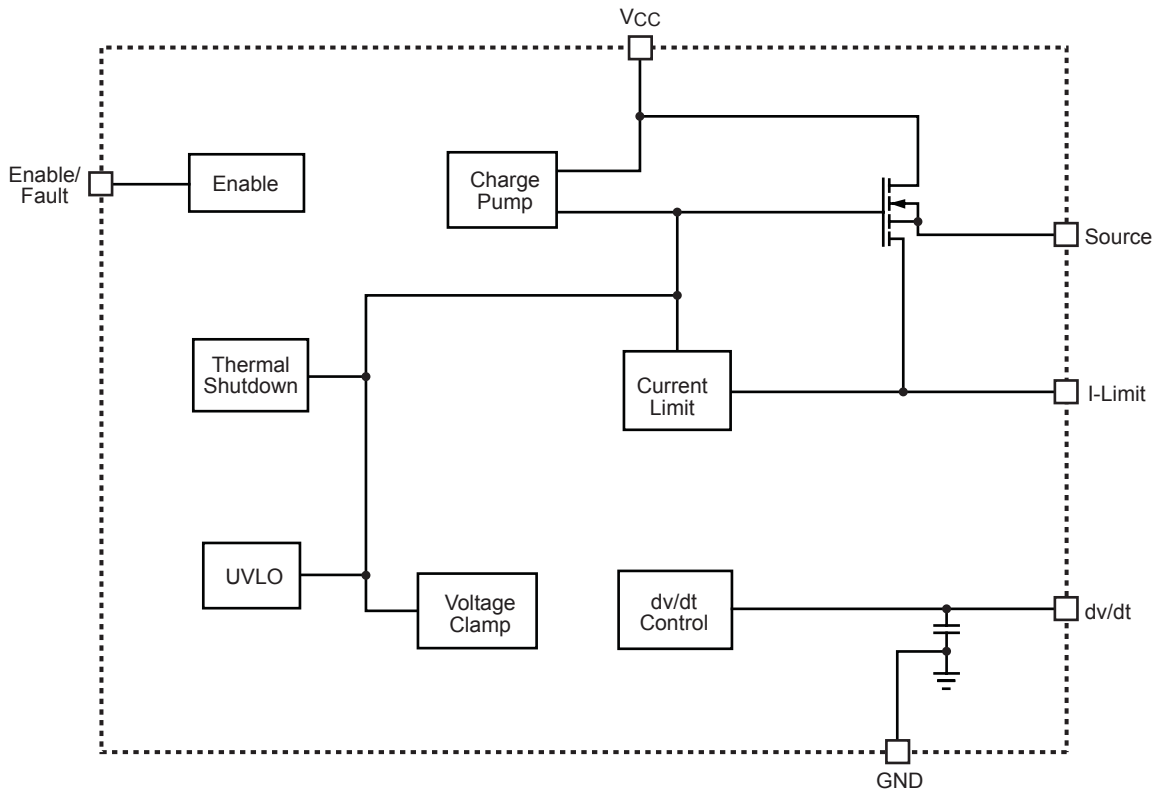


Figure 1—Functional Block Diagram



### Current Limit

The desired current limit is a function of the external current limit resistor.

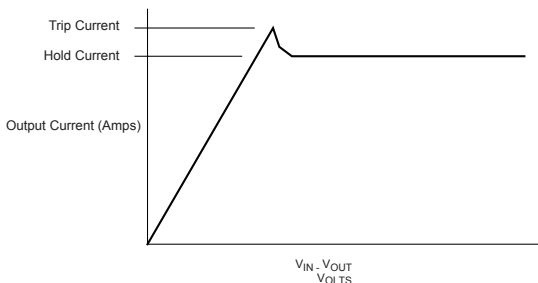
#### Current Limit vs. Current Limit Resistor ( $V_{CC}=5V$ )

| Current Limit Resistor ( $\Omega$ ) | 22  | 50  | 100 |
|-------------------------------------|-----|-----|-----|
| Trip Current (A)                    | 3.3 | 2.0 | 1.9 |
| Hold Current (A)                    | 2.1 | 0.9 | 0.6 |

The hold current refers to the current limit. However, the current limit is set to the “trip current” level when the output (source voltage) is near  $V_{CC}$ . As the output decreasing, the current limit is decreased to the “hold current” level.

In a typical application using a current limit resistor of  $22\Omega$ , the trip current will be 3.3A and the hold current will be 2.1A. If the device is in its normal operating state and passing 2.0A it will need to dissipate only 176mW with the very low on resistance of  $44m\Omega$ . For the package dissipation of  $50^\circ C/Watt$ , the temperature rise will only be  $+9^\circ C$ . Combined with a  $25^\circ C$  ambient, this is only  $34^\circ C$  total package temperature.

During a short circuit condition, the device now has 5V across it and the hold current clamps at 2.1A and therefore must dissipate 10.5W. At  $50^\circ C/watt$ , if uncontrolled, the temperature would rise above the MP5010 thermal protection ( $+175^\circ C$ ) and shutdown the device to cause the temperature to drop below a hysteresis level. Proper heat sink must be used if the device is intended to supply the hold current and not shutdown. Without a heat sink, hold current should be maintained below 600mA at  $+25^\circ C$  and below 360mA at  $+85^\circ C$  to prevent the device from activating the thermal shutdown feature.



### Rise Time

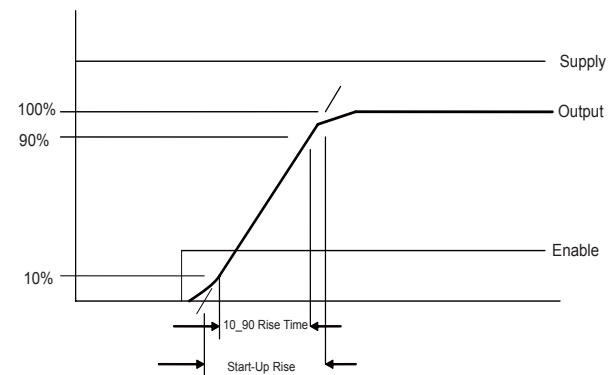
The rise time is a function of the capacitor ( $C_{dv/dt}$ ) on the  $dv/dt$  pin.

Rise Time vs.  $C_{dv/dt}$

$$\text{Rise Time} = K_{RT} * (50pF + C_{dv/dt}), K_{RT} = 28E6$$

| $C_{dv/dt}$              | none | 50pF | 500pF | 1nF  |
|--------------------------|------|------|-------|------|
| Rise Time (TYPICAL) (ms) | 1.4  | 2.8  | 15.4  | 29.4 |

The “start-up rise time” is measured by taking the 10% to 90% time and multiplied by 1.25 to get the “interpolated” 0% to 100% rise time.



### Fault and Enable Pin

The Enable/Fault Pin is a Bi-Directional three levels I/O with a weak pull up current (25uA typical). The three levels are low, mid and high. It functions to enable/disable the part and to relay Fault information.

Enable pin as an input:

1. Low and mid disable the part.
2. Low, in addition to disabling the part, clears the fault flag.
3. High enables the part (if the fault flag is clear).

Enable pin as an output:

1. The pull up current may (if not overridden) allow a “wired nor” pull up to enable the part.
2. An under voltage will cause a low on the enable pin, and will clear the fault flag.
3. A thermal fault will cause a mid level on the enable pin, and will set the fault flag.

The Enable/Fault line must be above the mid level for the output to be turned on.

The fault flag is an internal flip-flop that can be set or reset under various conditions:

1. Thermal Shutdown: set fault flag
2. Under Voltage: reset fault flag
3. Low voltage on Enable/Fault pin: reset fault flag
4. Mid voltage on Enable/Fault pin: no effect

Under a fault, the Enable/Fault pin is driven to the mid level.

There are 4 types of faults, and each fault has a direct and indirect effect on the Enable/Fault pin and the internal fault flag. In a typical application there are one or more of the MP5010 chips in a system. The Enable/Fault lines will typically be connected together.

#### Under Voltage Lock Out Operation

If the supply (input) is below the UVLO threshold, the output is disabled, and the fault line is driven low.

When the supply goes above the UVLO threshold, the output is enabled and the fault line is released. When the fault line is released it will be pulled high by a 25uA current source. No external pull up resistor is required. In addition, the pull up voltage is limited to 5 volts.

#### Thermal Protection

When thermal protection is triggered, the output is disabled and the fault line is driven to the mid level. The thermal fault condition is latched (meaning the fault flag is set), and the part will remain latched off until the fault (enable) line is brought low. Cycling the power below the UVLO threshold will also reset the fault flag.

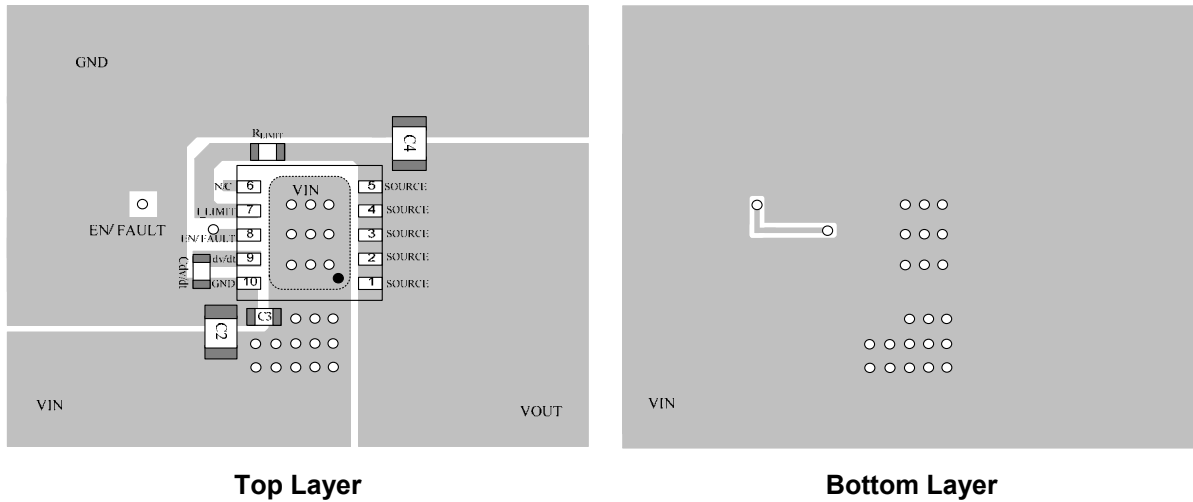
| Fault description  | Internal action   | Effect on Fault Pin                             | Effect on Flag | Effect on secondary Part                                    |
|--------------------|---|---|----------------|---|
| Short/over current | Limit current   | none  | none           | none  |
| Under Voltage      | Output is turned off  | Internally drives Enable/Fault pin to Logic low | Flag is reset  | Secondary part output is disabled, and fault flag is reset. |
| Over Voltage       | Limit output voltage  | None  | None           | None  |
| Thermal Shutdown   | Shutdown part. The part is latched off until a UVLO or externally driven to ground. | Internally drives Enable/Fault pin to mid level | Flag is Set    | Secondary part output is disabled.                          |

**PCB Layout**

PCB layout is very important to achieve stable operation. Please follow these guidelines and take below figure for reference.

Place R<sub>limit</sub> close to I<sub>limit</sub> pin, C<sub>dv/dt</sub> close to

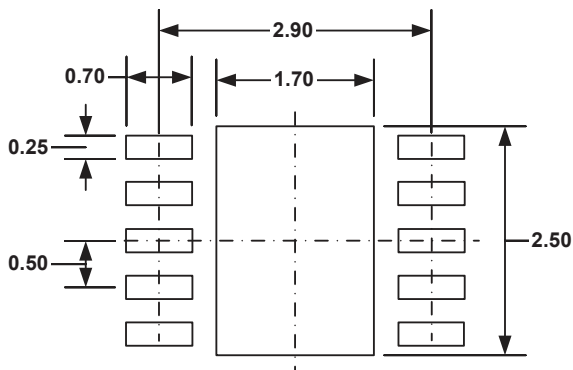
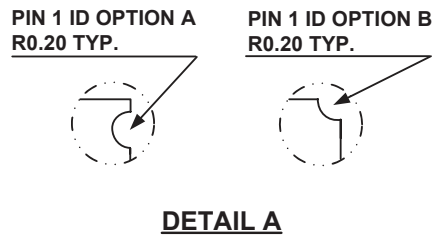
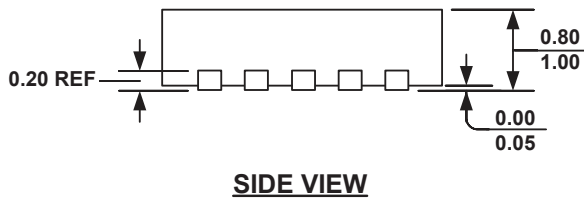
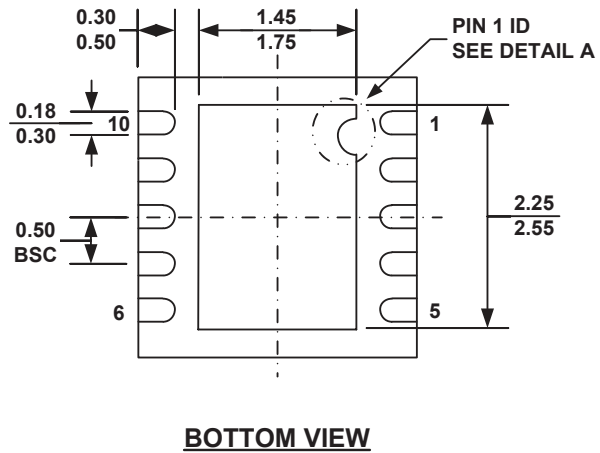
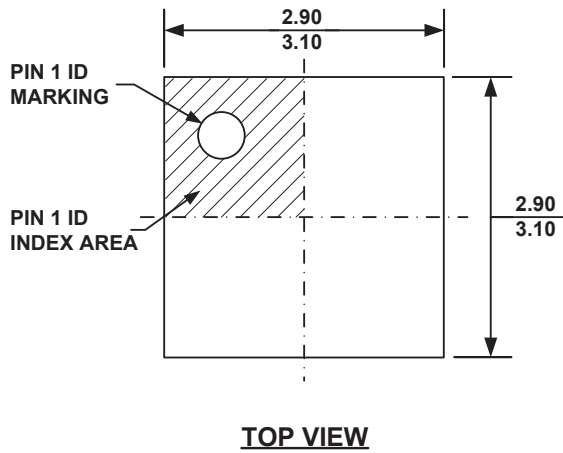
dv/dt pin and input cap close to V<sub>cc</sub> pin. Keep the N/C pin float. Put vias in thermal pad and ensure enough copper area near V<sub>cc</sub> and source to achieve better thermal performance.



**Figure 2—PCB Layout**

## PACKAGE INFORMATION

### QFN10 (3mm x 3mm)



#### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
- 5) DRAWING IS NOT TO SCALE.

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