IXYS

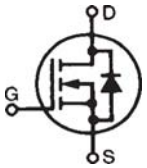
Preliminary Technical Information

High Voltage Power MOSFET

IXTF1N450

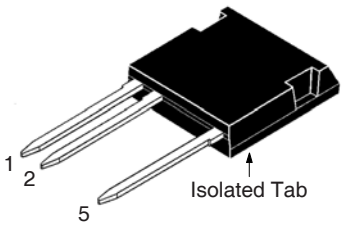
V_{DSS} = 4500V
I_{D25} = 0.9A
$R_{DS(on)}$ ≤ 95Ω

(Electrically Isolated Tab)



N-Channel Enhancement Mode

ISOPLUS i4-Pak™



1 = Gate 5 = Drain
2 = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	4500	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	4500	V
V_{GSS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	0.9	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	3.0	A
P_D	T_C = 25°C	165	W
T_J		- 55 ... +150	°C
T_{JM}		150	°C
T_{stg}		- 55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	Plastic Body for 10s	260	°C
F_C	Mounting Force	20..120 / 4.5..27	N/lb.
V_{ISOL}	50/60Hz, 1 Minute	4500	V~
Weight		6	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	3.5		6.0	V
I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
I_{DSS}	V_{DS} = 3.6kV, V_{GS} = 0V			10	μA
	V_{DS} = 4.5kV			50	μA
	V_{DS} = 3.6kV Note 2, T_J = 100°C		25		μA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 50mA, Note 1			95	Ω

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4500V~ Electrical Isolation
- Molding Epoxies meet UL 94 V-0 Flammability Classification

Advantages

- High Voltage Package
- Easy to Mount
- Space Savings
- High Power Density

Applications

- High Voltage Power Supplies
- Capacitor Discharge Applications
- Pulse Circuits
- Laser and X-Ray Generation Systems

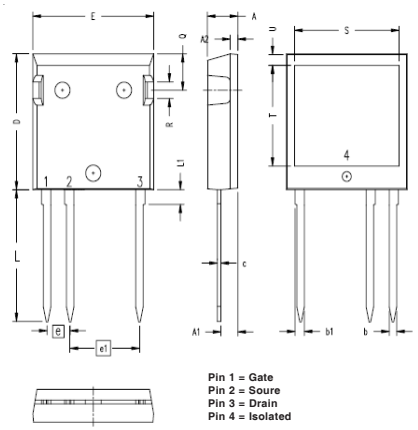
Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 50V, I_D = 200mA, Note 1	0.28	0.46		S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		1730		pF
C_{oss}			78		pF
C_{rss}			28		pF
R_{Gi}	Gate Input Resistance		21		Ω
$t_{d(on)}$	**Resistive Switching Times**		34		ns
t_r	V_{GS} = 10V, V_{DS} = 500V, I_D = 0.5A		60		ns
$t_{d(off)}$	R_G = 10Ω (External)		58		ns
t_f			127		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 1kV, I_D = 0.5A		40		nC
Q_{gs}			10		nC
Q_{gd}			20		nC
R_{thJC}				0.77	°C/W
R_{thCS}			0.15		°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			1	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			5	A
V_{SD}	I_F = 1A, V_{GS} = 0V, Note 1			2.0	V
t_{rr}	I_F = 1A, -di/dt = 50A/μs, V_R = 100V		1.75		μs

Notes: 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Part must be heatsunk for high-temp I_{DSS} measurement.

ISOPLUS i4-Pak™ (HV) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.085	1.17	2.16
b	.045	.055	1.14	1.40
b1	.058	.068	1.47	1.73
C	.020	.029	0.51	0.74
D	.819	.840	20.80	21.34
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.840	19.81	21.34
L1	.083	.102	2.11	2.59
Q	.210	.244	5.33	6.20
R	.100	.180	2.54	4.57
S	.660	.690	16.76	17.53
T	.590	.620	14.99	15.75
U	.065	.080	1.65	2.03

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ T_J = 25ºC

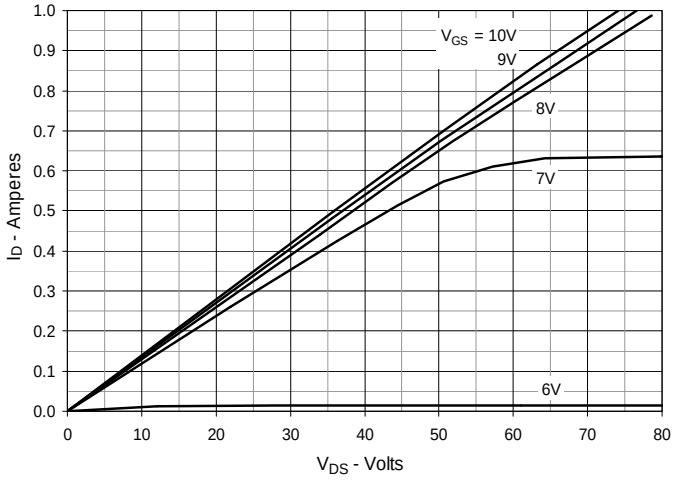


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

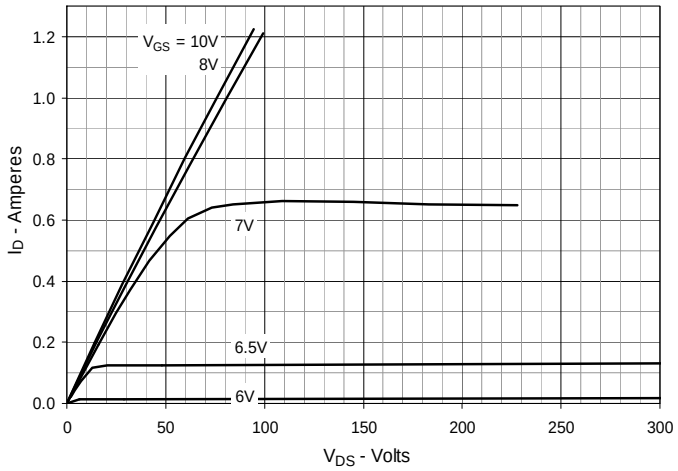


Fig. 3. Output Characteristics @ T_J = 125ºC

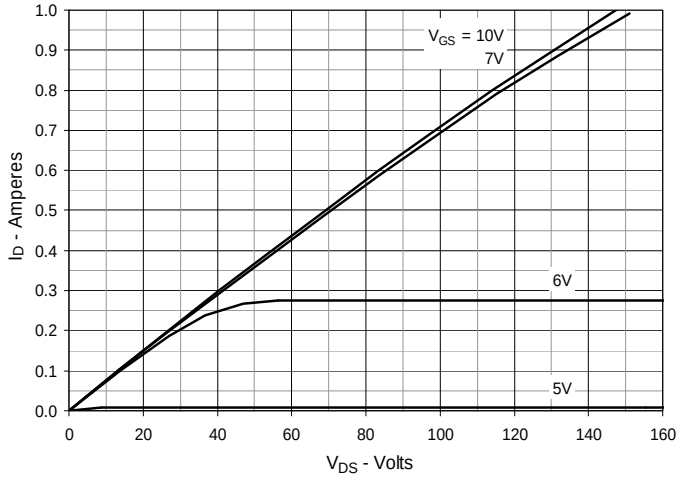


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 0.5A Value vs. Junction Temperature

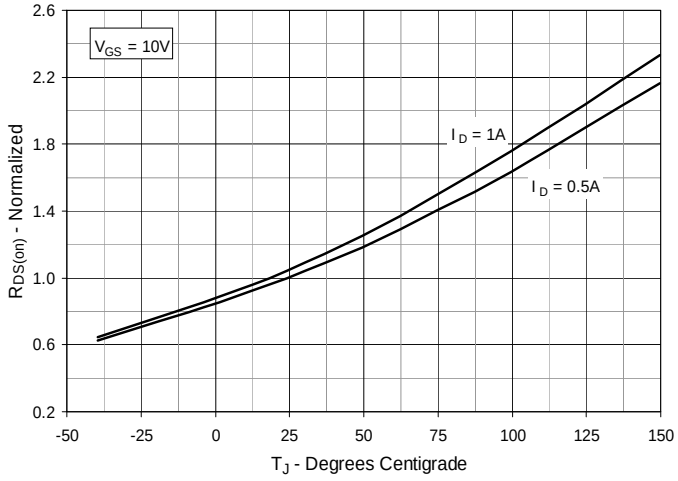


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 0.5A Value vs. Drain Current

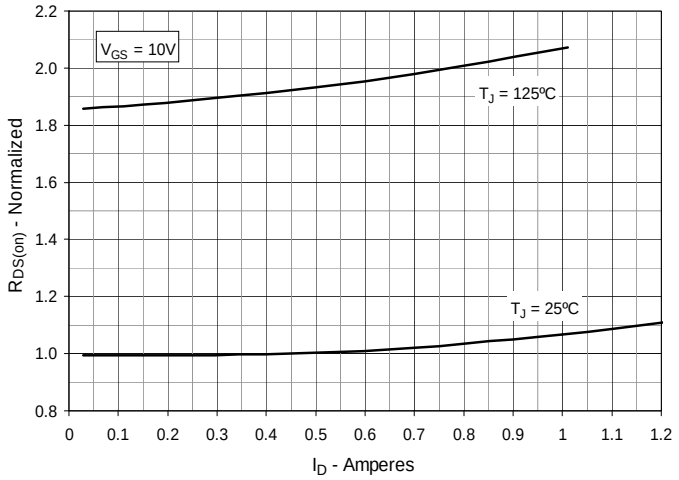


Fig. 6. Maximum Drain Current vs. Case Temperature

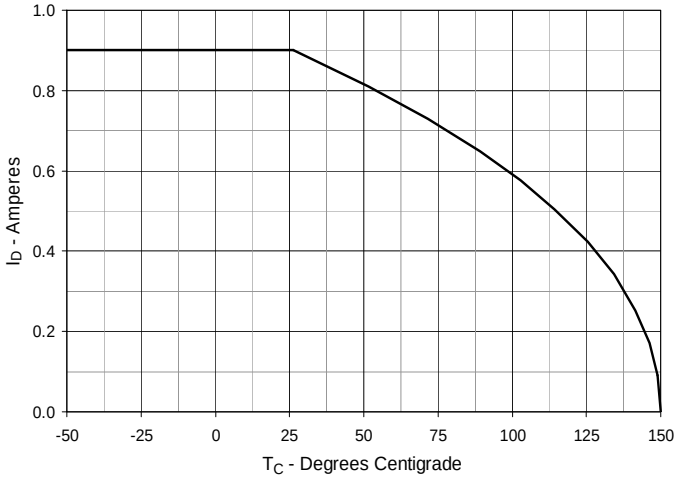


Fig. 7. Input Admittance

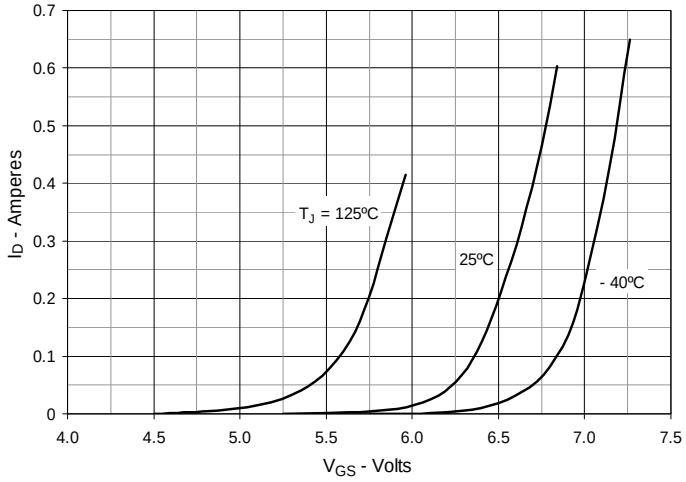


Fig. 8. Transconductance

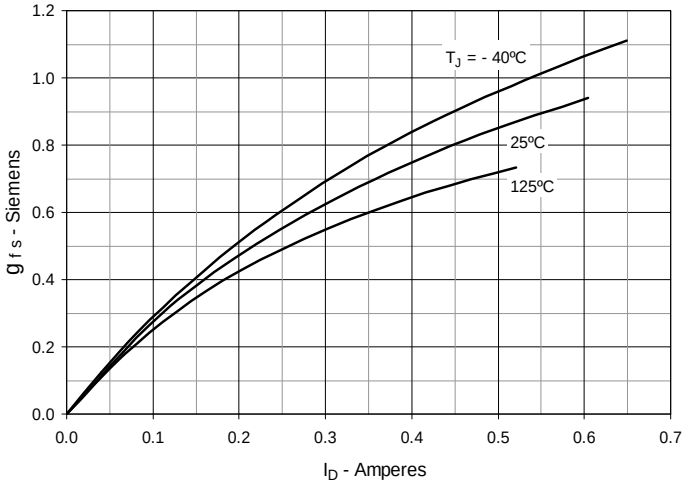


Fig. 9. Forward Voltage Drop of Intrinsic Diode

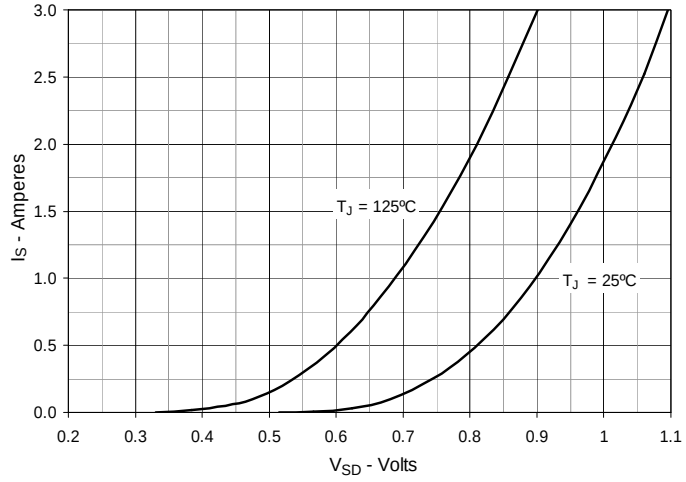


Fig. 10. Gate Charge

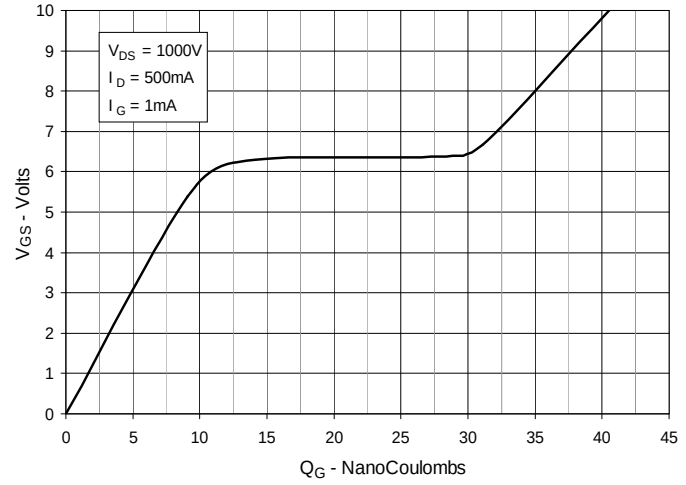


Fig. 11. Capacitance

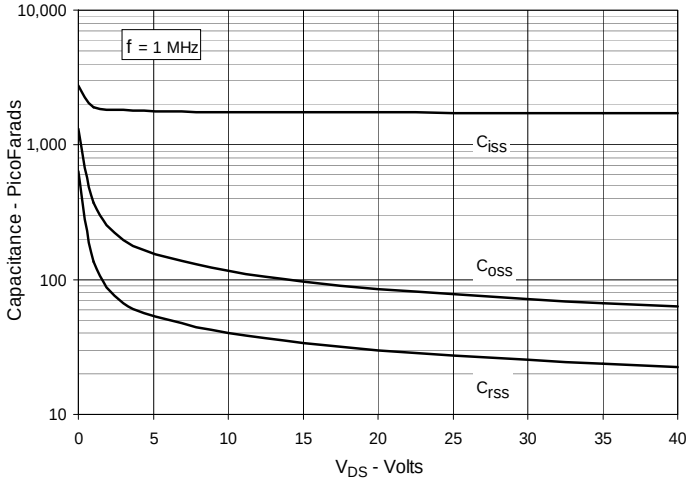


Fig. 12. Forward-Bias Safe Operating Area

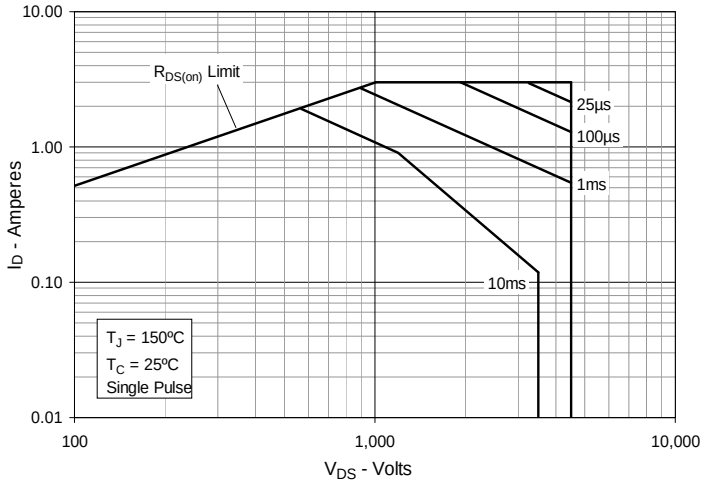


Fig. 13. Maximum Transient Thermal Impedance