Data Sheet | March 21, 2007 | FN6228.1

Dual, High Speed MOSFET Driver

The ISL55110 and ISL55111 are dual high speed mosfet drivers intended for applications requiring accurate pulse generation and buffering. Target applications include Ultrasound, CCD Imaging, Automotive Piezoelectric distance sensing and clock generation circuits.

With a wide output voltage range and low on resistance, these devices can drive a variety of resistive and capacitive loads with fast rise and fall times, allowing high speed operation with low skew as required in large CCD array imaging applications.

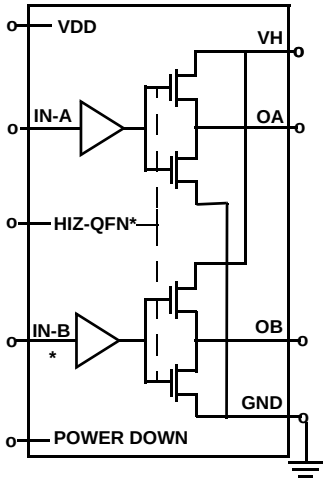
The ISL55110 and ISL55111 are compatible with 3.3V and 5V logic families and incorporate tightly controlled input thresholds to minimize the effect of input rise time on output pulse width. The ISL55110 has a pair of in-phase drivers while the ISL55111 has two drivers operating in antiphase. Both inputs of the device have independent inputs to allow external time phasing if required.

The ISL55110 has a power down mode for low power consumption during equipment standby times, making it ideal for portable products.

The ISL55110 and ISL55111 are available in 16 Ld Exposed pad QFN packaging and 8 Ld TSSOP. Both devices are specified for operation over the full -40°C to +85°C temperature range.

Functional Block Diagram

ISLI55110 and ISL55111 DUAL DRIVER



*** HIZ AVAILABLE IN QFN PACKAGE ONLY**

*** ISL55111 IN-B IS INVERTING**

Features

- 5V to 12V Pulse Magnitude
- High Current Drive 3.5A
- 6ns Minimum Pulse Width
- 1.5ns Rise and Fall Times, 100pF Load Time
- Low Skew
- 3.3V and 5V Logic Compatible
- In-Phase and Anti-Phase Outputs
- Small QFN and TSSOP Packaging
- Low Quiescent Current
- Pb-free Plus Anneal Available (RoHS compliant)

Applications

- Ultrasound Mosfet Driver
- CCD Array Horizontal Driver
- Automotive Piezo Driver Applications
- Clock Driver Circuits

Ordering Information

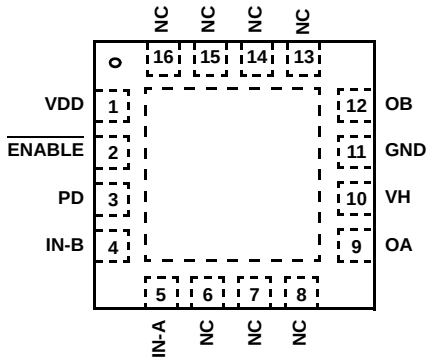
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL55110IRZ* (Note)	55 110IRZ	-40 to +85	16 Ld QFN (Pb-free)	L16.4x4A
ISL55110IVZ* (Note)	55110 IVZ	-40 to +85	8 Ld TSSOP (Pb-free)	M8.173
ISL55111IRZ* (Note)	55 11IRZ	-40 to +85	16 Ld QFN (Pb-free)	L16.4x4A
ISL55111IVZ* (Note)	55111 IVZ	-40 to +85	8 Ld TSSOP (Pb-free)	M8.173

*Add “-T” suffix for tape and reel.

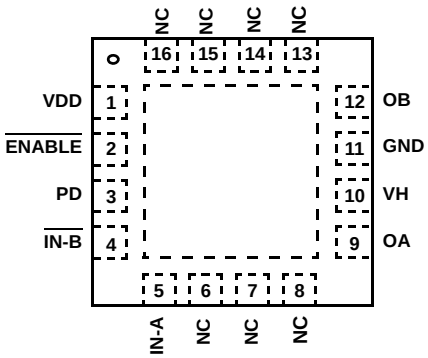
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

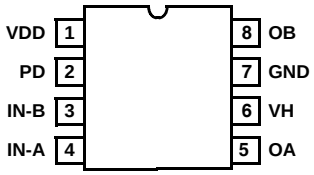
ISL55110
(16 LD QFN)
TOP VIEW



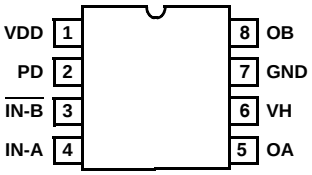
ISL55111
(16 LD QFN)
TOP VIEW



ISL55110
(8 LD TSSOP)
TOP VIEW



ISL55111
(8 LD TSSOP)
TOP VIEW



Pin Descriptions

PIN	FUNCTION
VDD	Logic Power.
VH	Driver High Rail Supply
GND	Ground, return for both VH rail and VDD Logic Supply.
PD	Power Down. Active Logic High places part in Power Down Mode.
$\overline{\text{ENABLE}}$	QFN Packages only. Provides high speed logic HIZ control of driver outputs while leaving device logic power on.
IN-A	Logic level input that drives OA to VH Rail or Ground. Not Inverted.
IN-B, $\overline{\text{INB}}$	Logic level input that drive OB to VH Rail or Ground. Not inverted on ISL55110, Inverted on ISL55111.
OA	Driver output related to IN-A.
OB	Driver output related to IN-B.

Absolute Maximum Ratings (T_A = +25°C)

VH+ to GND 14.0V
VDD to GND 6.5V
VIN_A, VIN_V, PDN, $\overline{\text{ENABLE}}$ . . . . . (GND-0.5V) to (VDD+0.5V)
OA, OB . . . . . (GND-0.5) to (VH+0.5V)
Maximum Peak Output Current . . . . . (300mA)
ESD HBM Rating 3KV

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
16 Ld (4x4) QFN Package (Note 2)	45
8 Ld TSSOP Package (Note 1)	140

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

Recommended Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
VH	Driver Supply Voltage		5	12	13.2	V
VDD	Logic Supply Voltage		2.7		5.5	V
T_A	Ambient Temperature		-40		+85	°C
T_J	Junction Temperature				+150	°C

DC Electrical Specifications

VH = +12V, VDD = 2.7V to 5.5V, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC CHARACTERISTICS						
VIX_LH	Logic Input Threshold - Low to High	I_{IH} = 1µA: VIN_A, VIN_B	1.32	1.42	1.52	V
VIX_HL	Logic Input Threshold - High to Low	I_{IL} = 1µA: VIN_A, VIN_B	1.12	1.22	1.32	V
VHYS	Logic Input Hysteresis	VIN_A,VIN_B		0.2		V
VIH	Logic Input High Threshold	PDN	2.0		VDD	V
VIL	Logic Input Low Threshold	PDN	0		0.8	V
VIH	Logic Input High Threshold	$\overline{\text{ENABLE}}$ - QFN only	2.0		VDD	V
VIL	Logic Input Low Threshold	$\overline{\text{ENABLE}}$ - QFN only	0		0.8	V
IIX_H	Input Current Logic High	VIN_A,VIN_B = VDD		10	20	nA
IIX_L	Input Current Logic Low	VIN_A, VIN_B = 0V		10	20	nA
II_H	Input Current Logic High	PDN = VDD		10	20	nA
II_L	Input Current Logic Low	PDN = 0V		10	15	nA
II_H	Input Current Logic High	$\overline{\text{ENABLE}}$ = VDD - QFN only			12	mA
II_L	Input Current Logic Low	$\overline{\text{ENABLE}}$ = 0V - QFN only	-25			nA

DC Electrical Specifications (Continued) VH = +12V, VDD = 2.7V to 5.5V, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER CHARACTERISTICS						
R_{DS}	Driver Output Resistance	OA, OB		3	6	Ω
I_{DC}	Driver Output DC current (>2s)			100		mA
I_{AC}	Peak Output Current	Design Intent verified via simulation.		3.5		A
VOH to VOL	Driver Output Swing Range	VH voltage to Ground	3		13.2	V
SUPPLY CURRENTS						
I_{DD}	Logic Supply Quiescent Current	PDN = Low		4.0	6.0	mA
I_{DD-PDN}	Logic Supply Power Down Current	PDN = High			12	µA
IH	Driver Supply Quiescent Current	PDN = Low, No resistive load D_{OUT}			15	µA
IH_PDN	Driver Supply Power Down Current	PDN = High			1	µA

AC Electrical Specifications VH = +12V, VDD = +3.6, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_R, t_F	Driver Rise/Fall Time	OA,OB: CL = No Load 10% to 90%, VOH-VOL = 12V 10% to 90%, VOH-VOL = 10V		 1.0 1.0		 ns ns
t_R, t_F	Driver Rise/Fall Time	OA, OB CL = 1nF 10% to 90%, VOH-VOL = 12V		6.7		ns
tpdR	Input to Output Propagation Delay	Figure 2, Load 100pF/1k		12.0		ns
tpdF	Input to Output Propagation Delay			9.3		ns
tpdR	Input to Output Propagation Delay	Figure 2, Load 220pF		12.5		ns
tpdF	Input to Output Propagation Delay			10.2		ns
tpdR	Input to Output Propagation Delay	Figure 2, Load 330pF		12.9		ns
tpdF	Input to Output Propagation Delay			10.6		ns
tpdR	Input to Output Propagation Delay	Figure 2, Load 680pF		14.1		ns
tpdF	Input to Output Propagation Delay			12.1		ns
tSkewR	Channel to Channel tpdR Spread with same loads both Channels	Figure 2, All Loads		<0.5		ns
tSkewF	Channel to Channel tpdF Spread with same loads both channels.	Figure 2, All Loads		<0.5		ns
FMAX	Maximum Operating Frequency		70			MHz
TMIN	Minimum Pulse Width		6			ns
PDEN*	Power-down to Power-on Time			0.7	1.0	ms
PDDIS*	Power-on to Power-down Time			1.4	1.6	ms
TEN*	ENABLE to $\overline{\text{ENABLE}}$ Time (HIZ Off)			0.3	0.7	ms
TDIS*	$\overline{\text{ENABLE}}$ to ENABLE TIme (HIZ On)			1.4	1.6	ms

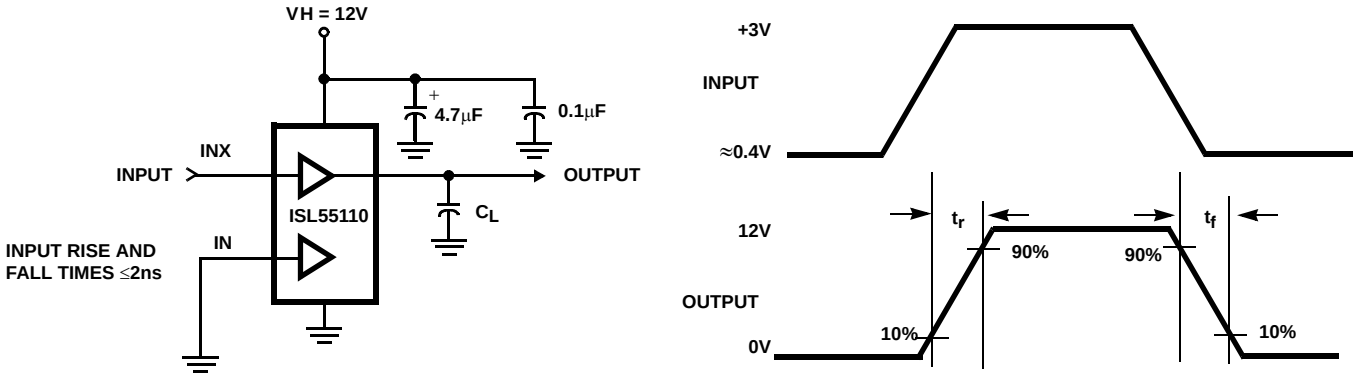
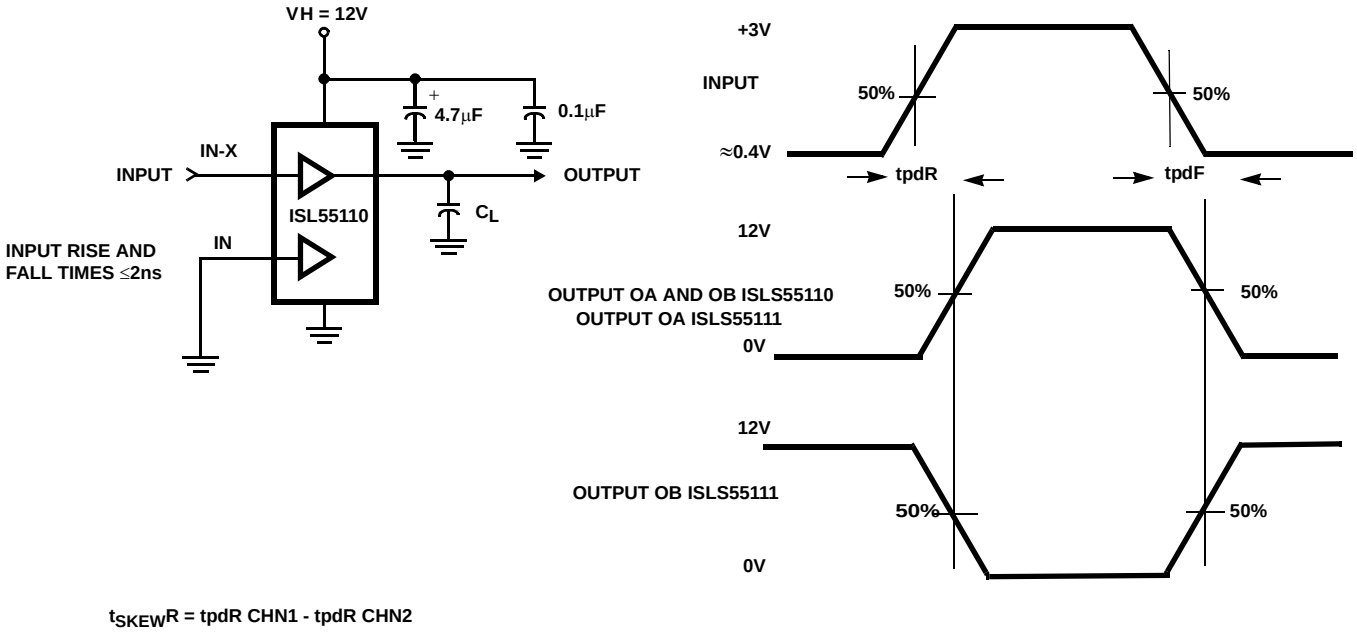


FIGURE 1. TEST CIRCUIT RISE (T_R)/FALL(T_F) THRESHOLDS



$t_{SKEW}R$ = tpdR CHN1 - tpdR CHN2

FIGURE 2. TEST CIRCUIT PROPAGATION TPD DELAY

Typical Performance Curves (See Typical Performance Curves Discussion)

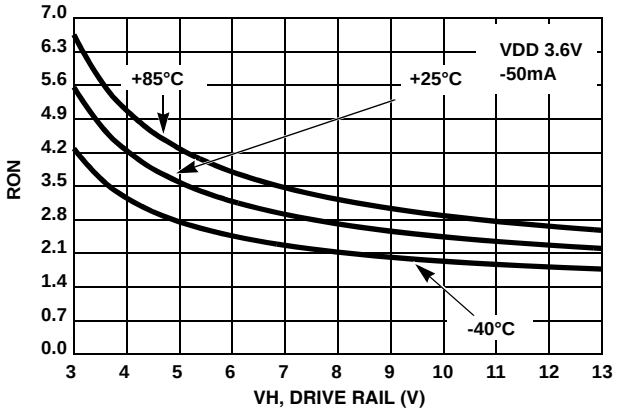


FIGURE 3. DRIVER RON vs VH SOURCE RESISTANCE

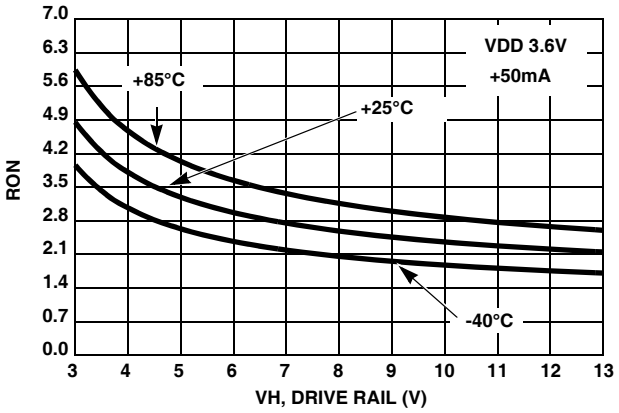


FIGURE 4. DRIVER RON vs VH SINK RESISTANCE

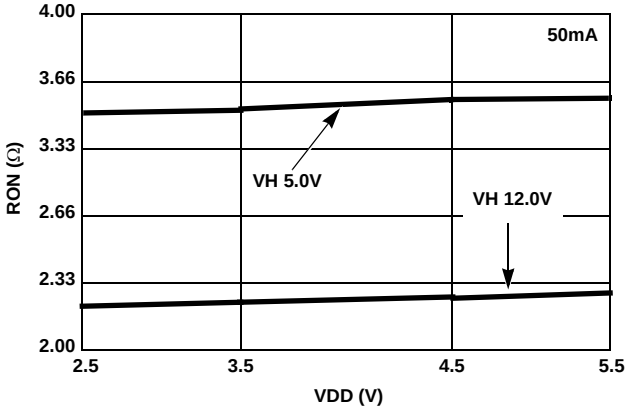


FIGURE 5. RON vs VDD SOURCE RESISTANCE

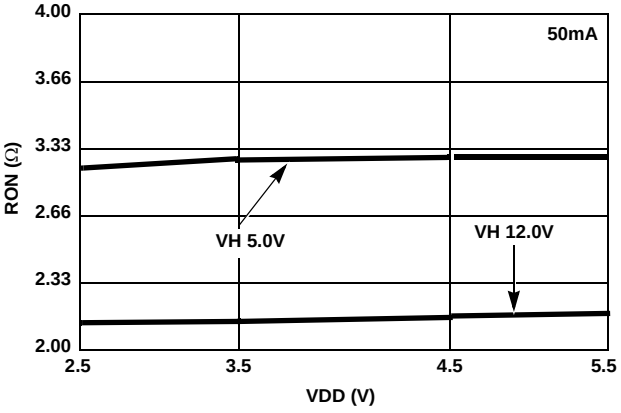


FIGURE 6. RON vs VDD SINK RESISTANCE

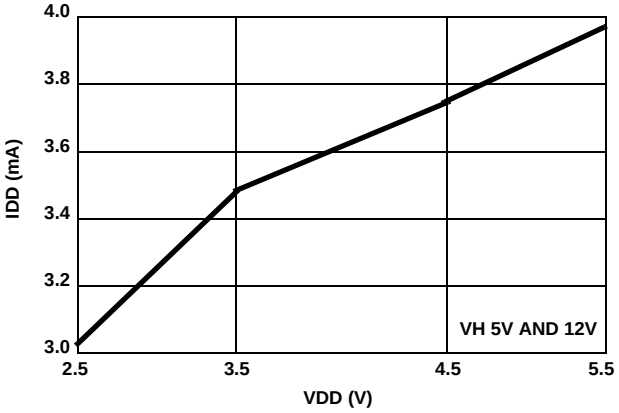


FIGURE 7. IDD vs VDD QUIESCENT CURRENT

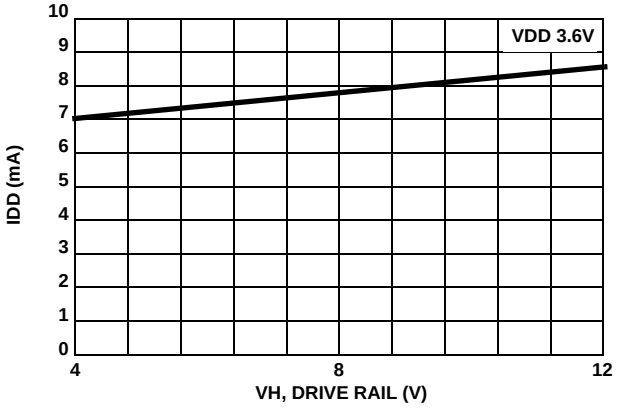


FIGURE 8. IDD vs VH @ 50MHz (NO LOAD)

Typical Performance Curves (Continued) (See Typical Performance Curves Discussion)

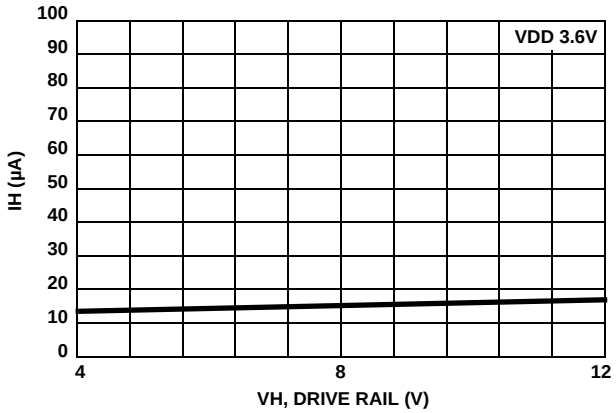


FIGURE 9. QUIESCENT IH vs VH

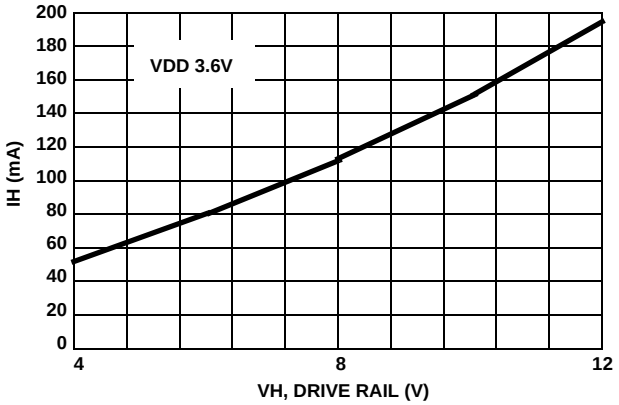


FIGURE 10. IH vs VH @ 50MHz (NO LOAD)

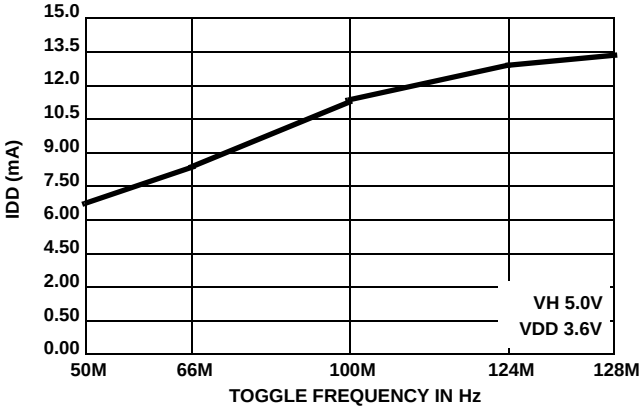


FIGURE 11. IDD vs FREQUENCY (DUAL CHANNEL, NO LOAD)L

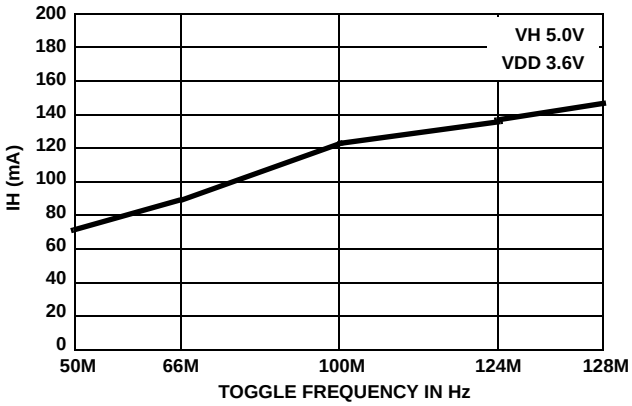


FIGURE 12. IH vs FREQUENCY (DUAL CHANNEL, NO LOAD)

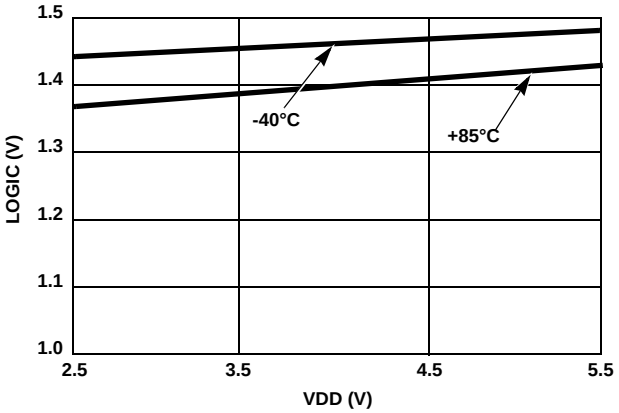


FIGURE 13. VIH LOGIC THRESHOLDS

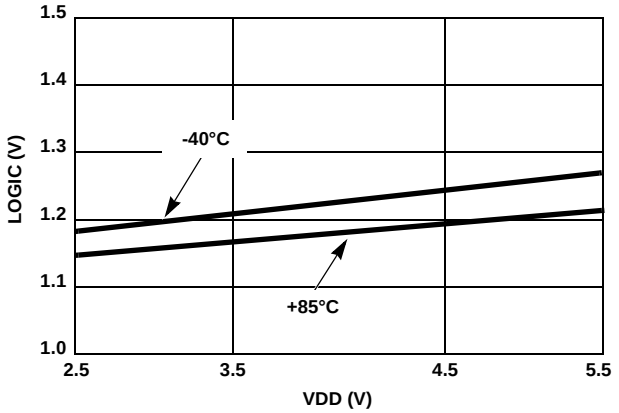


FIGURE 14. VIL LOGIC THRESHOLDS

Typical Performance Curves (Continued) (See Typical Performance Curves Discussion)

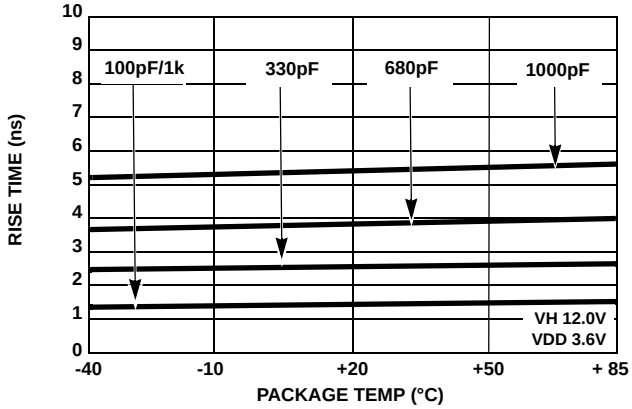


FIGURE 15. t_r vs TEMPERATURE

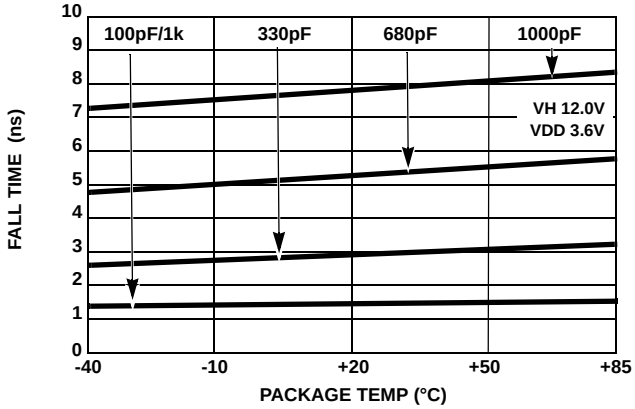


FIGURE 16. t_f vs TEMPERATURE

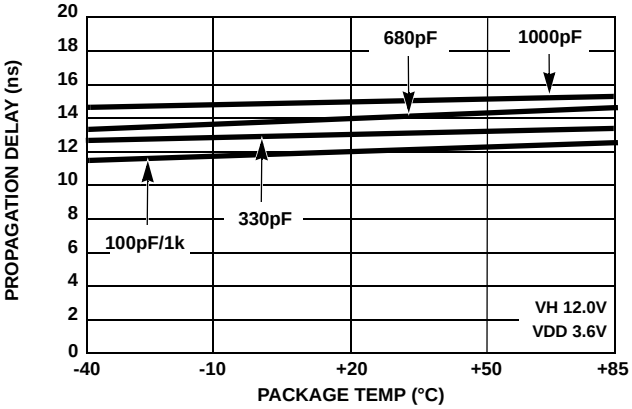


FIGURE 17. tpd_r vs TEMPERATURE

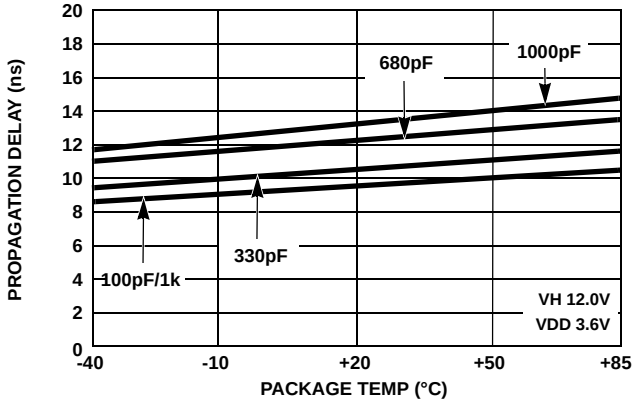


FIGURE 18. tpd_f vs TEMPERATURE

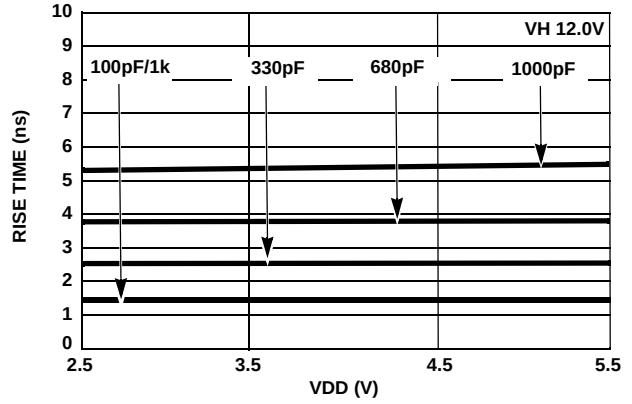


FIGURE 19. t_r vs VDD

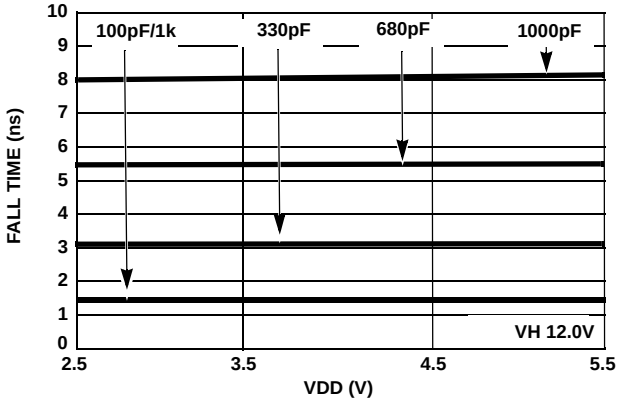


FIGURE 20. t_f vs VDD

Typical Performance Curves (Continued) (See Typical Performance Curves Discussion)

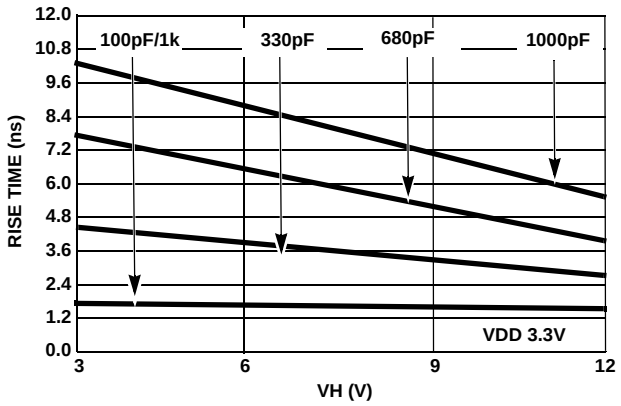


FIGURE 21. t_r vs VH

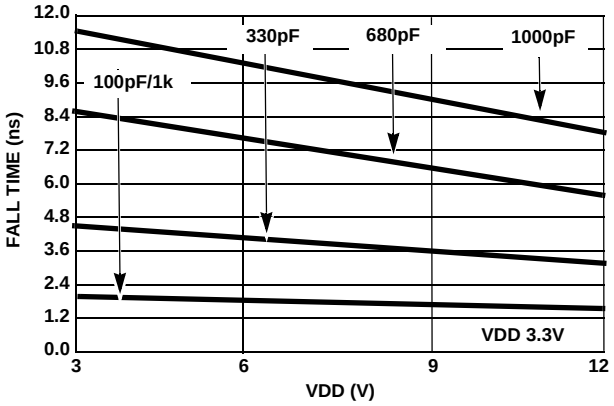


FIGURE 22. t_f vs VH

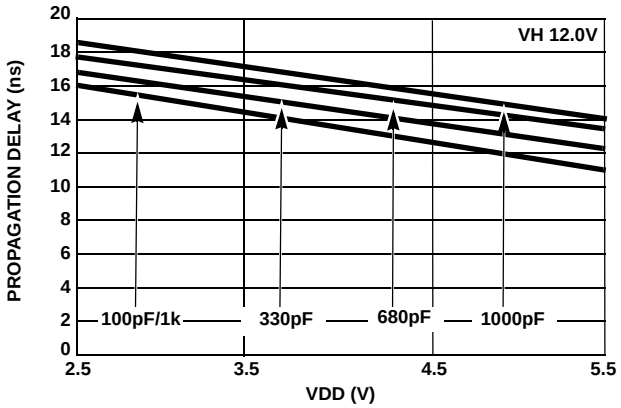


FIGURE 23. tpd_r vs VDD

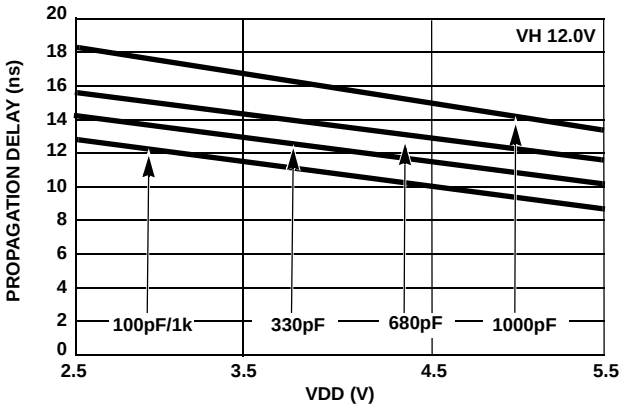


FIGURE 24. tpd_f vs VDD

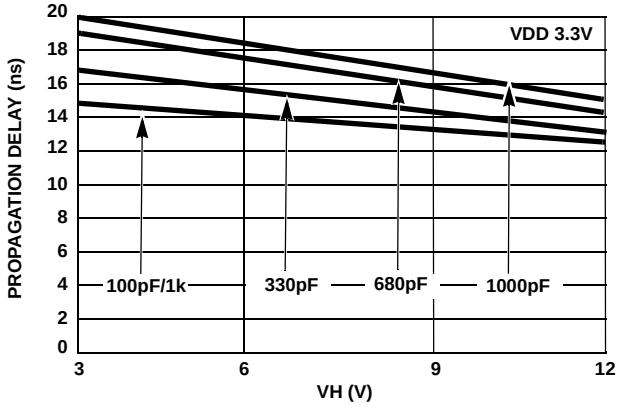


FIGURE 25. tpd_r vs VH

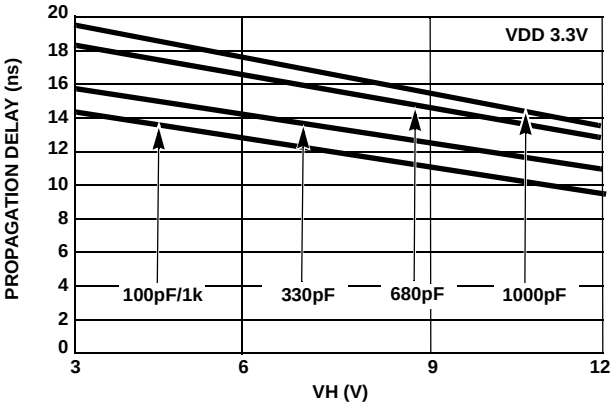


FIGURE 26. tpd_f vs VH

Typical Performance Curves (Continued) (See Typical Performance Curves Discussion)

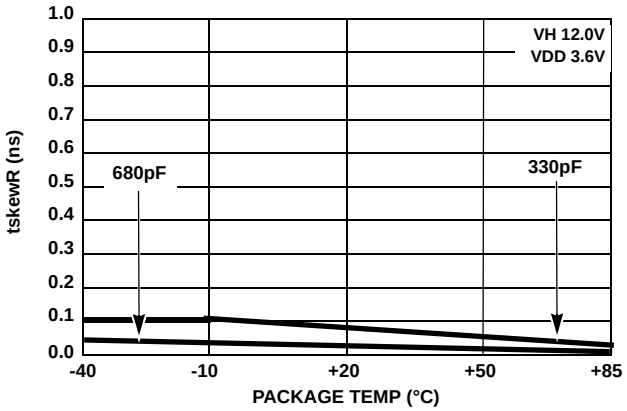


FIGURE 27. $tskew_r$ vs TEMPERATURE

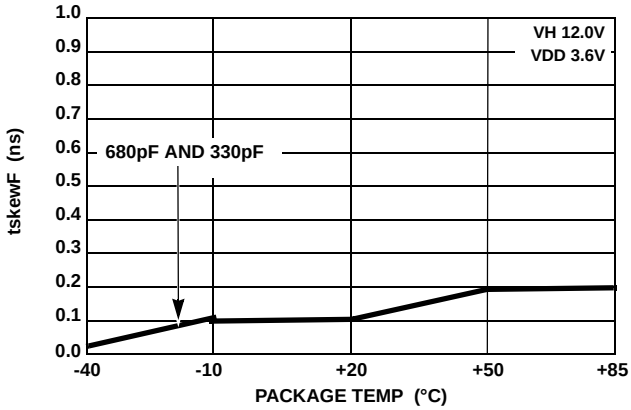


FIGURE 28. $tskew_f$ vs TEMPERATURE

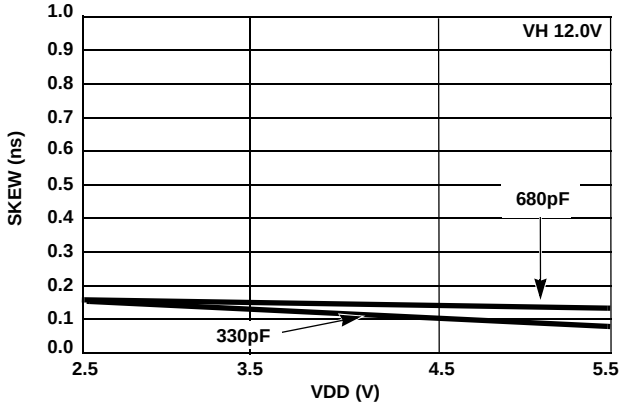


FIGURE 29. $tskew_r$ vs VDD

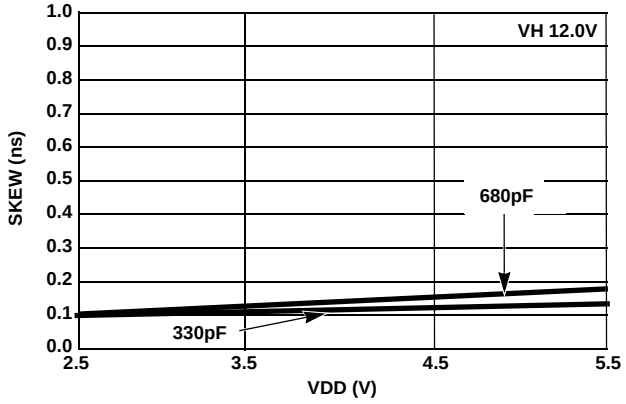


FIGURE 30. $tskew_f$ vs VDD

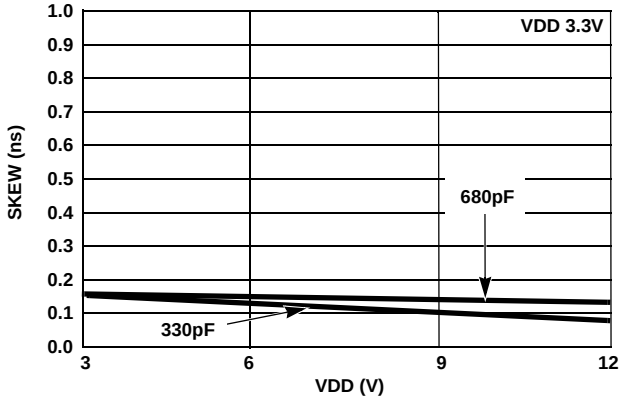


FIGURE 31. $tskew_r$ vs VH

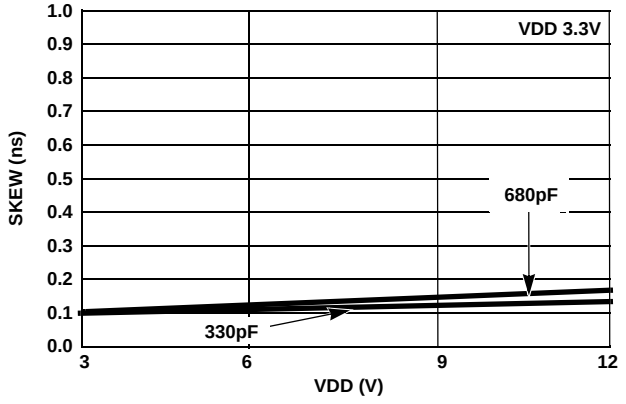


FIGURE 32. $tskew_f$ vs VH

Typical Performance Curves Discussion

RON

RON Source tested by placing device in Constant Drive High Condition and connecting -50mA constant current source to the Driver Output. Voltage Drop measured from VH to Driver Output for RON calculations.

RON Sink tested by placing device in Constant Driver Low Condition and connecting a +50mA constant current source. Voltage Drop from Driver Out to Ground measured for RON Calculations.

Dynamic Tests

All dynamic tests are conducted with ISL55110, ISL55111 Evaluation Board(s). Driver Loads are soldered to the Evaluation board. Measurements are collected with P6245 Active Fet Probes and TDS5104 Oscilloscope. Pulse Stimulus is provided by HP8131 pulse generator.

The ISL55110, ISL55111 Evaluation Boards provide Test Point Fields for leadless connection to either an Active Fet Probe or Differential probe. TP-IN fields are used for monitoring pulse input stimulus. TP-OA/B monitor Driver Output waveforms. C6 and C7 are the usual placement for Driver loads. R3 and R4 are not populated and provided for User-Specified, more complex load characterization.

Pin Skew

Pin Skew measurements are based on the difference in propagation delay of the two channels. Measurements are made on each channel from the 50% point on the stimulus point to the 50% point on the driver output. The difference in the propagation delay for Channel A and Channel B is considered to be Skew.

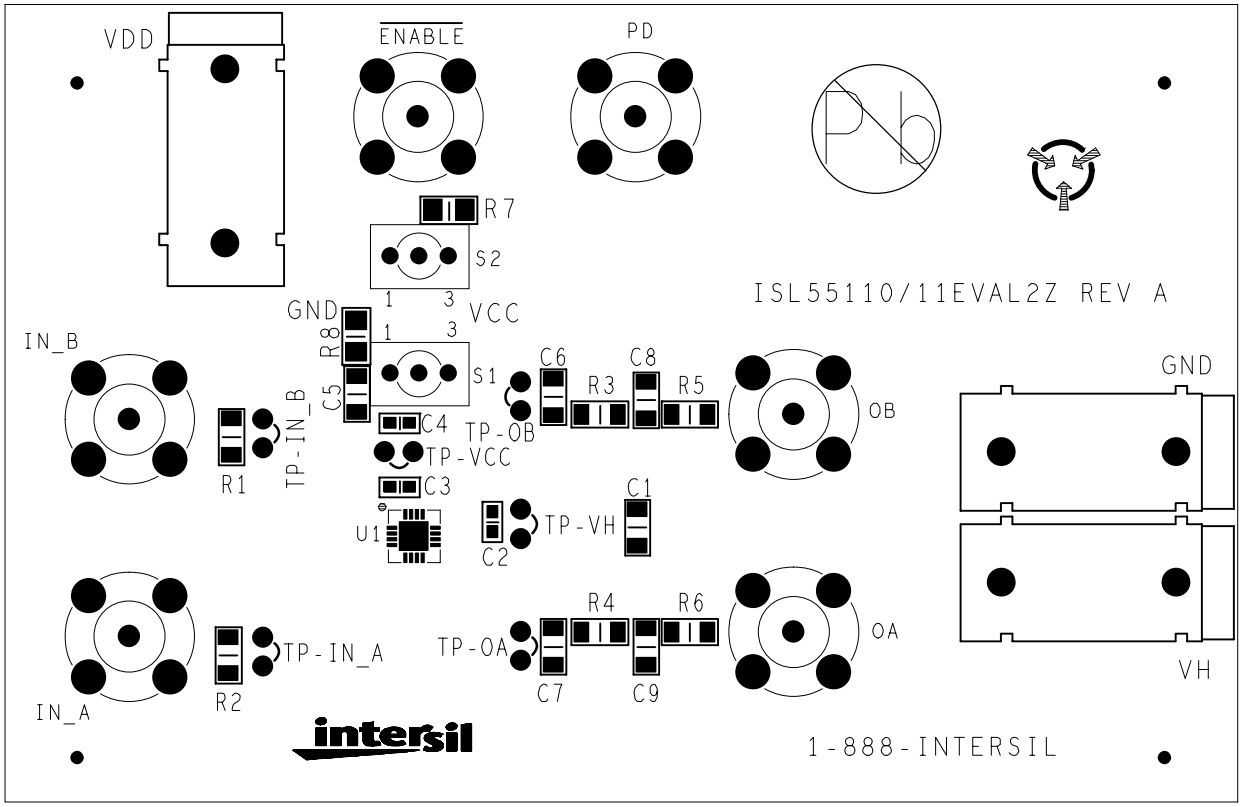
Both Rising Propagation Delay and Falling Propagation Delay are measured and reports as tSkewR and tSkewF.

50MHz Tests

50MHz Tests reported as No Load actually include Evaluation board parasitics and a single TEK 6545 fet probe. However no driver load components are installed, C6 through C9 and R3 through R6 are not populated.

General

Most dynamic measurements are presented in three ways. First over temperature with a VDD of 3.6V and VH of 12.0V. Second, at ambient with VH set to 12V and VDD data points of 2.5V, 3.5V, 4.5V and 5.50V. Third, the ambient tests are repeated with VDD of 3.3V and VH data points of 3V, 6V, 9V and 12V.



Detailed Description

The ISL55110 and ISL55111 are Dual High Speed Mosfet Drivers intended for applications requiring accurate pulse generation and buffering. Target applications include Ultrasound, CCD Imaging, Automotive Piezoelectric distance sensing and clock generation circuits.

With a wide output voltage range and low On Resistance, these devices can drive a variety of resistive and capacitive loads with fast rise and fall times, allowing high speed operation with low skew as required in large CCD array imaging applications.

The ISL55110 and ISL55111 are compatible with 3.3V and 5V logic families and incorporate tightly controlled input thresholds to minimize the effect of input rise time on output pulse width. The ISL55110 has a pair of in-phase drivers while the ISL55111 two drivers operating in antiphase. Both inputs of the device have independent inputs to allow external time phasing if required.

In addition to power MOS drivers, the ISL55110, ISL55111 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

Input Stage

The input stage is a high impedance input with rise/fall hysteresis. This means that the inputs will be directly compatible with both TTL and lower voltage logic over the entire VDD range. The user should treat the inputs as high speed pins and keep rise and fall times to <2ns.

Output Stage

The ISL55110, ISL55111 output is a high-power CMOS driver, swinging between ground and VH. At VH = 12V, the output impedance of the inverter is typically 3.0Ω. The high peak current capability of the ISL55110, ISL55111 enables it to drive a 330pF load to 12V with a rise time of <3.0ns over the full temperature range. The output swing of the ISL55110, ISL55111 comes within < 30mV of the VH and Ground rails.

Application Notes

Although the ISL55110, ISL55111 is simply a dual level-shifting driver, there are several areas to which careful attention must be paid.

Grounding

Since the input and the high current output current paths both include the ground pin, it is very important to minimize and common impedance in the ground return. Since the ISL55111 has one inverting input, any common impedance will generate negative feedback, and may degrade the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ISL55110, ISL55111 as is possible.

Bypassing

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A 4.7μF tantalum capacitor in parallel with a low inductance 0.1μF capacitor is usually sufficient bypassing.

Output Damping

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

1. Reduce inductance by making printed circuit board traces as short as possible.
2. Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
3. Use small damping resistor in series with the output of the ISL55110, ISL55111. Although this reduces ringing, it will also slightly increase the rise and fall times.
4. Use good by passing techniques to prevent supply voltage ringing.

Power Dissipation Calculation

The Power dissipation equation has three components: Quiescent Power Dissipation, Power dissipation due to Internal Parasitics and Power Dissipation because of the Load Capacitor.

Power dissipation due to internal parasitics is usually the most difficult to accurately quantitize. This is primarily due to Crow-Bar current which is a product of both the high and low drivers conducting effectively at the same time during driver transitions. Design goals always target the minimum time for this condition to exist. Given that how often this occurs is a product of frequency, Crowbar effects can be characterized as internal capacitance.

Lab tests are conducted with Driver Outputs disconnected from any load. With design verification packaging, bond wires are removed to aid in the characterization process. Base on laboratory tests and simulation correlation of those results, the following equation defines the ISL55110, ISL55111 Power Dissipation per channel:

P = VDD*3.3e-3 + 10pF*VDD^2*f + 135pF*VH^2*f + CL*VH^2*f (Watts/Channel)

Where:

1. 3.3mA is the quiescent Current from the VDD. This forms a small portion of the total calculation. When figuring two channel power consumption, only include this current once.

2. 10pF is the approximate parasitic Capacitor (Inverters, etc.), which the VDD drives

3. 135pF is the approximate parasitic at the DOUT and its Buffers. This includes the effect of the Crow-bar Current.

4. CL is the Load capacitor being driven

Power Dissipation Discussion

Specifying continuous pulse rates, driver loads and driver level amplitudes are key in determining power supply requirements as well as dissipation / cooling necessities. Driver Output patterns also impact these needs. The faster the pin activity, the greater the need to supply current and remove heat.

As detailed in the Power Dissipation Calculation Section, Power Dissipation of the device is calculated by taking the DC current of the VDD (logic) and VH Current (Driver rail) times the respective voltages and adding the product of both calculations. The average DC current measurements of IDD and IH should be done while running the device with the planned VDD and VH levels and driving the required pulse activity of both channels at the desired operating frequency and driver loads.

Therefore the user must address power dissipation relative to the planned operating conditions. Even with a device mounted per Note 1 or 2 under Thermal Information, given the high speed pulse rate and amplitude capability of the ISL55110, ISL55111, it is possible to exceed the +150°C “absolute-maximum junction temperature”. Therefore, it is important to calculate the maximum junction temperature for the application to determine if operating conditions need to be modified for the device to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads. Power also depends on number of channels changing state and frequency of operation. The extent of continuous active pulse generation will greatly effect dissipation requirements.

The user should evaluate various heat sink/cooling options in order to control the ambient temperature part of the equation. This is especially true if the user’s applications require continuous, high speed operation. A review of the Theta-j ratings of the TSSOP and QFN package clearly show the QFN package to have better thermal characteristics.

The reader is cautioned against assuming a calculated level of thermal performance in actual applications. A careful inspection of conditions in your application should be conducted. Great care must be taken to ensure Die Temperature does not exceed 150°C Absolute Maximum Thermal Limits.

Important Note: The ISL55110, ISL55111 QFN package metal plane is used for heat sinking of the device. It is electrically connected to the negative supply potential ground.

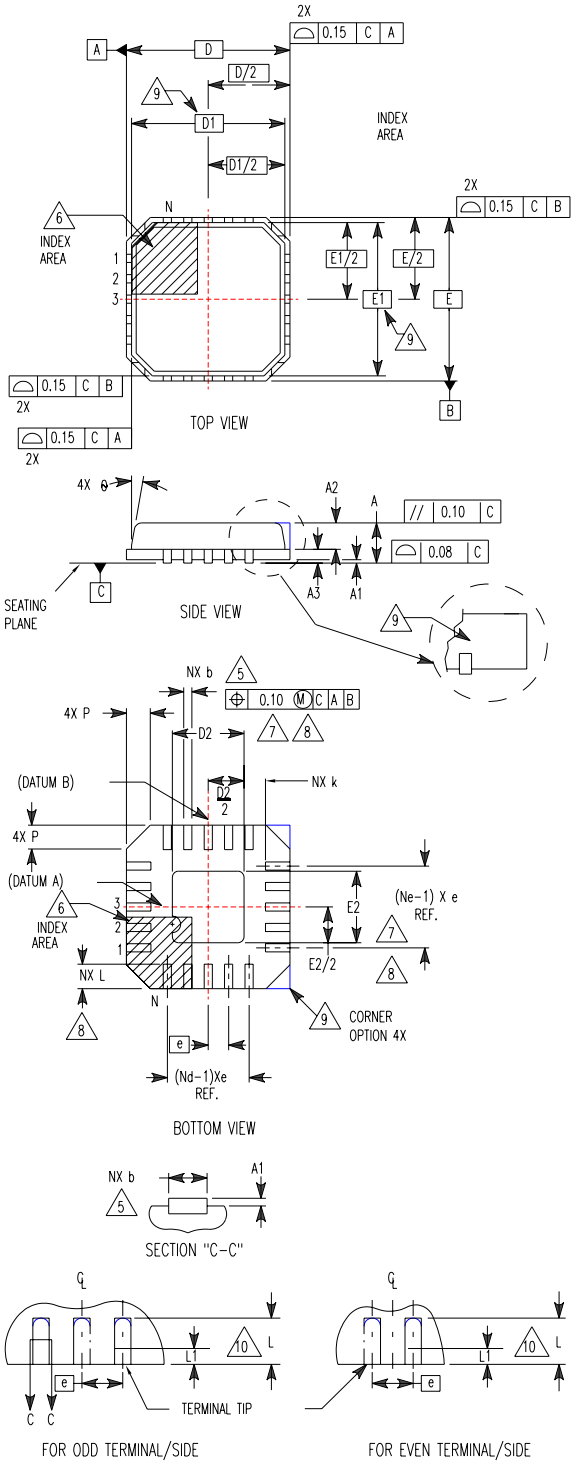
Power Supply Sequencing

The ISL55110, ISL55111 references both VDD and the VH driver supplies with respect to Ground. Therefore apply VDD, then VH. Digital Inputs should never be open. Do not apply slow analog ramps to the inputs. Again place decoupling as close to the package as possible for both VDD and especially VH.

Special Loading

With most applications the user will usually have a special load requirement. Please contact Intersil for Evaluation Boards or to request a device characterization to your requirements in our lab.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4A

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGD-10)

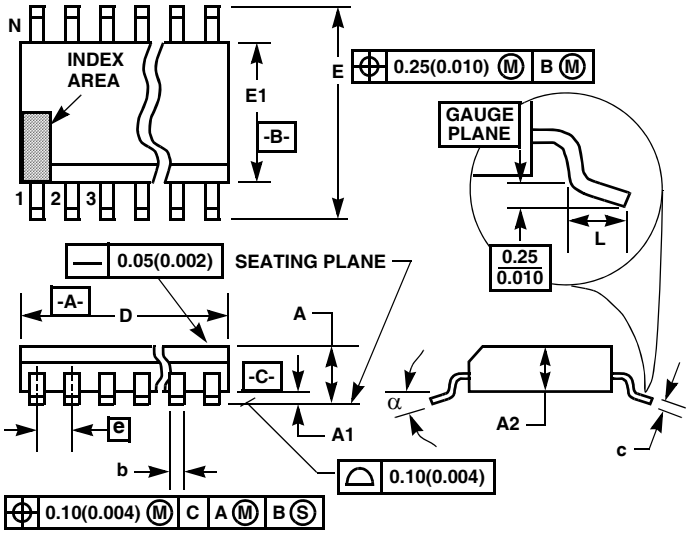
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.25	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	2.30	2.40	2.55	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	2.30	2.40	2.55	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 2 3/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M8.173

8 LEAD THIN SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

Rev. 1 12/00